TESI DI DOTTORATO

UNIVERSITÀ DEGLI STUDI DI NAPOLI "FEDERICO II"

DIPARTIMENTO DI INGEGNERIA ELETTRICA
E DELLE TECNOLOGIE DELL'INFORMAZIONE

DOTTORATO DI RICERCA IN
INGEGNERIA ELETTRONICA E DELLE TELECOMUNICAZIONI

DYNAMIC THERMAL FEEDBACK BLOCKS FOR ELECTROTHERMAL SIMULATION OF DEVICES, CIRCUITS AND SYSTEMS

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A. A. 2014–2015

“Ai miei nonni ”

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Chapter 1

Introduction

1.1 Why is electrothermal simulation important?

The effects of heating are various and affect the performance – speed and power dissipation – as well as the functionality, reliability and lifetime of electronic devices, circuits and systems. The behavior of electronic systems can be correctly modeled only by self-consistently solving the thermal and electrical problems in a coupled electrothermal (ET) simulation.

This is crucial for modern design due to [1, 2]:

- aggressive scaling, leading increase in power density;
- the use of advanced materials with low thermal conductivity;
- the adoption of insulation schemes (e.g., trench-based).

ET effects can significantly change the electronic system behavior in profound and a-priori unpredictable ways since *introduce a nonlinear feedback* in the devices operation, which is inherently nonlinear in itself. This feedback is caused by the fact that currents are determined by the voltage and temperatures – but temperature is determined by dissipated power, which is given by the product of voltage and current. By introducing a non-linear feedback loop:

- the whole system may become *destructively unstable*, leading to an unbounded increase of current and temperature (e.g., current hogging [3]);
- non-destructive *instabilities and oscillations* can occur, as described, e.g., in [4–6]. ET effects will often in these cases lead to a reduction in Safe Operating Area (SOA) [7–11].
- *bifurcations* can take place, i.e., more than one operating point exist [12–14].

Moreover, convergence is a sensitive issue for ET simulation since multiple

operating points can also exist due to the adopted mathematical form of the device model, leading to non-physical solutions [1]. Therefore, an effort must be also made in order to reduce the computational complexity of ET simulations. While ET effects have been historically relevant mainly for power devices and whole systems (e.g., including PCBs), the interest has spread also to integrated circuits (ICs) and radiofrequency (RF) devices. We report now some examples of ET effects for different applications.

Signal and power integrity

Overheating adversely impact power and signal integrity [1, 17, 18]: e.g., non-uniform chip-temperature affects RC delay in an interconnect line, and a thermally-induced propagation delay may lead to timing violation or clock

[1] As a simple example, let us consider the case of a diode that shows self-heating [15, 16] according to the feedback depicted below. The diode current is given by

$$I_D(V,T) = I_S \exp\left[\frac{V_g}{V_{T0}} - \frac{V_g}{V_T}\right]\left[\exp\frac{V}{nV_T} - \frac{V_g}{V_T} - 1\right], \tag{1.1}$$

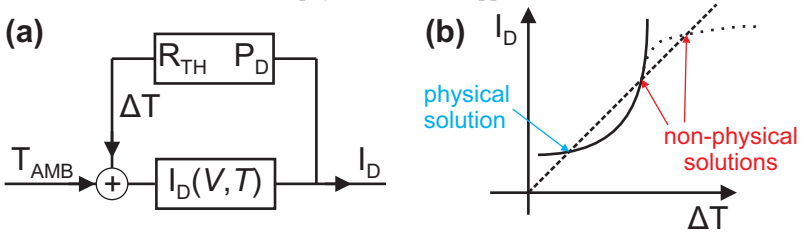
with voltage V, temperature T, activation energy V_g, ideality factor n, thermal voltage $V_T = kT/q$, and $V_{T0} = 0.25\,\text{mV}$. The temperature rise above ambient due to self-heating can be written as

$$\Delta T = R_{TH} \cdot V \cdot I = R_{TH} P_D \tag{1.2}$$

with R_{TH} thermal resistance (described in detail in Section 2.1), and $T = T_{AMB} + \Delta T$. Equation (1.2) can be rewritten as a function of current as

$$I = \frac{\Delta T}{V \cdot R_{TH}} \tag{1.3}$$

At a given voltage V, the two (1.1) and (1.3) must be both satisfied. This can be graphically represented in the $(\Delta T, I_D)$ plane, where the dashed line corresponds to the thermal feedback (1.2), and the solid line to the diode characteristic as a function of temperature (1.1). From the plot is apparent that self-heating leadsfor a diode to the existance of two solutions due to the interplay of (1.2) with a constant slope, and the exponential increase of (1.1). If an upper limit to numerical value of the exponential function is given in order to avoid overflow, represented with the dotted line, another non-physical solution appear.



skew [19]. With respect to this topic, Section 4.2 reports an ET simulation of an interconnect line in a highly-integrated module, while in Section 3.5 is devoted to the analysis of a power delivery network, proposing a clustering approach to reduce dynamic simulation time effort, and studying the possible adoption of carbon-based materials.

Power devices

The characterization of power devices is application-critical, and is often made by referring to standardized tests. In order to achieve a first-time right design, "simulated testing" would therefore be useful [20, 21].

As an example, the Unclamped Inductive Switching (UIS) test of an Insulated-Gate Bipolar Transistor (IGBT) is considered hereinafter [22]. Fig. 1.1 summarizes the circuit and typical behaviors for the UIS test, widely used to identify the maximum energy sustainable by a device subject to high-stress avalanche conditions. The idealized circuit used to perform the UIS involves a load inductor L, unclamped since there is no free-wheeling diode.

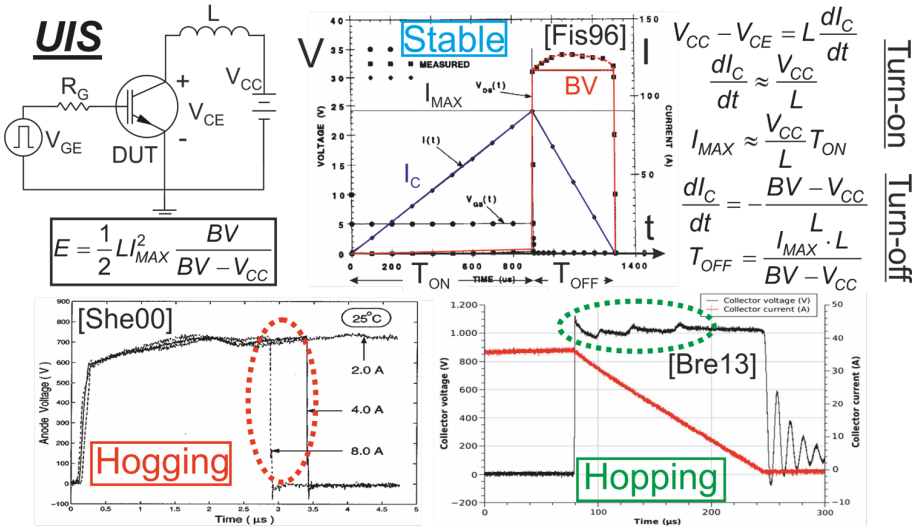


Fig. 1.1. Schematic summary of the UIS test: circuit, maximum sustainable energy, and three observable behaviors.

The typical UIS behavior can be described as follows, corresponding to uniform current/temperature distribution [23]:

- The gate of the device under test (DUT) is pulsed for a time T_{ON}, and during this time the current through the device increases linearly with a

slope given by the ratio of the applied voltage and the inductance value. At T_{ON} the current reaches its maximum value I_{MAX}.

- Afterward, the device is turned off and the inductor forces it into the breakdown region. During this phase the current decreases linearly again with a different slope, since the voltage over the inductor is given by the difference of the avalanche-sustaining breakdown voltage (BV), and the supply voltage.
- The energy dissipated can be computed with elementary observations.

However, it has been repeatedly evidenced that uneven current/temperature fields can occur in multicellular power devices subject to UIS test, thereby reducing the ruggedness due to the higher temperature peaks with respect to standard behavior, or even leading to sudden failures induced by hot spots well below the expected sustainable energy limit [24]. Stable current nonhomogeneities have been detected through measurements performed at individual pads [25] and maps obtained by lock-in thermography (LIT) [26]; in this case, the BV waveform either exhibits a small drop or it is negligibly impacted. Irreversible device failures have also been found to occur, which manifest themselves with a dramatic BV collapse [3, 27, 28], and are commonly associated to an unstable current crowding over a small device area (also referred to as *hogging*), as witnessed by a first-order circuit simulation approach [27] and LIT [28]. Lastly, a *hopping* phenomenon, i.e., a fast activation/vanishing of filaments over different device portions, has received attention in a number of papers [3, 29–33]. This mechanism, experimentally observed through infrared (IR) temperature maps [31] and current measurements carried out with a Rogowski coil setup [32], has been correlated with the occurrence of BV oscillations [3, 29, 31–33], as evidenced also by simple 2-D [29] and two-cell 3-D [3] finite element method (FEM) simulations.

Hogging and hopping phenomena can be simulated only by including ET effects. It is worth noting that the aforementioned uneven current/temperature fields reduce the device ruggedness due to the higher temperature peaks with respect to stable behavior, and might lead to sudden failures well below the expected sustainable energy limit. In Section 4.3 ET simulations are performed exhibiting hogging and hopping, with the latter ascribed to the S-shaped avalanche curve.

RF devices

Dynamic ET effects play an important role in determining the behavior of Power Amplifiers (PAs) operating according to WLAN standard defined by IEEE802.11. WLAN is based on a time-division duplexing system: the output PA of the mobile unit is continuosly switched on (for transmission) and off (for receiving) to save power, as in Fig. 1.2. After each switch the connection with the mobile unit is re-estabilished through a training sequence used to set the automatic gain control and to calibrate phase, amplitude and timing of the signal. The training signal lasts 20 µs and it is assumed that the transmit power level is constant until the end of the packet, which is *not* correct due to thermal effects. This results in higher dynamic Error Vector Magnitude (EVM), i.e., the magnitude of the difference between the measured vector for a coded symbol and the ideal vector, with respect to the one that would be measured in static condition [34].

Significant ET effects take also place when a PA is subject to a two-tone excitation. Under a two-tone excitation, if the difference frequency is small enough, a temperature and transconductance oscillation takes place. The transconductance change implies the generation of new spectral components, thus worsening the PA performance [35]. Therefore, it is crucial to account for dynamic ET effect for RF circuit analysis.

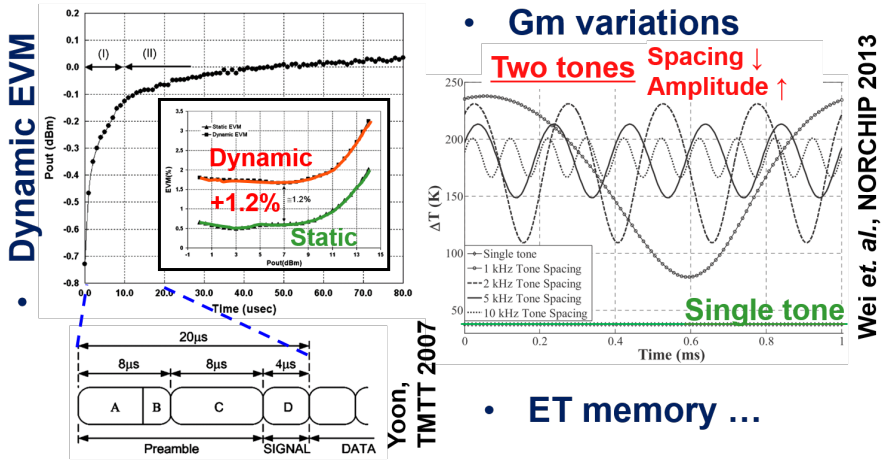


Fig. 1.2. Some examples of ET effects relevant for RF devices [34, 35].

1.2 Electrothermal simulation methods and TFBs

The approaches to ET simulation can be roughly divided into four classes:

1. Physics-based (device-level), in which the the simulator solves the *full physical model* for the electrical and thermal quantities.
2. Relaxation method, in which the thermal and electrical problems are treated *separately* by two simulators, and a supervisor is used to exchange data between them, as depicted in Fig. 1.3.
3. Model order reduction (MOR)-based methods, in which the whole system equations – given by discretization of PDEs – are reduced and projected with suitable manipulations in a state-space form (e.g., [36]). MOR-based methods are commonly used when multidomain simulations have to be performed such as for Micro Electro-Mechanical Systems (MEMS) [37], or specific models e.g., for transmission line detailed ET analysis [38].
4. Thermal Feedback Block (TFB)-based (sometimes referred to as "direct"), as depicted in Fig. 1.4. In this case a standard circuit tool (e.g., PSPICE [39]) is used to perform the coupled ET simulation, in which the thermal problem is modeled through an electrical equivalent with the *thermal equivalent of the Ohm's law*.

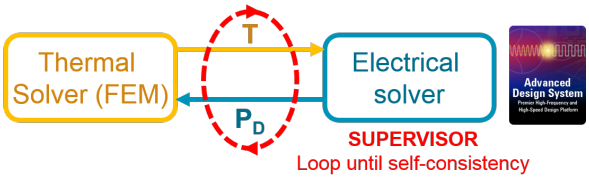


Fig. 1.3. Simplified scheme of a relaxation method.

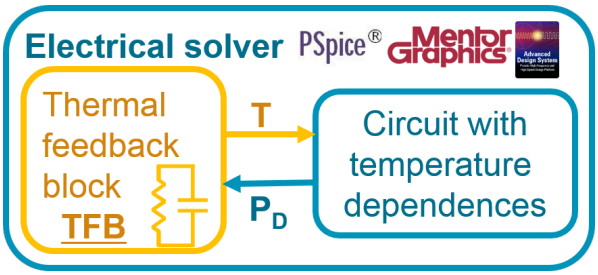


Fig. 1.4. TFB-based ET simulation scheme.

Physics-based (device-level)

In physics-based simulation a fully-coupled system of partial differential equations or integral-differential equations is written for the DUT. Considering an electronic device, going from the most detailed to the simples, there are [40]:

- The *Boltzmann Transport Equation* (BTE), which gives as output the statistic distribution of the carriers and phonons.
- The *Hydrodynamic model*, obtained as a moment approximation from the BTE, in which different temperatures are used for the crystal lattice, electron and holes.
- The *Thermodynamic model*, simple extension of the drift-diffusion, in which both the carriers and the crystal lattice are assumed to be at the same temperature.

The ET simulation at device level is the most detailed and in-depth method. However, it requires a very high computational effort. Therefore only some small device sections or idealized structures can be simulated.

Relaxation method

In the relaxation method, a dynamic ET simulation is performed according to the flowchart in Fig. 1.5, assuming for example SPICE as the circuit simulator, and COMSOL [41] as the thermal simulator. The main advantage of this method lies in the possibility of using stable commercial tools. However, the computational effort is still high enough that only fairly simple systems can be simulated; moreover, the numerical stability is an issue in the supervisor – i.e., the program responsible for interfacing the two tools – since the electrical and thermal problems time constants are usually characterized by different orders of magnitude, leading to extremely stiff problems.

TFB-based

A technique which is very effective and easy to integrate into the standard design flow involves the use of an electrical equivalent of the thermal problem through the *thermal equivalent of the Ohm's law* as fully detailed in the following Section: the temperatures and the dissipated powers are represented as voltages and currents, respectively.

We denote as *Thermal Feedback Block* (TFB) a SPICE-like circuit suited to describe the power-temperature feedback, i.e., that given as input the dissipated powers of the M active devices, provides as output their temperature rises over

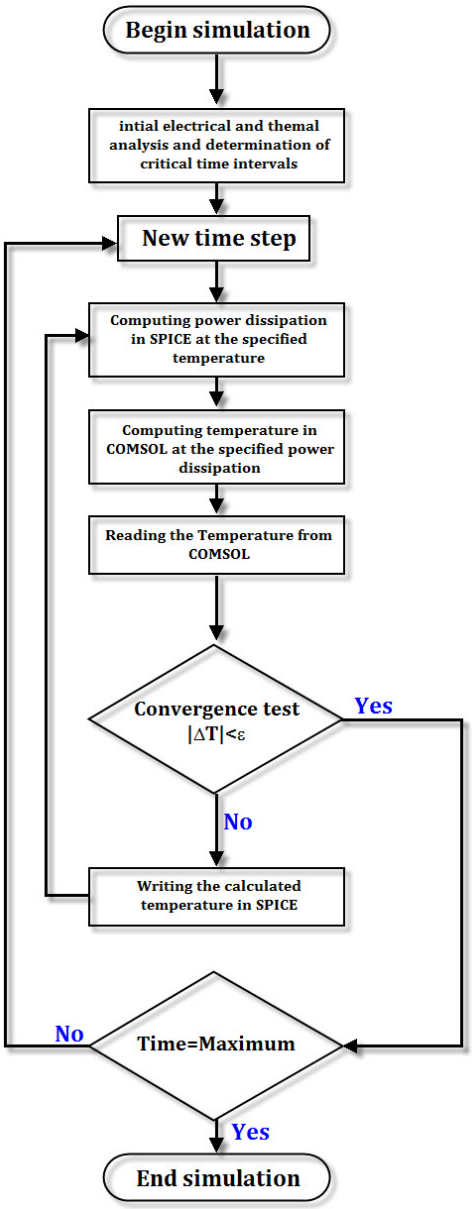


Fig. 1.5. ET simulation with relaxation method - flow chart [42].

ambient [2]. The TFB, besides enabling purely thermal analyses with arbitrary power profiles that would be unviable otherwise, can be also used to perform extremely effective ET simulations, as schematically depicted in Fig. 1.6:

- The electronic active components are implemented by means of the following procedure: the standard device is replaced by a subcircuit equipped with the conventional electrodes and two additional terminals, namely, an input node fed with the temperature rise above ambient, and an output node providing the dissipated power. The subcircuit is composed by (i) a standard device component as a main element, as well as (ii) resistances, and supplementary linear/nonlinear controlled sources to include specific physical mechanisms and to allow the variation of the temperature-sensitive parameters during the simulation run;
- The electrical macromodels are connected to the TFB in order to account for the power-temperature feedback: the temperature rise provided to each electrical device is determined at any time instant from the pow-

[2] Besides the techniques described in Chapters 2 and 3, TFBs can be also obtained
- directly from the Fourier heat equation discretization [43, 44];
- from analytical approximations of the Fourier heat equation solutions [45];
- from more advanced heat equations [46, 47];
- independently from boundary and initial conditions of the thermal problem [48, 49].

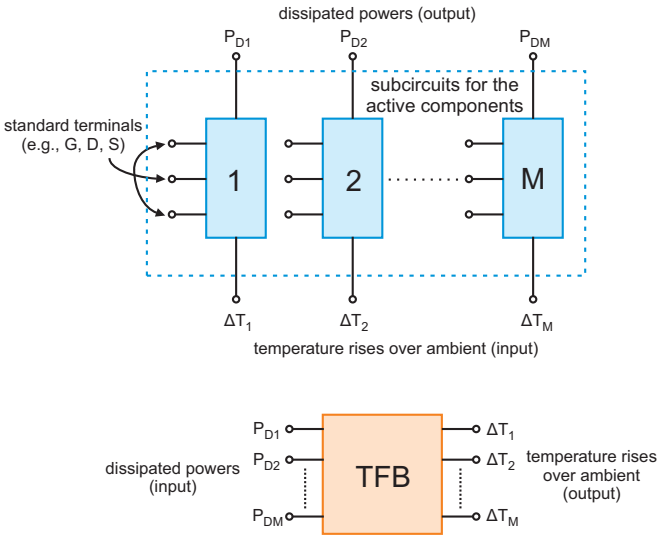


Fig. 1.6. Schematic representation of the strategy to perform an ET analysis in a circuit simulation tool.

ers dissipated by all the active components, i.e., the heat sources in the thermal model;
- As a result, the dynamic ET behavior of the electronic system is represented by a merely electrical network that can be solved by a commercial circuit simulator with little requirement in terms of CPU time and memory storage, as well as reduced possibility of convergence problems.

The aforementioned approach is suited to perform fast and effective dynamic ET analyses of electronic systems, circuits, and multicellular / multifinger devices, as described for a variety of case studies in Chapter 4.

1.3 Thesis outline

After this brief introductory chapter, featuring the motivation behind this work, the following 3 main core chapters are focused on thermal analysis, TFBs, and their applications.

TFBs assuming constants material parameters, i.e., *linear* thermal problems, can be built starting from either measurement or simulation data by resorting to many macromodeling techniques. In **Chapter 2** an *in-house tool* for the identification and synthesis of linear TFB is described, and the network topologies performance in PSPICE is compared. As an example, the extraction of a TFB for an ultra-high integrated system suffering from significative thermal issues is presented.

Contribuition that were made to overcome some of the limitation of linear TFBs are reported in **Chapter 3**. Starting from a suitable interpolation of linear TFBs, more general parametric TFBs are introduced that allows taking into account variations according to a number of design parameters. Subsequently, the tool denoted as FANTASTIC based on Multi-Point Moment Matching is presented as an advanced linear TFB, featuring unprecedented speed and accuracy with respect to conventional solutions. A nonlinear TFB is, then, introduced for a single heat source and its applicability shown with a relevant case study. Some advancements toward the use of energy-balance models to describe the heat propagation in state-of-the-art SiGe heterojunction bipolar transistors are presented. Lastly, a node clustering strategy for power delivery networks is presented, also comparing the performance of copper interconnects with carbon-based materials.

Chapter 4 is devoted to the application of TFBs in realistic cases of interest of dynamic ET simulations for electronic devices, circuits and systems.

Finally, **Chapter 5** provides the main conclusions.

Chapter 2

Identification and synthesis of linear TFBs

TFBs in which the material parameters are assumed to be temperature insensitive, can be obtained by resorting to *linear macromodeling* techniques as detailed in this Section, starting from either measurements or simulations. The thermal problem is described as an "input-output" process, where the heat dissipation takes place in some specific regions – heat sources (HSs) – and the temperature is to be modeled only in assigned positions which are relevant from an electrical viewpoint: e.g., for a bipolar junction transistor (BJT) heat dissipation occurs in the base-collector space-charge region while the temperature is to be evaluated at the base-emitter junction. The equation describing the linear thermal conduction problem in a non-nanometric bounded region is the Fourier heat equation, which relates the generated power density g [W/μm^3] and the temperature T[K]

$$\rho\left(\mathbf{r}\right)c\left(\mathbf{r}\right)\frac{\partial T\left(\mathbf{r},t\right)}{\partial t}=\nabla\cdot\left[k\left(\mathbf{r}\right)\cdot\nabla T\left(\mathbf{r},t\right)\right]+g\left(\mathbf{r},t\right) \tag{2.1}$$

being ρ is the mass density [kg/μm^3], c the specific heat [J/(kgK)] and k the thermal conductivity [W/ μmK] of the medium. Equation (2.1) is completed by considering uniform initial condition, and Dirichlet, Neumann or mixed boundary conditions (BCs). A compact thermal model describing the heat propagation, which can be synthesized into a TFB, is schematically represented as in Fig. 2.1. The *average* temperature rises over ambient $\Delta T_i = T_i - T_{AMB}$ induced by the dissipation of the spatially dependent power densities $g_i(\mathbf{r})$ (with total power P_{Di}) can be modeled through an equivalent

circuit with the *thermal equivalent of the Ohm's law*, namely with ΔT_i corresponding to voltages and P_{Di} to currents. Such correspondence is theoretically sound since there is a formal equivalence between a suitable RC network and (i) any spatial discretization of the linear Fourier conduction equation, and (ii) its solution as an eigenvalue problem [50, 51].

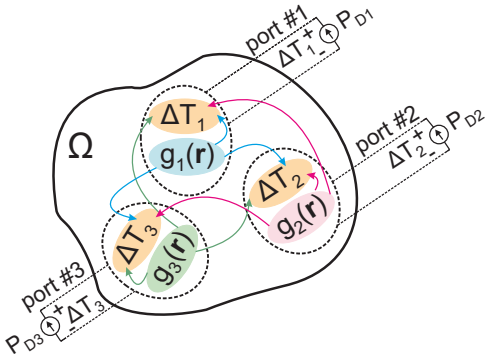


Fig. 2.1. Schematic representation of the compact thermal model for a problem with 3 heat sources [50, 51].

2.1 Thermal resistance and impedance

Self-heating

For the sake of simplicity, let us first consider the case of a single HS so as to provide some basic theory, corresponding to the case of one device or an isolated element in a more complex electronic system.

The *thermal resistance* R_{TH} is defined as the steady-state temperature increase over ambient subsequent to the dissipation of a power P_D, normalized to P_D itself

$$R_{TH} = \frac{T - T_{AMB}}{P_D} = \frac{\Delta T}{P_D} \tag{2.2}$$

R_{TH} is dependent on the material and geometric properties.

The transient thermal behaviour is described with the *thermal impedance* $Z_{TH}(t)$ [52], defined as the thermal *step* response of the device, i.e. the transient temperature rise over ambient due to the application of a power step of amplitude P_D, normalized by its amplitude

$$Z_{TH}(t) = \frac{\Delta T(t)}{P_D} \tag{2.3}$$

R_{TH} is the *steady-state* value of the thermal impedance, i.e.,

$$R_{TH} = \lim_{t\to\infty} Z_{TH}(t) \tag{2.4}$$

A typical plot for the thermal impedance is depicted in Fig. 2.2, with log time axis. Log time samples is used for both simulation and measurements since $Z_{TH}(t)$ spans multiple decades.

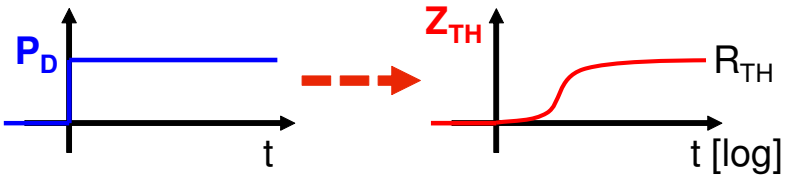


Fig. 2.2. Thermal impedance definition.

It is worth noting that this nomenclature, while commonly adopted in the literature, is *not* consistent with the usual one adopted in electrical circuit theory, where "impedance" is used to express the Fourier transform of the *impulse* response. We denote with the symbol $Z_{TH,impulse}(t)$ [K/W] the temperature rise above ambient generated by a power impulse applied at t=0, normalized to its amplitude, representing the derivative of the thermal impedance $Z_{TH}(t)$.

$$Z_{TH,impulse}(t) = \frac{d}{dt} Z_{TH}(t) \tag{2.5}$$

If $Z_{TH}(t)$ is known, due to the assumption of linearity corresponding to constant material parameters, the temperature rise above ambient due to the application of an arbitrary power profile $P_D(t)$ can be expressed as the convolution between $P_D(t)$ and $Z_{TH,impulse}(t)$

$$\Delta T = \int_0^t Z_{TH,impulse}(t-\tau) P_D(t) d\tau \tag{2.6}$$

Considering problem (2.1), $Z_{TH,impulse}(t)$ can be obtained by solving the heat equation as an eigenvalue problem [53]:

$$Z_{TH,impulse}(t) = \sum_{k=1}^{\infty} \Gamma_k e^{-\lambda_k t} \tag{2.7}$$

being λ_k real positive eigenvalues constituting a monotonically increasing sequence, and Γ_k positive shape factors for the considered physical domain. It

is worth noting that, due to properties of (2.7), $Z_{TH,impulse}(t)$ is positive and $Z_{TH}(t)$ is monotonic. Due to the linearity assumption of the thermal problem, it is possible to define the frequency and Laplace domain thermal impedance as the Fourier and Laplace transform of $Z_{TH,impulse}(t)$, respectively (as done, e.g., in [54] introducing a phasor notation for the power and temperature). There is a steadily increasing interest in the thermal impedances in the frequency domain, as shown by recent studies both for simulation [55–60] and most importantly for novel measurement techniques [54, 58, 61–64]. Taking the Laplace transform of (2.6) and (2.7), we get

$$\Delta T(s) = Z_{TH,impulse}(s) P_D(s) \tag{2.8}$$

$$Z_{TH,impulse}(s) = \sum_{k=1}^{\infty} \frac{\Gamma_k}{s + \lambda_k} \tag{2.9}$$

$Z_{TH,impulse}(s)$ being passive and Positive Real (PR) [53]. It is apparent that (2.9) can be interpreted as a single-port electrical equivalent of the thermal impedance, since it is the electrical impedance of a canonical Foster representation (form I) of a distributed passive lumped RC network, albeit of infinite length, with proper positive values for the parallel pairs of resistors R and capacitors C thus providing a non negative impulse response [53]. By considering a finite sized Foster network of n_c RC pairs, a finite *fit* is assumed, which will be characterized by an error depending on the number of poles used, i.e. on the fit accuracy:

$$Z_{TH,impulse}(s) = \sum_{k=1}^{n_c} \frac{\Gamma_k}{s + \lambda_k} \leftrightarrow Z_{TH,impulse}(s) = \sum_{k=1}^{n_c} \frac{R_k}{1 + sR_kC_k} \tag{2.10}$$

$$R_k = \Gamma_k/\lambda_k \quad \mathrm{C}_k = 1/\Gamma_k \tag{2.11}$$

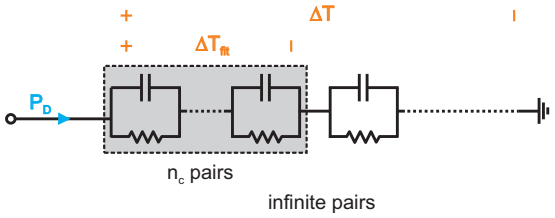


Fig. 2.3. Foster network for self-heating [52].

The thermal impedance can be characterized in the time domain by its thermal risetime, and in the frequency domain by its thermal cutoff frequency as depicted in Fig. 2.4:

- The *thermal risetime* t_R is defined as the difference of the time instants in which the thermal impedance is the 90 % and 10 % of its steady state value

$$t_R = t_{90\%} - t_{10\%} \tag{2.12}$$

- The *thermal cutoff frequency* f_{TH} is defined as the 3db frequency of $|Z_{TH}(f)|$ - namely, the value of frequency for which the thermal impedance spectrum is reduced with respect to the steady state value by a factor of $\sqrt{2}$

$$|Z_{TH}(f_{TH})| = \frac{R_{TH}}{\sqrt{2}} \tag{2.13}$$

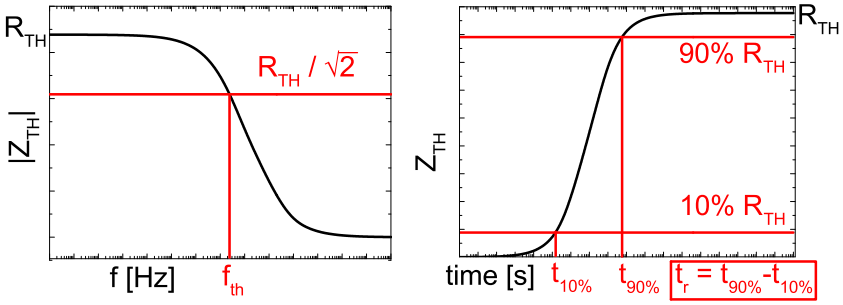


Fig. 2.4. Thermal cutoff frequency f_{TH} (left) and risetime t_R (right) of Z_{TH}.

Mutual heating

The single-port network can only be used to describe self-heating, i.e., the heating on a device/chip due to the power dissipated by the device/chip itself. If the electronic system under analysis includes M power-dissipating regions (corresponding to M HSs), the thermal interactions are taken into account through the *mutual (coupling) thermal impedance* $Z_{THij}(t)$, which – in analogy to (2.3) – is defined as

$$Z_{THij}(t) = \frac{\Delta T_i(t)}{P_{Dj}} = \frac{\Delta T_j(t)}{P_{Di}} \tag{2.14}$$

that is, it represents the temperature rise over ambient of a HS due to the activation of the other, normalized to the power dissipated by the latter. It must be remarked that, in spite of the (unfortunate) nomenclature, the mutual impedance must be considered as an indicator of the thermal coupling degree between the HSs.

Thermal impedance matrix

Self and mutual thermal impedances are the elements of the M×M *thermal impedance matrix* denoted with $\mathbf{Z}_{TH}$, symmetric due to the reciprocity of the thermal problem. In this case, the electrical equivalent is given by a M-port network relating the temperature rise over ambient $\Delta T_i(t)$ and power $P_{Dj}(t)$ defined at the *i*-th and *j*-th ports, respectively. The structure and properties described for the single-port in Fig. 2.3 can be generalized by introducing a RC *Multi-port* network [65]. The model is thus given in the form

$$\mathbf{Z}_{TH,impulse}(s) = \sum_{k=1}^{\infty} \frac{\mathbf{R}_k}{s - p_k} \tag{2.15}$$

where:

- all poles are real and stable;
- the residue $M \times M$ matrices $\mathbf{R}_k$ are symmetric and positive semi-definite;

thus $\mathbf{Z}_{TH,impulse}(s)$ is Positive Real (PR).

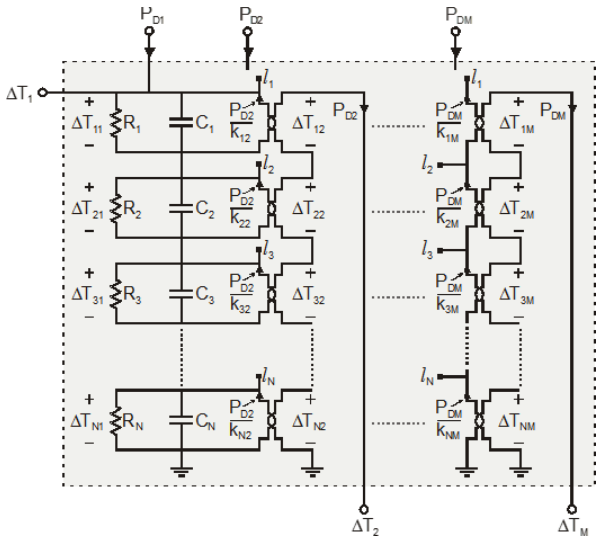


Fig. 2.5. Basic synthesis topology for the $\mathbf{Z}_{TH}$ matrix; labels l_1, l_2, ..., l_N identify network nodes.

For model (2.15) is possible to define a fit by considering a finite number of poles, as depicted in Fig. 2.5. The usual evaluation of $\mathbf{Z}_{TH}$ with a FEM tool is obtained by performing transient thermal simulations for all the HSs, activating only one of them at a time, while evaluating the temperature in all the regions.

2.2 Description of the in-house tool

An *in-house* tool has been developed for the extraction of TFBs starting from a measured or simulated thermal impedance matrix. The procedure, as schematically depicted in Fig. 2.6, involves two step:

1. *Identification* in which a compact model correctly describing the input data is obtained, starting either from time or frequency-domain data;
2. *Synthesis*: an equivalent electrical network providing the same step response of the model identified in the previous step is given as a netlist.

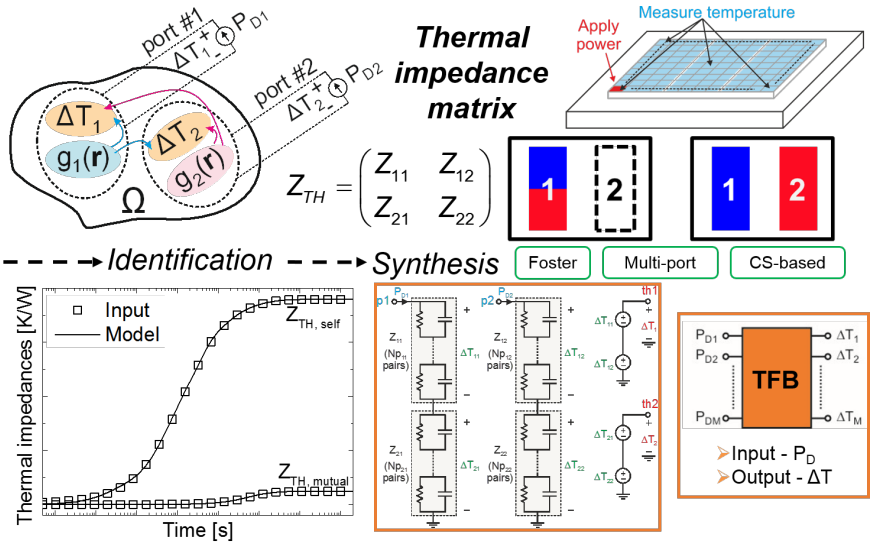


Fig. 2.6. Identification and synthesis schematic procedure.

The identification and synthesis sub-procedures are classified as depicted in Fig. 2.7 according to the form of input data, which can be given in the time or frequency domain, and to the *hypothesis on the time constants* that also define the synthesized topology:

- All terms of the $\mathbf{Z}_{TH}$ can be treated separately. This is the approach mostly used for microelectronics and power eletronics applications (see e.g., [52, 66–68]), and corresponds to the classical Foster network. The identification is performed in the time domain by resorting to the semi-empirical approach described in [69], or with optimization-based procedures as described in Section 2.3.1. In the frequency domain the Vector Fitting (VF) procedure [70–75] can be used, e.g., exploiting its open

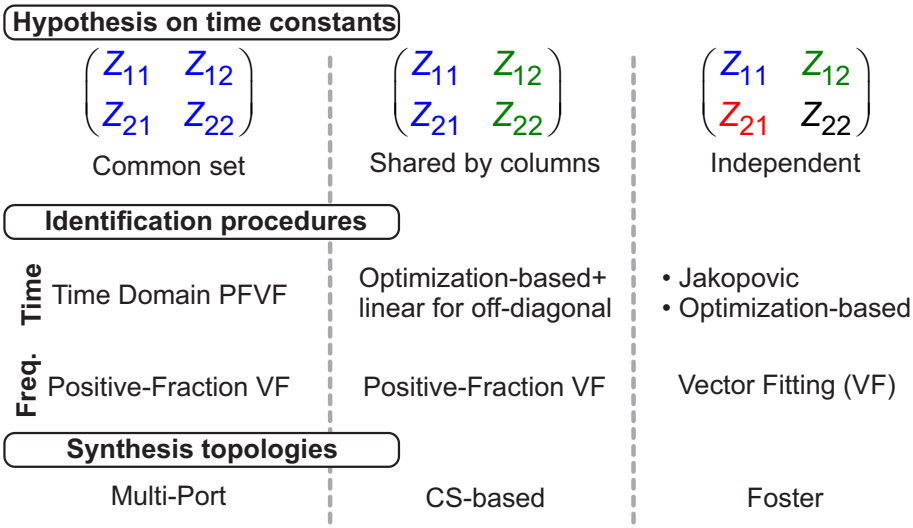


Fig. 2.7. Classification of the implemented identification and synthesis routines.

source implementation [76].

- At the other end of the spectrum, a common set of time constants can be assumed to be shared among all the element of the thermal impedance matrix, as obtained from the theory reported in [65]. In this case the identification can be performed with variants of the VF with passivity enforcement, such as the Positive Fraction VF (PFVF) [77, 78] for the frequency domain data, and the Time Domain VF (TDVF) [79, 80] with subsequent passivity enforcement [81–83] or the a-priori passive Time Domain PFVF (TDPFVF) [84] for time-domain data. The synthesis is then performed with the Multi-port topology [50, 51, 65, 78], relying on ideal transformers.
- Walkey *et al.* describe in [85, 86] a thermal network compactly describing thermal coupling for DC. Assuming that the mutual thermal impedances of a row/column of the thermal impedance matrix can be described with the same time constants of the self-heating one, the aforementioned network can be extended for the dynamical case [87]. The identification can be performed in the frequency domain with variants of the VF but considering a row instead of the full $\mathbf{Z}_{\mathrm{TH}}$ matrix; or in the time domain in two steps (1) as described for the Foster network for the terms Z_{ii} and (2) by solving a linear system for each mutual term Z_{ij}, $i \neq j$, in which the time constants are known.

2.2.1 Simple example on the applicability of the shared time constant hypothesis

Besides the theoretical derivation in [65], the time constants sharing between elements of $\mathbf{Z}_{TH}$ can be also seen in the following simple two-source case. Consider a homogeneous isotropic parallelepiped domain (with dimensions A, B, C), with adiabatic lateral/top faces, and isothermal bottom. Assume that two volumetric heat sources (VHS), denoted as #1 and #2 and shaped as parallelepipeds are located in the structure. VHS #1 is activated with a power step at t=0, and uniform power density g, while #2 is kept inactive. The dimensions of VHS #1 are $W = x_2 - x_1$, $L = y_2 - y_1$, and $H = z_2 - z_1$, as shown in Fig. 2.8.

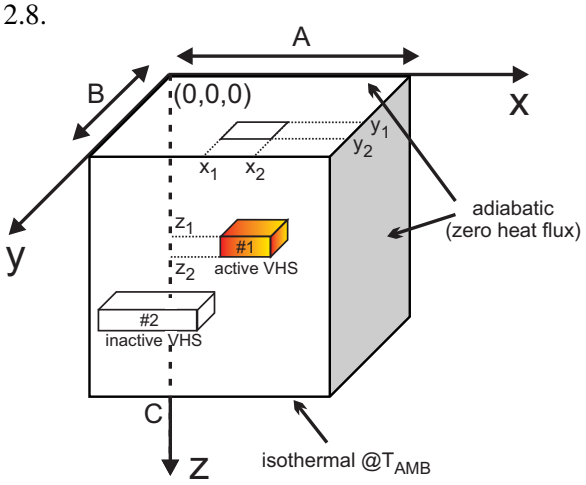


Fig. 2.8. Representation of a parallelepiped domain with two heat sources.

The dynamic temperature increase over ambient normalized to the power dissipated by #1 can be evaluated through the Green's function method [88,89], and is given by

$$Z_{TH}(x,y,z,t) = \frac{T(x,y,z,t) - T_{AMB}}{gWLH} = \frac{2}{kABCWLH} \cdot$$
$$\left\{ WL \sum_{p=1}^{\infty} \frac{1}{\nu_p^3} Z_p(z) \left[Z_p'(z_2) - Z_p'(z_1) \right] \left[1 - e^{-\alpha \nu_p^2 t} \right] + \right.$$
$$2W \sum_{n=1}^{\infty} \sum_{p=1}^{\infty} \frac{1}{\gamma_n \nu_p \left(\gamma_n^2 + \nu_p^2 \right)} Y_n(y) Z_p(z) \left[Y_n'(y_2) - Y_n'(y_1) \right] \cdot$$
$$\left. \cdot \left[Z_p'(z_2) - Z_p'(z_1) \right] \cdot \left[1 - e^{-\alpha \left(\gamma_n^2 + \nu_p^2 \right) t} \right] + \right.$$

$$2L\sum_{m=1}^{\infty}\sum_{p=1}^{\infty}\frac{1}{\beta_m\nu_p\left(\beta_m^2+\nu_p^2\right)}X_m(x)Z_p(z)\cdot$$
$$\cdot\left[X_m^{'}(x_2)-X_m^{'}(x_1)\right]\cdot\left[Z_p^{'}(z_2)-Z_p^{'}(z_1)\right]$$
$$\cdot\left[1-e^{-\alpha\left(\beta_m^2+\nu_p^2\right)t}\right]+$$
$$4\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\sum_{p=1}^{\infty}\frac{1}{\beta_m\gamma_n\nu_p\left(\beta_m^2+\gamma_n^2+\nu_p^2\right)}X_m(x)Y_n(y)Z_p(z)\cdot$$
$$\cdot\left[X_m^{'}(x_2)-X_m{}'(x_1)\right]\cdot\left[Y_n^{'}(y_2)-Y_n^{'}(y_1)\right]\cdot$$
$$\cdot\left[Z_p^{'}(z_2)-Z_p^{'}(z_1)\right]\cdot\left[1-e^{-\alpha\left(\beta_m^2+\gamma_n^2+\nu_p^2\right)t}\right]\Bigg\} \tag{2.16}$$

where $\alpha = k/(\rho c_p)$ is the thermal diffusivity, and

$$X_m(x)=\cos(\beta_m x),\quad Y_n(y)=\cos(\gamma_n y),\quad Z_p(z)=\cos(v_p z) \tag{2.17}$$
$$X_m^{'}(x)=\sin(\beta_m x),\quad Y_n^{'}(y)=\sin(\gamma_n y),\quad Z_p^{'}(z)=\sin(v_p z) \tag{2.18}$$
$$\beta_m=\frac{m\pi}{A},\qquad \gamma_n=\frac{n\pi}{B},\qquad v_p=\frac{\pi(p-1/2)}{C} \tag{2.19}$$

$Z_{TH}(x,y,z,t)$ [K/W] can be reviewed as a *thermal impedance field* due to the activation of VHS #1. By spatially averaging Z_{TH} over the volume of sources #1 and #2, the self-heating and mutual thermal impedances Z_{TH11} and $Z_{TH21}(=Z_{TH12})$ are obtained, respectively. From the inspection of (2.16), it is apparent that these impedances can be expressed as

$$Z_{TH11}(t)=\sum_{k=0}^{\infty}R_{TH11k}\cdot\left(1-e^{-t/\tau_k}\right) \tag{2.20}$$
$$Z_{TH21}(t)=\sum_{k=0}^{\infty}R_{TH21k}\cdot\left(1-e^{-t/\tau_k}\right) \tag{2.21}$$

i.e., *they share the same time constants* (albeit in infinite number), which solely depend on size and material properties of the domain. This result can be generalized to an arbitrary number M of HSs. In this case, all the elements of the matrix will share the same time constants.

2.3 Identification procedures

2.3.1 Time domain for single Z_{TH}

The transient step response of a single-element Foster Network, i.e. a series of n_c RC pairs depicted in Fig. 2.3 [52], is used to describe the time samples of the measured/simulated thermal impedance denoted with $\widetilde{Z}_{TH}(t)$

$$Z_{TH}(t) \approx \widetilde{Z}_{TH}(t) = \sum_{k=1}^{n_c} R_k \left[1 - \exp\left(-\frac{t}{\tau_k}\right)\right] \quad \tau_k = R_k \cdot C_k \tag{2.22}$$

The identification procedure recieves as input the time samples of $\widetilde{Z}_{TH}(t)$, and provides as output the values of the resistances R_k and the capacitances C_k (or the time constants τ_k). In the following the quantities with $\widetilde{\ }$ refer to the input data.

For the simple case of the one RC pair it is possible to formulate the problem as a linear interpolation with R_1=R_{TH} by simply applying a logarithm.

For more than one pair $n_c > 2$ it is possible to resort to the Jakopović method, fully-described in [69, 90], which is a semi-empirical optimization by reduction and elimination, relying on the proper setting of a few empirical parameters with no need to choose a starting point; however this method might be cumbersome to carry out automatically for large matrices $\mathbf{Z}_{TH}$.

Another procedure is based on `fminsearchbnd` by John d'Errico [91] an extension of the standard Matlab function `fminsearch` implementing the Nelder-Mead Simplex Method, that allows the use of constraints on the solution:

- the time constants must be positive $\tau_k > 0$;
- the resistances must be positive and $\sum_k R_k = \widetilde{R}_{TH}$, and thus also $R_k < \widetilde{R}_{TH} \forall k$.

The error to be minimized is the Root Mean Square (RMS) error normalized to the steady-state value defined as

$$Err_{RMS}(Z_{TH}) = \sqrt{\sum_{i=1}^{N_t} \left(\frac{Z_{TH} - \widetilde{Z}_{TH}}{\widetilde{R}_{TH}}\right)^2} \tag{2.23}$$

where N_t is the number of time instants. The *a-posteriori* identification accuracy can be evaluated by the following quantities in the time and frequency domains:

- Maximum relative error in the time domain excluding the very fast tran-

sient

$$Err_{rel,time} = max_i \left| \frac{\widetilde{Z}_{TH}(t_i) - Z_{TH}(t_i)}{\widetilde{Z}_{TH}(t_i)} \right|$$
$$\text{for } Z_{TH}(t_i) > t^* \quad \widetilde{Z}_{TH}(t^*) = 30\% \cdot \widetilde{R}_{TH} \tag{2.24}$$

- Risetime error (percentage)

$$Err_{t_r} = 100 \cdot \left| \frac{\widetilde{t}_R - t_R}{\widetilde{t}_R} \right| \tag{2.25}$$

- Cutoff frequency error

$$Err_{f_{TH}} = 100 \cdot \left| \frac{\widetilde{f}_{TH} - f_{TH}}{\widetilde{f}_{TH}} \right| \tag{2.26}$$

The convergence of the optimization can be accelerated by suitably chosing a starting point. A good starting point can be obtained by assuming n_c time constants logarithmically-spaced in the interval bounded by

- one decade less than $t_1 : \widetilde{Z}_{TH}(t_1) = 0.1\widetilde{R}_{TH}$
- one decade more than $t_2 : \widetilde{Z}_{TH}(t_2) = 0.9\widetilde{R}_{TH}$

The estimation can be further improved by considering N_{trial} random tests of n_c time constants, assuming logarithmically-uniform probability in the aforementioned interval. Given a set of time constants, the thermal resistances minimizing the RMS distance can be found as detailed in the following subsection. The trial which corresponds to the lowest error is given as input to `fminsearchbnd`. N_{trial} usually fixed to 1000, but it can be more since the solution of a linear problem is not too computationally onerous. The chosen interval for the τs has been found by trial and error as a compromise between accuracy and convergence issues: taking a larger time constants span leads to higher accuracy but often converge failure of the synthesized Foster network due huge differences in order of magnitude of τs leading to an extremely stiff numerical problem.

An alternative solution is given by the NonLinear Least Square (NLLS) optimization, again coupled with a proper optimization starting point [84]: $\widetilde{Z}_{TH}$ is approximated with the step response of a first-order system, the time constant of which can be simply evaluated. Such a response can be seen as the sum of n_c responses with coincident real positive time constants. The identification algorithm will then remove the repetitions minimizing the approximation error. The idea is similar to [92].

The in-house tool allows the user to choose either:

1. The number of target n_c RC pairs to perform the identification or
2. A target accuracy defined with respect to $Err_{rel,time}$ and the maximum number of trials. In this case the identification will start from a single RC pair, gradually increasing the number until (i) the target accuracy is met, (ii) the maximum number of trials has been reached or (iii) the error does not significantly decrease in the three subsequent steps.

2.3.2 Time domain for single Z_{TH} at *fixed* time constants

Let $\widetilde{Z}_{TH}(t)$ be known in N_t time instants denoted with t_i. Assuming n_c fixed time constants, a linear least square problem can be formulated as follows:

$$\min(S) = \min \sum_{i=1}^{N_t} \left\{ \widetilde{Z}_{TH}(t_i) - \sum_{k=1}^{n_c} R_k \left[1 - \exp\left(-\frac{t_i}{\tau_k} \right) \right] \right\}^2 = \min \sum_{i=1}^{N_t} \left\{ \widetilde{Z}_{TH}(t_i) - \sum_{k=1}^{n_c} R_k c_k(t_i) \right\}^2 \tag{2.27}$$

where $c_k(t_i)$ is given by

$$c_k(t_i) = \sum_{k=1}^{n_c} \left[1 - \exp\left(-\frac{t_i}{\tau_k} \right) \right] \tag{2.28}$$

and is a known quantity since only the time constants are present.

Equating the derivative of the quadratic distance S to 0, the minimum can be evaluated with the following overdetermined linear system in R_k

$$\frac{\partial S}{\partial R_k} = 0 \rightarrow \begin{bmatrix} a_{kl} & \cdots & \cdots \\ \vdots & \ddots & \ddots \\ 1 & \cdots & 1 \end{bmatrix} \underline{R} = \begin{bmatrix} b_k \\ \vdots \\ R_{TH} \end{bmatrix} \tag{2.29}$$

where

$$a_{kl} = \sum_{i=1}^{N_t} c_k(t_i) c_l(t_i) \tag{2.30}$$

$$b_k = \sum_{i=1}^{N_t} \widetilde{Z}_{TH}(t_i) c_k(t_i) \tag{2.31}$$

and the last row is the condition over the sum

$$\sum_{k=1}^{n_c} R_k = \widetilde{R}_{TH} \tag{2.32}$$

The aforementioned system can be readily solved with the built-in MATLAB command `lsqnonneg`.

2.3.3 Positive Fraction Vector Fitting

We recall from Section 2.1 that a finite fit of the thermal impedance matrix for M heat sources in the Laplace domain $\mathbf{Z}_{TH}(s)$ can be written as

$$\mathbf{Z}_{TH}(s) = \sum_{n=1}^{N_p} \frac{\mathbf{R}_n}{s - p_n} \tag{2.33}$$

where p_n is a vector of N_p real stable poles, and the corresponding residues $\mathbf{R}_n$ are N_p $M \times M$ matrices real, symmetric and positive semi-definite. The electrical equivalent for the thermal problem is a *concretely passive* [93] RC network i.e., with R and C positive and poles are real and stable, and the Foster expansion form of (2.33) is complete [53, 65]. All the aforemantioned properties must be preserved in the identified model. The identification is performed in a two-step process:

1. **Pole identification**. A set of *stable* poles is identified using the vector fitting (VF). In the identification process we also obtain a set of residues that might or might not be positive semi-definite and is discarded.
2. **Residue identification**. At fixed poles, the residues are obtained by formulating the following convex [94] optimization problem (subject to linear inequality constraints)

$$\{\mathbf{R}_n\} = \underset{\{\mathbf{R}_i\}}{\arg\min} \left\| \mathbf{Z}_{TH}(j\omega_k) - \widetilde{Z}_{TH}(j\omega_k) \right\|_2 \tag{2.34}$$

$$\mathbf{R}_n \succcurlyeq 0 \tag{2.35}$$

where (2.35) denotes positive semi-definite. The implementation of the optimization problem within the CVX software environment [95] is described in [78, 96, 97].

In order to perform the identification, the thermal impedance data must be available in the frequency domain. If time-domain measurements or simulations have been performed, those have to be preliminarily transformed in the frequency domain. Such transformation is cumbersome due to the logarithmical spacing in time between samples, and can be performed with Szekely's Network Identification by Deconvolution (NID) [98, 99] described in Section 2.3.6. However, an additional error might be introduced due to this step that could be avoided by implementing a similar identification procedure in the

time domain, as described in the two following subsection [79, 80, 82–84].

It is also worth noting that the bigger component of the identification error stems from the passivity enforcement (step 2). It is possible to synthesize the feedback network skipping step 2: however, in this case there will be in the synthesized network some RC pairs with *negative* resistance and capacitance and that can cause instability in the simulation of more complex circuits, even if by some it is even described as "advantageous" [100].

2.3.4 Time Domain Vector Fitting

In order to avoid a computationally-sensitive transformation from time-domain data to frequency-domain data, the identification can be performed directly in the time-domain with the generalized iterative TDVF scheme [79, 80, 101].

Let us now start from a single element of the thermal impedance matrix in the Laplace domain $Z(s)$ that is to be used to describe the input data of the thermal impedance $\widetilde{Z}(s)$

$$Z(s) \approx \widetilde{Z}(s) = \sum_{n=1}^{N_p} \frac{R_n}{s - p_n}, \tag{2.36}$$

The identification procedure has to optimize the vector of N_p poles p_n and N_p residues R_n so that the transient model response matches the original data. We define a set of initial poles q_n^0 at iteration $i = 0$ to be logarithmically distributed along the real negative axis (consistently to what is done in the nonlinear optimization described in Section 2.3.1). The model (2.36) can be thus written in the equivalent form

$$\widetilde{Z}(s) = \frac{\sum_{n=1}^{N_p} \frac{b_n}{s - q_n^0}}{1 + \sum_{n=1}^{N_p} \frac{c_n}{s - q_n^0}} \tag{2.37}$$

where the coefficients b_n and c_n are unknown. Considering a Laplace-domain power input $P(s)$, we want to enforce the following condition

$$\Delta T(s) \approx \widetilde{Z}(s) P(s). \tag{2.38}$$

Multiplying by the model denominator leads to

$$\left\{ 1 + \sum_{n=1}^{N_p} \frac{c_n}{s - q_n^0} \right\} \Delta T(s) \approx \left\{ \sum_{n=1}^{N_p} \frac{b_n}{s - q_n^0} \right\} P(s) \tag{2.39}$$

which translates, after converting to time domain and evaluating both sides at

the time points t_k, into

$$\Delta T(t_k) + \sum_{n=1}^{N_p} c_n \Delta T_n(t_k) \approx \sum_{n=1}^{N_p} b_n P_n(t_k), \tag{2.40}$$

where

$$\Delta T_n(t) = \int_0^t \Delta T(\tau) e^{q_n^0 (t-\tau)} d\tau, \tag{2.41}$$

$$P_n(t) = \int_0^t P(\tau) e^{q_n^0 (t-\tau)} d\tau = \frac{e^{q_n^0 t} - 1}{q_n^0}. \tag{2.42}$$

The numerical evaluation of $\Delta T_n(t_k)$ using the available temperature data has to be done carefully since the temperature is usually available at log-spaced time steps: a special handling of convolution integrals for speed and accuracy (recursive convolution with time-dependent coefficient) has to be used. Collecting now (2.40) for all time samples t_k leads to a linear system with unknowns b_n and c_n, which can be easily solved in Least Squares (LS) sense.

As standard in VF and TDVF applications [70, 79, 80], the coefficients c_n are used to find the roots of the model denominator in (2.37), which are denoted as q_n^1 and used as starting poles for the second iteration $i = 1$. Then, this pole relocation process is iterated until the set q_n^i stabilizes to the dominant poles of the model p_n according to

$$1 + \sum_{n=1}^{N} \frac{c_n}{s - q_n^0} = \prod_{n=1}^{N} \frac{s - q_n^k}{s - q_n^{k-1}} \tag{2.43}$$

Once these poles are known, the residues R_n are computed by solving the LS system having its k-th row

$$\sum_{n=1}^{N} R_n P_n(t_k) \approx \Delta T(t_k), \tag{2.44}$$

which is obtained by multiplying both sides of (2.36) by $P(s)$ and converting back to time domain.

The above procedure can be applied to self and mutual thermal impedances, leading to different pole/residue pairs for each element of the thermal impedance matrix. However, this procedure is most useful by using a *common pole set* by forming a pole relocation system (2.40), which collects all temperature responses at the same time, as fully detailed in [79, 80]. The passivity of the model can be enforced *a-posteriori* according to [82,83,102–104].

2.3.5 Time Domain Positive Fraction Vector Fitting

The passivity enforcement can also be done *a-priori* with a time-domain formulation of the PFVF. Let us now start from the model to be identified in the form (2.33). By applying a unit power step, the convolution integrals for each pole can be analytically solved, and the thermal impedance matrix is given by

$$\mathbf{Z}_{TH} = \sum_{n=1}^{N_p} \mathbf{R}_n \left(1 - e^{-t/\tau_n}\right) \tag{2.45}$$

where the time constants τ_n are related to the poles p_n by $\tau_n = -1/p_n$. The physical realizability conditions in the time domain are thus

$$\tau_n = -1/p_n > 0 \tag{2.46}$$

$$\mathbf{R}_n \geqslant 0 \tag{2.47}$$

where (2.47) is equal to the frequency-domain condition (2.35), and (2.34) stems from the monotonicity of the thermal impedance.

As done in the PFVF, also in the Time Domain Positive Fraction Vector Fitting (TDPFVF) the identification is performed in a two-step process:

1. **Pole identification**. A set of positive time constants (i.e., real stable poles) can be identified either (i) using TDVF on $\mathbf{Z}_{TH}$, or (ii) using one of the time identification procedures reported in Section 2.3.1 to perform an element-by-element identification and collecting the time constants in a vector $\bigcup_{i,j,n} \{\tau_{ij,n}\}$.
2. **Residue identification**. At given time constants, the residues are obtained by formulating the following convex optimization problem, corresponding to the frequency-domain problem given by (2.34), (2.35)

$$\{\mathbf{R}_n\} = \underset{\{\mathbf{R}_i\}}{\arg\min} \left\| \mathbf{Z}(t_k) - \widetilde{Z}(t_k) \right\|_2 \tag{2.48}$$

$$\mathbf{R}_n \geqslant 0 \tag{2.49}$$

Problem (2.48), (2.49) is convex and can be solved with CVX [95]. The optimal result is independent of the initial guess for residue matrices, which is automatically provided by the solver: therefore the accuracy is not directly related to that obtained in the first step, and is improved by the convex identification.

2.3.6 From time to frequency domain

With the Szekely's method [98, 99] the *time constant spectrum function* describing the thermal resistances associated to the logarithm of the time constants $R_{TH}(\zeta)$, $\zeta = log(\tau)$ of a thermal impedance is evaluated with high accuracy, thus allowing the conversion from time-domain samples to frequency domain data. The thermal impedance $Z_{TH}(t)$ can be written as a linear superposition of exponential time responses with the continuous-time integral

$$Z_{TH}(t) = \int_{-\infty}^{+\infty} R_{TH}(\zeta) \left[1 - \exp\left(-\frac{t}{\tau}\right)\right] d\zeta \tag{2.50}$$

Substituting $z = \exp(t)$, the derivative of $Z_{TH}(z)$ can be written as a convolution integral with known $W(z) = \exp[z - \exp(z)]$ [98, 99]

$$\frac{dZ_{TH}(z)}{dz} = R_{TH}(z) \otimes \mathrm{W(z)} \tag{2.51}$$

The time constant spectrum can be readily evaluated from (2.51) by transforming in the Fourier domain, in which the convolution corresponds to a simple product

$$R_{TH}(\Phi) = \frac{Z^{'}{}_{TH}(\Phi)}{W(\Phi)} \tag{2.52}$$

In the presence of noise $N(t)$, equation (2.52) suffers from an additional contribution, which is enhanced by the extremely small high frequency components of $W(\Phi)$

$$R_{TH}(\Phi) = \frac{Z^{'}{}_{TH}(\Phi)}{W(\Phi)} + \frac{N(\Phi)}{W(\Phi)} \tag{2.53}$$

The noise is not, however, a critical issue for the deconvolution step a noise filtering procedure based on a Bayesian estimation can be performed by resorting to the iterative formula (45) in [99], the convergence and noise properties of which are detailed respectively in [105], and [106]. Given the R_{TH} at the n-th step, the subsequent estimate at (n+1)-th step is given by [99, 105], with

$$R_{TH}^{n+1}(\Phi) = R_{TH}^{n}(\Phi) \left[W(\Phi) \otimes \frac{Z^{'}{}_{TH}(\Phi)}{W(\Phi) \otimes R_{TH}^{n}} \right] \tag{2.54}$$

It can be shown that a fairly small number of iteration (in the order of thousands) is adequate to achieve convergence and a significant reduction of noise [90, 99, 105].

2.4 Equivalent circuit topologies

2.4.1 Foster

The self-heating thermal impedance can be synthesized with a series of RC pairs [52], as depicted in Fig. 2.3.

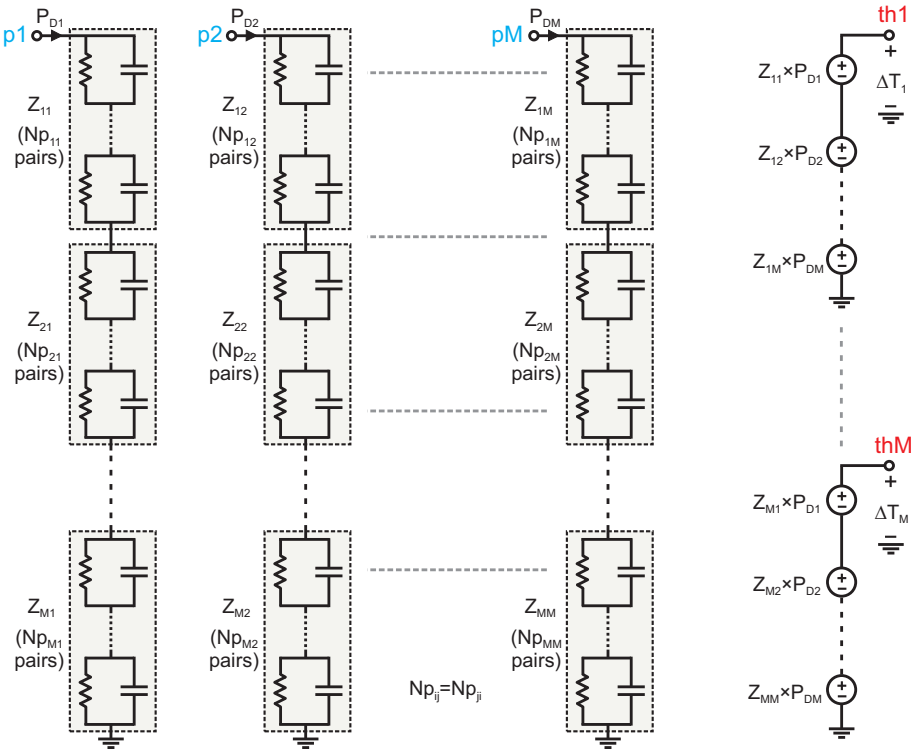


Fig. 2.9. Foster Network for $\mathbf{Z}_{TH}$.

The Foster topology can be used to account for the mutual interaction between HSs with the superposition principle by summing the temperatures (i.e., voltages) due to each contribution, as depicted in Fig. 2.9, in which each series of RC pairs of different length represent a single element of $\mathbf{Z}_{TH}$.

Let Np_S be the average RC cells number of the individual Foster networks

$$Np_S = \frac{1}{M^2} \cdot \sum_{i=1}^{M} \sum_{j=1}^{M} Np_{ij} \tag{2.55}$$

The Foster network requires

- $Np_S \cdot M^2$ RC pairs and M^2 controlled sources [68];
- the extraction of $Np_S \times (M^2 + M)$ parameters since $Z_{ij} = Z_{ji}$ $(i \neq j)$

The synthesis is performed automatically from the identification data. In the actual synthesis is convenient to place the self-heating thermal impedances first, as it has been found by trial and error to improve convergence. This can be explained by observing that the self-heating thermal impedance is the one with fastest response, i.e. characterized by lower τs. Since the RC cells are current-driven, the fastest cells at the top "pull up" easily the potential at the nodes of the other thermal impedances. If instead, a slow thermal impedance is at the input node, the upper potential is at the same forced to be slowly varying while the potential closer to the ground is pulled up fast. A further modification of the synthesis in Fig. 2.9 concerning the type of controlled source, is reported in Section 2.4.4.

It is important to test the synthesized block in PSPICE by simulating each thermal impedance, as the correct identification does not imply the network convergence during simulation. An automated test routine has been implemented to perform the simulation of each thermal impedance and the comparison with the input data. Convergence of the network is a necessary – albeit not sufficient – condition for the use of the TFB for dynamic ET simulations. Since PSPICE does not support a logarithmically spaced time instants, a fairly high number of points is taken into account by suitable partitioning of the simulation interval.

2.4.2 Multi-port

Given the identified $\mathbf{Z}_{TH}$in the form (2.33), the corresponding synthesis scheme is depicted in Fig. 2.5. The aforementioned scheme requires a further diagonalization for $\mathbf{R_n}$ leading to the values for R,C and the ratio of the ideal transformers [107].

Let $\mathbf{R}_n$ be diagonalizable, with eigenvector column matrix $\mathbf{T}_n$,

$$\mathbf{R}_n^* = \mathbf{T}_n^{-1}\mathbf{R}_n\mathbf{T}_n \tag{2.56}$$

and $\mathbf{R}_n^*$ is a diagonal matrix of eigenvalues

$$\mathbf{R}_n^* = \begin{pmatrix} r_{n,1}^* & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & r_{n,M}^* \end{pmatrix} \tag{2.57}$$

Each $\mathbf{R}_n$ matrix can be expressed as a sum of M sub-terms of rank-1 matrices

with only one non-zero element along the main diagonal

$$\mathbf{R}_n = \sum_{m=1}^{M} \mathbf{R}_{n,m} \tag{2.58}$$

$$\mathbf{R}_{n,m} = \mathbf{T}_n^{-1} \mathbf{R}_{n,m}^* \mathbf{T}_n \tag{2.59}$$

A real pole is syntesized by a single RC pair, with pole p_n and residue r_n related to R,C by

$$Z_{TH,n}(s) = \frac{1/C}{1/(RC)+s} = \frac{r_n}{s-p_n} \rightarrow C = \frac{1}{r_n}, \quad R = -\frac{r_n}{p_n} \tag{2.60}$$

All the RC cells in Fig. 2.5 are obtained with (2.60). Due to the diagonalization process, each identified poles corresponds to M RC pairs – i.e., there is a *pole repetition* with a factor M – since the $\mathbf{R}_n$ matrix has been expressed as a sum of M elements. It is worth noting the pole repetition is *not* present in the identified model in the form (2.33). The ideal transformer ratios can be obtained from the first column of the $\mathbf{R}_n$ matrix by collecting its (1,1) element

$$\begin{pmatrix} 1 & k_{n,1,1} & \cdots & k_{n,1,M-1} \\ k_{n,1,1} & k_{n,1,1}^2 & \cdots & k_{n,1,1}k_{n,1,M-1} \\ \vdots & \vdots & \ddots & \vdots \\ k_{n,1,M-1} & k_{n,1,1}k_{n,1,M-1} & \cdots & k_{n,1,M-1}^2 \end{pmatrix}_m \tag{2.61}$$

There is no ideal transformer component in SPICE. However an ideal transformer of ratio k can be implemented in SPICE with a current-controlled current-source at port (CCCS) 1 and a voltage-controlled voltage-source (VCVS) at port 2, as depicted in Fig. 2.10.

$$\begin{cases} V_1 = kV_2 \\ i_2 = -ki_1 \end{cases} \rightarrow \begin{cases} V_2 = \frac{1}{k}V_1 \\ i_1 = -\frac{1}{k}i_2 \end{cases} \tag{2.62}$$

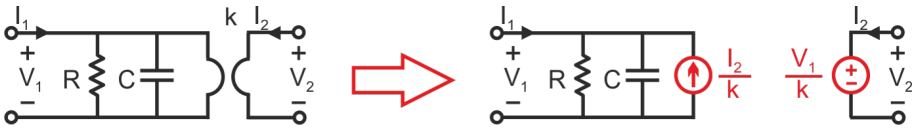


Fig. 2.10. SPICE implementation of an ideal transformer with controlled sources.

The synthesized TFB is depicted in figure 2.11. Assuming that N_{pG} poles are identified, there are:

- $N_{pG} \times M$ RC pairs and $2 \times N_{pG} \times (M^2 - M)$ controlled sources [108];
- $N_{pG} \times (M^2 + 1)$ parameters identified in a single step.

2.4.3 Controlled-Source based

Walkey *et al.* describe in [85, 86] a thermal network allowing a compact description of DC thermal coupling. Assuming the mutual thermal impedances Z_{ij} described with the same time constants of the self-heating Z_{ii} in the same column, such network can be extended for the dynamical case as depicted in Fig. 2.12. For this network the identification is performed in two subsequent steps:

1. self-heating Z_{ii} are identified as in Section 2.3.1: in this step the RC pairs in Fig. 2.12 are obtained;
2. mutual-heating Z_{ij} by solving the problem in Section 2.3.2, thus obtaining the transformer ratios R in Fig. 2.12.

Assuming N_{pCS} as the average poles for each self-heating thermal impedance, there are

- $N_{pCS} \times M$ RC pairs and $N_{pCS} \times (M^2 - M)$ controlled sources (decreasing in number with weaker thermal coupling)
- $2 \times N_{pCS} \times M$ parameters for the Z_{ii}, and $N_{pCS} \times (M^2 - M)$ transformer ratio R parameters for Z_{ji}

2.4.4 Note on the choice of the controlled sources

In the Modified Nodal Analysis (MNA) – the formulation upon which relies PSPICE – each additional network node introduces an unknown to be determined. A sum of voltages, as in the right side of the Multi-port synthesis (Fig. 2.11) with VCVS, can be more efficiently implemented by voltage-controlled current-sources (VCCS) in parallel to a unit resistor: this substitution is depicted in the case of M=2 in Fig. 2.13, and in the following Section we denote this topology as Multi-port B. Of course analogous substitution are to be made for the Foster and CS-based topologies. Further implementation-dependent optimization might be done by considering faster controlled components (e.g., POLY in PSPICE up to 64 inputs).

2.4.5 PSPICE implementation notes

In order to add a TFB in a PSPICE schematic, two file are needed:

- A `.lib` file including the netlist, that starts from the input and output pin definition. The `.lib` file can be easily adapted for different SPICE versions.
- A `.olb` file with the symbol of the component described in the `.lib` file. The `.olb` file can be generated from the represented `.lib` file

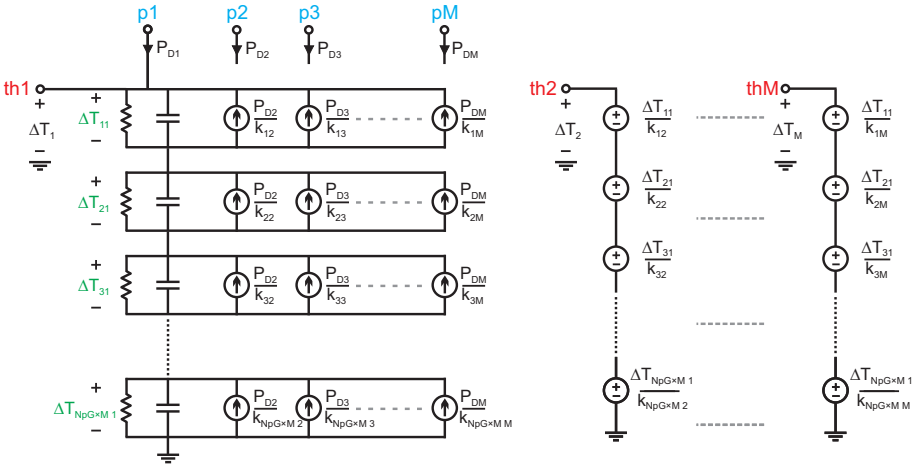


Fig. 2.11. Multi-port synthesis in PSPICE.

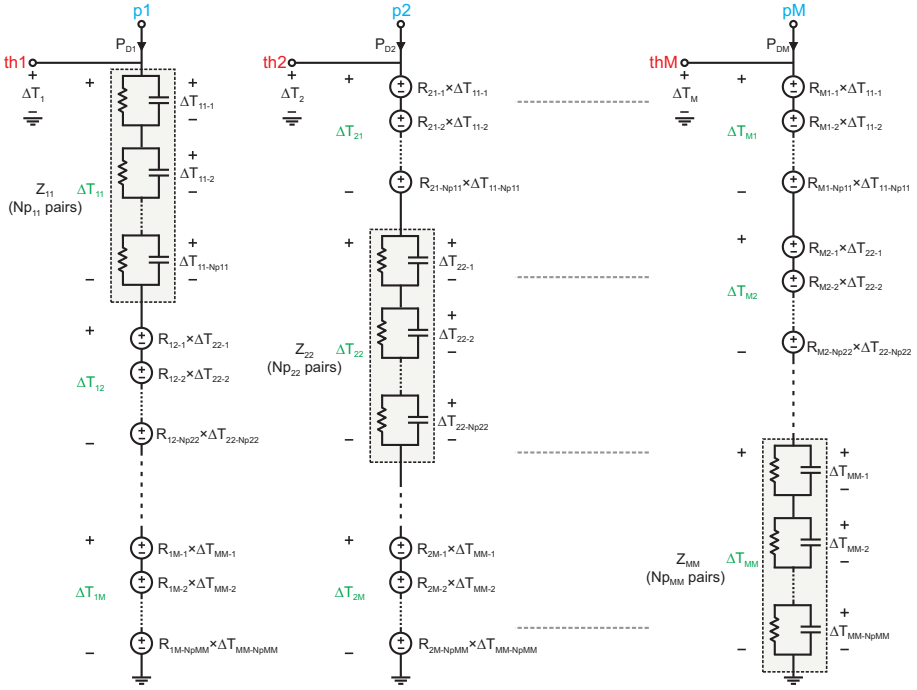


Fig. 2.12. Controlled-source (CS) based TFB.

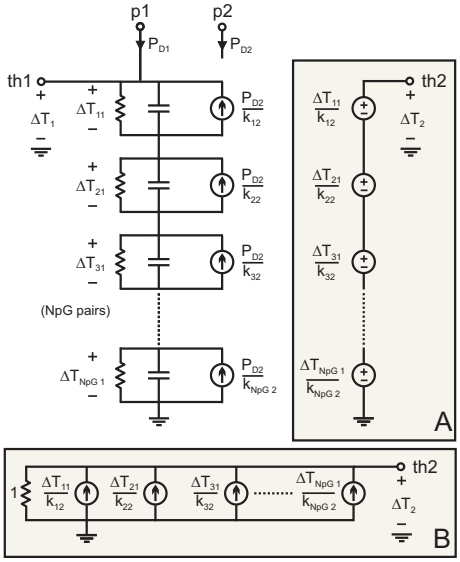


Fig. 2.13. Substitution of VCVS with VCCS in the multiport-B topology.

by using the command *Export to Capture Part Library* inside the *Model Editor* of the PSPICE accessories.

The TFB can subsequently be added:

- Adding the `.olb` file among the project libraries.
- Adding the `.lib` file in the "simulation profile".

2.5 Topologies performance comparison

The described topologies were compared in terms of identification effort and simulation time by considering as a case-study two power GaAs HBT arrays exhibiting different thermal coupling between the individual devices (weak in #1, tight in #2), and varying the number of transistors, as depicted in Fig. 2.14.

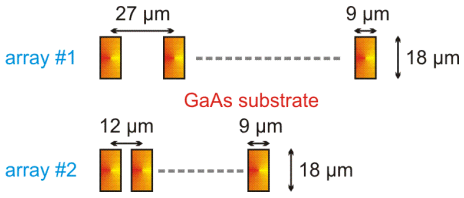


Fig. 2.14. Two GaAs HBT arrays with weak (#1) and tight (#2) thermal coupling between the individual devices.

Fig. 2.15 shows the transient nonuniform temperature field for array #1 with M=12, as determined by PSPICE simulation, and Fig. 2.16 depicts the number of components (a), and the CPU time needed to perform the aforementioned simulation (b) by imposing the same accuracy is the identification step. The main results can be summarized as follows:

- due to its intrinsic flexibility, the Foster network requires the longest identification time while more easily allowing a high degree of accuracy;
- the Foster circuit ensures the lowest number of components for a low thermal coupling, while the highest is embodied in the Multi-port topology(Fig. 2.16a);
- Foster and CS-based networks offer the fastest simulation run regardless of thermal coupling, while the Multi-port variants are adversely-affected by the pole repetition, which is not present in the identified model in the form (2.33) - the most compact in theory [51, 65] (Fig. 2.16b).
- The Multi-port variant B is more effective than the A counterpart, thus showing that the substitution described in Section 2.4.4 improves the efficiency.
- The use of the CS-based network can be suggested for structures with tight thermal coupling since it allows a fast identification, even if the average number of poles N_{pCS} (in Fig. 2.12) for the self-heating Z_{ii} is slightly higher than the one used for the Foster network with the same accuracy. It is worth noting that the CS-based network is the most compact for describing DC coupling effect.

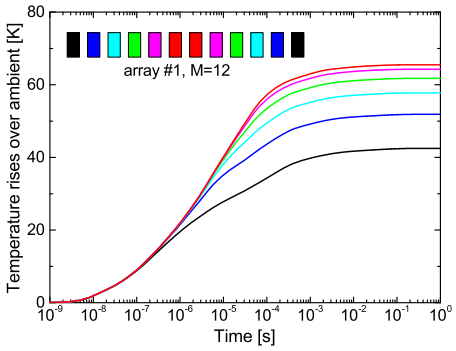


Fig. 2.15. Transient temperature rises over ambient for the individual devices of array #1 (M=12), as obtained by 1-s long ET simulation applying an emitter current I_E=120 mA and a collector-base voltage V_{CB}=3.4 V at the time instant t=0, with a step ceiling amounting to 0.1 ms.

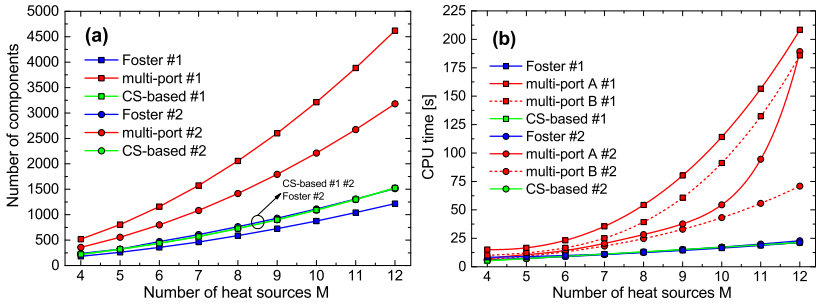


Fig. 2.16. Comparison between the TFBs for the same accuracy in identifying the thermal impedances, as obtained by suitably adjusting the number of RC pairs; (a) number of components and (b) CPU time needed to perform the ET simulation in Fig. 2.15 on a desktop PC.

2.6 Thermal analysis of UTCS

Emerging multichip technologies provide an opportunity to increase the integration density of semiconductor systems so as to yield smaller, lighter, and cheaper products. Nowadays, extremely dense modules are fabricated in UTCS technology [109], which exploits the recent advances in wafer thinning, as well as in attachment, bonding, and interconnection. In UTCS systems, multiple silicon chips thinned down to 10 μmare vertically integrated on a single (inactive) host silicon substrate, being the electrical insulation among them ensured by layers of benzocyclobutene (BCB), a photosensitive polymer with good planarization properties [110–113]; the resulting stack provides larger circuitry integration than in 2-D ICs. Unfortunately, UTCS architectures may be subject to exacerbated thermal effects dictated by (i) the high power density and (ii) the low thermal conductivity of BCB (about 800 times lower than that of silicon), which inhibits the downward heat propagation from the power-dissipating regions to the board [110,111,113]. As a consequence, the potential benefits of stacked architectures can be in principle achieved only by resorting to thermal-aware design techniques based on reliable simulations.

A 2-layer UTCS structure containing two 10-μm-thick silicon chips, is depicted in Fig. 2.17. The upper (2^{nd}-level) chip is vertically insulated from the buried (1^{st}-level) one by a BCB planarization layer; the lower chip is attached to the host silicon substrate by an adhesive BCB layer. The power-dissipating circuitries lie on the top of the chips. The substrate backside is soldered to the AlN package header by a Pb/Sn conductive grease. The header is assumed to be in close contact with the board at ambient temperature ($T_{\text{board}} = T_0$). The horizontal and vertical dimensions of the module are reported in Table 2.1, and

the parameters of the materials in Table 2.2. Adiabatic top and lateral faces of the domain are assumed, which is reasonable due to the small influence of natural convection [114]. It is noted that only one quarter of the structure can be considered, the missing portion being virtually recreated by applying adiabatic BCs over the planes of symmetry.

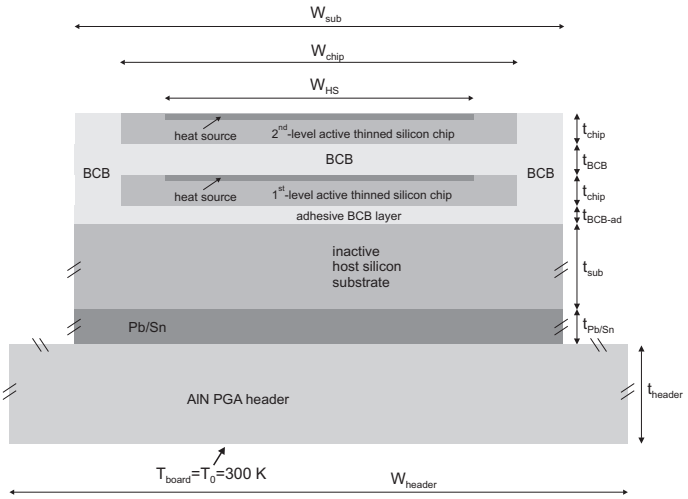


Fig. 2.17. Cross-section of the stacked two-chip UTCS module under test (not to scale).

Table 2.1. Values of the geometrical parameters indicated in Fig. 2.17.

Parameter	Value [μm]
W_{header}	15 000
W_{sub}	6 200
W_{chip}	5 620
W_{HS}	4 240
t_{chip}	10
t_{BCB}	10
$t_{\text{BCB-ad}}$	3
t_{sub}	500
$t_{\text{Pb/Sn}}$	50
t_{header}	760

Table 2.2. Values of the material parameters.

Material	ρ [kg/μm^3]	c [J/kgK]	k [W/μmK]
Si [4, 115, 116]	$2.330 \cdot 10^{-15}$	711	$1.48 \cdot 10^{-4}$
BCB [110, 117]	$1.051 \cdot 10^{-15}$	1 267	$1.80 \cdot 10^{-7}$
Pb/Sn [118]	$11.200 \cdot 10^{-15}$	137	$0.36 \cdot 10^{-4}$
AlN [119]	$3.260 \cdot 10^{-15}$	748	$1.50 \cdot 10^{-4}$

The thermal impedances vs. time Z_{TH11}, Z_{TH22}, and Z_{THm} were evaluated via 3-D thermal-only COMSOL simulations [41] by alternately activating the stacked silicon chips. The mesh, a detail of which is depicted in Fig. 2.18, was rather cumbersome to generate due to the presence of layers with thickness much lower than (i) horizontal dimensions, and (ii) thicknesses of other layers; it was created with smart selective refinement strategies – available in the recent software releases – and includes more than 1 million elements (tetrahedra), involving about 1.5 million DoFs. The numerical simulation of a transient thermal impedance over 2000 logarithmically-spaced time instants was found to last nearly 7 hours on a workstation equipped with 2 hexacore 2.43 GHz CPUs and a 100 GB RAM.

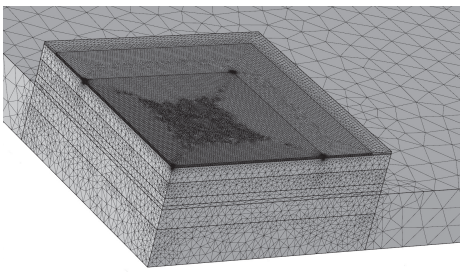


Fig. 2.18. Detail of the COMSOL mesh corresponding to the analyzed UTCS structure.

The identification and synthesis was performed according to the flow chart in Fig. 2.19. The full time-constant spectrum of the thermal impedances was computed by NID as described in Section 2.3.6. In particular, ~650 RC time constants were evaluated at this stage. By exploiting VF, 11 poles were demonstrated to be enough to achieve a very good accuracy. This procedure was performed without the need for real-pole enforcement, since no complex-conjugate poles appeared when representing thermal impedances obtained through detailed 3-D FEM simulations, although exceptions are expected if significant numerical or experimental noise affects the input impedance data;

in this case, proper pre-processing filtering or real-pole enforcement techniques are to be employed. By employing PFVF (Section 2.3.3), a Multi-port TFB (see Section 2.4.2) was determined for the structure under analysis.

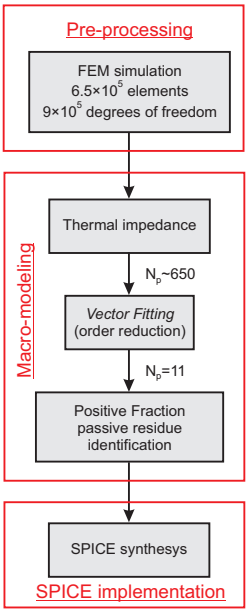


Fig. 2.19. Procedure based on PFVF for the TFB extraction as adopted in this Section.

Fig. 2.20 depicts the time evolution of the thermal impedances, as obtained by FEM simulations, the 11-pole synthesis, and a single-time-constant representation. An excellent agreement is achieved between numerical and 11-pole data. It is noteworthy that the thermal impedance of the top (2^{nd}) chip is higher than that of the buried (1^{st}) one, which is closer to the board kept at ambient temperature.

Fig. 2.21 shows the results of a PSPICE [39] purely-thermal simulation performed on the synthesized TFB; in particular, two power pulses with different durations and values were applied to the stacked thin silicon chips and the resulting temperature rises over ambient were determined.

Further studies on the UTCS structure have been performed:

- by including the temperature-dependence of the thermal conductivity, as reported in Section 3.3;
- by performing an ET simulation of a signal interconnect line, as described in Section 4.2.

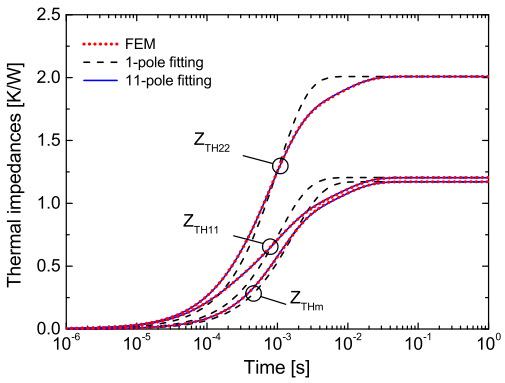


Fig. 2.20. Thermal impedances Z_{TH11}, Z_{TH22}, and Z_{THm}, as obtained by Comsol simulations (dotted lines), 1-pole fitting (dashed), and ll-pole synthesized network (solid).

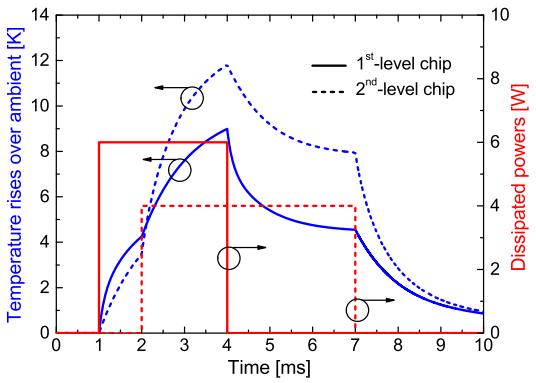


Fig. 2.21. Temperature rises over ambient and dissipated power pulses against time for the two stacked silicon chips, as obtained through a PSPICE simulation of the 11-pole TFB.

Chapter 3

Advanced TFBs and their applications

3.1 Parametric linear TFBs

A *parametric* (or *parameterized*) macromodel allows describing the variation of a thermal impedance matrix $\mathbf{Z}_{TH}$ according to some *design parameters* (e.g., layout and material parameters variations) in a given range of the design space. Parametric macromodels can be obtained from FEM discretization of the heat transfer equation (e.g., [120]), or with a data-driven approach, extending what is reported in Chapter 2 for linear TFBs following [121–125]. The adopted parametric approach:

- recieves as input the $\mathbf{Z}_{TH}(s)$ in the form (2.33) in given fixed points $\mathbf{g}$ of the design space in which the variations are to be explored: the input $\mathbf{Z}_{TH}(s, \mathbf{g}_k)$ are denoted as *root macromodels*, where k is an index denoting a specific point;
- returns as output a parametric macromodel starting from the aforementioned samples $\mathbf{Z}_{TH}(s, \mathbf{g}_k) \rightarrow \mathbf{Z}_{TH}(s, \mathbf{g})$ defined in *all* the points of the design space in a given range, obtained with a suitable interpolation of the root macromodels;
- the accuracy of the parametric macromodel is tested by comparison with *validation macromodels*, i.e. macromodels that have *not* been used to extract $\mathbf{Z}_{TH}(s, \mathbf{g})$ chosen in the points that are most critical for the interpolation.

In order to better describe the approach, we will refer to a specific problem, namely the parametric macromodeling of a High Electron Mobility Transistor

(HEMT).

HEMT introduction and problem definition

HEMTs are unipolar field-effect devices where the current conduction is due to a 2-D electron gas flowing through a low-resistivity thin undoped layer (also referred to as *channel*) located at the junction between two materials with different bandgaps. In this layer, high mobility is reached since the carriers are not subject to collisions with doping impurities and with the Si/SiO_2 lattice discontinuity like in conventional Si transistors. In addition, HEMTs enjoy outstanding properties like high breakdown field and high saturation drift velocity. All these benefits make such devices attractive for a large variety of high-frequency applications where high gain and low noise are required, like radars operating in extreme environments, microwave communications, and radio astronomy [126].

In particular, GaN HEMTs offer the highest output power and are considered the most appealing devices for microwave power amplifiers [127–131]. However, these transistors suffer from ET effects induced by the fast designer-induced growth in current (and power) density related to the higher signal bandwidth requirements for modern communications. The resulting raise in channel temperature reduces the low-field electron mobility, increases the source resistance, and lowers the saturation drift velocity, thereby entailing a distortion in the output characteristics, i.e., a decrease in the drain current for a given bias condition [132–136]. Such effects can be exacerbated in multifinger devices with an improperly-designed layout due to the thermal interactions between individual transistors.

We therefore want to analyze the ET behavior of an 8-finger (i.e., 8-gate) AlGaN/GaN HEMT grown on a 70-μm-thick 6H-SiC layer [137] as a function of the key layout parameters, namely, finger width W and center-to-center spacing (also denoted as *pitch*) L_{GG} between fingers, as depicted in Fig. 3.1: such analysis is devised to improve the thermal ruggedness.

The procedure for the identification of TFB must be in principle performed for any point in the design space. A drastic reduction in such effort can be achieved by using the parameterized macromodeling approach – explained in the following – since it allows determining $\mathbf{Z}_{TH}$ for any point in the design space so as to prevent (i) generating a new mesh and (ii) simulating a new $\mathbf{Z}_{TH}$ for any layout variation.

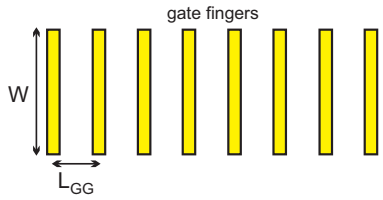


Fig. 3.1. Schematic top-view representation of the HEMT layout illustrating the gate fingers, the gate width W and pitch L_{GG}.

Extraction of a parametric macromodel

The technique presented in [123] (with additional references [121, 122, 124]) allows the generation of a parameterized macromodel $\mathbf{H}_{model}(s, \mathbf{g})$ to accurately represent a set of multidimensional data samples $\{(s_f, \mathbf{g}_k), \mathbf{H}(s_f, \mathbf{g}_k)\}$, which depend on the complex frequency $s = j\omega$ and M_G design variables $\mathbf{g} = (\mathrm{g}^{(m)})_{m=1}^{M_G}$, namely, W and L_{GG} in the aforementioned problem. A parameterized macromodel in a pole-residue form is given by

$$\mathbf{H}_{model}(s, \mathbf{g}) = \mathbf{C}_0(\mathbf{g}) + \sum_{n=1}^{N(\mathbf{g})} \frac{\mathbf{C}_n(\mathbf{g})}{s - p_n(\mathbf{g})} \tag{3.1}$$

where N is the number of poles.

1) Root macromodel extraction

The design space containing all design parameters $\mathbf{g}$ is partitioned into cells using hyperrectangles (regular grids) or simplices (regular and scattered grids) including the *estimation* and *validation* grid. The validation set points are located at the center of the cells of the estimation grid. Fig. 3.2 shows a possible normalizedn 2-D estimation and validation set with rectangular grid cells. Using any frequency-domain method reported in Chapter 2, univariate root macromodels $\mathbf{H}_{model}(s, \mathbf{g}_k)$ are computed at the estimation design space points. It is better to identify *passive* models since the passivity properties can be extendend from the root macromodels to the parametric one under certain assumptions [123].

2) Scaling and frequency shifting coefficient

A local parameterized macromodel is then associated to each cell that is a subdomain of the entire design space. We indicate a cell region of the design space as Ω_i, and the corresponding vertices as $\mathbf{g}_k^{\Omega_i}$. We note that each vertex

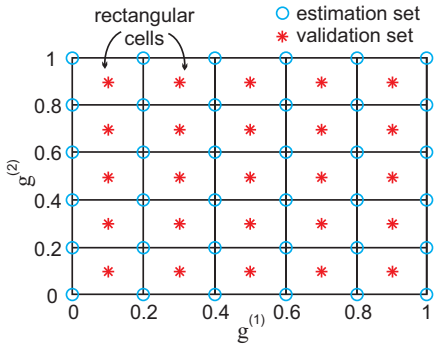


Fig. 3.2. Estimation and validation set with rectangular grid cells (normalized $\mathrm{g}^{(1)}, \mathrm{g}^{(2)}$ are considered).

corresponds to a *root macromodel* $\mathbf{H}_{model}(s, \mathbf{g}_k^{\Omega_i})$. For each cell, an optimization procedure is used to find amplitude and frequency scaling coefficients that make each vertex an accurate approximant of the other cell vertices (an error function to be minimized regulates the quality of this approximation). For each vertex $\mathbf{H}_{model}(s, \mathbf{g}_k^{\Omega_i})$, a set of amplitude $\alpha_{1,k}(\mathbf{g}_j^{\Omega_i}),\ j = 1, \ldots, Q$ and frequency $\alpha_{2,k}(\mathbf{g}_j^{\Omega_i}),\ j = 1, \ldots, Q$ scaling real coefficients are calculated

$$\min_{\alpha_{1,k}(\mathbf{g}_j^{\Omega_i}), \alpha_{2,k}(\mathbf{g}_j^{\Omega_i})} Err(\widehat{\mathbf{H}}_{model}(s, \mathbf{g}_k^{\Omega_i}), \mathbf{H}_{model}(s, \mathbf{g}_j^{\Omega_i})) \tag{3.2}$$

with

$$\widehat{\mathbf{H}}_{model}(s, \mathbf{g}_k^{\Omega_i}) = \alpha_{1,k}(\mathbf{g}_j^{\Omega_i}) \mathbf{H}_{model}(s\alpha_{2,k}(\mathbf{g}_j^{\Omega_i}), \mathbf{g}_k^{\Omega_i}) \tag{3.3}$$

$$\alpha_{1,k}(\mathbf{g}_j^{\Omega_i}) = \alpha_{2,k}(\mathbf{g}_j^{\Omega_i}) = 1,\ j = k \tag{3.4}$$

$$\alpha_{1,k}(\mathbf{g}_j^{\Omega_i}) \geqslant 0 \tag{3.5}$$

$$\alpha_{2,k}(\mathbf{g}_j^{\Omega_i}) > 0 \tag{3.6}$$

(3.5) and (3.5) being needed to build overall passive parametric macromodels [123].

3) Multivariate interpolation of (i) scaling coefficient, and (ii) root macromodels

Multivariate positive interpolation of the scaling coefficient is first performed, obtaining functions in $\mathbf{g}$ starting from the samples, i.e.,

$$\alpha_{1,k}(\mathbf{g}) \rightarrow \alpha_1(\mathbf{g}) \tag{3.7}$$

$$\alpha_{2,k}(\mathbf{g}) \rightarrow \alpha_2(\mathbf{g}) \tag{3.8}$$

Finally, a parametrization is obtained for the root macromodels, and thus the parametric macromodel $\mathbf{H}_{model}(s, \mathbf{g})$ can be obtained. Further details about the parametric macromodeling procedure can be found in [121–124].

Parameterized macromodel for thermal problems

Specifically for *thermal* parametric macromodels, a decomposition of the frequency-domain data samples of $\mathbf{Z}$ was presented to enhance the modeling accuracy and limit the computational cost of the simulations needed for the macromodel generation, extending [125, 138].

Considering the set of thermal impedance matrices at the estimation points $\mathbf{Z}(s_f, \mathbf{g}_k)$, the corresponding DC value $\mathbf{R}(\mathbf{g}_k)$ is extracted and the initial impedance data samples are pre-processed as

$$\widehat{\mathbf{Z}}(s_f, \mathbf{g}_k) = \mathbf{Z}(s_f, \mathbf{g}_k) \circ \mathbf{G}(\mathbf{g}_k) \tag{3.9}$$

where $\circ$ denotes the Hadamard product [139] (entrywise product of two matrices of the same size) and $\mathbf{G}(\mathbf{g}_k)$ is the Hadamard inverse of the matrix of thermal resistances $\mathbf{R}(\mathbf{g}_k)$ and therefore each of its entries is

$$G_{ij}(\mathbf{g}_k) = (R_{ij}(\mathbf{g}_k))^{-1} \tag{3.10}$$

The matrix $\mathbf{R}$ is real, symmetric with all positive elements and positive definite. Two macromodels are generated, $\widehat{\mathbf{Z}}_{model}(s, \mathbf{g})$ and $\mathbf{R}_{model}(\mathbf{g})$ starting from the data samples $\widetilde{\mathbf{Z}}(s_f, \mathbf{g}_k)$ and $\mathbf{R}(\mathbf{g}_k)$, respectively. $\mathbf{R}_{model}(\mathbf{g})$ does not depend on frequency and therefore a parameterized macromodel can be built using standard interpolation/approximation models (e.g., radial basis functions, polynomials, splines, etc.). Once both macromodels are generated, the model $\mathbf{Z}_{model}(s, \mathbf{g})$ representing the original thermal impedance data samples can be expressed as

$$\mathbf{Z}_{model}(s, \mathbf{g}) = \widehat{\mathbf{Z}}_{model}(s, \mathbf{g}) \circ \mathbf{R}_{model}(\mathbf{g}) \tag{3.11}$$

Considering a pole-residue form for $\widehat{\mathbf{Z}}_{model}(s, \mathbf{g})$

$$\widehat{\mathbf{Z}}_{model}(s, \mathbf{g}) = \mathbf{C}_0(\mathbf{g}) + \sum_{n=1}^{N(\mathbf{g})} \frac{\mathbf{C}_n(\mathbf{g})}{s - p_n(\mathbf{g})} \tag{3.12}$$

then (3.11) can be written as

$$\mathbf{Z}_{model}(s, \mathbf{g}) = \mathbf{C}_0(\mathbf{g}) \circ \mathbf{R}_{model}(\mathbf{g}) + \sum_{n=1}^{N(\mathbf{g})} \frac{\mathbf{C}_n(\mathbf{g}) \circ \mathbf{R}_{model}(\mathbf{g})}{s - p_n(\mathbf{g})} \tag{3.13}$$

It is worth remarking that this data decomposition is important for two main reasons:

- it allows enhancing the accuracy of the macromodel;
- the sampling in the design space to get dynamic and steady-state thermal response data samples can be decoupled, which helps reduce the overall computational cost to build a parameterized macromodel.

The workflow for the extraction of the parameterized macromodel can be summarized as follows:

- First, the thermal impedance matrices corresponding to the estimation and the validation points are computed through 3-D FEM transient simulation with logarithmically spaced time samples so as to capture the full evolution of the heat conduction.
- The full time-constant spectrum of the thermal impedances is achieved through NID: the time-domain data are thus converted into frequency-domain data.
- The frequency-domain data are identified using VF [70, 72], by which reduced-order root macromodels with around 20 poles are derived for each grid node.
- The parameterized macromodel is then obtained, and its accuracy checked with the validation data.

8-finger GaN HEMT parametric macromodeling and ET simulation

The 3-D FEM simulations have been performed with the commercial tool Comsol Multiphysics [41], with each channel associated to a thin heat source (THS). In our analysis, W is varied in the range 75 μm to 150 μm, while L_{GG} spans from 15 μmto 45 μm. From a thermal viewpoint, W mainly influences the self-heating thermal impedances, whereas L_{GG} mainly impacts the mutual impedances between fingers; it is worth noting that from the electrical point of view a variation in W modifies also the current handling capability of the whole device, which is instead independent of L_{GG}. Fig. 3.3 illustrates a portion of the Comsol grid corresponding to the device under test for W=75 μm and L_{GG}=30 μm. The number of elements (tetrahedra) is almost layout-independent, and amounts to about 2.5×10^5. The evaluation of the dynamic temperature field within the whole structure due to the activation of a single HS required about 3 hours on a workstation equipped with 2 hexa-core Intel Xeon E7450 CPUs and 100 GB RAM. Exploiting the structure symmetry, only 4 transient simulations were needed to compute the thermal impedance matrix for a given layout configuration, which led to a total of about 12 hours. The

dynamic estimation grid comprises the following 9 points: (W, L_{GG})=(75, 15), (75, 30), (75, 45), (112.5, 15), (112.5, 30), (112.5, 45), (150, 15), (150, 30), (150, 45) μm. The *static estimation grid* comprises 12 additional points: (W, L_{GG})=(75, 22.5) (75, 37.5), (93.75, 15), (93.75, 30), (93.75, 45), (112.5, 22.5), (112.5, 37.5), (131.25, 15), (131.25, 30), (131.25, 45), (150, 22.5), (150, 37.5) μm, the simulation of which required only 20 minutes for each point. The 4 *validation points* needed to assess the model accuracy over design space points not used for its generation, are (W, L_{GG})=(93.75, 22.5), (93.75, 37.5), (131.25, 22.5), (131.25, 37.5) μm. Once the parameterized macromodel has been extracted, the CPU time needed to perform a time-domain simulation of the thermal impedance matrix for assigned geometrical parameters is only 0.22 s on a normal PC equipped with an Intel Core2 Extreme CPU Q9300 2.53GHz and 8 GB RAM, with a significant gain compared to the time/memory required by a conventional approach.

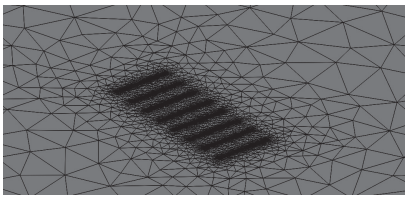


Fig. 3.3. Comsol mesh for the multi-gate HEMT under test with W=75 μmand L_{GG}=30 μm.

In order to fully characterize the accuracy of the proposed approach, the following errors were suitably defined:

- relative error exluding short times which are less relevant for ET simulations

$$Err_{rel}(Z_{ij}) = \max_t \left[100 \cdot \left| \frac{Z_{ij}(t) - Z_{ij,model}(t)}{Z_{ij}(t)} \right| \right] \qquad (3.14)$$

$$\text{for } t \geqslant t^*, Z_{ij}(t^*) = 0.3R_{ij}$$

- normalized relative error with respect to the steady-state values

$$Err_{norm}(Z_{ij}) = \max_t \left[100 \cdot \left| \frac{Z_{ij}(t) - Z_{ij,model}(t)}{Z_{ij}(t)} \right| \right] \cdot \frac{R_{ij}}{R_{max}} \qquad (3.15)$$

$$\text{for } t \geqslant t^*, Z_{ij}(t^*) = 0.3R_{ij}\,,\ R_{max} = \max_{ij}(R_{ij})$$

- steady-state relative and normalized relative errors: equations (3.14) and (3.15) , respectively, for $t \to \infty$

Fig. 3.4 depicts the comparison between the FEM data and the macromodel output at the estimation points (a) for the self-heating term $Z_{11}(t)$ at L_{GG}=30 µm and W=75, 112.5, 150 µm, and (b) for the mutual impedances $Z_{12}(t)$ and $Z_{13}(t)$ at W=112.5 µm and L_{GG}=15, 30, 45 µm.

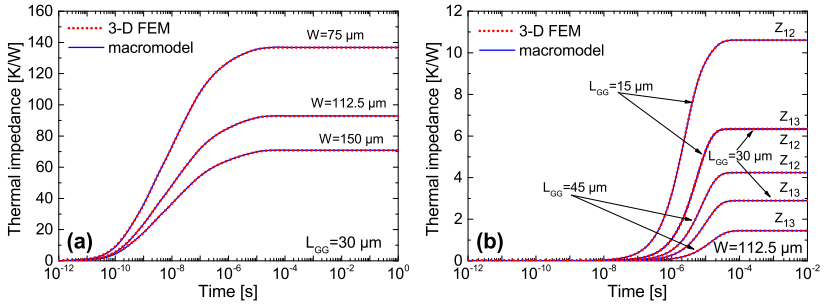


Fig. 3.4. Comparison between 3-D FEM (dotted lines) and macromodel results (solid) at the estimation points: (a) self-heating thermal impedance $Z_{11}(t)$ for transistors with L_{GG}=30 µm and W=75, 112.5, 150 µm; (b) mutual thermal impedances $Z_{12}(t)$ and $Z_{13}(t)$ for transistors with W=112.5 µm and L_{GG}=15, 30, 45 µm.

Fig. 3.5 shows a similar comparison for the validation points, depicting (a) $Z_{11}(t)$ at L_{GG}=22.5 µm and W=93.75, 131.25 µm, and (b) $Z_{12}(t)$ and $Z_{13}(t)$ at W=131.25 µm and L_{GG}=22.5, 37.5 µm.

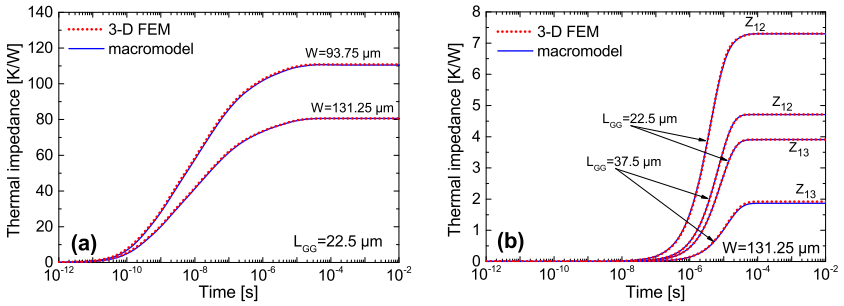


Fig. 3.5. Comparison between 3-D FEM (dotted lines) and macromodel results (solid) at the validation points: (a) self-heating thermal impedance Z_{11}(t) for transistors with L_{GG}=22.5 µm and W=93.75, 131.25 µm; (b) mutual thermal impedances Z_{12}(t) and Z_{13}(t) for transistors with W=131.25 µm and L_{GG}=22.5, 37.5 µm.

In spite of the coarseness of the estimation grid, the macromodel exhibits a good agreement with the input data, and the maximum values of the previously defined errors at all validation points are reported in Tab. 3.1. The correspond-

ing errors at the estimation points assume lower values than in Tab. 3.1, which is expected since the estimation points are used to generate the parameterized macromodel.

Table 3.1. Parameterized macromodel validation errors

Error definition	Value
Relative error (3.14)	10.8%
Normalized relative error (3.15)	2.75%
Steady-state relative error	10.4%
Steady-state normalied relative error	0.29%

The parameterized macromodel output is illustrated in Fig. 3.6, which shows the dependence of $Z_{11}(t)$ upon W for L_{GG}=30 µm, and of $Z_{12}(t)$ upon L_{GG} for W=112.5 µm.

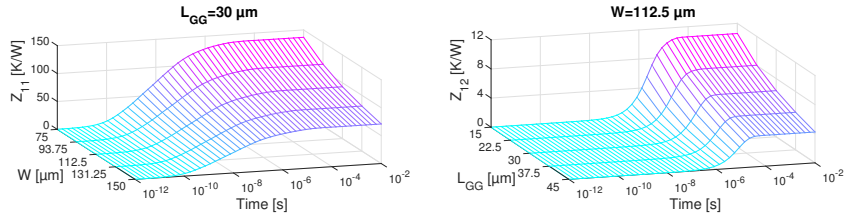


Fig. 3.6. Parameterized macromodel output for (left) self-heating thermal impedance $Z_{11}(t)$ as a function of time and W, and (right) mutual thermal impedance $Z_{12}(t)$ as a function of time and L_{GG}.

The dynamic ET simulations of the device under test were performed through PSPICE [39] by exploiting the strategy described in Section 1.2, with electrical macromodeling built according to [140]. The device was biased by applying V_{GS}=0 V and a 200 kHz V_{DS}=30 V pulse train with a 20% duty cycle. Simulations were very fast (a CPU time amounting to a few seconds was needed to analyze the device behavior over a time range of hundreds of µs) and no convergence issues were encountered in spite of the sharp edges of the pulses. Fig. 3.7 reports the temperature rise of the hottest finger for various layout configurations by keeping constant (a) the gate width W, and (b) the pitch L_{GG}. Results can be summarized as follows. The temperature peak becomes lower with increasing L_{GG} (Fig. 3.7a) since the thermal coupling between gate fingers decreases. A less intuitive behavior is obtained by increasing W (Fig. 3.7b): the higher current handling capability due to the larger finger area is effectively counteracted by the reduction in self-heating thermal impedances, and only a marginal temperature growth is observed.

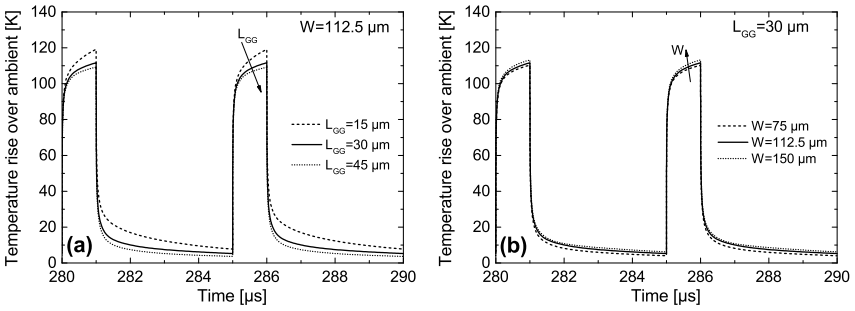


Fig. 3.7. ET simulation of a 8-finger HEMT biased with V_{GS}=0 V and a 200 kHz V_{DS}=30 V pulse train with a 20% duty cycle: temperature rise over ambient for the hottest finger at various layout configurations (a) at fixed W, and (b) at fixed L_{GG}.

3.2 FANTASTIC – a tool for model-order reduction-based TFBs

3.2.1 Tool flow-chart

An advanced category of linear TFBs is the one relying upon the Multi-Point Moment Matching (MPMM) algorithm by L. Codecasa [50, 51, 141–151]. Fig. 3.8 depicts the schematic flow-chart of the tool denoted as FAst Novel Thermal Analysis Simulation Tool for Integrated Circuits (FANTASTIC).

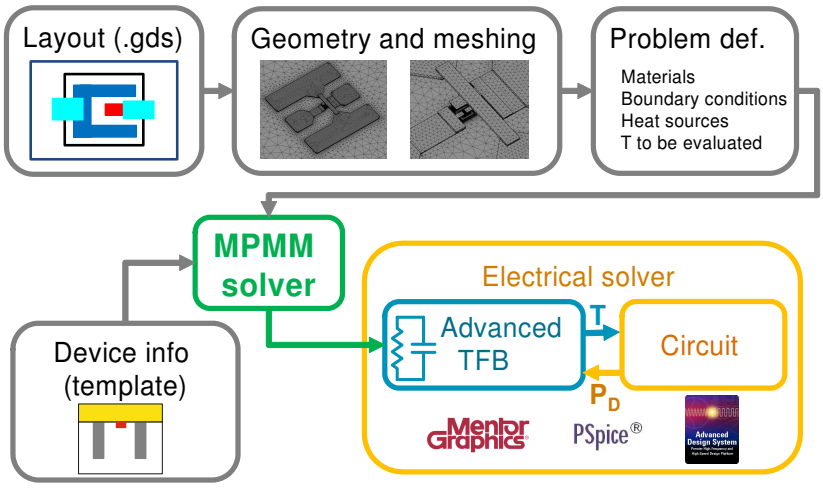


Fig. 3.8. Schematic flow-chart of the MPMM tool denoted as FANTASTIC.

FANTASTIC receives as input the DUT layout mask data and technological process information (e.g., thicknesses, mask biases) building the 3-D geometry with a custom script, exploiting Griesmann's GDS II Libraries [152]. The subsequent meshing is then performed with Comsol [41], or for simpler cases with the open source tool Salome [153]. The thermal problem is defined through the material parameters, the BCs, the HSs and the region where the temperature is to be evaluated. An alternative input possibility is given by the use of a simplified *template*, i.e., a very basic geometric structure (e.g., a trench-isolated transistor) completed with a small set of parameters provided by the user. In this way simple thermal analyses can be performed requiring no knowledge of thermal simulations.

FANTASTIC allows the performance of exceptionally fast dynamic thermal and ET analyses of integrated semiconductor devices. First, a FEM model

of the thermal problem is assembled by the tool starting from an input tetrahedral or Cartesian mesh. Then a Dynamic Compact Thermal Model (DCTM) is constructed, which, unlike other approaches, does not require brute-force transient thermal simulations. The overall computational complexity for the extraction and simulation of the DCTM is, in terms of CPU time and memory storage, much lower than that needed by the best available commercial FEM codes to carry out an accurate transient simulation for the same domain.

The achieved DCTM is then reformulated in a novel efficient Foster-like TFB. Thermal and ET simulations using such DCTM typically imply 4-5 orders of magnitude gains in CPU time and memory storage compared to the direct use of the FEM model. Moreover, no information is lost passing from the FEM model to the TFB constructed by the MPMM method, since after the thermal or ET simulation, the whole space-time distribution of the temperature rise and heat flow within the device can be reconstructed in a post-processing stage.

3.2.2 MPMM algorithm

Fig. 3.9 shows a simplified description of the MPMM algorithm.

First, the linear dynamic heat diffusion problem is imported, comprising: the mesh discretizing the geometry, the definitions of materials, boundary conditions and HSs. Parallelepipedal and tetrahedral meshes can be used. Arbitrary heat capacity and tensorial thermal conductivity distributions can be defined. Neumann's, Dirichlet's, or Robin's boundary conditions can be applied, and THS or VHS can be accounted for.

Secondly, the FEM is adopted for discretizing the heat diffusion problem (2.1). In particular the mass matrix $\mathbf{M}$ and the stiffness matrix $\mathbf{K}$ of the problem are constructed. High-order basis functions can be used: in particular second-order functions were used – as it is standard in Comsol –since first-order basis functions were shown to lead to insufficient accuracy. The degrees of freedoms (DoFs) of the temperature rise distribution, forming the N-row vector $\mathbf{x}(t)$, are solution to the *discretized* linear dynamic heat diffusion problem

$$\mathbf{M}\frac{d\mathbf{x}}{dt}(t) + \mathbf{K}\mathbf{x}(t) = \mathbf{g}(t), \tag{3.16}$$

in which the HS vector is

$$\mathbf{g}(t) = \mathbf{G}\mathbf{P}(t), \tag{3.17}$$

being $\mathbf{P}(t)$ the n-row vector of port powers, and G the $N \times n$ matrix, the n columns $\mathbf{g}_i$ of which are the port power density distributions. The port tem-

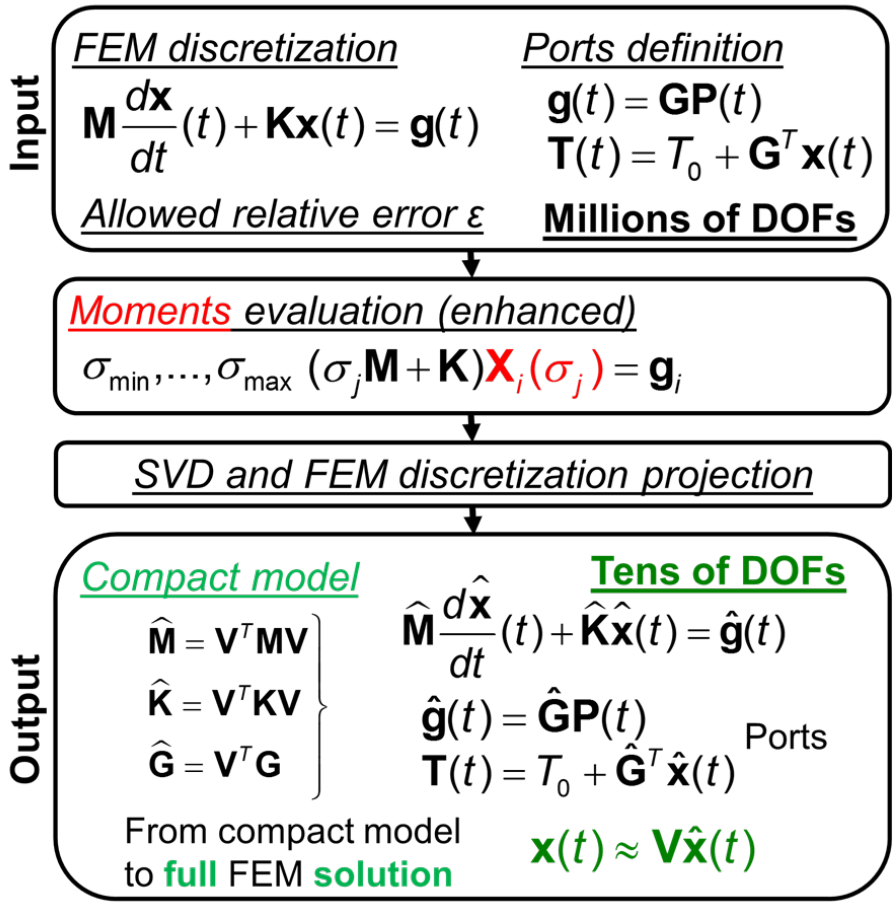


Fig. 3.9. Simplified flow chart of the MPMM algorithm.

peratures form the n-rows column vector $T(t)$, defined as [144]

$$\mathbf{T}(t) = T_0 + \mathbf{G}^T\mathbf{x}(t), \tag{3.18}$$

The discrete dynamic heat diffusion problem, which is a system of ordinary differential equations (ODEs), is *not* directly solved. Instead a DCTM is constructed by an enhanced version of the MPMM algorithm [144, 154]. In its basic form, the following dynamic heat diffusion problems are solved *in the complex frequency domain*

$$(\sigma_j\mathbf{M} + \mathbf{K})\mathbf{X}_i(\sigma_j) = \mathbf{g}_i \tag{3.19}$$

for a tiny number of real positive values σ_j of the complex frequency, thus evaluating with $i = 1, \ldots, n$ and $j = 1, \ldots, m$. The values σ_j of the complex frequency are *automatically determined on the real positive axis as a function of the desired relative error* ε as follows [154]. First, the minimum eigenvalue λ and maximum eigenvalue Λ of the discrete dynamic heat diffusion problem (3.16) have to be estimated. Next, the number m is determined as the smallest integer such that

$$4\exp(-m\pi^2/\log(4/k')) \leqslant \varepsilon, \tag{3.20}$$

being $k' = \lambda/\Lambda$. The complex frequencies are then given by

$$\sigma_j = \Lambda \mathrm{dn}\left[\frac{2j-1}{2m}K, k\right], \tag{3.21}$$

with $j = 1, \ldots, m$, in which K is the complete elliptic integral of first kind of modulus k, dn is the homonymous elliptic function of modulus k and $k = \sqrt{1-k'^2}$.

Lastly, by orthonormalizing vectors $\mathbf{X}_i(\sigma_j)$, with $i = 1, \ldots, n$ and $j = 1, \ldots, m$, an $N \times \hat{n}$ matrix of *moments* $\mathbf{V}$ is derived, that is used for projecting (3.16) – (3.18) and defining the DCTM, which results in

$$\widehat{\mathbf{M}}\frac{d\hat{\mathbf{x}}}{dt}(t) + \hat{\mathbf{K}}\hat{\mathbf{x}}(t) = \hat{\mathbf{g}}(t), \tag{3.22}$$

and

$$\hat{\mathbf{g}}(t) = \widehat{\mathbf{G}}\mathbf{P}(t), \tag{3.23}$$

$$\mathbf{T}(t) = T_0 + \widehat{\mathbf{G}}^T\hat{\mathbf{x}}(t) \tag{3.24}$$

where

$$\widehat{\mathbf{M}} = \mathbf{V}^T\mathbf{M}\mathbf{V}, \tag{3.25}$$

$$\hat{\mathbf{K}} = \mathbf{V}^T\mathbf{K}\mathbf{V}, \tag{3.26}$$

$$\widehat{\mathbf{G}} = \mathbf{V}^T \mathbf{G}. \tag{3.27}$$

and being $\widehat{\mathbf{g}}_i$ the n columns of matrix $\widehat{\mathbf{G}}$. Such DCTM allows approximating both the port temperatures T(t) and the whole space-time temperature distribution as

$$\mathbf{x}(t) \approx \mathbf{V}\hat{\mathbf{x}}(t). \tag{3.28}$$

It is worth noting that:

- The solution of (3.19) to determine the matrix of moments entails the solution of a small number of *linear systems*, which can be solved very quickly by suitably choosing the numerical algorithms exploiting the system properties (sparse, banded).
- The DCTM is a *compact* model in the sense that is a system of ODEs in the same form of the starting model, but requiring *tens* of DoFs instead of *millions*.
- Yet, no information is lost since from (3.28) is possible to recover the solution of the full FEM problem starting from the solution of the compact model.

The basic form of the MPMM algorithm provides the desired level of accuracy. Extending [144], it can be indeed rigorously proven an upper bound for the error of the thermal impulse matrices

$$\left\| \mathbf{Z}_{TH,impulse}(t) - \hat{\mathbf{Z}}_{TH,impulse}(t) \right\| \leqslant \varepsilon \left\| \mathbf{Z}_{TH,impulse}(t) \right\|, \tag{3.29}$$

in which

$$\left\| \mathbf{Z}_{TH,impulse}(t) \right\| = \sqrt{\int_0^{+\infty} \mathrm{tr}(\mathbf{Z}_{TH,impulse}^T(t)\mathbf{Z}_{TH}, impulse(t))\, dt}. \tag{3.30}$$

Similar results can be extended from the time to the frequency domain and can be stated for the whole space-time temperature distributions due to power impulses. They provide a strong theoretical guarantee for the convergence of the method. Moreover this convergence is very fast being exponential with respect to the number m of the determined complex frequencies, as a consequence of (3.20). As a result, in practice accurate DCTMs can always be obtained with small state-space dimensions. The MPMM algorithm efficiency can be further enhanced by fine-tuning of the numerical solution of the very few needed heat diffusion problems in the complex frequency domain, as detailed in Algorithm 1 [154].

Algorithm 1: Enhanced Multi-Point Moment Matching [154].

Set the relative error ϵ
for $i = 1, \ldots, n$ **do**
  Set the linear space $\mathcal{S}_0 = \varnothing$
1 Estimate the minimum eigenvalue λ_i and the maximum eigenvalue Λ_i
2 Determine the m_i complex frequencies $\sigma_1 > \sigma_2 \ldots \sigma_{m_i-1} > \sigma_{m_i}$
  for $j = 1, \ldots, m_i$ **do**
    if $j > 1$ **then**
3 Compute an approximation of $\mathbf{X}_i(\sigma_j)$ by using the compact thermal model $\mathcal{C}_{j-1}$
4 Solve the discrete dynamic heat diffusion problem at complex frequency σ_j for $\mathbf{X}_i(\sigma_j)$
5 Generate an orthonormal basis, forming the columns of matrix $\mathbf{V}_j$, spanning the linear space $\mathcal{S}_j$ spanned by $\mathcal{S}_{j-1}$ and $\mathbf{X}_i(\sigma_j)$
6 Generate the compact thermal model $\mathcal{C}_j$ by projecting the discrete heat diffusion equations onto the space $\mathcal{S}_j$
  Append the columns of $\mathbf{V}_{m_i}$ to the columns of matrix $\mathbf{V}$
7 Apply Singular Value Decomposition to $\mathbf{V}$
Project the discrete heat diffusion equations onto the space spanned by the columns of $\mathbf{V}$

3.2.3 Synthesis of advanced linear TFBs

By solving a generalized eigenvalue problem at negligible cost, the transformation of variables

$$\hat{\mathbf{x}}(t) = \hat{\mathbf{Q}}\hat{\xi}(t), \tag{3.31}$$

can be determined such that

$$\hat{\mathbf{Q}}^T\hat{\mathbf{M}}\hat{\mathbf{Q}} = \mathbf{1}_{\hat{n}}, \tag{3.32}$$

$$\mathbf{Q}^T\hat{\mathbf{K}}\hat{\mathbf{Q}} = \hat{\mathbf{\Lambda}}, \tag{3.33}$$

$$\hat{\mathbf{Q}}^T\hat{\mathbf{G}} = \hat{\mathbf{\Gamma}}, \tag{3.34}$$

in which $\hat{\mathbf{\Lambda}}$ is a diagonal matrix. With this change of variables the DCTM defined by (3.22) – (3.24) can be rewritten in the equivalent form

$$\frac{d\hat{\xi}}{dt} + \hat{\mathbf{\Lambda}}\hat{\xi}(t) = \hat{\mathbf{\Gamma}}\mathbf{P}(t), \tag{3.35}$$

$$\mathbf{T}(t) = \hat{\mathbf{\Gamma}}^T\hat{\xi}(t). \tag{3.36}$$

which allows approximating the relation among the port variables and reconstructing the DoFs of the FEM model in the form

$$\mathbf{x}(t) \approx \mathbf{V}\hat{\mathbf{Q}}\hat{\xi}(t). \tag{3.37}$$

The novel TFB, sketched in Fig. 3.10, is well-suited to be solved by means of MNA, as in SPICE-like circuit simulators, since all circuit elements are VCCS thus limiting the number of variables to $n + \hat{n}$. The depicted topology, which fully describes the thermal behavior of an electronic device, circuit or system, is general and can be implemented into any circuit simulator such as e.g., PSPICE, ELDO, LTSPICE, Agilent Advanced Design System (ADS); in order to achieve better performance, circuit simulator-specific commands can be employed.

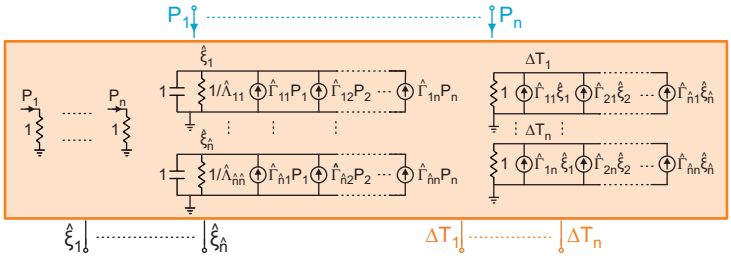


Fig. 3.10. Proposed equivalent TFB provided by FANTASTIC.

After the circuit simulation, as a post-processing stage, the whole space-time distribution of temperature rise can be reconstructed at negligible computational cost and memory storage, for both thermal and ET simulations, using (3.31). The output can then be plotted and analyzed with Paraview [155].

3.2.4 Dynamic thermal simulation of GaAs single-finger and multi-finger HBTs

Hereinafter, a purely-thermal parametric analysis of single-finger and multi-finger HBTs manufactured by RFMD [154, 156] with BiFET and HBT-only processes [157] is performed with FANTASTIC. Fig. 3.11 shows a simplified cross-section of a single-finger transistor. In BiFET devices, the additional pHEMT layers (that include an InGaP etch-stop and InGaAs channel) are located beneath the HBT, while in the HBT-only counterparts they are absent. It is worth noting that materials constituting pHEMT layers suffer from low thermal conductivity compared to GaAs. Both transistor categories are mesa isolated. The DUTs can be contacted using two different approaches, one involving first metal (0.74 μm Au), and another first metal with top metal (TM, 2.74 μm Au).

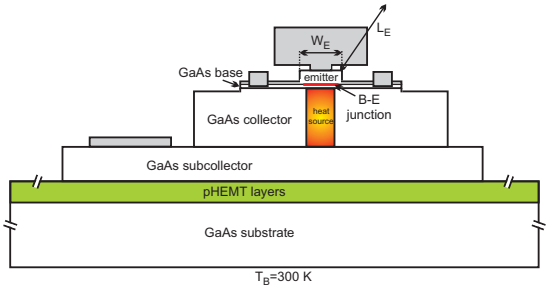


Fig. 3.11. Cross-section of a BiFET HBT under test evidencing the effective emitter width W_E and length L_E, as well as the heat source geometry.

Fig. 3.11 also shows the details of the thermal problem:

- heat dissipation occurs in the fully-depleted collector region; the thickness of the heat source is assumed to be that of the collector, while the horizontal size is slightly lower than the emitter one;
- the temperature is evaluated at the base-emitter junction;
- the bottom is assumed to be isothermal; this corresponds to the contact with an ideal baseplate at fixed temperature, which is the typical operating condition for the R_{TH} measurement;

- all the other surfaces are assumed adiabatic, i.e., the heat flow through them is negligible;
- widely accepted literature values were employed for the material parameters, including binary and ternary alloys as reported in [119, 158]; in particular, k=0.44$\times 10^{-4}$ W/µmK, c=322 J/KgK, ρ=5.32$\times 10^{-15}$ Kg/µm^3 were chosen for GaAs.

A commercial FEM program was used to generate the 3-D mesh for each device; the top-view of the mesh corresponding to the $\mathrm{W_E} \times \mathrm{L_E} = 2 \times 3.5$ µm^2 BiFET DUT is illustrated in Fig. 3.12. The number of tetrahedra for an HBT spans from 10^6 (for the shortest-emitter devices) to 1.5×10^6 (for the longest). The TFB extraction was found to require 7.5 min, with a further 1s for the transient step response $Z_{TH}(t)$ computation by using a fine discretization for the time axis, with 1 GB RAM occupation on a PC with a single i7-3820QM (quad core) 2.70 GHz CPU and 32 GB RAM; conversely, more than 8 hours and approximately 10GB RAM are needed when resorting to a traditional FEM solver.

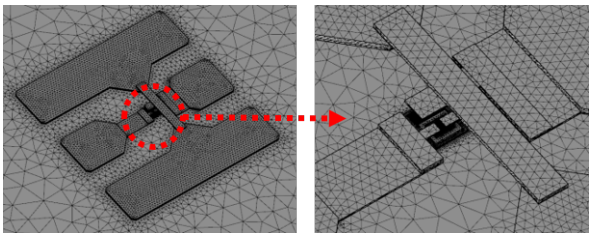


Fig. 3.12. Top-view of the mesh corresponding to the BiFET device with $\mathrm{W_E} \times \mathrm{L_E} = 2 \times 3.5$, and magnification of the mesa region.

Fig. 3.13 shows good matching between the experimental R_{TH} values extracted by resorting to the procedure in [159] and those computed by FANTASTIC for BiFET transistors with $\mathrm{W_E} = 2$ µm as a function of $\mathrm{L_E}$.

Fig. 3.14 shows Z_{TH} vs. time of BiFET HBTs with $\mathrm{W_E} = 2$ µm and various $\mathrm{L_E}$; a comparison with a few curves obtained for $\mathrm{W_E} = 1.6$ µm transistors evidences that the thermal performance degradation induced by the smaller mesa and heat source is exacerbated for shorter emitters. The figure also illustrates that an unacceptable inaccuracy arises when describing Z_{TH} with a single RC pair, while a good representation can be obtained by using at least 7-8 pairs e.g., by using the methods in Section 2.3.1: however, in this case, the information over the computational domain will be lost.

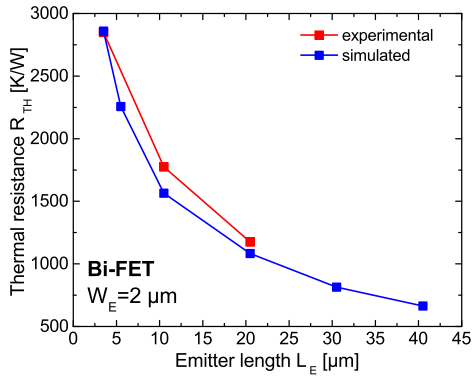


Fig. 3.13. Simulated (open squares) and experimental (filled) thermal resistance R_{TH} vs. emitter length L_E for devices sharing $W_E = 2\,\mu m$.

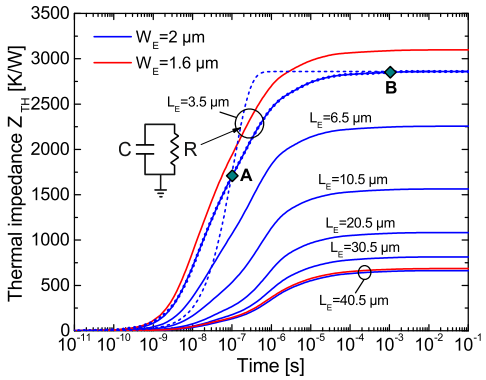


Fig. 3.14. Simulated thermal impedance $Z_{TH}(t)$ for transistors with W_E=2µm and various lengths L_E (blue), along with the curves corresponding to W_E =1.6 µm devices with L_E=3.5 and 40.5 µm (red). Also shown for the case L_E =3.5 µm is the Z_{TH} that would be obtained by using a single-pole representation with an optimized thermal capacitance (blue dot-dashed), and a Foster network with 7 RC pairs (blue dotted). A and B identify the operating points at which the temperature maps shown in Fig. 3.15 are taken.

FANTASTIC can be also used to gain an insight into the heat propagation within the structure. Fig. 3.15 depicts the distribution of the temperature rise over ambient normalized to the dissipated power (i.e., the Z_{TH} field) for the active region of the 2×3.5 μm^2 HBT at the time instants A and B indicated in Fig. 3.14, corresponding to 0.1 μs and 1 ms after the application of the power step, respectively, as computed by the FANTASTIC post-processing [155]. The heat propagation – analyzed through the observation of various temperature maps taken at time instants between A and B – can be described as follows. At point A the heat is still mostly confined within the mesa; afterward, it follows two paths to reach the backside metal (assumed to be an ideal thermal ground); in particular:

- the downward heat flow crosses the pHEMT layers and the GaAs substrate;
- the upward heat spreads into the whole metallization (including the pads), and then enters the substrate through a thin SiN layer on which the pads are sitting; this means that a *parasitic thermal shunt effect* takes place, which contributes to mitigate the junction temperature.

At point B, the temperature field is close to the steady-state conditions. It can be seen that the mesa is still much hotter than the surrounding regions.

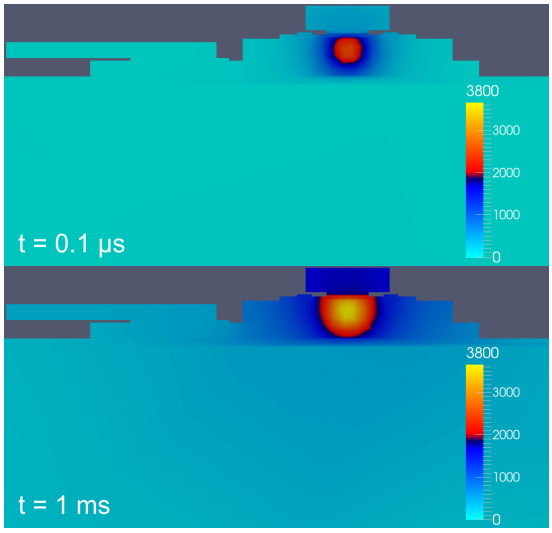


Fig. 3.15. Spatial distribution of the temperature rise above ambient normalized to the dissipated power [K/W] over a section vertically crossing the center of the heat source, as determined by FANTASTIC for the BiFET device with $W_E \times L_E$ =2×3.5 μm^2 at the operating points A and B indicated in Fig. 3.14.

Fig. 3.16 compares the Z_{TH} of BiFET DUTs with alternative variants, namely, HBT-only devices without pHEMT layers, TM structures, and BiFET with base-collector mesa reduced in width and length (in particular, the top mesa layer is shrunk by 1.7 and 1.3 μmalong W_E and L_E, respectively), the geometry of the HS being held fixed. An inspection of the curves reveals that:

1. in BiFET HBTs the heat flowing to the backside hits the pHEMT layers after 0.1 μs;
2. after that time, the impedance for the HBT-only DUTs can be reviewed as a downward-shifted version of the BiFET one. In particular, R_{TH} reduces by 5.5-6.5% regardless of the emitter length;
3. as far as TM transistors are concerned, it was found that R_{TH} decreases by 7-9% in comparison to the BiFET counterparts, thanks to the improved metal path for the upward heat;
4. merely shrinking the base-collector mesa increases R_{TH} by about 7% for the short-emitter device, with little impact on the longer one.

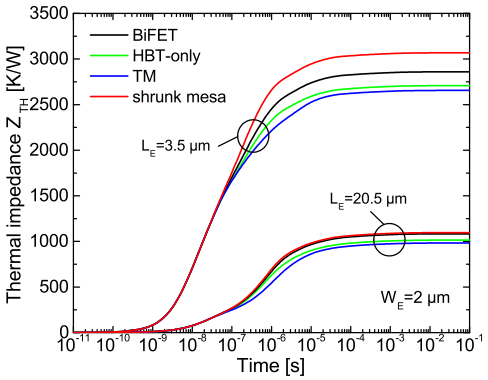


Fig. 3.16. Simulated $Z_{TH}(t)$ for devices with W_E=2 μm and L_E=3.5 and 20.5 μm: comparison between BiFET transistors (black), devices without pHEMT layers (green), TM HBTs (blue), and DUTs with shrunk base-collector mesa (red).

The above analyses confirm that FANTASTIC can provide simple guidance on what device feature the Z_{TH} should scale with. In particular, the size of the base-collector mesa gives rise to a fundamental trade-off between thermal and electrical performance; for example, undercutting the mesa [160] reduces the base-collector capacitance, but leads to an increase in Z_{TH} that can offset the electrical benefit. Important information is gained on the thermal performance sensitivity to emitter size and HS geometry. The results are summarized in Fig. 3.17.

	FEM std	FANTASTIC
Time	8 hrs	7.5 min
RAM	10 GB	1 GB

R_{TH} wrt BiFET:	HBT-only	Top Metal	Shrunk Mesa
L_E=3.5 µm	-5.5%	-7%	+7%
L_E=20.5 µm	-6.5%	-9%	+1%

Fig. 3.17. Summary of results for single-finger HBT.

As a second case-study, let us consider a four-finger HBT with area of each emitter given by $W_E \times L_E = 2 \times 3.5\ \mu m^2$. The 3-D mesh depicted in Fig. 3.18 is composed by 2.7 million of tetrahedra of grossly different dimensions, thus posing an ill-conditioned problem.

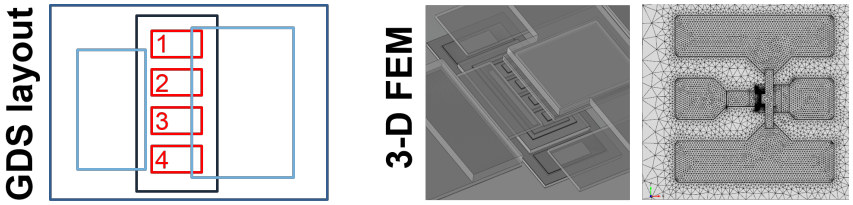


Fig. 3.18. HSs numbering in the simplified layout, detail of the geometry the mesa regions, and a top-view of the constructed mesh.

The usual evaluation of $\mathbf{Z}_{TH}$ with a FEM tool is obtained by performing transient FEM simulations for all the HSs, activating only one of them at a time. For the DUT, the evaluation of the curves depicted in Fig. 3.19 due to the activation of a single HS – #1 in Fig. 3.19a, and #2 in Fig. 3.19b – lasts 25 hours with 20 GB RAM occupation on a desktop PC equipped with 32 GB RAM and a quad-core i7-3820QM: therefore, 100 hours are needed to determine the whole Z_{TH}. Conversely, by exploiting the MPMM approach with a 2nd-order FEM discretization involving 3.7 million DoFs and an allowed relative error of 1×10^{-4}, only 1.5 hours and 6 GB RAM are required for the extraction of the TFB, with negligible time (< 1s) to perform each transient simulation. In spite of the short extraction time, an excellent agreement is achieved with the reference FEM simulations, as shown in Fig. 3.19, illustrating that the prescribed accuracy in terms of relative error is indeed correctly obtained. The order of the extracted TFB exploiting the topology in Fig. 3.10 is 57 for all the 4 HSs, which implies 574 components with single-input VCCS. The PSPICE

simulation time required to evaluate $\mathbf{Z}_{TH}$ is negligible, and reported to be 0.05 s in the output file. The PSPICE results are depicted in Fig. 3.19 as well.

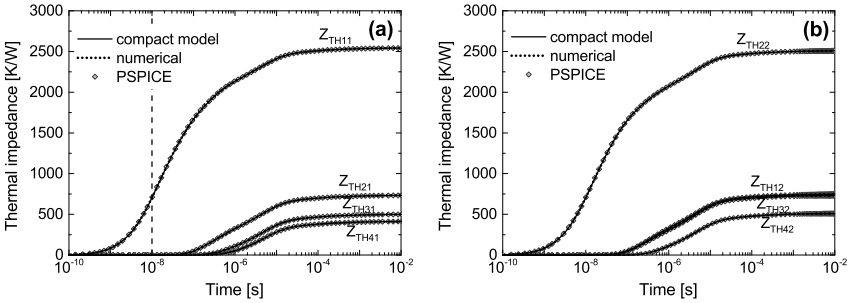


Fig. 3.19. Comparison between transient thermal impedance simulations performed with the compact model of FANTASTIC (solid), numerical FEM reference (dotted lines), and synthesized PSPICE network (rhombi), activating (a) the outer heat source #1 and (b) the inner #2.

Fig. 3.20 reports the spatial field of Z_{TH}, at 10 ns, 1 µs, and 10 ms after the application of the power step to the outer HS#1. For extremely short times, the heat is still confined within the HS, as can be seen from the normalized temperature rise at 10 ns. As it is witnessed by Fig. 3.19 at the vertical dashed line, before 100 ns no perceptible heating affects the inactive fingers (i.e., the mutual thermal impedances are 0 K/W). At 1 µs, the heat has reached the base-emitter junction closest to the activated heat source through lateral heat spreading in the common (lower) collector and subcollector mesa, and above through the metal contact that connects the emitter regions. The steady-state condition at 10 ms plainly evidences the heat spreading over the emitter contact.

FANTASTIC can also be used to analyze arbitrary HS that would be unviable to simulate with FEM. Let us now consider the concurrent application to all HSs of:

- power steps of 2.5 mW. As expected, the inner junctions #2 and #3 heat up more due to the stronger coupling with the surrounding HSs.
- upon reaching the steady-state condition for the power steps at 10ms, an additional source of $0.25\times[1-\cos(2pft)]$ mW with f=100 MHz.

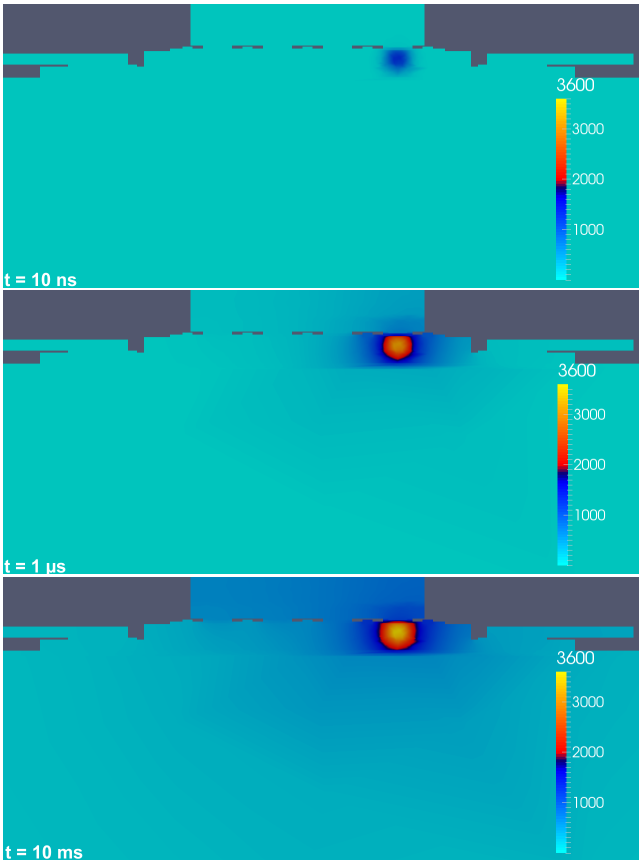


Fig. 3.20. Normalized temperature rise over ambient over a vertical section crossing the center of the HSs, as evaluated in a post-processing step at 10 ns, 1µs, and 10 ms.

Fig. 3.21 depicts the evolution of the average temperature rises over the base-emitter junctions, within a time range spanning from the previous steady-state condition to the new one; also reported is a detail of the temperature rise oscillations occurring in a 0.5 μs-long time window for the outer HSs #1 and #4. The time elapsed for the PSPICE simulation with the TFB amounts to 30 minutes, in spite of the very short maximum time step (0.1 ns); the same simulation would instead have been unviable using a FEM commercial tool. This example proves the applicability of the proposed approach for even complex dynamic ET simulations of electronic devices and circuits.

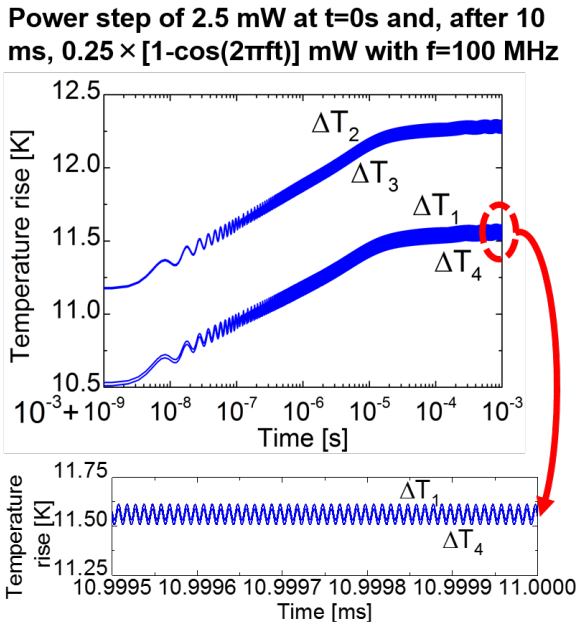


Fig. 3.21. PSPICE simulation of the DUT subject to the application of a power step of 2.5 mW and, after 10 ms, of a further input given by $0.25 \times [1 - \cos(2\pi f t)]$ mW with f=100 MHz to all HS: temperature rises after 10 ms for all fingers, and detail of the thermal oscillations for #1 and #4.

Summary of the advantages of FANTASTIC

The proposed tool FANTASTIC for dynamic thermal and ET simulations of electronic devices, circuit and systems is:

- **Fully automatic**
- **Accurate**. The desired level of approximation can be set a-priori. The tool allows evaluating the full space-time evolution of the temperature field and heat flow in the whole domain, unlike other compact models.
- **Exceptionally fast and less memory-demanding**. The CPU time needed by the tool for constructing the TFB is almost two orders of magnitude smaller than that required by standard commercial thermal FEM simulator for determining the power step thermal responses of the single power sources. Performing thermal and electrothermal simulations with the extracted TFB require negligible time with respect to the use of the FEM model.
- **Easily integrable into standard design flow**. A novel TFB is provided for efficient circuit simulation.

The tool can be used thus to improve the thermal ruggedness of electronic products.

3.3 Nonlinear TFB for one heat source

For some heat diffusion problems in electronic components, the temperature dependence of thermal conductivities cannot be neglected [161, 162]. This problem has earned recent interest by many authors [163–168].

The commonly adopted approach for constructing TFBs devised for *nonlinear* thermal problems is based on the Kirchhoff's transformation [169–171], by which the solution to the nonlinear heat diffusion problem is mapped onto the solution to a linear problem, and its improvement by Batty *et al.* [172–174]. However, these approaches in practice provide exact results only assuming *a single material* for the whole geometrical domain, while introducing large inaccuracies in realistic structures.

In order to overcome the aforementioned inacuracies, in [162, 175, 176] is reported an extension to the MPMM to nonlinear heat conduction starting from [164, 177–179] and exploting results [180, 181]. The nonlinear TFB for the case of a single heat source is depicted in Fig. 3.22, and its extension to the case of a generic M-port [182] is currently under investigation.

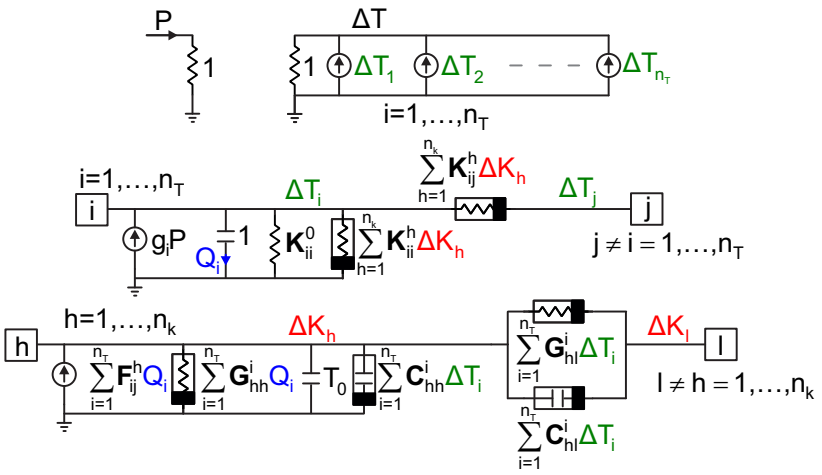


Fig. 3.22. TFB corresponding to the compact model reported in [162, 175, 176].

The TFB accuracy is demostrated by extending the analysis of Section 2.6 in the nonlinear case. Let us assume that the thermal conductivity can be written, as it is common for materials used in microelectronics:

$$k(\Delta T) = k_1 \left(1 + \frac{\Delta T}{T_0}\right)^m + k_2 \tag{3.38}$$

in which parameters k_1, k_2, and m have different values in the individual layers. Table 3.2 gives the material parameters adopted for the analysis. Two cases were analyzed: (i) case A, in which the thermal conductivity of BCB was considered to be temperature-insensitive, as assumed in [110], and (ii) case B, in which it was modeled as linearly increasing with temperature on the basis of the experimental data shown in [117]. Both cases A and B are nonlinear since the temperature dependences of the thermal conductivities of Si, Pb/Sn, and AlN are accounted for. The dissipated power density was assumed uniform within each HS.

Table 3.2. Values of the material parameters.

Material	ρ [kg/µm^3]	c [J/kgK]	k_0 [W/µmK]	k_1 [W/µmK]	m
Si [115, 183]	$2.330 \cdot 10^{-15}$	711	$1.48 \cdot 10^{-4}$	$1.48 \cdot 10^{-4}$	-1.33
A) BCB [110]	$1.051 \cdot 10^{-15}$	1 267	$1.80 \cdot 10^{-7}$	0	0
B) BCB [117]	$1.051 \cdot 10^{-15}$	1 267	$1.80 \cdot 10^{-7}$	$3.00 \cdot 10^{-7}$	1
Pb/Sn [118]	$11.200 \cdot 10^{-15}$	137	$0.36 \cdot 10^{-4}$	$0.36 \cdot 10^{-4}$	-1.10
AlN [119]	$3.260 \cdot 10^{-15}$	748	$1.50 \cdot 10^{-4}$	$1.50 \cdot 10^{-4}$	-1.57

Firstly, the case in which only the 2$^{\text{nd}}$-level circuitry is active was considered. The solution of the thermal problem was computed both with Comsol. This took less than 1 hour 15 minutes and less than 1 GB of RAM storage on a 2.3Ghz Intel Core i7. The resulting model can be exploited for determining the thermal behavior for any waveform of power $P(t)$. Here the case of a constantly dissipated power density q=5 μW/μm^3 (i.e., $P \approx 45$ W) is analyzed by comparing the results provided by the compact model and the TFB with those calculated by Comsol with low tolerances

Fig. 3.23a shows the resulting thermal impedances $Z_{\text{TH}}(t)$ for the fully linear case (i.e., that obtained by disregarding *all* the temperature dependences of the thermal conductivities), for the modified linear solution through the Kirchhoff and Batty *et al.*'s transformations, and for the nonlinear cases A and B, i.e. with $k_{BCB}(T_0)$ and $k_{BCB}(T)$. Fig. 3.23b depicts the profile of the temperature rise along the vertical axis crossing the center of the module, as evaluated by Comsol and the compact model; again, an excellent matching between the results is achieved. The figure evidences the sharp temperature drop occurring within the BCB layers.

These figures illustrate that the DCTM is suited to describe not only the thermal impedance $Z_{\text{TH}}(t)$ but also the whole space-time evolution of the tem-

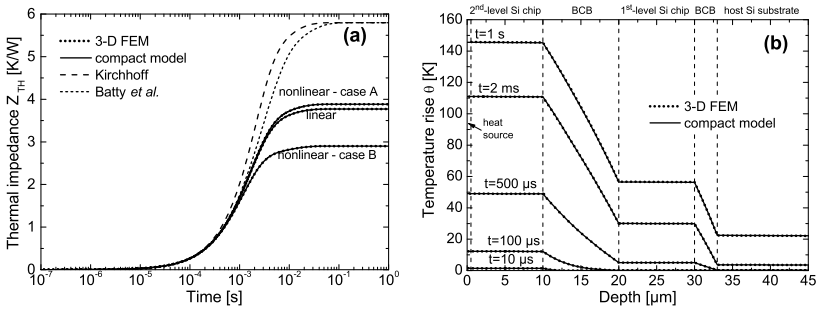


Fig. 3.23. Case of activation of the circuitry lying on the upper silicon chip: (a) thermal impedance against time for the linear and nonlinear cases, as simulated by Comsol (dotted lines) and obtained through the compact model (solid), along with the evolution determined by the mere application of the Kirchhoff's (dashed) and Batty *et al.*'s (short-dashed) transformations with the temperature dependence of Si; (b) vertical profile of the temperature rise along the module for the nonlinear case B, as computed by Comsol (dotted lines) and the compact model (solid) at five time instants.

perature rise with great accuracy, the discrepancy with respect to 3-D FEM results being lower than 0.2%.

From these results various observations are in order:

1. The thermal resistances $R_{\rm TH}$ are equal to 3.77, 3.88, and 2.90 K/W for the linear and the nonlinear cases A and B, respectively. In spite of the low BCB conductivity, the values are not high due to the large heat source area.
2. It can be easily inferred that the BCB dominates the thermal behavior. In case B, k_{BCB} linearly grows from 1.8×10^{-7} W/µmK at $T = 300$ K to 3.25×10^{-7} W/µmK at $T = 425$ K, thus leading to a cooling action high enough to prevail over the heating mechanism induced by the reduction in thermal conductivity of other materials; as a result, the thermal behavior of the module improves compared to the linear case. The large discrepancies between the results corresponding to the two cases A and B suggest that care must be taken in modeling the temperature dependence of the thermal conductivities of all materials belonging to the structure under test.
3. An inspection of the figure reveals the dramatic inaccuracy obtained by merely applying the Kirchhoff's transformation based on the law relating the thermal conductivity of Si to temperature with $m = -1.33$; in particular, $R_{\rm TH}$ differs by $\sim$50% and $\sim$100% from the *exact* values associated to the nonlinear cases A and B. Including the further time variable transformation by Batty *et al.* only a marginal improvement is gained for

medium times, while the steady-state results remain unchanged.

A similar analysis was repeated by activating only the HS describing the 1st-level chip. Fig. 3.24a shows that in this case the self-heating is considerably mitigated since the buried chip is closer to the board kept at ambient temperature. In particular, it is found that the thermal resistances R_{TH} amount to 1.21, 1.23, and 1.10 K/W for the linear and nonlinear cases A and B, respectively. It is worth noting that the plain reduction in the curve slope triggered by the heat reaching the silicon substrate takes place earlier than in the case with the 2nd-level circuitry activated. All the findings reported above concerning the accuracy of the compact model and the required CPU times and RAM storage still hold true in this case. This is evidenced in Fig. 3.24b, which depicts the profile of the temperature rise along a horizontal axis crossing the center of the module, as computed by both Comsol and the DCTM.

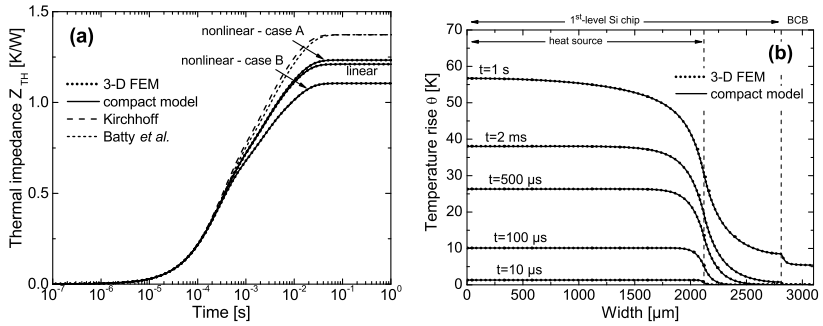


Fig. 3.24. Case of activation of the circuitry located on the buried silicon chip: (a) thermal impedance versus time for the linear and nonlinear cases, as simulated by Comsol (dotted lines) and determined through the compact model (solid), along with the evolution obtained by applying the Kirchhoff's (dashed) and Batty *et al.*'s (short-dashed) transformations based on the temperature dependence of the thermal conductivity of Si; (b) horizontal profile of the temperature rise along the module for the nonlinear case B, as evaluated by Comsol (dotted lines) and the compact model (solid) at five time instants.

Fig. 3.25 witnesses that the DCTM approach allows accurately following the temperature evolutions induced by short activations of the circuitry located on the chips – which are inherently cumbersome to be simulated at the edges of the square-wave power profiles (i.e., when the heat source turns on and off) if exploiting conventional 3-D FEM tools. In particular, three power pulses dissipated by the upper chip are considered, which are characterized by different levels and durations so as to keep constant the pulse area. The figure

depicts the transient behavior of the temperature rise averaged over both the circuitries, as evaluated by the DCTM and Comsol for the nonlinear case B. Consistently with the previous analyses, it is found that the approaches provide almost identical results, although for each power profile the DCTM simulation lasts less than 2s while Comsol requires more than 20 hours mainly due to the aforementioned issue.

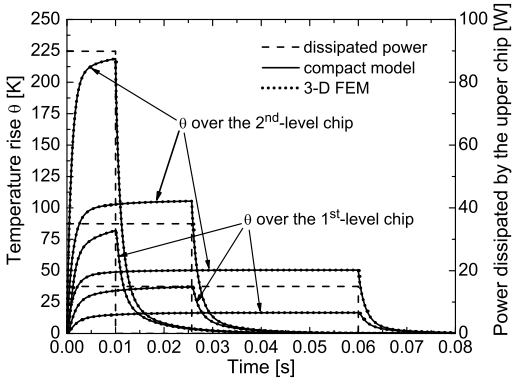


Fig. 3.25. (Left) Average temperature rises over the upper and buried silicon chips induced by (right) three profiles of power dissipated by the circuitry located on the 2^{nd}-level chip (dashed lines), as determined through Comsol (dotted) and the compact model (solid) for the nonlinear case B.

3.4 Thermal simulations of state-of-the-art SiGe HBTs

Thermal resistances of state-of-the-art SiGe HBT computed with classic heat conduction equation for transistors developed within the framework of the DOTFIVE project [184] were found to be much lower than experimental data (e.g., [185]) by considering standard bulk literature values for the material parameters. An improved model for heat transfer in nanoscale devices is thus needed since the Fourier heat equation does not account for sub-continuum effects relevant in devices with dimensions comparable or smaller than the average phonon mean free path (~300 nm in bulk Si), such as (see Fig. 3.26) [186–189]:

- Interaction between hot electrons and optical/acoustic phonons
- Phonon-boundary scattering (#1)
- Phonon-defect scattering (#2)
- Phonon-impurity scattering (#3)
- Localized heating effect (i.e., reduced number of phonons collisions in the BC SCR)

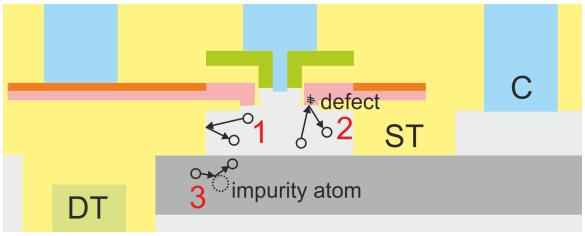


Fig. 3.26. Schematic view of some additional effects to be taken into account in order to correctly describe heat propagation.

The Lai and Majumdar model [190] for the two steps optical/acoustic phonon model has been implemented in Comsol and preliminarily tested on the detailed 3-D structure of an Infineon reference device with A_E=0.2×2.67 μm^2 by considering standard silicon [191], and SiGe [192] parameters. The Lai and Majumdar thermal model (illustrated in Fig. 3.27) is based on *energy balance* equations for ("slow") optical and ("fast") acoustic phonons, defining their two temperatures T_{op} and T_a, and an average lattice temperature T_L. The heating rate H is assumed to be composed by high energy electrons colliding exclusively with optical phonons. Heat conduction occurs only through acoustic phonons, and is therefore limited by the optical-to-acoustic phonons decay for small time and geometrical scales [193, 194]. It is worth noting that

this model is consistent with the Fourier equation, as for non-nanometric heat sources the Lai model results coincide with the ones obtained by solving the Fourier equation (i.e., $T_L = T_a = T_{op}$), while a discrepancy can be seen for nanometric heat sources due to energy storage in optical phonons[1]. Moreover, it must be remarked that the acoustic phonon temperature in steady state corresponds to the one obtained with the Fourier equation since, by posing the time derivatives to 0,

$$\nabla \cdot (k_a \nabla T_a) = -H \tag{3.39}$$

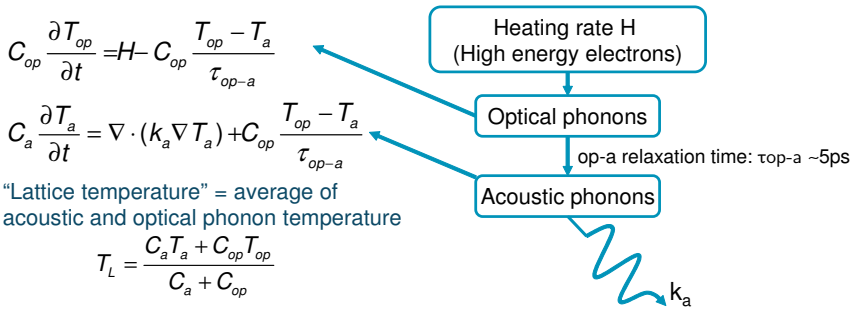
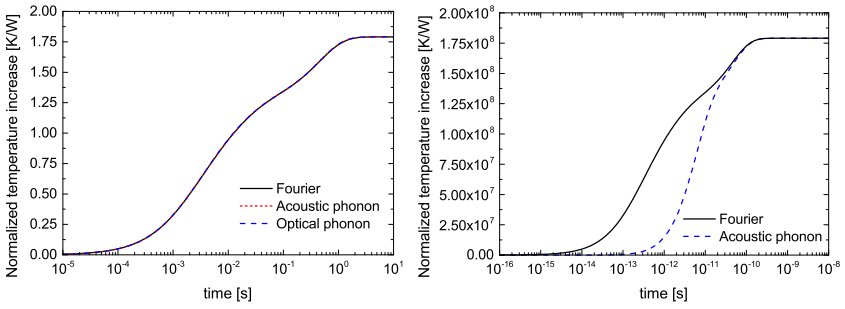


Fig. 3.27. Lai and Majumdar model [190] assuming heat generation through electron to optical phonon collisions and under relaxation time approximation for optical-to-acoustic phonon decay.

The heat generation term has been assumed uniform and constant in the first simulations, while a more detailed form is assumed in the following. The simulation parameters for the Lai model are listed in Tab. 3.3. For SiGe, C_{op} was assumed equal to the one reported for silicon [191], while τ_{op-a} was chosen as reported in [192]. For the remaining materials, C_a was assumed equal

[1] As an example, the figure below depicts the $Z_{TH}(t)$ as computed for a big (0.1 cm^3, on the left), and a nanometric (0.1 nm^3, on the right) HS inside a SiO_2 trench in a Si substrate – note the difference in the steady-state values and in the timerise.



to their usual volumetric specific heat, and C_{op} and τ_{op-a} equal to Si values: this way, consistency is kept to the Fourier equation for regions far from the HS.

Table 3.3. Parameters adopted in the energy-balance model.

C_a	Acoustic phonon volumetric specific heat	Si 1.00 [J/(K cm^3)]
C_{op}	Optical phonon volumetric specific heat	Si, SiGe 0.65 [J/(K cm^3)]
τ_{op-a}	Optical to acoustic phonon relaxation time	Si 5ps, SiGe 23ps

Phonon-boundary scattering and thin layers size effects were modeled with the simplified analytical method by Tornblad *et al.* [195], leading to a reduced anisotropic local thermal conductivity. The model is described by the following factors of thermal conductivity reduction

$$\frac{k_{x,y}(z')}{k_{bulk}} = 1 - \frac{1}{2}\exp\left(-\frac{z'}{z_{charxy}}\right)^{0.75} - \frac{1}{2}\exp\left(\frac{1-z'}{z_{charxy}}\right)^{0.75}, \quad (3.40)$$

$$z_{charxy} = 0.32 \cdot \frac{\Lambda}{D}$$

$$\frac{k_z(z')}{k_{bulk}} = 1 - \frac{1}{2}\exp\left(-\frac{z'}{z_{charz}}\right)^{0.95} - \frac{1}{2}\exp\left(\frac{1-z'}{z_{charz}}\right)^{0.95}, \quad (3.41)$$

$$z_{charz} = 0.72 \cdot \frac{\Lambda}{D}$$

where z' is the normalized position within layer (along the thickness), Λ is the phonon mean free path (300 nm for bulk silicon), D is the film thickness. The model (3.40) and (3.41) has been implemented for the Si and SiGe *inside the shallow trenches* and for the Si *in the emitter region*. For the dimensions in the order of fractions of μm, this implies a significant decrease in the thermal conductivity.

Simulations results for the standard Fourier equation and including sub-continuum effects are depicted in Fig. 3.28 and can be summarized as follows.

The phonon-decay limited heat conduction effect influences only a small spatial region, and a fairly large discrepancy between T_{op} and T_a can be seen in the HS region. The normalized temperature rise at the base-emitter-junction only exhibits a small difference that can be mostly ascribed to thermal conductivity reduction in the shallow trenches according to [195]. The thermal resistance is evaluated from the average temperature at the base-emitter junction. The simulated thermal resistance with the new model is still lower (by 33%) than the experimental value, yet better than the standard Fourier model (error of 42%).

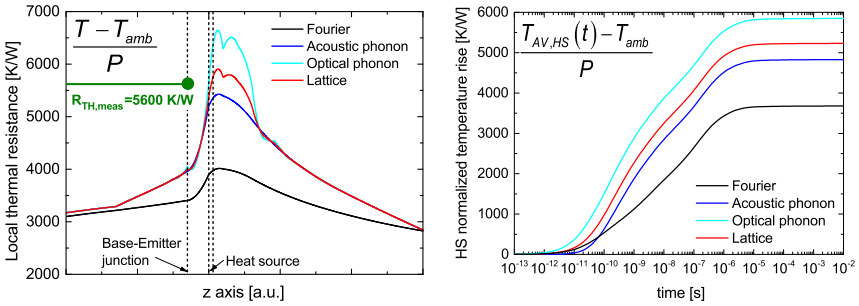


Fig. 3.28. (left) Normalized temperature increase along the vertical direction at center of heat source and (right) its average over the HS volume evaluated by solving the standard Fourier heat equation and exploiting the energy balance model and including equations (3.40) and (3.41).

A more detailed breakdown of the contribution to the R_{TH} increase toward the experimental value is depicted in Fig. 3.29.

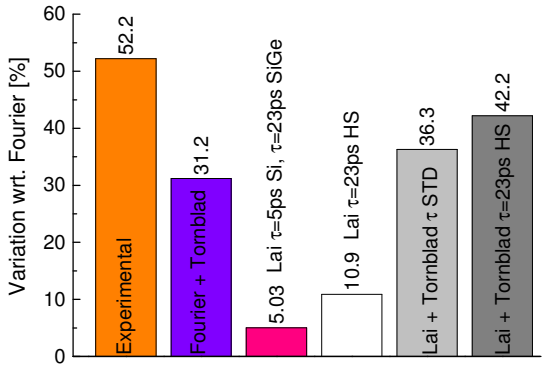


Fig. 3.29. Effects of various contributions to the R_{TH} increase.

A better agreement could be in principle be obtained by performing first-principles simulation with the BTE in order to compute the material parameters. In particular, optical to acoustic phonon relaxation time plays an important role in determining the discrepancy between the temperature rise obtained with the Fourier heat equation and the energy balance model. It is worth noting that BTE-based solvers, e.g. SHE [196], cannot be directly applied to a 3-D analysis of complex device architectures.

Further improvements of Fourier simulation

While it has not been possible yet to recover the whole discrepancy between simulation and experimental mesurement for the R_{TH}, further improvements can be made for the Fourier simulations, that have been used to quantify the backend impact on a DOTSEVEN [197] transistor structure manufactured with the B7HF500 process provided by Infineon.

First, the geometry of the backend was imported from the layout mask data with a custom script, which exploits Griesmann's GDS II Libraries [152] and technological process information. The meshing was performed by suitable domain decomposition and by resorting to selective region refinement tool with optimized mesh parameters. Fig. 3.30 depicts a detail of the mesh in the backend zone.

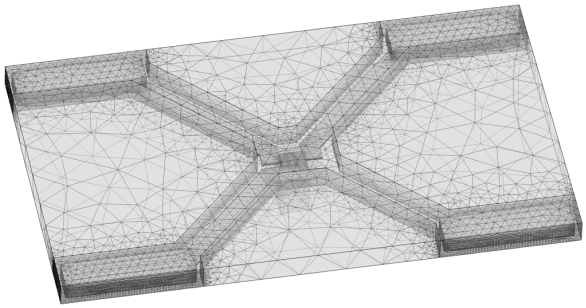


Fig. 3.30. Detail of the mesh for the backend obtained through suitable domain decomposition and selective-region meshing.

A detailed HS representation, i.e. the local dissipated power density, has been obtained from 2-D electrical simulations[2] by computing[3]

$$q\,[W/\mu m^3] = \mathbf{J} \cdot \mathbf{E} \tag{3.42}$$

and the result is represented in Fig. 3.31. The HS for the subsequent 3-D thermal simulation is then assumed uniform in the third dimension in the corresponding region of the emitter window.

The thermal conductivity depends on doping, especially at higher impurity concentration level such as more than 10^{20} cm^{-3} [199]. Recent molecular dynamics results [200] have been used to model the doping dependence of the

[2]Calibrated HD models for SiGe were extracted and TCAD simulations with commercial tools were performed by Dr. Grazia Sasso.

[3]More refined expressions for H, such as the hydrodynamic term in [198], can also be used and are under investigation.

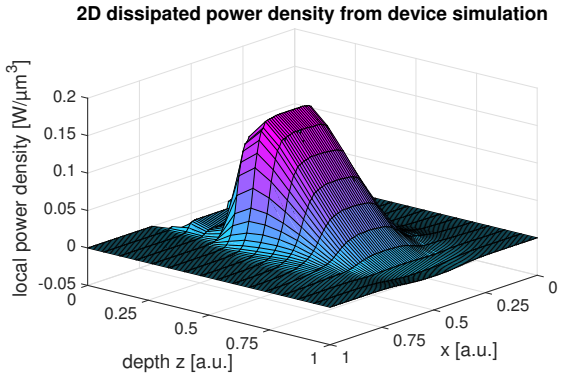


Fig. 3.31. Local power density corresponding to the heat source used in the thermal simulations as obtained through detailed 2-D device simulation.

thermal conductivity. The following equation was adopted

$$k_{doped,bulk} = \frac{k_{Si,bulk}(300K)}{1 + \left(\frac{A}{n/n_{norm}}\right)^{\alpha}} \tag{3.43}$$

where n is the doping concentration, $k_{Si,bulk}$ = 148 W/(mK) is the standard reference literature value for bulk silicon, and n_{norm} = 10^{20} cm^{-3}, A = 0.74186, α = 0.7411 for boron [200]. The same expression was adopted for arsenic thanks to a parameter calibration procedure relying on experimental results [199], which led to A = 1.698, and α = 0.8251. The resulting boron- and arsenic-impacted thermal conductivities are plotted in Fig. 3.32a. The total thermal conductivity used for thermal simulations is anisotropic and space-dependent using the doping profile information in (3.43), accounting for the further reductions due to germaniumin the SiGe layer [119] and due to the small layer thickness depdendence according to (3.40), (3.41) [195]. Fig. 3.32b depicts the thermal conductivity as a function of the depth within the HBT under analysis.

The thermal resistance is evaluated by applying the heat source depicted in Fig. 3.31, and then computing the average temperature rise above ambient over the base-emitter junction normalized to the applied power. Since the experimental values have been evaluated at low dissipated power, the temperature dependence of the thermal conductivity is negligible. Even though there is a discrepancy of 22% with the experimental results, simulations have allowed quantifying the relative effect of the backend on the thermal resistance; in particular, the backend cooling impact on the thermal behavior was suppressed by

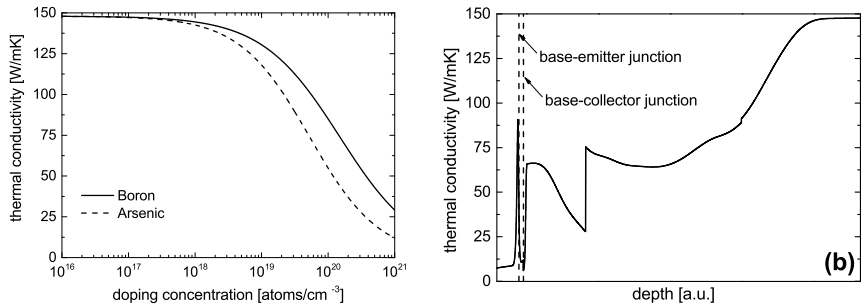


Fig. 3.32. (a) Implemented models for the thermal conductivity reduction with doping; (b) Thermal conductivity as a function of position obtained by combining concurring effects.

replacing the metal with silicon dioxide. It was found that only metal layers located in close proximity of the emitter have significant impact; metal and via 1 are the most relevant in decreasing the thermal resistance.

Results are summarized in Tab. 3.4, and Fig. 3.33.

Table 3.4. Thermal resistances evaluated by excluding layers of metal.

Experimental value: 7960 K/W

	Full backend	No metal 4 to 5	No metal 3 to 5	No metal 2 to 5	No metal 1 to 5	No metal 1 to 5 and no contacts
Simulation	6234 K/W	6234 K/W	6390 K/W	6575 K/W	8614 K/W	8804 K/W
Rel. diff.	[Reference]	Negligible	+2.5%	+5.5%	+38.2%	+41.2%

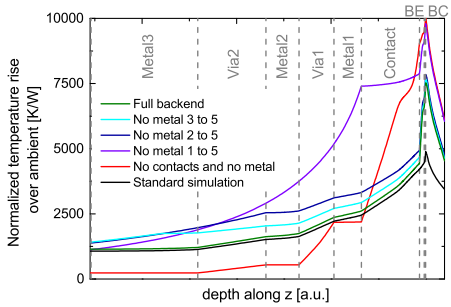


Fig. 3.33. Normalized vertical temperature rise over ambient evaluated crossing the center of the HS.

3.5 Node clustering for power delivery networks

Among the most temperature-sensitive components in large ICs, the power delivery networks (PDNs) are to be accurately analyzed due to the increasingly larger supplied currents and integration density. PDNs include many different sections such as power planes, metal traces, chips, packages, decaps, vias, C4 bumps. As a consequence, even though simple models are assumed for any of such subparts, the size of an equivalent network describing a PDN easily reaches the order of several millions of nodes. Therefore, a major and challenging problem associated to ET simulations of PDNs is the reduction of their computational cost.

Dynamic simulations and noise analysis can be simplified by exploiting a reduction strategy based on *clustering* starting from the much simpler steady-state solution: *macronodes* are defined on the basis of a criterion defining when the local interactions between two nodes can be neglected, and a reduced circuit is thus built.

The structure analyzed hereinafter is depicted in Fig. 3.34, and comprises a regular and uniform ground (GND) and supply (VDD) grids separated by an insulation layer.

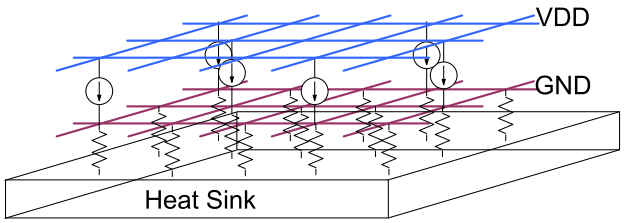


Fig. 3.34. Schematic of the PDN under test. The vertical resistances to the heatink model the thermal connection.

The electrical model of the PDN is described with a suitable connection of the single nodes depicted in Fig. 3.35a: each node is connected toward the adjacent ones with temperature-dependent resistors $R(T)$, whereas a current source J_0 and a capacitor C represent the current demand and the output capacitance of the active port (i.e., the load) connected between the VDD and GND grids. The PDN is built by replicating a basic *stamp* element, which is comprised by a square that is connected at opposing corners to the VDD and GND supply pins through a series resistance R_S.

A simplified, but realistic thermal model is here considered, based on the

well-known electrical equivalent of the thermal problems. The basic grid node is depicted in Fig. 3.35b, and the thermal equivalent model is built according to the following considerations:

- the grid discretization of the elementary stamp is small enough to exploit the concept of *characteristic thermal length,* [201, 202], thus allowing a one-to-one correspondence of electrical and thermal nodes. Therefore a network of thermal resistances R_{TH} corresponding to the PDN segments modeled by electrical resistances R can be built.
- heat transport occurs mainly along the conductors (grids and vias), i.e., heat propagation in the (insulating) dielectric is negligible;
- the heat production, modeled with current sources P_D, takes into account all the heat generation mechanisms (i.e., circuit dissipation and joule heating in the interconnects) [202, 203]. Let the voltage drop $V_{IR}(k)$ at the generic node k – corresponding to the one that would be observed from an IR drop analysis – be

$$V_{IR}(k) = V_{DD} - (V_{pwr}(k) - V_{gnd}(k)), \tag{3.44}$$

  with $V_{pwr}(k)$, $V_{gnd}(k)$ the k-th node potentials within the power and ground layers, respectively, and V_{DD} the supply voltage. $P_D(k)$ is thus given by $P_D(k) = J_0 \cdot V_{IR}(k)$.
- one side of the chip connected to a heat sink; the connection is modeled with additional thermal resistances R_{HS}.

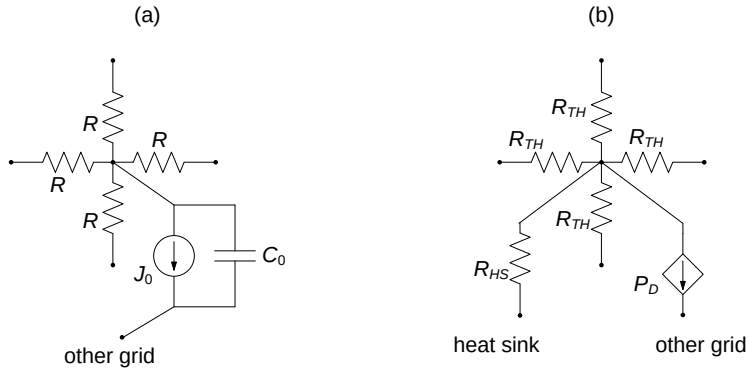


Fig. 3.35. Generic node of the grids for: (a) electrical, and (b) thermal model.

The two problems are coupled in a classical relaxation approach. The system is initially assumed to be at room temperature $T_0 = 300$ K. After the thermal problem is solved and the temperature distribution is known, the electrical

resistivity is updated according to

$$\rho(T) = \rho_0(1 + \alpha_0 \Delta T), \tag{3.45}$$

where ΔT is the temperature rise above ambient, $\alpha_0 = 0.0039\,\mathrm{K}^{-1}$ is the resistivity temperature coefficient (TC), and $\rho_0 = 1.72 \times 10^{-8}$ its value at $T = T_0$ for "bulk" copper (i.e., with transverse size of the order of 100 nm or more). For nanoscale sizes, phenomena like electromigration and boundary and grain scattering lead to different values: at a line width of 14 nm, it would be $\rho_0 = 8.19 \times 10^{-8}$ and $\alpha_0 = 0.0012\,\mathrm{K}^{-1}$ [204]. The update rule for the electrical resistance R between two nodes 1 and 2 is given by:

$$R(T) = R_0[1 + 0.5\alpha_0(\Delta T_1 + \Delta T_2)] \tag{3.46}$$

where R_0 is the value at room temperature T_0. By establishing convergence between the two problems, the final temperature distribution and the voltage drops are obtained.

A reduction strategy based on the following facts can be proposed:

- (i) the thermal problem can be considered a steady state one from the point of view of the signal processing time scale;
- (ii) the study of voltage drops at fixed temperature, as well as the thermal problem at assumed operation frequency, are linear algebraic problems with favorable properties;
- (iii) non linearity only arise when the electrical and thermal problems are coupled, due to temperature dependence of the resistance.

Observation (i) implies that a reduced network can easily be produced for dynamic / noise analysis ET starting from the solution of the same network in the simpler case of steady-state condition.

From (i)–(iii), it is apparent that a preliminary ET steady-state solution can be obtained by exploiting appropriate sparse efficient numerical solvers for the linear problems and a fast convergent relaxation cycle, requiring minutes on a desktop PC for networks of millions of nodes.

After an accurate ET steady-state solution has been achieved, the network can be very effectively reduced by a *node clustering* process as follows. First, a quantization is chosen (e.g., uniform by defining a step) and the nodes are classified according to their voltage drop and temperature level in *macronodes*. The connection between them is obtained with topological equivalence reductions, by: a) eliminating (short-circuiting) the connections among nodes belonging to the same macronode; b) properly accounting for the connections (e.g., parallel), in terms of resistances, current sources, capacitances between different macronodes.

This topological reduction process can be algebraically described with the help of classical circuit theory concepts. In fact, just checking the correspondence between original nodes and macronodes, it is possible to build directly the incidence matrices of the reduced electrical and thermal networks, as well as the conductance, capacitance, and current forcing vectors [205]. It is worth noting that the incidence matrix is extremely regular and sparse, and thus can be quickly assembled and solved in MATLAB. Moreover, the reduced network can be synthesized and simulated in PSPICE. Fig. 3.36 depicts a simple example of clustering for a structure of 5×5 nodes into 4 macronodes, where

$$G_{eq12} = 2G; G_{eq13} = 2G; G_{eq24} = 3G; G_{eq34} = 3G. \tag{3.47}$$

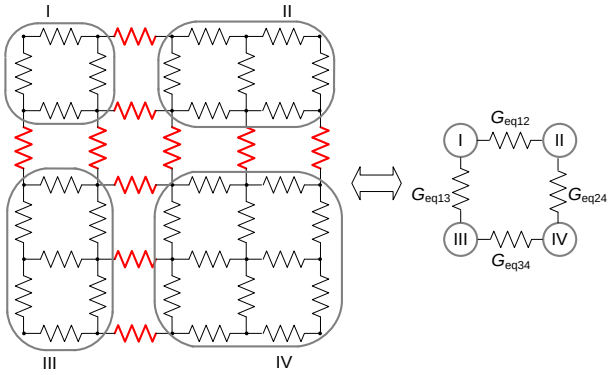


Fig. 3.36. A simple example of node clustering of 25 original nodes into 4 macronodes; resistances in red link nodes belonging to different macronodes.

As a case study, the proposed clustering strategy is applied to the generic PDN depicted in Fig. 3.34, with the two VDD and GND grids generated by a 20×20 replica along x and y of the basic stamp comprising of 2601 (51×51) nodes. Each single tract has a length $l = 5.88\,\mu\text{m}$, width $w = 2.67\,\mu\text{m}$and height $H = 0.668\,\mu\text{m}$, leading to $R_0 = 56\ \text{m}\Omega$, and $R_{TH} = 8473$ K/W. The two VDD and GND grids contain about 1 million (1020×1020) nodes each, for both the electrical and thermal equivalent network, thus totaling about 4 millions nodes. Furthermore we assume V_{DD}=1 V, $J_0 = 0.1$ mA, $R_S = 0.01\,\Omega$, $R_{HS} = 100 \cdot R_{TH}$, and uniform quantization with step 0.4 mK for ΔT, and 2μV for V_{IR}.

In Fig. 3.37 the voltage drop and thermal maps of the original and reduced model for the basic stamp are compared. At an overall reduction factor of 21 in terms of total nodes, the peak voltage drop error and mean normalized relative

error for voltage drop and temperature are both less than 1%.

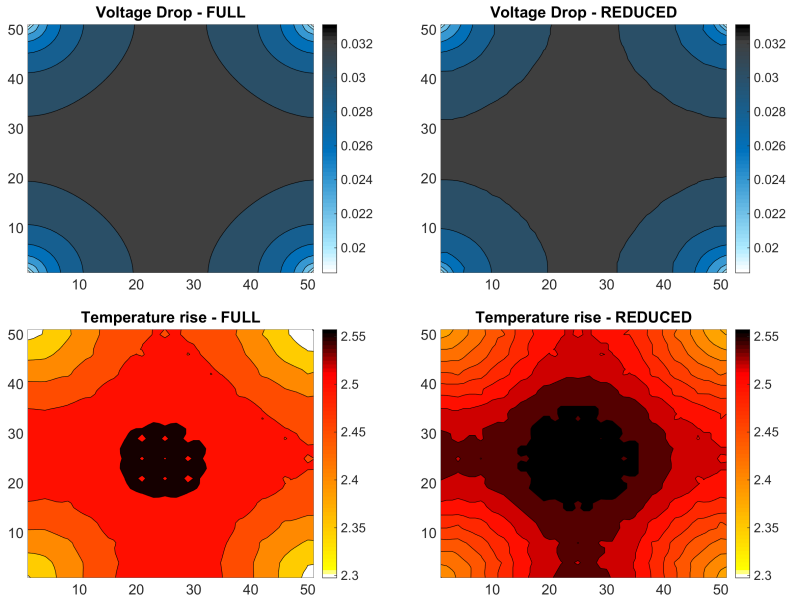


Fig. 3.37. Voltage drop and thermal maps for the case of basic stamp: (left) original solution; (rigth) reduced grid.

As for the reduction at the level of the full PDN, the preliminary ET steady-state solution took 44s on a PC with 32GB RAM and a quad-core processor, while additional 120s are needed for the reduction. After the node clustering, the reduced electrical (thermal) networks contain about 5600 (2000) nodes, so obtaining a compacting factor of about, 180 and 500, respectively.

Fig. 3.38 shows the voltage drop and thermal maps for the full PDN as well as for the reduced model appearing as "blurred" image of the full network, and exhibiting a very good agreement. In particular, the peak voltage drop is predicted within 0.5% accuracy and the mean normalized relative error is about 7.5% for both voltage drop and temperature rise.

Carbon-based PDN analysis

The aformentioned PDN was considered to be built in copper. However, The dramatic increase of copper resistivity at nanoscale has suggested to replace copper with carbon nanotubes (CNTs) or graphene nanoribbons (GNRs) in fabricating on-chip interconnects, due to the outstanding electrical, thermal

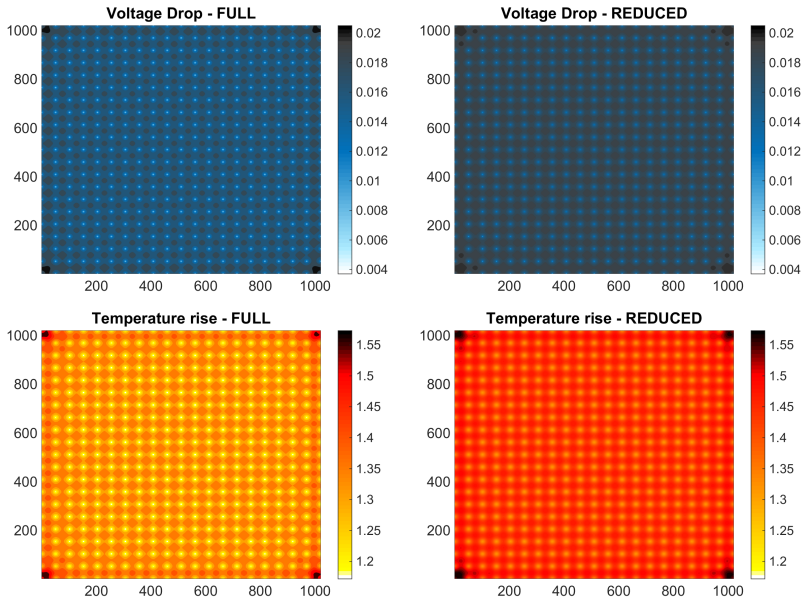


Fig. 3.38. Voltage drop and thermal maps for the case of full PDN: (left) original solution (1 million nodes); (rigth) reduced grid (5600 nodes for the thermal network, and 2000 nodes for the thermal network).

and mechanical properties of such carbon allotropes.

The performance of carbon-based materials have been intensely investigated for signal interconnects and PDNs [204, 206–209], concluding that carbon interconnects may outperform Cu ones at the chip global level, provided that "good quality" interconnects are fabricated. This means: good control of alignment, chirality, dimension, and density, and low contact resistances at the interfaces carbon/metals. For instance, global level power interconnects require a minimum density of 1/2.5 nm^2, if made by single-walled CNTs (SWCNTs) [206], or a minimum length of 20 μm, if made by multi-walled CNTs (MWCNTs) [208].

Due to technological limits, the physical parameters of a realistic carbon interconnect are sensibly different from the amazing values experimentally obtained for isolated samples. For instance, isolated CNTs may exhibit ballistic electrical transport for lengths up to μm, but in real CNT bundles the defects and the contacts may add huge parasitic resistances (of the order of 100 k Ω), hiding the effect of ballistic transport. Similarly, a huge thermal conductivity (3000-5000 W/mK) was reported for isolated CNTs or single GNRs, but this value drops to about 200 W/mK in CNT bundles [210] or GNR arrays [211].

The above considerations lead to the conclusion that the electrical performance of carbon interconnects are often overestimated. However, the greater stability of the resistance over temperature exhibited in some cases by a certain class of carbon lines, could be of great interest for PDNs. Indeed, a resistance TC close to zero or even negative has been theoretically predicted [204] and experimentally reported [212, 213].

As a first investigation, let us now consider the case of replacing the copper of the previously-considered PDN with a CNTs or GNRs [214]. The electrical resistance of a single CNT or GNR of length l may be put in the form [204, 215]:

$$R(T) = \frac{R_Q + R_{con}}{M(T)} + \frac{R_Q}{2M(T)} \frac{l}{\Lambda_{MFP}} \tag{3.48}$$

where R_Q is the *quantum resistance*, R_{con} is a lumped parasitic resistance due to non-ideal contacts, Λ_{MFP} is the mean free path and $M(T)$ is the total number of conducting channels. For Cu, the mean free path decreases with increasing T, thereby leading to a positive TC, as in (3.45). However, for MWCNTs and for all the GNRs, $M(T)$ is increasing with T and for some values of the line length, this leads to a negative TC. This theoretical behavior [204,215] has been demonstrated in[212,213]: for instance, in [213] for MWCNT lengths up to some tens of microns it has been reported a TC between -19 and -4 $\mathrm{m\Omega/K}$.

For the CNT interconnect, we consider each tract filled by a bundle of MWCNTs with outer diameter of 50 nm and filling factor 80%. We assume the realistic case where only 1/3 of the CNT shells are metallic, and the other are semiconducting [210, 211]. In addition, we include the effects of the contact resistance in (3.48). In a similar way, for GNR interconnect we assume an array made of GNRs of width w and length l with 1/3 metallic GNRs. Assuming the temperature-dependent model for $M(T)$ and Λ_{MFP} as in [204, 215], we obtain that for this case study the temperature behavior of R for the carbon lines may be fitted by (with negative TC)

$$R(T) = \alpha_0 + \alpha_1 T + \alpha_2 T^2 \tag{3.49}$$

with fitting coefficients in Tab. 3.5. It must be remarked that the room temperature resistance R_0 is smaller for Cu: $R_{0,Cu} = 56\ \mathrm{m\Omega}$, while $R_{0,CNT} = 152.4$ $\mathrm{m\Omega}$, and $R_{0,GNR} = 1.19\ \Omega$.

For the thermal resistance, considering a realistic value of thermal conductivity of 200 W/mK which has been experimentally reported for multi-CNTs or multi-GNRs [210, 211], we get $R_{TH,CNT} = R_{TH,GNR} = 850$ K/W that is one order of magnitude lower than the one obtained for bulk copper $R_{TH,Cu} = 8473$K/W.

Table 3.5. Fitting coefficients of equation (3.49)

	$\alpha_0\ \Omega$	$\alpha_1\ \mathrm{m\Omega/K}$	$\alpha_2\ \mu\Omega/\mathrm{K}^2$
CNT	0.42	-1.42	1.76
GNR	3.30	-10.15	10.45

Results of ET simulation obtained by relaxation are reported in the following. Fig. 3.39 depicts the maximum voltage drop and temperature rise as a function of the current drawn by each port J_0. It reveals, at realistic parameters values, an interesting trade-off between the voltage drop and the temperature rise for Cu and CNTs, leaving the GNR solution still non performant.

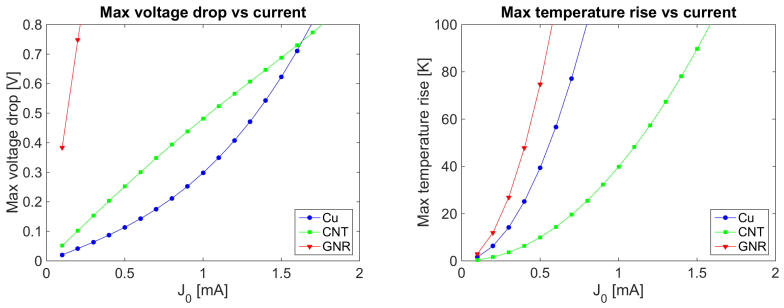


Fig. 3.39. (left) Max voltage drop (right) and max incremental temperature as a function of current for Cu, CNT and GNR.

Fig. 3.40 depicts the voltage drop and temperature maps for the case of Cu and CNT shown for the entire PDN, and for two basic stamps – one in the corner, and one at the centre – assuming $J_0 = 0.4$ mA.

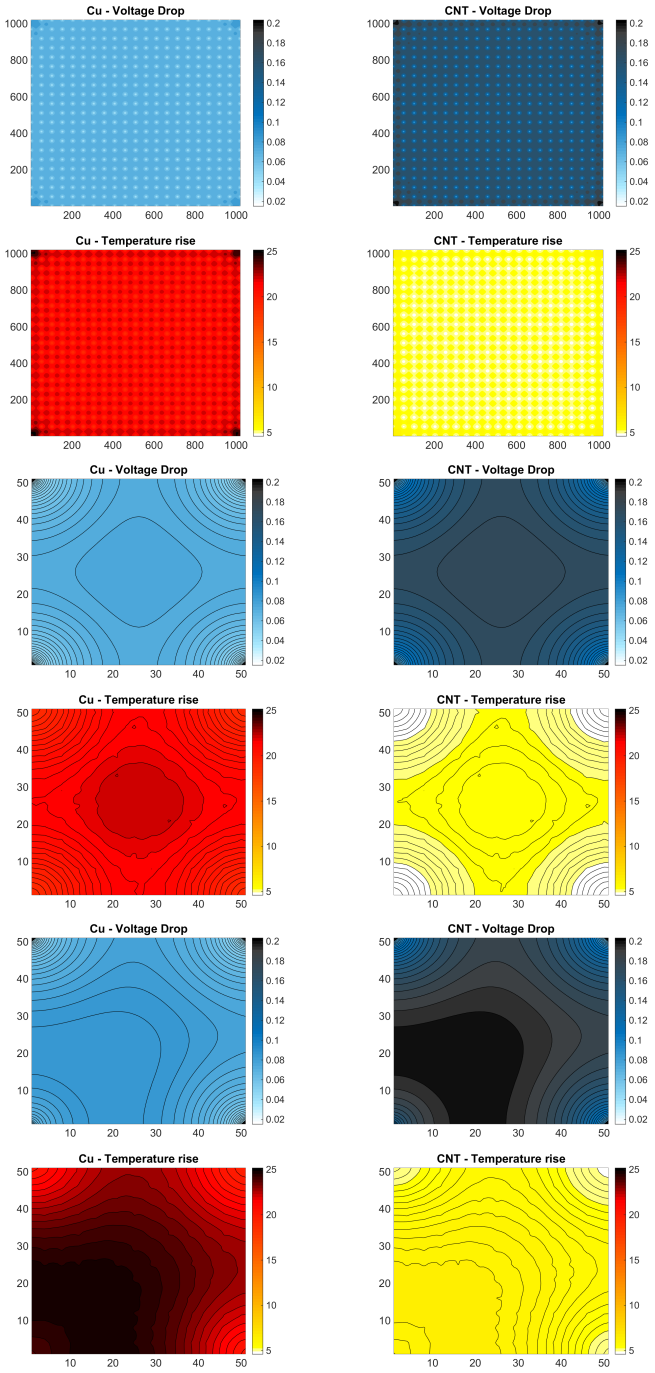


Fig. 3.40. (left) Cu and (right) CNT voltage drop and temperature rise for, (top) the entire PDN, (middle) a stamp located in the center , and (bottom) one in the corner.

Chapter 4

Dynamic electrothermal simulations exploiting TFBs

TFBs allow the execution of fast and effective dynamic ET simulations in a variety of applications for devices, circuit and systems. This assertion is hereinafter motivated through a wide range of case studies including basic analog circuits in advanced technologies (Section 4.1), a signal interconnect line in a highly-integrated module (Section 4.2), reliability testing for power devices (Sections 4.3 and 4.4), and for a string of solar panels subject to architectural shading (Section 4.5).

4.1 Basic analog circuits

4.1.1 Differential pair on Silicon on Glass

In Silicon on Glass (SOG) technology, resistive and capacitive parasitics are drastically reduced by surrounding the whole active silicon region with electrically insulating materials and applying a substrate transfer from silicon to glass (given a SOI structure, the glass substrate is attached to the front-wafer, and the silicon substrate is removed by etching, the oxide acting as an etch-stop) [216, 217]. Thus, the active region becomes a silicon island that can be reached by the electrical signals from the back-wafer. Fig. 4.1 illustrates the device status before the back-wafer contacting process step.

While a significant RF performance improvement is obtained, thermal issues are pushed to the extreme due to the low thermal conductivities of the materials enclosing the silicon island, which do not allow the heat to es-

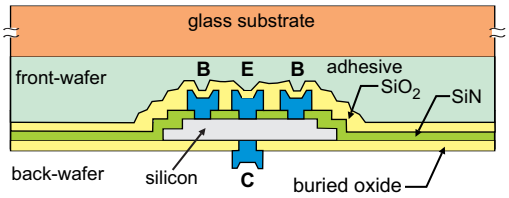


Fig. 4.1. Bipolar transistor fabricated in SOG [9, 14, 218].

cape from the power-dissipating region. Let us consider in the following two subsections a pair of trench-isolated SOG bipolar transistors with $W_E \times L_E$=1×20μm^2, BV_{CBO}=16.7 V in which the spacing between the edges of BJTs amounts to 62.5 μm. It was determined that $R_{TH,self} = 19000$ K/W, and $R_{TH,mutual} = 1200$ K/W, and Fig. 4.2 depicts $\mathbf{Z}_{TH}$ computed through calibrated 3-D simulations [9, 14, 218]. Further technology and layout details are reported in [9, 14, 218].

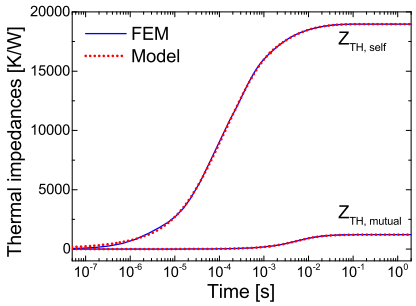


Fig. 4.2. $\mathbf{Z}_{TH}$ as obtained by FEM simulations and for the extracted TFB.

Due to significant thermal effects, the behavior of basic analog circuits can be dramatically distorted. As an example, let us consider a differential pair as depicted in Fig. 4.3, with resistances R_L both equal to 250 Ω. The circuit is assumed to be *ideally matched*, i.e., the two transistors are identical from both the electrical and thermal viewpoints. Simulations were carried out by using PSPICE with the approach outlined in Section 1.2. The BJT electrical macromodels, including impact ionization (II), were built according to [9, 13, 14, 219].

Fig. 4.4 illustrates the differential output voltage V_{od}=V_{o1}-V_{o2} and the collector currents I_{C1}, I_{C2} vs. input voltage V_{IN}, as obtained with an ET steady-state simulation by sweeping the base current I_{B1} and keeping the tail current I_E and supply voltage V_{CC} equal to 1.6 mA and 4 V, respectively. Fig. 4.4a shows that the conventional high-slope linear operating region of the voltage–transfer

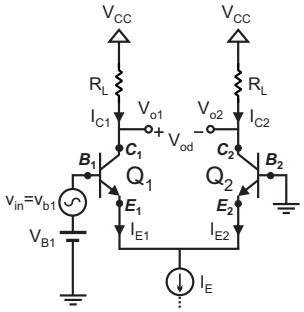


Fig. 4.3. Sketch of the analyzed bipolar differential pair

characteristic (VTC) where the pair behaves as an amplifier is replaced by a positive differential resistance branch (PDR), which translates into a hysteresis phenomenon under V_{IN}-controlled conditions [14]. Fig. 4.4 clarifies that for V_{IN}=0 V, besides the expected symmetric behavior (I_{C1}=I_{C2} $\approx$ $I_E/2$) two additional thermally-triggered asymmetric solutions arise, in which one transistor hogs the whole current and the other becomes dry (I_{C1} $\approx$ I_E, I_{C2} $\approx$0A and I_{C2} $\approx$ I_E, I_{C1} $\approx$0A) [14]. Fig. 4.4a also evidences that the self-heating thermal resistance of Q_1 and Q_2 must be reduced to values =6300 K/W in order to restore the desired linear region for the same thermal coupling and DC bias conditions.

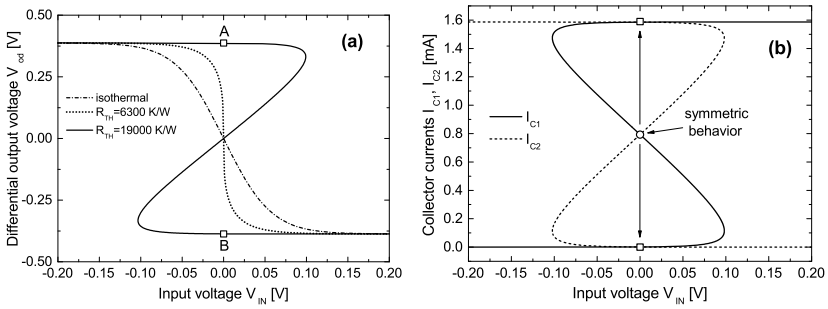


Fig. 4.4. (a) Differential output voltage V_{od}=V_{o1}-V_{o2} as a function of input voltage V_{IN} under ET (solid and dotted lines) and isothermal at T=300 K (dot-dashed) conditions; (b) collector currents I_{C1} (solid line) and I_{C2} (dashed) as a function of input voltage V_{IN}, as obtained by increasing the base current I_{B1} under ET conditions. In all cases, I_E =1.6 mA and V_{CC} =4 V.

In order to perform dynamic ET simulation, a TFB based on the Multi-port topology has been obtained, for which 5 poles (corresponding to 10 RC pairs in the synthesis) were found to guarantee a fairly good accuracy [220]. The

$\mathbf{Z}_{TH}$ synthesized in the TFB is depicted in Fig. 4.2.

A first transient simulation was performed by applying only the DC bias (namely, I_E=1.6 mA and V_{CC}=4 V) at time t=0. The resulting behavior of collector currents and temperatures is depicted in Fig. 4.5. As can be seen, the pair initially lies in the symmetric condition wherein the current I_E is equally divided between the devices. Subsequently, a bifurcation mechanism occurs, namely, the circuit evolves toward an asymmetric condition that is randomly chosen in an ideally-matched circuit, while being determined by the unavoidable discrepancies between transistors in real pairs [12]. In the case analyzed, the Q_2 branch conducts all the DC current, and the amplifier operates in point A of the VTC shown in Fig. 4.4a.

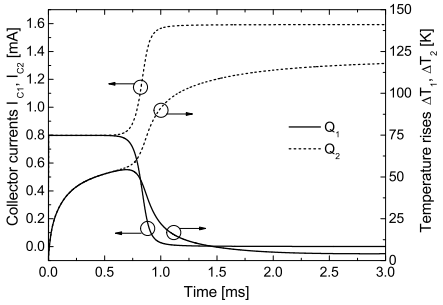


Fig. 4.5. Collector currents I_{C1} (solid line), I_{C2} (dashed) and temperature rises over ambient ΔT_1 (solid), ΔT_2 (dashed) vs. time, as obtained by applying I_E =1.6 mA and V_{CC} =4 V at t=0.

A transient analysis was then carried out for V_{IN}=0 V by applying the DC bias at t=0 and a small AC signal v_{in} with amplitude equal to 5 mV and frequency f=10 kHz at t=10 ms. Isothermal (at T=300 K) simulations revealed that:

- In the DC bias point the tail current I_E is identically partitioned between transistors Q_1 and Q_2.
- The circuit provides a differential-mode gain v_{od}/v_{in} of about -6.73. The behavior of voltage V_{od} is reported in Fig. 4.6.

Considering ET simulations, the pair operates in the previously mentioned hogging condition ($I_{C2} \approx I_E$, $I_{C1} \approx$0A, point A) when the AC signal is applied. As can be evinced from the V_{od} evolution illustrated in Fig. 4.6, the circuit does not behave as an amplifier any longer due to the VTC flattening.

Another transient analysis was performed by applying both the DC bias and AC signal at t=0, and considering various frequency values for v_{in}, namely,

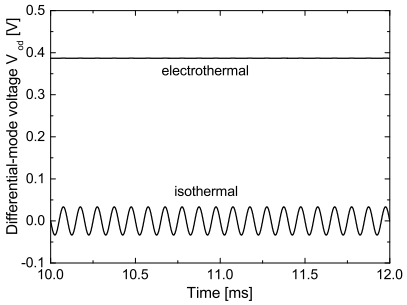


Fig. 4.6. Differential-mode voltage V_{od} as a function of time under isothermal and electrothermal conditions, as obtained by applying the DC bias at t=0 and the AC signal at t=10 ms.

1, 10, and 100 kHz. The evolution of currents I_{C1} and I_{C2} is depicted in Fig. 4.7. It is shown that the differential pair moves to the asymmetric mode at shorter times than in the case without AC signal applied. In particular, the Q_1 side is destined to bear all the DC current since the first halfwave of v_{in} is positive. It can be also observed that the time instant at which the current hogging condition is reached is almost independent of the frequency of signal v_{in}. In this case, the circuit operates in the DC point marked as B in Fig. 4.4a, where it does not behave as an amplifier.

As a rule of the thumb, one should apply proper bias conditions in order to avoid the thermally-induced DC bifurcation at V_{IN}=0 V by following the guidelines drawn in [12]. In particular, it is suggested to cautiously bias the circuit well inside the thermally stable region bounded by the *bifurcation locus* described by Eq. (10) in [12].

4.1.2 Current mirror in silicon-on-glass technology

Current mirrors are commonly recognized as the dominant building blocks in analog ICs. Although these circuits were traditionally used as DC biasing elements, in last decades the analysis of their transient behavior has become crucial in current-mode and mixed-signal applications, where they are subject to large current variations and – if improperly designed – may adversely impact the performance of the entire circuit [221]. A comprehensive study of the influence of ET effects on the behavior of bipolar current mirrors fabricated in SOG [216] and GaAs technologies has been presented in [13] for the steady-state case. It was demonstrated that severe self-heating of the individual devices may not only lead to a poor mirroring of the reference current I_{REF}, but also to a reduction in the safe operating area of the output transistor induced

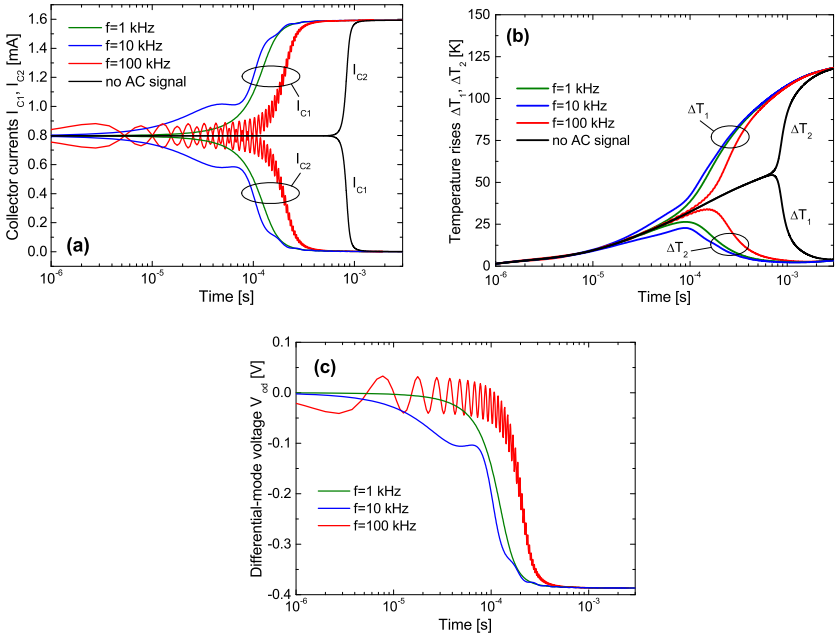


Fig. 4.7. (a) Collector currents I_{C1} and I_{C2}, (b) differential output voltage V_{od}, and (c) temperature rises over ambient ΔT_1 and ΔT_2, versus time for no AC signal (black), and for various frequencies of the AC signal v_{in}, namely, 1 (green), 10 (blue), and 100 (red) kHz, with V_{CC}, I_E, and v_{in} all applied at t=0.

by the occurrence of a flyback phenomenon, i.e., the onset of a negative differential resistance (NDR) branch in the I_{OUT}–V_{OUT} characteristics. The analysis was extended to include dynamic operation.

The bipolar SOG mirror shown in Fig. 4.8 is here considered, with same transistors employed in Section 4.1.1, and PSPICE-compatible macromodels built according to [8, 9, 14]. The input (Q_1) and output (Q_2) transistors are assumed identical; the supply voltage V_{CC} is connected to the Q_2 collector through a load resistance R_L. The current I_{REF} is varied from 0 to I_{REF1}=0.3 mA at t=0 s and from I_{REF1} to I_{REF2}=1 mA at t=150 ms. In this analysis, three combinations of values for the supply voltage and the load resistance are investigated, namely,

1. V_{CC}=5 V, R_L=500 Ω,
2. V_{CC}=5 V, R_L=5000 Ω,
3. V_{CC}=1 V, R_L=100 Ω,

which will lead to a different thermally-induced behavior.

Fig. 4.9 illustrates the ET steady-state I_{OUT}–V_{OUT} characteristics corre-

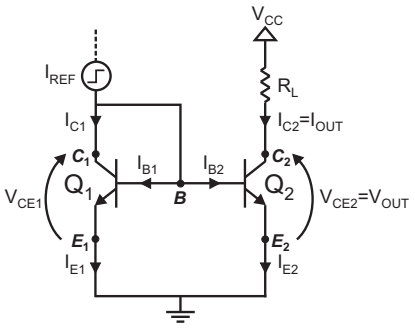


Fig. 4.8. Sketch of the analyzed bipolar current mirror.

sponding to I_{REF1} and I_{REF2}, which exhibit an S-like shape ascribed to the Q_2 heating. It is fairly clear that an increase in the reference current shrinks the safe operating area (SOA) of device Q_2 [13]. For a better understanding of the circuit behavior in Fig. 4.9 are also reported the corresponding isothermal (at T=300 K) curves, as well as the load lines (defined by $V_{OUT}=V_{CC}-R_L \cdot I_{OUT}$). The intersections between the load lines and the ET $I_{OUT}-V_{OUT}$ characteristics identify the quiescent operating points of transistor Q_2, which are designated as $A_{1,2,3}$ (I_{REF1}, case 1,2,3), $B_{1,2,3}$ (I_{REF2}, case 1,2,3). An inspection of the figure reveals that in various conditions (A_1, B_1, B_3) the mirroring action is severely degraded by ET effects, since the steady-state current I_{OUT} is much higher than the applied I_{REF}. Conversely, the normal operation of the circuit would be fully restored under isothermal conditions; in this case, the slight discrepancies between I_{OUT} and I_{REF} would be induced by the Early effect only.

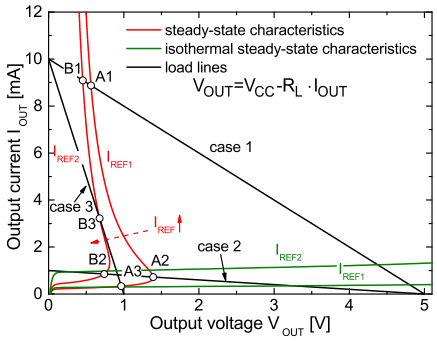


Fig. 4.9. Steady-state ET (red) and isothermal (green) $I_{OUT}-V_{OUT}$ characteristics of transistor Q_2 corresponding to I_{REF1} and I_{REF2}, along with the load lines associated to cases 1, 2, 3 (black).

Fig. 4.10 reports the transient I_{OUT} behavior for all the considered cases, showing that:

- in case 1, I_{OUT} is much larger than the applied I_{REF}, since the load line defines high-current quiescent points well inside the NDR region;
- in case 2, the huge R_L counteracts the transistor self-heating, thus restoring low I_{OUT} values (in particular, I_{OUT} at B_2 almost coincides with the current that would be obtained under isothermal conditions)
- in case 3, the mirror forces a large I_{OUT} transition due to the sharp slope of the load line, leading to a 25 ms-long response – while the expected rise time should be in the order of ns.

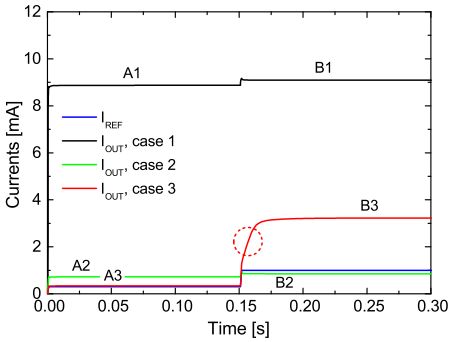


Fig. 4.10. I_{OUT} against time for all the cases analyzed in this work, along with the applied I_{REF} step; the steady-state conditions corresponding to I_{REF1} and I_{REF2} are labeled as in Fig. 4.9.

Fig. 4.11 shows the S-shaped steady-state $\Delta T_2 - V_{OUT}$ curves corresponding to the $I_{OUT} - V_{OUT}$ characteristics depicted in Fig. 4.9, as well as the dynamic ΔT_2 trajectories eventually ending in the quiescent points. The highest temperatures – which are expected to lower the device reliability – are reached for case 1 due to the high V_{CC} and the relatively low R_L. It is surprisingly found that the transition $I_{REF1} - I_{REF2}$, despite the increase in I_{OUT}, entails a ΔT_2 *reduction* for cases 1 and 2. This can be explained by considering that points A_1 and A_2 are associated to a higher V_{OUT} in comparison to B_1 and B_2, respectively, which – prevailing over the lower I_{OUT} – give rise to a higher dissipated power. The opposite behavior is detected for case 3 since the load line identifies a much larger current on the I_{REF2} characteristic (B_3) compared to the I_{REF1} one (A_3), while V_{OUT} remains almost unchanged.

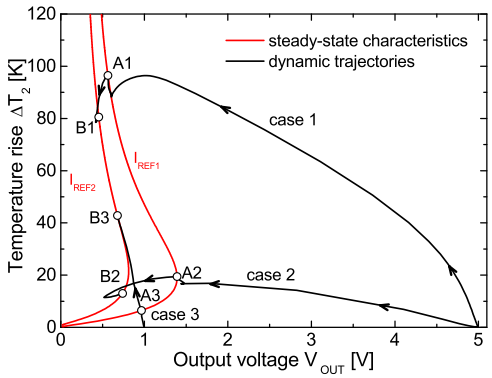


Fig. 4.11. Steady-state ET $\Delta T_2 - V_{OUT}$ characteristics associated to I_{REF1} and I_{REF2} (red), along with the dynamic temperature trajectories for cases 1, 2, 3 (black).

4.1.3 Common emitter amplifier with a SiGe HBT

In the following a dynamic ET analysis for a Common Emitter (CE) amplifier is performed [222]. The active element in the simple CE amplifier depicted in Fig. 4.12 is a SiGe HBT fabricated by Infineon Technologies within the framework of the European Project DOTFIVE [184] with key features maximum cut-off and oscillation frequencies f_T/f_{max}=190/250 GHz, and open-emitter breakdown voltage BV_{CBO}=6.8 V. The emitter area is given by $W_E \times L_E$=0.2×2.67 μm^2, W_E and L_E being the effective emitter width and length, respectively. The intrinsic transistor region is surrounded by shallow and deep trenches filled with electrically – and thermally – insulating materials in order to boost the RF performance [223].

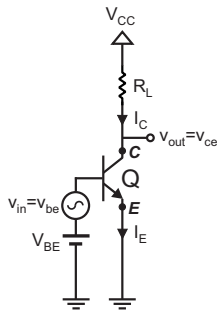


Fig. 4.12. Sketch of the CE amplifier under analysis.

The thermal resistance R_{TH} of the device was determined by a twofold approach, namely,

- Numerically, through 3-D thermal simulation performed with a FEM commercial software package [224]. The thermal conductivities of the materials were initially set to accepted literature values.
- Experimentally, by invoking an improved common-base variant [185, 225], of a classical approach based on simple DC measurements [159].

Unfortunately, a great discrepancy (~42%) arose between the numerical (3250 K/W) and experimental (5600 K/W) R_{TH} values, consistently with results recently obtained for STMicroelectronics transistors [185]. An effort is currently being made to understand the physical reason leading to the numerical underestimation, as also reported in Section 3.4. In order to retrieve the experimental value of R_{TH}, k was reduced to 68 W/mK for the silicon region enclosed by the shallow trench, and that can be ascribed to defects and finite size effects. The transient thermal impedance Z_{TH} was subsequently simulated, and the corresponding Foster network was identified and synthesized as reported in Chapter 2.

The comparison between FEM data, the calculated via the simplified semi-analytical method presented in [226] – in which the thermal problem is represented by considering a rectangular HS in a homogeneous silicon domain with k=140 W/mK superiorly limited by an adiabatic surface –, and their corresponding TFBs are shown in Fig. 4.13. The figure reveals that the FEM Z_{TH} is much higher than that evaluated through the simplified model in [226], although in the latter the cooling emitter contact (accounted for in the first) was replaced by a zero heat flux condition. This is due to the prevailing twofold heating action of the reduced thermal conductivity of the silicon, and the shallow/deep trenches, which inhibit the heat spreading.

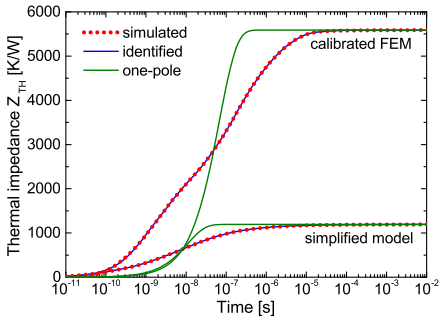


Fig. 4.13. Comparison between simulated (dotted lines) and identified (solid) thermal impedances corresponding to the 3-D FEM simulation and the simplified model proposed in [226].

The CE amplifier was then simulated with PSPICE [39], assuming V_{CC}=2V, V_{BE}=V_B=0.9V and R_L=50 Ω. The SiGe HBT was represented by a subcircuit with parameters calibrated through an extensive experimental campaign. A small AC signal v_{be}(=v_b) with a 2 mV semi-amplitude and assigned frequency was subsequently applied as input. The AC gain and the semi-amplitude of the temperature oscillation as a function of frequency are shown in Fig. 4.14 by accounting for the two aforementioned TFBs; also illustrated is the isothermal AC gain at 300 K . The DC biasing points are given by:

- TFB from FEM – I_C=4.15 mA, ΔT_j=42 K;
- TFB from simplified data – I_C=2.61 mA, ΔT_j=5.8 K;
- Isothermal $\Delta T_j = 0$ – I_C=2.38 mA.

As can be seen, the ET AC gains are both higher than the isothermal one (~2.4) over the whole frequency range. In particular, they reduce with frequency, eventually reaching a constant value beyond 8 GHz. The ET gain being higher the isothermal one is ascribable to:

1. the larger excursion of the output characteristics under ET conditions, as will be detailed in the following;
2. the higher biasing current.

Contribution 1 dominates at lower frequencies, where the temperature can follow the (slow) oscillation of the electrical signals, but lowers beyond 100 kHz, thus leading to a decrease in AC gain. The temperature fluctuations eventually extinguish for frequencies higher than 5 GHz, and the gain reduces to that corresponding to isothermal conditions at $T_j = 342$ K (FEM) or $T_j = 305.8$ K (simplified model), which in both cases is still higher than the T=300 K counterpart due to contribution 2.

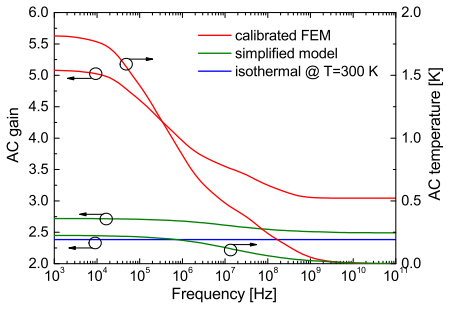


Fig. 4.14. AC gain (left) and temperature (right) of the CE SiGe amplifier by considering the TFBs corresponding to the 3-D FEM simulation (red) and the simplified model proposed in [226] (green); also shown is the AC gain corresponding to T=300 K (blue).

The AC results are corroborated by transient simulations conducted at assigned frequency values; it is confirmed that the amplitude of the dynamic output voltage shrinks with increasing frequency, thus reducing the AC voltage gain. In a similar fashion, the amplitude of the temperature oscillation (around the DC value T_j=341.73 K) reduces with frequency. The analysis depicted in Fig. 4.15 to the case of the FEM-based thermal network.

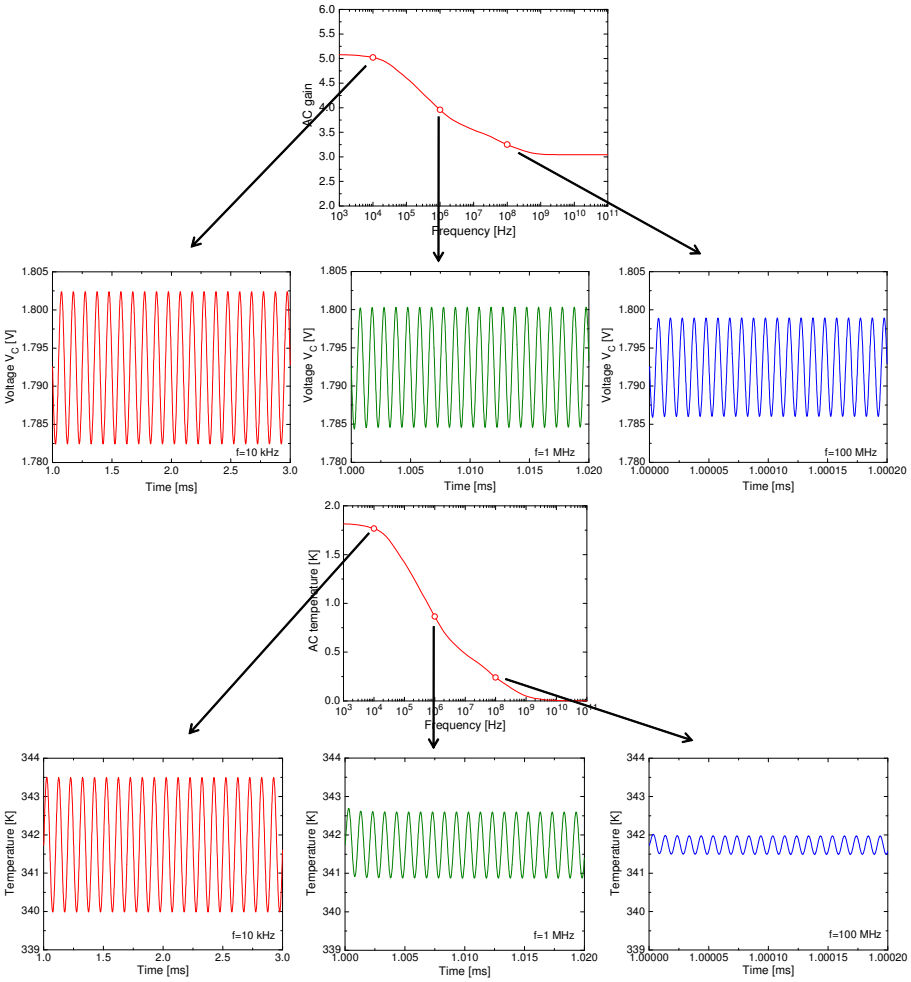


Fig. 4.15. Transient simulations of the CE amplifier: voltage and temperature oscillation at three fixed frequency values.

This behavior can be fully understood by resorting to the plots depicted in Fig. 4.16, in which:

- the black curve is the ET DC characteristic for V_{BE}=0.9 V;
- the red curves are the ET DC characteristics for V_{BE}=0.898 V and 0.902 V (describing the amplifier behavior at *low* frequencies);
- the blue curves are the isothermal (@T_j=341.73 K) DC characteristics for V_{BE}=0.898 V and 0.902 V (describing the amplifier behavior at *high* frequencies);
- the load line is represented in green.

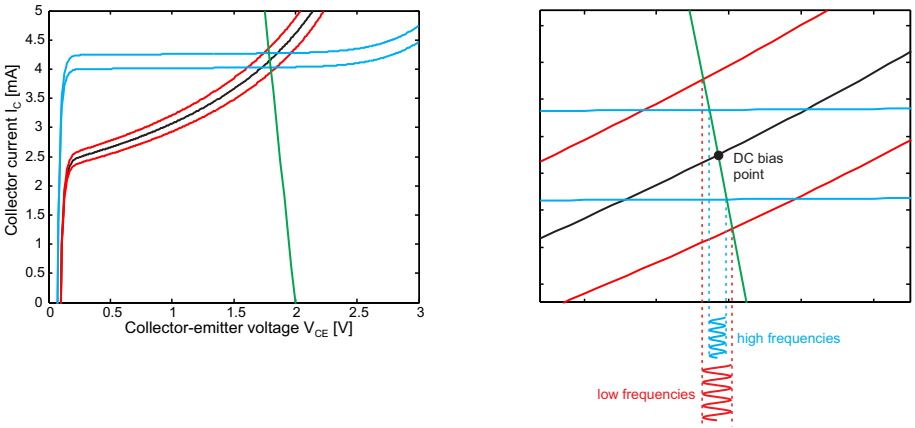


Fig. 4.16. (left) Steady-state I_C–V_{CE} characteristics: ET at V_{BE}=0.9 V (black); ET at V_{BE}=0.898 V and V_{BE}=0.902 V (red); isothermal at the FEM bias temperature for V_{BE}=0.898 V and V_{BE}=0.902 V. (right) Graphical description of the application of a small signal at low frequency in red, and high frequency in blue.

The DC bias point is given by the intersection between the load line and the ET characteristic I_C–V_{CE} at V_{BE}=0.9 V, which exhibits a positive slope induced by self-heating. For low frequencies, the temperature can follow the oscillations of electrical signals, and the dynamic operating point moves along the load line between the ET characteristics corresponding to V_{BE}=0.898 V and V_{BE}=0.902 V. The allowed v_{ce} oscillation amplitude is fairly high, and so is the AC voltage gain (~5). By increasing the frequencies, the dynamic operating point moves between the V_{BE}=0.898 V and V_{BE}=0.902 V characteristics, which are not purely ET any longer, since the temperature is not allowed to reach the DC values at those V_{BE}'s due to the fast variations of the electrical signals. Such characteristics are closer to the DC biasing point, thus reducing the AC voltage gain. For frequencies are higher than 8 GHz, T_j

cannot vary with respect to the DC value (341.73 K), and the operating point moves between the isothermal V_{BE}=0.898 V and V_{BE}=0.902 V characteristics at T_j=341.73 K; as a result, the AC gain is the same which would be obtained under isothermal conditions at T_j=341.73 K (~3), still greater than the isothermal AC gain at T_j=300 K due to the higher collector current at the bias point.

4.2 Interconnect line in UTCS

The structure for a 2-layer UTCS module described in Section 2.6 can be extended to account for an interconnect between the two chips as sketched in Fig. 4.17a, with face-to-face active circuitry regions of the chips connected by two tungsten vias and a 2-μm-thick copper line [114]; Fig. 4.17b reports an illustrative 3-D view of the active regions of the chips and the interconnect scheme.

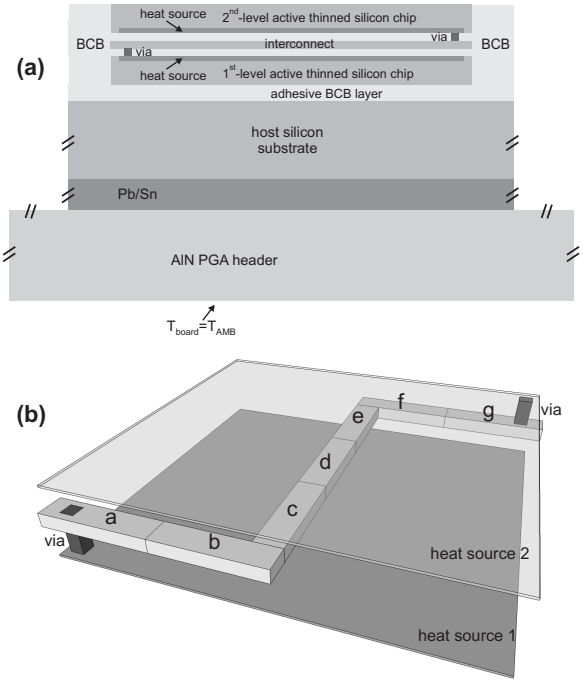


Fig. 4.17. (a) Cross-section of the analyzed 2-chip module in UTCS technology, and (b) illustrative 3-D view of the thermal representation of the circuitries lying on the chips and the interconnect scheme.

The module was thermally modeled by partitioning the (long) copper line into seven individual elements – identified with letters “a”, “b”, . . . , “g”; two additional HSs (1 and 2) were assumed to describe the circuitries embedded in the chips. Fig. 4.18 shows the mesh of the 2-chip module, comprising about 1.7×10^6 tetrahedra and involving 2.4×10^6 DoFs. A transient thermal simulation over 64 logarithmically-spaced time instants was found to last nearly 10 hours on a workstation equipped with 2 hexacore 2.43 GHz CPUs and 100 GB RAM.

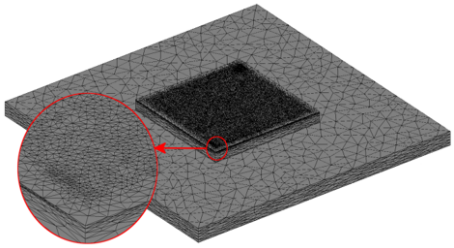


Fig. 4.18. Comsol mesh of the analyzed 2-chip module with a detail in the inset. No symmetry was available to be exploited.

Fig. 4.19 depicts the time evolution of the self-heating and mutual thermal impedances computed by activating the 1st-level chip, as obtained by 3-D FEM simulations and from a Multi-port TFB. The following observations are in order:

- the individual line elements designated as “g” and “a” are more heat-sensitive wrt the others due to their close proximity with the adiabatic lateral walls of the domain;
- in particular, element “g” owns the worst heat dissipation capability since it is connected to the 2nd-level chip, which suffers from the adiabatic condition at the top surface of the module;
- the other elements of the copper line are located far away from the vias, thus exhibiting an almost symmetrical behavior, the lowest thermal impedance being shared by the central sources “c”, “d”, and “e”, which are marginally affected by the lateral boundaries.

The TFB was then used to perform an ET simulation of the interconnect between the two chips. The copper line was modeled with the standard ladder RC circuit (e.g., [17,227]) that was connected to the TFB; in particular, the values of the resistance and capacitances associated to the individual line elements were evaluated as suggested in [228] and [229], respectively. The temperature

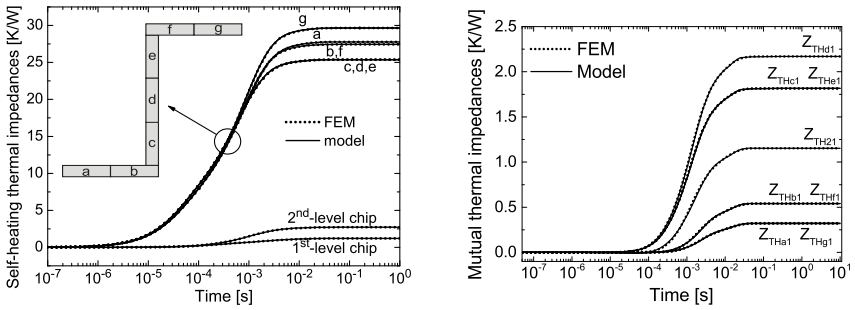


Fig. 4.19. (left) Self-heating thermal impedances, and (right) mutual thermal impedances obtained by activating the 1st-level chip, for the heat sources involved in the analyzed structure, namely, the circuitries embedded in the stacked chips, and the elements of the copper line (shown in the inset); numerical data (dot lines) are compared to results obtained with the synthesized network (solid).

dependent resistors – the TC of which is assumed equal to 4 mΩ/K [228, 230] – was implemented by replacing the traditional PSPICE "R" parts with Analog Behavioral Modeling (ABM) sources suited (i) to force a voltage drop depending on both the flowing current and the temperature computed by the TFB, as well as (ii) to evaluate the dissipated power that is in turn provided to the TFB. The coupled ET circuit is shown in Fig. 4.20. It can be exploited to accurately estimate in a few seconds the heating impact upon the propagation of a signal through the interconnect line [17, 227, 230] by varying within practical ranges the time evolution and level of the powers dissipated by the active chips, and the frequency of the signal. This analysis is recognized to be very important for the design of the interconnect system from a signal integrity viewpoint, since a significant thermally-induced propagation delay may lead to timing violation or clock skew [19].

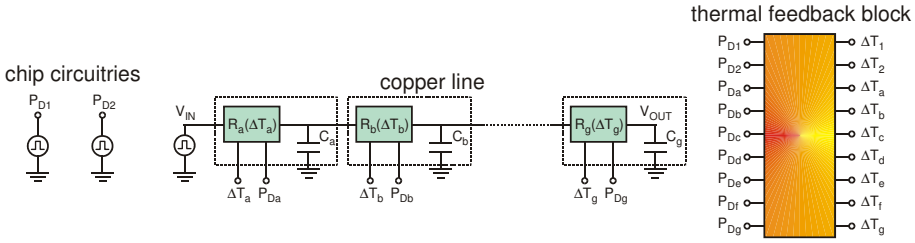


Fig. 4.20. Circuit for ET simulation of the interconnect line in Fig. 4.17 with temperature-dependent resistors and the extracted TFB.

A simulation was carried out by assuming that the active regions of the buried and top chips dissipate P_{D1}=45 W and P_{D2}=15 W, respectively, within different periods as depicted in Fig. 4.21a, along with the corresponding temperature rises over ambient ΔT_1 and ΔT_2 evaluated by the TFB. The temperature evolutions of the line elements are illustrated in Fig. 4.21b: a nonuniform temperature field takes place over the line, which peaks over the central portion and sharply decreases along the outer elements. The ET analysis was conducted over ns-wide time intervals starting at chosen instants associated to different heating conditions and identified in Fig. 4.21a, namely,

- t_1=0.11 s (only P_{D1} switched on, rising temperatures)
- t_2=0.20 s (only P_{D1} switched on, steady-state temperatures)
- t_3=0.41 s (P_{D1} and P_{D2} switched on, rising temperatures)
- t_4=0.50 s (P_{D1} and P_{D2} switched on, steady-state temperatures)

Fig. 4.21c details the temperature increments for the elements of the copper line due to P_{D1} and P_{D2} at the aforementioned instants.

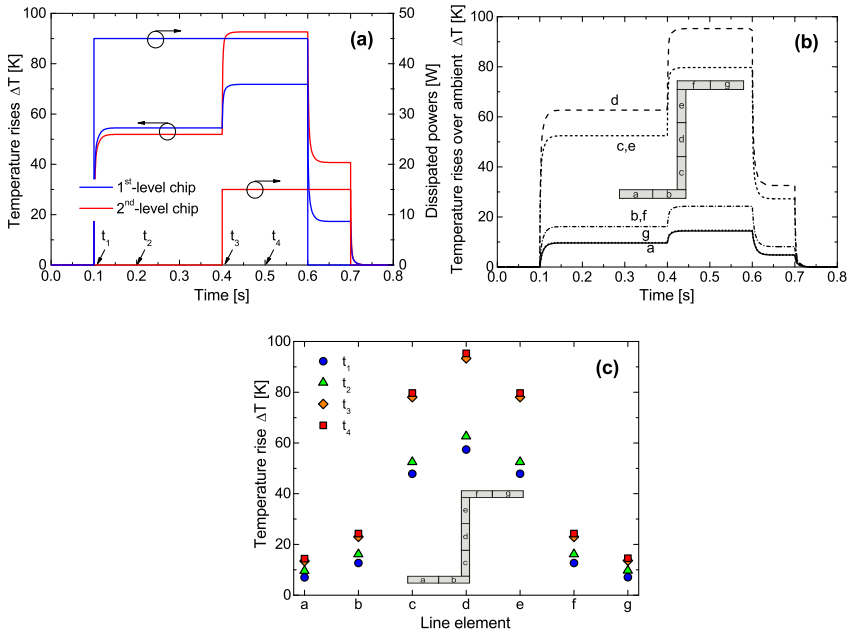


Fig. 4.21. (a) Temperature rises over ambient and dissipated power pulses against time for the two stacked silicon chips. Temperature rises over ambient due to the heat emerging from the dissipating chip circuitries for the elements of the interconnect line (shown in the inset), as obtained (b) through a PSPICE simulation versus time, and (c) along the line at fixed time istants.

The ET impact on the interconnect was investigated by applying to the line input a digital signal V_{IN} with 1 V amplitude and 1 GHz frequency with a 50% duty cycle, and by monitoring the output voltage V_{OUT}. Results are reported in Fig. 4.22a, which shows the high-low delays t_{PHL} corresponding to the assigned time instants, as well as the one that would be obtained under isothermal conditions at T=300 K (10 ps). As can be seen, as the temperature field increases over the line, the elementary resistances, and thus the delay, steadily grows; in particular, t_{PHL} is found to span from about 11.2 ps at t_1 (with a 12% rise) up to 12 ps at t_4 (20%). It can be therefore concluded that disregarding ET effects may lead to a significant underestimation of the actual delay. The transient V_{OUT} behavior against time for cases t_1 and t_4 is depicted in Fig. 4.22b, along with the ideal isothermal behavior.

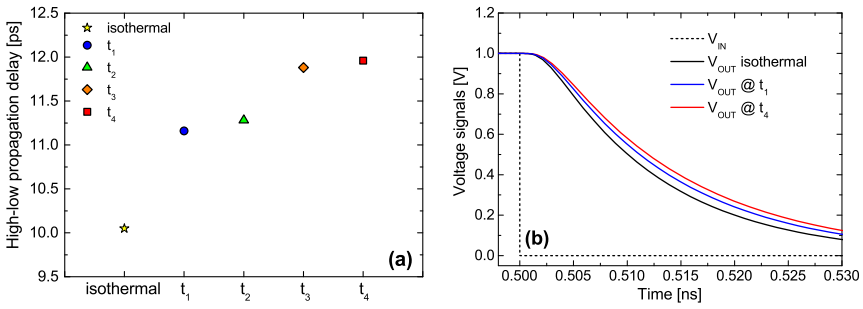


Fig. 4.22. (a) High-low delays of a digital 1-GHz voltage signal propagating along the interconnect line from the time instants shown in Fig. 4.21a; (b) V_{OUT} evolution for the t_1, t_4 cases, along with V_{IN}.

4.3 Unclamped Inductive Switching Test of a IGBT

Significant information on the physics underlying the behavior of an IGBT during the UIS test – described in Section 1.1 – can be in principle gained by high-granularity simulations accurately accounting for ET and II effects. The approach relying on TFB described in Section 1.2 is applied to explore the relation between the avalanche I–V characteristic of a 1.2 kV-rated IGBT with three emitter pads manufactured by Toyota and its behavior during the UIS transient, with particular emphasis on the occurrence of the hopping phenomenon [231].

4.3.1 TFB and electrical model

The device was discretized into 12 × 9 square cells so as to allow the description of uneven current and temperature field as depicted in Fig. 4.23.

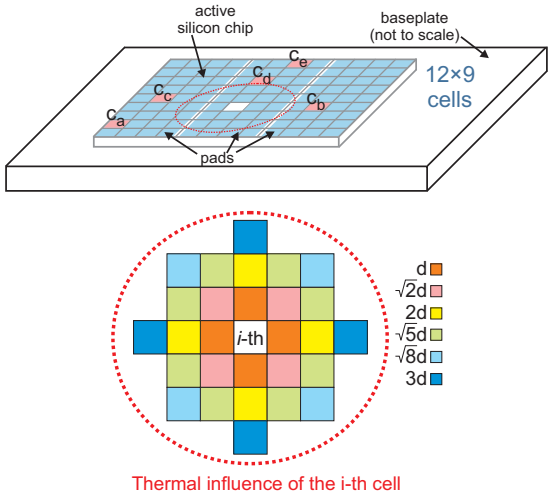


Fig. 4.23. (Top) Sketch of the IGBT structure partitioned into 12 × 9 elementary cells, highlighting the pads and the cells monitored in Fig. 4.26. (Bottom) Scheme illustrating all the cells thermally influenced by the i-th one. For the surrounding cells, also indicated is the correlation between color and center-to-center spacing from the i-th.

The identification and synthesis procedure was simplified by the following considerations:

- The same self-heating thermal impedance Z_{THii} is assumed *for all the cells*. This assumption is reasonable since the Z_{THii} of the inner 10 × 7 cells are almost identical, whereas those associated to the 38 cells located along the border are only slightly higher due to the adiabatic silicon boundary that partially inhibits the lateral heat flow.
- With the chosen discretization, an arbitrary i-th cell influences only a few surrounding cells from a thermal viewpoint. In particular, if d denotes the center-to-center spacing between the power-dissipating i-th cell and an adjacent one, the temperature rise over cells far from the i-th by more than $3d$ can be disregarded. A pictorial scheme illustrating the cells thermally impacted by the i-th is sketched in Fig. 4.23, where it is highlighted that cells sharing the same distance undergo the same thermal coupling: as a result, only 6 mutual thermal impedances

$Z_{THji}(j \neq i)$ are to be determined for each cell. Furthermore it can be seen that the $Z_{THji}(j \neq i)$ are almost coinciding regardless of the position of the i-th cell.

The output was given in a Foster network topology, since it allows to efficiently model a limited coupling between the cells (as reported in Section 2.5) [87].

The elecrical macromodel for each cell is obtained by suitably modifying the IGBT model proposed in [232]. The avalanche current I_{CAV} is generated by a nonlinear controlled source as $I_{CAV} = (M_{AV} - 1) \cdot (I_{CT} + I_{leak})$, where I_{CT} is the collector (i.e., anode) current in the absence of II effects, I_{leak} is a leakage current, and M_{AV} is the avalanche multiplication factor expressed as

$$M_{AV} = \exp\left(b_{AV} \cdot f_I \cdot \frac{V_{CE} - R_{AV} \cdot I_C}{f_T \cdot BV}\right) \tag{4.1}$$

In (4.1), I_C is the collector current (=I_{CT} + I_{CAV}), BV is the breakdown voltage at ambient temperature, b_{AV} and R_{AV} (Ω) are fitting parameters, the latter being used to describe the positive differential resistance (PDR) region in the I–V curves; f_T is a term that allows accounting for the PTC of BV and given by

$$f_T = \exp\left(a_{AV} \cdot \Delta T\right) \tag{4.2}$$

a_{AV} (K^{-1}) being a fitting parameter; f_I is a term that allows creating a negative differential resistance (NDR) branch expressed as

$$f_I = \exp\left\{c_{AV} \cdot \exp\left[d_{AV} \cdot \left(1 - \frac{I_C}{I_{CS}}\right)\right] \cdot I_C\right\} \tag{4.3}$$

where c_{AV} (A^{-1}), d_{AV}, and I_{CS} (A) are fitting parameters. It must be noted that $f_I \rightarrow 1$ for $I_C \gg I_{CS}$.

The individual subcircuits were electrically linked by short-circuiting gates and collectors, and connecting all emitters (i.e., cathodes) through a resistance network to account for the de-biasing effect across the metallization pattern; in particular, very high values were set for the resistances between the emitters of cells located on the borders of two different pads. The bond wires (i.e., the electrical grounds) were placed at the centers of the pads. Conversely, the interconnections among internal nodes belonging to different cells were disregarded.

The I_C–V_{CE} characteristic corresponding to V_{GE} = 0 V is defined as *avalanche curve*, and its shape determined by several technological parameters, e.g., doping profiles, lifetime control techniques, as well as trench position and depth, depending on the power device. The impact of the shape upon the UIS behavior was investigated by tailoring the parameters of the avalanche

multiplication factor M_{AV} so as to obtain the curves depicted in Fig. 4.24 along with the current $I_{C,MAX}$ = 27 A imposed at the turn-off beginning. It is shown that $I_{C,MAX}$ identifies 3 initial operating points lying on different regions of the characteristics, namely,

(A) a PDR branch,
(B) a low-slope NDR region upwardly limited by a flyback point followed by a PDR behavior at higher currents, and
(C) a full NDR region.

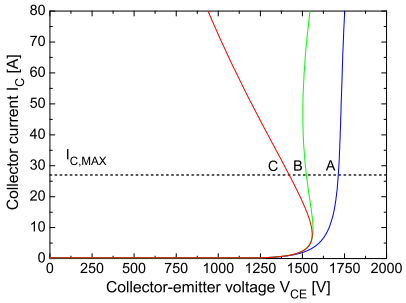


Fig. 4.24. Differently-shaped I_C-V_{CE} curves at V_{GE}=0 V and T=300 K; $I_{C,MAX}$ is the collector current at the beginning of the UIS transient.

Case A is expected to favor a uniform current distribution due to the stabilizing action of the PTC of voltage BV [3, 233], whereas cases B and C are likely to entail a current constriction mechanism, as reported in the basic papers [234, 235], as well as in [3, 31, 33, 233]. UIS simulations were performed by applying a supply voltage V_{CC} = 650 V and an inductor L = 4.4 mH, and were found to last only 2 minutes on a normal PC, although the maximum time step was set to 100 ns. Fig. 4.25 depicts the sustaining voltage BV and the total collector current for the cases reported in Fig. 4.24.

The results can be summarized as follows.

In case A, the expected behavior is monitored: BV first increases and then reduces as the current tends to extinguish, while the individual currents and temperatures are evenly distributed across the cells; in particular, a peak in temperature rise above ambient of 130 K is observed.

In case C, BV rapidly increases for 70 μs and then a convergence problem is encountered. An inspection of the simulated current/temperature maps reveals that the NDR operating point triggers a *hogging condition*, in which some circumscribed groups of cells try to bear the whole current. These filaments keep shrinking until the involved areas become smaller than the cell size,

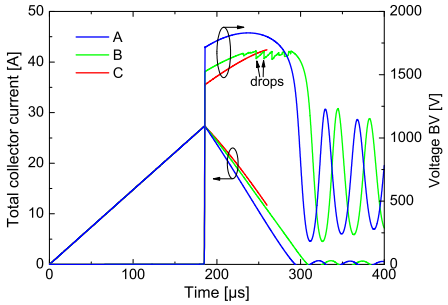


Fig. 4.25. Transient evolution of the total collector current (left) and of the avalanche-sustaining voltage (right) for cases A, B, and C. Two voltage drops are evidenced in the time interval where BV manifests a sawtooth-like behavior.

eventually entailing a convergence failure, which corresponds to a catastrophic destruction in a real device [3]. An interesting result is obtained for case B; it is found that, after about 40 µs from the UIS beginning, the sustaining voltage starts exhibiting an irregular behavior characterized by sudden drops. Consistently with previous findings [33], a *hopping phenomenon* is shown to take place, as illustrated in Fig. 4.26, which represents the evolutions of the individual collector currents and temperature rises of selected cells (identified in Fig. 4.23) during the UIS discharging.

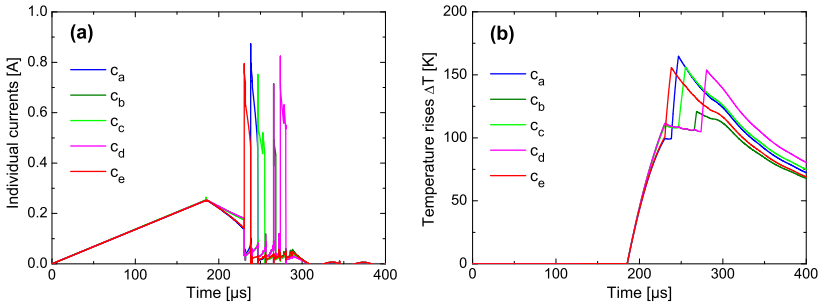


Fig. 4.26. Transient evolutions of (a) individual collector currents and (b) temperature rises over ambient for the cells identified in Fig. 4.23.

The following considerations – based on an extensive simulation campaign – can be made.

The hopping phenomenon can be ascribed to the S-like shape of the avalanche curves of the individual cells, and, in particular, to the high-current flyback behavior that restores a stabilizing PDR region, which – supported by the PTC of the BV voltage – may yield sudden jumps of the dynamic operating

points on each characteristic [33]. The hopping sequence is unpredictable due to the significant dependence on active area discretization, position of bond wires, emitter de-biasing, and small technological discrepancies among the cells; this likely applies to any simulation approach. The temperature peak over the device in case B can be far higher than that corresponding to case A; the computed thermal maps reveal that some cells heat up to more than 160 K over ambient (Fig. 4.26b); in particular, it was found that the peak value is relatively insensitive to discretization, moderate variations in emitter de-biasing, and cell discrepancies, whilst the cell(s) where the temperature peak takes place may change. Thus – although not usually leading to an irreversible device failure – case B unavoidably entails a reduction in sustainable energy and reliability. PSPICE simulations were found to be well-suited to capture the hopping occurrence and estimate a trustworthy temperature peak over the device. Similar simulations were performed by making use of the approach proposed in [31, 233], where the same discretization was considered for the electrical solver, and the CPU time was found to be more than 10 hours on a high-performance workstation.

Fig. 4.27 illustrate the collector current distribution determined before and after the two BV drops indicated in Fig. 4.25, and offer further evidence of the correlation between BV fluctuations and hopping.

- Before the first drop, the current is almost completely conducted by a few cells near the corners, when suddenly other cells close to the boundary switch on.
- Before the second BV drop various cells close to the border are bearing the whole current, when this condition is abruptly replaced by another in which all these cells become dry and the current entirely flows through the central area.

Experiments over a test IGBT structure coinciding with that analyzed in the previous sections were performed by a nondestructive in-house UIS tester and an IR camera with 50 Hz frame rate [236]. In particular, V_{CC} = 160 V, L = 10 mH were applied, and a turn-off current $I_{C,MAX}$ = 19.5 A was imposed. Simulations were conducted by adjusting the II model so that the avalanche curve of the whole device matches the experimental characteristic obtained through a transmission-line pulse system and placing electrical grounds in correspondence to the position of the bond wires. Fig. 4.28 shows the evolutions of total collector current and avalanche voltage during UIS discharging, as determined experimentally and through PSPICE simulations.

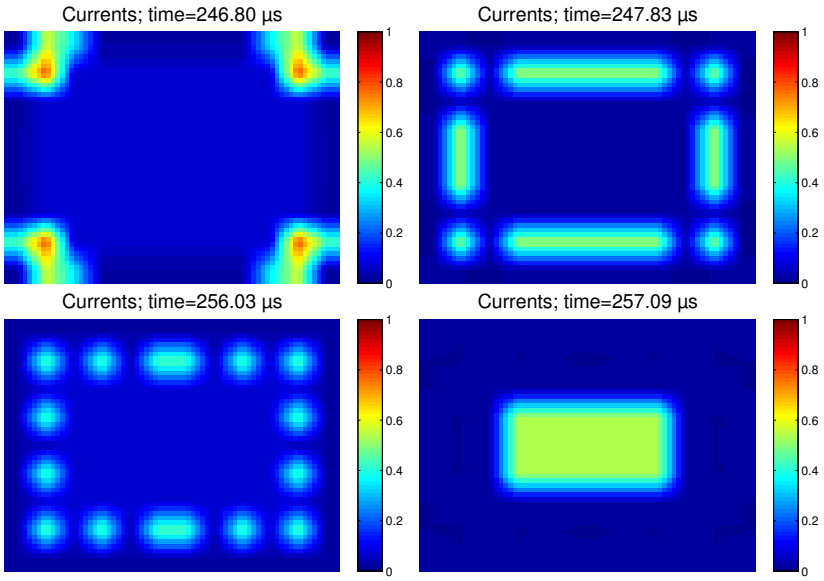


Fig. 4.27. Case B: current distribution over the active silicon area before (left) and after (right) the first (top), and second (bottom) BV drops indicated in Fig. 4.25.

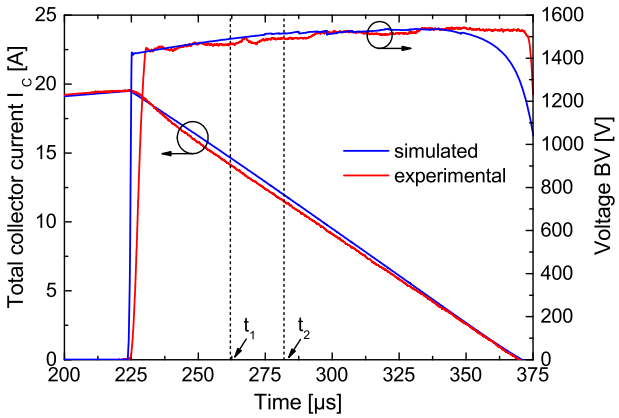


Fig. 4.28. Experimental and simulated transient evolution of the total collector current (left) and of the avalanche-sustaining voltage (right) during the UIS test for $I_{C,MAX}$ = 19.5 A. Also shown are the time instants t_1 and t_2 at which the temperature maps in Fig. 4.29 are taken.

The temperature maps illustrated in Fig. 4.29, obtained after 40 µs (t_1) and 60 µs (t_2) after the UIS beginning, provide overwhelming evidence of a hopping phenomenon, since the area subject to the maximum temperature moves from the right to the left pad. With the adopted approach it was possible to foresee the hopping triggering with a temperature peak slightly higher than the measured one, as illustrated in Fig. 4.30 (it is to be noted that the real device benefits from the cooling action of convection), while missing the exact transient temperature distribution.

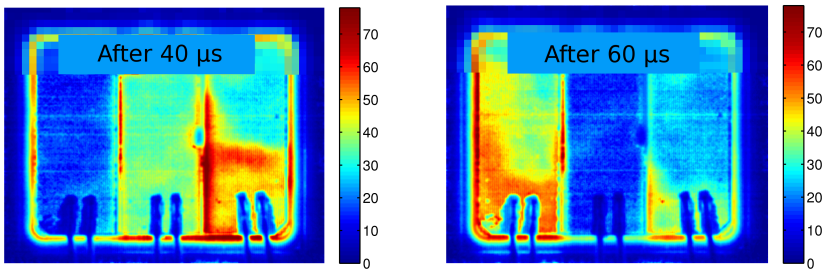


Fig. 4.29. IR temperature maps detected 40 µs (top) and 60 µs (bottom) after the UIS beginning for a turn-off current $I_{C,MAX}$=20 A.

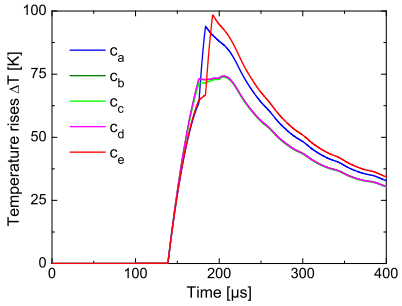


Fig. 4.30. Transient temperature rises over ambient for the cells identified in Fig. 4.23, as simulated by reproducing the experimental UIS conditions for the test IGBT shown in Fig. 4.28.

4.4 SC test of a SiC power MOSFET

Silicon carbide (SiC) power devices are promising candidates for energy distribution, as well as for automotive, aircraft, and spacecraft applications, thanks to their inherent features like high breakdown voltage, low on-state resistance, and excellent high-temperature capability [237]. Owing to the fact that SiC

transistors often operate under critical conditions, reliable simulation tools accounting for ET effects are needed for design optimization. However, this is a challenging task since the temperature dependences of the key parameters are rather different compared to traditional Si devices (e.g., the impact of SiC/SiO_2 interface traps must be taken into account).

In this section, the dynamic Short Circuit (SC) test of a 1200V 50 A 4H-SiC power MOSFET – manufactured by CREE [238] and depicted in Fig. 4.31 – is analyzed and simulated following the approach described in Section 1.2.

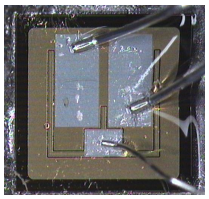


Fig. 4.31. Top-view picture of the SiC power MOSFET under test.

Thermal model

The DUT is subdivided into an assigned number of cells, as it was done for the IGBT in the previous Section. The device structure and the corresponding mesh – discretized into 200 cells – are shown in Fig. 4.32.

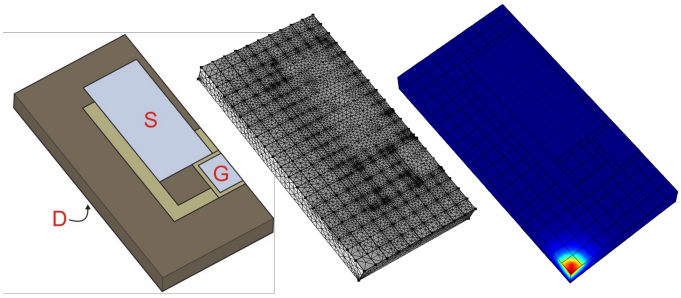


Fig. 4.32. Half device structure implemented in Comsol in draw mode, mesh comprising 1.2×10^5 elements (tetrahedra), and a simulation example obtained by activating the corner cell.

Only half a device was simulated due to symmetry, the missing portion being virtually restored by imposing an adiabatic condition over the plane of symmetry. The thermal conductivity of 4H-SiC was set to 250 W/mK; higher

values were found to lead to an underestimation of ET effects with respect to the experimental SC data reported in the following. Each of the 175 cells belonging to the active area is associated to an individual heat source. A Foster TFB was identified and subsequently synthesized. The Kirchhoff transformation [170,171] was implemented to account for the temperature dependence of the thermal conductivity by including 175 additional ABMs. It is worth noting that this is reasonable since a *bare die* device is considered, in which k_{SiC} play the most important role.

Transistor model

The model employed for the transistor cell is a variant of the classic Level 1 enriched to account for the temperature dependences of the relevant physical parameters [239]. Let T and T_0 be the temperature (assumed uniform) of the cell and the ambient temperature (27°C), respectively. The negative temperature coefficient (NTC) of the threshold voltage is described by the linear law

$$V_{TH}(T) = V_{TH}(T_0) - \varphi_{TH} \cdot (T - T_0) \tag{4.4}$$

where φ_{TH} is a fitting parameter.

The temperature dependence of the electron mobility in the channel is enabled through the power relationship

$$\mu_n(T) = \mu_n(T_0) \cdot \left(\frac{T}{T_0}\right)^{-m(T)} \tag{4.5}$$

the exponent *m* being given by

$$m = -a_m + (a_m + b_m) \cdot [1 - c_m \cdot \exp(-d_m \cdot T/T_0)] \tag{4.6}$$

where a_m, b_m, c_m, and d_m are fitting parameters.

The resistance of the lightly-doped drift region was modeled through the following expression:

$$R_D(V_{GS}, V_{drift}, T) = R_{D0}(T) + R_{D1}(T) \cdot \frac{V_{drift}}{V_1 + V_{drift}} \cdot \left(\frac{V_{GS}}{V_2}\right)^{-r} \tag{4.7}$$

where V_{drift}=V_{DS}-V_{ch} is the voltage drop across R_D, V_{ch} being the drop across the channel, and R_{D0}(T), R_{D1}(T) are given by

$$R_{D0}(T) = R_{D0}(T_0) \cdot \left(\frac{T}{T_0}\right)^{r_0} \tag{4.8}$$

$$R_{D1}(T) = R_{D1}(T_0) \cdot \left(\frac{T}{T_0}\right)^{r_1} \tag{4.9}$$

V_1, V_2, r, r_0, and r_1 being fitting parameters.

II effects are activated by multiplying the II-unaffected drain current by the avalanche factor [7]

$$M = 1 + a_{II} \tan\left[f_I\left(I_D\right) \cdot \frac{\pi}{2} \left(\frac{V_{DS}}{BV_{DS}\left(T\right)} \right)^{b_{II}} \right] \tag{4.10}$$

where BV_{DS} is the breakdown voltage, given by

$$BV_{DS}\left(T\right) = BV_{DS}\left(T_0\right) \cdot \exp\left[c_{II} \cdot \left(T - T_0\right)\right] \tag{4.11}$$

and f_I is a nondimensional term needed to account for the current dependence of M; a_{II}, b_{II}, and c_{II} are fitting parameters.

Subcircuit

A sketch of the cell subcircuit is represented in Fig. 4.33.

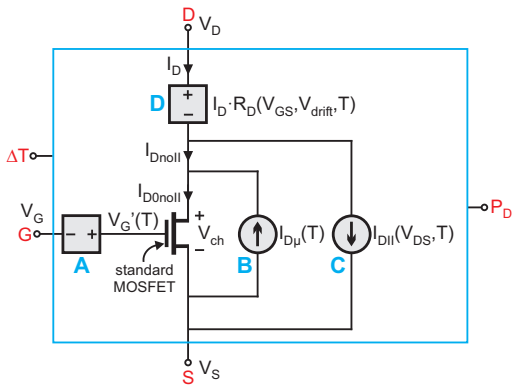


Fig. 4.33. Sketch of the subcircuit implementing the transistor model.

In order to activate the temperature-induced V_{TH} reduction described by (4.4), source **A** in series with the gate adds the voltage $\varphi \cdot \Delta T$ to V_G so that the overdrive voltage becomes

$$\begin{aligned} V_G{}' - V_S - V_{TH}\left(T_0\right) &= V_G + \varphi_{TH} \cdot \Delta T - V_S - V_{TH}\left(T_0\right) = \\ &= V_G - V_S - \left[V_{TH}\left(T_0\right) - \varphi_{TH} \cdot \Delta T\right] = V_{GS} - V_{TH}\left(T\right) \end{aligned} \tag{4.12}$$

Let us define as I_{D0noII} the II-free drain current conducted by the $V_{GS'}$-biased standard MOSFET, the mobility of which is $\mu_n(T_0)$. The relationship (4.5) is enabled by subtracting to I_{D0noII} the current $I_{D\mu}$ generated by source **B** given

by

$$I_{D\mu} = I_{D0noII} \cdot \left[1 - \left(\frac{T_0 + \Delta T}{T_0} \right)^{-m(T)} \right] \tag{4.13}$$

so that the II-free current I_{DnoII} becomes

$$I_{DnoII} = I_{D0noII} - I_{D\mu} = I_{D0noII} \cdot \left(\frac{T_0 + \Delta T}{T_0} \right)^{-m(T)} \tag{4.14}$$

Avalanching effects are included by adding to I_{DnoII} an II-induced current I_{DII} given by

$$I_{DII} = (M - 1) \cdot I_{D0noII} \tag{4.15}$$

which is calculated by source **C** according to (4.10); as a result, the drain current I_D at the cell terminal is

$$I_D = I_{DnoII} + I_{DII} = M \cdot I_{D0noII} \tag{4.16}$$

The bias- and temperature-dependent drift resistance given by (4.7) is taken into account by making use of source **D** that imposes the voltage drop $I_D \cdot R_D(V_{GS}, V_{drift}, T)$. The power $V_{DS} \cdot I_D$ dissipated by the cell is provided to the TFB to allow for the calculation of the temperature field.

Parameter extraction

The parameters in (4.4)–(4.6) were extracted from the isothermal I_D–V_{GS} transfer characteristics measured at various T_B by keeping constant V_{DS}, as reported in Fig. 4.34. The isothermal measurements were performed by means of an in-house 250 A-rated curve tracer suited to apply down to 1 μs-wide current pulses.

By applying the *quadratic extrapolation method* [240], it was found that:

- The device exhibits high values for $V_{TH}(T_0)$ (=6.3 V) and φ_{TH} (=18 mV/°C) compared to similarly-rated Si power MOSFETs. Both findings were attributed to the high density of SiO_2/SiC interface traps [241,242]. In particular, the fast V_{TH} reduction with temperature – due to the emission of inversion electrons from the traps – entails a severe PTC for I_D, which in turn exacerbates the ET feedback [243].
- The mobility μ_n is subject to a PTC at low temperatures, and to a NTC at high temperatures. This was again ascribed to the interface traps [244–246]. The TC of μ_n in a SiC power MOSFET is indeed due to the interplay between (i) the Coulomb scattering with the filled traps, leading to a PTC induced by the trap discharging with increasing tempera-

ture, and (ii) the acoustic-phonon scattering yielding an NTC, where (i) and (ii) prevail at low and high temperatures, respectively. Such a behavior is accurately described by the novel formulation (4.6) for power factor *m*, which is instead considered positive and temperature-independent for Si MOSFETs, where mechanism (i) is practically absent.

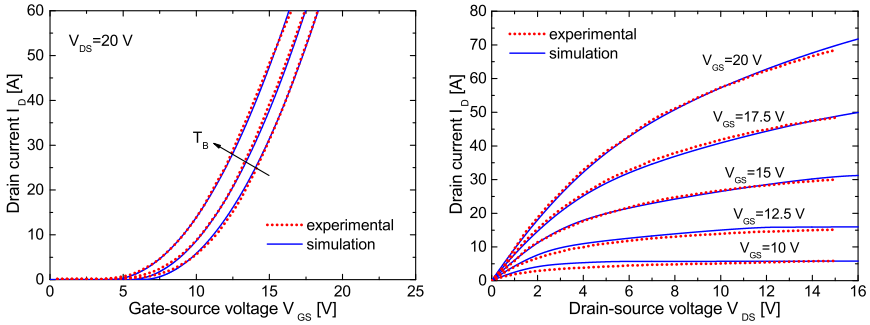


Fig. 4.34. Experimental (red dotted) vs. simulated (solid blue): (a) transfer characteristics at T_B =30, 75, and 150°C; (b) output characteristics for various V_{GS} values at T_B =30°C.

The drift resistance parameters in (4.7) were determined by comparing the model with the isothermal I_D–V_{DS} output characteristics obtained at various T_B by varying V_{GS}. Fig. 4.34b depicts the curve family at T_B=30°C, which evidences the gradual transition from linear to saturation region, typical of SiC power MOSFETs.

The calibrated subcircuit was adopted to evaluate the temperature coefficient of the drain current given by

$$\alpha_T = \left.\frac{\partial I_D}{\partial T}\right|_{V_{DS}} \tag{4.17}$$

with and without the traps-induced effects on the TCs of V_{TH} and μ_n; in particular, such effects were annihilated by reducing φ_{TH} from 18 to 3 mV/°C [247], and setting c_m=0 in (4.6) so as to eliminate the impact of Coulomb scattering on μ_n. Fig. 4.35 shows that the traps lead to a detrimental highly-positive α_T within a broad range of currents and temperatures.

Short-circuit test: simulation and experiment

The SC capability of the DUT was experimentally evaluated at various combinations of gate and supply voltages, by a custom 3 kA, 1.7 kV-rated tester

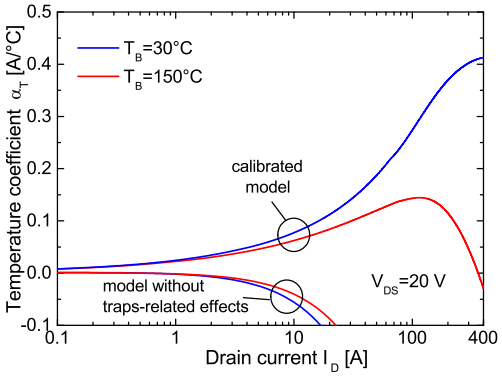


Fig. 4.35. Temperature coefficient of the drain current for the DUT at T_B=30 (solid lines) and 150°C (dashed) with and without the traps-induced effects on the TCs of threshold voltage and electron mobility.

featuring stray inductance of 250 nH, and handled by an FPGA-based circuit ensuring a 20 ns resolution for the gate voltage pulse [248].

The simulation of an SC test over several tens of μs was found to last less than 50 s. Fig. 4.37 reveals that for medium/high V_{GS} values the drain current I_D first increases due to the PTC induced by the reduction in threshold voltage and in Coulomb scattering, and then smoothly decreases since the NTC triggered by the acoustic-phonon scattering dominates [249]. The I_D evolution corresponding to φ_{TH}=3 mV/°C and c_m=0 for the case V_{DD}=100 V and V_{GS}=19 V is also reported, which provides overwhelming evidence that disregarding the effects of the interface traps leads to a dramatic simulation inaccuracy. Fig. 4.37 also reports the temperature and current density maps at chosen points of the SC curves where the behavior is dictated by the PTC. Almost uniform distributions are found regardless of biasing conditions and selected time instants, which witnesses that the layout is properly designed.

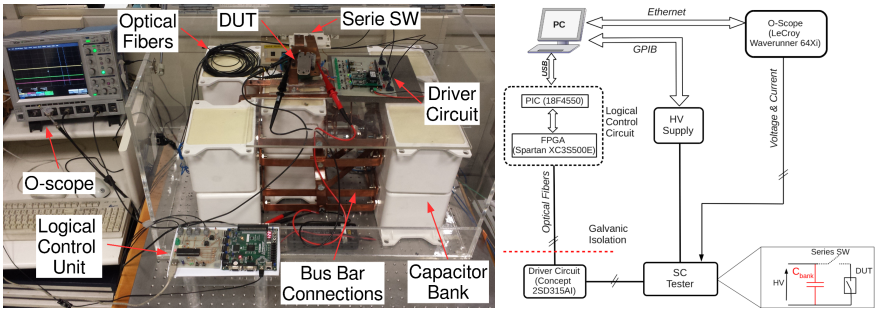


Fig. 4.36. Experimental SC tester [248].

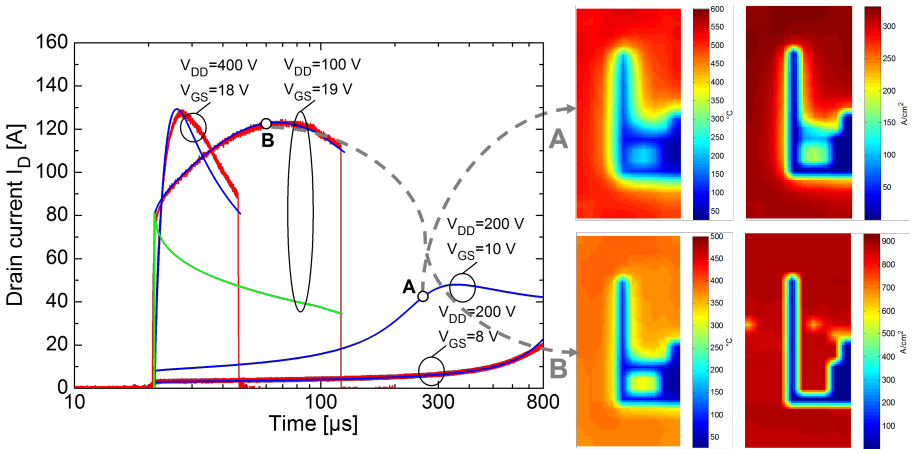


Fig. 4.37. (left) Time evolution of the drain current during short-circuit tests carried out for various combinations of V_{DD} and V_{GS} ; experimental data (red lines) are compared to PSPICE simulations (blue); also shown is the behavior that would be obtained by neglecting the traps-induced effects for the case V_{DD}=100 V, V_{GS}=19 V (green). (right) Temperature and current maps for points A and B.

This allows explaining the experimental observation that the DUT can sustain high dissipated powers without failure occurrences.

4.5 String of photovoltaic panels subject to architectural shading

4.5.1 TFB and temperature-dependent solar cell circuit

A 3-D FEM model of the a commercial solar panel was built and used to extract a TFB. The panel under analysis is the monocrystalline ET-M54050 50Wp manufactured by ET SOLAR – partitioned into two 20-cells subpanels equipped with bypass diodes [250] – mounted with tilt $\beta = 30°$, and oriented with azimuth $\gamma = -16°$ as in the available experimental setup.

Preliminary thermal-only analyses – considering as reference day June 15th, 2:00 PM, with a clear sky in Naples, Italy – were performed. The geometry and materials, built according to the datasheet data [250], are depicted in Fig. 4.38 and the parameter values are reported in Tab. 4.1 and Tab. 4.2. The external aluminum frame was neglected due to its small area of heat exchange. The mesh was generated with COMSOL [41], by exploiting selective meshing features since the horizontal dimensions are much larger than the thicknesses.

A significant issue is the choice of the correct BCs for the model. The

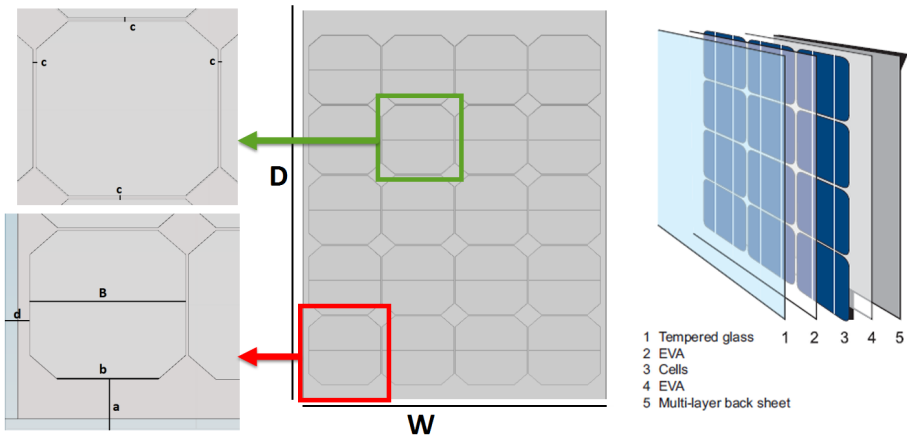


Fig. 4.38. Solar panel geometry data.

Table 4.1. Values of the geometry parameters depicted in Fig. 4.38.

Thicknesses [mm]	**Module** [mm]	**Cell** [mm]	**Spacings** [mm]
Glass = 3	D=719	B=127.25	a=32
EVA = 2.15	W=555	b=82	d=20
Si cells = 0.15			c=2
Back = 1			

Table 4.2. Values of the material parameters.

Material	ρ [kg/m^3]	**c** [J/kgK]	**k** [W/mK]
Glass	3000	500	1.8
EVA	960	2090	0.35
Si cells	2330	677	148
Tedlar	1200	1250	0.15

following BCs have been considered, as depicted in Fig. 4.39:

- The top surface of the panel is subject to the incident wind. Therefore both forced and free convection are considered. Moreover, radiant heat is emitted towards the sky from the top surface.
- The bottom surface is assumed to be shielded from the wind, i.e., only free convection and radiant heat towards the ground are considered.
- The side surfaces are assumed adiabatic: the thermal exchange through them is assumed negligible due to their small dimensions wrt the top and bottom surfaces.
- The solar panels composing the analyzed string are assumed to be thermally-decoupled, i.e. with independent thermal models.

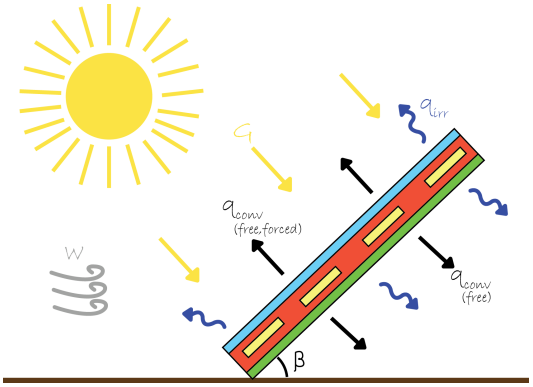


Fig. 4.39. Schematic representation of the BCs

Free convection is modeled according [251]: the average Nusselt number $\overline{Nu}$ is given by

$$\overline{Nu} = 0.68 + \frac{0.67 Ra^{\frac{1}{4}}}{\left[1 + \left(\frac{0.492}{\mathrm{Pr}}\right)^{\frac{9}{16}}\right]^{\frac{4}{9}}}, \; Ra \leqslant 10^9 \tag{4.18}$$

with the following adimensional parameters

$$\text{Prandtl's number } Pr = \frac{\nu}{\alpha} \tag{4.19}$$

being ν air kinematic viscosity, and α air's thermal diffusivity;

$$\text{Grashof's number } Gr = \frac{g \gamma_{IC} L^3 \cdot \cos(90^\circ - \beta)}{\nu^2} (T - T_{AMB}) \tag{4.20}$$

being $g = 9.8$ m/s^2 acceleration of gravity, γ_{IC} air isobaric compressibility,

and T local surface temperature;

$$\text{Rayleigh's number } Ra = Gr \cdot Pr \tag{4.21}$$

The average free heat transfer exchange coefficient $\overline{h}_{free}$ is evaluated from $\overline{Nu}$

$$\overline{h}_{free} = \frac{k_{air} \cdot \overline{Nu}}{L} \tag{4.22}$$

with air thermal conductivity $k_{air} = 2.614 \cdot 10^{-2}$ W/mK, L being the *characteristic length* given by the ratio between the surface and the perimeter of the area in which thermal exchange occurs $L = A/P$.

Forced convection is modeled with a slight modification of [252] considering the wind speed available from [253]. Defining θ_w as the angle between the wind direction and the normal vector to the panel, the equations at fixed angles are listed in Tab. 4.3.

Table 4.3. Forced heat transfer exchange $\overline{h}_{forced}$ as a function of wind speed w and incidence angle θ_w, after [252].

$\theta_{\mathbf{w}}$	**Equation**
$0°$	$\overline{h}_{forced} = 2.2w + 8.3$
$45°$	$\overline{h}_{forced} = 2.6w + 7.9$
$90°$	$\overline{h}_{forced} = 3.3w + 7.5$
$135°$	$\overline{h}_{forced} = 2.2w + 7.9$
$180°$	$\overline{h}_{forced} = 1.3w + 8.3$

Free and forced convection are composed according to [251]

$$\overline{h}_{tot} = \sqrt[3]{\left(\overline{h}_{free}\right)^3 + \left(\overline{h}_{forced}\right)^3} \tag{4.23}$$

Comparing h_{free} and h_{forced} and making use of (4.23) it can bee seen that even if a light wind is present, free convection can be neglected.

The power density q [W/m^2] exchanged between the panel surfaces and the ambient due to radiative contribution is given by [251]

$$q_{irr,front} = F_{front}\varepsilon_{front}\sigma\left(T_{front}^4 - T_{sky}^4\right) \tag{4.24}$$

$$q_{irr,back} = F_{back}\varepsilon_{back}\sigma\left(T_{back}^4 - T_{ground}^4\right) \tag{4.25}$$

for the front and the back, respectively, with *emissivity* $\epsilon_{front} = \epsilon_{glass} = 0.91$, $\epsilon_{back} = \epsilon_{tedlar} = 0.85$, $\sigma = 5.67 \cdot 10^{-8}$ Wm^{-2}K^{-4} being the Stephan-Boltzmann constant, assuming $T_{sky} = T_{ground} = T_{AMB}$ and with F *view*

factor given by

$$F_{front} = \frac{1 + \cos(\beta)}{2} \tag{4.26}$$

$$F_{back} = \frac{1 - \cos(180^\circ - \beta)}{2} \tag{4.27}$$

for the front toward the sky and for the back toward the ground, respectively.

In order to check the BCs, first simulations were run assuming uniform illumination with incidence irradiance on the plane of the panel $G = 931.34$ Wm^{-2} and comparing the cell temperatures with the commonly-adopted empirical equation in a wide range of operating condition

$$T_{cell} = T_{AMB} + \frac{G}{800}\left(T_{NOCT} - 20^\circ C\right) \tag{4.28}$$

where T_{NOCT} is the *nominal cell junction temperature*, being $T_{NOCT} = 44.5\,^\circ\mathrm{C}$. For the analyzed solar panel in the assumed operating condition, $T_{cell} = 54.9\,^\circ\mathrm{C}$ is obtained. This value has been compared to the one obtained from 3-D FEM simulations. Each cell is assumed to recieve the 95% of the incident power, i.e. $P_D = 0.95G \cdot A_{cell}$, and the *negative* converted power is determined by a purely-electrical simulation. Two cases have been considered:

1. Deactivating the radiative BCs, the average temperature of the cells is given by $\overline{T}_{cell,noqirr} = 69.15\,^\circ\mathrm{C}$
2. Including the radiative BCs, $\overline{T}_{cell,qirr} = 53.3\,^\circ\mathrm{C}$ is computed

From the aforementioned results is apparent that, while it is often found in the literature that is possible to neglect radiant BCs (e.g., [251]), this leads to a significant temperature overestimation.

A TFB to be used in a dynamic ET simulation is then built by exploiting FANTASTIC [154] (see Section 3.2) and is depicted in Fig. 4.40.

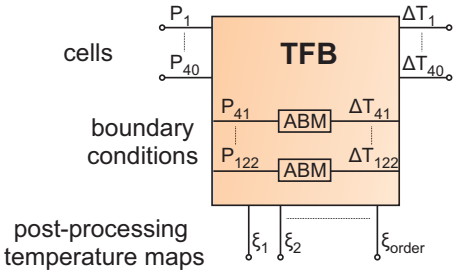


Fig. 4.40. TFB as obtained through FANTASTIC, suitably extended to take into account nonlinear radiative heat BCs.

Each solar cell is modeled with a HS; moreover, in order to model the nonlinear radiant heat BCs, additional HSs on the top and the back surface are considered by discretizing the surfaces with rectangles on top of the cells. The total number of heat sources is 122, with the one numbered for 1 to 40 for the solar cells. The dissipated power given as input to the cell is the sum of the incident power from the sun, diminished by the reflection and absorption of the layer on top of the cells, and the *negative* generated electrical power obtained from the circuit cell model described in the following subsection. The power and temperature corresponding to the surface discretization are closed in an internal feedback loop with a nonlinear ABM in order to model the radiant heat transfer and do not require user input. Besides the average temperature at the cells, which is used to perform the ET simulation, an additional set of nodes allows the user to evaluate the temperature field over the whole solar panel as in [154], unlike other compact thermal models.

The cells are described with the electrical subcircuit shown in Fig. 4.41 – improved variant of the classic one-diode model provided with two additional terminals compared to standard isothermal models, namely, a node carrying the dissipated power P_{cell} (defined as $-I_{cell} \cdot V_{cell}$) as an outcome, and another one providing as an input the temperature rise ΔT with respect to $T_{AMB}=T_0=27^{\circ}C$. The subcircuit accounts for [254]:

- the linear PTC κ [A/°C] of the PV current I_{ph} due to the bandgap shrinking and the resulting increase in the number of photons with enough energy to generate electron-hole pairs with the equation

$$I_{ph} = I_{scnom}\frac{G}{G_{nom}} + \kappa(\Delta T + 2) = I_{ph}(G, 25^{\circ}C) + \kappa(\Delta T + 2) \quad (4.29)$$

  where I_{scnom} is the short-circuit current under standard test conditions (STC), i.e., nominal irradiance $G_{nom} = 1000 W/m^2$ and cell temperature equal to 25°C, and G is the actual irradiance incident on the cell, obtained from *in-house* routines [255, 256].
- the temperature dependence of the I–V behavior of the intrinsic diode as in the equation

$$I_D = I_0 \exp\left[\frac{V_D + \phi_0 \Delta T}{n(V_{T0} + \frac{k}{q}\Delta T}\right] \quad (4.30)$$

  where I_0 is the reverse saturation current at T_0, n is the ideality factor, and ϕ_0 [V/K] is a coefficient dependent upon the physical features of the P-N junction, which was properly optimized to ensure a good description of the temperature dependence of the open-circuit voltage V_{oc}

reported in the datasheet.

- the PTC of the parasitic series resistance

$$R_S(T) = R_S(T_0) \cdot \left(\frac{T_0 + \Delta T}{T_0} \right)^{m_R} \tag{4.31}$$

where T_0 is expressed in Kelvin degrees (=300 K), and $m_R > 0$.

- avalanching effects according to the model proposed in [257]

$$I_{av} = -\frac{V_D}{R_{sh}} a_{II} \left[1 - \frac{V_D}{BV(T)} \right]^{-m_{II}} \tag{4.32}$$

where R_{sh} [Ω] is the shunt resistance, coefficient a_{II} and power factor m_{II} are dimensionless fitting parameters, and BV ($<$0 V) of the cell with temperature dependence given by

$$BV(T) = BV(T_0) \exp(b_{II} \Delta T) \tag{4.33}$$

b_{II} [K^{-1}] being another fitting parameter.

All the parameters of the cell subcircuits are reported in Tab. 4.4.

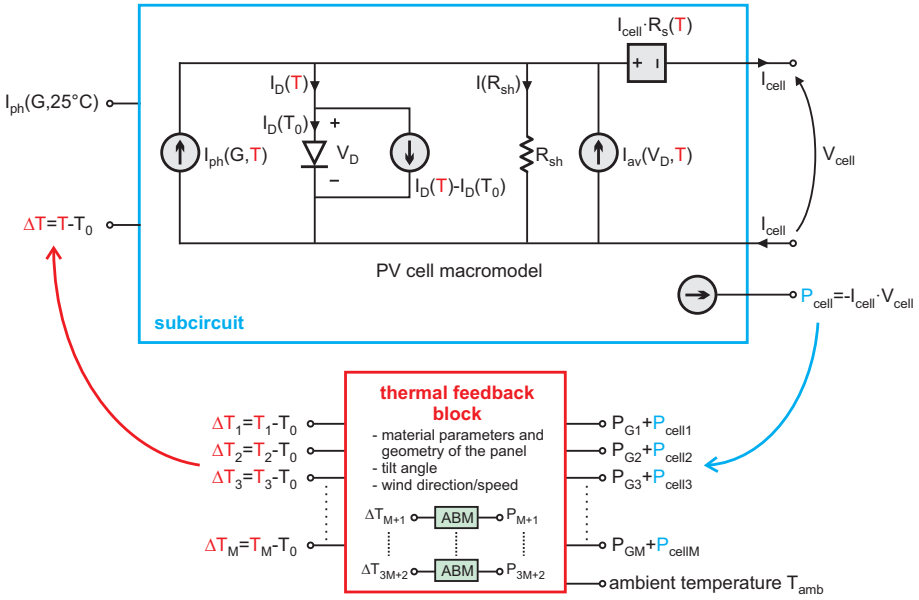


Fig. 4.41. Schematic of the cell subcircuit illustrating the connection with the TFB associated to the panel.

The subcircuits of the cells belonging to a panel are automatically linked

to the TFB, thereby leading to a purely electrical circuit suited to describe the dynamic ET behavior of the panel. Panel circuits can be in turn connected to give rise to a macrocircuit representing a PV plant, the solution of which is demanded to PSPICE [39].

Table 4.4. Values of the cell parameters.

Parameter	Value
I_{scnom}	2.8 A
κ	1.69 mV/°C
$I_0(T_0)$	8nA
n	1.2
ϕ_0	4.4 mV/°C
$BV(T_0)$	-10 V
a_{II}	0.1
m_{II}	1.1
R_{SH}	100 Ω
$R_S(T_0)$	12 mΩ
m_R	1.5

4.5.2 Simulation results

A dynamic ET analysis was conducted for a PV string composed by 5 series-connected ET-M54050 50Wp panels mounted on a rooftop in Naples, Italy, assuming the aforementioned reference day [258]. By employing the in-house routines presented in [256], it was determined that a quite low incidence angle θ of the Sun rays takes place (about $24°$), which represents a fairly favorable condition. By taking the values of the beam and diffuse irradiances on the plane of horizon (G_{bh}=725 W/m^2 and G_{dh}=230 W/m^2, respectively) from the PVGIS website [259], the whole irradiance incident on the panel G was evaluated to be 931 W/m^2, whence $I_{ph}(G, 25°C) \approx 2.6$ A.

Simulations were performed by emulating an architectural shadow falling on only one panel with the pattern evolution illustrated in Fig. 4.42 during an 1-hour-long time frame, in which a realistic MPPT action was accounted for by applying a time-dependent voltage V_{string}.

The CPU time amounted to about 1 hour on a normal PC in spite of the 5×10^5 PSPICE components. Results are reported in Fig. 4.43, which shows the key currents of the partially-shaded panel along with the string current I_{string}, and in Fig. 4.45, which depicts the temperatures and voltages of the cells highlighted in Fig. 4.44. All voltages and currents can be monitored in the entire string macrocircuit, thus offering an easy diagnosis of the shadow impact, which can be described as follows.

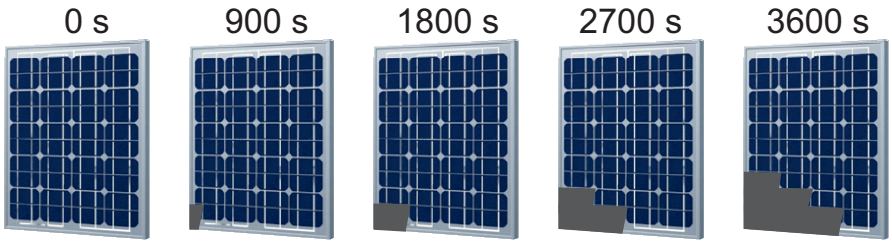


Fig. 4.42. Schematic representations of (a) the string under test and of (b) the shadow pattern vs. time on the shaded panel.

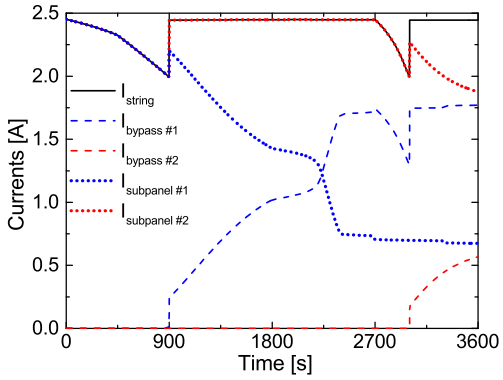


Fig. 4.43. Simulated evolution of the currents identified in Fig. 4.42.

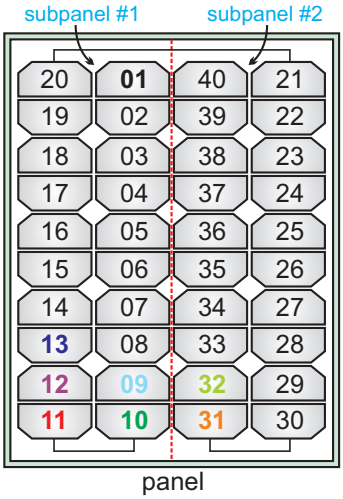


Fig. 4.44. Cell numbering of the shaded panel.

Between 0 and 900 s, only the corner cell 11 is obscured and enjoys a low temperature due to the irradiance decrease. I_{string} decreases since the inverter follows the MPP by increasing V_{string} and the bypass diode is not activated. At 900 s the MPP moves to a lower V_{string}, so that the bypass diode of subpanel #1 starts conducting, and I_{string} increases; in this scenario, cell 11 starts acting as a load ($V_{cell11} \approx$-9.5 V), thus *dissipating* power and heating up. As the shadow over cell 11 enlarges, $I_{subpanel1}$ reduces ($I_{bypass1}$ grows), the power dissipated by the cell decreases, and consequently the temperature, after reaching the maximum (about 90°C at 1400 s) starts reducing. It must be remarked that the temperature of cell 12 – which is still generating power – increases due to its close proximity to cell 11. After 1800 s, the shadow hits first cell 12 and then 10, the latter being marginally affected by the thermal coupling. At 2200 s, V_{cell12} reverses, thus favoring a V_{cell11} growth; at 2350 s, V_{cell11} exceeds V_{cell12} since $T_{cell11} > T_{cell12}$; as a result, $P_{cell12} > P_{cell11}$ and a brief T_{cell12} rise takes place. Eventually $V_{cell12}=V_{cell11}$ ($\approx$4.7 V) and $T_{cell12}=T_{cell11}$ at about 2700 s while both cells are cooling down. At 2650 s, cell 10 starts dissipating, and hence T_{cell10} exhibits a slight increase, which turns into a reduction at 3000 s since the whole reverse voltage in subpanel #1 is shared by three cells, namely, 10, 11, 12 (the common V_{cell} being equal to -3 V). At 2700 s, cells 9, 13, and 31 (the latter belonging to subpanel #2) are shaded, yet they are still generating power; from this time instant T_{cell9} and T_{cell13} reduce due to the concurrent effect of the steadily decreasing irradiance and of the lowering temperature of the neighboring cells 11, 12 (and also 10 after a while). At 3300 s, cells 9, 10, 11, 12, 13 of subpanel #1 are pushed into reverse mode. As subpanel #2 is shaded, a behavior resembling the one described for subpanel #1 is observed, with cells 31 and 32 playing the role of 11 and 12, respectively.

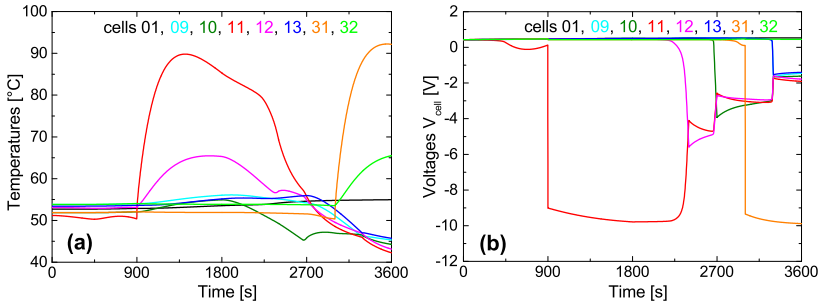


Fig. 4.45. (a) Temperatures and (b) voltages of the cells highlighted in Fig. 4.44.

Chapter 5

Conclusions

In this thesis it has been shown that TFB are a viable and easy to implement possibility for extremely efficient thermal and ET simulations, which are in high demand due to the ever increasing power and integration density in modern electronics. In particular:

- An *in-house* tool has been concieved, developed, and tested for the identification and synthesis of linear TFBs starting from simulation or measurement data either in time and frequency domain. The synthesis can be performed with three network topologies (with one being a novel extension), the performances of which have been compared.
- Parametric TFBs accounting for design parameters (e.g., layout dimensions) have been presented and exploited for thermal analysis of an 8-finger GaN HEMT.
- A tool denoted as FANTASTIC – based on the MPMM algorithm and featuring a novel linear TFB – has been presented, showing very high performance with respect to commercial solutions. FANTASTIC has been used to study the dynamic thermal behavior of a state-of-the-art GaAs HBT manufactured by RFMD.
- An automated synthesis routine for a TFB accounting for the temperature dependence of the thermal conductivity has been developed, and tested with a detailed thermal analysis of a highly-integrated UTCS structure.
- Improved Fourier & energy-balance heat propagation simulations have been performed for extremely detailed 3-D structures of SiGe HBTs manufactured by Infineon in the framework of European Project DOTSEVEN. The impact of the backend process over the thermal resistance

has been quantified.

- A node clustering strategy has been proposed for effective dynamic simulations of PDNs. Moreover, the behavior of carbon-based PDNs have been compared with standard copper, showing an interesting trade-off between electrical and thermal performances.
- Dynamic ET simulations relying on TFBs have been performed for a wide variety of applications at device-, circuit-, and system-level including: basic analog blocks in advanced technologies – bipolar differential pair, current mirror, CE amplifier; signal integrity analysis with the study of temperature-induced delay variations in a UTCS structure; reliability testing for power devices (UIS and SC); a string of 5 solar panels subject to architectural shading, presented for the first time in the literature.

Bibliography

[1] M. Pedram and S. Nazarian, "Thermal modeling, analysis, and management in VLSI circuits: Principles and methods," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1487–1501, Aug. 2006.

[2] Y. Zhan, S. Kumar, and S. Sapatnekar, "Thermally aware design," *Foundations and Trends in Electronic Design Automation*, vol. 2, no. 3, pp. 255–370, 2008.

[3] G. Breglio, A. Irace, E. Napoli, M. Riccio, and P. Spirito, "Experimental detection and numerical validation of different failure mechanisms in IGBTs during unclamped inductive switching," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 563–570, Feb. 2013.

[4] N. Rinaldi, "Small-signal operation of semiconductor devices including self-heating, with application to thermal characterization and instability analysis," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 323–331, Feb. 2001.

[5] L. Codecasa, D. D'Amore, and P. Maffezzoni, "Electro-thermal resonance in MOSFET devices," *Electronics Letters*, vol. 37, no. 1, pp. 57–58, 2001.

[6] L. Codecasa, "Electro-thermal chaotic oscillations of paralleled bipolar transistors," *Microelectronics journal*, vol. 35, no. 10, pp. 859–868, 2004.

[7] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part III - impact ionization," *IEEE Trans. Electron Devices*, vol. 53, no. 7, pp. 1683–1697, Jul. 2006.

[8] L. La Spina, V. d'Alessandro, S. Russo, N. Rinaldi, and L. K. Nanver, "Influence of concurrent electrothermal and avalanche effects on the safe operating area of multifinger bipolar transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 483–491, Mar. 2009.

[9] L. La Spina, V. d'Alessandro, S. Russo, and L. K. Nanver, "Thermal design of multifinger bipolar transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 8, pp. 1789–1800, Aug. 2010.

[10] V. d'Alessandro, N. Rinaldi, A. G. Metzger, and H. M. Banbrook, "On the safe operating area of bipolar cascode amplifiers," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2013, pp. 171–174.

[11] A. Metzger, V. d'Alessandro, N. Rinaldi, and P. J. Zampardi, "Evaluation of thermal balancing techniques in InGaP/GaAs HBT power arrays for wireless handset power amplifiers," *Microelectronics Reliability*, vol. 53, no. 9, pp. 1471–1475, 2013.

[12] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part II - two-finger devices," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2022–2033, Sept. 2005.

[13] N. Rinaldi, V. d'Alessandro, and L. K. Nanver, "Analysis of the bipolar current mirror including electrothermal and avalanche effects," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1309–1321, Jun. 2009.

[14] V. d'Alessandro, L. La Spina, L. K. Nanver, and N. Rinaldi, "Analysis of electrothermal effects in bipolar differential pairs," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 966–978, Apr. 2011.

[15] M. Rudolph, "Uniqueness problems in compact HBT models caused by thermal effects," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 5, pp. 1399–1403, May 2004.

[16] M. Rudolph, C. Fager, and D. E. Root, *Nonlinear transistor model parameter extraction techniques*. Cambridge University Press, 2011.

[17] A. H. Ajami, K. Banerjee, and M. Pedram, "Modeling and analysis of nonuniform substrate temperature effects on global ULSI interconnects," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 24, no. 6, pp. 849–860, Jun. 2005.

[18] H. Yu, J. Ho, and L. He, "Simultaneous power and thermal integrity driven via stapling in 3D ICs," in *Proc. IEEE/ACM International Conference on Computer-aided design (ICCAD)*, 2006, pp. 802–808.

[19] Y. Cheng, C. Tsai, C. Teng, and S. Kang, *Electrothermal Analysis of VLSI Systems*. Springer, 2000.

[20] M. Riccio, V. d'Alessandro, A. Irace, G. Rostaing, M. Berkani, S. Lefebvre, and P. Dupuy, "3-D electrothermal simulation of active cycling on smart power MOSFETs during short-circuit and UIS conditions," *Microelectronics Reliability*, vol. 54, no. 9, pp. 1845–1850, 2014.

[21] P. Mirone, L. Maresca, M. Riccio, G. De Falco, G. Romano, A. Irace, and G. Breglio, "An area-effective termination technique for PT-trench IGBTs," in *Proc. International Conference on Microelectronics (MIEL)*, 2014, pp. 273–276.

[22] M. Riccio, E. Napoli, A. Irace, G. Breglio, and P. Spirito, "Energy and current crowding limits in avalanche operation of IGBTs," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2013, pp. 273–276.

[23] K. Fischer and K. Shenai, "Dynamics of power MOSFET switching under undamped inductive loading conditions," *IEEE Trans. Electron Devices*, vol. 43, no. 6, pp. 1007–1015, 1996.

[24] S. Soneda, A. Narazaki, T. Takahashi, K. Takano, S. Kido, Y. Fukada, K. Taguchi, and T. Terashima, "Analysis of a drain-voltage oscillation of MOSFET under high dV/dt UIS condition," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2012, pp. 153–156.

[25] Y. Mizuno, R. Tagami, and K. Nishiwaki, "Investigations of inhomogeneous operation of IGBTs under unclamped inductive switching condition," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2010, pp. 137–140.

[26] M. Riccio, L. Rossi, A. Irace, E. Napoli, G. Breglio, P. Spirito, R. Tagami, and Y. Mizuno, "Analysis of large area trench-IGBT current distribution under UIS test with the aid of lock-in thermography," *Microelectronics Reliability*, vol. 50, no. 9–11, pp. 1725–1730, 2010.

[27] C.-C. Shen, A. R. Hefner, D. W. Berning, and J. B. Bernstein, "Failure dynamics of the IGBT during turn-off for unclamped inductive loading conditions," *IEEE Trans. Ind. Appl.*, vol. 36, no. 2, pp. 614–624, Mar.-Apr. 2000.

[28] G. Breglio, A. Irace, E. Napoli, M. Riccio, P. Spirito, K. Hamada, T. Nishijima, and T. Ueta, "Detection of localized UIS failure on IGBTs with the aid of lock-in thermography," *Microelectronics Reliability*, vol. 48, no. 8–9, pp. 1432–1434, 2008.

[29] T. Shoji, M. Ishiko, T. Fukami, T. Ueta, and K. Hamada, "Investigations on current filamentation of IGBTs under undamped inductive switching conditions," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2005, pp. 227–230.

[30] I. Pawel, R. Siemieniec, M. Rösch, F. Hirler, and R. Herzer, "Experimental study and simulations on two different avalanche modes in trench power MOSFETs," *IET Circuits, Devices and Systems*, vol. 1, no. 5, pp. 341–346, 2007.

[31] M. Riccio, A. Irace, G. Breglio, P. Spirito, E. Napoli, and Y. Mizuno, "Electro-thermal instability in multi-cellular trench-IGBTs in avalanche condition: Experiments and simulations," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2011, pp. 124–127.

[32] Y. Iwahashi, Y. Mizuno, M. Hara, R. Tagami, and M. Ishigaki, "Analysis of current distribution on IGBT under unclamped inductive switching conditions," *Microelectronics Reliability*, vol. 52, no. 9–10, pp. 2430–2434, 2012.

[33] A. Irace, P. Spirito, M. Riccio, and G. Breglio, "Voltage drops, sawtooth oscillations and HF bursts in breakdown current and voltage waveforms during UIS experiments," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2012, pp. 165–168.

[34] S.-W. Yoon, "Static and dynamic error vector magnitude behavior of 2.4-ghz power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 4, pp. 643–647, 2007.

[35] W. Wei, O. K. Jensen, and J. H. Mikkelsen, "Self-heating and memory effects in rf power amplifiers explained through electro-thermal," in *Proc. IEEE NORCHIP*. IEEE, 2013.

[36] D. Celo, X. Guo, P. Gunupudi, R. Khazaka, D. Walkey, T. Smy, and M. Nakhla, "The creation of compact thermal models of electronic components using model reduction," *IEEE Trans. Adv. Packag.*, vol. 28, no. 2, pp. 240–251, 2005.

[37] T. Bechtold, E. B. Rudnyi, and J. G. Korvink, "Dynamic electro-thermal simulation of microsystems - a review," *Journal of Micromechanics and Microengineering*, vol. 15, no. 11, pp. R17–R31, 2005.

[38] L. Codecasa, "Compact electro-thermal models of interconnects," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2013, pp. 309–314.

[39] PSPICE 16.6, *User's Manual*, Cadence OrCAD, 2012.

[40] D. Vasileska, S. M. Goodnick, and G. Klimeck, *Computational Electronics: Semiclassical and Quantum Device Modeling and Simulation*. CRC press, 2010.

[41] Comsol Multiphysics 3.5a, *User's Manual*, COMSOL AB, Stockholm, Sweden, 2008.

[42] S. Wünsche, C. Clauß, P. Schwarz, and F. Winkler, "Electro-thermal circuit simulation using simulator coupling," *IEEE Trans. VLSI Syst.*, vol. 5, no. 3, pp. 277–282, Sept. 1997.

[43] K. Fukahori and P. R. Gray, "Computer simulation of integrated circuits in the presence of electrothermal interaction," *IEEE J. Solid-State Circuits*, vol. SC-11, no. 6, pp. 834–846, Dec. 1976.

[44] A. R. Hefner and D. L. Blackburn, "Simulating the dynamic electrothermal behavior of power electronic circuits and systems," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 376–385, Oct. 1993.

[45] K. H. Kwok and V. d'Alessandro, "Fast analytical modeling of dynamic thermal behavior of semiconductor devices and circuits," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1031–1038, Apr. 2014.

[46] L. Codecasa, D. D'Amore, and P. Maffezzoni, "Thermal networks for heat wave equations," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2003, pp. 313–318.

[47] ——, "Thermal networks from phonon Boltzmann's transport equation part II - compact modeling," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2007.

[48] M.-N. Sabry, "Dynamic compact thermal models used for electronic design: a review of recent progress," in *Proc. International Electronic Packaging Technical Conference and Exhibition*, 2003, pp. 399–415.

[49] M.-N. Sabry and M. Dessouky, "A framework theory for dynamic compact thermal models," in *Proc. Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM)*, 2012, pp. 189–194.

[50] L. Codecasa, D. D'Amore, and P. Maffezzoni, "Compact modeling of electrical devices for electrothermal analysis," *IEEE Trans. Circuits Syst. I*, vol. 50, no. 4, pp. 465–476, Apr. 2003.

[51] L. Codecasa, "Compact models of dynamic thermal networks with many heat sources," *IEEE Trans. Compon. Packag. Technol.*, vol. 30, no. 4, pp. 653–659, Dec. 2007.

[52] E. Diebold and W. Luft, "Transient thermal impedance of semiconductor devices," *AIEE Transactions*, vol. 79, p. 719, 1961.

[53] L. Codecasa, "Canonical forms of one-port passive distributed thermal networks," *IEEE Trans. Compon. Packag. Technol.*, vol. 28, no. 1, pp. 5–13, Mar. 2005.

[54] P. Kawka, G. De Mey, and B. Vermeersch, "Thermal characterization of electronic packages using the Nyquist plot of the thermal impedance," *IEEE Trans. Compon. Packag. Technol.*, vol. 30, no. 4, pp. 660–665, 2007.

[55] G. De Mey, "Thermal conduction in phasor notation," *Proceedings of BETECH*, vol. 95, pp. 1–9, 1995.

[56] B. Vermeersch and G. Mey, "BEM calculation of the complex thermal impedance of microelectronic devices," *Engineering analysis with boundary elements*, vol. 31, no. 4, pp. 289–298, 2007.

[57] B. Vermeersch and G. De Mey, "Dynamic electrothermal simulation of integrated resistors at device level," *Microelectronics Journal*, vol. 40, no. 9, pp. 1411–1416, 2009.

[58] R. Sommet, A. Xiong, A. De Souza, and R. Quéré, "Dual approach for bipolar transistor thermal impedance determination," *Microelectronics Journal*, vol. 41, no. 9, pp. 554–559, 2010.

[59] B. Vermeersch and G. De Mey, "A shortcut to inverse Fourier transforms: Approximate reconstruction of transient heating curves from sparse frequency domain data," *International Journal of Thermal Sciences*, vol. 49, no. 8, pp. 1319–1332, 2010.

[60] T. Thein, C. Law, and K. Fu, "Frequency domain dynamic thermal analysis in GaAs HBT for power amplifier applications," *Progress In Electromagnetics Research*, vol. 118, pp. 71–87, 2011.

[61] I. Hasnaoui, A. Pottrain, D. Gloria, P. Chevalier, V. Avramovic, and C. Gaquiere, "Self-heating characterization of SiGe:C HBTs by extracting thermal impedances," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1762–1764, Dec. 2012.

[62] A. El Rafei, A. Saleh, R. Sommet, J. Nébus, and R. Quéré, "Experimental characterization and modeling of the thermal behavior of SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1921–1927, Jul. 2012.

[63] Y. Yang, R. Master, G. Refai-Ahmed, and M. Touzelbaev, "Transient frequency-domain thermal measurements with applications to electronic packaging," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 3, pp. 448–456, Mar. 2012.

[64] A. Sahoo, S. Fregonese, M. Weiß, B. Grandchamp, N. Malbert, and T. Zimmer, "Characterization of self-heating in Si–Ge HBTs with pulse, DC and AC measurements," *Solid-State Electronics*, vol. 76, pp. 13–18, 2012.

[65] L. Codecasa, D. D'Amore, and P. Maffezzoni, "Canonical forms of multi-port dynamic thermal networks," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2006, pp. 59–64.

[66] J. Brodsky, D. Zweidinger, and R. Fox, "Physics-based multiple-pole models for BJT self-heating," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 1993, pp. 249–252.

[67] D. Zweidinger, R. Fox, J. Brodsky, T. Jung, and S. Lee, "Thermal impedance extraction for bipolar transistors," *IEEE Trans. Electron Devices*, vol. 43, no. 2, pp. 342–346, Feb. 1996.

[68] U. Drofenik, D. Cottet, A. Musing, J.-M. Meyer, and J. W. Kolar, "Computationally efficient integration of complex thermal multi-chip power module models into circuit simulators," in *Proc. IEEE Power Conversion Conference (PCC)*, 2007, pp. 550–557.

[69] Z. Jakopović, Z. Benĉić, and R. Konćar, "Identification of thermal equivalent-circuit parameters for semiconductors," in *Proc. Workshop on Computers in Power Electronics*, 1990, pp. 251–260.

[70] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by Vector Fitting," *IEEE Transactions on Power Apparatus and Systems*, vol. 14, no. 3, pp. 1052–1061, Jul. 1999.

[71] R. Gao, Y. S. Mekonnen, W. T. Beyene, and J. E. Schutt-Ainé, "Black-box modeling of passive systems by rational function approximation," *IEEE Transactions on Advanced Packaging*, vol. 28, no. 2, pp. 209–215, May 2005.

[72] B. Gustavsen, "Improving the pole relocating properties of vector fitting," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1587–1592, Jul. 2006.

[73] D. Deschrijver, B. Gustavsen, and T. Dhaene, "Advancements in iterative methods for rational approximation in the frequency domain," *IEEE Trans. Power Del.*, vol. 22, no. 3, pp. 1633–1642, Jul. 2007.

[74] D. Deschrijver, "Broadband macromodeling of linear systems by vector fitting," 2007.

[75] D. Deschrijver, M. Mrozowski, T. Dhaene, and D. De Zutter, "Macromodeling of multiport systems using a fast implementation of the Vector Fitting method," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 6, pp. 383–385, Jun. 2008.

[76] [Online]. Available: http://www.energy.sintef.no/Produkt/VECTFIT/index.asp

[77] L. De Tommasi, D. Deschrijver, and T. Dhaene, "Single-input-single-output passive macromodeling via positive fractions vector fitting," in *Proc. IEEE Workshop on Signal Propagation on Interconnects (SPI)*, 2008.

[78] M. de Magistris and M. Nicolazzo, "On the concretely passive realization of reduced circuit models based on convex constrained positive real fractions identification," in *Proc. IEEE Workshop on Signal Propagation on Interconnects (SPI)*, 2011, pp. 29–32.

[79] S. Grivet-Talocia, "Package macromodeling via time-domain vector fitting," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 11, pp. 472–474, Nov. 2003.

[80] ——, "The time-domain Vector Fitting algorithm for linear macromodeling," *AEU-International Journal of Electronics and Communications*, vol. 58, no. 4, pp. 293–295, 2004.

[81] B. Gustavsen, "Computer code for passivity enforcement of rational macromodels by residue perturbation," *IEEE Trans. Adv. Packag.*, vol. 30, no. 2, pp. 209–215, May 2007.

[82] S. Grivet-Talocia and A. Ubolli, "Passivity enforcement with relative error control," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 11, pp. 2374–2383, Nov. 2007.

[83] ——, "A comparative study of passivity enforcement schemes for linear lumped macromodels," *IEEE Trans. Adv. Packag.*, vol. 31, no. 4, pp. 673–683, Nov. 2008.

[84] L. De Tommasi, A. Magnani, V. d'Alessandro, and M. de Magistris, "Time domain identification of passive multiport RC networks with convex optimization: An application to thermal impedance macromodeling," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2014.

[85] D. Walkey, T. Smy, R. Dickson, J. Brodsky, D. Zweidinger, and R. Fox, "Equivalent circuit modeling of static substrate thermal coupling using VCVS representation," *IEEE J. Solid-State Circuits*, vol. 37, no. 9, pp. 1198–1206, Sep. 2002.

[86] D. Walkey, T. Smy, D. Celo, T. MacElwee, and M. Maliepaard, "Compact, netlist-based representation of thermal transient coupling using controlled sources," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 23, no. 11, pp. 1593–1596, Nov. 2004.

[87] A. Magnani, V. d'Alessandro, M. de Magistris, and N. Rinaldi, "Thermal feedback networks for dynamic electrothermal simulations of devices and circuits: A critical perspective," in *45th GE conference*, 2013.

[88] J. Beck, K. Cole, A. Haji-Sheikh, and B. Litkouhi, *Heat conduction using Green's functions*. Hemisphere Publishing Corporation Washington DC, 1992.

[89] V. d'Alessandro and N. Rinaldi, "A critical review of thermal models for electro-thermal simulation," *Solid-State Electronics*, vol. 46, no. 4, pp. 487–496, 2002.

[90] S. Russo, "Measurement and simulation of electrothermal effects in solid-state devices for RF applications," 2010.

[91] J. D'Errico. (2005) fminsearchbnd, fminsearchcon. [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange/8277-fminsearchbnd

[92] M. de Magistris and L. De Tommasi, "An identification technique for macromodeling of long interconnects," in *Proc. IEEE Workshop on Signal Propagation on Interconnects (SPI)*, vol. 2005, 2005, pp. 185–188.

[93] V. Belevitch, *Classical network theory*. Holden-Day San Francisco, 1968, vol. 36.

[94] C. P. Coelho, J. Phillips, and L. M. Silveira, "A convex programming approach for generating guaranteed passive approximations to tabulated frequency-data," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 23, no. 2, pp. 293–301, Feb. 2004.

[95] M. Grant, S. Boyd, and Y. Ye, "Disciplined convex programming," *Global Optimization: From Theory to Implementation*, pp. 155–210, 2006.

[96] M. de Magistris and L. De Tommasi, "Identification of broadband passive macromodels for electromagnetic structures," *COMPEL - The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, vol. 26, no. 2, pp. 247–258, 2007.

[97] L. De Tommasi, M. de Magistris, D. Deschrijver, and T. Dhaene, "An algorithm for direct identification of passive transfer matrices with positive real fractions via convex programming," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 24, no. 4, pp. 375–386, 2011.

[98] V. Székely, "On the representation of infinite-length distributed RC one-ports," *IEEE Trans. Circuits Syst.*, vol. 38, no. 7, pp. 711–719, Jul. 1991.

[99] ——, "Identification of RC networks by deconvolution: chances and limits," *IEEE Trans. Circuits Syst. I*, vol. 45, no. 3, pp. 244–258, Mar. 1998.

[100] Y. Gerstenmaier, W. Kiffe, and G. Wachutka, "Combination of thermal subsystems by use of rapid circuit transformation and extended two-port theory," *Microelectronics Journal*, vol. 40, no. 1, pp. 26–34, 2009.

[101] V. d'Alessandro, M. de Magistris, A. Magnani, N. Rinaldi, S. Grivet-Talocia, and S. Russo, "Time domain dynamic electrothermal macromodeling for thermally aware integrated system design," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2013.

[102] P. Triverio, M. Nakhla, and S. Grivet-Talocia, "Passive parametric macromodeling from sampled frequency data," in *Proc. IEEE Workshop on Signal Propagation on Interconnects (SPI)*, 2010, pp. 117–120.

[103] ——, "Passive parametric modeling of interconnects and packaging components from sampled impedance, admittance or scattering data," in *Proc. Electronic System-Integration Technology Conference (ESTC)*, 2010.

[104] A. Ubolli, S. Grivet-Talocia, M. Bandinu, and A. Chinea, "Sensitivity-based weighting for passivity enforcement of linear macromodels in power integrity applications," in *Proc. Design, Automation and Test in Europe Conference and Exhibition (DATE)*, 2014.

[105] T. Kennett, W. Prestwich, and A. Robertson, "Bayesian deconvolution i: convergent properties," *Nuclear Instruments and Methods*, vol. 151, no. 1, pp. 285–292, 1978.

[106] ——, "Bayesian deconvolution ii: Noise properties," *Nuclear Instruments and Methods*, vol. 151, no. 1, pp. 293–301, 1978.

[107] T. Mangold and P. Russer, "Full-wave modeling and automatic equivalent-circuit generation of millimeter-wave planar and multilayer structures," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 6, pp. 851–858, Jun. 1999.

[108] V. d'Alessandro, M. de Magistris, A. Magnani, N. Rinaldi, and S. Russo, "Electrothermal reduced equivalents of highly integrated electronic systems with multi-port positive fraction Foster expansion," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2012, pp. 25–28.

[109] N. Rinaldi, S. Russo, and V. d'Alessandro, "Thermal effects in thin silicon dies: Simulation and modelling," pp. 287–308, 2011.

[110] S. Pinel, A. Marty, J. Tasselli, J.-P. Bailbe, E. Beyne, R. Van Hoof, S. Marco, J. R. Morante, O. Vendier, and M. Huan, "Thermal modeling and management in ultrathin chip stack technology," *IEEE Trans. Compon. Packag. Technol.*, vol. 25, no. 2, pp. 244–253, Jun. 2002.

[111] J. Palacín, M. Salleras, J. Samitier, and S. Marco, "Dynamic compact thermal models with multiple power sources: Application to an ultrathin chip stacking technology," *IEEE Trans. Adv. Packag.*, vol. 28, no. 4, pp. 694–703, 2005.

[112] F. Iker, D. S. Tezcan, R. C. Teixeira, P. Soussan, P. De Moor, E. Beyne, and K. Baert, "3D embedding and interconnection of ultra thin ($\ll$ 20 μm) silicon dies," in *Proc. of the Electronic Packaging Technology Conference (EPTC)*, 2007, pp. 222–226.

[113] A. Ziabari and A. Shakouri, "Fast thermal simulations of vertically integrated circuits (3D ICs) including thermal vias," in *IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM)*, 2012, pp. 588–596.

[114] V. d'Alessandro, M. de Magistris, A. Magnani, N. Rinaldi, and S. Russo, "Dynamic electrothermal macromodeling: An application to signal integrity analysis in highly integrated electronic systems," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 7, pp. 1237–1243, Jul. 2013.

[115] F. Bonani and G. Ghione, "On the application of the Kirchhoff transformation to the steady-state thermal analysis of semiconductor devices with temperature-dependent and piecewise inhomogeneous thermal conductivity," *Solid-State Electronics*, vol. 38, no. 7, pp. 1409–1412, 1995.

[116] J. Paasschens, S. Harmsma, and R. van der Toorn, "Dependence of thermal resistance on ambient and actual temperature," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2004, pp. 96–99.

[117] X. Xu and Z. Wang, "Thermal conductivity enhancement of benzocyclobutene with carbon nanotubes for adhesive bonding in 3-D integration," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 2, pp. 286–293, Feb. 2012.

[118] Y.-F. Chiu, Y.-L. Tsai, and W.-S. Hwang, "Mathematical modeling for the solidification heat-transfer phenomena during the reflow process of lead–tin alloy solder joint in electronics packaging," *Applied Mathematical Modelling*, vol. 27, no. 7, pp. 565–579, 2003.

[119] V. Palankovski and R. Quay, *Analysis and Simulation of Heterostructure Devices*. Springer, 2004.

[120] L. Codecasa, V. d'Alessandro, A. Magnani, and N. Rinaldi, "Parametric compact thermal models by moment matching for variable geometry," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2014.

[121] F. Ferranti, L. Knockaert, and T. Dhaene, "Guaranteed passive parameterized admittance-based macromodeling," *IEEE Trans. Adv. Packag.*, vol. 33, no. 3, pp. 623–629, Aug. 2010.

[122] ——, "Parameterized S-parameter based macromodeling with guaranteed passivity," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 10, pp. 608–610, Oct. 2009.

[123] ——, "Passivity-preserving parametric macromodeling by means of scaled and shifted state-space systems," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pp. 2394–2403, Oct. 2011.

[124] F. Ferranti, T. Dhaene, and L. Knockaert, "Compact and passive parametric macromodeling using reference macromodels and positive interpolation operators," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 2, no. 12, pp. 2080 –2088, Dec. 2012.

[125] F. Ferranti, T. Dhaene, S. Russo, A. Magnani, M. de Magistris, V. d'Alessandro, and N. Rinaldi, "Parameterized thermal macromodeling for fast and effective design of electronic components and systems," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2014.

[126] L. F. Eastman and U. K. Mishra, "The toughest transistor yet," *IEEE Spectrum*, vol. 39, no. 5, pp. 28–33, May 2002.

[127] R. Schwindt, V. Kumar, O. Aktas, J.-W. Lee, and I. Adesida, "AlGaN/GaN HEMT-based fully monolithic X-band low noise amplifier," *Physica Status Solidi*, vol. 2, no. 7, pp. 2631–2634, 2005.

[128] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.

[129] K. W. Kobayashi, Y. Chen, I. Smorchkova, B. Heying, W.-B. Luo, W. Sutton, M. Wojtowicz, and A. Oki, "Multi-decade GaN HEMT cascode-distributed power amplifier with baseband performance," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium (RFICS)*, 2009, pp. 369–372.

[130] K. Krishnamurthy, J. Martin, D. Aichele, and D. Runton, "A decade bandwidth 90 W GaN HEMT push-pull power amplifier for VHF/UHF applications," in *Proc. Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2011.

[131] F. Yamaki, K. Inoue, N. Ui, A. Kawano, and S. Sano, "A 65% drain efficiency GaN HEMT with 200 W peak power for 20 V to 65 V envelope tracking base station amplifier," in *Proc. IEEE International Microwave Symposium Digest*, 2011.

[132] R. Gaska, A. Osinsky, J. Yang, and M. S. Shur, "Self-heating in high-power AlGaN-GaN HFETs," *IEEE Electron Device Lett.*, vol. 19, no. 3, pp. 89–91, Mar. 1998.

[133] J. Albrecht, R. Wang, P. Ruden, M. Farahmand, and K. Brennan, "Electron transport characteristics of GaN for high temperature device modeling," *J. Appl. Phys*, vol. 83, no. 9, pp. 4777–4781, May 1998.

[134] W.-C. Liu, K.-H. Yu, R.-C. Liu, K.-W. Lin, K.-P. Lin, C.-H. Yen, C.-C. Cheng, and K.-B. Thei, "Investigation of temperature-dependent characteristics of an n^+/-InGaAs/n-GaAs composite doped channel HFET," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2677–2683, Dec. 2001.

[135] J. Kuzmík, P. Javorka, A. Alam, M. Marso, M. Heuken, and P. Kordoš, "Determination of channel temperature in AlGaN/GaN HEMTs grown on sapphire and silicon substrates using DC characterization method," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1496–1498, Aug. 2002.

[136] S. Russo, V. d'Alessandro, M. Costagliola, G. Sasso, and N. Rinaldi, "Analysis of the thermal behavior of AlGaN/GaN HEMTs," *Materials Science and Engineering: B – Advanced Functional Solid-State Materials*, vol. 177, no. 15, pp. 1343–1351, 2012.

[137] M. Peroni, P. Romanini, A. Pantellini, L. Mariucci, A. Minotti, G. Ghione, V. Camarchia, E. Limiti, A. Serino, and A. Chini, "Design, fabrication, and characterization of Γ-gate GaN HEMT for high-frequency/wide-band applications," in *Proc. Workshop On Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE)*, 2007, pp. 371–378.

[138] F. Ferranti, A. Magnani, V. d'Alessandro, S. Russo, N. Rinaldi, T. Dhaene, and M. de Magistris, "Effective electrothermal analysis of electronic devices and systems with parameterized macromodeling," *IEEE Trans. Compon., Packag., Manuf. Technol., accepted pending first review*.

[139] R. A. Horn and C. R. Johnson, *Topics in Matrix Analysis*. Cambridge University Press, 1994.

[140] F. Bertoluzza, G. Sozzi, N. Delmonte, and R. Menozzi, "Hybrid large-signal/lumped-element electro-thermal modeling of GaN-HEMTs," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3163–3170, Dec. 2009.

[141] L. Codecasa, D. D'Amore, and P. Maffezzoni, "Thermal networks for electro-thermal analysis of power devices," *Microelectronics Journal*, vol. 32, no. 10–11, pp. 817–822, 2001.

[142] ——, "Parameters for multi-point moment matching reduction of discretized thermal networks," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2002, pp. 151–154.

[143] ——, "Modeling the thermal response of semiconductor devices through equivalent electrical networks," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 8, pp. 1187–1197, 2002.

[144] ——, "An Arnoldi based thermal network reduction method for electro-thermal analysis," *IEEE Trans. Compon. Packag. Technol.*, vol. 26, no. 1, pp. 186–192, Mar. 2003.

[145] L. Codecasa, D. D'Amore, P. Maffezzoni, and W. Batty, "Analytical multipoint moment matching reduction of distributed thermal networks," *IEEE Trans. Compon. Packag. Technol.*, vol. 27, no. 1, pp. 87–95, Mar. 2004.

[146] L. Codecasa, D. D'Amore, and P. Maffezzoni, "Compact thermal networks for modeling packages," *IEEE Trans. Compon. Packag. Technol.*, vol. 27, no. 1, pp. 96–103, Mar. 2004.

[147] ——, "Multipoint moment matching reduction from port responses of dynamic thermal networks," *IEEE Trans. Compon. Packag. Technol.*, vol. 28, no. 4, pp. 605–614, 2005.

[148] ——, "A novel approach for generating boundary condition independent compact dynamic thermal networks of packages," *IEEE Trans. Compon. Packag. Technol.*, vol. 28, no. 4, pp. 593–604, 2005.

[149] ——, "Compact thermal networks for conjugate heat transfer by moment matching," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*. IEEE, 2008, pp. 52–57.

[150] L. Codecasa and L. Di Rienzo, "Stochastic thermal modeling by polynomial chaos expansion," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2013, pp. 33–38.

[151] ——, "Compact thermal models for stochastic thermal analysis," *Microelectronics Journal*, vol. 45, no. 12, pp. 1770–1776, 2015.

[152] U. Griesmann. [Online]. Available: https://sites.google.com/site/ulfgri/numerical/gdsii-toolbox

[153] [Online]. Available: http://salome-platform.org/

[154] L. Codecasa, V. d'Alessandro, A. Magnani, N. Rinaldi, and P. J. Zampardi, "Fast novel thermal analysis simulation tool for integrated circuits (FANTASTIC)," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2014.

[155] A. H. Squillacote and J. Ahrens, *The paraview guide*. Kitware, 2007.

[156] A. Magnani, V. d'Alessandro, L. Codecasa, P. Zampardi, B. Moser, and N. Rinaldi, "Analysis of the influence of layout and technology parameters on the thermal impedance of GaAs HBT/BiFET using a highly-efficient tool," in *Proc. Compound Semiconductor Integrated Circuit Symposium (CSICS)*. IEEE, 2014.

[157] M. Fresina, "Trends in GaAs HBTs for wireless and RF," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*. IEEE, 2011, pp. 150–153.

[158] R. Anholt, "Hbt thermal element design using an electro/thermal simulator," *Solid-State Electronics*, vol. 42, no. 5, pp. 857–864, 1998.

[159] D. E. Dawson, A. K. Gupta, and M. L. Salib, "CW measurement of HBT thermal resistance," *IEEE Trans. Electron Devices*, vol. 39, no. 10, pp. 2235–2239, Oct. 1992.

[160] W. Liu, D. Hill, H.-F. Chau, J. Sweder, T. Nagle, and J. Delaney, "Laterally etched undercut (leu) technique to reduce base-collector capacitances in heterojunction bipolar transistors," in *Proc. IEEE GaAs IC Symposium*, 1995, pp. 167–170.

[161] M. Rencz and V. Székely, "Studies on the nonlinearity effects in dynamic compact model generation of packages," *IEEE Trans. Compon. Packag. Technol.*, vol. 27, no. 1, pp. 124–130, Mar. 2004.

[162] L. Codecasa, V. d'Alessandro, A. Magnani, and N. Rinaldi, "Compact dynamic modeling for fast simulation of nonlinear heat conduction in ultra-thin chip stacking technology," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 11, pp. 1785–1795, Nov. 2014.

[163] K. Górecki and J. Zarebski, "Nonlinear compact thermal model of power semiconductor devices," *IEEE Trans. Compon. Packag. Technol.*, vol. 33, no. 3, pp. 643–647, 2010.

[164] C. Gu, "QLMOR: A projection-based nonlinear model order reduction approach using quadratic-linear representation of nonlinear systems," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 9, pp. 1307–1320, Sept. 2011.

[165] J. Marek, A. Chvála, D. Donoval, P. Pribytny, M. Molnar, and M. Mikolasek, "Compact model of power MOSFET with temperature dependent Cauer RC network for more accurate thermal simulations," *Solid-State Electronics*, vol. 94, pp. 44–50, 2014.

[166] K. Górecki and J. Zarebski, "A semiconductor device thermal model taking into account nonlinearity and multipathing of the cooling system," in *Journal of Physics: Conference Series*, vol. 494, no. 1, 2014, p. 012008.

[167] A. K. Sahoo, S. Fregonese, R. Desposito, K. Aufinger, C. Maneux, and T. Zimmer, "A geometry scalable model for non-linear thermal impedance of trench isolated hbts," 2014.

[168] A. Sahoo, S. Fregonese, P. Scheer, D. Celi, A. Juge, and T. Zimmer, "Nonlinear modelling of dynamic self-heating in 28 nm bulk complementary metal–oxide semiconductor technology," *Electronics Letters*, vol. 51, no. 7, pp. 581–583, 2015.

[169] W. B. Joyce, "Thermal resistance of heat sinks with temperature-dependent conductivity," *Solid-State Electronics*, vol. 18, no. 4, pp. 321–322, 1975.

[170] H. S. Carslaw, J. C. Jaeger *et al.*, *Conduction of heat in solids*. Clarendon Press Oxford, 1959, vol. 2.

[171] M. N. Özışık, *Boundary value problems of heat conduction*. Courier Corporation, 1989.

[172] W. Batty and C. Snowden, "Electro-thermal device and circuit simulation with thermal nonlinearity due to temperature dependent diffusivity," *Electronics Letters*, vol. 36, no. 23, pp. 1966–1968, Nov. 2000.

[173] K. Krabbenhoft and L. Damkilde, "Comments on 'Electro-thermal device and circuit simulation with thermal nonlinearity due to temperature dependent diffusivity'," *Electronics Letters*, vol. 37, no. 24, pp. 1481–1482, Nov. 2001.

[174] W. Batty, S. David, and C. Snowden, "Reply to Comment on 'Electro-thermal device and circuit simulation with thermal nonlinearity due to temperature dependent diffusivity'," *Electronics Letters*, vol. 37, no. 24, pp. 1482–1483, Nov. 2001.

[175] L. Codecasa, "Novel approach to compact modeling for nonlinear thermal conduction problems," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2013, pp. 164–169.

[176] ——, "Nonlinear dynamic compact thermal models by structure-preserving projection," *Microelectronics Journal*, vol. 45, no. 12, pp. 1764–1769, 2014.

[177] J. R. Phillips, "Projection-based approaches for model reduction of weakly nonlinear, time-varying systems," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 22, no. 2, pp. 171–187, Feb. 2003.

[178] M. Rewienski and J. White, "A trajectory piecewise-linear approach to model order reduction and fast simulation of nonlinear circuits and micromachined devices," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 22, no. 2, pp. 155–170, Feb. 2003.

[179] P. Li and L. T. Pileggi, "Compact reduced-order modeling of weakly nonlinear analog and RF circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 24, no. 2, pp. 184–203, Feb. 2005.

[180] T. Hélie and B. Laroche, "On the convergence of Volterra series of finite dimensional quadratic MIMO systems," *International Journal of Control*, vol. 81, no. 3, pp. 358–370, 2008.

[181] W. J. Rugh, *Nonlinear System Theory: The Volterra/Wiener Approach*. Johns Hopkins University Press Baltimore, 1981.

[182] L. Codecasa, V. d'Alessandro, A. Magnani, and N. Rinaldi, "Multi-port dynamic compact thermal models of nonlinear heat conduction," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2014.

[183] K. J. Negus, R. W. Franklin, and M. M. Yovanovich, "Thermal modeling and experimental techniques for microwave bipolar devices," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 12, no. 4, pp. 680–689, Dec. 1989.

[184] [Online]. Available: www.dotfive.eu/

[185] V. d'Alessandro, I. Marano, S. Russo, D. Céli, A. Chantre, P. Chevalier, F. Pourchon, and N. Rinaldi, "Impact of layout and technology parameters on the thermal resistance of SiGe:C HBTs," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2010, pp. 137–140.

[186] G. Chen, *Nanoscale energy transport and conversion: a parallel treatment of electrons, molecules, phonons, and photons*. Oxford University Press, USA, 2005.

[187] Z. M. Zhang, *Nano/microscale heat transfer*. McGraw-Hill New York, 2007.

[188] X. Wang, *Experimental Micro/nanoscale Thermal Transport*. John Wiley & Sons, 2012.

[189] T. S. Fisher, *Thermal energy at the nanoscale*. World Scientific, 2014.

[190] J. Lai and A. Majumdar, "Concurrent thermal and electrical modeling of sub-micrometer silicon devices," *Journal of Applied Physics*, vol. 79, no. 9, pp. 7353–7361, 1996.

[191] O. Muscato and V. Di Stefano, "Electro-thermal behaviour of a sub-micron silicon diode," *Semiconductor Science and Technology*, vol. 28, no. 2, p. 025021, 2013.

[192] T. Hori, T. Shiga, and J. Shiomi, "Phonon transport analysis of silicon germanium alloys using molecular dynamics simulations," *Journal of Applied Physics*, vol. 113, no. 20, p. 203514, 2013.

[193] E. Pop, S. Sinha, and K. E. Goodson, "Heat generation and transport in nanometer-scale transistors," *Proceedings of the IEEE*, vol. 94, no. 8, pp. 1587–1601, Aug. 2006.

[194] D. Vasileska, S. Goodnick, and K. Raleva, "Self-consistent simulation of heating effects in nanoscale devices," in *Proc. International Workshop on Computational Electronics (IWCE)*, 2009.

[195] O. Tornblad, P. Sverdrup, D. Yergeau, Z. Yu, K. Goodson, and R. Dutton, "Modeling and simulation of phonon boundary scattering in PDE-based device simulators," in *Simulation of Semiconductor Processes and Devices, 2000. SISPAD 2000. 2000 International Conference on*. IEEE, 2000, pp. 58–61.

[196] S.-M. Hong, A.-T. Pham, and C. Jungemann, *Deterministic solvers for the Boltzmann transport equation*. Springer Science & Business Media, 2011.

[197] [Online]. Available: www.dotseven.eu/

[198] E. Pop, "Energy dissipation and transport in nanoscale devices," *Nano Research*, vol. 3, no. 3, pp. 147–169, 2010.

[199] A. McConnell and K. E. Goodson, "Thermal conduction in silicon micro-and nanostructures," *Annual review of heat transfer*, vol. 14, no. 14, 2005.

[200] Y. Lee and G. S. Hwang, "Mechanism of thermal conductivity suppression in doped silicon studied with nonequilibrium molecular dynamics," *Physical Review B*, vol. 86, no. 7, p. 075202, 2012.

[201] Y. Zhong and M. D. Wong, "Fast algorithms for ir drop analysis in large power grid," in *Proc. IEEE/ACM International conference on Computer-aided design*. IEEE Computer Society, 2005, pp. 351–357.

[202] A. Todri-Sanial, "Electro-thermal characterization of through-silicon vias," in *Proc. IEEE EuroSimE*. IEEE, 2014.

[203] C. Knoth, H. Jedda, and U. Schlichtmann, "Current source modeling for power and timing analysis at different supply voltages," in *Proceedings of the Conference on Design, Automation and Test in Europe*. EDA Consortium, 2012, pp. 923–928.

[204] A. G. Chiariello, A. Maffucci, and G. Miano, "Circuit models of carbon-based interconnects for nanopackaging," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 11, pp. 1926–1937, 2013.

[205] A. Magnani, M. de Magistris, A. Maffucci, and A. Todri-Sanial, "A node clustering reduction scheme for power grid electrothermal analysis," in *Proc. IEEE Workshop on Signal Propagation on Interconnects (SPI), accepted for presentation*, 2015.

[206] A. Naeemi and J. D. Meindl, "Performance modeling for single-and multiwall carbon nanotubes as signal and power interconnects in gigascale systems," *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2574–2582, 2008.

[207] H. Li, C. Xu, N. Srivastava, and K. Banerjee, "Carbon nanomaterials for next-generation interconnects and passives: Physics, status, and prospects," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1799–1821, 2009.

[208] N. H. Khan and S. Hassoun, "The feasibility of carbon nanotubes for power delivery in 3-d integrated circuits," in *Design Automation Conference (ASP-DAC), 2012 17th Asia and South Pacific*. IEEE, 2012, pp. 53–58.

[209] A. Todri-Sanial, "Investigation of horizontally aligned carbon nanotubes for efficient power delivery in 3D ICs," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*. IEEE, 2014.

[210] Q. Zhang, G. Chen, S. Yoon, J. Ahn, S. Wang, Q. Zhou, Q. Wang, J. Li *et al.*, "Thermal conductivity of multiwalled carbon nanotubes," *Physical Review B*, vol. 66, no. 16, p. 165440, 2002.

[211] H.-Y. Cao, Z.-X. Guo, H. Xiang, and X.-G. Gong, "Layer and size dependence of thermal conductivity in multilayer graphene nanoribbons," *Physics Letters A*, vol. 376, no. 4, pp. 525–528, 2012.

[212] Q. Shao, G. Liu, D. Teweldebrhan, and A. Balandin, "High-temperature quenching of electrical resistance in graphene interconnects," *Applied Physics Letters*, vol. 92, no. 20, p. 202108, 2008.

[213] S. Vollebregt, S. Banerjee, K. Beenakker, and R. Ishihara, "Size-dependent effects on the temperature coefficient of resistance of carbon nanotube vias," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4085–4089, 2013.

[214] A. Magnani, M. de Magistris, A. Maffucci, and A. Todri-Sanial, "Carbon-based power delivery networks for nanoscale ICs: Electrothermal performance analysis," in *Proc. IEEE NANO, submitted*, 2015.

[215] A. G. Chiariello, A. Maffucci, and G. Miano, "Temperature effects on electrical performance of carbon-based nano-interconnects at chip and package level," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 26, no. 6, pp. 560–572, 2013.

[216] L. K. Nanver, N. Nenadovic, V. d'Alessandro, H. Schellevis, H. W. Van Zeijl, R. Dekker, D. B. De Mooij, V. Zieren, and J. W. Slotboom, "A back-wafer contacted silicon-on-glass integrated bipolar process - part I: The conflict electrical versus thermal isolation," *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 42–50, Jan. 2004.

[217] N. Nenadovic, V. d'Alessandro, L. K. Nanver, F. Tamigi, N. Rinaldi, and J. W. Slotboom, "A back-wafer contacted silicon-on-glass integrated bipolar process - part II: A novel analysis of thermal breakdown," *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 51–62, Jan. 2004.

[218] S. Russo, L. La Spina, V. d'Alessandro, N. Rinaldi, M. de Magistris, and L. Nanver, "Thermal transient behavior of silicon-on-glass BJTs," in *Proc. International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2009.

[219] N. Nenadovic, V. d'Alessandro, L. La Spina, N. Rinaldi, and L. K. Nanver, "Restabilizing mechanisms after the onset of thermal instability in bipolar transistors," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 643–653, Apr. 2006.

[220] V. d'Alessandro, M. de Magistris, A. Magnani, N. Rinaldi, and S. Russo, "Dynamic electrothermal analysis of bipolar devices and circuits relying on multi-port positive fraction Foster representation," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2012, pp. 29–32.

[221] D. Nairn, "Analytic step response of MOS current mirrors," *IEEE Trans. Circuits Syst. I*, vol. 40, no. 2, pp. 133–135, Feb. 1993.

[222] A. Magnani, V. d'Alessandro, N. Rinaldi, M. de Magistris, and K. Aufinger, "Dynamic electrothermal macromodeling techniques for thermal-aware design of circuits and systems," in *Proc. IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 2013, pp. 227–230.

[223] P. Chevalier, T. Meister, B. Heinemann, S. Van Huylenbroeck, W. Liebl, A. Fox, A. Sibaja-Hernandez, and A. Chantre, "Towards THz SiGe HBTs," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2011, pp. 57–65.

[224] I. Marano, "Analytical modeling and numerical simulations of the thermal behavior of bipolar transistors," 2008.

[225] V. d'Alessandro, G. Sasso, N. Rinaldi, and K. Aufinger, "Scaling influence on the thermal behavior of toward-THz SiGe:C HBTs," in *Journal of Physics: Conference Series*, vol. 494, no. 1. IOP Publishing, 2014, p. 012002.

[226] R. Joy and E. Schlig, "Thermal properties of very fast transistors," *IEEE Trans. Electron Devices*, vol. 17, no. 8, pp. 586–594, Aug. 1970.

[227] N. Spennagallo, L. Codecasa, D. D'Amore, and P. Maffezzoni, "Evaluating the effects of temperature gradients and currents nonuniformity in on-chip interconnects," *Microelectronics Journal*, vol. 40, no. 7, pp. 1154–1159, 2009.

[228] A. Hastings, *The Art of Analog Layout*. Prentice Hall, 2001.

[229] W. H. Chang, "Analytical IC metal-line capacitance formulas," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-24, no. 9, pp. 608–611, Sept. 1976.

[230] Y. Shao, X. Li, and J. Mao, "Electrothermal coupling analysis of CMOS gates driving interconnects," *Proc.IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, pp. 1–4, 2012.

[231] V. d'Alessandro, A. Magnani, M. Riccio, Y. Iwahashi, G. Breglio, N. Rinaldi, and A. Irace, "Analysis of the UIS behavior of power devices by means of SPICE-based electrothermal simulations," *Microelectronics Reliability*, vol. 53, no. 9–11, pp. 1713–1718, 2013.

[232] R. Kraus, P. Tuerkes, and J. Sigg, "Physics-based models of power semiconductor devices for the circuit simulator SPICE," in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, vol. 2, 1998, pp. 1726–1730.

[233] M. Riccio, G. De Falco, L. Maresca, G. Breglio, E. Napoli, A. Irace, Y. Iwahashi, and P. Spirito, "3D electro-thermal simulations of wide area power devices operating in avalanche condition," *Microelectronics Reliability*, vol. 52, no. 9–10, pp. 2385–2390, 2012.

[234] P. Hower, "Avalanche injection and second breakdown in transistors," *IEEE Trans. Electron Devices*, vol. ED–17, no. 4, pp. 320–335, Apr. 1970.

[235] G. K. Wachutka, "Analytical model for the destruction mechanism of GTO-like devices by avalanche injection," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1516–1523, Jun. 1991.

[236] M. Riccio, G. Breglio, A. Irace, and P. Spirito, "An equivalent time temperature mapping system with a 320× 256 pixels full-frame 100 kHz sampling rate," *Review of Scientific Instruments*, vol. 78, no. 10, pp. 1 061 061–1 061 063, 2007.

[237] M. Ostling, R. Ghandi, and C.-M. Zetterling, "SiC power devices–present status, applications and future perspective," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. IEEE, 2011, pp. 10–15.

[238] [Online]. Available: http://www.cree.com/Power/Products/MOSFETs/Bare-die/CPMF-1200-S080B

[239] V. d'Alessandro, A. Magnani, M. Riccio, G. Breglio, A. Irace, N. Rinaldi, and A. Castellazzi, "SPICE modeling and dynamic electrothermal simulation of SiC power MOSFETs," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2014, pp. 285–288.

[240] B. J. Baliga, *Modern Power Devices*. Wiley, 1987.

[241] J. Wang, T. Zhao, J. Li, A. Q. Huang, R. Callanan, F. Husna, and A. Agarwal, "Characterization, modeling, and application of 10-kV SiC MOSFET," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1798–1806, Aug. 2008.

[242] S. Chen, C. Cai, T. Wang, Q. Guo, and K. Sheng, "Cryogenic and high temperature performance of 4H-SiC power MOSFETs," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2013, pp. 207–210.

[243] P. Spirito, G. Breglio, V. d'Alessandro, and N. Rinaldi, "Thermal instabilities in high current power MOS devices: Experimental evidence, electro-thermal simulations and analytical modeling," in *Proc. International Conference on Microelectronics (MIEL)*, vol. 1, 2002, pp. 23–30.

[244] A. Pérez-Tomás, P. Brosselard, P. Godignon, J. Millán, N. Mestres, M. Jennings, J. A. Covington, and P. A. Mawby, "Field-effect mobility temperature modeling of 4H-SiC metal-oxide-semiconductor transistors," *Journal of applied physics*, vol. 100, no. 11, p. 114508, 2006.

[245] L. Cheng, A. K. Agarwal, S. Dhar, S.-H. Ryu, and J. W. Palmour, "Static performance of 20 A, 1200 V 4H-SiC power MOSFETs at temperatures of -187 C to 300 C," *Journal of electronic materials*, vol. 41, no. 5, pp. 910–914, 2012.

[246] X. Huang, G. Wang, Y. Li, A. Q. Huang, and B. Baliga, "Short-circuit capability of 1200V SiC MOSFET and JFET for fault protection," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2013, pp. 197–200.

[247] V. d'Alessandro and P. Spirito, "Achieving accuracy in modeling the temperature coefficient of threshold voltage in MOS transistors with uniform and horizontally nonuniform channel doping," *Solid-State Electronics*, vol. 49, no. 7, pp. 1098–1106, 2005.

[248] L. Maresca, M. Cardonia, G. Avallone, M. Riccio, G. Romano, G. De Falco, A. Irace, and G. Breglio, "Development of a new short-circuit tester for 1.7 kv high current power devices," in *Proc. IEEE MIEL*. IEEE, 2014, pp. 85–88.

[249] A. Castellazzi, T. Funaki, T. Kimoto, and T. Hikihara, "Thermal instability effects in SiC power MOSFETs," *Microelectronics Reliability*, vol. 52, no. 9–10, pp. 2414–2419, 2012.

[250] [Online]. Available: http://www.etsolar.com.ar/folletos/ET-M54050(50w).pdf

[251] S. Armstrong and W. Hurley, "A thermal model for photovoltaic panels under varying atmospheric conditions," *Applied Thermal Engineering*, vol. 30, no. 11, pp. 1488–1495, 2010.

[252] S. Sharples and P. Charlesworth, "Full-scale measurements of wind-induced convective heat transfer from a roof-mounted flat plate solar collector," *Solar Energy*, vol. 62, no. 2, pp. 69–77, 1998.

[253] [Online]. Available: http://it.windfinder.com/

[254] V. d'Alessandro, F. Di Napoli, P. Guerriero, and S. Daliento, "A novel circuit model of PV cell for electrothermal simulations," 2014.

[255] P. Guerriero, F. Di Napoli, F. Cominale, V. d'Alessandro, and S. Daliento, "Accurate analysis of small shadows effects on photovoltaic systems yield," in *Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2014 International Symposium on*. IEEE, 2014, pp. 987–992.

[256] V. d'Alessandro, F. Di Napoli, P. Guerriero, and S. Daliento, "An automated high-granularity tool for a fast evaluation of the yield of PV plants accounting for shading effects," 2014.

[257] J. Bishop, "Computer simulation of the effects of electrical mismatches in photovoltaic cell interconnection circuits," *Solar cells*, vol. 25, no. 1, pp. 73–89, 1988.

[258] V. d'Alessandro, A. Magnani, L. Codecasa, F. Di Napoli, P. Guerriero, and S. Daliento, "Dynamic electrothermal simulation of photovoltaic plants," in *Proc. IEEE ICCEP*, 2015.

[259] [Online]. Available: http://re.jrc.ec.europa.eu/pvgis/

List of publications

[C01] V. d'Alessandro, M. de Magistris, A. Magnani, N. Rinaldi, and S. Russo, "Electrothermal reduced equivalents of highly integrated electronic systems with multi-port positive fraction foster expansion," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2012, pp. 25–28.

[C02] V. d'Alessandro, M. de Magistris, A. Magnani, N. Rinaldi, and S. Russo, "Dynamic electrothermal analysis of bipolar devices and circuits relying on multi-port positive fraction foster representation," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2012, pp. 29–32.

[C03] V. d'Alessandro, M. De Magistris, A. Magnani, N. Rinaldi, S. Grivet-Talocia, and S. Russo, "Time domain dynamic electrothermal macromodeling for thermally aware integrated system design," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2013.

[C04] A. Magnani, V. d'Alessandro, M. de Magistris, and N. Rinaldi, "Thermal feedback networks for dynamic electrothermal simulations of devices and circuits: A critical perspective," in *45th GE conference*, 2013.

[C05] A. Magnani, V. d'Alessandro, N. Rinaldi, M. De Magistris, and K. Aufinger, "Dynamic electrothermal macromodeling techniques for thermal-aware design of circuits and systems," in *Proc. IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 2013, pp. 227–230.

[C06] L. De Tommasi, A. Magnani, V. d'Alessandro, and M. De Magistris, "Time domain identification of passive multiport RC networks with convex optimization: An application to thermal impedance macromodeling," in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2014.

[C07] F. Ferranti, T. Dhaene, S. Russo, A. Magnani, M. De Magistris, V. d'Alessandro, and N. Rinaldi, "Parameterized thermal macromodeling for fast and effective design of electronic components and systems,"

in *Proc. IEEE Workshop on Signal and Power Integrity (SPI)*, 2014.

[C08] V. d'Alessandro, A. Magnani, M. Riccio, G. Breglio, A. Irace, N. Rinaldi, and A. Castellazzi, "SPICE modeling and dynamic electrothermal simulation of SiC power MOSFETs," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2014, pp. 285–288.

[C09] L. Codecasa, V. d'Alessandro, A. Magnani, and N. Rinaldi, "Parametric compact thermal models by moment matching for variable geometry," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2014.

[C10] L. Codecasa, V. d'Alessandro, A. Magnani, and N. Rinaldi, "Multiport dynamic compact thermal models of nonlinear heat conduction," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2014.

[C11] L. Codecasa, V. d'Alessandro, A. Magnani, N. Rinaldi, and P. J. Zampardi, "Fast novel thermal analysis simulation tool for integrated circuits (FANTASTIC)," in *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2014. *Best poster award in Tools Development*.

[C12] A. Magnani, V. d'Alessandro, L. Codecasa, P. J. Zampardi, B. Moser, and N. Rinaldi, "Analysis of the influence of layout and technology parameters on the thermal impedance of GaAs HBT/BiFET using a highly-efficient tool," in *Proc. Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2014.

[J1] V. d'Alessandro, M. De Magistris, A. Magnani, N. Rinaldi, and S. Russo, "Dynamic electrothermal macromodeling: An application to signal integrity analysis in highly integrated electronic systems," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 3, no. 7, pp. 1237–1243, Jul. 2013.

[J2] V. d'Alessandro, A. Magnani, M. Riccio, Y. Iwahashi, G. Breglio, N. Rinaldi, and A. Irace, "Analysis of the UIS behavior of power devices by means of SPICE-based electrothermal simulations," *Microelectronics Reliability*, vol. 53, no. 9–11, pp. 1713–1718, 2013.

[J3] L. Codecasa, V. d'Alessandro, A. Magnani, and N. Rinaldi, "Compact dynamic modeling for fast simulation of nonlinear heat conduction in ultra-thin chip stacking technology," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 11, pp. 1785–1795, 2014.

Under review and submitted

[J4r] F. Ferranti, A. Magnani, V. d'Alessandro, S. Russo, N. Rinaldi, T. Dhaene, and M. De Magistris, "Effective electrothermal analysis of electronic devices and systems with parameterized macromodeling," accepted in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, pending first review.

[C13r] V. d'Alessandro, A. Magnani, L. Codecasa, F. Di Napoli, P. Guerriero, and S. Daliento, "Dynamic electrothermal simulation of photovoltaic plants," accepted for presentation at *ICCEP* 2015.

[C14r] A. Magnani, M. de Magistris, A. Maffucci, and A. Todri-Sanial, "A node clustering reduction scheme for power grid electrothermal analysis," accepted for presentation at *IEEE SPI* 2015.

[C15s] A. Magnani, M. de Magistris, A. Maffucci, and A. Todri-Sanial, "Carbon-Based Power Delivery Networks for Nanoscale ICs: Electrothermal Performance Analysis," submitted to *IEEE NANO* 2015.

The PhD activities have benefited from numerous collaborations with other universities and industries, as graphically reported below.

[C3] [C5] [J2] [C6] [C7] [C8], [J4r]

[J3] [C9] [C10] [C11] [C12] [C13r]

[C12]

[C14r], [C15s]

List of acronyms

ABM – Analog Behavioral Modeling
ADS – Advanced Design System
BC – Boundary condition
BCB – Benzocyclobutene
BJT – Bipolar Junction Transistor
BTE – Boltzmann Transport Equation
BV – Breakdown Voltage
CCCS – Current Controlled Current Source
CE – Common Emitter
CNT – Carbon NanoTube
CS – Controlled Source
DCTM – Dynamic Compact Thermal Model
DoF – Degree of Freedom
DUT – Device Under Test
ET – ElectroThermal
EVM – Error Vector Magnitude
FANTASTIC – FAst Novel Thermal Analysis Simulation Tool for ICs
FDM – Finite Difference Method
FEM – Finite Elements Method
GNR – Graphene NanoRibbon
HBT – Heterojunction Bipolar Transistor
HEMT – High Electron Mobility Transistor
IC – Integrated Circuits
IGBT – Integrated Circuits
II – Impact Ionization
IR – Infrared
LIT – Lock-In Thermography
LS – Least Squares
MEMS – Micro Electro-Mechanical Systems
MNA – Modified Nodal Analysis
MOR – Model Order Reduction
MOSFET – Metal Oxide Semiconductor Field Effect Transistor
MPMM – Multi-Point Moment Matching
MWCNT – Multi-Walled Carbon NanoTube
NDR – Negative Differential Resistance

NID – Network Identification by Deconvolution
NLLS – Non Linear Least Squares
NTC – Negative Temperature Coefficient
ODE – Ordinary Differential Equation
PA – Power Amplifier
PDE – Partial Differential Equation
PDN – Power Delivery Network
PDR – Positive Differential Resistance
PFVF – Positive Fraction Vector fitting
PR – Positive Real
PSPICE – SPICE simulator by Cadence
PTC – Positive Temperature Coefficient
RF – Radio Frequency
RMS – Root Mean Square
SC – Short Circuit
SOA – Safe Operating Area
SOG – Silicon On Glass
SPICE – Simulation Program with Integrated Circuit Emphasis
STC – Standard Test Condition
SWCNT – Single-Walled Carbon NanoTube
TC – Temperature Coefficient
TDPFVF – Time Domain Positive Fraction Vector Fitting
TDVF – Time Domain Vector Fitting
TFB – Thermal Feedback Block
THS – Thin Heat Source
TM – Top Metal
UIS – Unclamped Inductive Switching test
UTCS – Ultra-Thin Chip-Stacking technology
VCCS – Voltage Controlled Current Source
VCVS – Voltage Controlled Voltage Source
VF – Vector Fitting
VHS – Volumetric Heat Source
VTC – Voltage-Transfer Characteristic

Ringraziamenti

Dopo aver descritto in inglese i risultati del mio lavoro, sento ora il bisogno della mia lingua per cercare di esprimere al meglio ciò che provo e ringraziare di cuore tutti coloro che mi hanno accompagnato in questo percorso di vita e di studi.

Inannzitutto, sono enormemente grato al prof. Enzo d'Alessandro per la condivisione della sua esperienza, per tutti i suoi preziosi insegnamenti, e per la costante vicinanza con la quale ha sempre smorzato le mie insicurezze – non dimenticherò di certo tutte le volte in cui, nonostante i numerosissimi impegni di lavoro, ha ascoltato le mie presentazioni, persino dalla Germania!

Un sentito grazie, poi, al prof. Lorenzo Codecasa per avermi aperto gli occhi (e la mente) su molti aspetti delle simulazioni FEM e della programmazione efficientissima, e per la fraterna ospitalità che mi ha offerto a Milano. Soprattutto, un FANTASTICo grazie per il lavoro al quale mi ha dato l'onore di partecipare!

Un grazie speciale a Salvatore Russo, che, oltre ad avermi magistralmente guidato nell'uso del COMSOL, mi ha consentito un po' di relax in questo periodo di stress con i videogiochi che mi ha regalato. Voglio ringraziare Grazia Sasso per l'indispensabile supporto che mi ha sempre offerto (specie in occasione delle scadenze del DOTSEVEN) e per avermi fatto da preziosa guida in California. E, parlando di California, non posso certo dimenticare Andrè Metzger, che mi ha ospitato nella sua splendida villa con vista su Mission Bay e con il quale ho vissuto momenti di puro divertimento: spero davvero, un giorno, di poter anche *lavorare* con lui ;) – me lo riprometto fortemente!

Sono molto contento di avere avuto l'occasione di imparare da tante persone con diverse specializzazioni con le quali ho avuto l'onore di collaborare. Il mio ringraziamento va agli "optoelettronici" – prof. Giovanni Breglio, prof. Andrea Irace e Michele Riccio – per lo stimolante lavoro fatto insieme e per i dati sperimentali forniti, senza i quali alcune simulazioni non avebbero mai acquistato la giusta concretezza. Sono grato a Francesco Ferranti e Luciano De Tommasi, grazie ai quali ho potuto comprendere meglio aspetti delle tecniche di identificazione e di macromodeling. E non posso certo non ringraziare il gruppo del fotovoltaico – prof. Santolo Daliento, Pierluigi Guerriero e Fabio di Napoli – per gli interessantissimi lavori e discussioni, e per avermi fatto sentire parte integrante del loro affiatatissimo team!

La vita non è solo lavoro – tranne che quando manca poco ad una scadenza[1] –

[1] Ovvero, sempre.

e vorrei ringraziare tutti coloro che mi sono stati vicini nella vita quotidiana. Grazie, quindi, a Darjin e (di nuovo) a Fabio per la vivace e piacevolissima compagnia di questi anni e, in particolare, per la bellissima serata di cinema e biliardo trascorsa insieme (che spero di replicare quanto prima). Un pensiero grato a Luca, Peppe, Giorgio, Michele, Gianpaolo e Gianlorenzo, compagni di avventura in questo dottorato, ed a Fabio "il dottore", mio vicino di scrivania che ha sopportato stoicamente il suono della mia tastiera meccanica.

Un grazie lieve e dolce a Janaina per la sua incontenibile allegria e per la forte motivazione che ha saputo infondermi. Il giusto ringraziamento, poi, al mio gruppo di amici storico: Fabrizio, Vincenzo "Piccettino", Alessandro "il Nitti", Attilio, Luca "Giorg", Rudy ed, in particolare, a Paco "Hombre", che non mi ha mai fatto mancare la sua voce, nemmeno mentre nasceva e cresceva la sua splendida famiglia.

Ed ora i ringraziamenti conclusivi.

Dovrei ringraziare la mia famiglia per il sostegno continuo, la tenera pazienza e l'immenso affetto in ogni piccola cosa, ma non lo farò in questa sede. A loro dico grazie ogni giorno.

La mia profonda gratitudine va al prof. Massimiliano de Magistris, oltre che per motivi di lavoro, per aver saputo comprendere le mie difficoltà ed incoraggiarmi affettuosamente al raggiungimento della laurea ad un punto estremamente delicato della mia vita: gli dedico tutta la gioia di questo momento.

Infine, il mio ringraziamento, forse il più grande, va al prof. Niccolò Rinaldi, che, dedicando l'attenzione e la cura di uno straordinario docente alla mia formazione, mi ha regalato la meravigliosa opportunità di approfondire una splendida materia.
E di farmela amare.

L'anima mia gustava di quel cibo
che, saziando di sé, di sé asseta