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Reliability Analysis of Power Electronic Devices

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Introduction

Technology of power semiconductor devices has been experimented a constant improvement, in some aspect even faster than the counterpart of the signal devices. That is because the necessity of converting energy with loosing the less amount of power has been more and more important during the years. Nowadays it is not unusual to find energy conversion systems which present efficiency near and over to 95%, that is only a small amount of the input energy is lost by dissipation in the system itself. In order to achieve these figures, the most of the attention has been paid in enhancing the characteristics of the power electronic devices that represent the core of a conversion system, and are often responsible for the most amount of power dissipation. The issue related to power dissipation not only belongs to the energy lost in the conversion process, but also to the fact that the dissipation of energy always produces heat which must correctly dissipated in order to avoid the temperature to rise over dangerous values. In particular applications, the latter is even more important than the energy loss. This is particularly true in automotive applications where the working environment imposes very harsh operative conditions. What is more, the trend has been and still is to reduce the size of the electronic system as well as to increase the power capacity and this leads to even higher power densities.

From what said one of the most important aims of power devices manufacturer is to improve the ruggedness and the reliability of the components. This is generally guaranteed by considerations related to the specific application the devices must operate into. This is relatively simple to achieve for devices which are dedicated to single applications, where all the constraints and the power absorption profile is well known from the beginning. On the other hand, there are components which are not designed for functioning in a particular application and, as a conse-

quence, must be usually over designed so that they can safely withstand various operative conditions, often beyond the nominal conditions, even if for a small time.
Recent technologies like the usage of trench gates are nowadays dominant in applications where a high attention is placed in DC or high current pulsed applications, whilst planar technologies are still diffused in utilizations where low thermal resistance and maximum forward bias safe operating area (FBSOA) is a dominating constraint. To accomplish the desirable ruggedness in power switch applications, designers should understand trade-off of each power device type as they apply to the target application. In this scenario, the reliability analysis of power electronic devices, either conducted in the design phase, by means of simulation, or as experimental validation, by means of proper tests, are of paramount importance. These analyses require a very thorough evaluation of the device, and the acquisition of a statistically large sample of failure currents and energies. The population should be free as much as possible from defected devices that fail at lower energies, and those which are malfunctioning must be removed in order to ensure, hopefully, a full imperfection-free selection of devices.
In the field of reliability analysis, this thesis mainly deals with investigation of electrothermal interactions inside a power devices and its effect on the reliability of the device itself and the system either.

Thesis content

The thesis is divided in three section and one appendix.

First section introduces two power devices which are analysed in the rest of this work, namely the Power MOSFET and the IGBT. These devices shares same features, mainly related to the voltage-driven nature, but also significant difference hold due to the unipolar nature of the Power MOSFET against the bipolar one of the IGBT.
In the section, a brief description of the working principle as well as the physical mechanisms taking place inside the devices are provided. The whole operative conditions are singularly addressed and particular attention is posed in describing the static and dynamic performances. What is more, a brief overview of the common failure mechanisms is also presented.

Finally, in the last part, two common test for evaluating the ruggedness of the devices are illustrated.

Second section is about the simulation analysis of reliability. The section starts with an enumeration of the most used methods to perform electrothermal simulation of the power devices. For each method, a brief historical digression is provided, in order to show the improvements during the years.
The section continues with the description of a novel electrothermal simulation environment dedicated to simulation of avalanche operations. Reliability analysis of avalanche conditions are performed on IGBT for dedicated to AC/AC conversion.
Then, a second simulation approach is presented, for simulations of short circuit conditions. The short circuit effects are analysed by means of testing the behaviour of a low voltage Power MOSFET dedicated to automotive application in order to study the effect of thermal instabilities produced by the high temperatures.
For both the simulation analyses, conclusion are drawn at the end of each subsection.

Third section In this section, an experimental set up, base of a diffused topology, is presented for the evaluation of I-V blocking characteristic of power devices.
The importance of the knowledge of this characteristic is firstly pointed out. Then, the circuit is described and the solutions designed for improving the basic topology are addressed. These solutions are validated by means of SPICE simulations as well as experimental measurements. utilized for measuring the characteristics of a Power MOSFET first, and secondly of an IGBT, to the purpose of validate the theoretical achievements shown in scientific literature. Finally, a last experiment is presented, which is conducted on two devices with different geometries in order to point out the effect of the geometry on the avalanche ruggedness.

Appendix A An appendix is provided which show the analysis, by means of TCAD simulations, of the dynamic avalanche phenomenon occurring in high voltage IGBTs turn off transients. In particular, a

high voltage Trench IGBT is considered and its behaviour is analysed when it switches off, starting from high current densities.
Unstable distribution of the current and formation of filaments are reported and the effect on the reliability are hence provided.

Chapter 1: Physics of Semiconductor Devices

Power MOSFET and IGBT are the preferred power devices in power application because the ease of control logic and circuitry, being them voltage controlled devices. In addition, they normally do not absorb power from the input terminal unless during switching phases, so they required driving circuit with low power rates. Since they share the same control criteria, the physic of the two devices has a lot of common points. Nevertheless, both has some significant differences which make them suitable for very different applications. In the following, the basic theory of the two devices is analysed, with particular attention on the mechanisms which can lead to the failure of the device.

1.1 The Power MOSFET

The vertical power metal-oxide-field effect transistor (Power MOSFET) was introduced for the first time in the 1970s as an alternative to power BJTs, largely diffused in that period. The noticeable features of having a very high input impedance makes it immediately preferable with respect to the BJT because of its ease of control. In addition, for the very high switching speed and low output impedance it was considered the perfect device for high power, high frequency applications. Nevertheless, the use Power MOSFET is nowadays confined in low voltage application. The reason lays on the increasing trend of the on state resistance with the maximum sustainable voltage. In fact, this resistance produces a relevant potential drop when a high current flows along the device, and therefore the resulting power dissipation of the device is considerably high. Being the resistance strongly depend on the maximum voltage capability of the device, for values higher than 600 V, the on state losses

would be unacceptably high.
In the first versions of the Power MOSFET, the source diffusion were used to define the length of the electron channel under the gate terminal. With this approach, without expensive techniques, it was possible to reduce the channel resistance and also to increase the current capability [1]. In addition, by applying appropriate design methodologies, the internal resistance was more and more reduced down to a minimum values limited by additional parasitics resistances basically present in the structure. A further improvement was done in the 1990s, when the gate terminal was designed in trenches so to create a vertical channel which nearly removes the parasitic resistance produced by the JFET region between the source diffusions. The resulting device was called UMOSFET or Trench MOSFET and it is the technology which is nowadays designed with.
Improvements in the modern technologies have made possible to manufacturer more complicated Power MOSFET structure which sensibly reduce the on state drop, and therefore it is quite usual to find devices with breakdown voltage of 800-900 V [2, 3].

1.1.1 Basic structure

The basic structure of a Power MOSFET recalls the signal version of the devices and also its working principle: the application of a sufficient high positive voltage between the gate and source terminal creates a channel of electrons which move from the source to the drain, higher potential, diffusion. The movement of these charges produces a current flowing from the drain terminal to the source terminal, according to the usual convention that the direction of the current is opposite to the electron flow. The main difference between a signal MOSFET and a Power MOSFET is that the drain region is diffused vertically in order to sustain the high electric field that develops in the structure when the device is in off state and must withstand high voltages. With this design, the electron flow is vertical from the source to the drain and the device is therefore called *Vertical Drain MOS* (VDMOS). The presence of the epitaxial region introduces also an intrinsic PiN diode structure formed by the $P^+ - N^- - N^+$ regions. By having a diode intrinsically fabricated in the structure, the Power MOSFET is suitable for application where the flow of current can be reverted.
In figure 1.1 is depicted the basic cross section of a VDMOS structure.

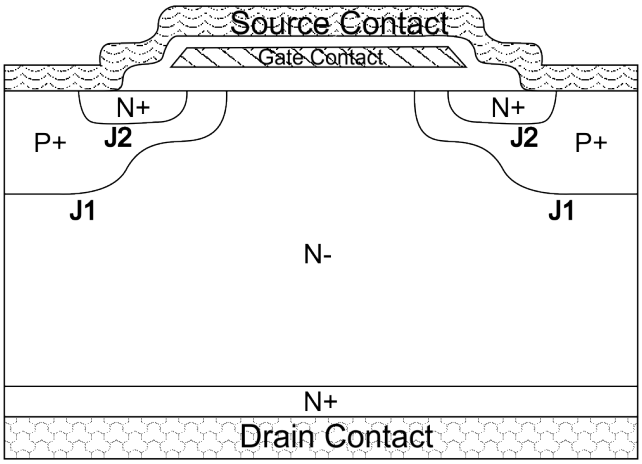


Figure 1.1: VDMOS cross section.

This device structure is fabricated by starting with an Ntype epitaxial layer grown on a heavily doped N^+ substrate. The channel is formed by the difference in lateral extension of the P-base and N^+ source regions produced by their diffusion cycles. Both regions are self-aligned to the left-hand side and right-hand side of the gate region during ion implantation to introduce the respective dopants. A refractory gate electrode, such as polysilicon, is required to allow diffusion of the dopants under the gate electrode at elevated temperatures. In the blocking state, that is when the gate-source voltage is zero, the junction J1 sustains the whole voltage and the electric field develops in the low doped region. When a positive voltage is applied between gate and source terminal, the channel created under the gate let the electron to flow from the source to the drain. Along this path, the charges cross the channel, accumulates under the gates and subsequently crosses the JFET region, formed by two consecutive P-body diffusions. Finally they move across the low doped drain region towards the substrate where the are collected by the drain terminal. Each region introduces a resistive effect which contributes to the overall internal resistance of the Power MOSFET and which is responsible of the high voltage drop into the device. An optimal design is required to minimize each of the components of the internal resistance, considering that the component introduced by the low-doped region cannot be reduced because this region is responsible for the maximum voltage capability. In order to overtake the effect of

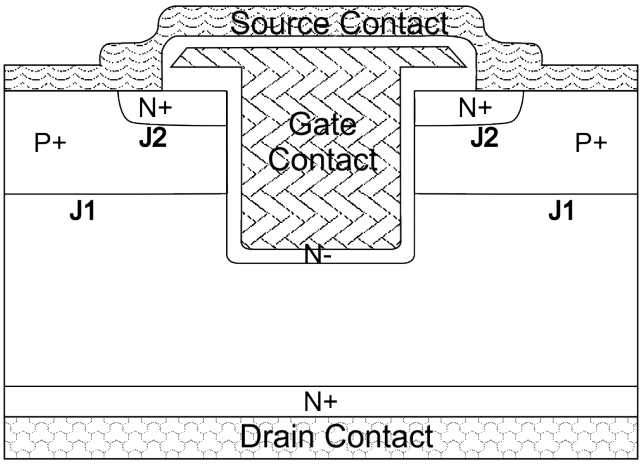


Figure 1.2: Cross section of a Trench Power MOSFET.

resistance of JFET region, it has been developed the trench gate power MOSFET, whose structure is depicted in the Figure 1.2. This structure essentially eliminates the JFET region under the gate terminal, by providing a vertical flow of the electron in the channel formed along the trench sides.

1.1.2 Static characteristics

The static behaviour of a Power MOSFET can be described in the same way as the correspondent signal device[1]. In particular, the metal-oxide-semiconductor (MOS) structure is characterized by a threshold voltage V_{TH}, that is the voltage for which the electron concentration under the gate contact becomes equal to the p-base doping concentration. From the definition of V_{TH}, the behaviour of signal MOSFET can be divided in three operative regions, according to the values of the gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}). In particular:

- for $V_{GS} \leq V_{TH}$, the channel under the gate is not formed so there is no flow of charge in the structure and the drain current I_D is zero. To be precise, a rigorous analysis must take into account a subthreshold current, which depends exponentially on the V_{GS}[2];

[1] In the following, a n-type MOSFET will be referred to. The analyses can be easily extend to the p-type version.

[2] Analysis of subthreshold current modelling is presented in [4]

- for $V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$, the channel is formed and the current flow between the drain to the source terminals. In this condition the dependence of the drain current and drain-source voltage is linear and the devices is equivalent to a resistor whose value depends on the gate-source voltage.

- for $V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$, the voltage drop between drain and source "pinches-off" the channel. The effective voltage drop applied at the channel edges remains constant and the current slightly increases due to progressive reduction of the channel length (*effect of channel modulation*).

The I_D-V_{DS} characteristics are depicted in Figure 1.3 for different gate voltages.

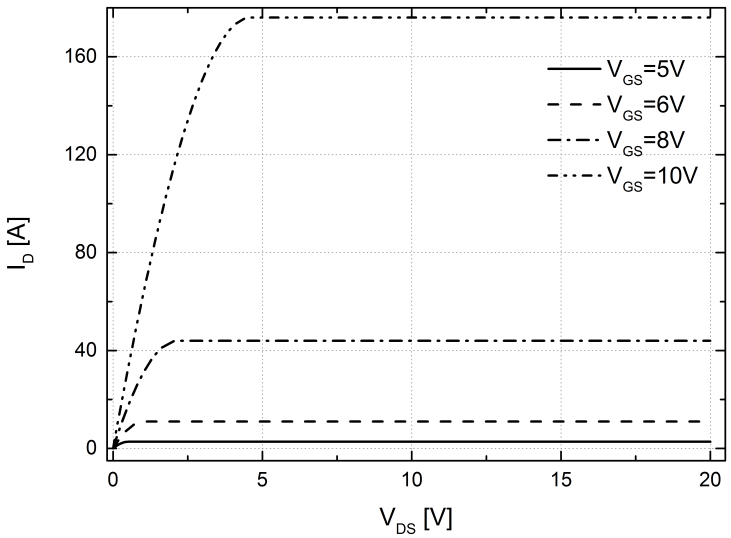


Figure 1.3: Simulated I_D-V_{DS} characteristic of MOSFET with different V_{GS}.

The I_D-V_{GS} characteristic, also known as trans-characteristic, is shown in Figure 1.4 evaluated at a fixed V_{DS} of 10 V and for different temperatures. A power MOSFET shows a threshold voltage typically of 3-4 V because of the thick gate oxide needed to withstand possible voltage spike induced on the gate during switching operation (the maximum voltage admitted on the gate is usually 20 V for safe operating modes).

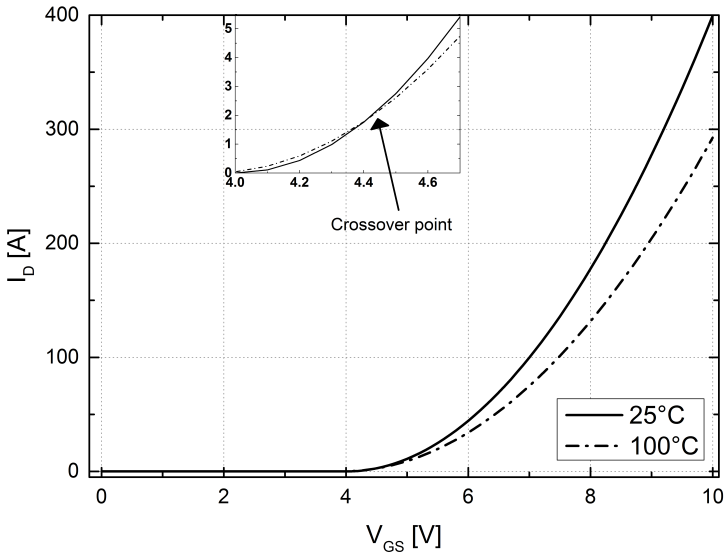


Figure 1.4: Simulated I_D-V_{GS} characteristic of MOSFET at V_{DS}=10 V.

The effect of the temperature on the current is of particular interest. As shown in the figure, by considering a fixed V_{GS}, larger then the threshold voltage, the device presents two opposite behaviours: for gate voltages slightly larger than the threshold voltage, the current increases with temperature whilst the behaviour reverts as V_{GS} grows. This is because the drain current in the linear region is proportional either to the threshold voltage V_{TH}, which has a positive dependence on the temperature, and to the carriers mobility μ_n which shows an opposite behaviour. With the increasing of the V_{GS} the effect of the first becomes less prominent and the mobility effect drive the current-temperature evolution. The value of V_{GS} that determines the boundary of the two regions is called cross-over point and it is much below the usual V_{GS} for all modern Power MOSFET devices operating in normal conditions. The negative feedback of drain current and temperature of the power MOSFET, at rated V_{GS} is very important because it ensures a uniform distribution of the current in multicellular structures.

1.1.3 On state conduction losses of the VDMOS

The voltage drop in on state causes a power dissipation which is the main limiting factor for low frequency operation. As a consequence, it is important to consider the different components that give the overall on state resistance R_{ON} of the power MOSFET and their dependence on the structure, as well as on the maximum voltage. With reference to the general VDMOS cell structure indicated in Figure 1.5, one can define the components of the resistance R_{ON} presented in the linear region ($V_{GS} > V_{TH}$, $V_{DS} \ll V_{GS} - V_{TH}$)[5]:

- The resistance of the source region with N+ diffusion, R_n^+. It only represents a small portion of resistance compared to other components that form R_{DSon}. It can be ignored in high-voltage Power MOSFETs;
- The channel resistance due to the electron flow into the channel (already seen in signal MOS), indicated as R_{CH};
- As the gate drive voltage is supplied, charges start to accumulate in the epitaxial layer surface and forms a current path between the channel and the JFET region. The resistance of this accumulation region is called R_A. The resistance varies according to the the charge in the accumulation layer and the mobility of the free carriers at the surface. If the gate electrode is reduced, its effect is the same as reducing the length of the accumulation layer, so the value of R_A;
- The JFET region resistance due to the electron flow into the N^- region that separates the two following P-body regions, indicated as R_{JFET};
- The resistance due to the electron flow into the epitaxial, low doped, drain region of thickness W_D down to the high doped drain region, indicated as R_{EPI}.
- The resistance of the substrate region. It can be ignored in high-voltage MOSFETs. In low-voltage MOSFETs, where the breakdown voltage is below 50 V, it can have a large effect on the total on resistance.

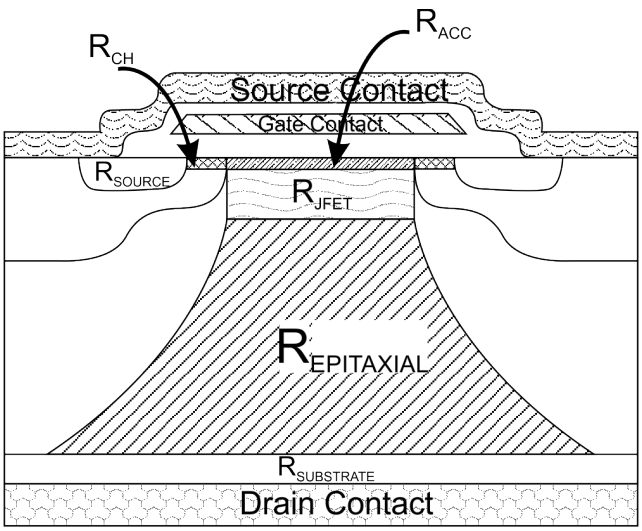


Figure 1.5: Components of the VDMOS internal resistance.

The R_{CH} and R_{JFET} components are mainly depending from the pitch of the elementary cell. The last component depends from the doping N_D and thickness W_D of the low doped drain region that are in turn also dictated by the maximum voltage $V_{DS_{MAX}}$ requirements for the device. As a consequence, the R_{EPI} component can be comparable with the other resistance components for a low voltage power MOSFET, while it will largely increase the R_{ON} value for an high voltage device. The Table 1.1 shows the impact of the main components of the device on state resistance for two devices rated for different voltage, namely 50 V and 600 V.

R_{ON} COMPONENT	V_{DSMAX}=50 V	V_{DSMAX}=600 V
R_{CH}	40%	2%
R_{ACC}	30%	2%
R_{JFET}	9%	1%
R_{EPI}	15%	90%

Table 1.1: Impact of the resistance components on the on state voltage drop for 50 V and 600 V Power MOSFETS.

As it shown in the table, for the low voltage power MOSFET the epitaxial layer contribution on the overall R_{ON} value is comparable to the R_{CH} and R_{JFET}. In this case, the accumulation region introduces a significant drop also. The first three component in the table are mainly determined by the cell pitch C and by the cell density of the chip. From 100 V onwards, the R_{EPI} component becomes relevant and it increases with voltage requirements. For values higher than 300 V it is essentially the only significant contribution to the on state voltage drop. Due to the limitation in static power dissipation, Power MOSFET diffusion is large up to 600 V application. Above this value, the silicon IGBT becomes preferable.

1.1.4 Transient Characteristics

One of the most interesting characteristic of Power MOSFET is the high commutation speed. This is very important for high frequency switching applications where the commutation times between blocking state and conduction state must be small. In this scenario Power MOSFET has a remarkable operation frequency up to 100 MHz [6]. The commutations from one state to the other are governed by the voltage applied at the gate terminal and therefore the analysis of the switching characteristics lays on the response of the device to voltage variations on the gate. The equivalent circuit shown in Figure 1.6 shows the elements which are mostly involved in switching transition.
In this figure, R_G is the is the distributed resistance of the gate and is approximately inversely proportional to active area, L_S and L_D are the strain inductances on the source and drain terminals. C_{GS}, C_{GD} and C_{DS} are the capacitances between the output terminals. The sum of C_{GD} and C_{GS} capacitances is the input capacitance of the device C_{iis}. The gate-drain capacitance, also known as Miller capacitance, consists on the series of the oxide capacitance and the depletion capacitance and shows a non linear behaviour with the voltage. In particular, when the device is in the blocking state, C_{DS} is mainly determined by the depletion capacitance and its value is low because the depletion region is thick; on the other hand, when the device is conducting, the depletion capacitance is very small because of the accumulation layer under the gate and therefore the C_{DS} is mainly determined by the oxide capacitance and its value is consequently large. This behaviour is shown in Figure 1.7.

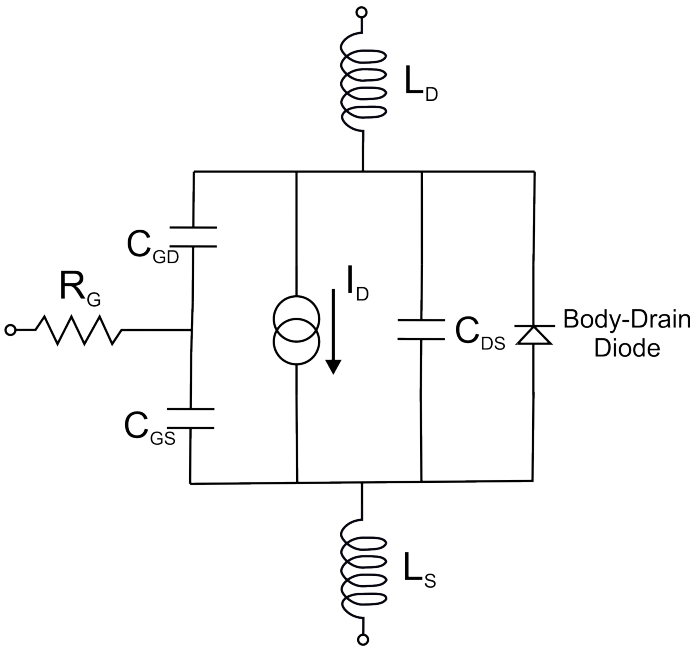


Figure 1.6: Equivalent switching model of the Power MOSFET.

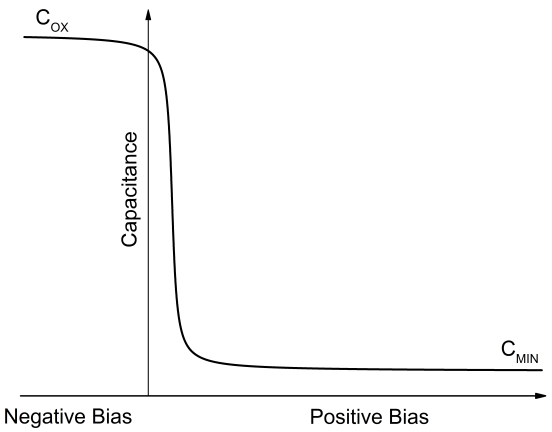


Figure 1.7: Dependence of the C_{DS} on the bias voltage.

To investigate the on- and off-switching characteristics, the simple power electronic circuit shown in Figure 1.8 is considered. Here a current is dictated by a load inductor which is usually simplified by a constant current source because of its high value. The flyback diode D is used to pick up the load current when the switch is off.

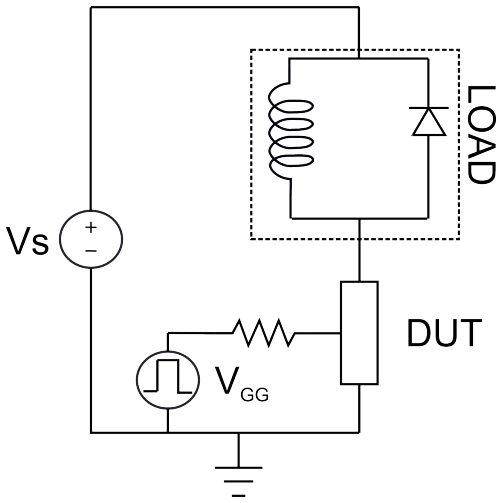


Figure 1.8: Simple power switching circuit for the analysis of the switching behaviour of a Power MOSFET.

Turn-on characteristics In this analysis the device is initially in the off state and the load current I_0 is consequently flowing into the diode. At time t_0, the driving circuit applies the voltage V_{GG} and starts to charge C_{GS} through R_G. The gate-source voltage controls the flow of the drain-to-source current I_D. During the time interval t_0-t_1 the voltage values is lower than the threshold voltage and the MOSFET remains in the blocking region with no current flow, regardless of V_{DS}. During this interval a gate current flows in order to charge the gate-source capacitance and the V_{GS} grows exponentially according to the $R_G C_{GS}$ time constant. For $t > t_1$ the V_{GS} reaches the threshold voltage and the device starts to conduct with a current proportional to the gate-source voltage. Assuming t_2 as the time when the drain current reaches the load current, during the interval t_1-t_2, V_{GS} keeps on rising exponentially while the gate current decreases exponentially as I_D approaches I_0. At t_2 the load current flows completely in the Power MOSFET and the diode

starts to switch off, that is, the voltage across the MOSFET decreases. During this phase the device is in pinch-off regime due to the high V_{DS}. As long as this regime persists, the V_{GS} voltage remains constant and a current from the driving circuit flows in the Miller capacitance because of the variation at the drain voltage. At time t_3 the device enters in the triode regime, the V_{DS} almost approaches the forward voltage drop and the gate voltage starts to rise again, with the same behaviour as in t_1-t_2 until it reaches finally the value of V_{GG}. The time evolution of the key electrical quantities is depicted in Figure 1.9. During the interval t_1-t_3 the voltage current product is large and the power dissipation is significant too.

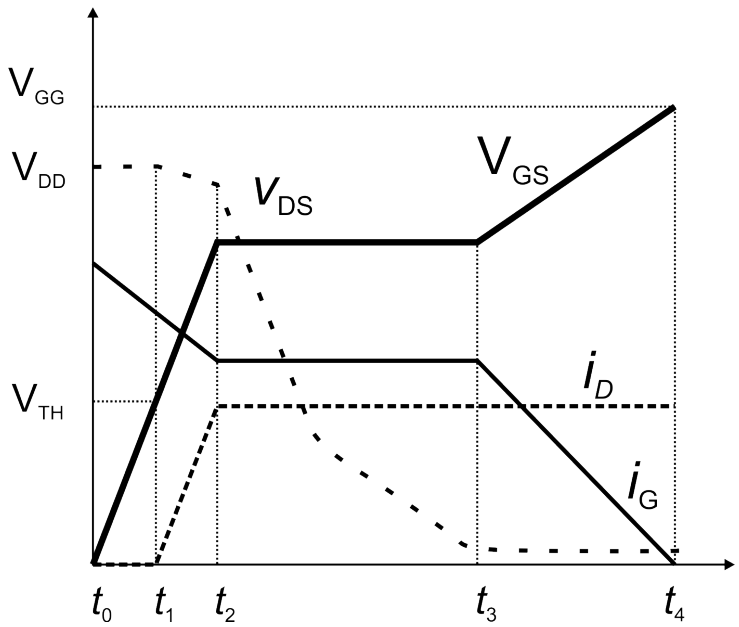


Figure 1.9: Power MOSFET turn-on waveforms.

Turn-off characteristcs In the initial state, the Power MOSFET is in the triode regime and it conducts the load current I_0 with the forward voltage drop V_{ON} and the diode is in the off state. At time t_0, the driving circuit brings the node V_{GG} to zero and the turn-off switching starts. In the initial phase, the gate-source voltage decreases exponentially, with a $R_G C_{GS}$ time constant, down to the value which brings the device in

pinch-off regime, at time t_1. Between $t_0 - t1$, a gate current flows from the C_{GS} towards the driving circuit. At time t_1 the voltage across the device starts to increase and a current is flowing in the Miller capacitance because the gate voltage is constant in the whole the pinch-off region. The device still brings the load current. This regime holds from t_1 to t_2 when the voltage at the drain is higher enough to switch on the diode D. As the diode turns on, its current increases and, as a consequence, the current in the Power MOSFET decreases and reaches zero, at time t_3. During $t_2 - t_3$, the gate-source voltage falls until it reaches the threshold voltage and the Power MOSFET switches off. During the time interval $t_1 - t_3$ the power dissipation in the device is significant. From t_3 to t_4 the gate voltage keeps on falling until it reaches zero. Figure 1.10 depicts the turn-off waveforms.

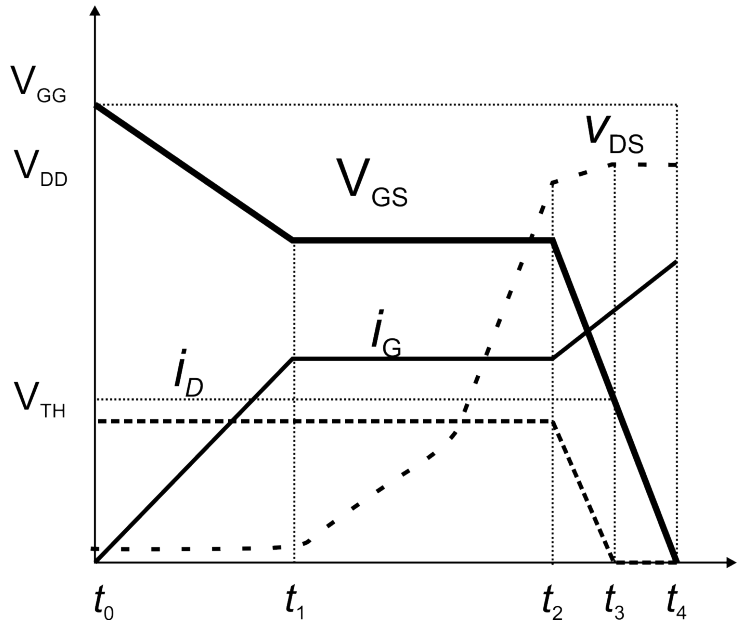


Figure 1.10: Power MOSFET turn-off waveforms.

1.1.5 Safe Operating Area

The safe operation area (SOA) of a device provides the current and voltage limits the device can safely operates into. If the operative trajectory

of the device completely lays in the SOA, no failures should occur. Typical SOA for a MOSFET device is shown in Figure 1.11.

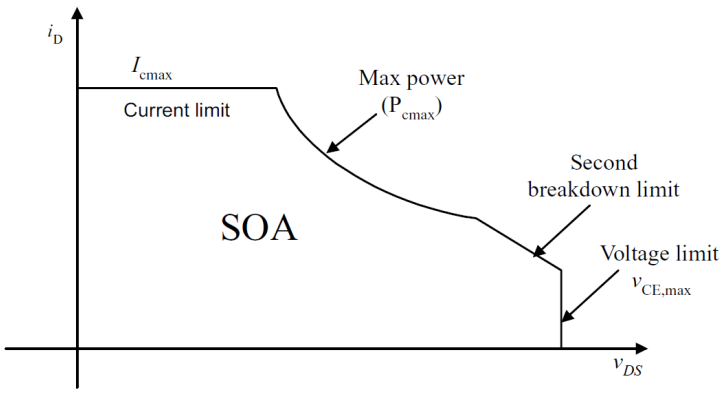


Figure 1.11: Safe Operating Area of a Power MOSFET.

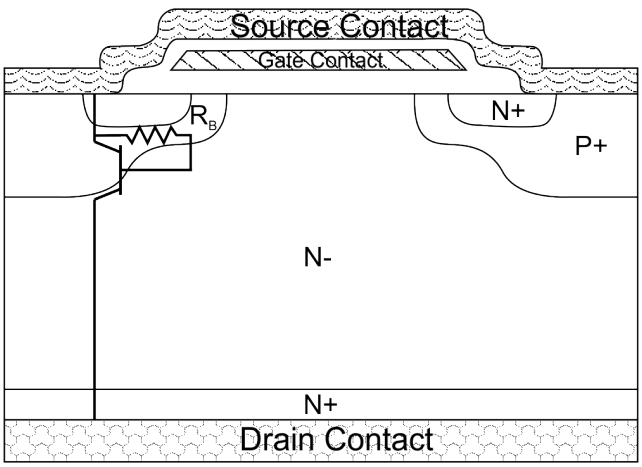


Figure 1.12: Parasitic bipolar transistor in Power MOSFET.

The maximum current limit while the device is in on state is determined by the maximum power dissipation, and it is directly related to its internal resistance. In particular, the positive relation, between on resistance and temperature, further limits the diffusion of the device for high voltage application. However, in the suitable range of application, today's commercial MOSFET devices have excellent high operating temperatures. As the drain-source voltage starts increasing, the device starts

leaving the on-state and enters the pinch-off region. During the transition time the device exhibits large voltage and current simultaneously. At higher drain-source voltage values that approach the avalanche breakdown it is observed that power MOSFET suffers from a second breakdown phenomenon. The second breakdown occurs when the MOSFET is in the blocking state and a further increase in V_{DS} causes a sudden drop in the blocking voltage. The source of this phenomenon can be addressed to the presence of a parasitic n-type bipolar transistor as shown in Figure 1.12. When the drain voltage approach the breakdown value, a significant current flows in the device because of avalanche multiplication. This current flows from the drain region, where the avalanche occurs, towards the body region, where it is collected by the source/body contact. Because of the parasitic resistance of the body region, a voltage drop arises that can directly bias the source/body junction, despite of the two region are externally shorted by the contact. In this case, the breakdown voltage of the NPN transistor passes from the higher value of BV_{CB0} (open emitter breakdown voltage) to the lower BV_{CE0} (open base breakdown voltage). In order to reduce this effect, the body doping must be increased but this would modify the threshold voltage. The Trench MOSFET shown in Figure 1.2 reduce the path of the current in the body region and therefore the occurrence of the second breakdown is significantly reduced, limited to very high current density.

1.2 The Insulated Gate Bipolar Transistor (IGBT)

The IGBT is a semiconductor device with four alternating layers (P-N-P-N) that is controlled by a metal-oxide-semiconductor (MOS) gate structure without regenerative action. This mode of operation was first experimentally discovered by [7] in vertical device structures with a V-groove gate region and reported in the literature in 1979, where it was named "Vgroove MOSFET device with the drain region replaced by a p-type Anode Region". First manufactured prototypes suffered of latch-up phenomena during the operation range. The first proposal reporting latch-free device was issued in 1980 [8]. Complete suppression of the parasitic thyristor action and the resultant non-latch-up IGBT operation was achieved by Nakagawa et al. [9]. Once the latch-up phenomenon had been completely overtaken, the interest for the device grew remarkably as it proved to be a very robust device. This is because it shows a significantly smaller forward voltage drop compared to a equal rated Power MOSFET, sharing however the same input characteristics, namely high input resistance, voltage control, and zero current absorption from the driving terminal during the static states. What is more, it was demonstrated that the power density capability of the IGBTs can easily reach the value of $5 \times 10^5\,\mathrm{W\,cm^{-2}}$ [10]. Nowadays, thanks to the technological improvements, IGBT has become the most important power devices for medium and high power applications.

1.2.1 Basic structure

Figure 1.13 depicts the cross section of a basic IGBT structure for a Planar Non-Punch-Through IGBT (NPT-IGBT), here considered as exemplary design; a lot of different structures have been in fact presented over the years. The device is composed by paralleling thousands elementary cells, a design which is common to all the power devices. For the IGBT, as for the Power MOSFET, the multicellular design poses no issues because it has an intrinsic thermal stability. As mentioned before the structure shows a P-N-P-N thyristor structure, that can be activated by the voltage on the gate terminal. More in detail, the N+ region is the emitter diffusion, which represents the source of the MOSFET part of the device, the P-body region is the body of the MOSFET part of the device and the collector of the vertical PNP structure present into the IGBT. As in the Power MOSFET, the doping concentration of

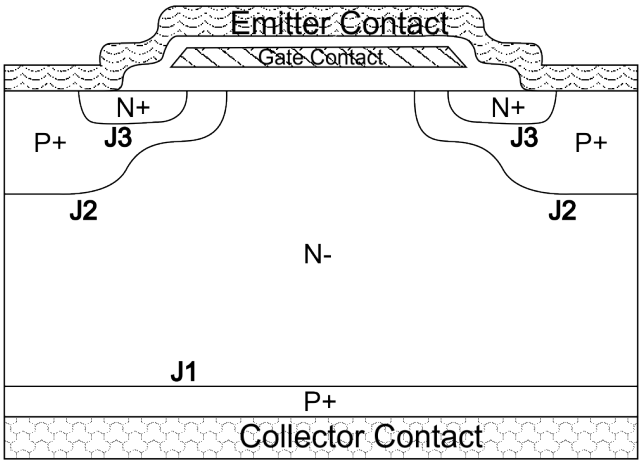


Figure 1.13: Cross section of an IGBT elementary cell.

the P-body region at the Silicon/Oxide interface defines the threshold voltage of the MOSFET part of the device. The structure presents the thick low-doped region, common of all the power devices, which sustains the voltage when the device is in the blocking state. In the IGBT, this region represents either the low-doped drain of the MOSFET and the n-base of the vertical PNP. The P+ region is the collector of the IGBT (the emitter of the vertical PNP) and it is also called hole-injecting layer. The NPT structure is usually made by starting from a low doped silicon wafer with a thickness which depends on the blocking voltage of the device. The back of the structure is obtained by doping diffusion up to the junction J1. The top designs of a planar IGBT is made with the same technological steps of the Power MOSFET. In particular, Self-Aligned process is used in order to reduce the parasitic resistance of the structure.

1.2.2 Device operation

The presence of the P+ collector layer is the key of the success of the IGBT since it allows the conductivity modulation into the drift-layer in on state conditions. If the gate-emitter voltage is kept to zero, the device is in the blocking state. In this situation, by increasing the Collector voltage, the collector-drift junction (J1) becomes forward biased, while the P-body-drift junction (J2) is reversely biased and the current

flow is limited by the leakage current of this junction. This is called forward blocking condition, and the limit of this condition is the breakdown of J2 that is the open base breakdown voltage of the PNP. By applying a negative potential to the collector terminal, and still keeping the gate-emitter voltage to zero, junction J1 is reversely biased while J2 is directly biased. This is the reverse blocking condition. Being the NPT structure symmetric with respect to the drift layer, the forward blocking capability is equal to the reverse blocking capability, assuming high level of doping for the P-base and collector regions. In general, according to the particular structure considered, the reverse blocking and forward blocking modes can be different and also have different breakdown voltages. The device on-state condition is achieved when a gate-emitter voltage higher than the threshold voltage is applied. In this condition, a positive collector-emitter voltage let the electrons to flow across the MOSFET channel under the gate and then across the drift region. At the same time, holes are injected from the collector, because of the directly biased collector-drift junction, and they flows in the drift region and recombines with electrons injected by the channel. In this condition the double injection occurs into the drift layer because of both the holes injected from the collector-drift and the electrons coming from the N-MOSFET channel. The exceeding holes are collected by the collector of the PNP. As long as the free charge concentration in the drift is lower than the doping, the only excess of carriers is represented by the holes that don't recombines with the electrons. As the current density increases, the density of the mobile charges becomes higher than the doping concentration of the drift layer. In this condition, in order to keep the neutrality of the charge in the drift layer, high concentrations of both electrons and holes are reached, and the voltage drop is consequently reduced. This effect, which is also present in all the bipolar power devices, is called conductivity modulation. Therefore an IGBT presents a voltage drop lower than the Power MOSFET considering the same current density and the same voltage rate. Because of the overall doping profile, the P-body/drift junction cannot be directly biased in on-state, therefore the vertical PNP never enters in saturation mode. However, when the voltage drop across the inversion layer becomes comparable to the difference between the gate voltage and threshold voltage, the MOSFET enters in pinch-off condition, limiting its own current, and consequently the overall current as well. Even though the conductivity

modulation has the upside of reducing the on voltage drop, it has also a major drawbacks. In fact, during the on-state, for the conductivity modulation to occur, a high amount of charges must be stored. When the device is switched off by applying zero voltage between gate and emitter, the channel of electrons is rapidly removed but the remaining charge stored in the drift region is removed only by means of the recombination phenomenon, because there is no external terminal accessing to the drift region, and it takes further time for the device to be depleted of charges. During the charge removal time the device exhibits the typical collector current tail which differentiates the IGBT from the Power MOSFET. From what said before, a clear drawbacks arise between forward voltage drop and turn-off switching times: by increasing the excess charge concentration in the drift layer, the forward voltages is reduce but it takes more time for the device to turn-off.

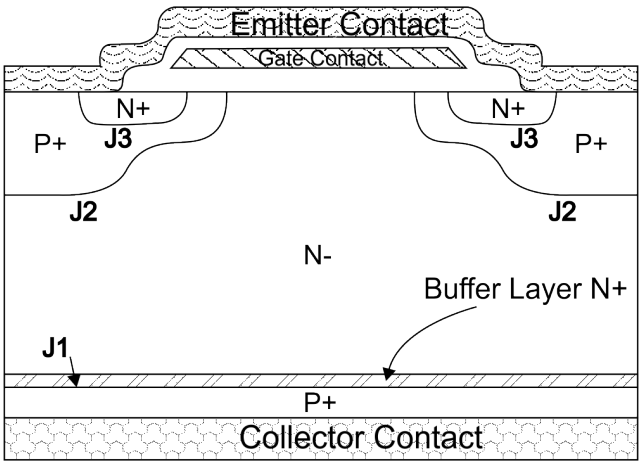


Figure 1.14: Cross section of a Punch-Through IGBT.

A structure which reduces the off switching time, but having a larger on state voltage drop, is presented in Figure 1.14 [11]. The structure, named Punch-Through IGBT (PT_IGBT), has an additional highly N doped buffer layer between the collector and drift region. Because higher electron density in the Buffer layer, the holes injected from the collector, partially recombines with the electrons of the buffer and the overall injection efficiency of the collector junction is reduced. Moreover, the minority carrier lifetime in the base region is reduced. This leads to a lower charge concentration in the drift layer, which turns into an higher

voltage drop in the on state, and to a faster recombination of excess charges during the turn-off phase, that is a shorter turn-off times. Besides the particular structure considered, lifetime control techniques can be adopted to reduce the lifetime of the free carriers in the drift region, therefore reducing the recombination times and consequently increasing the switching speed.
As already mentioned, the lower on voltage drop of the IGBT makes it preferable with respect to Power MOSFET in terms of on state static power dissipation. It is however important to point out that the overall voltage drop is produced, besides from the drift region, also from the contribution of the internal resistances already shown in the Power MOSFET, due to the similarity of the two devices in the top part of the structure. Therefore, as long as the voltage requirements are low, the contribution of the additional resistances are relevant and the benefits of the conductivity modulation in the drift region are not so evident. Practically, for applications up to 600 V, Power MOSFET is still the most diffused device because of its higher speed, while for higher voltage applications the IGBT is considered the most interesting device.

1.2.3 Static Characteristic

The analysis of the forward conduction characteristics of an IGBT can be conducted by means of two equivalent circuit shown in Figure 1.15. The first model is based on a PiN-rectifier in series with a MOSFET and it gives only an approximation of the device behaviour in the forward state. In fact, this model does not consider the current produced by the holes flowing into the P-base region. The P-base-drift junction is in fact reverse biased during forward mode and therefore the free charge density must be zero as approaching the junction. As a consequence, the IGBT conductivity modulation in the drift region is identical to the PiN-rectifier near the collector junction, but it is less than a PiN-rectifier near the p-base junction [7]. Therefore, a second model, based on a Darlington configuration of a Power MOSFET, whose current supplies the base current of a PNP transistor, is considered which gives a deeper and more precise description of the conduction characteristics. The analysis of the IGBT operations by means of these models shows that IGBT has a voltage drop produced by the collector-drift junction which is the same of a Power diode. If the collector-emitter voltage is lower than the diode threshold voltage, there is no significant current

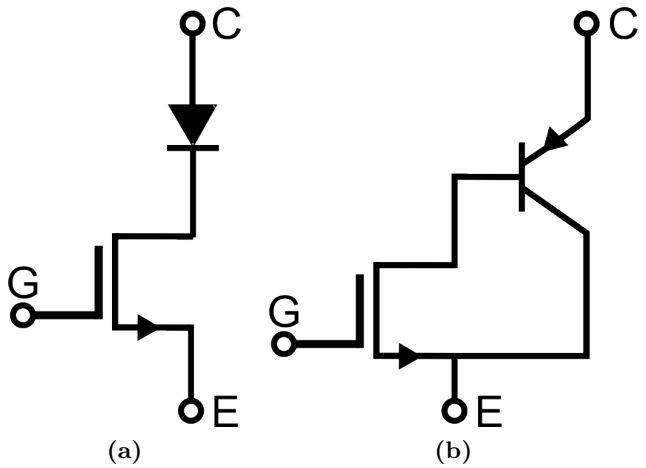
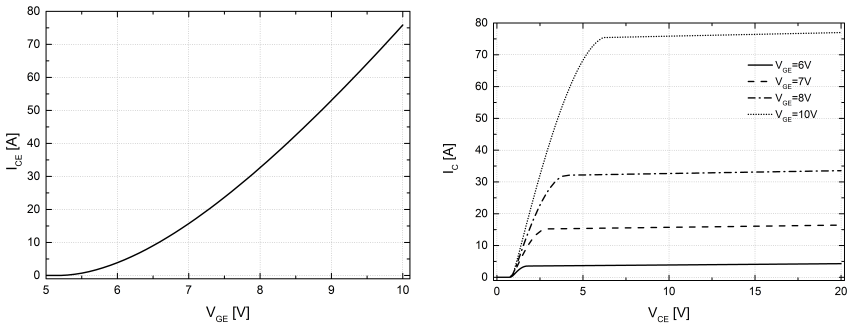


Figure 1.15: Equivalent model of an IGBT: a) Power MOSFET and diode; b) Power MOSFET and PNP transistor in Darlington configuration

flowing into the device. What is more, the device current is controlled by the gate-emitter voltage which creates the electron channel between the emitter and the drift region. By increasing the gate-emitter voltage, more electrons are injected in the drift regions and the overall current increases. The $I_C - V_{GE}$ characteristic has the same behaviour of the one of a Power MOSFET. As already mentioned, the IGBT enters in the saturation region when the MOSFET current saturates due to the pinch-off. These conclusions can be drawn from both the models in Figure 1.15. On the other hand, analysis conducted on the second model shows an important effect. In fact, because of the large thickness of the drift region and its low doping concentration, the PNP transistor has a low current gain factor and this means that the Power MOSFET in the equivalent circuit of the IGBT carries a major portion of the total collector current. Therefore, the IGBT on-state voltage drop includes also the significant drop across the MOSFET portion. In particular, the low value of the conductivity modulation near the P-base junction causes a substantial drop across the JFET resistance of the MOSFET in addition to the voltage drop across the channel resistance and the accumulation layer resistance [12]. If the lifetime in the drift region is large, the PNP gain is large and as a consequence the MOSFET current contribution to

the overall collector current is lower. In this condition, the voltage drop across the MOSFET component of IGBT is a small fraction of the total voltage drop. When lifetime control techniques must be used to increase the speed, the current gain of the bipolar transistor is reduced and the voltage drop of the device is increased. The static characteristic of the IGBT are shown in Figure 1.16.



(a) **(b)**

Figure 1.16: IGBT simulated static characteristic: a) $I_C - V_{GE}$, V_{CE}=10 V; b) $I_C - V_{CE}$ at different gate-emitter voltages.

In order to decrease the resistance of the MOSFET current path, trench IGBTs have been developed. The structure is shown in Figure 1.17.

In this structure, the elimination of the JFET and accumulation regions reduces the resistance offered by the MOSFET current. Trench structure produces also a higher robustness to latching because it reduces the resistance path in the P-base region.

1.2.4 Transient Characteristic

For the analysis of the IGBT switching behaviour it will be referred to the same simple circuit used for the Power MOSFET with an inductive load clamped by a free-wheeling diode1.8. The consideration about the inductor load can be extended also for the IGBT case, and therefore it will be represented as a constant current source during the on- and off-switching of the device.

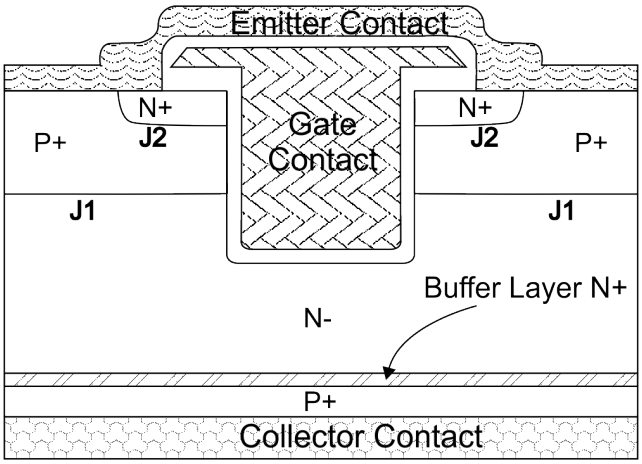


Figure 1.17: Structure of a Trench IGBT.

Turn-on characteristics The turn-on switching performance of the IGBT is dominated by its MOS structure, and therefore the same analysis of the Power MOSFET turn on can be done. In particular, when the voltage V_{GG} is applied by the driving circuit, the gate potential starts to increases exponentially, according to the input capacitance and resistance. This behaviour holds until the device is able to bring the load current and subsequently the flyback diode turns-off and the potential at the collector node starts to fall. During this phase, both the collector voltage and current are high and therefore the power dissipation is high. The collector voltage falls initially to a value which is similar to the forward drop of a Power MOSFET. That is because it takes a finite time for conductivity modulation to take place inside the drift layer, and, after then, the voltage drop falls to its minimum value. At this point the gate potential start to rise again up to the value set by the driving circuit and the turn-on switching ends.

Turn-off characteristcs Turn-off transient starts by driving the external gate terminal V_{GG} to zero. As a consequence, the gate-emitter voltage drops exponentially down to the value which leads the device in saturation. Collector voltage and current remain constant during this phase. A this point, the collector voltage rises, but the current is still constant, as determined from the saturation condition. By increasing the collector voltage, a current flows into the Miller capacitance towards

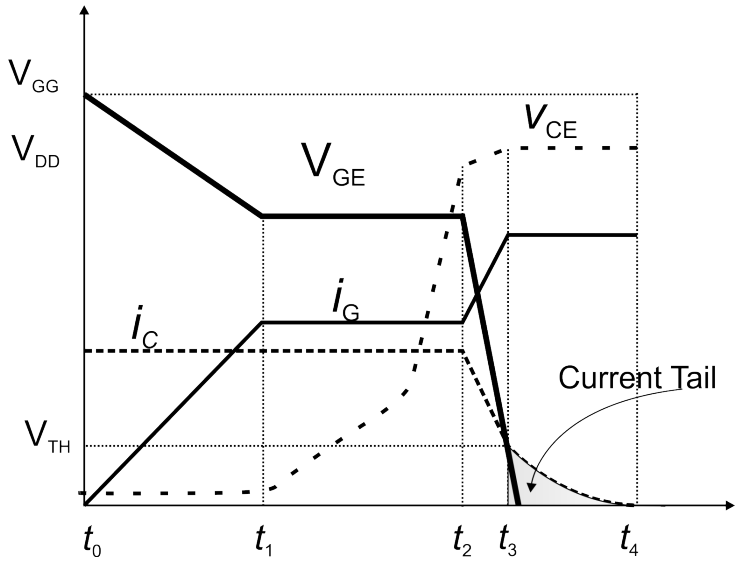


Figure 1.18: IGBT turn-off characteristics.

the driving circuit, across the gate resistance. This resistance determines the current flowing in the Miller capacitance and, as a consequence, the rate of rise of the collector voltage and it is a critical project parameter. The flyback diode starts to conduct when the collector voltage reaches a sufficient high voltage and its current increases. as a consequence, the IGBT current decreases to a finite value because of the stored charge of the drift region. The high minority-carrier concentration stored in the drift region supports the collector current after the MOS channel is turned off. Recombination of the minority carriers in the wide-base region gradually decreases the collector current and results in a current tail. The interval needed for the charge to recombine is usually large because the excess of charge is high for reducing the on voltage drop. In this phase the collector voltage is at its maximum value and the finite current determines a significant power dissipation in the device. Due to the large duration of the current tail, the IGBT operating frequency is limited and there is a trade-off between on-state losses and switching times. In order to partially overtake this drawback, localised control of lifetime is used in order to reduce the recombination time of the free carriers in the drift region. Turn-off waveforms are reported in Figure 1.18.

1.2.5 Latch-up of Parasitic Thyristor

Considering the carriers path in the IGBT structure, a portion of the minority carriers injected into the drift region from the collector flows directly to the emitter terminal. The negative charge of electrons in the inversion layer attracts the majority of holes and generates the lateral component of hole current through the p-type body layer. This lateral current flow develops a voltage drop across the spreading resistance of the P-base region. If this current is significant, the base-emitter junction of the NPN-parasitic BJT can become forward biased. By designing a small spreading resistance, the voltage drop is lower than the built-in potential and therefore the parasitic thyristor between the P^+-collector region, drift region, P-base region, and $N+$-emitter does not latch up. Larger values of on-state current density produce a larger voltage drop, which causes injection of electrons from the emitter region into the P-base region and hence turn-on of the NPN-transistor. The NPN current drives the PNP-transistor to the on state, and therefore the parasitic thyristor will latch up and the gate loses control over the collector current.

Under dynamic turn-off conditions the magnitude of the lateral hole current flow increases and latch-up can occur at lower on-state currents compared to the static condition. The parasitic thyristor latches up when the sum of the current gains of the NPN- and PNP-transistors is larger than one. When the gate voltage is removed from IGBT with a clamped inductive load, its MOSFET component turns off and reduces the MOSFET current to zero very rapidly. As a result the drain-source voltage rises rapidly and is supported by the junction between the N^--drift region and the P-base region. The depletion layer extends more in the drift region as a consequence of the lower doping, therefore reducing the effective base width of PNP. Hence, the current gain of the PNP-transistor portion, α_{PNP}, increases and a greater portion of the injected holes into the drift region will be collected at the junction of P-base and N^--drift regions. Therefore, the magnitude of the lateral hole current increases, and also the lateral voltage drop does. As a result the parasitic thyristor will latch up even if the on-state current is less than the static latch-up value. Reducing the gain of the NPN- or PNP-transistors can prevent the parasitic thyristor to latch-up. However, a reduction in the gain of the PNP-transistor increases the IGBT on-state voltage drop so the latch up ruggedness must be incremented by reduction of the gain

of the NPN-transistor. Reduction of carrier lifetime, use of Buffer layer, and use of deep P^+-body diffusion improve the latch-up immunity of IGBT. Nevertheless, inadequate extension of the P^+-region may fail to prevent the device from latch-up. Also, care should be taken that the P^+-diffusion does not extend into the MOS channel because this causes an increase in the MOS threshold voltage.

1.2.6 Safe Operating Area

IGBT Safe Operating Area represents the values of current and voltage for which the device can safety operate. As like as the Power MOSFET, it gives an immediate indication of the maximum limits of the device. For the IGBT it must be separately considered the case of forward operations, that is when the gate-emitter voltage is positive, and reverse operations, when the gate-emitter voltage is zero or negative. As a consequence, two SOAs are considered.

Forward Biased Safe Operating Area (FBSOA) The FBSOA is represented of the safe operations conditions when the devices turns-on and both electrons and holes flows in the IGBT and the collector voltage is still at high values. In these condition the limits depends on different phenomena. In particular, the maximum sustainable voltage depends on the breakdown phenomenon,while for lower voltage the limit is imposed by the maximum power dissipation. Finally, for very low voltage the maximum current is limited by the latch-up phenomenon. For the avalanche breakdown is important to underline that the maximum value can be significantly different from the one stated by the doping concentration in the drift region. When the current flowing in the device is significant, the net charge concentration in the drift region is increased with respect the doping concentration because of the holes injected by the collector/drift junction. Being the breakdown voltage inversely dependent on the charge concentration, the breakdown voltage reduces with the current. What is more, this value is further reduced by the gain of PNP transistor which amplifies the avalanche current.

Reverse Biased Safe Operating Area (RBSOA) In reverse biased condition, the IGBT is in blocking state, that is no electrons flow in the device in normal operation and there is only a holes current. The RBSOA is therefore limited only by the avalanche phenomenon of the

P-base-drift junction. The hole concentration increases the value of the net charge in the drift region and hence the breakdown voltage is lower than avalanche breakdown voltage determined by the background donor concentration and it reduces with the increasing of the current. It is also lower than the correspondent FBSOA breakdown voltage because there is no concentration of electrons that partially compensates the holes. RBSOA is also limited, for lower voltage, to latch up effect. When an IGBT turns off the device current is determined only by the holes flowing from the collector to the body contact across the drift and P-base region. When the voltage drop produced by the P-base parasitic resistance is sufficient for turns on the NPN transistor, the parasitic thyristor turns on and latch up occurs. This phenomenon limits the maximum current flowing in the structure for low voltage values.
The IGBT FBSOA is depicted in Figure 1.19.

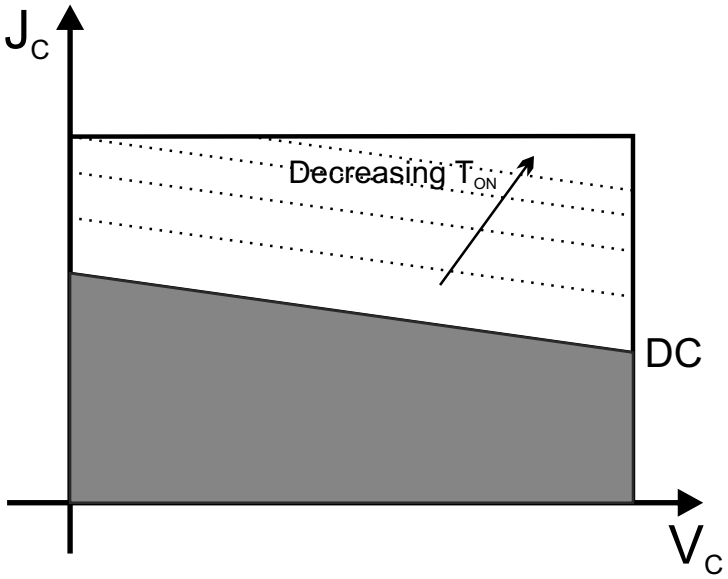


Figure 1.19: Safe Operating Area of an IGBT at different durations of the on time.

1.3 Compact Models

Compact Modelling refers to the development of models for semiconductor devices for use in circuit simulations. The models are used to reproduce device terminal behaviours with accuracy, computational efficiency, ease of parameter extraction, and relative model simplicity for a circuit or system-level simulation. Most of the compact models of a power device are usually not physical, that is they don't reproduce the real phenomena which takes place into the device, but rather try to represent the electrical behaviour as seen from the external terminals. Some of the models are, in turn, derived from physical approach and in this case the compact models implement, by means of proper elements, the analytical expression which describe the physical behaviour of the device. The latter are usually much more complicated and suffer of convergence issues or can be used proficiently only for particular analyses. What is more, the dependence on temperature of the electrical behaviour of power devices has been thoroughly investigated in the past in order to considers the self-heating that induced limitation of the Safe Operating Area (SOA). The simulation of self-heating effect in power-devices is nowadays quite easily performed and a number of different techniques and even commercial software packages have been developed to perform this task. Nevertheless, having the power devices a multicellular structure with a large area, an electro-thermal simulation that accounts for the interaction between a large number of elementary cells must be performed in order to consider electrical and thermal lateral interplay between nearest neighbour cells. Simulations of multicellular structures which also includes self-heating effects represents, even today, a very hard task. Approaches used for these simulations are analysed in the second chapter. One of this approach is implemented by means of one dimensional compact models for the electrical behaviour and thermal behaviour. It is therefore important introduce a brief historical layout of the several models which have been proposed for the power devices. In this section, compact modelling of Power MOSFET and IGBT are considered.

1.3.1 Power MOSFET

The compact modelling development process for a Power MOSFET is usually based to adapt the model of signal MOSFET in order to imple-

ment the additional effects which are present in the power device and which are not included in the signal model. For the static behaviour, this means to include the additional drops produced by the internal resistances and to consider the internal PiN diode. The dynamic behaviour must include the dependence of the gate-drain capacitance on the drain voltage.
Being the equation of the signal MOSFET well established in the scientific literature, the most of the models are based on analytical description with additional equations for the effects proper of the Power MOSFETs. A two-component MOSFET resistor model appropriate for computer-aided circuit design has been first reported in [13] where the effects of velocity saturation, mobility reduction, non uniform impurities concentration in the channel, and spreading resistance in the drift region are considered. A first model of the on state resistance has been proposed by [14] in the 1980. In [15], a large signal model of the device has been reported in 1983. In 1985, a SPICE II Power MOSFET model including the effect of the JFET region was proposed by [16]. Later paper of Yee et al. [17] recommends to omit the JFET transistor and affirms that a simple resistor can be added to include the effect of the epitaxial resistance. In 1990, a Power MOSFET model optimized for resonant converters simulations was developed [18]. Self-heating effects on the electrical device behaviour was modelled by Kraus et al. [19] in 1992, including the thermal parameters of the device and the package. Later articles introduce model dedicated for Trenches Power MOSFETs [20, 21]. Finally, a model describing the avalanche phenomenon in the Power MOSFET was developed in 1997 [22].

1.3.2 IGBT

Historical IGBT models can be divided into four principal category [23]. The first category *mathematical*, refers to analytical models based on semiconductor physics. By means of simplifications in the physical phenomena, results in analytical expressions can be obtained which model the electrical behaviour of the device. Several early IGBT models were based on semiconductor physics. Turn-off behaviour of the IGBT was first modelled by Baliga [24] as a MOSFET driven PNP transistor, allowing the separation of the electron and hole current flow. Kuo et al. [25] gives an analytical expression for the forward conduction voltage taking into account the conductivity modulation in the base of both

punch-through (PT) and non-punch-through (NPT) IGBTs. However, this model is not complete for circuit simulation because the MOSFET section, which is critical in transient simulation, has not been included. Hefner [26] and Hefner et al. [27] developed the first complete one-dimensional (1-D) analytical, charge controlled model suitable for circuit simulator implementation. Kraus et al. [28] modelled non-zero minority carrier concentration at the emitter edge of the base by averaging a sinusoidal lateral distribution. Dynamic carrier distribution was approximated by a polynomial. An important feature of the IGBT, namely, the enhancement of base conductivity modulation resulting from the accumulation layer under the gate, was modelled with a P-i-N diode for a Trench IGBT (T-IGBT) [29].

The second IGBT modelling category is *semimathematical*. Such models are partially based on physics in combination with existing models (in the Spice family, Saber, etc.) for other components. Most of the models in this category use existing MOSFET and BJT models connected with other parts to account for some specific effects in an IGBT. The efforts for this models are aimed to include the power device features by modifying the model already developed for the basic components. As an example, in [30], a modified Ebers-Moll model was used for the BJT. This category of models has not the same accuracy as the as mathematical models, because they use model of commercial power BJTs which however have different characteristics with respect the wide-base internal BJT of the IGBT structure.

The third model category is *behavioural* or *empirical*. These models aim to reproduce the electrical behaviour without considering the real device physic. Measured IGBT characteristics are fitted by different methods. The resultant expressions are then used in a simulator to model the IGBT. In [31], IGBT output characteristics are modelled by a resistor and a current source. A look-up table method is used for obtaining the values of the resistance and the current source. The models of this category are unable to predict DC or transient characteristics.

The last IGBT model category is referred to as semi-numerical. This models are a mixed solutions between the first category and the FEM. In particular the finite element methods are used to model the wide base, which is the most difficult part to be analytically described, while the other device parts are modelled by means of analytical expressions. Because of the complexity and difficulty in modelling IGBT base, nu-

merical methods were employed to improve the accuracy of some models. In [32], as an example, the ambipolar diffusion equations are solved numerically in the base region. The models in this category have been implemented into Saber, but it is quite complicated to implement them into normal circuit simulators.

1.3.3 Thermal Networks

The design of a power electronics system requires to pay particular attention on the thermal constraints as well as the electrical characteristics. Over designing the system adds unnecessary cost and weight; under designing the system may lead to overheating and even system failure. The optimal solution is not always easy to find and it requires to know the heat generated by each device and the effects of the heating on the other components. In this scenario, thermal simulations significantly help to achieve a good comprehension of the thermal behaviour of the system. Different ways can be used for modelling a thermal domain. In particular, as like as simulation of electrical systems, two are the main approaches, namely FEM analyses and compact models analyses. FEM analyses is described in more detail in the next chapter and here a brief description of thermal models will be provided.
Compact models of a thermal domain is mainly related to find a simpler and faster way to solve the heat transfer equations applied to power devices and electrical components in general. The basic principles of thermal analysis are similar to those in the electrical domain. Understanding one domain simplifies the task of becoming proficient in the other. This is especially clear when we consider thermal conduction. The approach can be extended to the other heat transfer physics, namely convection and irradiation.
Each thermal domain can be characterized by two variables, that is temperature and thermal power. As shown in Figure 1.20, the thermal power variable can be thought of as the parameter that flows from one reference point to another and it is equivalent to the current in an electrical system. On the other hand, temperature can be thought as the variable that forces the flow of heat and it has in the current the electrical counterpart. In each domain the forcing function is a difference in potential; in one domain it represents temperature and, in the other, the voltage [33]. Both systems have impedances the regulates the flow of the through variable. With this equivalence it becomes easy to model

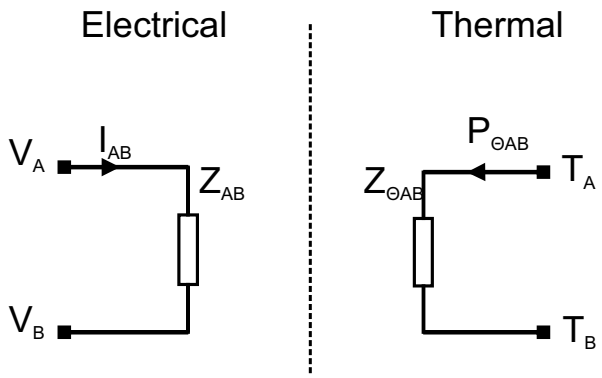
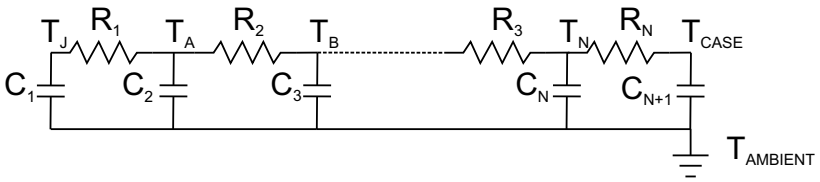
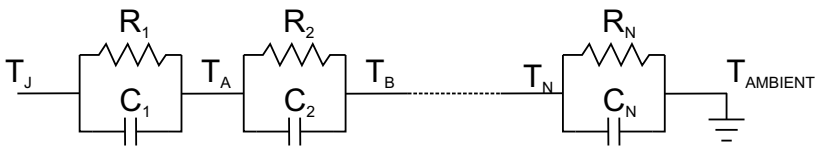


Figure 1.20: Fundamental relationships in the electrical and thermal domains.

a thermal network and solve the equation by means of the same analytical approaches seen for the electrical analyses. For what concerns the power devices, the thermal behaviour can be modelled using two equivalent electrical network [34]:



(a)



(b)

Figure 1.21: a) Grounded Capacitor Thermal Network ("Cauer" Ladder); b) Non-Grounded Capacitor Thermal Network ("Foster" Ladder).

- **Grounded Capacitor Thermal Network ("Cauer" Ladder)**. The grounded-capacitor network describes each "node" of

the thermal system with a connection to thermal "ground" by means of a thermal capacitance. DC temperature drop is obtained by thermal resistance between nodes. The main advantage of a grounded-capacitor network is that it derives from the fundamental heat transfer physics. An exemplary network is shown in Figure 1.21a. It is simply convenient to draw the network as in the figure because, as the lower edge of each capacitance attaches directly to ground, the connections between the "nodes" are essentially through the resistors.

Being this network based on a physical description, is it possible that some of the "nodes" of the model can actually represent a point of the physical system. As an example, each R-C couple can be the description of silicon junction, back of silicon chip, baseplate, board, heat sink and finally ambient. Clearly, not all the nodes necessarily have a physical counterpart. What is more, such simple representation is not always a reliable model of the heat flow, especially when the flows has not a single path. In this case, more chains are required for modelling correctly the overall thermal problem.

- **Non Grounded Capacitor Network ("Foster" Ladder)**. The non-grounded-capacitor network (Figure 1.21b) synthesizes the thermal systems by means of the series of R-C paralleled couple. Contrast with the Cauer network, this approach is non-physical because, having such a connections, the capacitance takes into account the variation in the time of temperature drop between two neighbour nodes, and this terms is not clearly present in heat transfer equation, which in turns considers the variation of a single node temperature with respect to ground. However, there is a mathematical simplicity underlying such schematic. In their mathematical description, each resistor-capacitor pair models a single contribute, with a unique time constant, to the overall system response. Therefore, by using a Foster ladder, every transient temperature evolution can be fitted by properly choice of the number of R-C pairs and values of each pair. In this terms, the Foster network is composed by a series of exponential terms consisting of amplitudes and time constants for fit to the Temperature versus Time diagram to whatever degree of accuracy is desired.

The dynamic ET feedback is enabled through a pre-processing stage articulated in the following steps:

- Transient 3-D thermal-only simulations of the DUT are preliminarily carried out through a FEM tool, the accuracy of results being ensured by a careful device representation, as well as by the adoption of smart mesh-refinement strategies. For this task, each individual cell resulting from the aforementioned discretization is associated to a heat source; by alternately activating only one source and monitoring the transient temperature increase over all the cells, the time evolution of the self-heating and mutual thermal impedances are numerically determined.
- The matrix of thermal impedances is modelled with an equivalent electrical network including linear controlled sources, as well as resistances and capacitances, the values of which are optimized by resorting to a custom routine (identification and synthesis step).
- An ET feedback block embodying the selected topology – devised to evaluate the temperature of each cell from the powers dissipated by all cells – is automatically generated and connected to the subcircuits.

Therefore to fit the thermal behaviour of a particular domain it requires a pre-processing effort to accurately determine the matrix of thermal impedances for the transistor, and thus identify/synthesize the feedback block.

1.4 Characterization Tests of the Reliability of Power Devices

1.4.1 Unclamped Inductive Test (UIS)

All semiconductor devices are rated for a certain max reverse voltage which limits the SOA of Power Devices. Operation above this threshold will cause high electric fields in reversed biased p-n junctions. Due to impact ionization, the high electric fields create electron-hole pairs that leads to increased current due to avalanche multiplication. The reverse current flow through the device causes high power dissipation, associated temperature rise, and potential device destruction. Power devices are normally chosen with a maximum sustainable voltage higher than the maximum voltage of the application where they are used. Therefore the avalanche operation should be never experiment in normal conditions. Nevertheless, either because the presence of parasitic elements in the interconnection, or because of not perfect clamping of circuit inductance it is not uncommon that devices experiments overvoltage spikes and the avalanche operations is likely to occur, especially for high speed voltage swings. What is more, some applications, such as automotive fuel injection, are designed for the avalanche to occur in normal operative condition [35, 36]. For this reason, the characterization of the capability of a power device to withstand the avalanche event must be evaluated. As an example, some power semiconductor devices are designed to withstand a maximum amount of avalanche current for a limited time and, therefore, is avalanche rated for up to that current. Others will fail very quickly after the onset of avalanche. The difference in performance lays on from particular device physics, design, and manufacturing. As a consequence, ways to measure the avalanche capability has been designed. The most common approach is represented by the Unclamped Inductive Switching (UIS) test [37–39]. The circuit representation of a UIS test is depicted in Figure 1.22.

In the UIS test the active device is turned on in order to charge the inductor up to the current which the device must be tested at. Then, the device is turned off and due to the current continuity in the inductance, the device is forced to operates in avalanche in order to let the inductor to discharge on the device. During this phase, the energy stored in the inductor is dissipated in the device. The test is repeated for increasing value of current and discharging times in order to evaluate the maximum

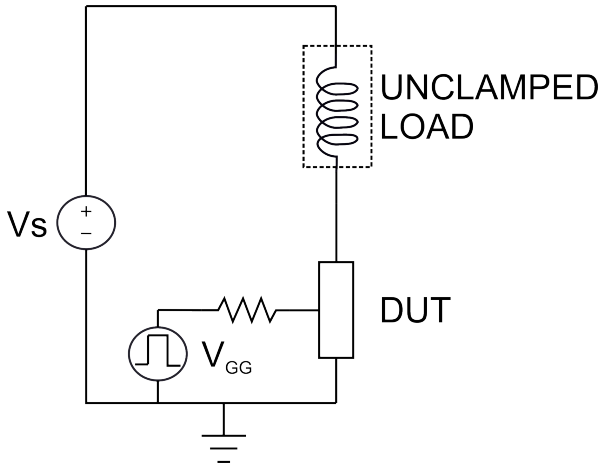


Figure 1.22: Circuit diagram of Unclamped Inductive Switching(UIS) test.

energy that device can sustain in avalanche operation. The amount of the energy is expressed by the following relation:

$$E_{AS} = \frac{L \cdot I_{AV}}{2} \frac{V_{DUT}}{V_{DUT} - V_{DD}} \tag{1.1}$$

The measured energy values depend on the avalanche breakdown voltage, which tends to vary during the discharge period due to the temperature increase. Also note that for low voltage devices $V_{DUT} - V_{DD}$ may become quite small, limiting the use of this circuit since it introduces high-test error. The typical waveform of a UIS test are shown in figure 1.23.

1.4.2 Short Circuit Test

Power devices used in power electronic applications need to be protected from failure under external fault conditions. Such faults mostly result from the occurrence of a short circuit at the load end. As an example, in automotive applications, motor winding insulation failure may cause a fault in the system [40]. Also there is always a threat of wiring misconnections at the motor terminals creating a possibility for the drive output terminals to be short-circuited. As a consequence of the occurrence of a short circuit event, the device current is limited only by its

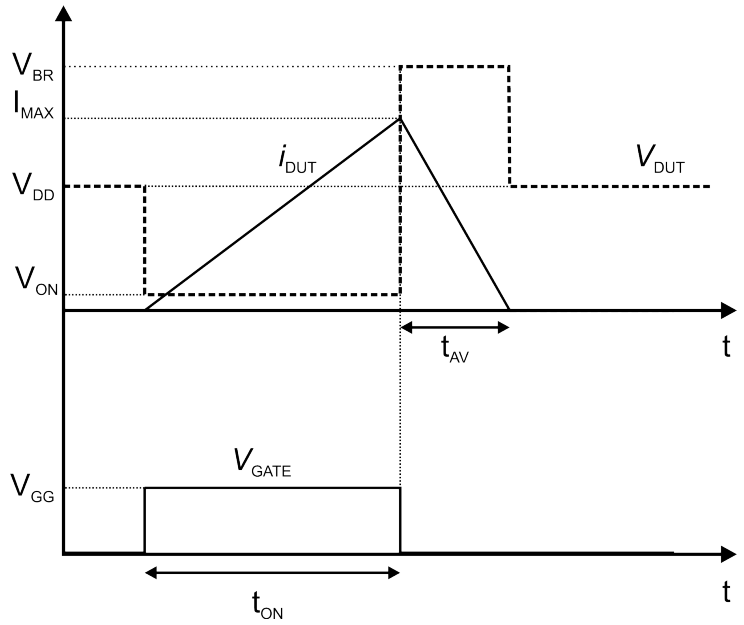


Figure 1.23: Typical waveforms of Unclamped Inductive Switching(UIS) test.

internal resistance and therefore the current flowing in the device itself is very high. Short circuit can happen while the device's normal function and can be divided into two different types [41, 42]. The first is short-circuiting when the device was in on state, which is called "fault under load" and the second is a circumstance where the device turns on under short circuit, which is called "hard switch fault". Fault under load (FUL) is a situation where short-circuit takes place when the device is in on state, so the voltage across the device is low before short circuit. In half bridge configuration, short circuit can happen with a shoot-through when the device on the opposite side turns on while the DUT remains turned on. In the second case, short-circuit is caused when the device is turned on from off state with DC link voltage applied to the device. In such case, di/dt and the value of the fault current are directly proportional to charging speed of the input capacitance.

A test circuit for the short circuit capability of a power device is shown in Figure 1.24.

A voltage is applied from the capacitor, directly on the device under

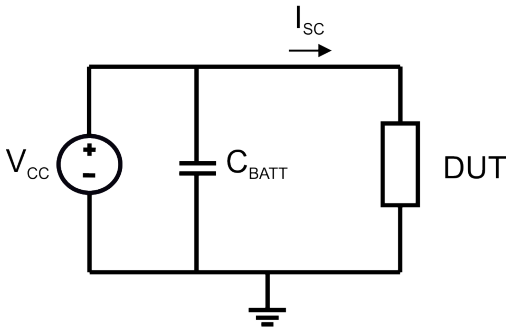


Figure 1.24: Circuit diagram of Short Circuit test.

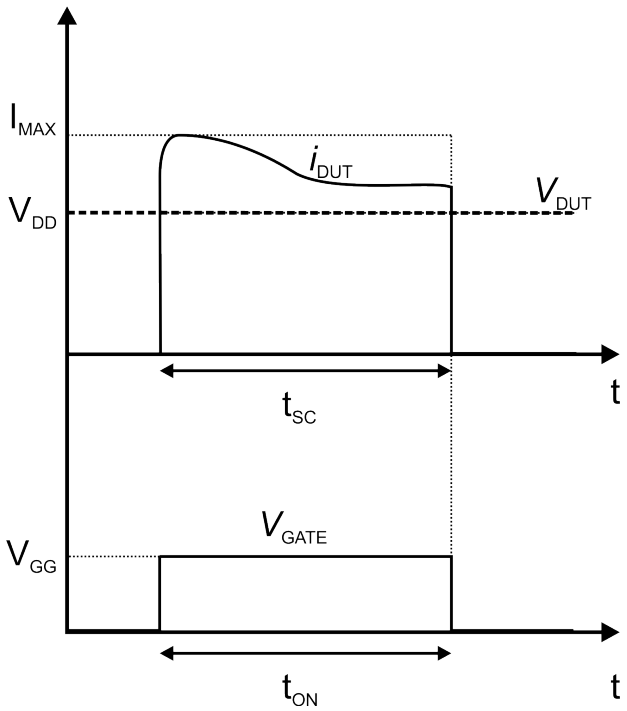


Figure 1.25: Typical Short Circuit test waveforms.

test. A pulse of voltage is applied to the gate and as a consequence the device experiments a pulse of short circuit current. The test is repeated with low rate of repetition ad for increasing duration until the device fails in order to determine the maximum pulse duration, and there-

fore the maximum energy, which the device can sustain in short circuit conditions. Typical waveforms of the short circuit test are shown in Figure 1.25. Typical short circuit pulse duration of IGBTs with respect the saturation voltage is depicted in Figure 1.26 [43].

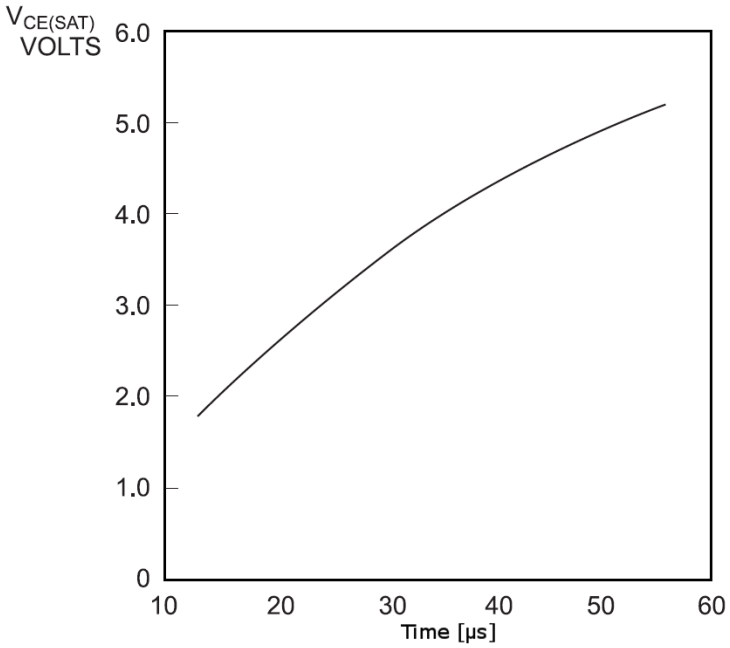


Figure 1.26: Permissible short circuit time for IGBTs vs saturation voltage.

1.5 References

[1] M.E. Alperin et al. "Development of the Self-Aligned Titanium Silicide Process for VLSI Applications". In: *Solid-State Circuits, IEEE Journal of* 20.1 (Feb. 1985), pp. 61–69. ISSN: 0018-9200. DOI: 10.1109/JSSC.1985.1052277.

[2] G Deboy et al. "A new generation of high voltage MOSFETs breaks the limit line of silicon". In: *Electron Devices Meeting, 1998. IEDM'98. Technical Digest., International*. IEEE. 1998, pp. 683–685.

[3] Wataru Saito et al. "Over 1000V semi-superjunction MOSFET with ultra-low on-resistance below the si-limit". In: *Power Semiconductor Devices and ICs, 2005. Proceedings. ISPSD'05. The 17th International Symposium on*. IEEE. 2005, pp. 27–30.

[4] K. Joardar et al. "An improved MOSFET model for circuit simulation". In: *Electron Devices, IEEE Transactions on* 45.1 (Jan. 1998), pp. 134–148. ISSN: 0018-9383. DOI: 10.1109/16.658823.

[5] Fairchild Semiconductor. *MOSFET Basics*. Application Note 9010. 2000.

[6] Cobbold and S.P. Richard. *Theory and Application of Field-Effect-Transistors*. Ed. by John Wiley & Sons. New York, 1970.

[7] B.J. Baliga et al. "The insulated gate rectifier (IGR): A new power switching device". In: *Electron Devices Meeting, 1982 International*. Vol. 28. 1982, pp. 264–267. DOI: 10.1109/IEDM.1982.190269.

[8] H.W. Becke and C.F. Wheatley. *Power MOSFET with an anode region*. US Patent 4,364,073. Dec. 1982.

[9] A. Nakagawa, H. Ohashi, and T. Tsukakoshi. "High voltage bipolar-mode MOSFETs with high current capability". In: *Conference o Solid State Devices and Materials*. 1984.

[10] A. Nakagawa et al. "Experimental and numerical study of non-latch-up bipolar-mode MOSFET characteristics". In: *Electron Devices Meeting, 1985 International*. Vol. 31. 1985, pp. 150–153. DOI: 10.1109/IEDM.1985.190916.

[11] Hideo Iwamoto et al. “A new punch through IGBT having a new N-buffer layer”. In: *Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the 1999 IEEE*. Vol. 1. 1999, 692–699 vol.1. DOI: 10.1109/IAS.1999.800025.

[12] H-R Chang and B.J. Baliga. “500-V n-channel insulated-gate bipolar transistor with a trench gate structure”. In: *Electron Devices, IEEE Transactions on* 36.9 (Sept. 1989), pp. 1824–1829. ISSN: 0018-9383. DOI: 10.1109/16.34248.

[13] M.D. Pocha and R.W. Dutton. “A computer-aided design model for high-voltage double diffused MOS (DMOS) transistors”. In: *Solid-State Circuits, IEEE Journal of* 11.5 (Oct. 1976), pp. 718–726. ISSN: 0018-9200. DOI: 10.1109/JSSC.1976.1050803.

[14] S.C. Sun and James D. Plummer. “Modeling of the on-resistance of LDMOS, VDMOS, and VMOS power transistors”. In: *Electron Devices, IEEE Transactions on* 27.2 (Feb. 1980), pp. 356–367. ISSN: 0018-9383. DOI: 10.1109/T-ED.1980.19868.

[15] R.A. Minasian. “Power MOSFET dynamic large-signal model”. In: *Solid-State and Electron Devices, IEE Proceedings I* 130.2 (Apr. 1983), pp. 73–79. ISSN: 0143-7100. DOI: 10.1049/ip-i-1.1983.0018.

[16] G.M. Dolny, H.R. Ronan Jr., and C.F. Wheatley Jr. “A SPICE II Subcircuit Representation for Power MOSFETs Using Empirical Methods”. In: *The Power Electronics Design Conference Proceedings*. Oct. 1985, pp. 147–153.

[17] H.P. Yee and P.O. Lauritzen. “SPICE models for power MOSFETS: an update”. In: *Applied Power Electronics Conference and Exposition, 1988. APEC’88. Conference Proceedings 1988., Third Annual IEEE*. IEEE. 1988, pp. 281–289.

[18] G.A. Franz et al. “Use of accurate MOS models for optimizing resonant converter designs”. In: *Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE*. Oct. 1990, 1564–1568 vol.2. DOI: 10.1109/IAS.1990.152394.

[19] R. Kraus, P. Turkes, and H.J. Mattausch. "Modelling the self-heating of power devices". In: *Power Semiconductor Devices and ICs, 1992. ISPSD '92. Proceedings of the 4th International Symposium on.* 1992, pp. 124–129. DOI: 10.1109/ISPSD.1992.991248.

[20] F. Morancho et al. "Modelling and performance of vertical trench MOSFET in power electronics". In: *Semiconductor Conference, 1995. CAS'95 Proceedings., 1995 International.* Oct. 1995, pp. 53–56. DOI: 10.1109/SMICND.1995.494862.

[21] K.G.P. Dharmawardana and G. Amaratunga. "Modeling of high current density trench gate MOSFET". In: *Electron Devices, IEEE Transactions on* 47.12 (Dec. 2000), pp. 2420–2428. ISSN: 0018-9383. DOI: 10.1109/16.887031.

[22] P. Rossel et al. "Avalanche characteristics of MOS transistors". In: *Microelectronics, 1997. Proceedings., 1997 21st International Conference on.* Vol. 1. Sept. 1997, 371–381 vol.1. DOI: 10.1109/ICMEL.1997.625274.

[23] Kuang Sheng, Barry W Williams, and Stephen J Finney. "A review of IGBT models". In: *Power Electronics, IEEE Transactions on* 15.6 (2000), pp. 1250–1266.

[24] B.J. Baliga. *Modern power devices.* A Wiley-Interscience publication. Wiley, 1987. ISBN: 9780471819868. URL: http://books.google.it/books?id=5xxTAAAAMAAJ.

[25] Di-Son Kuo, Chenming Hu, and Steven P. Sapp. "An analytical model for the power bipolar-MOS transistor". In: *Solid-State Electronics* 29.12 (1986), pp. 1229 –1237. ISSN: 0038-1101. DOI: http://dx.doi.org/10.1016/0038-1101(86)90128-0. URL: http://www.sciencedirect.com/science/article/pii/0038110186901280.

[26] Allen R. Hefner. "Analytical modeling of device-circuit interactions for the power insulated gate bipolar transistor (IGBT)". In: *Industry Applications, IEEE Transactions on* 26.6 (Nov. 1990), pp. 995–1005. ISSN: 0093-9994. DOI: 10.1109/28.62382.

[27] Allen R. Hefner and D.M. Diebolt. "An experimentally verified IGBT model implemented in the Saber circuit simulator". In: *Power Electronics, IEEE Transactions on* 9.5 (Sept. 1994), pp. 532–542. ISSN: 0885-8993. DOI: 10.1109/63.321038.

[28] R. Kraus and K. Hoffmann. "An analytical model of IGBTs with low emitter efficiency". In: *Power Semiconductor Devices and ICs, 1993. ISPSD '93., Proceedings of the 5th International Symposium on.* May 1993, pp. 30–34. DOI: 10.1109/ISPSD.1993.297102.

[29] F. Udrea and G. Amaratunga. "A unified analytical model for the carrier dynamics in trench insulated gate bipolar transistors (TIGBT)". In: *Power Semiconductor Devices and ICs, 1995. ISPSD '95., Proceedings of the 7th International Symposium on.* May 1995, pp. 190–195. DOI: 10.1109/ISPSD.1995.515033.

[30] Z. Shen and T.P. Chow. "An analytical IGBT model for power circuit simulation". In: *Power Semiconductor Devices and ICs, 1991. ISPSD '91., Proceedings of the 3rd International Symposium on.* Apr. 1991, pp. 79–82. DOI: 10.1109/ISPSD.1991.146071.

[31] Ying-Yu Tzou and Lun-Jun Hsu. "A practical SPICE macro model for the IGBT". In: *Industrial Electronics, Control, and Instrumentation, 1993. Proceedings of the IECON '93., International Conference on.* Nov. 1993, 762–766 vol.2. DOI: 10.1109/IECON.1993.338985.

[32] D. Metzner, T. Vogler, and D. Schroder. "A modular concept for the circuit simulation of bipolar power semiconductors". In: *Power Electronics, IEEE Transactions on* 9.5 (Sept. 1994), pp. 506–513. ISSN: 0885-8993. DOI: 10.1109/63.321036.

[33] Freescale Semiconductor. *Thermal Analysis of Semiconductor Systems.* BASICTHERMALWP/REV.0. 2008.

[34] ON Semiconductor. *Thermal RC Ladder Networks.* Application Note D8221/D. Apr. 2006.

[35] H. Bauer and Robert Bosch. *Automotive Handbook.* Bentley Publishers, 2000. ISBN: 9780837606149. URL: https://books.google.it/books?id=W0dnPwAACAAJ.

[36] International Rectifier. *Power MOSFET Avalanche Design Guidelines*. Application Note AN-1005. 2005.

[37] JEDEC Standard JESD24-10. *SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD*. Electronic Industries Association. 1990.

[38] R.R. Stoltenburg. "Boundary of power-MOSFET, unclamped inductive-switching (UIS), avalanche-current capability". In: *Applied Power Electronics Conference and Exposition, 1989. APEC' 89. Conference Proceedings 1989., Fourth Annual IEEE*. Mar. 1989, pp. 359–364. DOI: 10.1109/APEC.1989.36987.

[39] K. Fischer and K. Shenai. "Dynamics of power MOSFET switching under unclamped inductive loading conditions". In: *Electron Devices, IEEE Transactions on* 43.6 (June 1996), pp. 1007–1015. ISSN: 0018-9383. DOI: 10.1109/16.502137.

[40] R. Chokhawala and G. Castino. "IGBT fault current limiting circuit". In: *Industry Applications Magazine, IEEE* 1.5 (Sept. 1995), pp. 30–35. ISSN: 1077-2618. DOI: 10.1109/2943.407082.

[41] Fairchild semiconductor. *IGBT Basic II*. Application Note 9020. Apr. 2002.

[42] R.S. Chokhawala, J. Catt, and L. Kiraly. "A discussion on IGBT short-circuit behavior and fault protection schemes". In: *Industry Applications, IEEE Transactions on* 31.2 (Mar. 1995), pp. 256–263. ISSN: 0093-9994. DOI: 10.1109/28.370271.

[43] Internatuional Rectifier. *Protecting IGBTs Against Short Circuit*. Application Note 984.

Chapter 2: Simulation Analyses of Power Semiconductor Devices and Systems

Simulations of power electronic devices and systems have become mandatory in modern industrial applications. The possibility to evaluate the performances of a device before the manufacturing process has significantly reduced the manufacturing costs. What is more, the simulations environments gives the possibility to investigate the causes of failures and to analyse the degradation of the performances produced by the ageing of the devices.

In this chapter different approaches, presented in scientific literature, for device simulations will be briefly introduced, underlining both upsides and downsides, and explaining the best applications they are optimized for.

In the first part, a novel electrothermal simulator for wide area power devices has been implemented for the analysis of avalanche condition of power devices. The simulator environment will be presented and it will be used for the avalanche simulations of a Trench-IGBT device, with particular focus on the understanding the stability and instability that the device experiments when avalanche breakdown occurs into a device, and their effect on to the reliability.

In the second part, effect of instabilities of short circuit operations will be addressed. For the purpose, a second electrothermal simulation environment, oriented to simulate general applications and different devices, has been developed, whose structure will be described as well. The proposed simulator will be used for the simulation of low voltage Power MOSFETs for automotive applications. These simulation aim to accurately reproduce the failures experimented by devices in order to predict

or to overcome in the design phase the arise of these failures. As a consequence, results provided by short circuit simulations will be validated by comparison with experimental data provided by electrical and thermal measurements.

2.1 Common methods of Power Device and System Simulations

2.1.1 Simulation Program with Integrated Circuit Emphasis (SPICE)

Simulations by means of compact models can be implemented with many simulating languages. The most common approach is to implement the model by means of SPICE simulation [1]. A Simulation performed in SPICE makes use of equivalent and compact models for describing the complex, non-linear behaviour of the semiconductor devices, and this simplifies the solution of the circuits. As a consequence, SPICE simulations requires generally low computational efforts, therefore they represents the best option where time and calculation resources are the major constraints, for example in a designing phase where repetitive simulations must be performed by changing geometrical and/or electrical parameters.
SPICE is a program developed at Berkeley University of California in 1970. First version of the program, known as SPICE1 was announced in 1973 [2] as a developed and upgraded version of the previous tool, named CANCER (Computer Analysis of Nonlinear Circuit Excluding Radiations) [3]. The main characteristic of the first SPICE version was the implementation of the Gummel and Poon's model of Bipolar Transistors [4]. In the following years, the diffusion of SPICE grew rapidly and a second version of the program, SPICE2, was presented in 1975 [5, 6]. The second version of the program soon became very diffused in the university and industry. SPICE2 simulator implements a modified version of the Node Analysis [7]. In 1989, the third version of SPICE was developed. Modern version of SPICE has strong numerical convergence capability and provides advanced model for the description of the semiconductor devices behaviour. In addition, the possibility to implement analytical function largely increased the possibility of the SPICE simulations to reproduce the complicated physic mechanisms which govern the operation of semiconductor device. In parallel to the development of the

original program, several commercial version have been produced during the years, among which the most noticeable are PSPICE, oriented to simulation of power devices, and ELDO, which is diffused especially for simulation of integrated circuit. Most of the efforts of the commercial software has been spent in development of friendly graphic interface for creating schematic and analysing the results.

Since its first appearance, SPICE was used for simulation of VLSI circuits [8–10], analog circuit [11, 12], and power circuit as well [13–15]. The usage of the SPICE simulation have been extended, during the years, to thermal simulation also [16–18], overtaking the basic feature of the first SPICE versions which did not account for changing the temperature of the simulations. The implementation of temperature simulation was the first step for the electrothermal simulations to be performed in SPICE.

During the 1970s a lot of works had been published on device level simulations of power semiconductor devices. The idea at the basis of these simulations was to extend the SPICE upsides for replicating the behaviour of power devices. The basic descriptions of signal devices already present in SPICE at that period were insufficient for describing the characteristics of power devices. Large area and increased dimensions are in fact responsible of additional phenomena which are either not correctly described or not present at all in the signal device. First works of Silicon Controlled Rectifiers device simulations appeared between late '70s and early '80s [19–21] and from the same years the first models for simulations of Power MOSFET and Power Diodes are dated [22, 23]. In late 80's the device levels simulation slowly extended to all power devices [24, 25]. All these models were basically one dimensional, that is the description of the device neglects the lateral interactions of charges and electric field. Two dimensional models were developed only in recent years [26] but the complicated description makes them hard to converge. The limitation of the 2D simulations has been partially overcome by the introduction of multicellular description of the device [27, 28], where the device is subdivided into an assigned number of individual sub-device, each representing a single macrocell of the multicellular device. The multicellular approach accounts for the occurrence of non uniform current/temperature distributions across the device but the lateral interplay between the elementary cells develops between the external terminals of each 1D sub-device. For this reason, the multicellular description does not actually account for the internal lateral coupling of the device which

is still a big issue to overcome at all. Provided this, the SPICE simulators are nowadays largely diffused for simulations of large area power devices with hundreds of cell. The diffusion of multicellular simulations have increased the interest for accounting on the physic of the interactions between thermal and electrical phenomena. The electrothermal effects, in fact, are essential for describing correctly the operations of power devices where the self heating is not negligible and, what is more, where the large geometry can produce non uniform temperature distribution in the structure. Electrothermal simulation have been first presented in the 90's when the first models included temperature dependent electrical parameters [29, 30]. These models were used to extend the multicellular approach for electrothermal simulations [31, 32]. In order to describe the thermal behaviour of a power device, compact models presented in 1.3.3 can be used. Electrothermal multicellular simulations represent the state of the art of simulations at device level.

Recent contribution of d'Alessandro et al. [33] presents a 3D simulation of Unclamped Inductive Switching test of IGBTs. Here, the 3-D simulation strategy accounts for electrothermal effects and is based on a multicellular circuit representation of the whole device under test. Each subdevice is modelled with a subcircuit, which, besides the conventional, purely electrical, terminals, is equipped with a temperature (input) and a power (output) node, and includes a transistor macromodel that is based on a standard device as a basic element, and additional parts to account for the temperature dependence of the key parameters and to describe specific physical mechanisms. In particular, the model is based on to the IGBT model proposed by Kraus et al. [34] with modifications for taken into account the avalanche multiplication dependence on the temperature. The device thermal behaviour is modelled by means of Foster RC ladder with as many junction thermal nodes as the number of the electrical sub-devices. Current sources connected to each junction node account for the power generation of the cells. This approach was developed to perform fully coupled dynamic electrothermal simulations inside SPICE. In figure 2.1 is depicted a schematic representation of the simulation method.

A more recent contribution is based on the same approach [35]. Here, a SPICE based electrothermal simulation of Power MOSFET is performed either in short circuit and in UIS in order to evaluate the ageing effect of the metal connections on the device performances. Different from

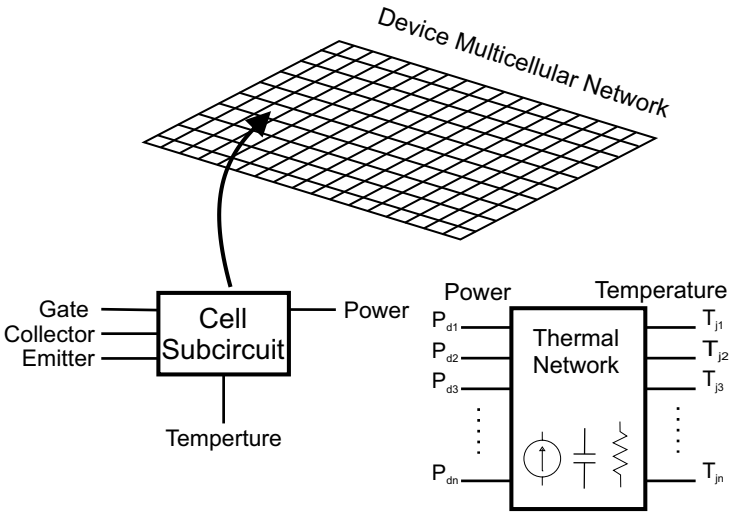


Figure 2.1: Schematic representation of a SPICE electrothermal simulation.

the previous work, the thermal network is realized by implementing a numerical solver of the heat transfer equation by means of finite differences methods (FDM) [36, 37]. This approach has the upside to avoid the preprocessing stage needed for calibrate the thermal network, which is required if the Foster or Cauer network is used. On the other hand, with this tool only simple geometries (e.g. rectangular, slices structures) can be simulated.

2.1.2 Device Simulation by means of Finite Elements Method (FEM)

The Finite Element Method (FEM) is a numerical technique, developed in the early '40s, which let to obtain the solution of differential equations in general-shaped domains [38, 39]. Despite to its early development, the first FEM analyses applied to the electronic field are dated in late '70s [40–42]. Since its first applications, FEM simulations usage has been grew more and more throughout the years because of its upsides. From a mathematical point of view, the main advantage of the FEM methods is that, even by using a very coarse mesh, the conservation of the charge is always valid in each point of the domain. Other important upsides are that it is easy to treat complicated, irregular geometries, and higher

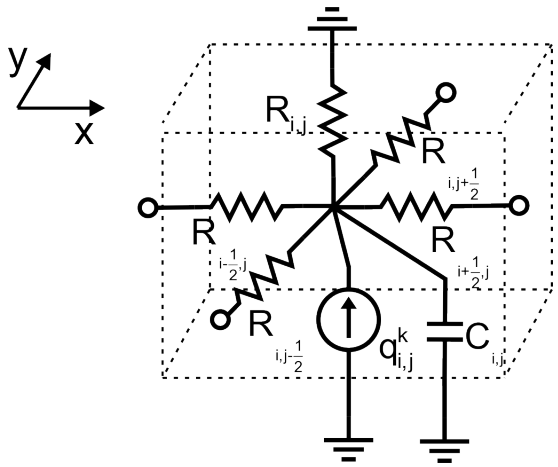


Figure 2.2: Equivalent circuit of the thermal model by means of FDM.

order approximations are more readily constructed [43]. Implementations of computational mesh, which can be locally refined in dimensions in order to achieve a better resolutions in regions of rapid change, is easier to implement than in finite difference methods [44]. The rapid grows of FEM simulation led to the implementation of tools dedicated to the development and analysis of semiconductor devices. This simulation environments are commonly referred to Tecnhology Computer Aided Design (TCAD). The predictive capability of TCAD simulators is well proved in CMOS and VLSI systems [45, 46] as well as in power semiconductor devices field [47, 48] and for this reason they are used by most of the semiconductor companies, in the different technology steps of the development cycle, and for academic purposes as well. Several commercial TCAD tools are currently available, as an example, Synopsys TCAD commercial tool suite (formerly ISE tools) [49] and ATLAS by SILVACO [50] are among the most diffused. The analyses conducted by means of TCAD simulators have been spread to large area devices only in late '80s because the specific behaviour of power semiconductor devices, requires very sophisticated methods to guarantee successful simulation [51, 52]. The first simulation have been applied to the description of a single cell of a device, and using an *area factor* parameter to extend the results to an equivalent large area device [53–55]. Due to the progress of the computer calculation capabilities, the FEM simulation have been successively extended to multicellular simulations [56,

57].

2.1.3 Mixed Mode Simulations

Mixed mode circuit simulations are generally referred as simulation which mixes the compact description of SPICE models with the numerical solutions of the physic by means of FEM solvers. Numerical analyses can be conducted for example to solve the equation of a devices while the rest of the circuit, where the devices is simulated into, is simulated by normal SPICE models [58, 59]. Early work in of Franz [60] and Michelet [61] conducted mixed mode simulations using SPICE in combination with behavioural or piecewise-linear description based simulator. In 1994, a review presented by Kang et al. [62] stated that the approaches based on two different simulators would have been overtaken by simulations implemented in a single tool because of the less computation efforts required. However, both the method are nowadays diffused due to the upgrading of the computer calculation capabilities.
As long as two separate programs are used for the simulations, the coupling of the programs develops in such a way that the device and circuit equations are handled subsequently. The first tool provide solution for the second program and vice versa, in iterative way. This approach is also referred in literature as *two-level Newton* algorithm or decoupled methods [63, 64]. The upside of this algorithm lays on the usage of two different tools, that is device simulation and circuit simulation, working separately, and therefore the best tool for each simulation can be chosen. From a pure mathematical aspect, the two-level Newton algorithm is the best option for the simulation of DC point [63]. A second approach for the mixed mode simulations consists on to incorporate the device and circuit equation into one single equation system. This approach is usually called *full-Newton* algorithm [65, 66] or fully coupled method. The advantage of the fully-coupled method lays on the better performances in the transient analyses [63]. What is more, the inclusion of all the equations in a unique system gives the simulation a better capability to solve problems with high grade of correlations, that is, where the coupling between the simulators is very strong [67].
When it comes to electrothermal simulations, the two approaches explained above can be applied to electrical and thermal simulations. That is, the two-level Newton method is used when a separate analysis (i.e. with separate tools) must be conducted. In this case a Finite Element

Method solver can be used for the thermal analysis in order to achieve a better description of the complicated geometries of a power device structure as well as to obtain accurate solutions. What is more, by describing a geometry with FEM solvers it is easy to change position and dimensions of all geometry-related features of a device and the model is then ready to be simulated. This is not true for the compact R-C network that require time-consuming preprocessing stages every time the geometry is changed (see 1.3.3). Another approach, based on analytical solution of the thermal equations, using Fourier Series decomposition, has been proposed which combine low computation efforts with reasonable accuracy [68, 69]. The drawback of this method is that the description of unheated parts is lack of accuracy for high speed thermal transients [70, 71].
An electrothermal simulation performed with fully coupled method, on the other hand, is preferred for one-tool simulations with high grade of coupling. As an example, in the fully coupled approach, if the simulations is conducted with SPICE programs, then the thermal simulation must be conducted by means of SPICE thermal equivalent network (see 2.1.1). Same happens if a device simulation is conducted.

2.2 Simulation of Power Devices in Avalanche Operation

2.2.1 Physics of The Avalanche Phenomenon

The IGBT are widely used in switching applications where the avalanche phenomenon can occur and an higher robustness of the active silicon power devices is requested. The avalanche breakdown phenomenon has been studied since the beginning of the silicon device development. Great effort has been given to the physical mechanisms which lead to the presence of Negative Differential Resistance (NDR) in the blocking I-V curves of different families of semiconductor devices. The subject has been investigated by means of both the analytical, experimental and simulative point of view.

When the electric field of a reversely biased p/n junction reaches the critical value, the impact ionization generation phenomenon occurs in a reduced layer of the depletion region and the voltage drop at which this happens is called Breakdown Voltage [72]. The avalanche breakdown operation is generally considered stable either from electrical and thermal point of view. In more detail, the effect of a rise of temperature produces an increases of the breakdown voltage. As a consequence, if the current distribution is not uniform along the device (this can be particularly true for large area devices) the consequent temperature unevenness acts as a balancing mechanism which leads the current to spread out uniformly. Despite of the supposed stability of the phenomenon, experimental evidences as well as theoretical studies report that devices can show instability effects during avalanche breakdown [73, 74]. The analyses conducted on devices, experimenting such instabilities, have shown the presence of a Negative Differential Resistance (NDR) behaviour for a finite range of current densities [75]. It has been theoretically shown by means of thermodynamic principles that, when a generic structure exhibits a NDR region into the I-V curve in current-controlled conditions, the current becomes inhomogeneous in planes orthogonal to the current flow direction [76]. The phenomenon is likely to happen in bipolar devices, particularly in IGBTs and other four layer devices (e.g. thyristors, GTOs, etc.), when the concentration of the charges, generated by avalanche multiplication, is larger enough to produce a modification of the electric field profile [77]. The instability of operations in NDR regions can be explained from a more physical point of view in this way: starting from an uniform distribution of the current at a current density

value in the range of the NDR region, a infinitesimal local increase of the current causes an infinitesimal reduction of the local voltage. This phenomenon is explained graphically in Figure 2.3. The local reduction of the voltage drop causes the attraction of the neighbouring carriers with the relative increase of the current. The positive feedback finally turns into focalization of the current. Being the NDR positive feedback concurrent with the negative feedback produced by temperature increase, the focusing of the current does not lead always to the premature destruction of the device since the temperature effect leads to the filament movement in colder regions, as demonstrated in [78, 79].

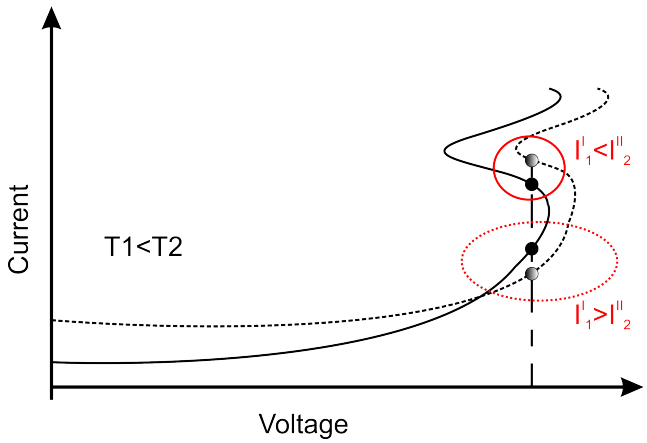


Figure 2.3: Thermal Instability of NDR part of an avalanche characteristic.

2.2.2 Simulation of Avalanche Operation

The analyses of a large area device which experiments the avalanche breakdown can be conducted by means of experiments (see 1.4.1) or by simulations. For what concerns the simulations, the most accurate results are obtained by using TCAD simulations and, in fact, a lot of TCAD simulations have been conducted on power devices operating in avalanche [78, 80]. The limit of a TCAD simulations, however, is that, apart from specific structures with high level of symmetry, the simulation cannot be easily conducted in 3D and also the area which can be simulated is limited.

In order to evaluate the global effects of avalanche breakdown on an entire device different approaches are therefore needed, which loose accuracy in favour of the dimension of the simulated domain. These approaches are mainly implemented with compact electrical models in order to describe the occurrence of avalanche multiplication with simpler expressions. The simulation can be conducted by using numerical models [81], SPICE simulators [33] (as already mentioned in 2.1.1), or in mixed mode [82].

2.2.3 A Novel 3D electrothermal simulator for wide area power devices operating in avalanche condition Da modificare

A novel simulator has been developed for studying the electrothermal effect of the power device large area on to the reliability in avalanche conditions [83]. The simulator has been implemented with a mixed-mode iterative approach. The electrical part of the simulation is implemented in $MATLAB^{®}$ language [84] whilst the thermal simulation is conducted with a FEM solver, namely $COMSOL^{®}$ Multyphysics [85]. As already pointed out in 2.1.3, the Finite Element Method guarantees an accurate reproduction of the thermal behaviour of complicated structures.
In order to reproduce electrothermal avalanche transients, a description of the electrical and thermal environment is required.

Implementation of the electrical simulator The electrical circuit that must be simulated is the one for performing UIS test (see 36). The solution of an electrical circuit can be obtained, numerically, by means of different algorithm. Among the others, Modified Nodal Approach (MNA) has generally recognized as a very flexible and easy-implementing approach for the numeric solution of electrical network and in addition it has the noticeable upside to yield to well-behaved numerical diagonal matrices that are easy to handle with low computational efforts [86]. The final goal of this method is the solution of the following, linear expression:

$$\begin{bmatrix} Y_R & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} \underline{V} \\ \underline{I} \end{bmatrix} = \begin{bmatrix} \underline{J} \\ \underline{F} \end{bmatrix} \tag{2.2}$$

The vector of the unknowns is composed by the term $\underline{\mathrm{V}}$, which is in turn composed by all the nodes potential, whilst $\underline{\mathrm{I}}$ considers the unknown cur-

rents which flow in the branches of the electrical network that contain voltage sources and other elements whose current is the controlling variable.
The term Y_R represents the admittance matrix for the branches that don't contain voltage sources, current controlling elements, etc.; it is essentially the basic matrix which is used in the simple Nodal Approach. The term B is referred to the additional branches and in particular represents the derivative of each unknown current with respect the vector of unknown currents and therefore it contains ± 1's for the elements whose branch relations are introduced. Terms C and D represents the derivative of the branch constitutive relations with respect to the vector of the unknowns. Finally, the terms $\underline{\mathrm{J}}$ and $\underline{\mathrm{F}}$ are the circuit excitations which includes the external excitations and the virtual excitations obtained by the linearisation of the capacitors and inductors.
In order to clarify the process, the MNA is applied to the simple circuit in Figure 2.4.

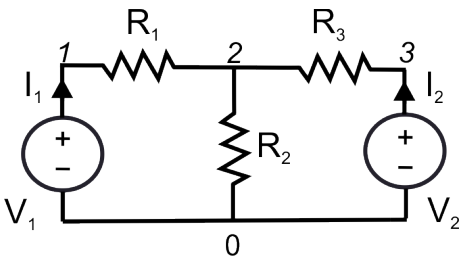


Figure 2.4: Simple circuit for the Modified Node Analysis explanation.

By applying Kirchhoff's current law to the three circuit nodes, and considering positive the current which flows out from the node, it follows:

$$\begin{cases} u_1 G_1 - u_2 G_1 - I_1 & = & 0 \\ -u_1 G_1 + u_2 (G_1 + G_2 + G_3) - u_3 G_3 & = & 0 \\ -u_2 G_3 + u_3 G_3 - I_2 & = & 0 \\ u_1 & = & V_1 \\ u_3 & = & V_2 \end{cases} \tag{2.3}$$

where $u_1 ... u_3$ are the unknown potentials. The overall vector of unknowns considers also the currents I_1 and I_2 that must be calculated as well. By looking at the system, and in particular at the Left Hand Side of the equations, one can write the MNA matrix components as

expressed by the following equations:

$$Y_R = \frac{\partial LHS_{1..3}}{\partial u_{1..3}} \quad and \quad B = \frac{\partial LHS_{1..3}}{\partial I_{1,2}}, \tag{2.4}$$

for the first three rows, and, for the last two rows:

$$C = \frac{\partial LHS_{4,5}}{\partial u_{1..3}} \quad and \quad D = \frac{\partial LHS_{4,5}}{\partial I_{1,2}}. \tag{2.5}$$

From these relations, the MNA matrix can be calculated. The equations for the network in Figure 2.4 can be then rearranged in a matrix form:

$$\left[\begin{array}{ccc:cc} G_1 & -G_1 & 0 & -1 & 0 \\ -G_1 & G_1+G_2+G_3 & -G3 & 0 & 0 \\ 0 & -G_3 & G_3 & 0 & -1 \\ \hdashline 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{array}\right] \left[\begin{array}{c} u_1 \\ u_2 \\ u_3 \\ I_1 \\ I_2 \end{array}\right] = \left[\begin{array}{c} 0 \\ 0 \\ 0 \\ V_1 \\ V_2 \end{array}\right]. \tag{2.6}$$

The matrix in 2.6 has a sparse looking and it is the more prominent the larger are the nodes of the circuit. The sparsity is a very good property for numerical resolutions as a sparse matrix reduces significantly the computational requirements. The circuit which has been considered so far doesn't contain dynamic elements like inductors and capacitors. This elements have a time-differential constitutive relation and for this reason cannot be directly handled by the MNA, but a time discretization is required in order to derive an equivalent circuit for each element. The most used methods for handling with dynamic elements are Euler Method (either Backward or Forward) [87], Trapezoidal [88] and Gear Method [89]. By using the Backward Euler Method, as it is assumed to be the most stable, the capacitor equation is represented in terms of an implicit integration scheme as:

$$i(t_n) = C\frac{v(t_n) - v(t_{n-1})}{h}, \tag{2.7}$$

where $h = t_n - t_{n-1}$ is the time step, and $v(t_{n-1})$ is the capacitance voltage at previous time point. Equation 2.7 can thus be represented by a conductance of $\frac{C}{h}$ in parallel with a current source $C\frac{v(t_{n-1})}{h}$. For the inductance, a complementary representation holds, with the series

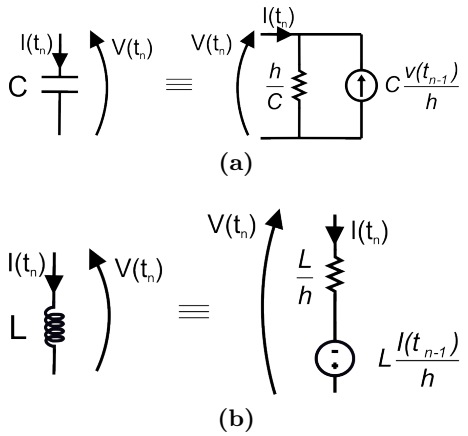


Figure 2.5: Backward Euler equivalent circuit of: a) Capacitor; b) Inductor.

of a conductance of $\frac{h}{L}$ and a voltage source of $L\frac{I(t_{n-1})}{h}$, where $i(t_{n-1})$ is the inductor current at the previous time point.
With the Backward Euler method, as a consequence, the dynamic elements are converted in elements which can be included straightforward in the MNA.
At this stage, the device electrical implementation has not be considered so far. One possibility is to use a compact model to reproduce the electrical behaviour of a power device. However, if one is interested in simulate only the avalanche behaviour of the device and the effect of the temperature, a useful and easier solution is to represent the device as a bipole whose I-V relation reproduces the non linear I-V static blocking characteristic of the device itself; the thermal dependence is included by considering curves at different temperatures. In this case, the description of the behaviour of the device is essentially static, and its current (voltage) is completely determined by its voltage (current) and temperature. In order to take into account the spatial effects, which play a major role in the instability in avalanche operations, the device has been divided in a parallel of sub-devices, according to the multicellular concept [90]. The schematic representation of multicellular structure is depicted in the Figure 2.6. How it is shown in the picture, the connection between each sub-device is guaranteed by resistors which represent the resistance of the metal interconnection.

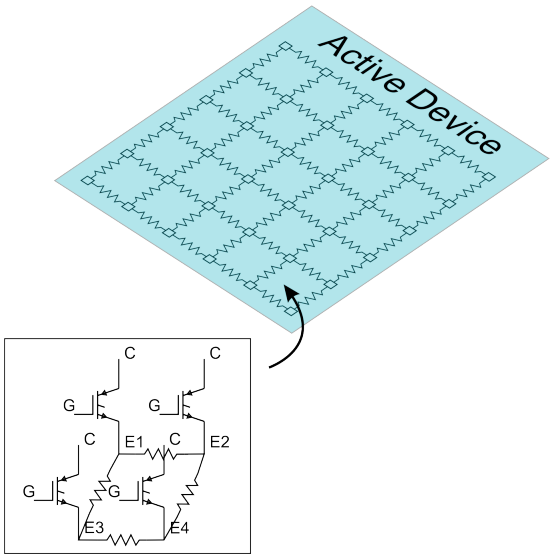


Figure 2.6: Schematic representation of a multicellular IGBT device.

The solution of the electrical circuit must consider the non linearity of the bipoles the device is composed of. By considering a single, non linear bipole, the iterative Newton-Raphson method has been used to linearise the problem. The basic operation of an iterative linearisation algorithm is to find a linear representation of the problem at each iterative step, and, when passing from one step to the following, to find a better approximations for the solution [91]. Like for all iterative algorithms, a proper convergence criterion must be set according to the required precision of the solution. In the following, a description of the Newton-Rhapson method is provided, by applying it to the simple circuit shown in Figure 2.7a.
The diode I-V expression can be seen either as function of the voltage and function of the current. Here, the function $V = f(I)$ is considered. From this position, and considering the circuit in Figure 2.7a, it follows:

$$V_D = f(I_D) = R(I_A - I_D). \tag{2.8}$$

Hence, the purpose of the algorithm is to find the value of I_D that solves the equation 2.8. At this purpose, the first order Taylor's series development of the function f around an arbitrary base current I_{D0} is considered:

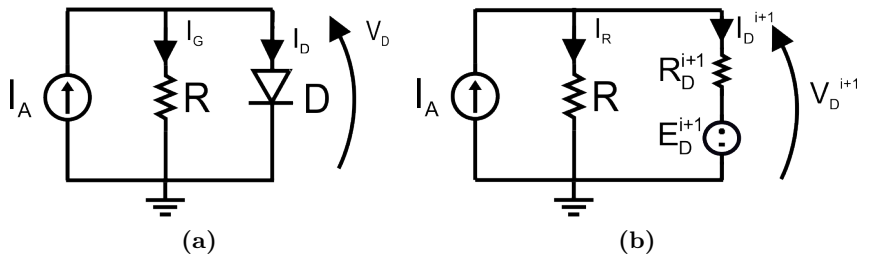


Figure 2.7: a) Reference circuit; b) Equivalent according to Newton-Raphson method

$$V_D = f(I_D) = f(I_{D0}) + (\frac{\partial f}{\partial I}(I_{D0}))(I_D - I_{D0}) = \\ V_{D0} + R^{'}(I_{D0})(I_D - I_{D0}), \tag{2.9}$$

where $R^{'}$ is the differential resistance of the curve V-I at I_{D0}. By substituting 2.9 in 2.8, the solving equation becomes:

$$R(I_A - I_D) = V_{D0} + R^{'}(I_{D0})(I_D - I_{D0}). \tag{2.10}$$

Because of the approximation, the solution I_D of the above equation will be different from the actual solution, and it becomes the new trial operating point for the diode. As a consequence, the iterative process becomes:

$$R(I_A - I_D^{i+1}) = V_D^{i+1} = V_D^i + R^{'}(I_D^i)(I_D^{i+1} - I_D^i). \tag{2.11}$$

The expression 2.11 can be represented in a circuit as the series of a resistance of $R_D^{i+1} = R^{'}(I_D^i)$ and a voltage source of $E_D^{i+1} = V_D^i - R^{'}(I_D^i)(I_D^i)$. The equivalent circuit representation is depicted in Figure 2.7b.
As reported in literature, the NR method converges to the roots in a quadratic manner [92]. However, the convergence is not always guaranteed. For example, the algorithm oscillates around the solution if the non linear function has a discontinue derivative and the initial guess point if far from the solution. This is, as example, the case for a typical IGBT S-shaped blocking characteristic with both PDR and NDR regions. Modifications of the basic Newton-Raphson algorithm has been

proposed in order to overcome this issue [93]. However, in case of non monotonic functions, another problem occurs that can harms the convergence trend of the algorithm. In order to show this problem, the circuit constituted by the parallel of two non-linear bipoles which share the same characteristic is considered, as shown in Figure 2.8a. In this case, by neglecting all the parasitic elements, the two bipoles must have the same voltage drop.

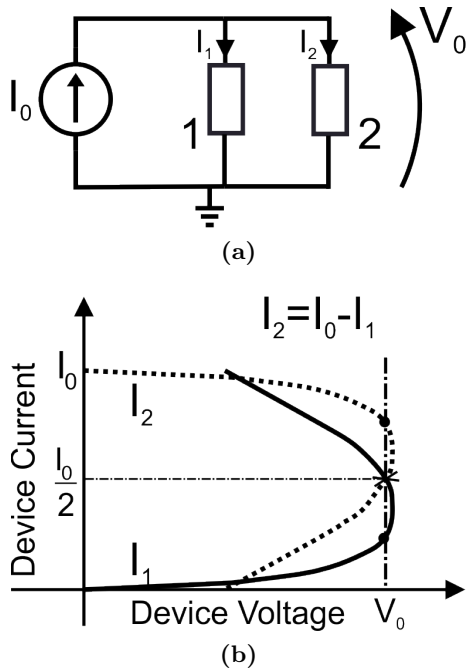


Figure 2.8: a) Example of multi-solutions circuit; b) Graphical solutions.

When a current is forced to flow, for example by the inductance during a UIS test, it must be shared among the two devices. One can assume that the current will equally distribute among the bipoles, but, as shown in the Figure 2.8b, when the I-V characteristic present opposite trends, another solution is possible when one device brings the most of the current, that is, the current flows not uniformly. If the two bipoles are seen as the sub-devices of a multicellular description, it follows that the current is actually shrink in half a part of the device. It is important to underline, however, that this uncertainty of the solution is because

a static analysis has been conducted. A unique solution is guaranteed if the guess initial point is near to the actual solution and, also, if the dynamic of the system is taken into account, that is, the current working point must be in the vicinity of the point at the previous simulated time. The equivalent network representation of the UIS circuit, by means of MNA and NR method, is shown in Figure 2.9. Here, also the output capacitance of the device is included, as it dictates the rate of changes of the voltage across the device.

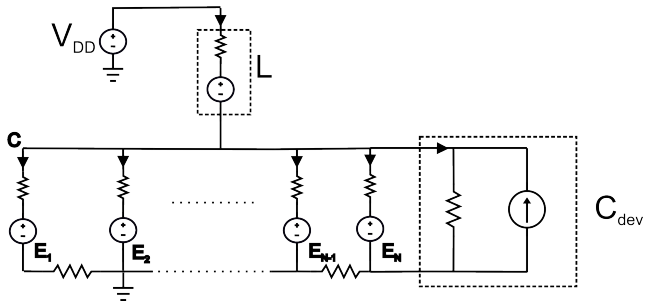


Figure 2.9: Schematic representation of a multicellular IGBT device.

Implementation of the Thermal Simulator The choice to make use of a FEM approach for the thermal simulation simplifies a lot the design and implementation of the thermal solver. The geometrical structure can be designed directly in the FEM graphical interface or by means of script, in order to recall the real structure. In order to couple COMSOL and MATLAB, the LiveLink feature of the COMSOL program has been used. LiveLink are a set of Matlab functions specifically designed for the communication between the programs. With this functions, all the functionalities of COMSOL can be governed by MATLAB. Heat source in the device can be represented as a surface source (2D approach) or as a volume one (3D approach). In the first case, heat power, evaluated by the electrical solver, is considered to be generated in a surface. In the second case volume heat power is obtained as a linearly distributed 3D profile. For avalanche simulations, where the heat dissipation is developed in all the low doped region, that is where the high electric field develops, a 3D power source produces the most accurate results [94]. What is more, the profile of the heat generation is not constant in the vertical direction having the electric field a linear trend. As

a consequence, the power dissipation is linearly decreasing in the vertical dimension.

Thermal simulator is implemented to be independent from the electrical one. It means that each simulator can have either the same or a different mesh. This provides the choice of the best meshing method according to the problem requirements, and the solution is very effective for a FEM software which generally has a powerful meshing engine. In particular, 3-D geometries are generally meshed with tetrahedral elements, in order to minimize computational time [95]. However, additional features can be used to combine different meshes algorithm for different part of the device structure.

Implementation of the time-step control Time dependent simulations are performed with discretization of the time variable so that a static problem is solved at each instant. The step which dictates the developing of the simulation along the time is a paramount variable and it needs careful attention to be defined. In particular, for the electrical simulation analysed in 2.2.3, the time step appears explicitly in the components which reproduces the behaviour of capacitances and inductances. What is more, the time step influences also the static convergence. In fact, the iterative Newton-Raphson algorithm that solves the non linearity has the most chances of rapid convergence if the initial guess point is near to the solution. As the guess point is generally taken as the point of the previous time, it is important that the step is not such large that the variation is too high. The requirements for a smooth convergence of the electrical problem, lead therefore to a small time step. However, a too small time step means to solve the overall system in a large number of time points and this would negatively affect the computational efforts. A trade-off is demanded in order to achieve ease of convergence with reasonable computational times. Generally, the time step is changed during the simulation according to the gradient of the potentials and the current, by definition of highest limits for the rate of change. In SPICE, for example, the time step is evaluated at every simulation point according to either second order of currents and voltages derivative or third order of derivative, according to the particular time integration method used [96].

In the electrothermal avalanche simulations scenario, also the thermal physic plays a not negligible role. Besides the normal conditions, where

the temperature dynamic is much slower than the electrical evolution, and therefore the time step is dictated only by the velocity of electrical processes, in avalanche operations there is a strong electrothermal coupling, being the avalanche phenomenon strongly dependent on the temperature. For this reason, the correlation among the electrical problem and the thermal problem must be considered as well in the determination of the suitable time step. In order to consider the electrical requirements and to comply with electrothermal interactions, a dedicate time step algorithm has been implemented. The algorithm is based on a simple guess and try prediction approach, that is, starting from an initial time step, the subsequent step is controlled by the convergence of the current point simulation.

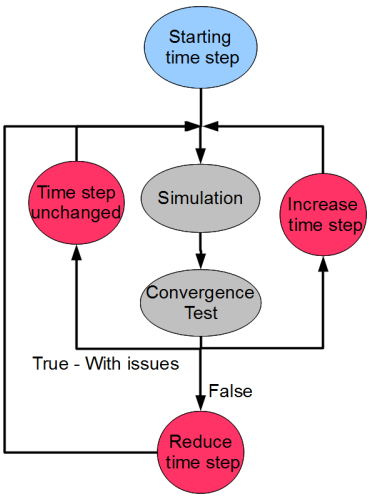


Figure 2.10: Algorithm for the calculation of time step.

More in detail, if the simulation runs smoothly then the next time step is increased of a factor α_1; if the convergence is achieved, but with a number of electrothermal iterations higher then a value M_{iter}, the next time step is equal to the current step; finally, if the current simulation does not converge, starting from the last successfully computed point, simulation is performed at a new time but with a step reduced of a factor α_2. Parameters α_1, $alpha_2$, and the maximum number of iterations M_{iter} can be properly tuned for the particular simulation. A schematic representation of the control algorithm of the time step is depicted in Figure 2.10.

The Complete Simulation Environment The representation of the complete simulator concept is reported in Figure 2.11.

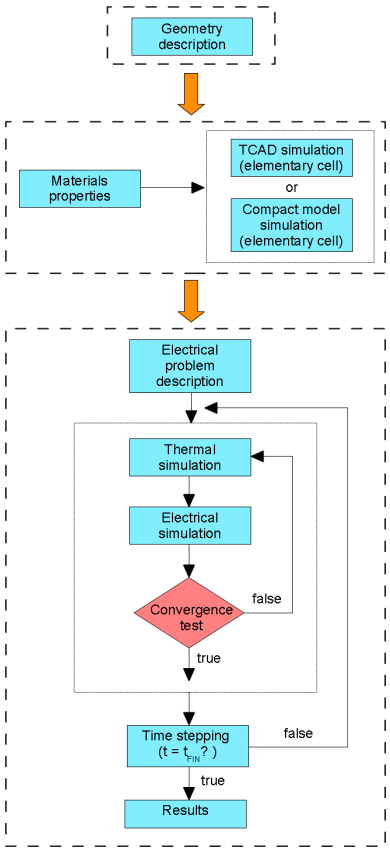


Figure 2.11: 3D electro-thermal simulator scheme.

2.2.4 Simulation of thermal stability of IGBTs during UIS test

The analysis of the stability during avalanche operations is carried out on IGBTs by means of the electrothermal simulator described in the previous section. For the purpose, a 900V Trench-IGBT with an area of about $1\,\mathrm{cm}^2$ is considered. The electrical description of the device is included in the static blocking I-V characteristics provided by TCAD simulations, in a temperature range that goes from 300 K to 450 K. These

characteristics are depicted in Figure 2.12 scaled in A cm^{-2}. Up to about 30 A cm there is a weak positive differential resistance (PDR) in the I–V curves followed by a snap-back point where the differential resistance becomes negative (NDR). At very high current another snap-back point is present before the device enters in the latch-up current region.

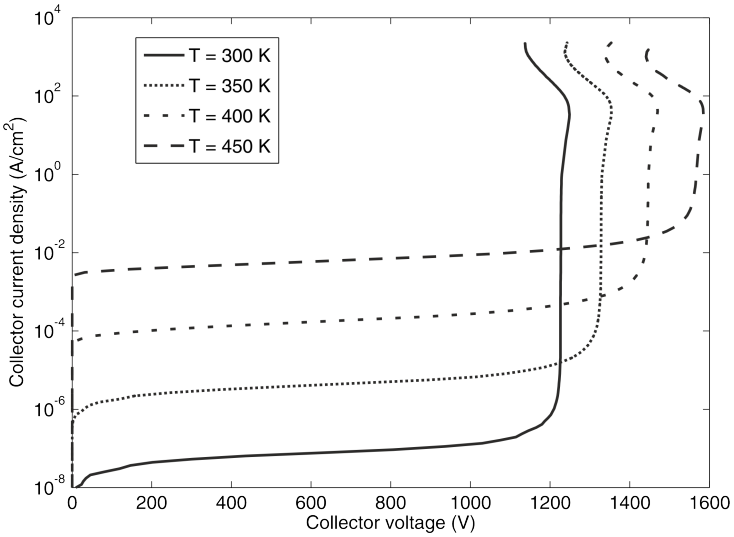


Figure 2.12: Static blocking characteristics of the considered Trench IGBT.

The real structure of the device has been replicated for the thermal simulation to be performed onto. In particular geometry is schematically depicted in Figure 2.13 and consists on a four layer parallelepiped which represents the devices, laying on an aluminium–ceramic–aluminium sandwich structure, the latter representing the substrate cooler. The second layer of the device, starting from the bottom, represents the IGBT drift-layer. The first and the third layers are the collector and emitter regions, respectively. The fourth layer represents the aluminum emitter contact. The structure includes also the connecting wires of the emitter contacts. Passive cells are also considered, which surround the active area delimited by the emitter contacts.
As already pointed out in the description of the thermal simulator, in the avalanche simulation the power dissipation has essentially a 3D distribution. As electrical simulation is performed as 2D environment, and therefore returns a 2D power dissipation profile, the thermal power is

obtaining by linear extrusion of the electrical profile along the vertical direction, as reported in Figure 2.13.

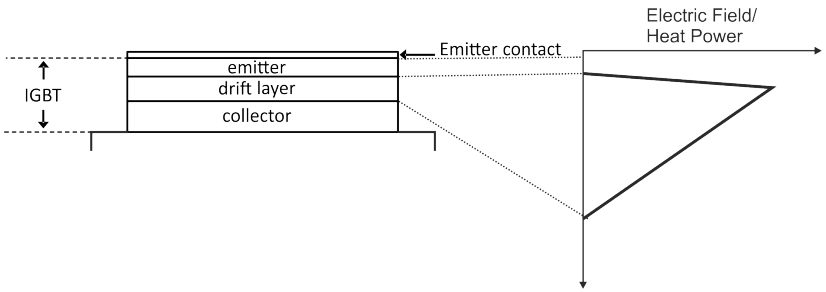


Figure 2.13: Structure of the Trench IGBT for the thermal simulation.

The first analysis conducted lays on the evaluation of the effect of the emitter layer resistivity onto the avalanche electrical behaviour. For the purpose, the device active area is divided in a 72×46 macrocells grid. With this subdivision, a maximum dimension of 200 µm is achieved. This solution is a good compromise between geometrical resolution and computational effort. A set of three isothermal simulation has been performed in order to evaluate the I–V curve for three layout, with 1, 4 and 8 emitter bond-wires respectively. Results of the simulation are depicted in Figure 2.14 and show that the effect of the emitter resistance is particularly evident at high levels of current. Here the layout with one emitter wire, where the effect of the voltage drop across the emitter contact is the most prominent, shows the highest voltage drop for a fixed current with respect to the other layouts. The voltage drop reduces by increasing the emitter wires, and is minimum for the single macrocell, as expected.
The results obtained by the previous simulations are indicative of the effect of emitter resistance though it happens at very high currents which the device doesn't work normally at. At normal current values, the thermal interaction and the instability produced by working in NDR region affects the most the reliability of the device. As a consequence, UIS electrothermal simulations are conducted starting from a current firstly set in the PDR part and secondly in the NDR region.

Analysis of Avalanche Operations in Stable Conditions Two operations in PDR region are simulated with different initial condition.

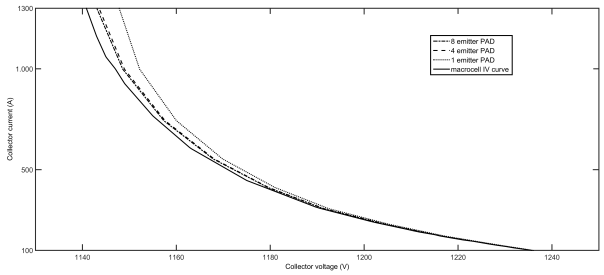


Figure 2.14: Isothermal IV curve for single macro-cell, 72×46 macro-cells with 8 emitter-pad, 4 emitter-pad and 1 emitter-pad.

In particular, as a general understanding of the avalanche operations, the first simulation is performed with initial uniform temperature distribution along the device, $T(x, y, z) = 300\,\mathrm{K}$. The initial current is set to 10 A and the inductance value is chosen to have a UIS duration of 50 µs. With this value of inductance, an initial turn-on transient of 1.5 µs is required in order to bring the current to the desired value. The resulting current and voltage waveforms of the device are shown in Figure 2.15. From the figure it is possible to see that the breakdown voltage initially increases due to the self-heating effect which predominates onto the positive resistance behaviour of the device. At about half of the discharge the effect of the positive resistance becomes more evident and the breakdown voltage decreases.

In Figure 2.16, temperature and power dissipation profile during the time are shown. The maximum temperature value is reached at a time t^* of about 37 µs, that is roughly at the three quarters of the discharge time, as theoretically expected for high voltage devices where the thickness of the low-doped region is not negligible [97]. Therefore the device experiments highest thermal stress when almost at the end of the UIS transient. The spatial current distribution has been evaluated at t^* and it is reported in Figure 2.17, normalized to the maximum value. Here, as expected from the theoretical thermal stability of PDR region, all the macrocells carries virtually the same amount of current.

The latter operative condition is a clear proof that if the current flows uniformly across the device, in PDR operation it remains uniform during the discharge. It is however important to understand the effect of the PDR stability when the current is initially flowing not uniformly

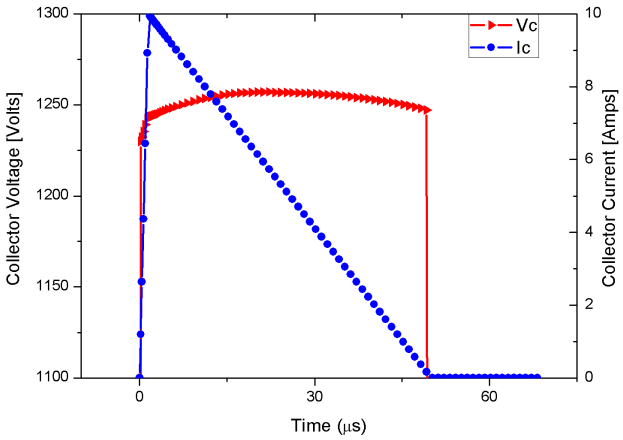


Figure 2.15: Current and voltage waveforms during UIS discharge operating in PDR.

along the device area. In these condition, the stability must drive the current to be equally shared among the macrocells. In order to verify this behaviour, a temperature inhomogeneity is introduced at the beginning of the UIS discharge, that is half part of the device is at 320 K and the other 300 K. A second simulation is therefore performed with this initial condition and with the same parameters as the previous one. The resulting current evolution along the time, measured either on a macrocell in the left half and in the right half of the device is reported in Figure 2.18. From the figure it is evident that, at the beginning of the UIS discharge, the whole current is virtually carried by half device (reflecting the initial unbalanced temperature distribution). During the time, however, the distance between the two curves decreases, showing that the current distribution becomes uniform on the device.

Analysis of Avalanche Operations in Unstable Conditions In this paragraph electrothermal simulation of the IGBT under consideration is performed for evaluate the unstable behaviour shown by the NDR part of the I-V avalanche characteristic. At this purpose the same UIS discharge test previously conducted for PDR, is here analysed with initial current set in NDR region. Initial temperature is uniform onto the

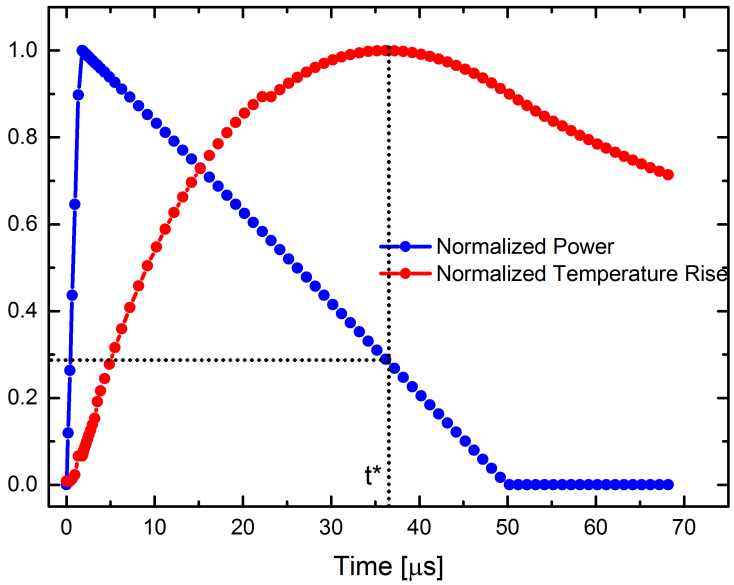


Figure 2.16: Temperature and power dissipation waveforms during UIS discharge operating in PDR.

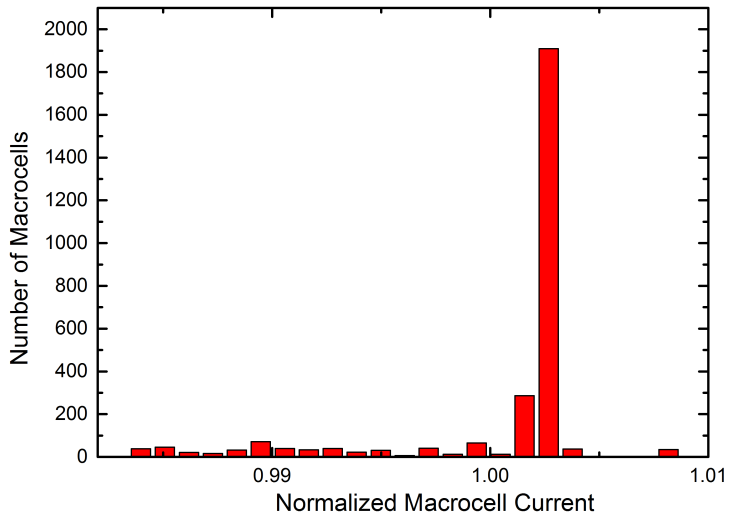


Figure 2.17: Normalized current distribution along the IGBT area in correspondence of the maximum temperature.

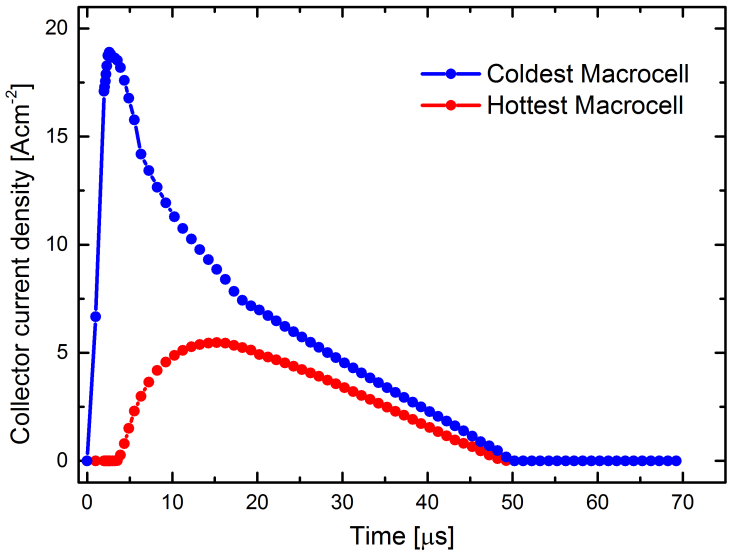


Figure 2.18: Current density in the hottest (red curve) macro-cell and in the coldest one(blue curve).

device, $T(x, y, z) = 300\,\mathrm{K}$, and the initial current is 60 A, discharging in 50 µs. A higher temperature increase is expected due to the higher current density inside the device. What is more, phenomena of instability are expected as well, because of the thermal instability. The current distribution obtained by the simulation are summarized by means of 2D map of the active area, measured at different times, and reported in Figure 2.19. The first map, taken at the beginning of the UIS discharge shows a current distribution nearly uniform along the device area, being the small differences produced either by emitter contact resistivity and by the geometrical layout. However, even these small non uniformities can be amplified by the positive feedback of the electrothermal interaction.

As a consequence, during the time, the inhomogeneities become more prominent and the current distribution tends to shrink in a small area. Such a behaviour is confirmed by the current maps taken at 4 µs and 6 µs respectively after the beginning of the avalanche has occurred. The phenomenon is therefore extremely fast and it mostly depends on to the strong of the electrothermal interaction. As a completion of the analysis, the temperature distribution after 6 µs is shown in Figure 2.20.

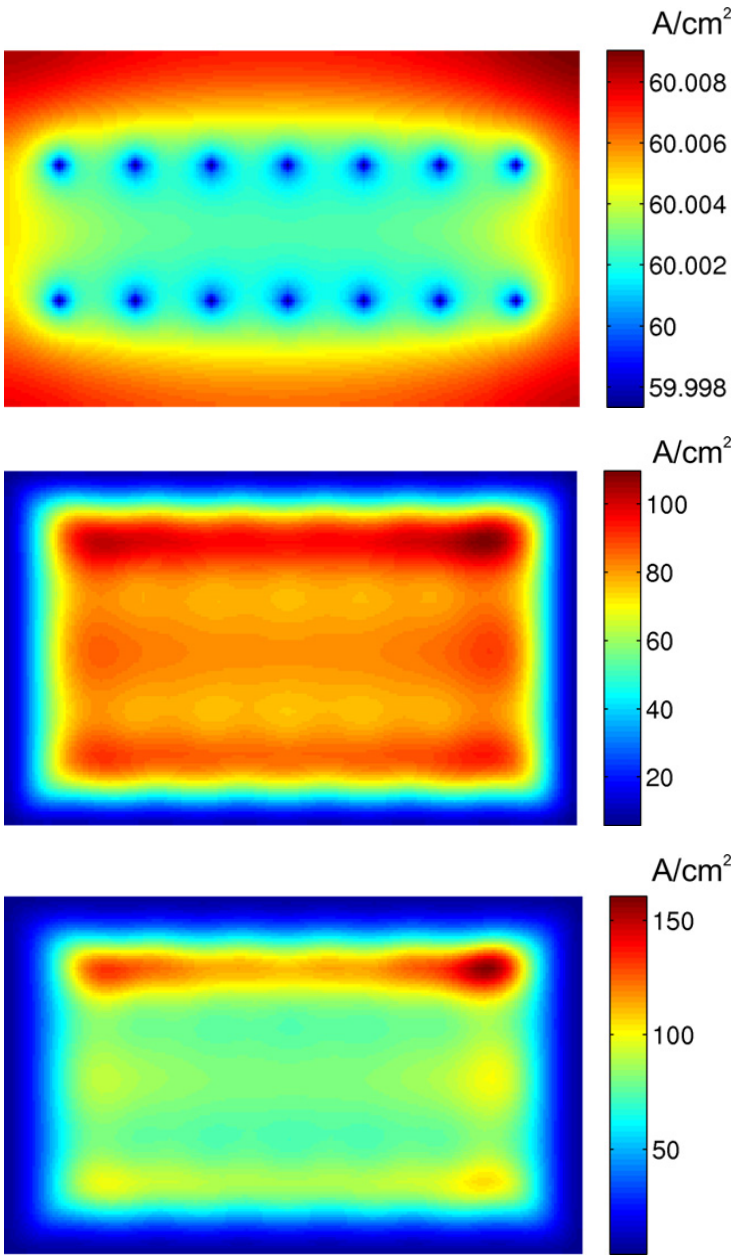


Figure 2.19: Device current distribution along the time during UIS avalanche simulation in NDR region: a)initial distribution; b) at 4 µs; c) at 6 µs.

The figure shows that the in correspondence of a temperature difference of 5 K the current density changes from 50 A cm^{-}2 to 150 A cm^{-2}, that is the current increases of a factor of 3 for 5 K difference. The strong instability of the NDR regions represents an important issue to consider in order to achieve high avalanche reliability.

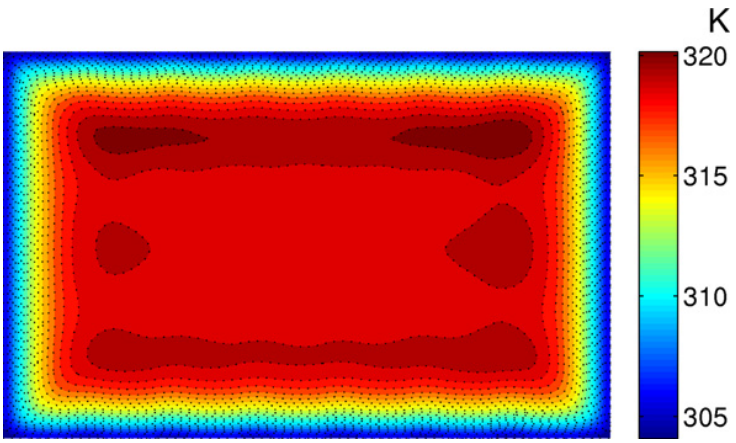


Figure 2.20: Device temperature distribution of UIS avalanche simulation in NDR region after 6 µs from the beginning of the discharge.

2.2.5 Simulation of Power Devices Avalanche Operation: Conclusions

This section handles with the investigation of reliability of Power Devices operating in avalanche condition. It has been shown that the avalanche operation can either affect the robustness or not according to the particular part of the I-V characteristic the device is working at. In particular, the NDR region present a thermally unstable behaviour and the resulting positive feedback between electrical and thermal phenomena can lead to a non uniform current distribution. In this regime, very high current densities are likely to flow in a small area of the device, leading to strong increases of the temperature. The electrothermal interaction has been shown to be very fast and only few microsecond are required for the current to shrink in a narrow area. Possible countermeasures to this effect must be aimed to the modification of the shape of I-V avalanche characteristic. It represents, as a matter of fact, the principal reference to predict the reliability of a power device which ex-

periments the avalanche condition. From an engineering point of view, a possible modification of the I-V curve can be obtained modifying the lifetime in low doped region. The technique is very effective and it is also attractive for industries which already makes use of processes which control the lifetime, by means of impurities implantation. By changing the peak energy level of the implant, or the position, one can change the lifetime in a localized part of the device. The modification of the lifetime affects, however, the conduction losses also, by modifying the on state voltage drop, so a trade-off among avalanche robustness and on state performance holds and both the regimes must be carefully addressed.

2.3 Simulation of Power Devices in Short Circuit Operation

2.3.1 The Short Circuit fault into Power Devices

The increasing demand of power semiconductor devices with an high reliability, especially in application fields like automotive or high power converters, has increased the necessity of a deep comprehension of the failure mechanisms which lead to a possible premature destruction of the device in both nominal and fault conditions. The Short-Circuit is one of the most critical conditions which a device can be subjected to and it is of great interest the investigation of the features of the device structure which can enhance the capability in this extreme condition. As already pointed out in 1.4.2, two types of fault conditions are possible whether the Short Circuit occurs during while the device is in the on state or the Short Circuit condition is already present when the device is turned on. Both conditions are very stressful for the device and lead to a significant energy dissipation inside the device. Basically, the Short Circuit condition is very harsh because of the high voltage and high current that at the same time occur in the device which, by means of the Joule effect, lead to a quick increase of the temperature into the structure (with a distribution dependent on the geometry of the device) [98, 99].

2.3.2 Simulation of Short Circuit Operation

Being the short circuit operation very interesting for industrial application, a lot of efforts have been spent in the past to correctly simulate such operative conditions. The solutions implemented for the electrothermal short circuit simulations are basically the same developed for the analysis in avalanche. Short circuit, however, is easy to simulate as the mechanism of the current flows is virtually the same of normal operation, that is the current can be turned off by the control terminal. The difference, of course, is the amount of energy dissipated, and therefore the increases of the temperature. In particular, short circuit phenomenon is considered to be more harmful than avalanche phenomenon when the long term reliability is considered, even at the same amount of energy dissipated [100]. Recent works have proposed several method for electrothermal simulations by means of mixed mode simulation approaches [35, 101]. TCAD simulations are helpful in the design phase of the basic device cell, but, due to the limitation in the maximum num-

ber of cell which can be simulated, they are not suitable for taking into account the effects of the layout of the device.
In the following section, electrothermal simulations in short circuit are presented in order to evaluate the importance of the device geometry on to the distribution of the current along the area and to evaluate the effect of instabilities that could arise in such operative mode.

2.3.3 A Novel 3D electro-thermal simulations of power semiconductor devices

In order to simulate the device behaviour in short circuit conditions, a novel simulation environment for analysis of electro-thermal interaction in power semiconductor devices has been implemented [102]. The developed solution is a mixed mode iterative simulator based on the joint use of SPICE program $ELDO^{®}$ [103], manufactured by Mentor Graphics, and $COMSOL^{®}$ Multiphysics.
The iterative scheme recalls the simulative approach already seen in 2.2.3. The thermal simulation is performed in the same way as already shown in the UIS simulation but a significant modification consists on the adoption of a SPICE software for the electrical simulation. The reasons for the usage of SPICE software are basically two:

- the analysis of different configurations can be easily implemented by definition of proper netlists;
- the description of the device can be made with implementation of custom SPICE models or by using models provided by the manufacturer.

As a consequence, this approach guarantees the electrothermal simulation to be used in wide field of applications and devices.
The thermal simulation by means of FEM analysis provide high accuracy of the temperature distribution and also a better description of the complicated geometrical features of the device.

Time Step control The solution here proposed differs from the one presented in 2.2.3 also for the different algorithm which regulates the time step of the simulation. In this case, in fact, the electrical time step is defined by the SPICE software itself, therefore the control is limited to time step of the electrothermal interaction. In particular, the electrical

and thermal simulation duration is defined according to the coupling level of electrical and thermal phenomena in order to guarantees the convergence of the electrothermal itherative process. This algorithm assumes that, for the imposed duration, either the electrical analysis and the thermal one converge. The case of non convergence of one or both the simulations is explicitly considered and properly addressed. A detailed working principle of the time step definition is here described:

- if both the electrical and thermal simulation converges and the iterative process takes less than M_{iter} iteration then the next time step is increased of a factor α_1;
- if both the electrical and thermal simulation converges but with a number of electrothermal iterations higher then M_{iter}, the next time step is equal to the current step;
- if the current simulation or the thermal simulation does not converge, or if the electrothermal iterations are large than $M_{iter,max}$, starting from the last successfully computed point, simulation is performed at a new time but with a step reduced of a factor α_2.

Parameters α_1, α_2, and number of iterations M_{iter} and $M_{iter,max}$ can be changed for achieving better performances.

The complete simulator A schematic description of the simulator is depicted in 2.21.

2.3.4 Short Circuit reliability evaluation of Power MOSFETs for Automotive Application

Automotive applications are particularly sensible to short circuit failures because the applications is often subjected to failure of motor winding insulation or wiring misconnections at the motor terminal, as already pointed out in 1.4.2. For this reason, a test to evaluate the short circuit capability of power devices is mandatory [104]. The test is generally aimed to either evaluate the maximum energy amount that the device can be safely sustaining in short circuit and to measure the capability of the control system to intervene in order to switch off the short circuit current. Among the different power devices, in automotive applications it is common to use Power MOSFETs, as the voltage requirements are

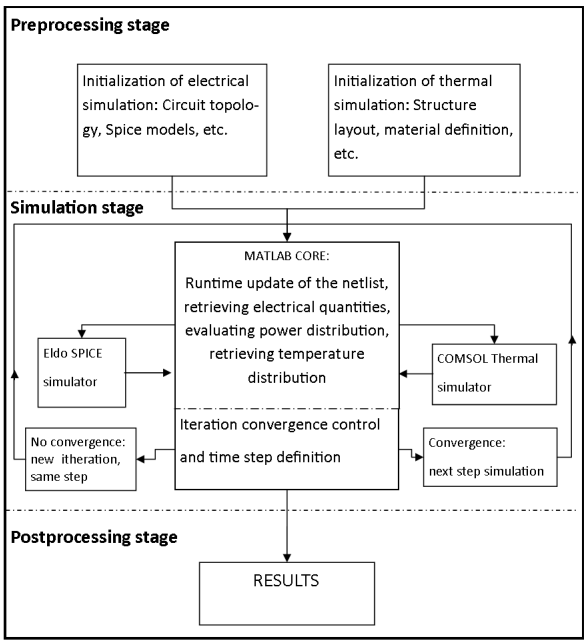


Figure 2.21: Schematic representation of electrothermal simulator by means of ELDO-COMSOL conjunction.

low and a high speed transitions are demanded. More in detail, Power MOSFETs with integrated gate control circuitry are used for sensing the short circuit events and switching off the device [105]. Power MOSFET has shown to have a thermally stable behaviour when in full conduction because of the negative dependence of mobility with temperature. However, it has been proved that instability phenomena can occur if the device works in particular conditions [106]. More in detail, the analysis conducted in [107] results in a definition of an analytical boundary for thermal stability operations:

$$\alpha(t) = \frac{\partial I_D}{\partial t} = \frac{1}{V_{DS} R_T(t)}, \tag{2.12}$$

where α is the derivative of the current with respect the temperature,

V_{DS} is the drain-to-source voltage and R_T is the device thermal resistance. The equation 2.12 can be represented in a $\alpha - I$ plane in order to evaluate graphically the stability region. The graphics is depicted in 2.22. The picture shows that the device exhibits instability for a range of currents which changes according to the product $V_{DS} \cdot R_T(t)$. More in detail, the larger is the product, either for high drain-to-source voltage and high thermal resistance, the larger is the instability region.

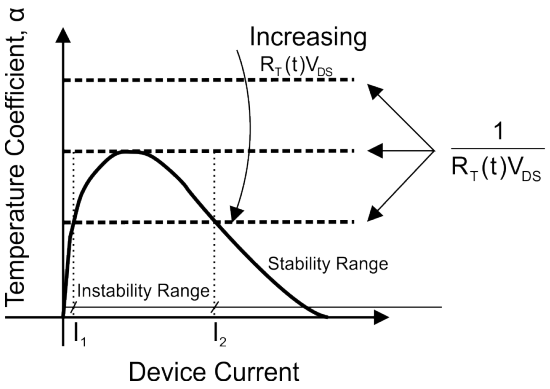


Figure 2.22: Thermal instability of Power MOSFET.

In short circuit, where V_{DS} is equal to the supply voltage, if the thermal resistance is not lower enough, thermally instability can occur and the device current increases with temperature. This phenomenon increases a lot the possibility of device failure and must be carefully addressed in the design phase, particularly for evaluating the device thermal resistance.
In order to analyse this unstable behaviour, 3D electrothermal simulations have been conducted on a low voltage Power MOSFET. The main goal of the simulations is to evaluate the effect of the device geometry on to the reliability in short circuit operations, that is to understand what is the impact of geometrical features on the maximum sustainable energy in short circuit failures. At the purpose, a $STripFET^{TM}II$ technology Power MOSFET (STB210NF02), which is provided with a TO-263 D^2PAK package, is chosen as device under test. The technical sheet reports a 20 V breakdown voltage, 120 A continuous drain current and $R_{DS}(ON) \leq 3.2\,\mathrm{m}\Omega$.
Starting from the characteristics drawn into the data sheet, a SPICE model can be calibrated in order to replicate the electrical behaviour of the device. In particular, a simple SPICE Level 1 model is used as

representation of the elementary macrocell used in the multicellular description of the device. The calibration requires the evaluation, by means of measurements, of the transconductance K_{P0} and zero-bias threshold voltage V_{th0} at ambient temperature. With this values, a first MOSFET SPICE model can be implemented at ambient temperature. The subcircuit representing the device must be enhanced in order to fit the electro-thermal behaviour of the DUT. AS a consequence, a drain resistance R_D, which explicitly models the voltage drop across the channel and drift regions, and dependence of the drain current on to the temperature are included in the model. In order to achieve dependence on the temperature, the threshold voltage and electron mobility expressions are modified, as proposed in [31]. The first has the following dependence on the temperature:

$$V_{th}(T) = V_{th}(T_0) - \alpha_{th}(T - T_0), \tag{2.13}$$

where α_{th} is a coefficient which has to be determined by the experimental data. Considering the expression of the overdrive voltage in the current expression and inserting the equation 2.13 it derives:

$$V_{GS} - V_{th}(T) = V_{GS} - V_{th}(T_0) + \alpha_{th}(T - T_0). \tag{2.14}$$

As a consequence, a behavioural voltage source can be connected between the driving circuit and the gate terminal to consider the reduction of threshold voltage with temperature. The variation of the electron mobility with temperature is modelled by modulation of the transconductance parameter of the SPICE model, K_P:

$$K_P(T) = K_{P0}\left(\frac{T}{T_0}\right)^{-m}, \tag{2.15}$$

where m is a parameter obtained by the calibration process. The complete SPICE netlist presents three electrical nodes (gate, drain and source) and a thermal one (operating temperature). The schematic of the overall short circuit test is represented in Figure 2.23.
In Table 2.1 are collected the values for the calibrated model together with the parasitic elements used for the following simulations.
The short circuit simulation is performed with the typical supply voltage of automotive application, 14.4 V. Figure 2.24 reports the comparison between the transcharacteristics obtained by measurement and simulation at two temperature: 30 °C and 150 °C. As already pointed out,

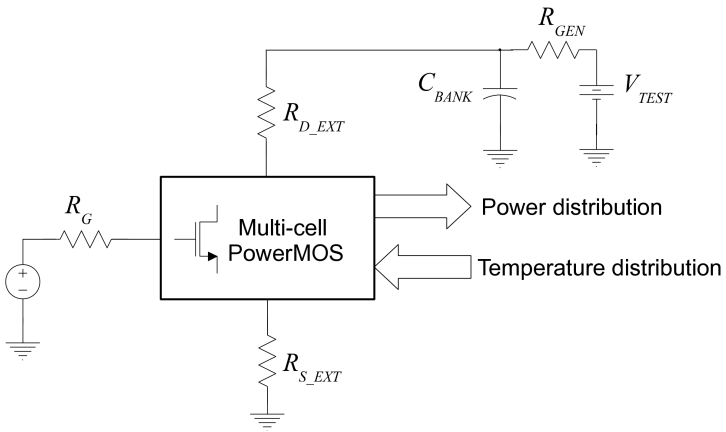


Figure 2.23: Schematic representation of ET simulation in short-circuit application.

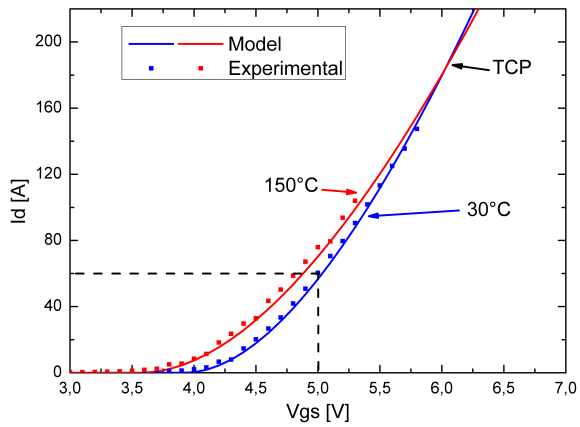


Figure 2.24: Experimental and model comparison of the DUT ID-VGS characteristic.

the drain-to-source voltage is set to 14.4 V. The two curves show a good matching, demonstrating the effectiveness of the SPICE description. As already seen for avalanche simulations, here also a multicellular approach is used, in order to take into account the spatial distribution of the current. In particular, the device has been subdivided in a network

Parameter	Description	Value
K_{P0}	Transconductance parameter	$122\,\mathrm{A\,V^{-2}}$
V_{th0}	Threshold voltage	$3.92\,\mathrm{V}$
R_D	Intrinsic drain resistance	$1.50\,\mathrm{m\Omega}$
RD_{EXT}	External drain resistance	$2.00\,\mathrm{m\Omega}$
RS_{EXT}	External source resistance	$2.00\,\mathrm{m\Omega}$
LD_{EXT}	Parasitic drain inductance	$50\,\mathrm{nH}$
LS_{EXT}	Parasitic source inductance	$50\,\mathrm{nH}$
LG_{EXT}	Parasitic gate inductance	–
α_{th}	Threshold voltage thermal coefficient	$3.00\,\mathrm{mV\,K^{-1}}$
m	Mobility thermal coefficient	1.25

Table 2.1: SPICE parameters.

of 30×50 macrocells. In the figure is also indicated the point the device operates at: with $V_{GS} = 5\,\mathrm{V}$ the device operates in the unstable region, therefore a positive current-temperature derivative is expected.
The domain for the thermal simulation is realized directly in COMSOL software and recalls the real device geometry. In particular, in order to further improve the accuracy, also the bond wires on top of the aluminium layer are considered, even if with a simplified geometry and limited to the part which is directly connected with the device. Such kind of simplifications in the thermal domains let to reduce the complexity of the thermal mesh, and therefore simulation times, without affecting significantly the correctness of the results [108]. Geometrical parameters of the domain are summarised in Table 2.2.

Parameter	Value
Active area length	5.6 mm
Active area width	4.6 mm
Chip thickness	400 µm
Aluminium top layer thickness	5 µm
Thermal mesh nodes	5000

Table 2.2: Chip dimensions and meshing details.

The heat source is placed into the silicon layer and it is considered uni-

formly distributed into a 20 µm thick volume in the top part of the silicon layer, according to the fact that for low voltage Power MOSFETs the large contribution to the voltage drop is due to the channel resistance, accumulation layer and epitaxial region, the latter being less prominent than the first two contributions [72]. The complete meshed domain is depicted in Figure 2.25.

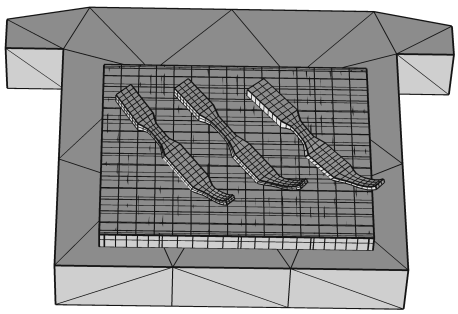


Figure 2.25: Geometry of the meshed device for the thermal simulation.

Simulation of 3 ms short circuit is conducted in order to evaluate the electrical behaviour and the maximum temperature. What is more, the analysis of the effect of device geometry over the temperature is also investigated.
Resulting electrical waveforms are depicted in Figure 2.26. At the same time, experimental measurements conducted on the same device, are used as a comparison for the simulation results. The latter are depicted in the same Figure superposed to the simulated waveforms.
As shown in the Figure, the electrothermal description made for the simulation correctly replicates the behaviour of the real device. The accuracy of the description is obtained with a fine fitting of the SPICE model.
The analysis of the temperature distribution along the device is first

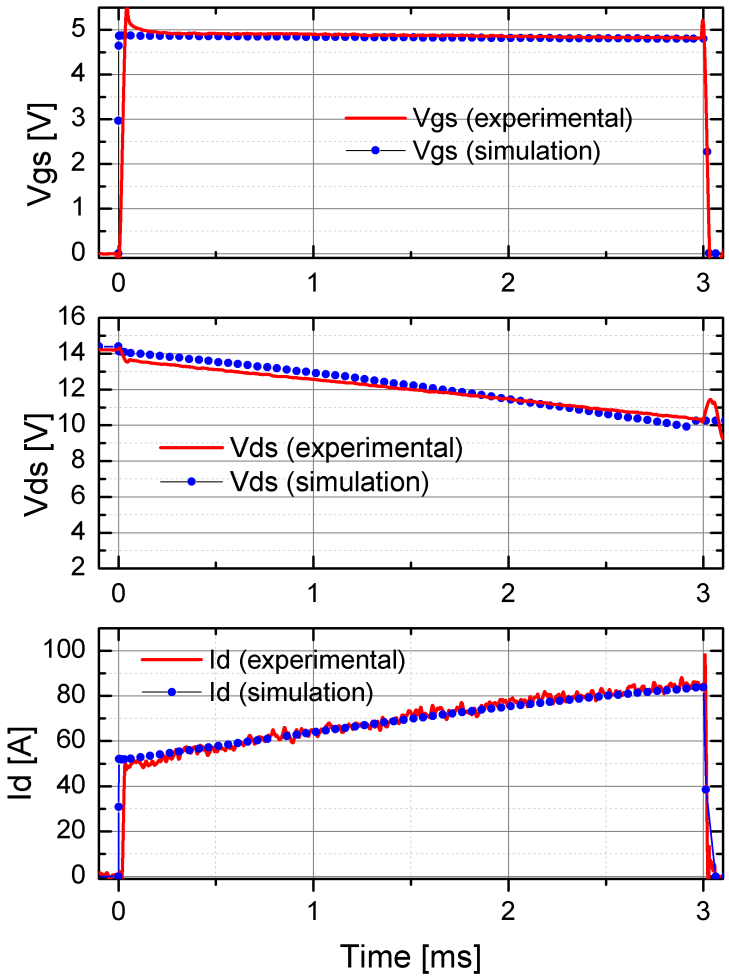


Figure 2.26: Comparison between experimental and simulation waveforms during the short-circuit test.

performed experimentally, by means of InfraRed thermography measurements, using a state-of-the-art transient thermography system [109]. The resulting thermal maps are depicted in Figure 2.27–1 for different times. The maps clearly show that the geometry of the device plays a deep contribution onto the thermal behaviour and this is also accentuated by the instability of the chosen operative point. More in details, the temperature distributes non uniformly along the device and has more

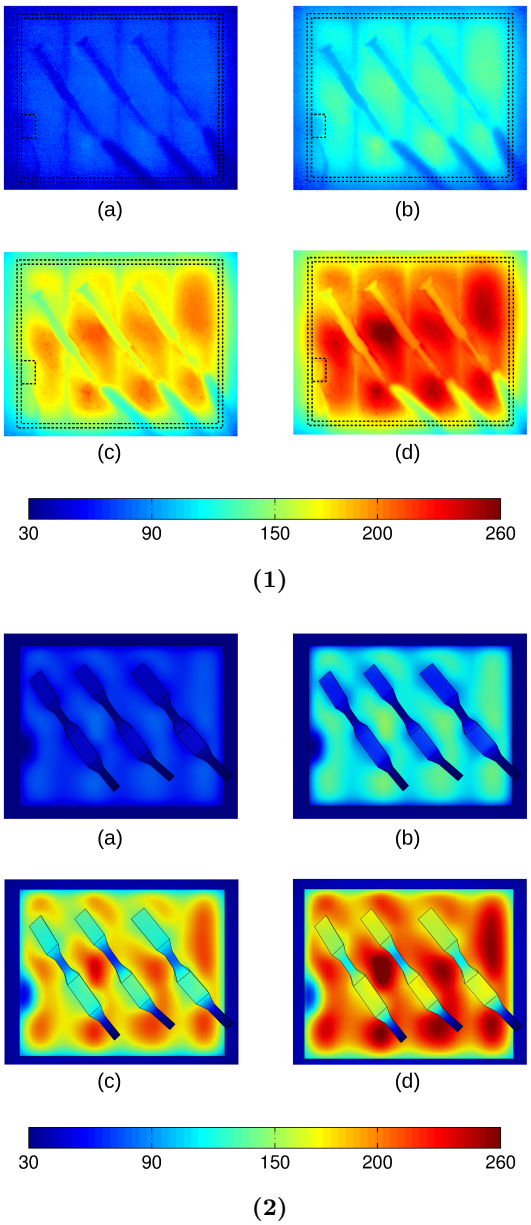


Figure 2.27: 1) Experimental and 2) Simulated temperature maps at different times during short circuit: a) $t = 0.5\,\text{ms}$; b) $t = 1.2\,\text{ms}$; c) $t = 1.9\,\text{ms}$; d) $t = 2.5\,\text{ms}$.

peaks localised between the bond wires with maximum temperature spot located between the first and the second wire, starting from the left. In a unstable region of operation, this effect is also more important because the positive feedback between current and temperature amplifies the non uniformities.

In order to show that the phenomenon is strongly related to the geometry, the surface temperature distribution obtained by the simulation on the structure of Figure 2.25, taken at the same times of the experiments, is shown in Figure 2.27–2. From the comparison between the experimental maps and the simulated ones it can be clearly evinced that, by a correct reproduction of the device geometrical layout, is possible to simulate the effect of self heating with high accuracy.

The complicated geometry of a power device is therefore an important aspect to consider when maximum temperature of operation must be evaluated, as the approximation of considering the temperature uniformly distributed leads to significant inaccuracies, especially in short circuit failure analyses. It is also important to underline that this effect is present also when the device operates in stable condition. The main difference is that, in stable conditions, the difference are attenuated because the current flows in colder regions.

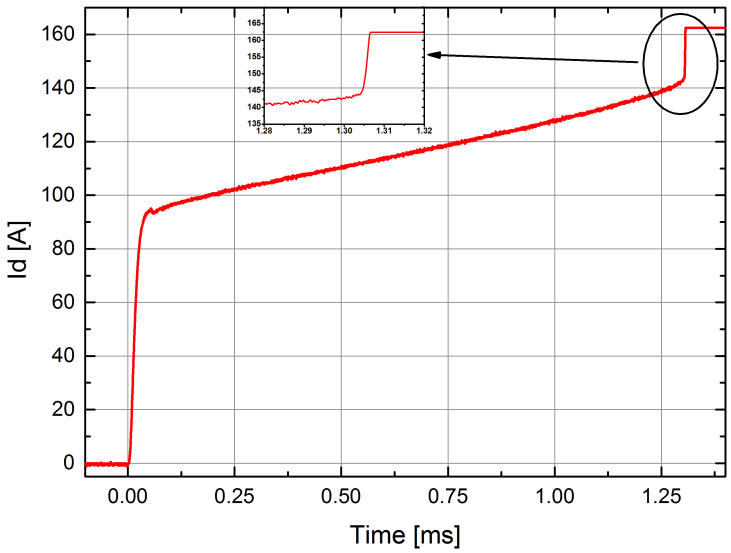


Figure 2.28: Experimental evidence of a short circuit failure.

When the short circuit failure holds for long times, the device fails because of the high temperature reached. Figure 2.28 shows the results of experimental measurement of the failure in a short circuit test for the considered power device. In this case, a $V_{GS} = 5.5\,\mathrm{V}$ is imposed and the initial device current is about 95 A. For this value of current the device still operates in unstable region, as the minimum stable current, from Figure 2.24 is at 180 A. As can be seen from the electrical waveforms, the short circuit current increases almost linearly, because of the positive electrothermal interaction, up to 145 A at 1.45 ms. After that, the current experiments an abrupt increase of slope and raises almost vertically with a slope of about $6\,\mathrm{A\,\mu s^{-1}}$. The phenomenon that governs this failure mode is dictated by the thermally generated leakage current, which shows an exponential dependence with temperature.

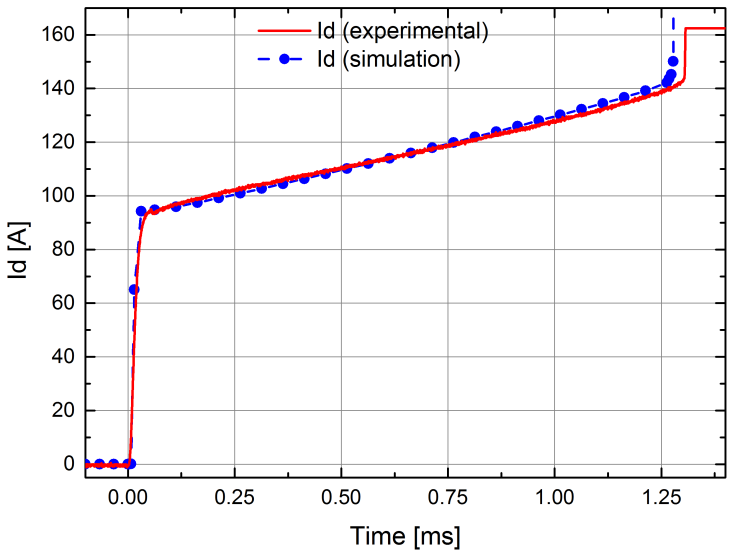
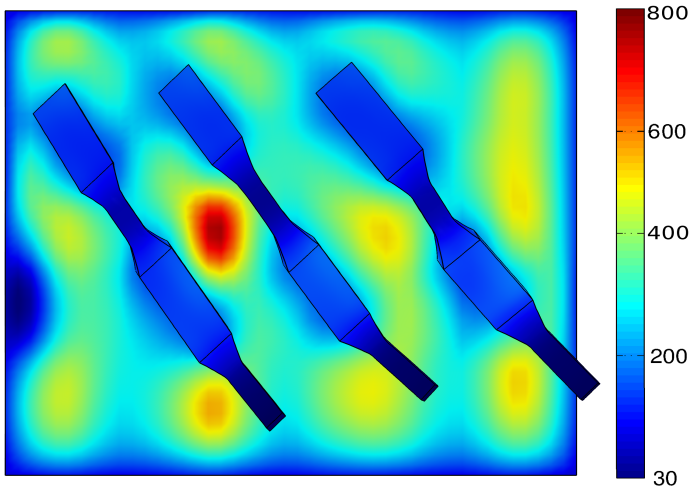


Figure 2.29: Experimental evidence of a short circuit failure.

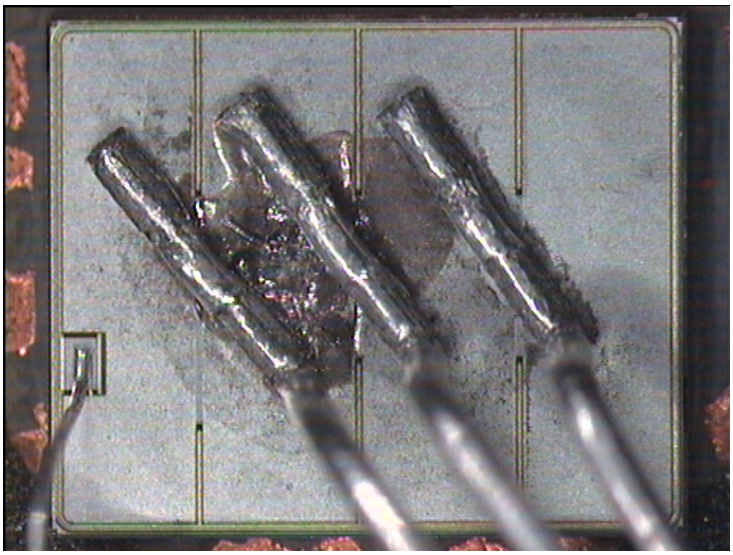
This behaviour can be included in the simulation with a modification in the SPICE model. More in detail, a temperature dependent current source is included that has the following expression [110]:

$$I_{leak}(T) = I_{leak}(T_{REF}) \left(\frac{T}{T_{REF}}\right)^{b} exp\left(-\frac{E_G}{K_B T}\right), \tag{2.16}$$

where T_{REF} is the reference temperature, K_B is the Boltzmann constant,



(a)



(b)

Figure 2.30: a) Simulation device temperature distribution at failure; b) Image of failed device.

E_G is the bandgap energy at ambient temperature, supposed weakly dependent on temperature variation, and b is a fitting parameter.
By means of this expression, the current increases also because of the leakage current generation. By proper fitting of equation 2.16 the contribution of the leakage generation can be tuned in order to recall what obtained in the experiments. As a demonstration, Figure 2.29 reports the comparison between the experimental waveforms already shown in Figure 2.28 and the result obtained by the simulation which models also the leakage current dependence on the temperature. Figure 2.29 clearly shows how good is the replication of the failure electrical waveforms, with the simulated failure starting few hundreds of nanoseconds before the actual failure. The analysis conducted by the simulation also let to evaluate the temperature map of the device in correspondence of the failure, which is not possible with experimental set up. The resulting temperature profile is depicted in Figure 2.30a, and shows that the hot spot of temperature which has been already indicated in the previous simulation, reaches a temperature of nearly 800 K which correspond to an estimation of T_{CRIT} for the considered Power-MOSFET.
As confirmation of the failure mechanism and also to confirm the hot spot position that has been previsioned by the simulation, an image of the device after the failure is shown in Figure 2.30b. Here a fail spot is clearly visible and it corresponds at the place the simulation indicated as hot spot point.

2.3.5 Simulation of Power Devices in Short Circuit Operation: Conclusions

In this section, the reliability of power devices in short circuit condition has been addressed. In particular, a simulation environment has been developed for conducting electrothermal simulation of wide area devices experimenting short circuit condition. The simulator has been used for evaluating the effect of geometry on to the current and temperature distribution. Short circuit simulations have been performed on a low voltage Power MOSFET for automotive applications. The simulations have shown that device can experiment thermal instability and that this behaviour significantly affects the reliability of the device. In these conditions, the assumption of uniform temperature distribution along the device area underestimates the actual maximum temperature inside the device. What is more, the analysis of latch up failure due to the

thermal increase of the leakage current has been conducted.
The simulations findings have been validated by experimental evidences of the phenomenon and it has been found out that a correct reproduction of the physical phenomenon can be obtained in simulation with accurate reproduction of the device structure.

2.4 References

[1] Brian Kerridge. *PC-based analog simulation: EDN Special Report*. Tech. rep. EDN, 1990.

[2] Laurence W. Nagel and D.O. Pederson. *SPICE (Simulation Program with Integrated Circuit Emphasis)*. Tech. rep. UCB/ERL M382. EECS Department, University of California, Berkeley, Apr. 1973. URL: http://www.eecs.berkeley.edu/Pubs/TechRpts/1973/22871.html.

[3] Laurence W. Nagel and R. Rohrer. "Computer analysis of nonlinear circuits, excluding radiation (CANCER)". In: *Solid-State Circuits, IEEE Journal of* 6.4 (Aug. 1971), pp. 166–182. ISSN: 0018-9200. DOI: 10.1109/JSSC.1971.1050166.

[4] H. K. Gummel and H. C. Poon. "An Integral Charge Control Model of Bipolar Transistors". In: *Bell System Technical Journal* 49.5 (1970), pp. 827–852. ISSN: 1538-7305. DOI: 10.1002/j.1538-7305.1970.tb01803.x. URL: http://dx.doi.org/10.1002/j.1538-7305.1970.tb01803.x.

[5] Laurence W. Nagel. "SPICE2 : A Computer Program to Simulate Semiconductor Circuits". In: *ERL Memo ERL-M520* (1975). URL: http://ci.nii.ac.jp/naid/10014700971/en/.

[6] Ellis Cohen. *Program reference for SPICE2*. Tech. rep. DTIC Document, 1976.

[7] Chung-Wen Ho, Albert E. Ruehli, and Pierce A. Brennan. "The modified nodal approach to network analysis". In: *Circuits and Systems, IEEE Transactions on* 22.6 (June 1975), pp. 504–509. ISSN: 0098-4094. DOI: 10.1109/TCS.1975.1084079.

[8] Andrei Vladimirescu and Sally Liu. *The simulation of MOS integrated circuits using SPICE2*. Tech. rep. DTIC Document, 1980.

[9] H Jo de Man. "Computer-aided design for integrated circuits: trying to bridge the gap". In: *Solid-State Circuits, IEEE Journal of* 14.3 (1979), pp. 613–621.

[10] AL Sangiovanni-Vincentelli and NBG Rabbat. "Techniques for time-domain analysis of lsi circuits". In: *IEE Proceedings G (Electronic Circuits and Systems)*. Vol. 127. 6. IET. 1980, pp. 292–301.

[11] Joseph G Tront et al. "Computer-aided analysis of RFI effects in operational amplifiers". In: *Electromagnetic Compatibility, IEEE Transactions on* 4 (1979), pp. 297–306.

[12] Richard Dean Davis. "Design and analysis of NMOS operational amplifier with depletion loads". In: *MS Thesis Illinois Univ., Urbana-Champaign. Coordinated Science Lab.* 1 (1979).

[13] EF Oberst. *Analysis of three-phase power-supply systems using computer-aided design programs*. Tech. rep. California Univ., Livermore (USA). Lawrence Livermore Lab, 1977.

[14] S Ben-Yaakov. "SPICE simulation of PWM DC-DC convertor systems: voltage feedback, continuous inductor conduction mode". In: *Electronics Letters* 25.16 (1989), pp. 1061–1063.

[15] MH Pong and RD Jackson. "Computer-aided design of power electronic circuits". In: *IEE Proceedings B (Electric Power Applications)*. Vol. 132. 6. IET. 1985, pp. 301–306.

[16] Ronald S Vogelsong and Chris Brzezinski. "Simulation of thermal effects in electrical systems". In: *Applied Power Electronics Conference and Exposition, 1989. APEC'89. Conference Proceedings 1989., Fourth Annual IEEE*. IEEE. 1989, pp. 353–356.

[17] Mark E Liffring and Robert J Spier. "Simulating discrete semiconductors with differing junction temperatures on SPICE". In: *1988 IECEC; Proceedings of the Twenty-third Intersociety Energy Conversion Engineering Conference, Volume 3*. Vol. 3. 1988, pp. 457–461.

[18] RP Pokala and D Divekar. "Thermal analysis in SPICE". In: *Computer-Aided Design, 1989. ICCAD-89. Digest of Technical Papers., 1989 IEEE International Conference on*. IEEE. 1989, pp. 256–259.

[19] BW Williams. "State-space thyristor computer model". In: *Electrical Engineers, Proceedings of the Institution of* 124.9 (1977), pp. 743–746.

[20] Youl-Kyu Suh. "SCR modeling by using SPICE". In: (1983).

[21] A Barili, G Cottafava, and E Dallago. "A SPICE2 SCR model for power circuit analysis". In: *Computer-Aided Design* 16.5 (1984), pp. 279–284.

[22] RA Minasian. "Power MOSFET dynamic large-signal model". In: *IEE Proceedings I (Solid-State and Electron Devices)* 130.2 (1983), pp. 73–79.

[23] CH Xu and D Schroder. "Modelling and simulation of power MOSFETs and power diodes". In: *Power Electronics Specialists Conference, 1988. PESC'88 Record., 19th Annual IEEE.* IEEE. 1988, pp. 76–83.

[24] R.J. McDonald and J.G. Fossum. "High-voltage device modeling for SPICE simulation of HVIC's". In: *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 7.3 (Mar. 1988), pp. 425–432. ISSN: 0278-0070. DOI: 10.1109/43.3176.

[25] CH Xu and D Schroder. "A power bipolar junction transistor model describing the static and the dynamic behavior". In: *Power Electronics Specialists Conference, 1989. PESC'89 Record., 20th Annual IEEE.* IEEE. 1989, pp. 314–321.

[26] Masataka Miyake et al. "Temperature dependence of switching performance in IGBT circuits and its compact modeling". In: *Power Semiconductor Devices and ICs (ISPSD), 2011 IEEE 23rd International Symposium on.* IEEE. 2011, pp. 148–151.

[27] M Macchiaroli et al. "Improved electro-thermal simulation of power devices". In: Therminic. 2002.

[28] S Schroder, Dirk Detjen, and Rik WAA De Doncker. "Multi-cell circuit model for high-power thyristor-type semiconductor devices". In: *Industry Applications, IEEE Transactions on* 39.6 (2003), pp. 1641–1647.

[29] David T Zweidinger, Sang-Gug Lee, and Robert M Fox. "Compact modeling of BJT self-heating in SPICE". In: *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 12.9 (1993), pp. 1368–1375.

[30] FF Protiwa, O Apeldoorn, and N Groos. "New IGBT model for PSPICE". In: *Power Electronics and Applications, 1993., Fifth European Conference on.* IET. 1993, pp. 226–231.

[31] V d'Alessandro, F Frisina, and N Rinaldi. "SPICE simulation of electro-thermal effects in new-generation multicellular VDMOS transistors". In: *Microelectronics, 2002. MIEL 2002. 23rd International Conference on.* Vol. 1. IEEE. 2002, pp. 201–204.

[32] C Abbate et al. "Turn-off instabilities in large area IGBTs". In: *Microelectronics Reliability* 54.9 (2014), pp. 1927–1934.

[33] Vincenzo d'Alessandro et al. "Analysis of the UIS behavior of power devices by means of SPICE-based electrothermal simulations". In: *Microelectronics Reliability* 53.9–11 (2013). European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, pp. 1713 –1718. ISSN: 0026-2714. DOI: http://dx.doi.org/10.1016/j.microrel.2013.07.083. URL: http://www.sciencedirect.com/science/article/pii/S0026271413002588.

[34] R. Kraus and K. Hoffmann. "An analytical model of IGBTs with low emitter efficiency". In: *Power Semiconductor Devices and ICs, 1993. ISPSD '93., Proceedings of the 5th International Symposium on*. May 1993, pp. 30–34. DOI: 10.1109/ISPSD.1993.297102.

[35] Michele Riccio et al. "3-D electrothermal simulation of active cycling on smart power {MOSFETs} during short-circuit and {UIS} conditions". In: *Microelectronics Reliability* 54.9–10 (2014). SI: {ESREF} 2014, pp. 1845 –1850. ISSN: 0026-2714. DOI: http://dx.doi.org/10.1016/j.microrel.2014.08.011. URL: http://www.sciencedirect.com/science/article/pii/S0026271414003722.

[36] Guang-Ping Shen, Min Qin, and Qing-An Huang. "SPICE Model with Lumped Circuits for A Thermal Flow Sensor". In: *Sensors, 2006. 5th IEEE Conference on*. Oct. 2006, pp. 1444–1447. DOI: 10.1109/ICSENS.2007.355905.

[37] R. Fizesan and D. Pitica. "Circuit models for power/ground planes on PCBs using SPICE method". In: *Design and Technology of Electronics Packages, (SIITME) 2009 15th International Symposium for*. Sept. 2009, pp. 155–160. DOI: 10.1109/SIITME.2009.5407382.

[38] A Hrennikoff. "Solution of problems of elasticity by the framework method". In: *Journal of applied mechanics* 8.4 (1941), pp. 169–175.

[39] Richard Courant et al. "Variational methods for the solution of problems of equilibrium and vibrations". In: *Bull. Amer. Math. Soc* 49.1 (1943), pp. 1–23.

[40] J.J. Barnes and R.J. Lomax. "Two-dimensional finite element simulation of semiconductor devices". In: *Electronics Letters* 10.16 (Aug. 1974), pp. 341–343. ISSN: 0013-5194. DOI: 10.1049/el:19740270.

[41] P Calzolari, S Graffi, and G Pierini. "Finite-difference and finite-element methods for the semiconductor flow equations". In: *International Symposium on Finite Element Methods Problems, Conference Proceedings*. 1974.

[42] Peter E Cottrell and EM Buturla. "Steady-state analysis of field effect transistors via the finite element method". In: *Electron Devices Meeting, 1975 International*. Vol. 21. IEEE. 1975, pp. 51–54.

[43] John J Barnes and Ronald J Lomax. "Finite-element methods in semiconductor device simulation". In: *IEEE Transactions on Electron Devices* 24 (1977), pp. 1082–1089.

[44] RJ Lomax. "Preservation of the conservation properties of the finite element method under local mesh refinement". In: *Computer Methods in Applied Mechanics and Engineering* 12.3 (1977), pp. 309–314.

[45] Mark R Pinto et al. "ULSI technology development by predictive simulations". In: *Electron Devices Meeting, 1993. IEDM'93. Technical Digest., International*. IEEE. 1993, pp. 701–704.

[46] Hiroo Masuda et al. "TCAD strategy for predictive VLSI memory development". In: *Electron Devices Meeting, 1994. IEDM'94. Technical Digest., International*. IEEE. 1994, pp. 153–156.

[47] Giovanni Breglio et al. "Study of a failure mechanism during UIS switching of planar PT-IGBT with current sense cell". In: *Microelectronics Reliability* 47.9 (2007), pp. 1756–1760.

[48] Andrea Irace et al. "Effect of a buffer layer in the epi-substrate region to boost the avalanche capability of a 100V Schottky diode". In: *Microelectronics Reliability* 46.9 (2006), pp. 1784–1789.

[49] Integrated Systems Engineering. *ISE TCAD Tool, Version 9.5 Manual*. 2004.

[50] SILVACO International. *ATLAS: 2-D Device Simulation Software*. 2000.

[51] Gerhard A Franz. "Numerical issues in power device simulation and modelling". In: *Computers in Power Electronics, 1988., IEEE Workshop on*. IEEE. 1988, pp. 43–48.

[52] Andrea F Franz. "BAMBI–A Design Model for Power MOSFET's". In: *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 4.3 (1985), pp. 177–189.

[53] Jerry G Fossum, Robert J Mcdonald, and M Ayman Shibib. "Network representations of LIGBT structures for CAD of power integrated circuits". In: *Electron Devices, IEEE Transactions on* 35.4 (1988), pp. 507–515.

[54] AA Keshavarz et al. "Computer simulation of ionizing radiation burnout in power MOSFETs". In: *Nuclear Science, IEEE Transactions on* 35.6 (1988), pp. 1422–1427.

[55] B Jayant Baliga. "The MOS-gated emitter switched thyristor". In: *Electron Device Letters, IEEE* 11.2 (1990), pp. 75–77.

[56] Masakazu Yamaguchi et al. "High-speed 600V NPT-IGBT with unclamped inductive switching (UIS) capability". In: *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD'03. 2003 IEEE 15th International Symposium on*. IEEE. 2003, pp. 349–352.

[57] Daniel Donoval and Andrej Vrbicky. "Analysis of the electrical and thermal properties of power DMOS devices during UIS supported by 2-D process and device simulation". In: *Advanced Semiconductor Devices and Microsystems, 2004. ASDAM 2004. The Fifth International Conference on*. IEEE. 2004, pp. 211–214.

[58] J Gregory Rollins and John Choma. "Mixed-mode PISCES-SPICE coupled circuit and device solver". In: *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 7.8 (1988), pp. 862–867.

[59] John RF McMacken and Savvas G Chamberlain. "CHORD: a modular semiconductor device simulation development tool incorporating external network models". In: *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 8.8 (1989), pp. 826–836.

[60] Gerhard A Franz. "Multilevel simulation tools for power converters". In: *Applied Power Electronics Conference and Exposition, 1990. APEC'90, Conference Proceedings 1990., Fifth Annual*. IEEE. 1990, pp. 629–633.

[61] Robert W Michelet. "A multi-simulator environment for power supply simulation". In: *Applied Power Electronics Conference and Exposition, 1991. APEC'91. Conference Proceedings, 1991., Sixth Annual*. IEEE. 1991, pp. 278–284.

[62] Y Kang and JD Lavers. "Power electronics simulation: Current progress and future development". In: *Computers in Power Electronics, 1994., IEEE 4th Workshop on*. IEEE. 1994, pp. 169–174.

[63] Kartikeya Mayaram and Donald O Pederson. "Coupling algorithms for mixed-level circuit and device simulation". In: *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 11.8 (1992), pp. 1003–1012.

[64] N Rabbat, Alberto L Sangiovanni-Vincentelli, and Hsueh Hsieh. "A multilevel Newton algorithm with macromodeling and latency for the analysis of large-scale nonlinear circuits in the time domain". In: *Circuits and Systems, IEEE Transactions on* 26.9 (1979), pp. 733–741.

[65] Conor S Rafferty, Mark R Pinto, and Robert W Dutton. "Iterative methods in semiconductor device simulation". In: *Electron Devices, IEEE Transactions on* 32.10 (1985), pp. 2018–2027.

[66] Georg Digele, Steffi Lindenkreuz, and Erich Kasper. "Fully coupled dynamic electro-thermal simulation". In: *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* 5.3 (1997), pp. 250–257.

[67] Matthias Heil. "An efficient solver for the fully coupled solution of large-displacement fluid–structure interaction problems". In: *Computer Methods in Applied Mechanics and Engineering* 193.1 (2004), pp. 1–23.

[68] B Du et al. "Transient thermal analysis of power devices based on Fourier-series thermal model". In: *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*. IEEE. 2008, pp. 3129–3135.

[69] Ian Swan et al. "A fast loss and temperature simulation method for power converters, Part II: 3-D thermal model of power module". In: *Power Electronics, IEEE Transactions on* 27.1 (2012), pp. 258–268.

[70] Ian R Swan et al. "3-D thermal simulation of power module packaging". In: *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*. IEEE. 2009, pp. 1247–1254.

[71] Mohammad Shahjalal, Hua Lu, and Chris Bailey. "A review of the computer based simulation of electro-thermal design of power electronics devices". In: *Thermal Investigations of ICs and Systems (THERMINIC), 2014 20th International Workshop on*. IEEE. 2014, pp. 1–6.

[72] B Jayant Baliga. *Fundamentals of power semiconductor devices*. Springer Science & Business Media, 2010.

[73] M Riccio et al. "Electro-thermal instability in multi-cellular Trench-IGBTs in avalanche condition: experiments and simulations". In: *Power Semiconductor Devices and ICs (ISPSD), 2011 IEEE 23rd International Symposium on*. IEEE. 2011, pp. 124–127.

[74] Hideharu Egawa. "Avalanche characteristics and failure mechanism of high voltage diodes". In: *Electron Devices, IEEE Transactions on* 11 (1966), pp. 754–758.

[75] Roman Baburske, Josef Lutz, and Birk Heinze. "Effects of negative differential resistance in high power devices and some relations to DMOS structures". In: *Reliability Physics Symposium (IRPS), 2010 IEEE International*. IEEE. 2010, pp. 162–169.

[76] BK Ridley. "Specific negative resistance in solids". In: *Proceedings of the Physical Society* 82.6 (1963), p. 954.

[77] Antonio Caruso, Paolo Spirito, and Gianfranco Vitale. "Negative resistance induced by avalanche injection in bulk semiconductors". In: *Electron Devices, IEEE Transactions on* 21.9 (1974), pp. 578–586.

[78] H-J Schulze et al. "Limiting factors of the safe operating area for power devices". In: *Electron Devices, IEEE Transactions on* 60.2 (2013), pp. 551–562.

[79] Roman Baburske et al. "Destruction behavior of power diodes beyond the SOA limit". In: *Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium on*. IEEE. 2012, pp. 365–368.

[80] N Lophitis et al. "Experimentally validated three dimensional GCT wafer level simulations". In: *Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium on*. IEEE. 2012, pp. 349–352.

[81] Toru Toyabe et al. "A numerical model of avalanche breakdown in MOSFET's". In: *Electron Devices, IEEE Transactions on* 25.7 (1978), pp. 825–832.

[82] J Rhayem et al. "Novel 3D electro-thermal robustness optimization approach of super junction power MOSFETs under unclamped inductive switching". In: *Proc. IEEE Int'l Conf. on Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM)*. Citeseer. 2012, pp. 69–73.

[83] Michele Riccio et al. "3D electro-thermal simulations of wide area power devices operating in avalanche condition". In: *Microelectronics Reliability* 52.9 (2012), pp. 2385–2390.

[84] MATLAB. *version 7.12.0 (R2012a)*. Natick, Massachusetts: The MathWorks Inc., 2012.

[85] COMSOL Multiphysics. *version 4.0*. Stockholm, Sweden: COMSOL, 2012.

[86] Chung-Wen Ho, Albert E Ruehli, and Pierce A Brennan. "The modified nodal approach to network analysis". In: *Circuits and Systems, IEEE Transactions on* 22.6 (1975), pp. 504–509.

[87] Albert Ruehli et al. "Stable time domain solutions for EMC problems using PEEC circuit models". In: *Electromagnetic Compatibility, 1994. Symposium Record. Compatibility in the Loop., IEEE International Symposium on*. IEEE. 1994, pp. 371–376.

[88] Fernando L Alvarado, Robert H Lasseter, and Juan J Sanchez. "Testing of trapezoidal integration with damping for the solution of power transient problems". In: *Power Apparatus and Systems, IEEE Transactions on* 12 (1983), pp. 3783–3790.

[89] Charles William Gear. *Efficient Stepsize Control for Output and Discontinuities*. Department of Computer Science, University of Illinois at Urbana-Champaign, 1982.

[90] V d'Alessandro et al. "A novel SPICE macromodel of BJTs including the temperature dependence of high-injection effects". In: *Microelectronics, 2004. 24th International Conference on*. Vol. 1. IEEE. 2004, pp. 253–256.

[91] Carl T Kelley. *Solving nonlinear equations with Newton's method*. Vol. 1. Siam, 2003.

[92] James M Ortega and Werner C Rheinboldt. *Iterative solution of nonlinear equations in several variables*. Vol. 30. Siam, 1970.

[93] Donald A Calahan. *Computer-Aided Network Design: Revised Edition*. Tech. rep. DTIC Document, 1972.

[94] V d'Alessandro and N Rinaldi. "A critical review of thermal models for electro-thermal simulation". In: *Solid-State Electronics* 46.4 (2002), pp. 487–496.

[95] Marshall Bern and David Eppstein. "Mesh generation and optimal triangulation". In: *Computing in Euclidean geometry* 1 (1992), pp. 23–90.

[96] William J McCalla. *Fundamentals of computer-aided circuit simulation*. Vol. 37. Springer Science & Business Media, 1987.

[97] A Agnone et al. "A New Thermal Model for Power Mosfet Devices Accounting for the Behavior in Unclamped Inductive Switching". In: *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*. IEEE. 2007, pp. 1006–1012.

[98] Malay Trivedi and Krishna Shenai. "Investigation of the short-circuit performance of an IGBT". In: *Electron Devices, IEEE Transactions on* 45.1 (1998), pp. 313–320.

[99] J Lutz and T Basler. "Short-circuit ruggedness of high-voltage IGBTs". In: *Microelectronics (MIEL), 2012 28th International Conference on*. IEEE. 2012, pp. 243–250.

[100] Gilles Rostaing et al. "Reliability of power MOSFET-based smart switches under normal and extreme conditions for 24V battery system applications". In: *Microelectronics Reliability* 53.9 (2013), pp. 1703–1706.

[101] Stefano de Filippis et al. "ANSYS based 3D electro-thermal simulations for the evaluation of power MOSFETs robustness". In: *Microelectronics Reliability* 51.9 (2011), pp. 1954–1958.

[102] G De Falco et al. "ELDO-COMSOL based 3D electro-thermal simulations of power semiconductor devices". In: *Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), 2014 30th Annual*. IEEE. 2014, pp. 35–40.

[103] Mentor Graphics. *ELDO*. Wilsonville, Oregon, USA: Mentor Graphics, 2014.

[104] AEC-Q101 006 REV. *Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems*. Automotive Electronics Council. Sept. 2006. URL: `http://www.aecouncil.com/AECDocuments.html`.

[105] B Jayant Baliga. "An overview of smart power technology". In: *Electron Devices, IEEE Transactions on* 38.7 (1991), pp. 1568–1575.

[106] G Breglio et al. "Electro-thermal instability in low voltage power MOS: experimental characterization". In: *Power Semiconductor Devices and ICs, 1999. ISPSD'99. Proceedings., The 11th International Symposium on*. IEEE. 1999, pp. 233–236.

[107] P Spirito et al. "Analytical model for thermal instability of low voltage power MOS and SOA in pulse operation". In: *Power Semiconductor Devices and ICs, 2002. Proceedings of the 14th International Symposium on*. IEEE. 2002, pp. 269–272.

[108] Paolo Cova, Nicola Delmonte, and Roberto Menozzi. "Thermal characterization and modeling of power hybrid converters for distributed power systems". In: *Microelectronics Reliability* 46.9 (2006), pp. 1760–1765.

[109] G. Romano et al. "An ultrafast IR thermography system for transient temperature detection on electronic devices". In: *Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), 2014 30th Annual*. Mar. 2014, pp. 80–84. DOI: `10.1109/SEMI-THERM.2014.6892219`.

[110] Simon M Sze and Kwok K Ng. *Physics of semiconductor devices*. John Wiley & Sons, 2006.

Chapter 3: Experimental characterization of Blocking Characteristics of Power Semiconductor Devices

The blocking I-V characteristic of a power device plays an important role in the definition of the device behaviour in avalanche condition. Recent works have been shown that such a characteristic let to predict physical phenomena as well as failure mechanisms that takes places into the device when it experiments avalanche breakdown [1, 2]. As already pointed out in 2.2.1, instability can arise that is indicated by the presence of a Negative Differential Resistance region. In particular, either the width of this region and the current boundaries determine weather the device is likely to experience harmful avalanche transients and therefore they give an indication of the avalanche ruggedness. Recent works have also underlined that the I-V blocking characteristic of T-IGBT is somehow dependent on the gate drive potential [3]. In particular, the shape of the characteristic changes if the gate is switched off to 0 V or to -15 V. In this section, a system to measure the I-V blocking characteristic of a power device is presented, and it is applied to the measurements of Power MOSFETs and IGBTs characteristics.

3.1 Measuring of Blocking Characteristic: The Transmission Line Pulse (TLP) Test

From what said, it is evident that, in order to achieve a prediction of power device avalanche behaviour, the measurement of its blocking characteristic is mandatory. The measuring process, however, is not immediate as it is important to guarantee that the device temperature is constant along all the measurement. As a consequence, the temperature

must be imposed externally and the self heating off the device must be negligible. Hence, the measurement cannot be performed by running UIS test, because the relative duration of a UIS test goes from hundreds of microseconds to several milliseconds, and for this durations the self heating effect cannot be neglected. What is more, due to the linear decreasing slope of the current in the UIS test, it is uneasy to measure the current and the voltage with a sufficient accuracy. The best solution consists to apply to the device short, rectangular pulses of current in order to avoid a significant self heating of the device. To this purpose, the pulses width must be comprised in a range of hundreds of nanoseconds, that is a value hundreds times lower than the one of a common UIS test. In order to achieve this pulses the best solution is to use a Transmission Line Pulse system, which is largely used to test the ESD capability of integrated circuit [4, 5].

Transmission Line Pulsing (TLP) system was first presented by Maloney et al. [6] in 1985 as a new method to measure the ruggedness of the integrated circuit to electrostatic discharges (ESD). During following years, several modifications have been proposed to the original TLP circuit. In [7], a classification of several topologies of TLPs is presented, classified in base of impedance, multiple reflections, and position of the probe for measuring current and voltage. In particular, a first classification is made by considering whether the topology acts with constant current or constant impedance. The first topology uses a resistor in the order of megaohms to produce a current which is independent on the variations of DUT impedance, while the second category consists of three topology in which differences are in weather reflected wave or transmitted one or both are measured. Particular considerations are required when the system is used for the characterization of power devices. In this case, the current values which are significant for the applications are much larger than the one measured in ICs and the breakdown voltage are even more larger. As a consequence, the system must be adapted for high power application.

The typical circuit of a TLP systm is depicted in Figure 3.1. The circuit operation can be divided in two part, according to the state of the switch S_1. When S_1 is in the off state, then the the application of the supply voltage charges the transmission line to the voltage V_s. In this phase, the series between the switch and the DUT must sustain the primary voltage of the transmission line and therefore the switch maximum voltage must

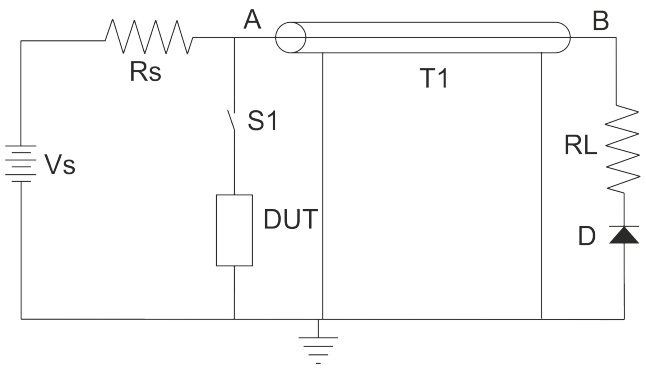


Figure 3.1: Circuit of Transmission Line Pulse test.

satisfies the following relation:

$$V_{sw,max} \leq V_a(t) - V_{DUT,max}. \tag{3.17}$$

The second port of the transmission line is closed on to the series of a matched resistance and a diode and in this operation is considered as an open load. At the end of this phase, whose duration depends on to the impedance of the line and the resistance R_S, the potential of the node A reaches the value of V_S. The second phase starts as the switch is closed: in this case the circuit becomes the one depicted in Figure 3.2a with the charge accumulated by the transmission line which discharges on to the DUT, supposed in off state, and brings it into avalanche. From the equivalent circuit of Figure 3.2b it is clear that the current flowing in this condition can be expressed by the following relation:

$$I_{DUT} = \frac{V_B(t) - V_{BR,DUT}}{R_{LINE}}, \tag{3.18}$$

where R_{LINE} is the internal impedance of the line. From equation 3.18 it follows that there is a linear relation between the current and the supply voltage and the larger is this latter, the larger will be the current.
It is important to underline that, because of the nature of a transmission line, which can be seen as a distributed capacitance, the voltage $V_B(t)$ stays constant during the time needed to the voltage wave produced on to the DUT side to be transmitted to the secondary side and then back again, that is a duration of:

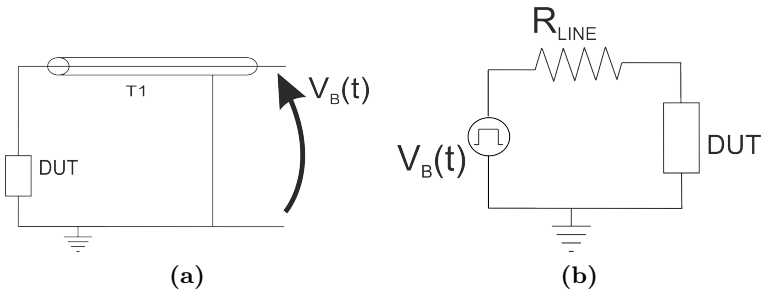


Figure 3.2: a) TLP circuit with switch S_1 open; b) Equivalent circuit.

$$t_{pulse} = \frac{2L}{v_L}, \tag{3.19}$$

being L the transmission line length and v_L its velocity of propagation. By proper choice of the transmission line length, the duration of the pulse can be changed to the suitable value. In this phase, the series of diode and resistance represents a matched load for negative pulses produced by the mismatch between the DUT impedance and the transmission line impedance and it is particularly required for devices with impedance much lower than the transmission line one.
With this basic set up the current is limited by the breakdown voltage of the DUT and therefore the larger it is the breakdown voltage of the device, the larger must be the supply voltage in order to measure the same amount of current. In the following, different solutions are evaluated, by means of SPICE simulation, in order to increase the current capability of the TLP system [8].
The first consideration is made about the choice of the best device used as switch. As a matter of fact, a fast transition is required between the first and the second phase of operation and the switch must turn on in a short time compared to the duration of the pulse, as its resistance is in the path of the current discharging into the DUT. As a consequence, the best option is to use a Power MOSFET which has transition times in the order of tens of nanoseconds. However, the speed is only one requirement as it has already pointed out that another constraint is dictated by its breakdown voltage in order to fulfil the relation in 3.17. For DUT with high voltage rating it is easy to satisfy the requirement with the voltage capability of common Power MOSFET whilst it is more

difficult the lower is the DUT breakdown voltage. For this reason, in low voltage DUT cases an IGBT switch becomes the only workable solution. To that end, a characterization of the effect of the switch on to the TLP pulse is performed.
The circuit simulated is the basic setup shown in Figure 3.1 and in the analysis the switch is implemented by a Power MOSFET (Device 1) and an IGBT (Device 2), both rated at 600 V. The results of the simulation are shown in Figure 3.3 and confirm that the current pulse obtained by using Device 1 is larger than the value of the current pulse corresponding to Device 2. Hence, as soon as the voltage requirements are compatible with commercial devices, a Power MOSFET is preferable with respect an IGBT device.

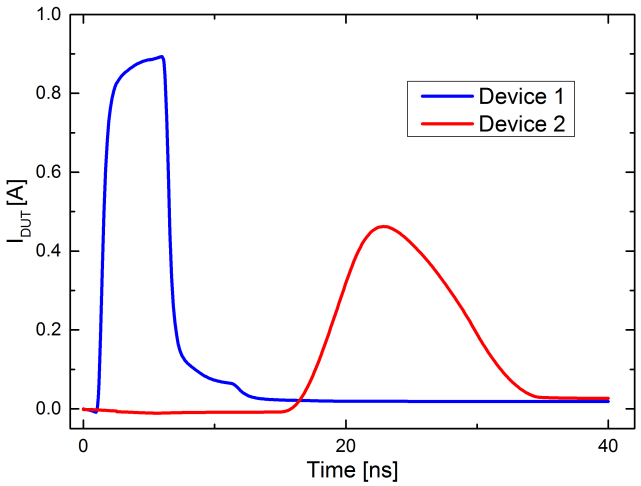
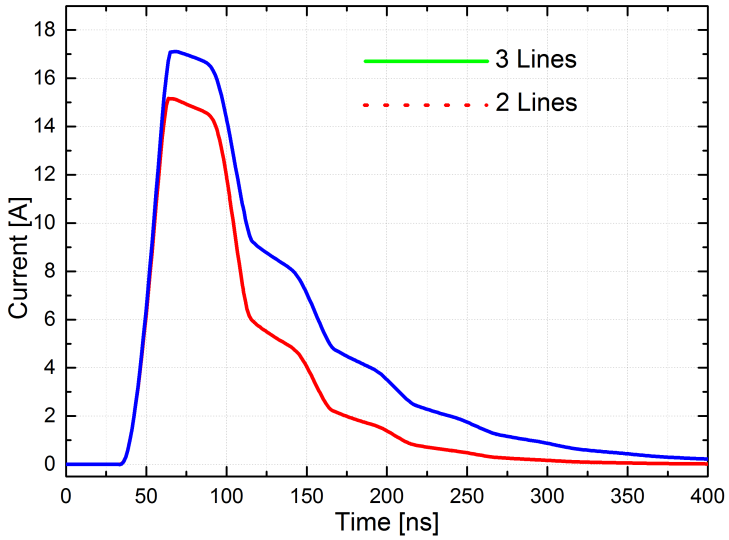
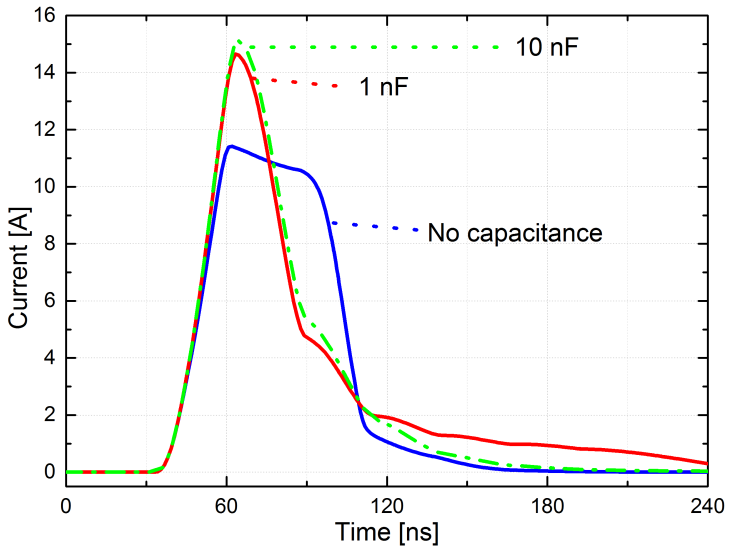


Figure 3.3: Comparison between current pulses obtained by using Power MOSFET (Device 1) or IGBT (Device 2) as switch.

Second consideration concerns the investigation of usage of multiple paralleled transmission line in order to increase the charge stored which directly affects the current pulse. To this end, configurations with two and three paralleled transmission lines are investigated. Results in Figure 3.4a show that the difference between two and three transmission lines are not evident enough to justifies the increased weight and size which would result into using an increased number of transmission lines. A last analysis is conducted by introducing a capacitance in parallel to the transmission line. This solution can be seen as a modification of



(a)



(b)

Figure 3.4: a) Current pulses for two and three paralleled transmission lines; b) Effect of capacitance in parallel to the transmission line on the current pulse.

the previous analysis. The transmission line can be also represented as distributed capacitance. In this case, a concentrated capacitor is used which provides a current boost but with a limited duration, and can be used when the current limit of the TLP system is reached, even with two parallel transmission lines. This solution, however, limits the duration where the current is constant and hence reduces the time useful for the measurements. Pulse waveforms of this last simulation are depicted in Figure 3.4b. Here, two values of capacitance are considered, namely 1 nF and 10 nF, in order to find the best capacitance value. As it can be shown, the parallel of the capacitance and the transmission line increases in fact the current value. However, the difference between the two value is not significant whilst the modification of the pulse shape is quite relevant, as already presumed.
Simulations are performed combining two transmission lines and a capacitance in order to validate the hypotheses developed so far. In Table 3.1, are summarizes the positive and negative aspects of these solutions.

	1 T-Line	2 T-Lines in parallel	2 Series T-lines	2 T-Lines with capacitance
Pulse shape	Flat	Slightly distorted	Very flat	Highly distorted
Current capability	Medium	Medium/High	Poor	High current peak

Table 3.1: Combination of transmission lines and capacitance available.

A circuit has been realized recalling the basic configuration of the TLP. By means of additional switch all the configuration listed in Table 3.1 can be arranged. The highest value reachable for the supply voltage is 2000 V. According to the voltage constraint of the switch, two devices are used according to the breakdown voltage of the DUT which has to be tested. In particular, for DUT of breakdown voltage up to 600 V, it has been used an 1200 V IGBT (TOSHIBA GT25Q101), while, for higher breakdown voltage DUT has been used a CoolMOS rated at 650 V (Infineon 20N60C3).
A first measurement is performed on to a low voltage DUT, namely a

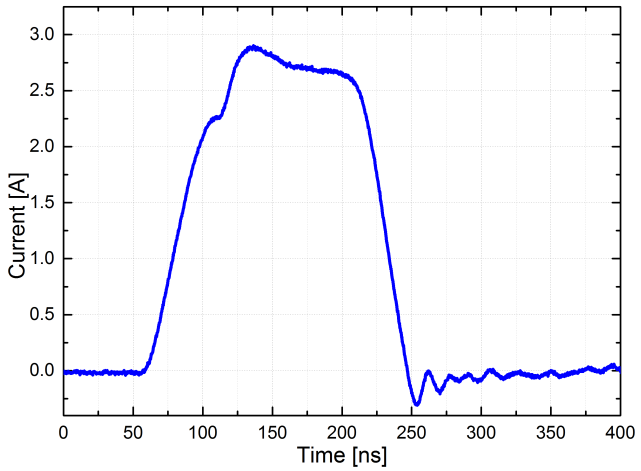


Figure 3.5: Experimental current pulse on a 30 V Schottky diode DUT.

30 V Schottky diode, to verify the correctness of the operations of the TLP. In this experiment, the supply voltage is set to 100 V, and the CoolMOS Power MOSFET is used as switch, due to the low supply voltage. Also, a single line with capacitance of 1 nF is used. The resulting pulse waveform is depicted in Figure 3.5 and it can be seen that the pulse shape is reasonably square and the width is of 200 ns.

Once the effectiveness of the circuit is validated, the setup can be used for evaluation of I-V blocking characteristics of power devices.

3.1.1 I-V blocking characteristic of a Power MOSFET

A 500 V PowerMOSFET I-V blocking characteristic has been measured at four different operating temperatures, namely 30 °C, 50 °C, 75 °C and 100 °C. In Figure 3.6 are reported the avalanche characteristics of this device. The maximum current reachable for this device is 20 A, at ambient temperature, after that the device fails. In the observed current range, the considered Power MOSFET, shows mainly a positive differential resistance (PDR) trend as provided by the theory.

3.1.2 I-V blocking characteristic of an IGBT

The I-V blocking characteristic of a 1200 V Trench IGBT has been also measured. Measurements results are reported in Figure 3.7. Due to

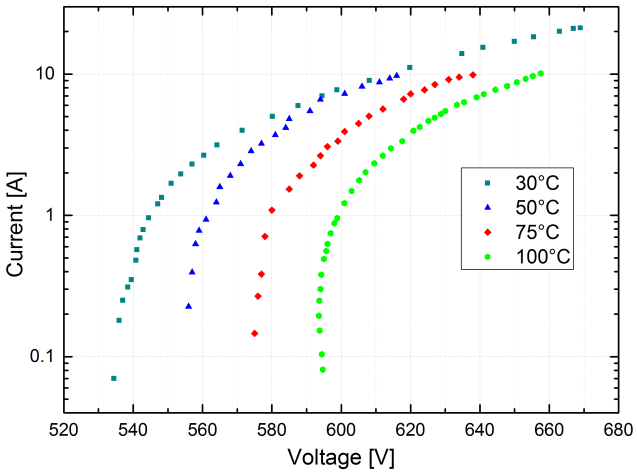


Figure 3.6: Experimental I-V blocking characteristics of a 500 V Power MOSFET DUT at 30 °C, 50 °C, 75 °C and 100 °C.

the high breakdown voltage, the maximum current obtained is 10 A. However, in the measured current range, the IGBT exhibits a Negative Differential Resistance behaviour, particularly prominent at 75 °C and 100 °C. For these temperatures the device suffer of thermal instability and, in fact, it has failed during the measurements at 100 °C.

3.1.3 Effect of the cell pitch on the distribution of current during avalanche operation of Trench IGBT

The TLP circuit has been also used for evaluating the characteristic of two families of 1200 V Trench Field Stop IGBTs, based on the same technology, but with different pitch geometries, that is with different distance between two consecutive trenches. In particular, Device B has been designed with a pitch doubled with respect the Device A. The measurement of the I-V blocking characteristic is shown in Figure 3.8. It can be noted that in the case of the double-pitch structure the breakdown voltage is lower and the transition to positive differential resistance (PDR) is shifted at very low current. As a consequence, Device A shows a wider NDR region and it is expected to present a lower avalanche ruggedness than device B. This assumption has been proved by UIS measurements conducted on both the devices and importance of the cell pitch on the avalanche ruggedness has been carried out [9].

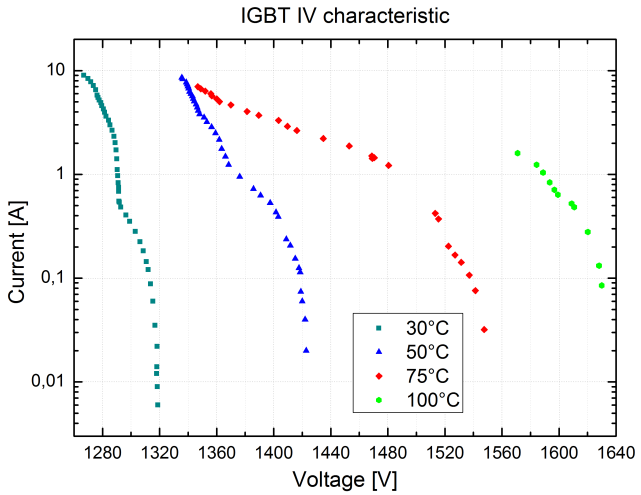


Figure 3.7: Experimental I-V blocking characteristics of a 1200 V IGBT DUT at 30 °C, 50 °C, 75 °C and 100 °C.

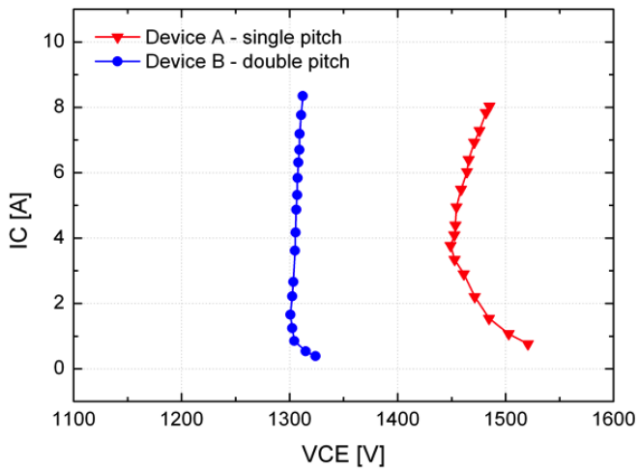


Figure 3.8: Experimental I-V blocking characteristics of Device A (single pitch) and Device B (double pitch).

3.2 Conclusions

In this chapter experimental analysis of the I-V blocking characteristic has been carried out. In particular, a TLP system which is capable of generating short, flat pulses of current has been implemented.
By means of this setup, the I-V blocking characteristics of a Power MOSFET and an IGBT have been measured in order to confirm the theoretical and simulation results widely diffused in scientific literature. In particular, the IGBT has shown to have a NDR region in the characteristic which limits the avalanche ruggedness whilst the Power MOSFET has confirmed to be a more robust device presenting PDR trend for the same current range.
Finally, the TLP circuit has been used to validate the effect of the geometry of two IGBTs belonging to two families which have different cell pitches. The results have shown that the device with double pitch geometry experiments the avalanche breakdown for a lower voltage but presents a smaller NDR region and this make it to be much more rugged for avalanche operations. This results have been also confirmed by UIS test conducted on both the device.

3.3 References

[1] Giovanni Breglio et al. "Experimental detection and numerical validation of different failure mechanisms in IGBTs during unclamped inductive switching". In: *Electron Devices, IEEE Transactions on* 60.2 (2013), pp. 563–570.

[2] S Huang et al. "An experimental and numerical investigation of IGBT blocking characteristics". In: *Power Electronics and Motion Control Conference, 2000. Proceedings. IPEMC 2000. The Third International*. Vol. 1. IEEE. 2000, pp. 407–411.

[3] M Riccio et al. "Impact of gate drive voltage on avalanche robustness of trench IGBTs". In: *Microelectronics Reliability* 54.9 (2014), pp. 1828–1832.

[4] G Meneghesso et al. "ESD robustness of smart-power protection structures evaluated by means of HBM and TLP tests". In: *Reliability Physics Symposium, 2000. Proceedings. 38th Annual 2000 IEEE International*. IEEE. 2000, pp. 270–275.

[5] Leo G Henry et al. "Transmission-line pulse ESD testing of ICs: A new beginning". In: *Compliance Engineering, http://www.ce-mag. com/ce-mag. com/archive/01/03/0103CE_046. html* (2001).

[6] TJ Maloney and N Khurana. "Transmission line pulsing techniques for circuit modeling of ESD phenomena". In: *proc. EOS/ESD symp.* Vol. 7. 1985, pp. 49–54.

[7] Steven H Voldman et al. "Standardization of the transmission line pulse (TLP) methodology for electrostatic discharge (ESD)". In: *Electrical Overstress/Electrostatic Discharge Symposium, 2003. EOS/ESD'03.* IEEE. 2003, pp. 1–10.

[8] Michele Riccio et al. "Transmission line pulse system for avalanche characterization of high power semiconductor devices". In: *SPIE Microtechnologies*. International Society for Optics and Photonics. 2013, 87640U–87640U.

[9] M Riccio et al. "Cell pitch influence on the current distribution during avalanche operation of trench IGBTs: Design issues to increase UIS ruggedness". In: *Power Semiconductor Devices & IC's (ISPSD), 2014 IEEE 26th International Symposium on*. IEEE. 2014, pp. 111–114.

Appendix A: Dynamic Avalanche Simulation of High Voltage Trench FS-IGBT

Application engineers require robust power semiconductors in order to get the most out of their converters. One important issue is to avoid electrical device overstress due to extreme switching situations. For this reason, in high power demanded applications, the trend is to slow down the operation frequency and transition times in order to avoid overvoltage and over current spikes onto the devices during transitions [1]. Unfortunately, the reduction of switching times leads to higher power dissipation and dynamic stresses. What is more, larger space occupation is due to increased size of reactive components. It could be advantageous to reduce the switching time and let the device to experiment these rare overstress events. Modern power devices are often capable to withstand sporadic overstresses produced by extreme switching conditions. Even if the capability of power devices has been proved by relevant experimental result [2], nonetheless there are a lot of doubts about if the accumulation of multiple high stresses over the time could produce a long term degradation on the device. One of the most important effect which could limits the long term reliability of a power device is the occurrence of dynamic avalanche phenomenon during the turn-off transition, a phenomenon particularly relevant for high voltage devices where the voltage slope is very steep. Dynamic avalanche regime has been studied for different devices families [3, 4] up to more recent works on IGBT devices, both planar structures [5] and Trench structures [6, 7]. Most analyses show that dynamic avalanche as well as static avalanche can be an unstable phenomenon which can lead, in some cases, to creation of filaments of current during the turn-off of the circuit [8]. According to whether the filament is moving or not, the device is likely to survive or to be harmed during the voltage transition. A

previous work conducted on GTOs [3] has been demonstrated that the occurrence of a filament has effects on the external voltage and therefore an experimental evidence of the filamentation has been observed. Similar results have been shown in [5] on planar IGBT, where the collector voltage exhibits several glitches when filament is formed in the structure. In this contribution we analyze, by means of TCAD simulations, the effects of the filamentation in a high voltage T-IGBT on to the collector voltage when the dynamic avalanche occurs, in order to understand if the same effects on the external voltage can be observed in this kind of device.

A.1 Simulation Conditions and Physical Description of The Structure

TCAD simulations by means of DESSIS Suite has been conducted on a 6.5 kV Trench IGBT structure. For taking into account the effect of filamentation, a multicellular structure, composed by array of cells, is considered. Thermal crosstalk among nearest neighborhood cells as well as lateral coupling effect on the physics must be taken into account, therefore the structure is an integrated IGBT with multiple equal cells physically connected. Turn-off simulation is performed in two steps. The first simulation brings the device in the steady state condition: the gate is raised to 15 V and then the collector is ramped up to the desired current value in each case as quasi-stationary simulation. With this pre-simulated device the main turn-off simulation is performed in a second transient simulation in mixed-mode.
The SPICE schematic adopted to simulate the turn-off of the device is reported in Figure A.1. The Area Factor parameter of the device has been chosen in order to have an equivalent area of $1\,\mathrm{cm}^2$ and the other components have been scaled accordingly to the real area of the module. Finally, the model of Van Overstraeten and DeMan has been used for modeling the impact ionization in the structure.

A.2 Simulation Results

Dynamic avalanche operation A first turn-off simulation has been performed with a current value of $57\,\mathrm{A/cm}^{-2}$ and with a battery voltage of 3300 V. The gate voltage is switched from 15 V to −15 V. For analyzing the worst case switching condition, no external gate resistance has

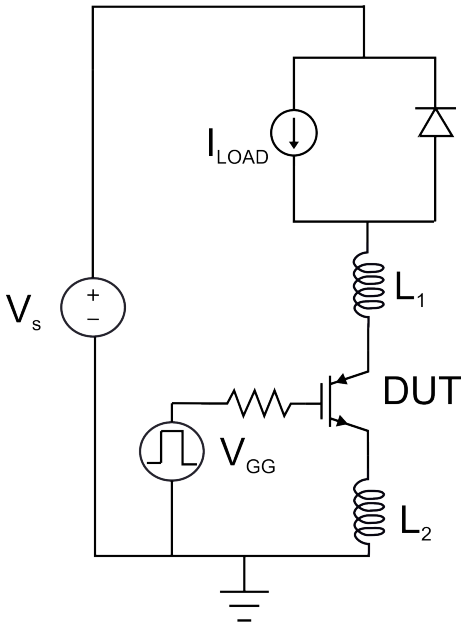


Figure A.1: Turn-off circuit for mixed mode simulations. DUT in red is simulated with FEM simulation.

been consider but a resistance of 100 mΩ has been included for the parasitic resistance of the wires. The total value of the inductance L2 has been set to 2.9 µH. Resulting waveforms of this simulation are shown in Figure A.2.
It can be seen that when the collector voltage reaches a value of approximately 2000 V, the gradient lowers because of the inset of dynamic avalanche [8]. No other effect can be evinced form the collector voltage waveform. Even if present, dynamic avalanche phenomenon has no different effects with respect to the results obtained with single cell simulation.

Onset of current filamentation From Wachutka [9], the onset of filaments is strictly related to instability in the structure: in this case, even a slight difference (for example a difference in the mesh) can be amplified and leads to non-uniform current distribution. The instability appears at higher level of charge concentrations because of the bending of the electric field profile inside the structure, which finally turns in

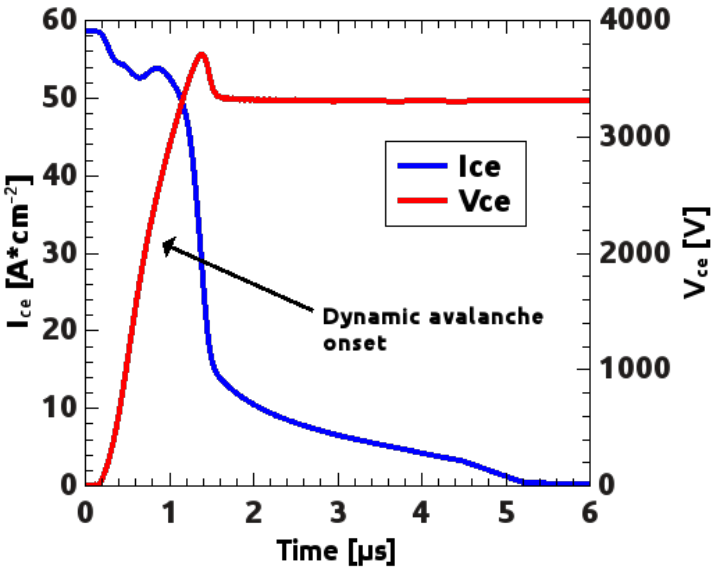


Figure A.2: Collector voltage and current during turn-off: 58 A, 3.3 kV.

negative differential resistance in the I-V reverse characteristic. This effect is usually shown at very high current density [3].

For this reason, simulation has been performed by increasing the initial current up to values of 120 A/cm^{-2}. Also, the battery voltage has been raised to 4000 V in order to extend the turn-off duration. Figure A.3 reports the collector voltage and current for the simulation at 120 A/cm^{-2}. The effect of dynamic avalanche is clearly visible after 200 ns when collector voltage reaches a value slightly higher than 1000 V. At the time of 1 µs, the collector voltage exhibits an abrupt reduction of slope which only lasts for few nanoseconds and then it returns to rise with the same gradient as before. This glitch of voltage is determined by an increasing charge concentration inside the structure, and it is the indication of filamentation occurring in the structure. Even if present, this modification of the external voltage is not clearly evident, especially if compared to the glitches reported in the previous works. This uncertainty, related to whether the filament is created or not, is very dangerous because in fact the current can shrink to a filament during the turn off and there are no chances to see it from the experiment, apart if the device fails

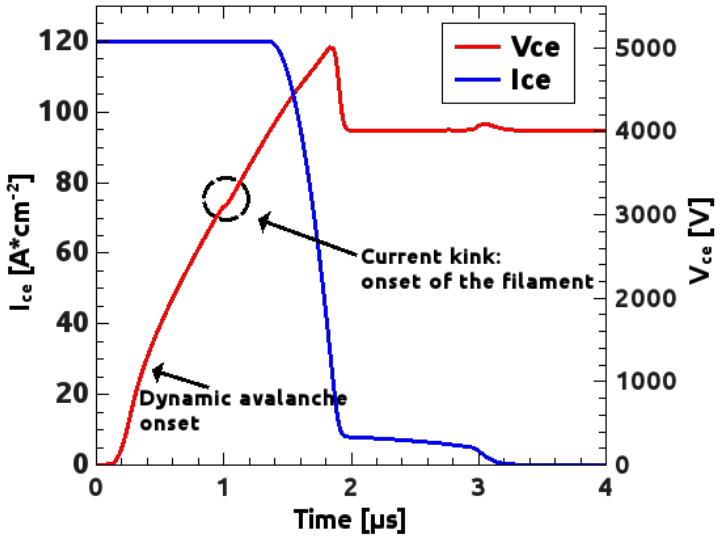


Figure A.3: Collector voltage and current during turn-off: 120 A, 4 kV.

for the very high current density. The conduction current density is reported in Figure A.4, where the filament on the right side of the device is clearly visible. Its evolution along the time is shown in Figure A.5a. In particular, a filament is formed at the emitter side of the structure and remains in the same position for the all turn-off transient. The temperature profile along the structure is shown in Figure A.5b during time, taken under the trench, and it increases up to a value of 426 K in correspondence of the filament, staying at a value of nearly 410 K in the remaining structure. The ripple of the current and temperature is related to the periodic nature of structure as it is composed of more elementary cells.

In order to extend the analysis to higher current density, a third simulation has been performed with an initial current density of 300 A cm^{-2}. Figure A.6a and A.6b summarize the result obtained.

From the current density distribution during the time, again taken at a depth of 10 µm (Figure A.6a), it is still visible the appearing of a filament at the centre of the structure, even after a short time of 620 ns. In this case, nevertheless, the filament walks out during the time towards the edge of the structure. The explanation of this phenomenon can be given by looking at the temperature profile in the structure, shown in

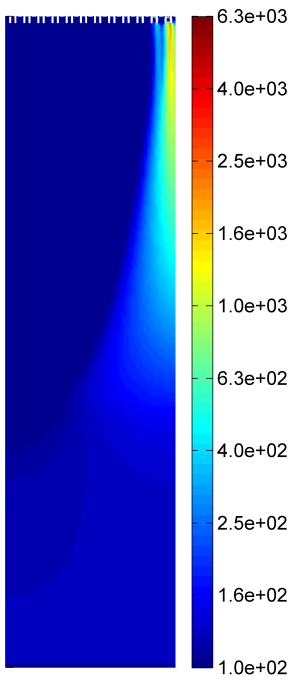
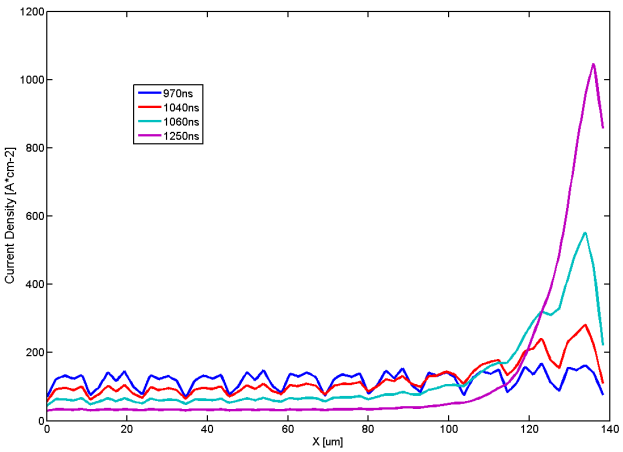


Figure A.4: Filamentation of the current. Conduction current density in the structure.

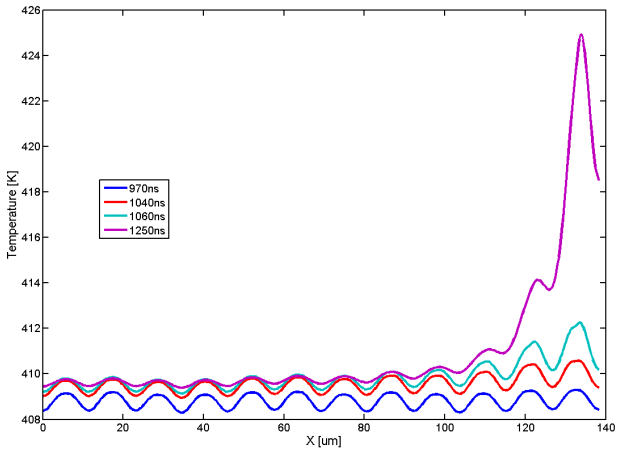
Figure A.6b. As one can see, the filament is moving away from the place where temperature increases: this is because the impact ionization phenomenon is inversely dependent on the temperature [4]. The filament starts to move when the temperature reaches a value of nearly 440 K and this is the explanation why the movement is not visible in the previous case. Even if the current is filamenting in the structure, this time there is no evidence of this effect on the voltage waveform (Figure A.7). This could be related either to the movement of the filament or to the position where the filament appears.

A.3 Conclusion

In this section, dynamic avalanche behaviour of high voltage multicellular Trench-IGBT structure has been investigated, with the support of TCAD simulations, in order to analyse the filamentation phenomenon



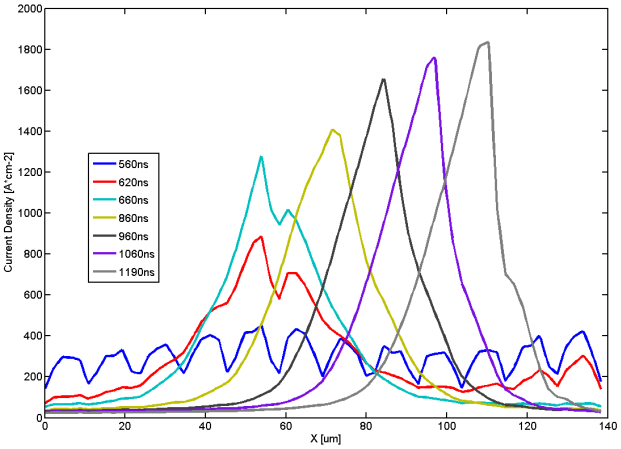
(a)



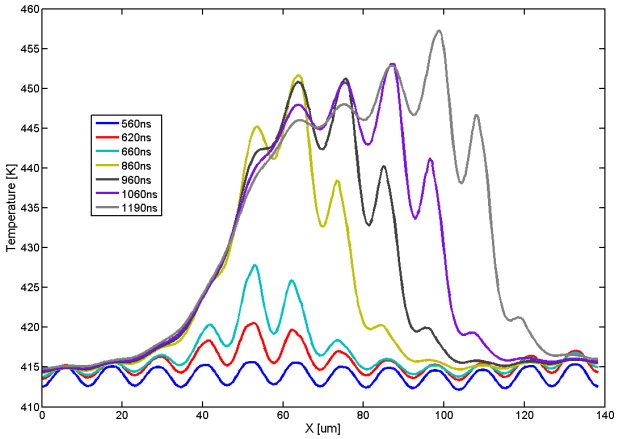
(b)

Figure A.5: Initial current of 120 A/cm^{-2}. Cross section at 10 µm of depth, at different times. a) Current density. b) Temperature.

and to understand possible influence on the external electrical waveforms. According to the current densities the device must turn-off, non uniform current distribution along the device can be reported. In partic-



(a)



(b)

Figure A.6: Initial current of $300\,\mathrm{A/cm^{-2}}$. Cross section at $10\,\mu\mathrm{m}$ of depth, at different times. a) Current density. b) Temperature.

ular, the current shrinks to a narrow filament and as a consequence, the current density becomes very high. A first simulation, where the device switches off a current of $120\,\mathrm{A\,cm^{-2}}$ has shown that the increased local charge concentration in the structure, due to the filamentation, produces

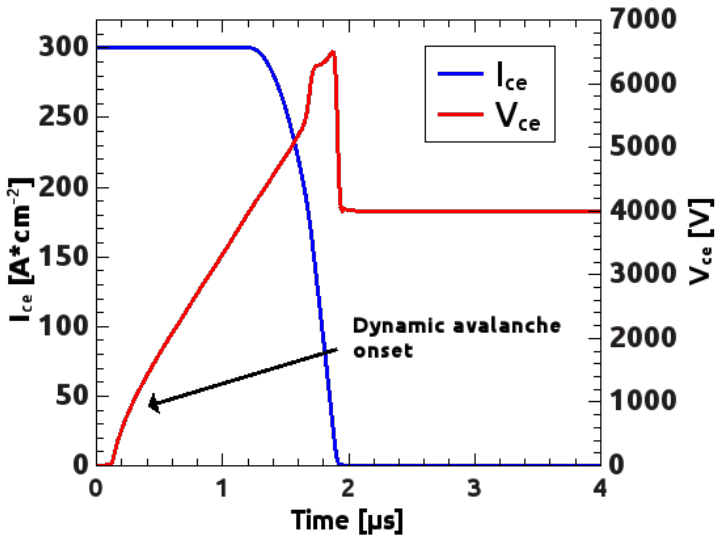


Figure A.7: Collector voltage and current during turn-off: 300 A, 4 kV.

a modification of the rising steepness of the external collector voltage. For higher current densities different behaviour has been found. In fact, a simulation with an initial current of 300 A cm^{-2}, the appearing of the filament does not produce any effect of the external collector voltage. As a consequence, from what has been evinced by the simulation, there are not clear modifications on the external collector voltage which give the indications that a filament of current actually occurs in the structure.

A.4 References

[1] H. Schlangenotto and H. Neubrand. "Dynamic Avalanche during turn-off of GTO-thyristors and IGBTs". In: *Electrical Engineering* (1989).

[2] A Wacker and E Schöll. "Criteria for stability in bistable electrical devices with S-or Z-shaped current voltage characteristic". In: *Journal of applied physics* 78.12 (1995), pp. 7352–7357.

[3] J Oetjen et al. "Current filamentation in bipolar power devices during dynamic avalanche breakdown". In: *Solid-State Electronics* 44.1 (2000), pp. 117–123.

[4] F-J Niedernostheide et al. "Periodic and traveling current-density distributions in high-voltage diodes caused by avalanche injection". In: *Power Electronics and Applications, 2005 European Conference on*. IEEE. 2005, 10–pp.

[5] Petra Rose et al. "Investigations on the stability of dynamic avalanche in IGBTs". In: *International symposium on power semiconductor devices & ICS*. 2002, pp. 165–168.

[6] B. Heinze et al. "Ruggedness of high voltage diodes under very hard Commutation Conditions". In: *Power Electronics and Applications, 2007 European Conference on*. Sept. 2007, pp. 1–10. DOI: 10.1109/EPE.2007.4417776.

[7] Andreas Müller-Dauch et al. "Source side thermal runaway of trench IGBTs, dependence on design aspects". In: *Power Semiconductor Devices and IC's, 2006. ISPSD 2006. IEEE International Symposium on*. IEEE. 2006, pp. 1–4.

[8] Josef Lutz and Roman Baburske. "Dynamic avalanche in bipolar power devices". In: *Microelectronics Reliability* 52.3 (2012), pp. 475–481.

[9] Gerhard K Wachutka. "Analytical model for the destruction mechanism of GTO-like devices by avalanche injection". In: *Electron Devices, IEEE Transactions on* 38.6 (1991), pp. 1516–1523.