TESI DI DOTTORATO

UNIVERSITÀ DEGLI STUDI DI NAPOLI "FEDERICO II"

DIPARTIMENTO DI INGEGNERIA ELETTRICA E
DELLE TECNOLOGIE DELL'INFORMAZIONE

DOTTORATO DI RICERCA IN
INGEGNERIA ELETTRONICA E DELLE TELECOMUNICAZIONI

COMPACT ELECTRO-THERMAL MODELING OF IGBT FOR APPLICATION CIRCUIT EFFECTIVE DESIGN

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A. A. 2013–2014

"If something can not be expressed in numbers, it's not science: it's opinion."
(Robert Anson Heinlein)

"There is only a means to advance science: contradict the science already constituted."
(Gaston Bachelard)

"In questions of science, the authority of a thousand people is not worth as much as the humble reasoning of a single individual."
(Galileo Galilei)

Acknowledgments

This work has been carried out as part of the collaboration between Department of Electrical Engineering and Information Technologies (DIETI) of University of Naples "Federico II" and the "Vishay Intertechnology (Diodes Division)".
My special thanks are addressed to my supervisor Professor Giovanni Breglio for the effective advices and teachings during our talks and to Professor Andrea Irace for its precious support.
Many thanks also to Michele, Luca e Giuseppe who always encouraged and assisted me with their great enthusiasm and passion.
Furthermore, a special thank goes to "Vishay Semiconductor Italiana" for laboratory equipments, sample devices and any sort of appliances which made all the activities possible. In particular, I would like to thank Vishay people, Luigi, Nabil, Davide, Rossano, Carmelo, Marco, Enzo, Filippo and our dear Annamaria for supporting me with their great knowledge and experience in power devices development and characterization during my period there.

Domenico Cavaiuolo

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Introduction

Nowadays, power semiconductor devices are recognized to be the key components of all power electronic systems aimed to a more effective management of the energy flow and conversion, since concerns towards environmental issues are becoming of crucial relevance. As a result, power electronics is invading the modern society with an increasingly number of applications which serve all areas of human life, such as transportation, household appliances, aerospace, industry and telecommunications. In this scenario, IGBT (Insulated Gate Bipolar Transistor) plays an important role being the preferred power device for medium/high power applications due to their excellent performances and features. The rapid development in IGBT technology is leading to a growth of interest in device modeling, since it is necessary to thoroughly understand IGBT operation in modern power converters in order to optimize its design. Whereby, the use of CAD tools and their simulation results has become necessary both for IGBT design parameters investigation even prior to fabrication and for analysis of device electro-thermal behaviour in circuit applications. As part of the CAD methodology, *compact modeling* refers to the development of models for power semiconductor devices used mainly in SPICE-based circuit simulators: they are aimed to properly reproduce device electrical behaviour with accuracy, computational efficiency and ease of parameter extraction for a circuit or system-level simulation. In particular, IGBT SPICE compact models are strongly required by device and circuit designers, and this justifies the efforts of both industrial world and scientific research community to look for more accurate and time-efficient compact models, as technology advances. This dissertation deals with the PSpice optimized implementation of an improved IGBT electro-thermal model based on the Kraus model, aimed to represent a useful and effective tool for effective design of IGBT circuital applications. This purpose is pursued by means of both simulation and experimental results, which are critically analysed and compared to demonstrate benefits brought by model enhancements in terms of accuracy,

speed and convergence. Moreover, the modeling of Field-Stop layer is developed for Kraus-based model in order to reproduce some features typical of the modern FS IGBT technology.

Thesis contents

The thesis focuses on the development of a PSpice IGBT electro-thermal model, starting from the model proposed in literature by Kraus, and on its use in predictive simulation analysis of IGBT behaviour within circuital applications. The work is divided into five chapters plus three appendices, and the outline is the following:

Chapter 1 deals with a brief excursus on main power semiconductor devices and their application in power electronics. The most important theoretical approaches and strategies for the modeling of power semiconductor devices are reported. Hence, a six-level classification based on model increasing complexity is presented, with reference to their application in TCAD and ECAD simulators. In particular, an optimum trade-off between device physics approximation and model simplicity is achieved with compact models, which are intended to be implemented into SPICE circuit simulators to be effectively used by both device and circuit designers.

Chapter 2 deals with the description of the main aspects of IGBT physics and technological structures, with particular focus on its steady-state and transient operation modes, which determine device electrical behaviour in circuit applications. Then, the state of art in the field of IGBT compact modeling is presented: a huge number of IGBT behavioural, mathematical and semi-mathematical models have been proposed in literature over the years. They are mainly compared in terms of accuracy, speed and convergence properties and unfortunately only two models are actually implemented within SPICE simulators as built-in library: the NIGBT model, based on the Hefner model included in PSpice OrCad and the HiSIM model implemented in ELDO SPICE. Furthermore, some IGBTs manufacturers provide itself SPICE sub-circuits to simulate their products, where a drastic trade-off between convergence and accuracy is present. In this scenario, the semi-mathematical model proposed by Kraus seems to be the best choice to develop an enhanced and optimized PSpice IGBT model for electro-thermal simulations, since it offers good trade-off between accuracy and speed with relative low complexity.

Chapter 3 deals with the development steps to implement into PSpice

OrCAD simulator an improved and optimized version of the Kraus Non-Punch-Through IGBT model suitable for electro-thermal device simulations. First of all, some enhancements to increase model accuracy respect to the initial Kraus model version are pursued: in particular, the PiN injection effect responsible for reduction of on-state voltage in IGBT devices, is properly modelled by adding a parameter that increases Mosfet electron current in linear region, as formulated in the Hefner model. Moreover, a more accurate expression of conductivity modulated base resistance and the Miller's model for avalanche breakdown are implemented too. Therefore, the temperature dependencies of semiconductor physical parameters are considered in case of TIGBT and some circuital modifications are performed to allow electro-thermal simulations by defining the temperature as a network voltage node. The so-constructed model is then validated on a commercial IGBT device: the set of model parameters is defined by means a proposed parameters calibration procedure based on curve-fitting method and implemented in MATLAB environment (Appendix B). The comparison performed between experimentally measured IGBT DC and transient characteristics and simulation results shows the improvements in both accuracy and convergence gained with proposed model respect to model provided by manufacturer, even at different operating junction temperature values.

Chapter 4 deals with the use of the optimized and improved PSpice IGBT model for predictive analysis of device electro-thermal behaviour within application circuits. As case-studies three different scenarios are considered both in laboratory experimental measurements and in PSpice simulations: the first application concerns the short-circuit test performed in order to investigate IGBT capability to sustain high voltage and current conditions for a certain time interval. In fact, circuit designers are very interested in device short-circuit response at different conditions in order to optimally design electrical and thermal circuit parameters. Furthermore, the second situation is related to the IGBT operation within a DC-DC step-down converter, where device power dissipation strongly affects the converter efficiency determining the choice of an IGBT rather than another. Finally, a more complex circuit application concerns the design of an IGBT short-circuit protection circuit and the definition of its main parameters: since the SC protection strategy is usually embedded into IGBT gate-drivers, circuit designer needs only to choose some external components according to rough design rules which don't take into account the peculiarity of the IGBT device used. So, accurate

electro-thermal simulation of IGBT behaviour during, for instance, activation of desaturation SC protection circuit, is fundamental for optimization of the design of most important circuit parameters.

Chapter 5 deals with the extension of the Kraus-based PSpice model to Field-Stop devices, by means the addition of Field-Stop layer physical equations. In particular, the analytical formulation obtained under hypotheses of doping concentration, thickness and carriers injection-level typical of FS technology, is introduced into the Kraus model, by modifying boundary conditions of ADE within the n^- drift region. The most critical points for model development regard the expression of n^- drift region steady-state carriers charge as function of FSL parameters and the synthesizing of the FSL diffusion current continuity equation for FSL carriers charge evaluation by means an equivalent sub-circuit. Eventually, some qualitative simulations are performed to verify model capability to reproduce FS IGBTs typical features, with reference to IGBT single-cell TCAD simulations.

Scientific contributions

The main scientific contributions of this work are the following:

- Collection, organization and analysis of the state of art documentation in the field of IGBT compact modeling.
- Implementation of an improved and optimized PSpice Kraus-based electro-thermal IGBT model for PSpice simulator.
- Construction and verification of laboratory test machine setup for measurement of IGBT static and dynamic characteristics.
- Definition and implementation of a new automated procedure for parameters calibration of SPICE IGBT models, using a MATLAB-PSpice interface.
- Extension of PSpice Kraus-based model to Field-Stop IGBT devices.

Chapter 1

Compact modeling of power semiconductor devices

It's now plain for all that, due to the increasingly dependence of modern society upon electrical appliances for comfort, transportation, and healthcare, which motivate great advances in power generation, power distribution and power management technologies, power devices currently have a major impact on the global economy and energy saving, because they define the cost and the efficiency of power systems. It is estimated that more than half of the total electricity used on the earth is controlled by power devices, and this figure is expected to grow further in the next years, as a consequence of renewable energy sources expansion and developments of semiconductor power devices new technologies. As the physics scale of semiconductor devices decreases and the complexity of the physical structure increases, finer modeling techniques and more accurate models have been developed to be implemented in *TCAD* [1] or *ECAD/EDA* [2] (i.e. SPICE-based electronic circuit simulators). With respect to TCAD modeling in which usually high computational time FEM (*Finite-Element-Method*) analysis is performed to locally solve device physical basic equations, *compact models* implemented within SPICE-based circuit simulators are characterized by optimum trade-off between accuracy and speed and they have low complexity and high flexibility. Although the

[1] TCAD (*Technology Computer Aided Design*) is a branch of electronic design automation that models semiconductor fabrication and semiconductor device operation.

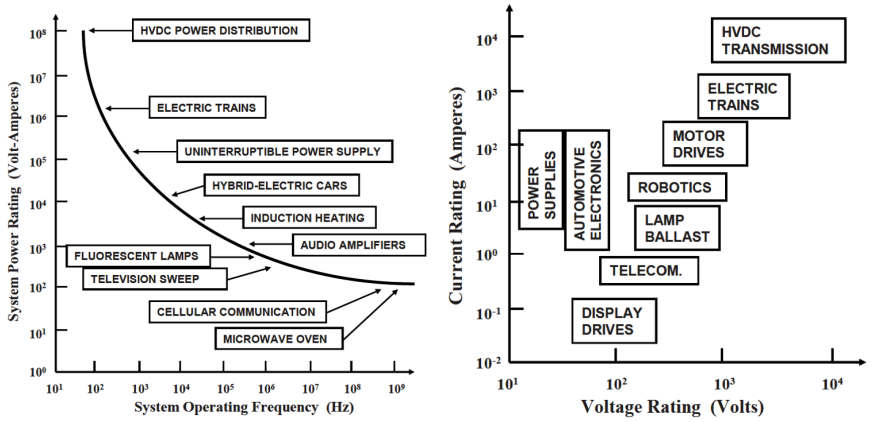
[2] ECAD (*Electronic Computer Aided Design*) or EDA (*Electronic Design Automation*) is a category of software tools for designing and simulating electronic systems such as analog/digital circuits, printed circuit boards and integrated circuits.

main users of these models are still the power system designers, power devices development engineers and researchers are firmly focusing on the use of accurate and robust compact models to investigate the cell-to-cell electrothermal interaction in multi-cellular structure, in order to reproduce and explain physical semiconductor phenomena affecting devices circuit operation and reliability. Since compact modeling is a critical step in the design cycle of modern power devices and systems, it has certainly emerged as the most important vehicle for information transfer from technology fabrication to circuit and product design.

1.1 An overview of power semiconductor devices

Power semiconductor devices constitute the heart of modern power electronic apparatus and are now present in all areas of human life where a use or management of electrical power is necessary. In fact, the largest part of the generated electric energy is consumed after undergoing several transformations, many of them carried out by power electronic converters in which the main portion of the power losses is dissipated by power semiconductor devices. Hence, they are required for systems which operate over a broad spectrum of power levels and frequencies. The main applications for power devices are shown in fig. 1.1a as a function of operating frequency : high power systems, such as HVDC power distribution and traction drives, requiring the control of megawatts of power, operate at relatively low frequencies. As the operating frequency increases, the power ratings decrease for the devices, with typical microwave devices handling about 100 W [1]. Another approach to classification of applications for power devices is in terms of their current and voltage handling requirements, as shown in fig. 1.1b.

Currently, these devices are almost all based on the mature and well established Silicon technology. However, Si exhibits some important limitations regarding its blocking capability, operation temperature and switching frequency. Therefore, a new generation of power devices technology is required for power converters in applications where electronic systems based on traditional Si power devices cannot operate. Among the possible candidates to be the base materials for these new power devices, WBG (*Wide-Band-Gap*) semiconductors such as SiC *(Silicon-Carbide)* and GaN *(Gallium-Nitride)* present a the better trade-off between theoretical characteristics (high-voltage blocking capability, high-temperature operation and high switching frequencies), and real commercial availability of the starting material (wafers) and maturity of



(a) (b)

Figure 1.1: Power electronics applications in a) power-frequency and b) I-V ratings domains.

their technological processes [2]. In fig. 1.2 the limit of Silicon technology in terms of specific on-resistance and blocking voltage is traced and compared with SiC and GaN performances. So, thanks to the superior material properties of WBG semiconductors respect to conventional semiconductors (Si, Ge) which allow operation at higher switching speed, higher voltage and higher temperature, WBG semiconductors power devices are invading the global market as a result of technological improvements and reduction of overall manufacturing cost.

1.1.1 Classification and application

In power electronics applications a semiconductor device operates as an electronic switch: during the steady-state conditions it is properly driven in order not to operate in saturation region, where unacceptable power losses would occur, but in linear-region. Whereby, power devices operate only in two stable modes: the full-conduction mode (ON-state) where the external circuit imposed current is permitted to flow through the device, ideally without any voltage drop across it, and the blocking-mode (OFF-state) when current flow is completely disrupted, and an high voltage is sustained by the device. The transitions between the two states can be induced by the external circuit con-

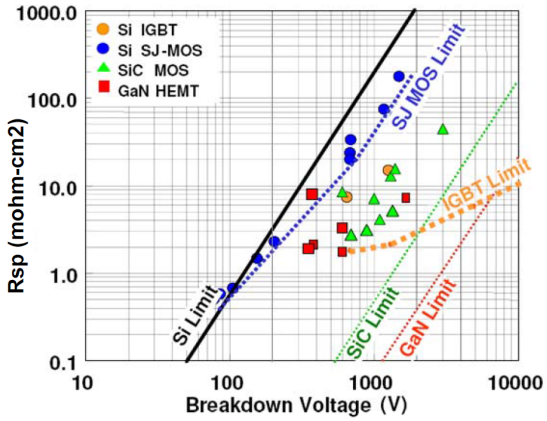


Figure 1.2: Si and WBG semiconductors technological limits.

DEVICE	POLARITY	DIRECTIONALITY	CONTROLLABILITY
Power Diode	bipolar	unidirectional	uncontrollable
TRIAC	bipolar	bidirectional	turn-on controllable
SCR	bipolar	unidirectional	turn-on controllable
GTO	bipolar	unidirectional	turn-off controllable
Power BJT	bipolar	unidirectional	controllable
MCT	bipolar	unidirectional	controllable
Power Mosfet	unipolar	bidirectional	controllable
IGBT	bipolar	unidirectional	controllable

Table 1.1: Classification of main semiconductor power devices.

ditions (i.e. in case of power diodes) or by control circuits and must be as fast as possible in order to minimize the switching power losses. Since the size of power electronics equipment is dramatically decreasing concurrently with the increase of switching frequency, technology efforts are aimed to achieve higher speed transitions by developing new device technologies.

In literature it's possible to come across a number of different criteria for the classification of power semiconductor devices, according to their physical characteristics, modes of operation and controllability properties, which are summarized in table 1.1 in case of main devices:

- TRIAC - **Tri**ode for **A**lternating **C**urrent;
- SCR - **S**ilicon-**C**ontrolled **R**ectifier;
- GTO - **G**ate **T**urn-**O**ff Thyristor;

- BJT - **B**ipolar **J**unction **T**ransistor;
- MCT - **M**os-**C**ontrolled **T**hyristor
- MOSFET - **M**etal **O**xide **S**ilicon **F**ield-**E**ffect **T**ransistor;
- IGBT - **I**nsulated **G**ate **B**ipolar **T**ransistor.

As concerns the field of application served by each power device, it depends on their physical, design, and technological properties to manage high current when is in on-state or high blocking voltage in off-state and to have small losses when making transitions from one state to the other.

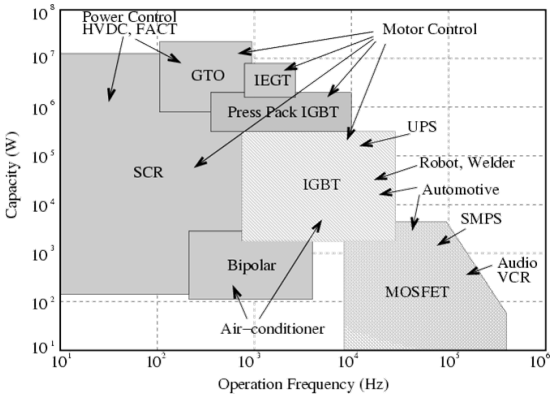


Figure 1.3: Application systems for main silicon power semiconductor switches.

In fig. 1.3 an overview of power system applications served by main power semiconductor switches in the power-switching frequency domain is shown. Three most used categories of devices can be easily identified: thyristors (TRIACs and SCRs) are favored for the low frequency, high power applications, IGBTs for the medium frequency and power applications, and power Mosfets for the high frequency applications. On the high power end of the chart, thyristors are available that can individually handle over 6000 V and 2000 A, enabling the control of over 10 MW of power by a single monolithic device. These devices are suitable for the HVDC power transmission and traction applications. For the broad range of systems that require operating voltages in the range of 300-3000 V with significant current handling capability, the IGBT has been found to be the optimum solution. When the current requirements fall below

1 A, it is feasible to integrate multiple devices on a single monolithic chip to provide greater functionality for systems such as telecommunications and display drives. However, when the current exceeds a few amperes, it is more cost effective to use discrete power Mosfets with appropriate control ICs to serve applications such as automotive electronics and switch mode power supplies. Although the advantages of silicon power devices technology, the development of WBG semiconductor devices is dramatically upsetting this situation, opening up new perspectives not even imaginable until a few years ago.

1.2 Modeling of power semiconductor devices

The rapid developments in semiconductor technology over the past few years have led to a remarkable increase in interest in device modeling. It is necessary to understand the detailed operation of the devices and to optimize their design: this implies that device modeling now plays an essential role in modern technology. As the scale of the semiconductor devices decreases and the complexity of the physical structure increases, the modeling concepts become more complicated. Also, the difficulty connected with measuring some of the semiconductor device's parameters means that the results obtained from the theoretical characteristics must be highlighted. Modeling also allows new device structures to be accurately investigated prior to fabrication. For the development of power semiconductor device models, several physical effects have to be considered with high priority since they dominate the static and dynamic device characteristics [3]. These effects are not described correctly by standard device models (or they are not included at all) because their influence on low-power devices is less important or negligible. An accurate description, however, is essential for power devices. In table 1.2 an overview of the main physical effects and their importance for the different power devices is given.

1.2.1 Resistivity modulation

In order to sustain high blocking voltages, power semiconductor devices have a thick lightly doped semiconductor layer. The resistance of this region determines the voltage drop and power loss when the device is in its conduction mode. This resistance is variable and its dependence on voltage or current can be highly non-linear. In unipolar devices (Mosfet), the variations are caused by variations of the effective current conducting area and by the mobility degradation with an increasing electric field. In bipolar devices (diode, BJT, thyristor,

	Power Diode	Power BJT	Thyristor/ GTO	Power Mosfet	IGBT/ MCT
Resisitivity Modulation	++	++	++	++	++
Charge Storage	++	++	++	+–	++
MOS-Capacitances	–	–	–	++	++
Electro-thermal	+	+	+	+	+
Breakdown	++	++	+	+	++

Table 1.2: Relevance of basic physical phenomena for different power devices (++ very important, + important, +–less important, – not applicable).

GTO, IGBT, MCT), the low-doped layer is swamped by electrons and holes when the device is in its on state. The density of the injected charge carriers can be much higher than the level of the doping concentration, and the resistivity of the region is significantly reduced. The general expression of resistance of a region with the boundaries x_r and x_l and and the area A is given by:

$$R = \int_{x_l}^{x_r} \frac{dx}{qA(\mu_n n(x) + \mu_p p(x))} \tag{1.1}$$

where $n(x)$ and $p(x)$ are respectively the electron and hole density profile, μ_n and μ_p the mobilities of the charge carriers. In most cases, the charge carriers are not distributed homogeneously, so their density depends on position, or even the mobilities also cannot be considered as constants. During transient operation, the variation of the resistivity does not follow the changing current instantaneously, this effect can influence the switching behavior (e.g., forward recovery of power diodes), and in order to take it into account, a dynamic description of the charge distribution is necessary. Even if a solution of the time-dependent charge densities is found, the calculation of the resistance remains difficult since the integration of 1.1 is not possible without simplifications.

1.2.2 Charge storage

The charge carriers, which are stored in the lightly doped region of bipolar devices during the conduction mode, must be extracted before the device can reach its blocking state. This effect causes switching delays and switching energy losses. Standard low-power models for circuit simulation use a quasi-static description of the charge carriers. It means that the charge distribution is always a function of the instantaneous voltages at the device terminals. This

method is completely insufficient for power devices. A real dynamic description derived from the basic physical equations is required instead. The charge stored in a low-doped region of a power device varies, under transient operation, with both time and position. This variation is determined by the *ambipolar diffusion equation* (ADE):

$$\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{{L_a}^2} + \frac{1}{D_a}\frac{\partial p(x,t)}{\partial t} \tag{1.2}$$

where:

- $p(x,t)$ is the holes (minority carriers) excess concentration in the n^- region (cm^{-3});
- $D_a = \dfrac{2D_nD_p}{D_n + D_p}$ is the ambipolar diffusion coefficient (cm^2/s);
- $L_a = \sqrt{D_a\tau_B}$ is the ambipolar diffusion length (cm);
- τ is the high-level injection lifetime (s).

This equation is valid in the case of high-level injection when hole and electron densities (n and p) are approximately equal. The slope of the charge carrier distribution is related to the currents, this relation is described by the transport equation:

$$I_t = \left(1 + \frac{1}{b}\right)\left(I_n - qAD_a\frac{\partial p}{\partial x}\right) \tag{1.3}$$

where I_n is the electron current, I_t is the total current, the sum of electron and hole current and $b = \mu_n/\mu_p$ is the ambipolar mobility ratio. The integral of 1.2 together with the condition in 1.3 yields the charge control equation:

$$\frac{dQ}{dt} = -\frac{Q}{\tau} + I_n(x_r) - I_n(x_l) \tag{1.4}$$

where x_r and x_r are the boundaries of the considered region and Q is the charge in this region. One current component at each border is determined by the neighboring region. The total current is then obtained with 1.3, but this requires a solution of 1.2. Unfortunately, an exact analytical solution is not possible in the general case.

1.2.3 MOS capacitances

Devices with isolated gate (Mosfet, IGBT and MCT) have large capacitances which vary strongly with voltage in the different regions of operation. The capacitance of greatest importance is that between anode and gate. These are normally the output and input terminals of the device, and the resulting feedback has a dominating influence on the switching behavior. The capacitor is formed by the metal–oxide–semiconductor (MOS) structure resulting from the isolation of the gate from the semiconductor region. The value of the gate-anode capacitance C_{ga} can be calculated for the gate charge Q_g, according to the following relation:

$$C_{ga} = \frac{dQ_g}{dV_{ga}} = C_{ox}\frac{dV_{ox}}{dV_{ga}} \tag{1.5}$$

where C_{ox} is the capacitance of the plate capacitor which is determined by oxide thickness and area of the structure. The voltage V_{ox} across the oxide is an highly non-linear function of the gate-anode voltage V_{ga} since at the surface of the semiconductor, below the gate, different states of the charge are possible. These states are called accumulation, depletion and inversion. Depending on the state, the derivative in 1.5 can vary between one and zero. Solutions of 1.5 are usually obtained with approximations treating the states separately, but this can lead to problems of abrupt changes in the capacitance or its derivative at transitions between different regimes of operation. Furthermore, dynamic transition states are possible.

1.2.4 Electro-thermal interaction

Due to high energy losses, power devices can heat up significantly during operation. The device characteristics depend strongly on the device temperature, therefore, the changing temperature influences the device behavior. To consider this interaction between thermal and electrical characteristics, electrothermal device models are required. The device junction temperature T_j is calculated with the equation of heat transport:

$$\frac{\partial T_j(x,t)}{\partial t} = \frac{\lambda}{C'_{th}}\frac{\partial^2 T_j(x,t)}{\partial x^2} + \frac{P'}{C'_{th}} \tag{1.6}$$

where C'_{th} is the thermal capacitance per volume, λ is the thermal conductivity of the material and P' is the generated thermal energy per volume.

Thermal models usually use an average device temperature, which is then applied to the temperature-dependent parameters of the model equations. The temperature, however, is distributed inside the device and high temperature peaks can be localized in small regions.

1.2.5 Breakdown

Breakdown in power semiconductor devices occurs not only in the case of failure: in many applications breakdown happens during regular operation of the device (e.g., at turn off of GTO's). The most common breakdown mechanism is the avalanche effect due to impact ionization, but Zener breakdown and Punch-Through are also possible. The current increase due to the generation of charge carriers by impact ionization can be expressed by a multiplication factor M_p:

$$I_p(W) = M_p I_p(0) = \frac{I_p(0)}{1 - \int \alpha_p(x) \int_0^W (\alpha_n(x') - \alpha_p(x'))dx' dx} \tag{1.7}$$

where α_n and α_p are the ionization coefficients which depend on the electric field $E(x)$:

$$\alpha_p(x) = a_p^{-\frac{b_p}{E(x)}}, \alpha_n(x) = a_n^{-\frac{b_n}{E(x)}}$$

The integral in 1.7 cannot be solved analytically since the electrical field is not constant. Furthermore, there is a feedback of the generated charge carriers on the electric field and during transient operation, the onset of the avalanche breakdown can be shifted significantly by the current flowing through the high-field region (dynamic avalanche). Usually, however, a constant breakdown voltage is used to model breakdown.

1.3 Levels of power devices model

In the last decades, many models have been proposed and classified according to their accuracy and complexity characteristics: in [4] there are six proposed model levels that can be adopted for implementation in any circuit simulator or finite element (or finite difference) simulator. The categorization of the levels begins with simple behavioral models and then moves to more complex physics-based models. Different model levels have been developed using

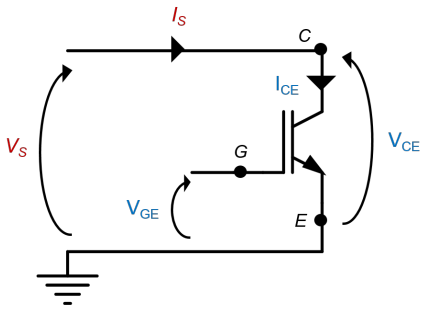
different programming languages: a brief review of these six model levels is presented below.

1.3.1 Level 0 model

The Level 0 model is a behavioral model that does not have a real physical representation. In other words, this model can be considered as an ideal electrical switch with two states: off-state, when there is no current flow and the device is in blocking condition, and on-state when it is in conduction mode with no forward voltage drop. In order to assist numerical convergence during the simulation, the commutation time may either be zero (instantaneous) or finite. Thermal or power loss estimation cannot be obtained with this model: some parameters, such as voltage drop at rated current or reverse blocking voltage and maximum forward current, should be specified in order to use the model for a particular device. The model allows fast, rough simulation and can be used in the early stages of the design process, for example in simulation of many switching cycles. This kind of model can be simply implemented, for instance, in MATLAB [3] environment [5] with only a few lines of code: in fig. 1.4a-b a schematic of external circuit current-voltage conditions imposed on IGBT and the MATLAB code for device Level 0 implementation are reported. We suppose that the circuit supplied current I_S is smaller than the maximum device DC current ($Imax$ is a parameter): once each of the following device parameters is defined (by experimental measurement or from datasheet), the model acts as an ideal switch between conduction and blocking states without any switching losses.

- *Vcesat* : ON-state voltage drop @ rated current [V];
- *Vbr* : OFF-state breakdown voltage [V];
- *Vth* : gate threshold voltage [V];
- *Imax* : ON-state maximum current [A];
- *Ileak* : OFF-state leakage current [μA].

[3] MATLAB (*Matrix Laboratory*) is a multi-paradigm numerical computing environment and fourth-generation programming language developed by MathWorks.



(a) Schematic of device-circuit interaction.

```
%IGBT Level0 model
IF (Vge>Vth) %ON-STATE
    Vce=Vcesat;  Ice=Is;
    ELSE %Vge>=Vth %OFF-STATE
        IF (Vs<Vbr) %blocking mode
            Vce=Vs;  Ice=Ileak;
            ELSE %Vs>=Vbr %breakdown
            Vce=Vbr;  Ice=Is;
        END
END
```

(b) MATLAB Level0 implementation.

Figure 1.4: Example of Level 0 modeling of IGBT device, with a) schematic representation and b) MATLAB code.

1.3.2 Level 1 model

A Level 1 model is also a behavioral model, suitable for basic system-level modeling where the circuit methodologies are tested, validated, and compared. It only represents the basic properties of the devices: voltage drop as a function of forward current and temperature and turn-on and turn-off switching losses as a function of current and voltage. Breakdown voltage limits, maximum forward conduction-current limits, and maximum junction-temperature limits are imposed. The junction temperature of the device is estimated by the simple multisection resistor-capacitor (RC) equivalent network. For instance, in a Level 1 model for IGBT device, the forward voltage drop and dependence on current and temperature would be modeled as follows [6]:

$$V_{ce,sat}(I_{ce}, T_j) = d(T_j)I_{ce} + e(T_j)I_{ce}^2 \tag{1.8}$$

where $d(T_j) = d_0 + d_1 T_j$ and $e(T_j) = e_0 + e_1 T_j$ are temperature dependent coefficients extracted from manufacturer datasheet I-V device output characteristic; d_0, e_0 and d_1, e_1 are respectively evaluated from $V_{ce,sat}$ values at two extreme temperatures (e.g., T_0=25°C and T_1=125°C). On the other hand, the dependence on temperature of the device total switching losses are:

$$E_{TOT,sw}(I_{ce}, T_j) = k(I_{ce}, T_j)I_{ce} \tag{1.9}$$

where $k(I_{ce}, T_j) = a(T_j) + b(T_j)I_{ce} + c(Tj)I_{ce}^2$ is a current-temperature dependent coefficient. The thermal factors:

- $a(T_j) = a_0 + a_1 T_j$;
- $b(T_j) = b_0 + b_1 T_j$;
- $c(T_j) = c_0 + c_1 T_j$.

are to be extracted from datasheet total switching losses curves versus IGBT collector current and junction temperature. The terms a_0, b_0, c_0 and a_1, b_1, c_1 are respectively evaluated at two extreme temperatures as well as in previous case.

1.3.3 Level 2 model

Level 2 models predict the same basic physical properties and behaviour as the switching characteristics of semiconductor devices. They are one dimensional and are a simplified physical-properties-based system. These models include all of the features of the Level 1 model, but they are not behavioural models. They accurately describe the dynamic characteristic within the device, except the operating area. An example of a Level 2 model is a lumped-charge model usually based on lumped-parameter approach and standard charge control method. The basic idea of is to divide the device into several critical regions: each of these regions contains one charged storage node and up to two connection nodes. Then, the charge nodes are linked using a set of equations related by semiconductor physics and circuit theory. Based on the physical equations, the injected carrier distribution inside the device is determined with a given external circuit condition. The voltage drops across each segment are calculated based on the carrier distribution at different nodes. The lumped charge model captures some of the physical behaviour of the device, but it does not provide adequate detail for the carrier distribution profile in the base and low-doped drift regions. The models are not easy to adapt to incorporate all thermal dependencies and implementation for use in circuit simulators. The lumped-charge approach has been successfully used to create power diode, BJT, SCR, GTO, MCT and Mosfet models and it has been also used for IGBT modeling, as demonstrated in [7] and [8], where the lumped-charge technique is chosen to develop models for both for standard no-buffer layer and buffer-layer IGBT, achieving good results in terms of accuracy and parameters extraction method.

1.3.4 Level 3 model

Level 3 models are typically full physics-based models. Beside the external electrical characteristics, internal physical and electrical information, such as the junction temperature and carrier distribution in different regions of the device, can be obtained. This requires solving the ambipolar diffusion equation in 1.2 by using some of the numerical algorithms: Fourier series, Laplace transformation, internal approximation, or difference methods. In most cases, due to high level injection that occurs in lightly doped drift region of bipolar power semiconductor devices, the ADE is assumed to be one dimensional. For instance, in [9] the solution of 1.2 is obtained using a Laplace transformation:

$$P(x,s) = P_0 \frac{\sinh\left[\sqrt{\frac{w^2}{D_a\tau}}\sqrt{1+s\tau_B}\left(1-\frac{x}{w}\right)\right]}{\sinh\left(\sqrt{\frac{w^2}{D_a\tau}}\sqrt{1+s\tau}\right)} \tag{1.10}$$

where $P(x,s)$ and P_0 are respectively the Laplace transform of $p(x,t)$ and p_0 (holes excess concentration at p edge of the $n^- region$) and w is the width of quasi-neutral region. Level 3 models using Fourier series solutions for solving the ADE in the lightly doped drift region have been developed for Si power diodes and IGBTs and recently extended to GaN and SiC devices. Another example of IGBT Level 3 model is the well-known Hefner model that combines an approximated solution for PNP base region minority carrier profile with a charge-control technique, to obtain the actual steady-state and transient behaviour in case of both Non-Punch-Through (NPT) [10] and Punch-Through (PT) [11] IGBTs.

1.3.5 Level 4 model

This is a complete, complex physical-properties-based model that captures all of the relevant physical parameters of the device, such as the motion of charge carriers and the associated electrical fields. The models are process based and should be able to have full two- or three-dimensional representation of the device design. They can also give information about the failure behavior of the device during operation outside of the safe operation area. The models could be implemented for example in TCAD simulators by using finite-element-method (FEM), but due to their complexity, no Level 4 analytical models

exists. A possible solution to preserve the good accuracy of the FEM simulation while significantly reducing the computational time is to implement an hybrid-model [12], in which some parts of device are analytically formulated according to the criteria of simpler model Levels (e.g., Level 3 model).

1.3.6 Level 5 model

These models have the ability to precisely simulate degradation effects that occur in the device during long periods of operation. The models take long-term radiation and degradation into account as well as any effects due to power or thermal cycling. Such models can be used to predict a failure of the device due to degradation, the device aging and life expectancy, so they are powerful tools for power semiconductor devices reliability analysis, both in design and circuit operation applications. Unfortunately, because of their complexity, very few Level 5 models for power semiconductor devices exist.

1.4 CAD methodology: compact models

As said before, all existing models of power devices have been properly conceived and theorized to enhance the effectiveness and reliability of simulation tools in device and circuit design development. In fact, the synergistic combination of modeling and simulation tools, known as *Computer-Aided Design* (CAD), helps with the critical analysis and detailed understanding at various levels, including:

- system and circuit design,
- device engineering,
- process development,
- integration into manufacturing.

As device technology becomes more complex, both in number of process steps and physics involved, the demands on simulation capabilities are also increasing and computer simulations turn out to be the only way to investigate physical phenomena which cannot be directly studied through practical measurements. CAD simulations exhibit a remarkable predictive valence upon calibration to proper experimental data. The generation of predictive models plays a crucial role in reducing development cycle times and costs in semiconductor industry.

1.4.1 TCAD/ECAD : compact models

TCAD (Technology CAD) is the field of engineering that simulates the fabrication processes and physical behaviour of power devices. It uses a process recipe and layout information to simulate the several fabrication process steps (e.g., lithography, deposition, etc) and obtain a 3D structure of the device, as depicted in fig. 1.5, where an IGBT cell structure is modelled in *Synopsys Sentaurus* TCAD environment.

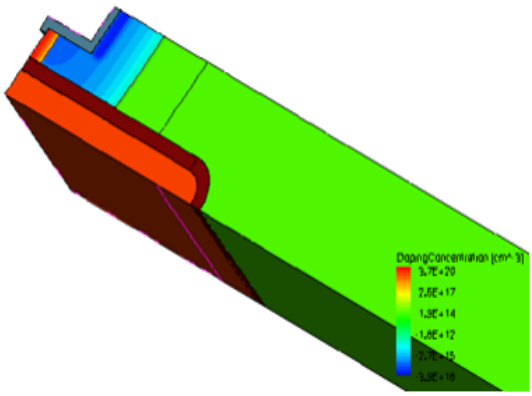


Figure 1.5: Example of IGBT cell structure developed in *Synopsys Sentaurus* TCAD environment.

Today, the role of TCAD is much wide and includes also the analysis and characterization of the devices themselves. The most used TCAD simulators in the field of semiconductor power devices (provided by Silvaco, Synopsis, etc.), are based on most accurate model levels (e.g., Levels 4,5): hence, main device physical characteristics are taken into account and device operation is simulated by solving the semiconductor transport equations at certain operating conditions through accurate numerical 3D FEM (Finite Elements or Differences Method) algorithm. The advantages and disadvantages of TCAD modeling are reported in table 1.3. By using simulation methods technology designers can observe what is going on inside the devices (useful in the development phase) which is impossible with experimental measurement techniques performed on devices themselves.

On the other hand, ECAD (Electronic CAD) environments provide the tools for generating a physical representation of the converters and circuits

Advantages
Fairly arbitrary devices (doping, geometry)
Realistic doping profiles from process simulation
2D/3D effects
Non-local effects (via appropriate transport model)
Quantum mechanical effects
Temperature dependencies
Sensitivity of device/circuit figures of merit to process parameters
Better predictivity for scaled/modified devices
Disadvantages
Performance (high computational time)
Convergence sometimes costly/difficult to obtain
Realistic doping profiles from process simulation

Table 1.3: Advantages and disadvantages of TCAD numerical device simulation.

in general from an high-level description. Traditionally, the designer started with a schematic representation at a transistor or logical level using device behavioral models such as Level 0 or Level 1, but, due to the increasing of device physical features and complexity of modern power circuits, the trend is to employ higher level ones, in particular Level 2, Level 3 and in some cases also Level 4 models. In fact, these types of models for power devices are sufficiently simple to be incorporated in circuit simulators and are sufficiently accurate to make the outcome useful to circuit designers: they are universally called and known as ***compact models*** [4] [13].

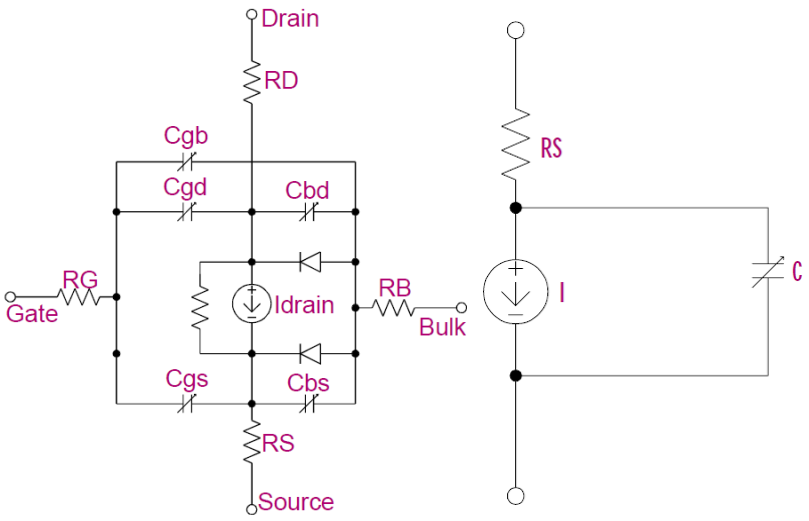
1.4.2 Compact SPICE modeling

Almost all the commercial specialized ECAD software vendors (like Cadence, Synopsys, Mentor, MicroSim, Intusoft, etc.) have developed simulation tools based on the well-known **SPICE** [5] simulator. SPICE commercial versions such as PSpice (owned by Cadence) or HSPICE (owned by Synopsys) represent a powerful tool for electronic circuits simulation thanks to simple user interfaces, effective finite-differences-method algorithm for solution evaluation

[4] *Compact modeling* concept in electronic field is anyhow applicable to any kind of analog/digital circuit elements such as passive devices, semiconductor devices, ICs, etc.

[5] *SPICE* (Simulation Program with Integrated Circuit Emphasis) is a general-purpose, open source analog electronic circuit simulator, used circuit design to analyze and predict circuit integrity and operation.

and types of analysis which can be performed (DC, transient, DC sweep, MonteCarlo, Worst-Case, etc.). Moreover, these simulators are offering enhanced support for the design of power electronic circuits by including standard compact models of main power devices (fig. 1.6): users can simply access to a few layout-dependent model parameters which must be evalauted and calibrated for a given technology.



(a) Mosfet model schematic. (b) Diode model schematic.

Figure 1.6: Schematic of power device models embedded in PSpice OrCad Suite.

Moreover, commercial and industrial SPICE simulators are systematically updated with many other device models as technology advances and previous models become inadequate. However, each simulator has usually a different type of model embedded: to attempt standardization of these models (so that a set of parameters may be used in different simulators), an industry working group was formed, the *Compact Model Council*, to choose, maintain and promote the use of standard models. The special challenge in developing such models for circuit simulation results from the need to simultaneously fulfill contradicting requirements like high quantitative accuracy, low demand of computation power, and physical and easy accessible model parameters. Although SPICE compact models represent the favorite tools for circuit designers, they are becoming attractive also in a number of applications concerning

different phases of power devices development from their design, to product analysis and circuit operation: in fact SPICE models and circuit simulation have been traditionally the main linkages between processing technology and product design.

1.4.3 Hierarchical CAD methodology

During the intermediate phase of power devices design, when devices structures are not established, *Mixed-mode* circuit [6] device simulation tool provided by most used TCAD softwares, can be used to investigate device behavior in circuit. The motivation are:

- compact models are inconvenient/not available;
- quick analysis with a circuit simulation;
- optimization of devices;
- exploitation of new device designs

In mixed-mode device simulation the solution of the basic transport equations for the semiconductor devices is directly embedded into the solution procedure for the circuit equations [14]: the use of compact models is thus avoided and much higher accuracy is obtained. Nevertheless, since numerical 3D simulation requires large computational time and processing resources, the simulated circuit operation must be very simple: hence, it's not possible to reproduce complex converters operation, but only a few switching cycles of device can be simulated. On the other hand,the need of increase product innovation, reduce prototyping has led to the improvement of the CAD methodology and its application from the beginning of the development phase of a power electronic circuit, in order to accurately predicts the functionality and reliability of a specific power circuit design. This problem can only be tackled through a rigorous hierarchical approach to CAD, as depicted in Fig 1.7, in which TCAD process and device simulations provide information for the development of compact models, suitable for circuit and system level analysis (ECAD).

While measurement data are traditionally used to characterize SPICE models, the use of TCAD simulation to represent nominal data has been on the rise,

[6] A *mixed-mode* simulation combines complex multi-dimensions TCAD model of device with SPICE compact models of other circuit elements and circuit network.

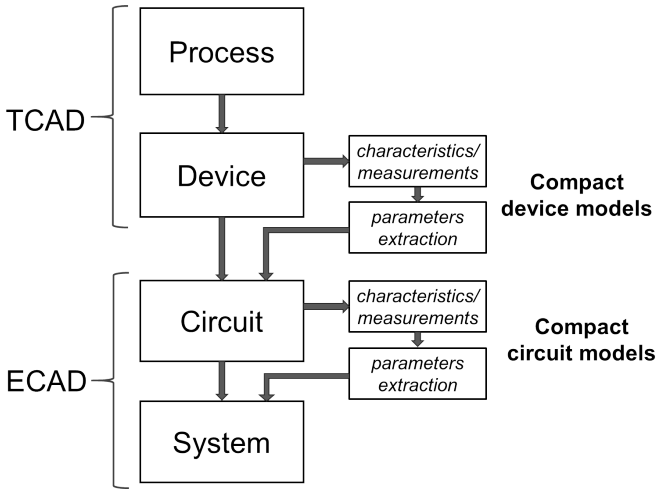


Figure 1.7: Hierarchical approach in device and system simulation analysis.

particularly during the pre-silicon or early development stages when measured data are unavailable and an early start on product design is required. Although the application of TCAD modeling in generation and extraction of nominal SPICE models and definition of technology targets has increased, several major improvements are needed to better support product design. In fact, model predictability is the most fundamental driving force behind TCAD modeling, but it is particularly important in applications such as the setting of processing technology targets for pre-silicon compact SPICE models characterization that are of the most importance to product design.

1.4.4 Combined SPICE/FEM approach

Another important application of device compact SPICE modeling regards the electro-thermal simulation of multicellular devices. The simulation of self-heating effect in power-devices is nowadays quite easily performed and a number of different techniques and even commercial software packages have appeared to perform this task. Nevertheless, when the device have a multicellular structure with a large area, an electro-thermal simulation that accounts for the interaction between a large number of elementary cells becomes a very hard task. The best solution to this problem is to use a compact 1D model for the electrical part coupled with a full 3D simulator for the thermal one [15].

Accordingly, the reasons of the renewed relevance of compact models lie in

their optimum trade-off between accuracy and low computational rate. Since continued down-scaling of semiconductor devices has made it necessary to incorporate new physical phenomena, while extended applications have led to the inclusion of the secondary and ternary effects in order to achieve the required model accuracy, considerable efforts are aimed to compact model reformulation in such a way that dramatically increased accuracy and model sophistication are accomplished without a prohibitive decrease in the computational efficiency.

Chapter 2

IGBT SPICE Modeling: Kraus Model

The Insulated Gate Bipolar Transistor (IGBT) represents the most commercially advanced device of a new family of power semiconductor devices synergizing high-input impedance MOS-gate control with low forward-voltage drop bipolar current conduction. It reduces the size and the complexity of controlling circuitry and the rate of power dissipation in power circuits, thereby drastically reducing the system cost. For these and more reasons, it is an established device in medium frequency, medium power applications such as uninterruptible power supplies (UIS), industrial motor-drives and domestic and automotive electronics. As IGBT voltage and current ratings increase, its application range is extending to high power applications: fabrication of a 5 kV device has already been optimized and 3.3 kV, 1200 A devices are commercially available. Nowadays, structure design improvements of medium power IGBTs and introduction of *WBG* semiconductors are really contributing to further increase the device performances, enabling circuit operation at higher frequencies. As a result of this pervasion, IGBT SPICE models are required by circuit designers and device manufacturers to predict circuit behaviour, to understand device internal mechanisms and to improve structures. Various circuit simulators including Saber, simulators of SPICE family, and some others are commercially available for IGBT modeling. The majority of IGBT models are used in one (or several) of these simulators. Based on the same core program, simulators of SPICE family (PSpice, SPICE, HSPICE, IG-SPICE, Contec-SPICE, SmartSPICE, etc.) have different features for various applications: for instance, Saber is a comprehensive multi-technology circuit simula-

tor which has strong program capability. At state of art, all the proposed models and SPICE implementations show distinctive features which make them attractive for both circuit and device designers but all these characteristics at least have not been unified into a single model. Moreover many issues regarding the well-known trade-off between accuracy and speed, easy accessibility to model parameters, availability of a general IGBT model[1], model standardization, convergence, etc., still affect IGBT SPICE modeling: this makes the challenge of research in the field of compact IGBT models very hard, but new developments are still to come due to rapid improvements in IGBT technology, SPICE numerical algorithm optimization and system computing capability.

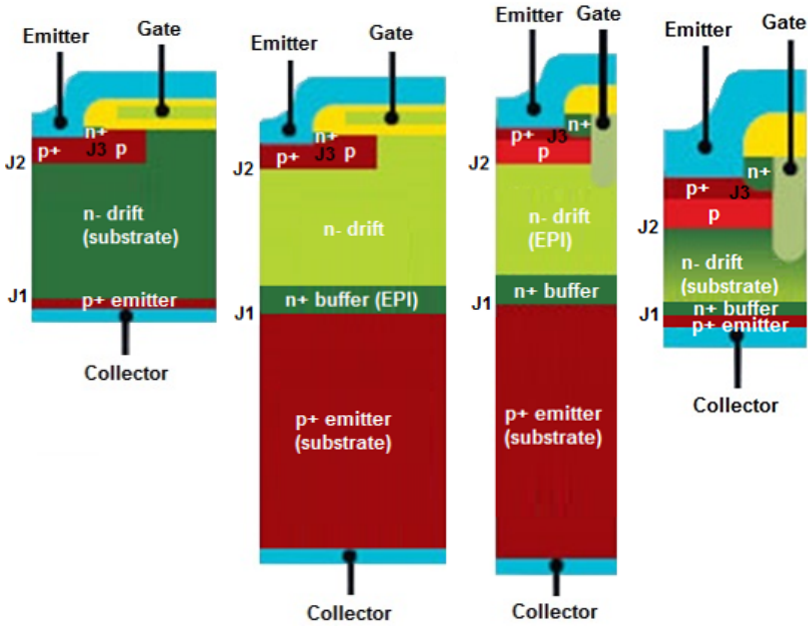
2.1 Main physics of IGBT

2.1.1 Structures and technologies

The IGBT overall electrical behaviour at its terminals strictly depends on its structure and its physics. The IGBT structure is formed by using four (N-P-N-P) alternating semiconductor layers: this creates a basic thyristor structure that is made inoperative by including a deep n^+ diffusion and short circuiting the P-base and the n^+ IGBT emitter regions. The device is optimized for DC circuit applications where no reverse bias is applied to the device because it operates exclusively in the first quadrant of the I-V characteristics. Traditionally, two are the main IGBT structures [1], concerning the confinement of electric field within the base region: the symmetric blocking structure is often referred to as the *Non-Punch-Through* (NPT) IGBT (fig. 2.1a) because the electric field has always a triangular profile and never extends through the entire width of the lightly doped n^- drift region. On the contrary, the asymmetric IGBT structure is distinguished by the introduction of an n^+ buffer layer within the n^- drift region: this layer is sometimes referred to as the field-stop layer (FSL). In the asymmetric structure, the forward-blocking voltage can be supported by a thinner n^- drift region resulting in a reduction of the on-state voltage drop: this structure is often referred to as the *Punch-Through* (PT) IGBT (fig. 2.1b) because the electric field "punches through" the entire lightly doped n^- drift region, assuming a trapezoidal profile due to the presence of buffer-layer.
These two headings of IGBT classification differ widely with regard to their fabrication technology, structural details, carrier profiles, lifetimes and trans-

[1] A general IGBT model is intended as a model capable to reproduce physical behaviour of different device technologies, such as planar,trench gated or NPT, PT, FS devices.

port mechanism. Being a MOS-controlled devices, at the upper part of an IGBT there is a gate structure: soon after the development of the first planar IGBT (DIGBT), it was recognized that significant improvements in the on-state voltage drop could be achieved by utilizing the *trench-gate* structure for IGBT (TIGBT) (fig. 2.1c-d). The trench-gate structure provides a stronger drive current to the wide-base PNP transistor in the IGBT resulting in superior high-level injection of carriers. Another important technological step was the development of a new asymmetric structure, the *Field-Stop* IGBT (fig. 2.1d), characterized by better overall performances due to reduction of p^+ emitter thickness, an implanted n buffer, and no lifetime control techniques.



(a) Planar NPT. (b) Planar PT. (c) Trench PT. (d) Trench FS.

Figure 2.1: The main structures of IGBT device.

According to its structural and physical properties, the IGBT can be roughly seen as a cascade of a PNP bipolar transistor and a n-channel Mosfet (fig. 2.2), where the PNP base current is provided by the MOS channel electron current, (considering the parasitic NPN transistor always turned-off) and the total current is the sum of Mosfet drain current and PNP collector current.

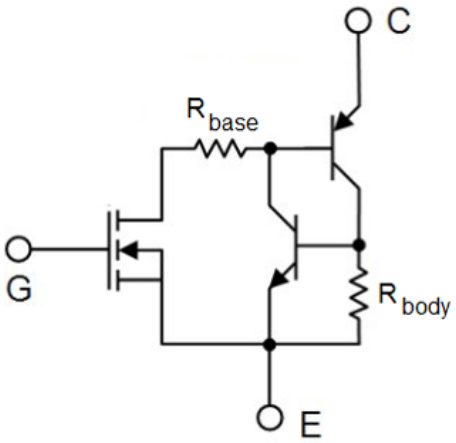


Figure 2.2: Equivalent schematic for the IGBT structure.

The resistances R_{base} and R_{body} are respectively the *conductivity-modulated* base resistance (1.1) and the parasitic body diffused resistance, responsible for turn-on of the parasitic NPN bipolar transistor and so for thyristor latch-up trigger. Almost all SPICE model implementations of IGBT are based on this configuration , where the MOS and BJT parts are separately analyzed and modeled and thus joined together to obtain the IGBT overall electrical output behaviour.

2.1.2 Blocking and conduction modes

An IGBT SPICE model is expected to reproduce the device static characteristics considering a number of physical and structural phenomena. The IGBT is capable of supporting high voltages when the gate terminal is shorted to the emitter one by the external gate control circuit. When a positive bias is applied between collector and emitter terminals of both NPT and PT IGBT structure, junction J_1 is forward biased while junction J_2 becomes reverse biased. The applied voltage is supported across the reverse-biased junction J_2 with the depletion region extending in the n^- base (drift) region toward junction J_1. The maximum forward-blocking voltage capability of the NPT IGBT is determined by breakdown of the open-base PNP transistor and thus by the thickness of the n^- drift region, its doping and the carrier lifetime.

In case of PT structure, where the lightly doped base region becomes completely depleted at relative small voltage and n^+ buffer layer is designed to

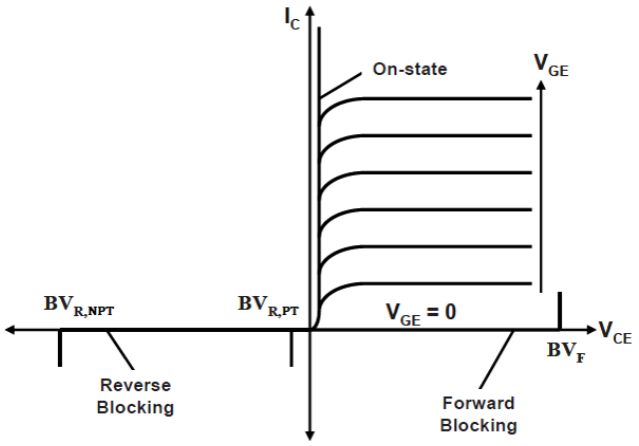


Figure 2.3: Output characteristics of an IGBT device.

avoid the *reach-through* [2] (the gain of PNP must be as low as possible), the forward-blocking IGBT capability is determined by the thickness of the lightly doped n^- base. On the other hand, when negative bias is applied, the junction J_1 is reverse-biased and supports the voltage: while the symmetric structure has also the reverse-blocking capability (determined as well by the open-base PNP breakdown voltage), the asymmetric one cannot support reverse-blocking due to presence of high-doped n^+ buffer layer and p^+ emitter regions. This is acceptable for utilization of PT IGBT in DC circuits, especially for motor drives, where a diode is connected in anti-parallel across the IGBT device. The IGBT passes to conduction mode when an inversion layer channel under the gate terminal, which connects the n^+ emitter region to the n^- base region, is induced by the application of a positive bias voltage (greater than the threshold voltage) between gate-emitter terminals. This allows the transport of electron current from the n^+ IGBT emitter region to the n^- base (with positive voltage applied to the collector which serves as the base drive current for the PNP transistor), promoting the injection of holes from the p^+ collector/n^- base junction J_1. Consequently, current flow occurs from the collector terminal to the emitter terminal with a bipolar component associated with the wide-base PNP transistor and a unipolar component via the channel of the Mosfet region. The

[2] The reach-through phenomenon occurs when the depletion region of reverse-biased junction J_2 reaches the high carrier concentration p^+ emitter region (junction J_1) before avalanche takes place in the n^- drift: then a further increase of the collector-emitter voltage causes the electric field to reach its critical value (for Si is $2 \times 10^5 V/cm$) at which avalanche begins.

n^- base (n^- drift) region of the IGBT structures operates with high-level injection conditions during current flow: the *conductivity modulation* occurring in the base reduces the resistance R_{base} of the n^- base, reducing the IGBT overall on-state voltage drop. In fact, referring to a NPT structure, the total on-state voltage drop can be evaluated as:

$$V_{on} = V_{p^+n^-} + V_{base} + V_{Mosfet} \tag{2.1}$$

where where $V_{p^+n^-}$ is the voltage drop across the p^+ emitter/n^- base junction (J_1), V_{base} is the voltage drop across the n^- base region after accounting for conductivity modulation due to high-level injection conditions, and V_{Mosfet} is the voltage drop across the Mosfet portion [16]. In case of PT device, also the voltage drop across the n^- base/n^+ buffer junction must be considered for evaluation of total V_{on}. The forward IGBT output characteristics are shown in fig. 2.3 for different values of gate-emitter voltage bias. While an accurate modeling of V_{base} is necessary in linear region and may require consideration of two dimensional effects, carrier distribution, mobility modeling including carrier-carrier-scattering and the band-gap-narrowing effect in the heavily emitter region, the Mosfet channel dominates IGBT behaviour in saturation region. A simplified expression of IGBT saturation current due to Mosfet channel "pinch-off", and taking into account the PNP base transport factor α_{PNP}, is given below:

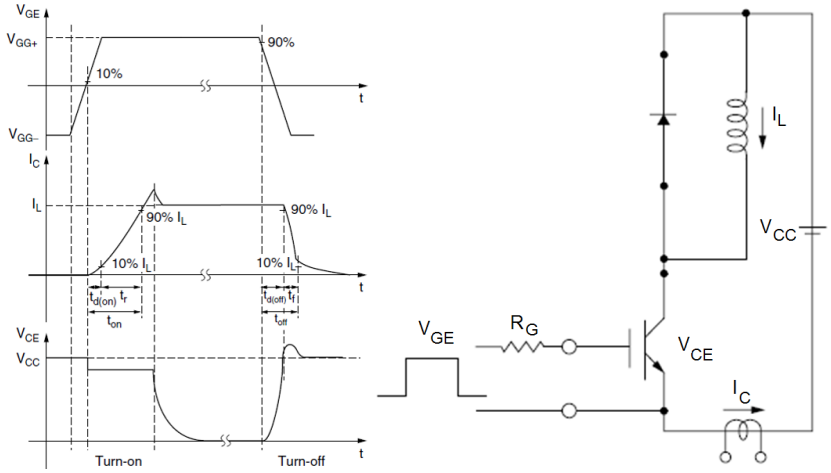
$$I_{c,sat} = \frac{1}{1-\alpha_{PNP}} \frac{\mu_s C_{ox} W_{ch}}{2L_{ch}} (V_{ge} - V_{th})^2 \tag{2.2}$$

where L_{ch} and W_{ch} are respectively the length and the width of the Mosfet channel [3] and μ_s and C_{ox} the electron channel mobility and gate-oxide capacitance. So an accurate modeling of saturation region (but also linear region as well) needs account for channel effects such as channel length modulation, velocity saturation, electric field dependent mobility, doping concentration gradient and subthreshold current. There are other important physical and structural effects in an IGBT device, such as avalanche phenomena occurring when device is approaching its own typical breakdown voltage or latch-up of parasitic thyristor due to activation of structural NPN transistor, but SPICE models often require simplification especially of second-order effects in order to achieve good performances in computational time and convergence.

[3] The channel length L_{ch} is a cell parameter, while the channel width W_{ch} can be assumed as an area factor in an IGBT model, in which the device, made of a certain number of cells, is simplified as one macroscopic cell with an equivalent channel width.

2.1.3 Transient characteristics and features

Since the most popular application for IGBT devices is for variable frequency motor control in automotive, heating and air-conditioning power circuits, SPICE models must faithfully reproduce its dynamic characteristics. An example of the typical switching IGBT gate-emitter voltage V_{ge}, collector current I_c and collector-emitter voltage V_{ce} waveforms in these kind of power circuits can be obtained with a simplified UIS (Unclamped Inductive Test) circuit configuration (fig. 2.4b) and are shown in fig. 2.4a:



(a) IGBT turn-on and turn-off waveforms.

(b) UIS circuit configuration.

Figure 2.4: Qualitative IGBT switching characteristics obtained with and UIS circuit configuration.

During the turn-on of the IGBT a voltage is applied to the gate of the device and it rises according to the values of gate-emitter capacitance C_{ge}, non-linear depletion gate-collector capacitance C_{gc} and series resistance R_g. When the gate equals the threshold voltage, MOS channel is formed and collector current I_c begins to rapidly rise according to MOS trasconductance and PNP injection characteristics, till the final steady-state value I_L: during this transition some time parameters are used to define IGBT turn-on characteristics such as turn-on time t_{on}, turn-on delay-time $t_{d(on)}$ and rise-time t_r. In transient case, differently from steady-state conditions, the drift region in the IGBT structure does not get modulated in proportion to the current density due to the finite rate for

the diffusion of minority carriers. A portion of the drift region remains without conductivity modulation when the current increases at a rapid rate. Since this portion of the n^- drift region has a high resistance due to its low doping concentration, the voltage drop across the IGBT is much greater than under steady-state operation. On the contrary, during IGBT turn-off when the gate voltage goes below the threshold voltage, the MOS channel disappears and the base current supply of the PNP transistor is cut off. With the PNP transistor being turned-off, the excess electrons and holes in the n^- drift region are either swept out of the region or recombined. The IGBT is subsequently in off-state, and the reverse voltage is blocked by junction J_3 between the P-body and the n^- drift region. The turn-off time of an IGBT is relatively slow (depending on IGBT technology) because many minority carriers are stored in the n^- region. When the gate is initially brought below the threshold voltage, the n^- region contains a very large concentration of electrons, and there is a significant injection of electrons and holes across the junction between the p^+ emitter and n^- region. As the electron concentration in the n^- drift region decreases, the injection current decreases, leaving the rest of the electrons to recombine with the holes. Therefore, the turn-off of an IGBT has two phases: an injection phase where the collector current falls very quickly, and a recombination phase in which the collector current decreases more slowly (*current tail*). This tailing time can be reduced by carrier lifetime control techniques such as electron, neutron, helium irradiation or platinum diffusion. Also during turn-off transient a number of parameters are defined as well: turn-off time t_{off}, turn-off delay-time $t_{d(off)}$ and fall-time t_f. Concerning IGBT dynamic characteristics, models must especially take care of rapid $\frac{dV_{ce}}{dt}$ occurring during hard-switching transients in common circuit application and of variation of carriers profile in n^- base region, according to the particular device structure (NPT or PT).

2.1.4 Temperature effects

As a semiconductor device, IGBT behaviour is sensitive to operating temperature. Temperature dependent models are useful to examine the reliability of their designs and devices at elevated temperatures. Usually temperature effects are considered in SPICE models by setting the device junction temperature at a certain level during the simulation. It has been shown that the IGBT junction temperature variation during a normal switching cycle is typically less than two Kelvin, which is readily verifiable with a two dimensional

numerical device simulator. Therefore, while setting a constant junction temperature is acceptable for simulating single cycle switching behaviour at the given temperature, power circuits SPICE model users need accurate modeling of temperature effects. The fact that almost all the basic semiconductor physics parameters are temperature dependent makes it a complicated procedure to consider the temperature dependence of the SPICE model. Fortunately, only the temperature dependence of a few parameters needs to be considered to model the temperature dependence of the IGBT behaviour such as $\mu_n, \mu_p, D_n, D_p, n_i, v_{nsat}, v_{psat}, E_g, \tau$, etc. The significant difference between temperature dependencies of PT [17] and NPT [18] devices is important for IGBT: for example, it is well known that, while the on-state voltage of PT IGBT have a small positive temperature coefficient at typical operating current levels, temperature coefficients of the NPT IGBT on-state voltage is strongly positive. Another important phenomena is that turn-off losses of a PT IGBT is much more sensitive to junction temperature than that of a NPT IGBT, which results in lower high frequency operation reliability for the PT IGBT. For the PT IGBT, the greatly increased base carrier lifetime at higher temperature results in larger amount of excess base carriers hence the higher and longer tail current. In a NPT IGBT, the low collector injection efficiency together with the already-high base carrier lifetime at the room temperature means that the stored base charge does not increase significantly with temperature. As said before, although the IGBT junction temperature is almost constant during a switching cycle, assuming a constant junction temperature is not valid for simulations involving transient thermal effects. Transient temperature dynamics (self-heating) are important for simulations on short-circuit behaviour, high frequency and high temperature operating stability, system thermal behaviour at start-up and steady-state, etc. In order to model the dynamic electro-thermal effects, an extra thermal circuit has to be modeled simultaneously with the electrical circuit including the temperature dependent model. The interactions between the two circuits have to be accounted for by calculating the time dependent device junction temperature from the thermal circuit and the power dissipation from temperature dependent device electrical behaviour.

A detailed description of the physics of the IGBT is outside the scope of this work, so for more details and a deeper analysis of IGBT physics and operation we advise the reader to refer to [1] and [19].

2.2 State of art of IGBT SPICE modeling

A classification of IGBT models proposed in literature over the years, which can be implemented as compact models within Saber or SPICE family simulators is given in [20] and includes four categories:

- **behavioural** models: simulate the IGBT behaviour without considering their physical mechanism. Measured IGBT characteristics are fitted by different methods, so they are cost effective but they lack in accuracy;
- **mathematical** (or **analytical**) models: based on semiconductor physics and solving physics equations with different simplifications results in analytical expressions describing carrier and electrical behaviour;
- **semi-mathematical** (or **semi-analytical**) models: partly based on physics while combining existing models (in the SPICE family, Saber, etc.) for other components. Most of the models in this category connect existing Mosfet and BJT models in a circuit simulator while using other parts to account for some specific effects in an IGBT;
- **semi-numerical** models: implemented in Saber, where ADE are numerically solved in base region and analytical modeling is used for other parts of the device, show the opposite trade-off, good results in transient behaviour, but very high computational time that makes them unsuitable for normal SPICE simulators.

Although satisfactory IGBT models are available for circuit simulation, comprehensive physical models for device mechanism understanding are not. As a bipolar power device, IGBT switching behaviour is dominated by the distributed charge in the wide n^- base. Describing the behaviour of this charge, which is governed by the ambipolar carrier transport equation (ATE),

$$I_n = qAn\mu_n E + qAD_n\frac{dn}{dx} \tag{2.3}$$

$$I_p = qAp\mu_p E + qAD_p\frac{dp}{dx} \tag{2.4}$$

is the main challenge in IGBT SPICE modeling. In steady-state this equation reduces to an ordinary differential equation, and the 1-D solution is used by many of the mathematical models. However, 2-D distribution of carriers in the IGBT base has significant effects on IGBT static characteristics. For

Author	Reference	Year	Classification
Shen *et al.*	[21]	1993	Mathematical
Kim *et al.*	[22]	1993	Semi-mathematical
Hefner	[10]-[23]-[24]	1988,1990,1994	Mathematical
Mihalic *et al.*	[25]	1995	Semi-mathematical
Kawaguchi *et al.*	[26]	1995	Semi-mathematical
Udrea *et al.*	[27]-[28]	1995	Mathematical
Fatemizadeh *et al.*	[29]-[30]	1993,1996	Mathematical
Zhang *et al.*	[31]	1996	Semi-mathematical
Petrie *et al.*	[32]	1996	Semi-mathematical
Musumeci *et al.*	[33]	1996	Semi-mathematical
Strollo	[9]	1997	Mathematical
Kraus *et al.*	[34]-[35]-[36]	1993,1997,1998	Mathematical
Sheng *et al.*	[37]-[38]	1996,1999	Mathematical
Igic *et al.*	[39]	2002	Mathematical
Kang *et al.*	[40]-[41]	2003	Semi-mathematical
Azar *et al.*	[42]-[43]	2004	Semi-mathematical
Chibante *et al.*	[44]-[45]	2003,2005	Semi-mathematical
Cotorogea	[46]	2009	Mathematical
Chimento *et al.*	[7]	2011	Mathematical
Miyake *et al.*	[47]-[48]	2008,2013	Semi-mathematical

Table 2.1: Benchmark of compact models for SPICE implementation.

dynamic transients, no satisfactory one dimensional analytical solution of the ATE has been obtained. Another limitation aspect is gate capacitances modeling: large gate capacitance variation for negative gate bias having significant effects on the transient gate waveforms and negative gate capacitance induced by the accumulation layer under the gate are not considered in SPICE models. Convergence and speed for most mathematical models are not satisfactory. Although convergence improvements have been made in various circuit simulators, convergence failure still occurs for many applications, particularly more complicated multi-IGBT circuits. Moreover, the parameter extraction procedures, which are useful tools for definition of model parameters, are available only for a few models.

Neverthless, most of SPICE implementation of theorized IGBT models are based on *mathematical* and *semi-mathematical* models because of their better trade-off between accuracy and speed, since they are able to reproduce the most important device static and dynamic phenomena with minimum computational effort. In table 2.1 there is a list of mathematical and semi-mathematical models proposed in literature over the years, which have been also implemented in a circuit simulator of SPICE family (PSpice, IG-SPICE,

HSPICE, etc.): in the next subsections an overview of the most popular and used models will be presented, and for more details, please refer to sources indicated in table 2.1.

2.2.1 Hefner model: OrCad PSpice NIGBT

Hefner [10]-[23] developed the first mathematical complete one-dimensional (1-D) analytical, charge controlled model suitable for circuit simulator implementation such as IG-SPICE [24] and Saber [49]. The *Non-quasi static* (NQS)[4] effects, caused by the fast penetration of the space charge layer (SCL) edge, were considered in modeling the increase of inductive turn-off voltage and non-linear capacitances between terminals, which affect dynamic behaviour, were also included; the expression for the conductivity modulated base voltage is given in a simplified form. The model was extended to a Punch-Through structure [11] and to a dynamic electro-thermal model [50].

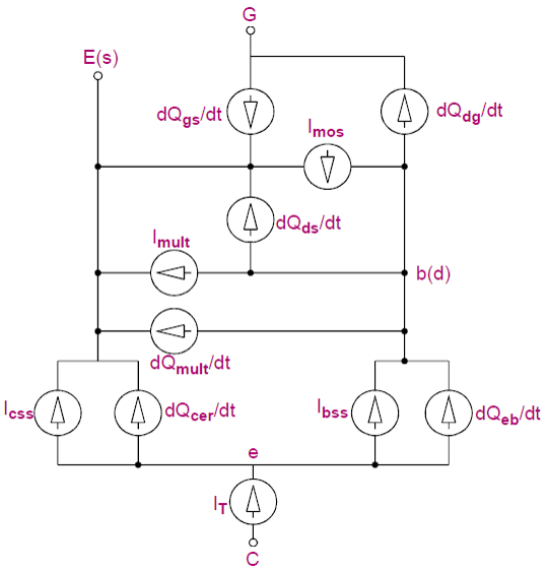


Figure 2.5: Schematic of OrCad PSpice NIGBT model based on Hefner's one.

[4]The Non-quasi static effects in case of IGBT models, refer to the description of charge carriers. The charge distribution in n^- base is assumed to be dependent both on instantaneous voltage and on the previously evaluated charge value.

An optimized version of the Hefner's model for NPT devices is implemented within the circuit simulator PSpice, and in most software which use this kind of simulator, such as, for example, OrCad or MicroCap. In particular the Hefner based *NIGBT* model is embedded in the OrCad PSpice Suite [51] library and only a few number of physical parameters can be defined by user via a parameters extraction technique (e.g., the one proposed by Hefner in [52]) or the model extraction tool provided by simulator designer. A simplified schematic of NIGBT model, very close to the Hefner version, is depicted in figure 2.5.

2.2.2 Kraus model

Another important contribution to IGBT compact modeling was brought by Kraus *et al.*, who proposed a semi-mathematical charge-controlled based model [36] for SPICE simulators implementation. Although some of the major IGBT manufacturers, such as "Infineon Technologies", are developing and providing to users Kraus-based IGBT models in the form of SPICE model files [5] for all devices marketed in their portfolio (including NPT,PT and FS devices with trench-gate structures too), currently there are no circuit simulator with an embedded implementation of Kraus model. In the next section we will analyze in details the Kraus model because it is the core of the new proposed IGBT model, then presented in chapter 3.

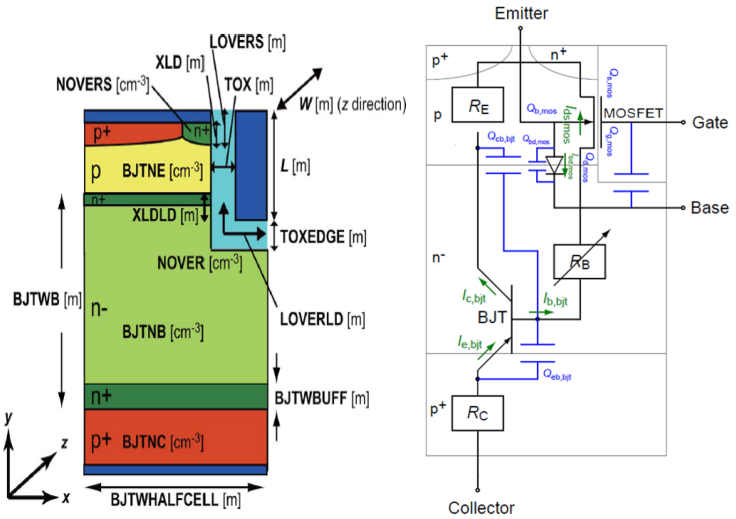
2.2.3 HiSIM model

A physics-based IGBT compact model for power electronic circuit simulators has been proposed in [48]: it's the first surface-potential-based model for circuit simulation based on the drift-diffusion approximation. In fact, the model is constructed as a combination of a Mosfet part, modeled with the advanced surface potential-based charge-oriented model HiSIM (Hiroshima University STARC IGFET Model), and a bipolar junction transistor (BJT) part with a conductivity-modulated base resistance in between them: it's named "HiSIM-IGBT" [6]. The model considers the potential distribution from the Mosfet chan-

[5] A SPICE model with file extension *.mod* is a text list of analytical expression, electrical devices, parameters and nodes written with SPICE syntax, which represent an equivalent electrical network of the model.

[6] While an IGBT generally has three terminals (Collector, Gate, and Emitter), HiSIM-IGBT considers four terminals (Collector, Gate, Emitter, and Base) because it has been developed based on the Mosfet-model framework HiSIM, together with the bipolar-junction-transistor (BJT) model.

nel to the two BJT junctions explicitly by solving important internal node potentials self-consistently. The IGBT output current at the collector terminal is governed by the base resistance of the bipolar part and the Mosfet characteristics.



(a) Major device structural parameters. (b) Schematic of Eldo HiSIM-IGBT.

Figure 2.6: The HiSIM IGBT model.

HiSIM-IGBT considers all controlling potentials in the base region calculated under fully dynamic load conditions, and which includes an advanced surface potential-based charge-oriented Mosfet model HiSIM. The approach assures that the dynamic interaction between the MOS and BJT part is accurately taken into account. The IGBT structure considered by HiSIM-IGBT model is shown in fig. 2.6a: some of the model most important structural and physical parameters are reported. The model developers also provide in [53] a parameters extraction technique for the definition of main model parameters. An optimized implementation of the HiSIM-IGBT model has been embedded in the SPICE simulator "Mentor SPICE Eldo": the equivalent model schematic is shown in fig. 2.6b. The complicated IGBT structure, which combines a bipolar junction transistor (BJT) with a Mosfet for base-current switching, imposes challenging problems on compact modeling for circuit simulation.

2.3 The Kraus model for NPT IGBT

The semi-mathematical NPT IGBT model proposed by Kraus *et al.* for SPICE circuit simulator implementation, based on base charge-control approach, is presented in [36]. In the previous works, basis for the development of the model were laid, although modeling approach was still complex for SPICE simulators and it could only be used in Saber: in [34] non-zero minority carrier concentration at the emitter edge of the base is modeled by averaging a sinusoidal lateral distribution, while an analytical 1-D polynomial approximated solution of carrier dynamic distribution is presented in [54]. Also a parameters extraction methodology for physical parameters definition is given in [35]. An important feature of the IGBT, namely, the enhancement of base conductivity modulation resulting from the accumulation layer under the gate, is modeled with a PiN diode for a Trench IGBT (TIGBT) by Azar *et al.* in [42]. The model is constructed as a combination of a Mosfet and a BJT: for the Mosfet part a standard SPICE model can be used while for the bipolar part, however, a standard SPICE model is not suitable since it cannot correctly reproduce the device characteristics due to high-level injection and non-quasi-static (nqs) effects during transient. Therefore a special equivalent circuit is used to model the typical device behaviour.

2.3.1 Model construction: charge-control approach

The core of the Kraus model is the evaluation of base charge Q_B as function of the minority carriers distribution in quasi-neutral region. In fig. 2.7 the structure of the bipolar part of a Non-Punch-Through IGBT is shown: the Mosfet part, taken into account through a Mosfet Level 1 SPICE model with model parameters V_{th} and K_p [7], defines the electron current I_{nC} entering the emitter IGBT contact (cathode).

The width of depletion or space-charge layer (SCL) region x_j and thus of quasi-neutral base region w, is function of built-in voltage across J_2 and of the PNP bipolar transistor base-collector voltage V_{bc}, which depends on external IGBT anode-to-cathode [8] bias voltage V_{AK}:

[7] The SPICE Level 1 Mosfet model parameters V_{th} and K_p are respectively the MOS threshold voltage and the linear transconductance.

[8] In order to distinguish the emitter and collector regions of internal PNP bipolar transistor from IGBT collector and emitter terminals, the latter will be referred to respectively as anode and cathode.

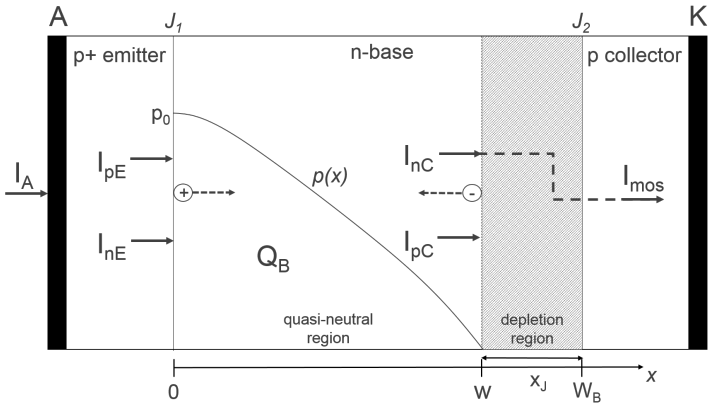


Figure 2.7: Structure of NPT IGBT: steady-state base charge carriers distribution.

$$x_j = \sqrt{\frac{2\epsilon_0 \epsilon_{Si}(V_{bc} + V_{J_2})}{qN_B}} \tag{2.5}$$

$$w = W_B - xj \tag{2.6}$$

Defining as I_Q the diffusion current in n^- base region due to the carriers charge Q_B, and considering the opposite sign for electron and holes currents, the following current continuity equations are always valid:

$$\begin{cases} I_{nC} = I_{nE} + I_Q, \\ I_{pC} = I_{pE} - I_Q, \\ I_{pE} + I_{nE} = I_{pC} + I_{nC} = I_A \end{cases} \tag{2.7}$$

where I_{nE}, I_{pE} and I_{nC}, I_{pC} are the electron-hole currents respectively at the PNP emitter and collector edges of n^- base region and I_A is the total IGBT output current (anode current). The PNP bipolar transistor in the IGBT structure is a lighlty-doped, wide-base, low-gain device operating under high-level injection conditions for practical current densities: so the the time-dependent ambipolar diffusion equation (ADE) 1.2 is solved in base quasi-neutral region to evaluate the excess holes density profile $p(x,t)$ in the n^- base quasi-neutral region. In the steady-state case, the ADE reduces to 2.8 and the holes profile $p(x)$ is calculated assuming, as boundary conditions, an hole density equal to

p_0 at emitter edge of the base and a zero-carriers concentration at the collector edge ($x = w$), because in forward operation mode the junction J_2 is reverse-biased.

$$\frac{\partial^2 p(x)}{\partial x^2} = \frac{p(x)}{{L_a}^2} \qquad (2.8) \qquad \begin{cases} p(0) = p_0 \\ p(w) = 0 \end{cases} \qquad (2.9)$$

Therefore, the steady-state solution for $p(x)$, given also in [19], is:

$$p(x) = p_0 \frac{\sinh\left(\frac{w-x}{L_a}\right)}{\sinh\left(\frac{w}{L_a}\right)} \qquad (2.10)$$

The steady-state carriers charge Q_{B0} is the integral of hole density distribution within the quasi-neutral base region, according to the following expression:

$$Q_{B0} = qA \int_0^w p(x)dx = qAL_a p_0 \tanh\left(\frac{w}{2L_a}\right) = \frac{p_0}{n_i} Q_{s0} \qquad (2.11)$$

defining, for simplification, a state-charge equal to $Q_{s0} = qAL_a n_i \tanh(\frac{w}{2L_a})$. The instantaneous base charge Q_B (general expression, considering also transient case) must satisfy the diffusion current continuity equation 2.12, that in steady-state case reduces to 2.13:

$$I_Q = \frac{Q_B}{\tau_B} + \frac{dQ_B}{dt} \qquad (2.12) \qquad I_{Q0} = \frac{Q_{B0}}{\tau_B} \qquad (2.13)$$

where τ_B is the high-level injection base lifetime. In order to find the value of Q_{B0} for each value of bias voltage V_{AK}, a system of dependent equations must be imposed by express a current component at each structure interface as function of the base-charge itself. At the PNP emitter edge of the n^- base where the junction J_1 is forward-biased, the well-known "junction's law" correlates the electron emitter current I_{nE} to the excess holes density p_0 and thus Q_{B0}, through the model parameter I_{sE}, that takes into account the emitter injection properties [19]:

$$I_{nE} = I_{sE} \frac{p_0^2}{n_i^2} = I_{sE} \frac{Q_{B0}^2}{Q_{s0}^2} \qquad (2.14)$$

On the other hand, at the edge of quasi-neutral region towards the PNP collector, the electron current I_{nC} is governed by Mosfet characteristics while

the hole current I_{pC} must be evaluated as function of Q_{B0} too. Since under high-level injection conditions ATEs (Ambipolar Transport Equations) (2.3-2.4) become coupled, they can be expressed as function of the total current I_A:

$$I_{nC} = \frac{b}{1+b} I_A + qAD_a \frac{dp(x)}{dx}|_{x=w} \tag{2.15}$$

$$I_{pC} = \frac{1}{1+b} I_A - qAD_a \frac{dp(x)}{dx}|_{x=w} \tag{2.16}$$

where $b = \dfrac{\mu_n}{\mu_p}$ is the mobility ratio. Hence, with the derivative of $p(x)$ at $x = w$ equal to

$$\frac{dp(x)}{dx}|_{x=w} = -p_0 \frac{1}{\sinh\left(\dfrac{w}{L_a}\right)}, \tag{2.17}$$

the value of steady-state PNP collector hole current is:

$$I_{pC} = \frac{1}{b} I_{nC} + \left(1 + \frac{1}{b}\right)(F_1 Q_{B0}) \tag{2.18}$$

with $F_1 = \dfrac{1}{\tau_B \left(\cosh\left(\dfrac{w}{L_a}\right) - 1\right)}$ is a function of bias voltage V_{AK}, by means the width w of quasi-neutral base region.

2.3.2 Transient solution for ADE

As evidenced in 1.2, the excess hole density $p(x,t)$ in the n^- base is a time-dependent function too: the general solution which takes into account also the transient case, can be expressed through a polynomial expansion, as proposed in [54]. Whereby, in the base charge continuity equation 2.12, the time derivative of Q_B must be considered and it's:

$$\frac{dQ_B}{dt} = \frac{Q_{B0}}{\tau_B} - \frac{Q_B}{\tau_B} + \frac{Q_{B0} - Q_B}{T_D} \tag{2.19}$$

where T_D is a strongly varying factor due to fast variation of depletion region width x_j with IGBT V_{AK} voltage, equal to:

$$T_D = \frac{0.1\dfrac{w^2}{D_a}}{1 + \dfrac{w}{12D_a}\dfrac{dx_j}{dt}} \tag{2.20}$$

By substituting 2.19 in the 2.12, the instantaneous base charge Q_B must satisfy the following condition, to take into account of transient case, that is:

$$I_Q = \frac{Q_{B0}}{\tau_B} + \frac{Q_{B0} - Q_B}{T_D} \tag{2.21}$$

From the above expression, and referring to 2.14 and to 2.7, it's possible to explicitly calculate the steady-state base charge Q_{B0} as function of Mosfet current I_{nC} and instantaneous base charge, that is:

$$Q_{B0} = \frac{2Q_{BD}}{F_3 + \sqrt{F_3^2 + \dfrac{4T_D I_{sE} Q_{BD}}{Q_{s0}^2}}} \tag{2.22}$$

where $Q_{BD} = Q_B + T_D I_{nC}$ and $F_3 = 1 + \dfrac{T_D}{\tau_B}$.

The time dependence of excess hole density profile $p(x,t)$ affects also the expression of PNP collector side hole current I_{pC}, according to:

$$I_{pC} = \frac{1}{b} I_{nC} + \left(1 + \frac{1}{b}\right)\left(F_1 Q_{B0} + F_2\left(I_0 - I_Q\right)\right) \tag{2.23}$$

where $I_0 = \dfrac{Q_{B0}}{\tau_B}$ and F_2 is equal to:

$$F_2 = 0.5\left(1 + \tanh\left(\frac{w}{6D_a}\frac{dx_j}{dt}\right)\right) \tag{2.24}$$

In steady-state condition the value of transient base current I_Q is equal to its steady-state value I_0, reducing the 2.23 to 2.18. Another important feature of the model is the evaluation of conductivity modulated base resistance R_B, that, as already mentioned, is generally expressed by 1.1. Assuming high-level injection in n^- base, a simplified expression for numerical implementation of R_B, as function of base-charge Q_B is:

$$R_B \cong \int_0^w \frac{dx}{qA(\mu_n N_B + (\mu_n + \mu_p)p(x,t))} \cong \frac{W_B^2}{\mu_n Q_n + (\mu_n + \mu_p)Q_B} \tag{2.25}$$

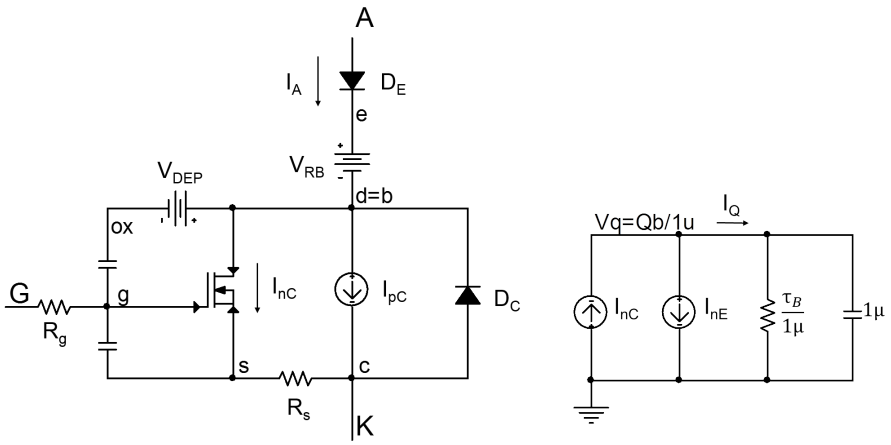
where $Q_N = qAN_BW_B$ is the background mobile carriers base charge. Moreover, in transient case, MOS capacitances effects are dominant, in particular the gate-source capacitance and the gate-drain capacitance that is strongly non-linear with IGBT V_{AK} transient voltage. While the fist capacitance is modeled with a constant model parameter C_{gs}, the gate-drain capacitance is obtained with the series of a constant value C_{ox} (gate oxide capacitance, a model parameter) and a variable voltage source, named depletion voltage, that is function of instantaneous drain-to-gate voltage according to:

$$V_{DEP} = V_{dg} + V_N \left(1 - \sqrt{1 + \frac{V_{dg}}{V_N}}\right), \quad V_N = qN_B\epsilon_0\epsilon_{Si}\left(\frac{A_{gd}}{C_{ox}}\right) \tag{2.26}$$

where A_{gd} is another model parameter, representing the gate-drain overlap area.

2.3.3 PSpice model: advantages and drawbacks

A simplified circuital implementation of Kraus NPT model is shown in fig. 2.8a.



(a) IGBT equivalent circuit . (b) Subcircuit for Q_B evaluation.

Figure 2.8: Schematic of the Kraus IGBT NPT model.

A few elements have been also added such as R_g, the internal gate resistance and R_s, the body region spreading resistance, SPICE diode model D_E

	Symbol	Parameter	Unit
Geometrical	A	device active area	cm^2
	A_{gd}	gate-drain overlap area	cm^2
Mosfet	V_{th}	MOS threshold voltage	V
	K_p	MOS transconductance	A/V^2
	C_{ox}	gate oxide capacitance	F
	C_{gs}	gate-source capacitance	F
	R_g	gate internal resistance	Ω
	R_s	source (body) resistance	Ω
Bipolar	W_B	metallurgical base width	cm
	N_B	base doping concentration	cm^{-3}
	τ_B	base high-level injection lifetime	s
	I_{sE}	electron emitter saturation current	A
	I_{sC}	electron collector saturation current	A
	C_{jE}	base-emitter depletion capacitance	F
	C_{jC}	base-collector depletion capacitance	F

Table 2.2: Model parameters for Kraus IGBT NPT model.

which defines the J_1 built-in voltage and diode D_C which models the IGBT blocking capability through the SPICE avalanche modeling (model parameter BV). The sub-circuit in fig. 2.8b synthesizes the base diffusion current I_Q continuity equation 2.12 in order to evaluate the instantaneous value of the base-charge Q_B from the voltage node $V_q = \dfrac{Q_B}{1\mu}$. The so-constructed Kraus-based IGBT model for Non-Punch-Through device has been implemented in PSpice OrCad environment: in table 2.2 model parameters are listed and in Appendix A the complete model PSpice implementation is reported, including circuital parts, analytical expressions, physical constants and device models.

As discussed before, the Kraus IGBT model implementation in PSpice simulator shows a number of advantages which make it competitive for circuit simulation respect to other models proposed in literature. In addition to the purely theoretical characteristics and to the analytical development, model owns some features which are fundamental for SPICE users:

- small number of parameters;
- good numerical convergence;
- low complexity;
- simple parameters extraction technique;
- extensibility (possibility of adding new features).

Model drawbacks and lacks	Notes
buffer-layer effects	*for PT and FS devices*
avalanche modeling	*SPICE diode breakdown characteristics*
gate capacitances for TIGBT	*constant capacitances*
constant mobilities	*the mobility is constant with doping*
MOS transconductance in linear region	*different from saturation region*
temperature dependencies for TIGBT	*thermal coefficients are different*
accurate base-resistance modeling	*extension to saturation region*

Table 2.3: Drawbacks of Kraus IGBT NPT model.

Since the model is based on a semi-mathematical approach, the adoption of SPICE embedded models of diodes and Mosfet, realizes a drastic reduction of model complexity and of number of model parameters. Moreover, the approximation of polynomial solution for holes profile in n^- base contributes to reduce the number of analytical equations and to make them more suitable for numerical processing. Another important feature is the relative low number of parameters: the model physical parameters can be defined from design device developers or from a simple extraction technique on experimental characteristics. Despite this, the strength of Kraus model is its extensibility, that is the possibility of increasing model accuracy by adding some specific features in order to take into account of other static or dynamic effects and structural and physical device characteristics for a custom application. Model extension, however, is pursued at the expense of increasing of model complexity, simulation speed and convergence issues, as well as increase of model parameters. On the contrary, as often noted, model strengths in terms of speed and convergence properties are in a trade-off with model accuracy: in fact, many physical phenomena, which are fundamental in IGBT operation are even not considered in Kraus model. In table 2.3 a list of model "lacks" is given: in particular the structural model construction conceived for NPT devices doesn't make it suitable for PT or FS devices, as well as the simplified gate capacitances and temperature effects modeling are not capable of reproducing physical effects in a trench-gate device (TIGBT).

Therefore, although the Kraus model for IGBT seems to be very attractive for SPICE implementation, a lot of issues still need to be overcome and improvements can be made: in the next chapter a new version of Kraus model for FS trench-gate devices will be presented and discussed, which takes into account the most important device physical phenomena in order to make the model suitable for for both circuit simulation and device design applications.

Chapter 3

Optimized PSpice IGBT electro-thermal model

The large demand for effective and useful SPICE IGBT models both for device design and circuit simulation has led to several contributions in terms of proposed modeling strategies and approaches as analyzed in chapter 2. As result of a fine and detailed analysis of state of art in the field of IGBT models, we have identified Kraus model as the best choice in terms of compromise between accuracy and speed: furthermore, not less important, Kraus "open" approach allows to easily bring updates to model with new features, refinements and adds according to user requests or to technological developments which always bring changes and modifications to devices structure and characteristics. So Kraus model is the perfect base point to develop a more complex and more accurate model for SPICE implementation. In this chapter some improvements are introduced to Kraus standard NPT model and temperature dependencies of model physical constants and equations are properly implemented in case of trench-gate devices aimed to electro-thermal simulations analysis, by taking care of optimization in PSpice simulator. The resulting optimum performances in terms of speed, convergence, small number of parameters and ease of parameters extraction, motivate its effective use in modeling devices of different technologies, such as PT anf FS devices. In fact, as demonstrated in [55], in case of Hefner model (actually it's valid for any kind of SPICE model, included Kraus NPT model), it's always possible to evaluate a set of model parameters, slightly far from their physical values, which allows to properly match the experimental IGBT characteristics via a simple and general parameters calibration procedure, even when model doesn't reflect

exactly the device structure. Hence, the accuracy of model is validated on a commercial device, a 30 A Field-Stop trench-gate IGBT with blocking voltage of 600 V, using a proposed automated parameters extraction and calibration procedure implemented in MATLAB environment and discussed in Appendix B.

3.1 Improvements to Kraus IGBT NPT model

The base version of Kraus IGBT model for Non-Punch-Through devices without temperature dependence of physical parameters has been presented in chapter 2 and an OrCad PSpice implementation is reported in Appendix A. However, due to simplifications and approximations needed to ensure a reduction of number of parameters and of execution time in simulation, some device first order physical characteristics are not well modeled: this results in low accuracy and model is even not capable of reproducing characteristics of commercial NPT devices.

3.1.1 SPICE Level 1 Mosfet: transconductance

As already seen, the SPICE Level 1 Mosfet is used within the semi-mathematical Kraus approach to model the MOS part of the IGBT: only two parameters have to be defined, the MOS threshold voltage V_{th} and the equivalent MOS transconductance K_p. Although real device structure is made up of hundreds of elementary cells, a 1D compact model is often used as an equivalent macroscopic cell [1] and the Level 1 MOS trasconductance parameter is defined to implicitly incorporate (Mosfet aspect ratio $\frac{W}{L}$ is equal to 1, its standard value) information about cell pitch p_c, device active area A and MOS channel length L_{ch}, as well as gate oxide properties capacitance C_{ox} and electron channel mobility μ_s, according to the following expression:

$$K_p = \frac{W_{ch,eq}}{L_{ch}} k_p = \frac{1}{2} \frac{A}{p_c L_{ch}} \mu_s C_{ox} \tag{3.1}$$

with $k_p = \frac{1}{2}\mu_s C_{ox}$ and $W_{ch,eq} = \frac{A}{p_c}$. Therefore, K_p IGBT transconductance is evaluated as constant parameter for a given device and influences

[1] The IGBT total channel active area is modeled with a macroscopic Mosfet with L_{ch} equal to elementary cell channel length and $W_{ch,eq}$ equal to elementary cell channel width W_{ch} multiplied the number of cells N_{cell}.

the Level 1 Mosfet drain output current equations in two of the three different operation regions, as shown below:

$$\begin{cases} \textbf{Cut-off region}: \quad V_{gs} \leq V_{th} \\ I_{DS} = 0 \\ \textbf{Linear region}: \quad V_{gs} > V_{th}, \quad V_{ds} \leq V_{gs} - V_{th} \\ I_{DS} = \dfrac{W}{L} k_p \left[\left(V_{gs} - V_{th} \right) V_{ds} - \dfrac{V_{ds}^2}{2} \right] \left(1 + \lambda V_{ds} \right) \\ \textbf{Saturation region}: \quad V_{gs} > V_{th}, \quad V_{ds} > V_{gs} - V_{th} \\ I_{DS} = \dfrac{W}{L} k_p \left(V_{gs} - V_{th} \right)^2 \left(1 + \lambda V_{ds} \right) \end{cases} \tag{3.2}$$

However, respect to a pure Mosfet device, the equivalent MOS part of an IGBT exhibits a different physical behaviour in conduction mode, that is due to an increased carrier concentration near the accumulation region under the gate-to-drain overlap surface. In fact, as shown in fig. 3.1, the $P^+N^-N^+_{acc}$ layers form a PiN diode structure, and the carrier recombination near the $N^-N^+_{acc}$ interface will tend to increase the carrier concentration in this area, adding a significant contribution to the MOS current that is also largely responsible for the lower on-resistance especially in trench-gate structures due to their large accumulation area.

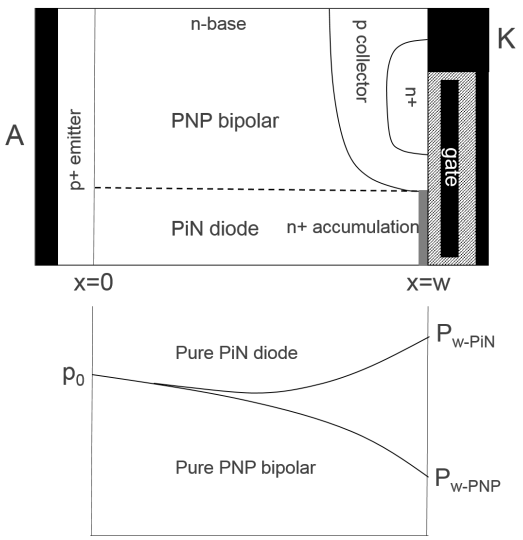


Figure 3.1: PiN injection effect in IGBT structure.

In [42] this effect is taking into account by solving the ambipolar diffusion equation (2.9) with a different boundary condition at the PNP collector edge of the base: this assumption suggests that in steady state condition, a rate of holes injected at the PNP collector actually recombines in the accumulation region reducing the bipolar holes current flowing to the cathode of the IGBT. Numerical simulations in [56] show that the actual carrier profile in the base of an IGBT follows neither $p_w = 0$ condition used in PSpice implementation of Kraus model, nor a pure PiN behaviour, where all holes recombine in the accumulation layer (fig. 3.1): a geometrical parameter γ is defined to adjust the boundary condition in the middle of two extremes behaviour. Despite this approach is valid and quite accurate, it substantially affects model speed since the new boundary conditions results in an increase of model equations and their complexity. Alternatively, the PiN effect can be obtained with a modification in Mosfet current, as implemented in Hefner model [49], where a new parameter K_f (linear transconductance factor) is defined in order to modify the Mosfet overall transconductance in linear region, as appears from Mosfet drain current equations:

$$\begin{cases} \textbf{Cut-off region}: \quad V_{gs} \leq V_{th} \\ I_{MOS} = 0 \\ \textbf{Linear region}: \quad V_{gs} > V_{th}, \quad K_f V_{ds} \leq V_{gs} - V_{th} \\ I_{MOS} = \dfrac{K_p K_f \left[\left(V_{gs} - V_{th} \right) V_{ds} - \dfrac{K_f V_{ds}^2}{2} \right]}{\left[\left(1 + \theta \left(V_{gs} - V_{th} \right) \right] \right.} \\ \textbf{Saturation region}: \quad V_{gs} > V_{th}, \quad K_f V_{ds} > V_{gs} - V_{th} \\ I_{DS} = \dfrac{K_p \left(V_{gs} - V_{th} \right)^2}{\left[2 \left(1 + \theta \left(V_{gs} - V_{th} \right) \right) \right]} \end{cases} \tag{3.3}$$

By comparing these equations with SPICE Level 1 Mosfet static equations 3.2, it can be noticed that the Mosfet electron current of the IGBT is exactly the drain current of a standard Mosfet biased with a drain-to-source V_{ds} voltage equal to $V_{ds}^* = K_f V_{ds}$. Hence, it's possible to implement the Hefner approach for modeling the PiN effect in Kraus PSpice model by only means of a simple modification: as shown in PSpice schematic of fig. 3.2, the internal IGBT V_{ds} voltage is multiplied by K_f and then imposed as drain-source voltage across the Level 1 Mosfet model through the controlled voltage source $VDSKF$.

Therefore, the equivalent Mosfet current, taking into account the different transconductance between linear and saturation regions, is replicated by the

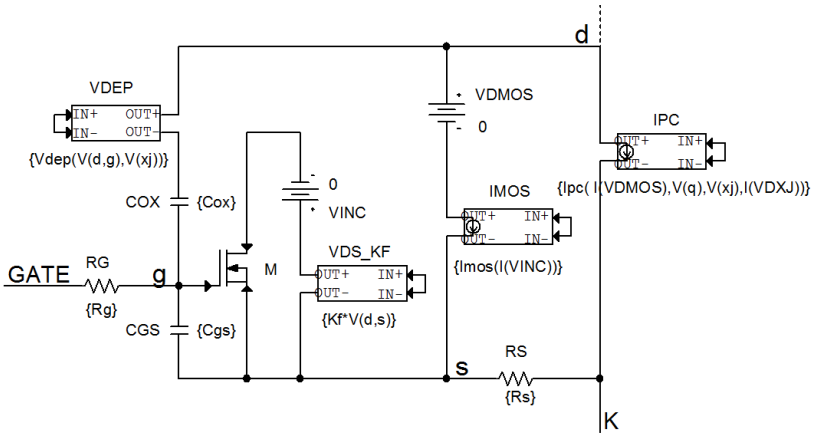


Figure 3.2: Introduction of K_f parameter into PSpice Kraus model.

controlled current source $IMOS$ that serves as electron current flowing to the body of the IGBT structure.

In fig. 3.3 the simulated IGBT output characteristic at $V_{ge} = 10V$ is plotted for different values of parameter K_f: simulations are referred to a single NPT 600V IGBT elementary cell with standard model parameters, that will be taken as reference for qualitative analysis. The IGBT collector current density J_c increases with increasing K_f: parameter K_f depends strongly on gate-to-drain area and for this reason becomes very important for trench-gate devices modeling.

3.1.2 Conductivity modulated base resistance

As we discussed in the chapter 1, one of the main important issue for IGBT modeling is to thoroughly consider the effect of conductivity modulation thet is mainly responsible for reduction of on-state voltage. This effect is strongly dependent on base carriers charge and becomes more important as injection level increases at higher collector current density. The simplified formulation of base conductivity modulated resistance R_B proposed in Infineon model (based on Kraus model) and reported in 2.25, provides good accuracy in steady-state conditions and low complexity due to some assumptions:

- high-injection level in the base;
- quasi-neutral region width w equal to metallurgical base width W_B;

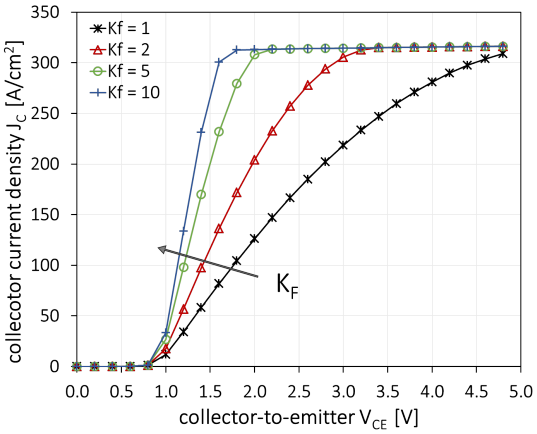
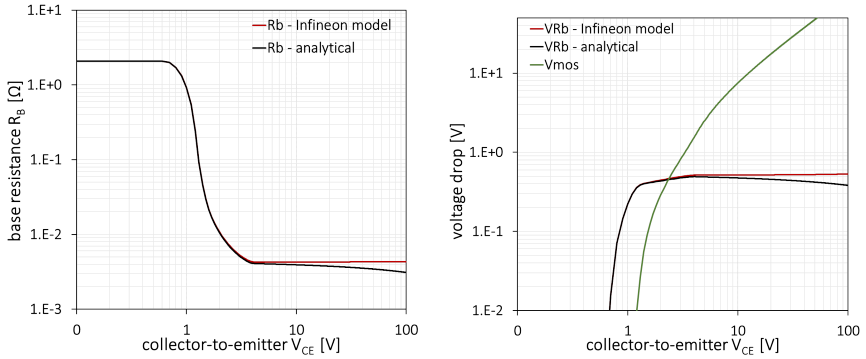


Figure 3.3: Simulated output characteristic at $V_{ge} = 10V$ of a standard 600V NPT IGBT cell for different values of parameter K_f.

- constant base lifetime and diffusion length in the base.;
- hole and electron mobilities not dependent on the doping.

The hypothesis of high-injection level in base, on which Kraus model is based, is valid for device acting in normal operation. The approximation of $w \cong W_B$ can be considered only for low on-state collector-to-emitter V_{ce} voltage values, when depletion region width is very small and the carriers charge fills virtually the entire base: nevertheless, when the V_{ce} voltage increases the contribution of R_B on base voltage drop becomes negligible, as it possible to appreciate in fig. 3.4a, where simulation of analytical expression of IGBT base resistance versus collector-to-emitter voltage, for an output DC characteristic at $V_{ge} = 15V$, is compared with its approximated expression given in Infineon model. Moreover, in fig. 3.4b, the base voltage drop curves corresponding to the two base resistance expressions are plotted (same conditions) and compared with Mosfet voltage drop, that is significantly larger during IGBT forward conduction mode. Although R_B simplified expression in 2.25 fairly differs from analytical one when IGBT collector current saturates, its contribution to overall IGBT voltage drop remains small respect to increasing voltage across reverse-biased PNP base-collector junction (that is internal Mosfet V_{ds}).

However, the expression of R_B ceases to be valid if we consider the effect of base conductivity modulation on IGBT switching losses during device



(a) (b)

Figure 3.4: Qualitative simulations of steady-state a) base resistance R_B and b) base voltage drop V_{RB} for the output IGBT characteristic at V_{ge}=15V: comparison between analytical expression and its approximation proposed by Infineon.

transient, especially in hard-switching conditions. As pointed up in [57], a correct description of R_B is therefore required to correctly predict the amount of dissipated power in circuit applications. A more detailed description of base resistance must take into account the effects of smaller carriers charge during IGBT turn-on respect to the stationary case that results in a change of effective diffusion lengths of carriers in the base: in fact it's possible to define a variable diffusion length λ, equal to:

$$\lambda = \sqrt{\frac{D_a Q_B}{I_n(w) - I_n(0)}}. \tag{3.4}$$

During steady-state operation, when the difference between electron currents at emitter and collector edges of base is related to stationary carriers charge Q_{B0} through the base lifetime τ_B, λ becomes equal to L_a, while it is set to infinity during turn-off transient when $I_n(0) > I_n(w)$, causing a linear distribution of holes within the base, according to the approximated following function:

$$p(x) \cong p_0 \frac{\sinh\left(\frac{w-x}{\lambda}\right)}{\sinh\left(\frac{w}{\lambda}\right)} \tag{3.5}$$

with $p_{s0} = \frac{p_0}{\sinh\left(\frac{w}{\lambda}\right)}$. Inserting equations 3.4 and 3.5 in the general integral formulation of R_B (2.25), and integrating, the resulting expression leads to the equation which determines the general form of base resistance:

$$R_B = \frac{2\lambda}{qA\left(\mu_n + \mu_p\right)\sqrt{N_{eff}^2 + p_{s0}^2}}\, artanh\left(\frac{\sqrt{N_{eff}^2 + p_{s0}^2}\, tanh\left(\frac{w}{2\lambda}\right)}{N_{eff} + p_{s0}\, tanh\left(\frac{w}{2\lambda}\right)}\right) \tag{3.6}$$

where $N_{eff} = \frac{\mu_n}{\mu_n + \mu_p} N_B$ is the effective n^- base doping. The incidence of the new general expression of R_B on reference 600 V IGBT simulated switching losses in an inductive hard-switching circuit conditions is demonstrated in fig. 3.5, where E_{on} and E_{off} are evaluated as function of device base lifetime (model parameter τ_B) and compared with results obtained using the Infineon base resistance expression (2.25): Kraus model using simplified base resistance predicts a lower value of E_{on} (about 15%) and, as lifetime becomes smaller (for example in in modern Field-stop trench-gate devices), the evaluation of E_{off} is lower too respect the one predicted with model using the new transient expression of base resistance.

Hence, the 3.6 is considered in PSpice Kraus model implementation by adding the equation in table 3.1 and the dependencies of VRB controlled voltage source on Mosfet electron current and time derivative of depletion region width.

The PSpice simulator embedded library doesn't provide the function for "hyperbolic arc tangent", so it must be explicitly implemented with its equivalent formulation in terms of exponential functions. The addition of a few more equations in the model for R_B results in an increase of model complexity which however doesn't particularly worsen the model speed and convergence rate in both static and dynamic simulations.

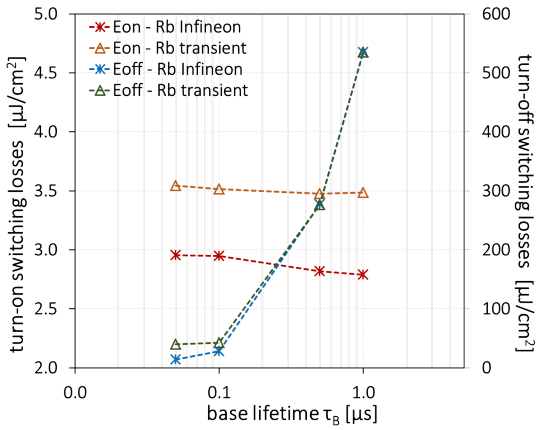


Figure 3.5: Behaviour of a NPT 600 V IGBT turn-on and turn-off switching losses with device base lifetime τ_B, simulated in hard-switching inductive circuit conditions: comparison between Infineon (2.25) and transient (3.6) expressions for R_B, implemented in Kraus model.

SPICE equations
.PARAM Neff={un*Nb/(un+up)}
.FUNC ps0(IMOS,VQ,XJ,IXJ) {p0(IMOS,VQ,XJ,IXJ)/sinh(w/La)}
.FUNC lambda(IMOS,VQ,XJ,IXJ) {SQRT(Da*Qb(VQ)/
+ (Inc(IMOS)-Ine(IMOS,VQ,XJ,IXJ)))}
.FUNC artanh(IMOS,VQ,XJ,IXJ) {0.5*log((1+x(IMOS,VQ,XJ,IXJ))
+ /(1-x(IMOS,VQ,XJ,IXJ)))}
.FUNC x(IMOS,VQ,XJ,IXJ) {(SQRT(Neff**2+ps0(IMOS,VQ,XJ,IXJ)**2)*
+ tanh((Wb-XJ)/(2*lambda(IMOS,VQ,XJ,IXJ)))/
+ (Neff+ps0(IMOS,VQ,XJ,IXJ)*tanh((Wb-XJ)/
+ (2*lambda(IMOS,VQ,XJ,IXJ))))}
.FUNC Rb(IMOS,VQ,XJ,IXJ) {(2*lambda(IMOS,VQ,XJ,IXJ)/(q*A*
+ (un+up)*SQRT(Neff**2+ps0(IMOS,VQ,XJ,IXJ)**2)))*
+ artanh(IMOS,VQ,XJ,IXJ)}
.FUNC VRB(IA,IMOS,VQ,XJ,IXJ) {IA*Rb(IMOS,VQ,XJ,IXJ)}

Table 3.1: SPICE analytical functions for transient R_B implementation in Kraus model.

3.1.3 Avalanche breakdown

In the standard Kraus model, the typical breakdown characteristic of the IGBT is abruptly modeled by means a SPICE diode model (diode DC in fig. 2.8), in which only three parameters are defined, according to IGBT model parameters:

- $IS = I_{sC}$: diode reverse electron saturation current;
- $CJ = C_{jC}$: zero-bias PN junction capacitance;
- $BV = BV_{ce}$: reverse breakdown voltage.

In fact the diode *DC* is used to model the PNP collector-base junction that is reverse-biased during forward conduction and blocking mode, providing only a leakage current by means the saturation current parameter "I_{sC}", while it experiences breakdown phenomena when IGBT internal V_{dk} voltage approaches BV_{ce} value at any gate-to-emitter voltage values. Although this approach is convenient in terms of model simplicity and convergence properties, it doesn't provide the actual physical behaviour of avalanche breakdown occurring in real bipolar device and in particular in the IGBT structure. Hence, a more accurate modeling of avalanche breakdown phenomena at high collector-to-emitter voltage is required in a number of applications: for instance, great emphasis has been giving for many years to the study and investigation of IGBT behaviour and ruggedness in avalanche conditions ([58]-[59]-[60]) via electro-thermal multi-cellular device analysis which rely on SPICE compact modeling for IGBT electrical behaviour simulation. Furthermore, the development of new fast FS TIGBT technologies has focused the attention of circuit and device engineers on the dynamic avalanche phenomena: during device turn-off transition, the high electric field in base strongly interacts with *plasma* due to high-injection of both electrons and holes, contributing to the reduction of breakdown voltage below its steady-state value and to current filamentation ([61]-[62]-[63]). Although a compact modeling of dynamic avalanche would be very complex to achieve [2] and future developments are expected, the introduction of a more accurate model for avalanche breakdown in Kraus model is highly required. With reference to Hefner IGBT model [49] and its implementation in OrCad PSpice library (NIGBT model), the well-known Miller impact ionization model for bipolar transistor is adopted, that is also proposed

[2] A compact dynamic avalanche model must integrate, for example, electro-thermal effects in IGBT overall structure and even more the dependence of breakdown voltage with carriers injection level, and so with IGBT collector current.

for IGBT in [1]. The model is based on the evaluation of impact ionization multiplication coefficient:

$$M = \frac{1}{1 - \left(\frac{V_{cb}}{BV_{ce}}\right)^n}, \tag{3.7}$$

where V_{cb} is the voltage across reverse-biased collector-to-base IGBT junction and BV_{ce} is the IGBT breakdown voltage, at which M tends to infinity; $n = 6$ in case on P^+N junction. Breakdown voltage BV_{ce} can be set as a model parameter or can be evaluated from the physical equation depending on base doping N_B:

$$BV_{ce} = 5.34 \times 10^{13} N_B^{-3\backslash 4}. \tag{3.8}$$

The current due to impact ionization, also called avalanche current, is the product of current in absence of impact ionization phenomena and the multiplication coefficient. In case of an IGBT device it can be written as:

$$I_{av} = MI_c = M(I_{pc} + I_{nc} + I_{gen}), \tag{3.9}$$

where I_c is the IGBT collector current I_{gen} is the base leakage current due to thermally generated charges, equal to:

$$I_{gen} = \frac{qAn_i x_j}{\tau_B}. \tag{3.10}$$

The implementation of avalanche breakdown model within the PSpice Kraus model is pursued by adding a controlled current source between IGBT model schematic internal collector-base terminals, similarly to Hefner model approach, as shown in fig. 3.6.

Anyhow, the expression of avalanche current in case of Kraus model needs to be slightly modified, because a current source equal to 3.9 placed in parallel to IGBT total current, implies that currents I_{pc} and I_{nc} would be multiplied by factor $M + 1$. Therefore, the correct expression for I_{av} is the following:

$$I_{av} = (M - 1)(I_{pc} + I_{nc}) + MI_{gen} \tag{3.11}$$

The SPICE equations needed to analytically model avalanche current source are reported in table 3.2.

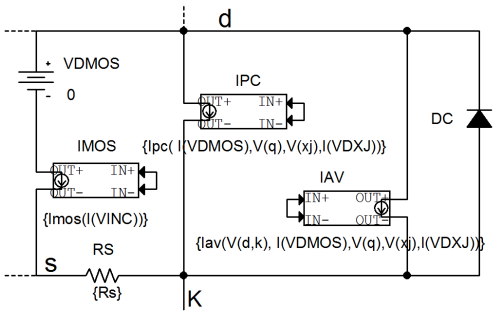


Figure 3.6: Addition of avalanche breakdown in PSpice Kraus model.

SPICE equations
.FUNC Igen(XJ) {LIMIT(q*ni*A*XJ/tb,0,1e6)}
.FUNC Mav(VDK) {1/(1-((VDK/BVce)**6))}
.FUNC Iav(VDK,IMOS,VQ,XJ,IXJ) {(Mav(VDK)-1)*
+ (Ipc(IMOS,VQ,XJ,IXJ)+IMOS)+
+ Mav(VDK)*Igen(XJ)}

Table 3.2: SPICE analytical functions for avalanche breakdown implementation in Kraus model.

Note that in PSpice model 3.6 the reverse-biased diode *DC* has not been removed, since the contribution of its reverse leakage current is negligible respect to avalanche current: rather it serves to ensure numerical convergence for collector-to-base voltage values over the breakdown voltage.

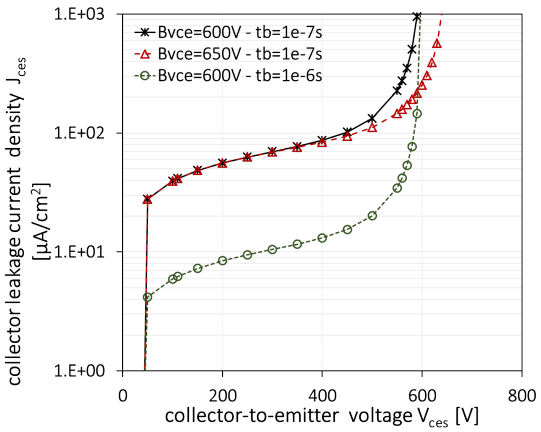


Figure 3.7: IGBT blocking characteristics simulated with improved Kraus model: qualitative behaviour versus parameters τ_B and $BVce$.

The qualitative behaviour of reference NPT 600 V IGBT blocking characteristic (V_{ge}=0V) simulated using improved Kraus model is plotted in fig. 3.7, in which the incidence of model parameters base lifetime τ_B and breakdown voltage BV_{ce} is verified on both IGBT overall leakage current and avalanche breakdown.

3.2 Temperature dependencies for ET model

One of the major requirements of an IGBT compact model is its capability to reproduce device characteristics at different temperatures. Most of SPICE simulators such as PSpice Cadence OrCad, allow to perform DC and transient simulations using devices models provided in the embedded library at a certain temperature value: however, it's not possible to perform electro-thermal simulations by considering transient thermal effects which are crucial for power devices. Hence, the need of a SPICE model which offers an accessible external node, in addition to electrical terminals, for junction temperature variation becomes essential. In case of IGBT device many electro-thermal mod-

els ([50]-[64]-[65]) have been proposed which consider the effect of device junction temperature on physical constants by modeling the silicon thermal characteristics. Although considerable improvements have been made also for Kraus model as presented in [43] and [35], commercial SPICE models based on Kraus model, such models provided by Infineon Tehcnologies, still suffer from some limitations:

- the temperature dependence of physical constant is based on planar-gate devices;
- some model parts are too complex;
- junction temperature is not a network node;
- no temperature dependence for avalanche breakdown.

The aim of this section is to explain some improvements proposed to PSpice implementation Kraus model in order to take into account the temperature dependencies in trench-gate devices and to make the model suitable for electro-thermal transient simulations.

3.2.1 Physical constants in TIGBT

Several dominant physical parameters associated with semiconductor devices are sensitive to temperature variations, causing their dependent device characteristics to change dramatically. In [17] experimental relations for main physical parameters of trench-gate IGBTs are given. The most important of these parameters are:

i) the minority carrier lifetimes (which control the high-level injection lifetimes);

ii) the hole and electron mobilities;

iii) the free-carrier concentrations (also ionized impurity-atoms);

iv) the intrinsic carrier concentration value n_i.

Almost all of the impurity atoms are assumed to be ionized at temperatures above 120 K (-150 °C) and are considered to be the impurity doping concentration values in the analysis. The n^- drift region in an IGBT is under high-level

injection conditions during forward conduction and as such, recombination events there are described by the effective high-level carrier base lifetime, τ_B:

$$\tau_B(T_j) = \tau_{B0} * \left(\frac{T_j}{300}\right)^{1.5}, \tag{3.12}$$

where T =300 K is the ambient temperature and T_j the junction temperature (in Kelvin). The pre-factor τ_{B0} is the base carrier lifetime (model parameter) at ambient temperature ($T_{amb} \cong 300K$) and the temperature exponent in may vary slightly depending on the details of device fabrication and design. The empirical relations for electron and hole mobility as a function of temperature, are given in 3.13 and 3.14: carrier-to-carrier scattering effects are not included in the equations.

$$\mu_n(T_j) = \mu_{n0} * \left(\frac{300}{T_j}\right)^{2.5}, \tag{3.13}$$

$$\mu_p(T_j) = \mu_{p0} * \left(\frac{300}{T_j}\right)^{2.5} \tag{3.14}$$

where u_{n0} and u_{p0} are electron and hole mobilities at ambient temperature. Whereby, according to the Einstein's law, ambipolar diffusion coefficient D_a is also a temperature dependent physical parameter:

$$D_n(T_j) = \frac{k_B \mu_{n0} T_j}{q} \left(\frac{300}{T_j}\right)^{2.5}, \quad D_p(T_j) = \frac{k_B \mu_{p0} T_j}{q} \left(\frac{300}{T_j}\right)^{2.5}, \tag{3.15}$$

and therefore:

$$D_a(T_j) = \frac{2 D_n(T_j) D_p(T_j)}{D_n(T_j) + D_p(T_j)} = \frac{2 k_B \mu_{n0} \mu_{p0} T_j}{q\,(\mu_{n0} + \mu_{p0})} \left(\frac{300}{T_j}\right)^{2.5}; \tag{3.16}$$

k_B (J/K) is the Boltzmann constant and q (C) the electron charge. The intrinsic carrier concentration, n_i, appears as a physical constant in the model as well and its temperature dependence is given by:

$$n_i(T_j) = \frac{3.88 \times 10^{16} T_j^{1.5}}{\exp\left(\frac{7000}{T_j}\right)}. \tag{3.17}$$

In this approximation of silicon intrinsic concentration bandgap narrowing is not considered. The IGBT has two further parameters which are affected by temperature: the MOS-gate threshold voltage and MOS channel transconductance. These are approximated by:

$$V_{th}(T_j) = V_{th0} - 9 \times 10^{-3}(T_j - 300), \tag{3.18}$$

$$K_p(T_j) = K_{p0}\left(\frac{300}{T_j}\right)^{0.8}, \tag{3.19}$$

where V_{th0}, K_{p0} are model parameters defined at ambient temperature T_j=300 K. Although model parameter K_f is basically a factor, in Kraus model it's is considered as temperature dependent as well as K_p, in order to better fit IGBT DC characteristics at different temperatures.

$$K_f(T_j) = K_{f0}\left(\frac{300}{T_j}\right)^{0.8}. \tag{3.20}$$

Hereafter, an experimentally extracted modeling of IGBT breakdown voltage dependence on temperature is proposed, which is fundamental for electro-thermal simulations of IGBT devices under avalanche test conditions. The commercial devices used in experimental measurements are a Field-Stop trench-gate 600 V-30 A IGBT and a Punch-Through planar-gate 600 V-100 A IGBT. Considering the IGBT forward blocking characteristics (V_{ge}=0V) and defining the IGBT experimental breakdown voltage as the collector-to-emitter voltage V_{ces} value at which device leakage collector current equals 10 mA [3], the behaviour of BV_{ce} versus temperature for both devices is plotted in fig. 3.8, where experimental data are fitted with an exponential function:

$$BV_{ce}(T_j) = BV_{ce0}\left(\frac{T_j}{300}\right)^{0.3}, \tag{3.21}$$

with BV_{ce0} equal to breakdown device voltage at ambient temperature ($T_j = 300K$).

[3]The value of collector current at which breakdown voltage is measured must be properly chosen according to device leakage current at rated collector-to-emitter voltage (V_{ce}=600V) and at maximum device temperature ($T_j = 175\ ^\circ$C): these information are all contained in device datasheets.

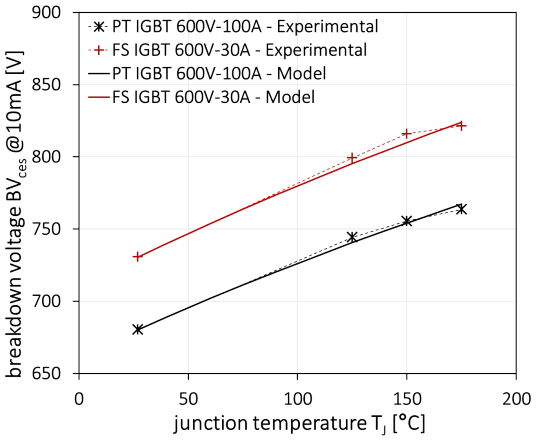


Figure 3.8: Experimental breakdown voltage measurements versus T_j at $V_{ge} = 0V$ and $I_{ces} = 10mA$: fitting model.

3.2.2 Schematic and equations adjustments

First of all, in order to make the PSpice NPT Kraus model suitable for electro-thermal circuit simulation, a internal network voltage node must be created (3.9a) to be accessible as an external device terminal as depicted in fig. 3.9b: hence, model equations need to be upgraded with dependence on temperature voltage node.

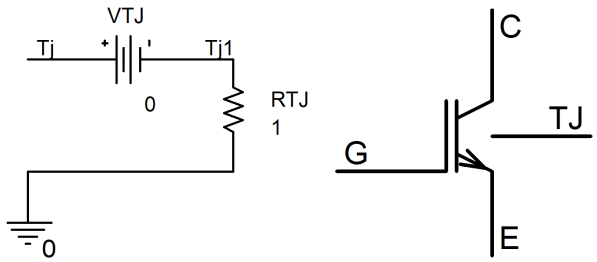


Figure 3.9: Temperature dependent model: a) temperature internal voltage node and b)PSpice model symbol with temperature terminal.

An important adjustment of both model schematic and equation to take

into account temperature dependence of PNP emitter-base junction behaviour modelled with diode *DE*, concerns its reverse saturation electron current I_{sE} and so its built-in voltage $V_{bi,J1}$: in fact, since I_{sE} is defined as model parameter at ambient temperature, it's expression versus temperature needs to be evaluated. Unfortunately, being the temperature T_j a network voltage node, it's not possible in PSpice to use a node's explicit expression within diode model definition. Hence, the proposed approach is to leave the given ambient temperature parameter value I_{sE0} as a diode DE model parameter and to model junction voltage temperature dependence by means a controlled voltage source *dVDE* (fig. 3.10), that introduces the variation of diode built-in voltage with temperature $\frac{dV_{bi}}{dt}$ using the typical PN junction thermal coefficient $-2mV/K$, only when diode *DE* is in forward conduction:

$$\begin{cases} dV_{bi}(T_j) = 0 & V_{e_1,e_2} < dV_{bi}(T_j) \\ dV_{bi}(T_j) = -2 \times 10^{-3}\,(T_j - 300) & V_{e_1,e_2} \geq dV_{bi}(T_j) \end{cases} \tag{3.22}$$

where V_{e_1,e_2} is the voltage across *DE* diode model. In PSpice model implementation the T_j is given in $^\circ C$: controlled voltage source *dVDE* value is always zero at ambient temperature (not depending on V_{e_1,e_2}) while it reduces at increasing temperature resulting in a reduction of overall PNP emitter-base voltage drop $V_{e1,A}$.

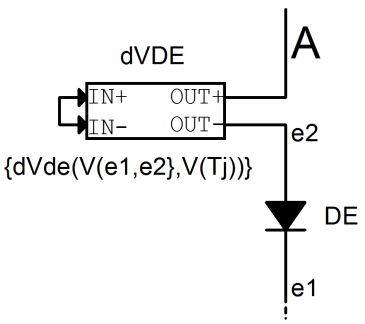


Figure 3.10: Schematic for diode DE built-in voltage dependence on T_j.

However, parameter I_{sE} appears explicitly in some model analytical functions, so it needs to be modified to take into account the temperature changes. The analytical expressions of reverse electron saturation current versus T_j and at ambient temperature are the following:

$$I_{sE}(T_j) = \frac{qAD_{nE}\left(T_j\right) n_i\left(T_j\right)^2}{L_{nE}\left(T_j\right) N_E}, \tag{3.23}$$

$$I_{sE0} = \frac{qAD_{nE0} n_{i0}^2}{L_{nE0} N_E}, \tag{3.24}$$

where N_E is the p^+ emitter doping concentration and D_{nE} and L_{nE} are respectively the electron (minority carriers in p^+ emitter) diffusivity and diffusion length (D_{nE0} and L_{nE0} their values at T_j =300 K). Assuming the approximation of transparent emitter $L_{nE} \cong W_E$ (W_E is the width of p^+ emitter region) and divided the 3.23 by 3.24, expression of I_{sE} as function of model parameter I_{sE0} and of temperature T_j is given:

$$I_{sE}(T_j) = I_{sE0} \frac{D_{nE}(T_j)\ n_i(T_j)^2}{D_{nE0}\ n_{i0}^2}. \tag{3.25}$$

Furthermore, the base lifetime τ_B dependence on temperature must be taken into account in model equations as well as in carriers base charge Q_B evaluation sub-circuit (fig. 2.8b), since a constant value resistor ($R_Q = \frac{\tau_B}{1\mu}$) can no longer be used for charge decay rate modeling. The modified schematic is depicted in fig. 3.11: a controlled current source is added as a temperature-variable resistance and a resistor $Rcon$ is needed to ensure convergence [4]. Hence, base carrier lifetime τ_B and transient carriers charge Q_B dependencies on device junction temperature can be clearly appreciated by simulating the variation of IGBT collector current during turn-off inductive switching for reference IGBT model, with particular focus on increase of current tail (fig. 3.12).

The dependencies on temperature of IGBT MOS electorn current through parameters V_{th}, K_p and K_f are also implemented in Kraus PSpice model: the 3.18 is obtained via a controlled voltage source placed between internal gate MOS resistance R_g and Mosfet Level 1 model gate terminal. On the contrary, the expression in 3.19 is implemented as a variation in Mosfet current, since the latter is a linear function of K_p: so controlled current source *IMOS* replicates the Level 1 Mosfet current and multiplied it by K_p thermal coefficient equal to $\left(\frac{300}{T_j}\right)^{0.8}$. In order to take into account the 3.20, it is added to expression of controlled voltage source *VDSKF* in which parameter K_f is used, as discussed

[4]The value of resistor $Rcon = 1$ M Ω is such that the current flowing in is negligible compared to I_{nC}, I_{ne} and capacitive current I_{cQ} at any operation conditions.

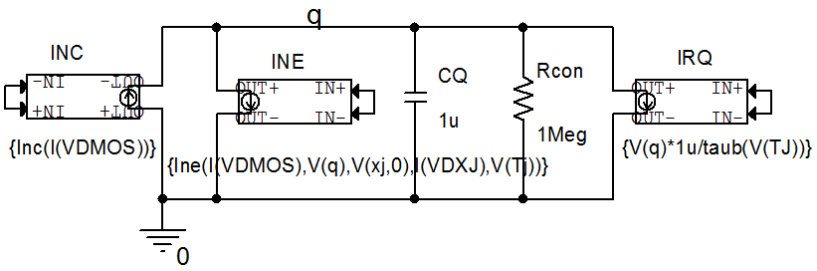


Figure 3.11: Schematic of base charge sub-circuit with T_j dependence.

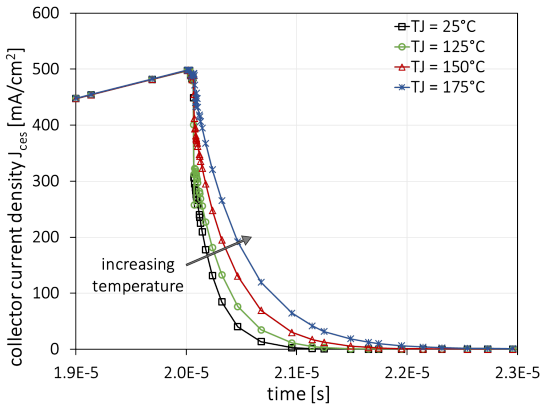


Figure 3.12: Effect of base lifetime τ_B temperature dependence on simulated inductive turn-off collector current waveform for reference IGBT model.

in previous section. The overall IGBT MOS-gate part of the PSpice model with modifications related to T_j is reported in fig. 3.13.

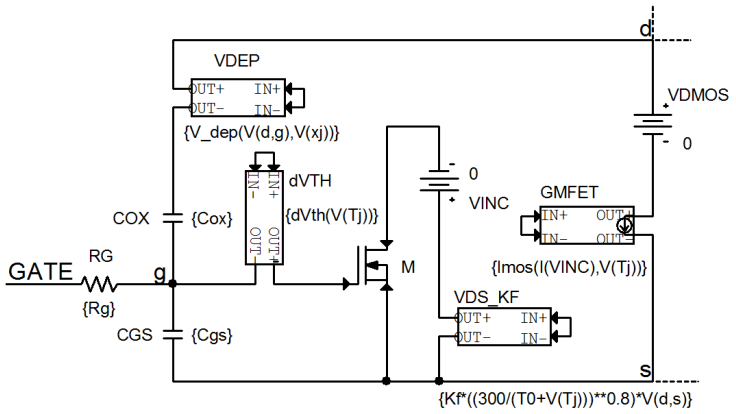


Figure 3.13: MOS-gate part of Kraus model with changes due to T_j.

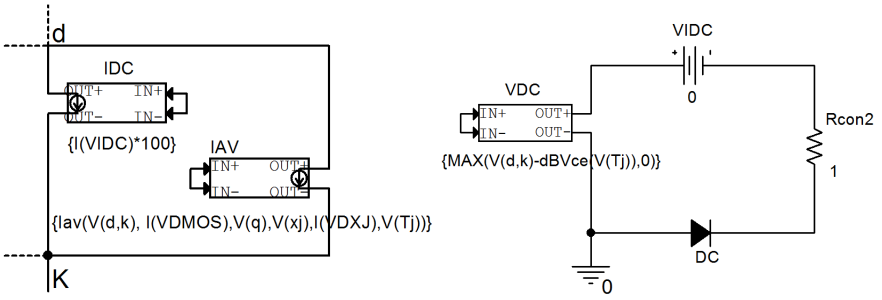
The combined effect of all model temperature dependent physical parameters are verified by simulating the DC IGBT output characteristics (V_{ge}=10V) at different temperatures of reference NPT 600 V device single cell, as shown in fig. 3.15a.
Finally, the IGBT breakdown voltage dependence on temperature is modeled by inserting the 3.21 into avalanche multiplication coefficient M_{av} and adding, in place of diode *DC*, a controlled current source *IDC* that replicates the current of sub-circuit in fig. 3.26b to achieve model convergence.

Defining the IGBT delta breakdown voltage ΔBV_{ce} as:

$$\Delta BV_{ce}(T_j) = BV_{ce}(T_j) - BV_{ce0}, \tag{3.26}$$

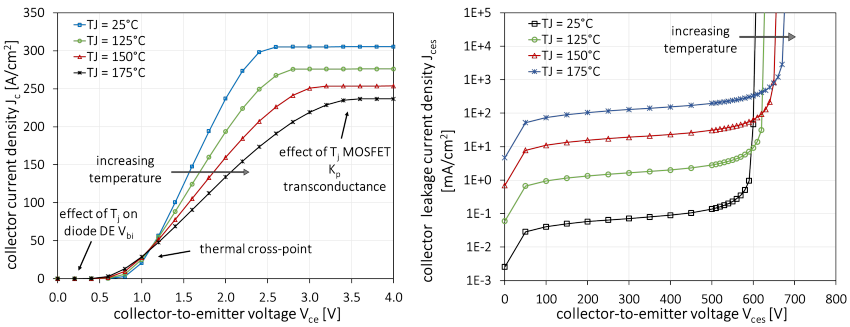
the diode DC in sub-circuit is always reverse-biased with a cathode-to-anode voltage equal to $V_{dk} - \Delta BV_{ce}$. So, since breakdown voltage parameter BV of diode DC is a constant value (BV=BV_{ce0}), the diode experiences avalanche breakdown when the V_{dk} reaches the correct IGBT breakdown voltage $BV_{ce}(T_j)$ at any temperature value, corresponding to a V_{ka} voltage value across DC exactly equal to BV_{ce0}. The qualitative effect of temperature on simulated IGBT blocking characteristic is shown in fig. 3.15b, in case of reference Kraus model.

The complete implementation in PSpice OrCad is of electro-thermal NPT IGBT Kraus-based model is reported below: in fig. 3.16 the schematic of



(a) (b)

Figure 3.14: Avalanche breakdown T_j dependence in PSpice Kraus model: a) main schematic change and b) sub-circuit for model convergence



(a) (b)

Figure 3.15: Simulation of IGBT characteristic versus T_j for device reference single cell model: a)DC output characteristic at $V_{ge} = 10V$ and b) blocking characteristic.

IGBT is depicted, where the three device electrical terminals *A*, *K* and *GATE* [5] are visible, in addition to temperature terminal T_j. In PSpice schematic the list of model parameters is also given, with their initial standard values. The list of all SPICE implemented analytical expressions, included equations of physical parameters and additional expressions for temperature dependence so far discussed, are reported in table 3.3: note the explicit dependence on network voltage node T_j that is expressed in °C (T_0=273 K).

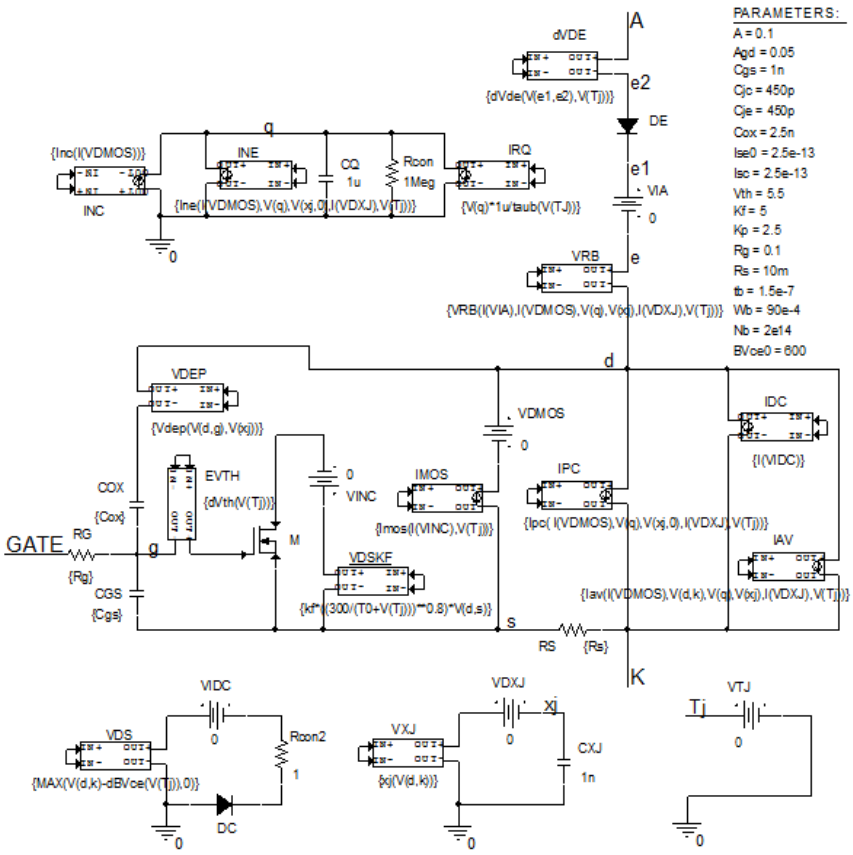


Figure 3.16: PSpice schematic of the Kraus IGBT NPT electro-thermal model with all adjustments.

[5] The diode nomenclature for IGBT power terminals (A-K) is used in order to distinguish external IGBT collector and emitter terminals from internal PNP ones.

Physical constants and silicon properties at $T_j = 300K$
.PARAM q=1.602e-19 eps0=8.85e-14 epsi=11.8 kB=1.38e-23 ni0=1.45e10
+ un0=1350 up0=450 Dn0=36 Dp0=11.7 vnsat0=1.07e7 vpsat0=0.83e7
.PARAM T0=273
.PARAM VN={q*Nb*eps0*epsi*((Agd/Cox)**2)}
.PARAM QN={q*A*Nb*Wb}
Physical parameter VS T_j
.FUNC taub(TJ) {tb*(((T0+TJ)/300)**1.5)}
.FUNC un(TJ) {un0*((300/(T0+TJ))**2.5)}
.FUNC up(TJ) {up0*((300/(T0+TJ))**2.5)}
.FUNC b(TJ) {un(TJ)/up(TJ)}
.FUNC ni(TJ) {1e-10*3.88e16*((T0+TJ)**1.5)/(exp(7000/(T0+TJ)))}
.FUNC Dn(TJ) {kB*(T0+TJ)*un0*((300/(T0+TJ))**2.5)/q}
.FUNC Da(TJ) {(2*kB*un0*up0/(q*(un0+up0)))*(T0+TJ)*
+ ((300/(T0+TJ))**2.5)}
.FUNC La(TJ) {SQRT(Da(TJ)*taub(TJ))}
.FUNC vnsat(TJ) {vnsat0/(0.26+0.74*TJ/300)}
.FUNC vpsat(TJ) {vpsat0/(0.63+0.37*TJ/300)}
.FUNC Ise(TJ) {Ise0*Dn(TJ)*1e20*(ni(TJ)**2)/(Dn0*(ni0**2))}
Model analytical equations
.FUNC Imos(IVINC,TJ) {LIMIT(IVINC*((300/(TJ+T0))**1.5),0,1e6)}
.FUNC dVth(TJ) {(TJ-27)*5e-3}
.FUNC Inc(IMOS) {LIMIT(IMOS,0,1e6)}
.FUNC Ipc(IMOS,VQ,XJ,IXJ,TJ) {LIMIT((1/b(TJ))*Inc(IMOS)+(1+1/b(TJ))*
+ (Qb0(IMOS,VQ,XJ,IXJ,TJ)*F1(XJ,TJ)+F2(XJ,IXJ,TJ)*MAX
+ ((-Qb0(IMOS,VQ,XJ,IXJ,TJ)+Qb(VQ))/TD(XJ,IXJ,TJ),0)),0,1e6)}
.FUNC Ine(IMOS,VQ,XJ,IXJ,TJ) {LIMIT(Ise(TJ)*
+ ((Qb0(IMOS,VQ,XJ,IXJ,TJ)/Qs0(XJ,TJ))**2) ,0 ,1e6)}
.FUNC dVdE(VD,TJ) {IF(VD¡-2e-3*(TJ-27),-2e-3*(TJ-27),0)}
.FUNC Vdep(VDG,XJ) {MAX(VDG,0)+VN*(1-SQRT(1+MAX(VDG,0)/VN))}
.FUNC coshyp(XJ,TJ) {(exp((Wb-XJ)/La(TJ))+exp((Wb-XJ)/(-La(TJ))))/2}
.FUNC F1(XJ,TJ) {LIMIT(1/(taub(TJ)*(coshyp(XJ,TJ)-1)),-1e6,1e6) }
.FUNC F2(XJ,IXJ,TJ) { 0.5*(1+tanh(((Wb-XJ)/(6*Da(TJ))) * dxj(IXJ))) }
.FUNC F3(XJ,IXJ,TJ) {LIMIT(1+TD(XJ,IXJ,TJ)/taub(TJ), -1e6, 1e6) }
.FUNC TD(XJ,IXJ,TJ) { LIMIT((0.1*(Wb-XJ)*(Wb-XJ)/Da(TJ))/
+ (1+((Wb-XJ)/(12*Da(TJ)))*dxj(IXJ)), -1e6,1e6) }
.FUNC Qs0(XJ,TJ) {LIMIT(q*A*La(TJ)*1e10*ni(TJ)*
+ tanh((Wb-XJ)/(2*La(TJ))),0,1e6) }
.FUNC Qbd(IMOS,VQ,XJ,IXJ,TJ) {LIMIT(Qb(VQ)+Inc(IMOS)*TD(XJ,IXJ,TJ) , 0,1e6)}
.FUNC Qb0(IMOS,VQ,XJ,IXJ,TJ) {2*Qbd(IMOS,VQ,XJ,IXJ,TJ)/(F3(XJ,IXJ,TJ)+SQRT(
+ (F3(XJ,IXJ,TJ)**2)+4*TD(XJ,IXJ,TJ)*Ise(TJ)*
+ Qbd(IMOS,VQ,XJ,IXJ,TJ)/(Qs0(XJ,TJ)**2))) }
.FUNC I0(IMOS,VQ,XJ,IXJ,TJ) {LIMIT(Qb0(IMOS,VQ,XJ,IXJ,TJ)/taub(TJ),0,1e6)}
.FUNC p0(IMOS,VQ,XJ,IXJ,TJ) {1e10*ni(TJ)*Qb0(IMOS,VQ,XJ,IXJ,TJ)/Qs0(XJ,TJ)}
.FUNC Qb(VQ) {LIMIT(VQ*1u,-1e6,1e6)}
.FUNC w(XJ) { LIMIT(Wb-XJ,1e-4,Wb)}
.FUNC xj(VDK) { LIMIT(SQRT((2*eps0*epsi*(VDK))/(q*Nb)),0,Wb-1e-4) }
.FUNC dxj(IXJ) {LIMIT(IXJ,-1,1)/1n}
Base resistance equations
.FUNC Neff(TJ) {un(TJ)*Nb/(un(TJ)+up(TJ))}
.FUNC ps0(IMOS,VQ,XJ,IXJ,TJ) {p0((IMOS,VQ,XJ,IXJ,TJ))/sinh((Wb-XJ)/La(TJ))}
.FUNC lambda(IMOS,VQ,XJ,IXJ,TJ) {SQRT(Da(TJ)*Qb(VQ)/
+ (Inc(IMOS)-Ine(IMOS,VQ,XJ,IXJ,TJ)))}
.FUNC artanh(IMOS,VQ,XJ,IXJ,TJ) {0.5*log((1+x(IMOS,VQ,XJ,IXJ,TJ))
+ /(1-x(IMOS,VQ,XJ,IXJ,TJ)))}
.FUNC x(IMOS,VQ,XJ,IXJ,TJ) {(SQRT(Neff(TJ)**2+ps0(IMOS,VQ,XJ,IXJ,TJ)**2)
+ *tanh((Wb-XJ)/(2*lambda(IMOS,VQ,XJ,IXJ,TJ))))/
+ (Neff(TJ)+ps0(IMOS,VQ,XJ,IXJ,TJ)*tanh((Wb-XJ)/
+ (2*lambda(IMOS,VQ,XJ,IXJ,TJ))))}
.FUNC Rb(IMOS,VQ,XJ,IXJ,TJ) {(2*lambda(IMOS,VQ,XJ,IXJ,TJ)/(q*A*(un(TJ)+up(TJ))*
+ SQRT(Neff(TJ)**2+ps0(IMOS,VQ,XJ,IXJ,TJ)**2)))*
+ artanh(IMOS,VQ,XJ,IXJ,TJ)}
.FUNC VRB(IA,IMOS,VQ,XJ,IXJ,TJ) {IA*Rb(IMOS,VQ,XJ,IXJ,TJ)}
Avalanche breakdown equations
.FUNC dBVce(TJ) {BVce(TJ)-BVce0}
.FUNC BVce(TJ) {BVce0*(((T0+TJ)/300)**0.3)}
.FUNC Igen(XJ,TJ) {LIMIT((q*1e10*ni(TJ)*A*XJ)/taub(TJ),0,1e6)}
.FUNC Mav(VDK,TJ) {1/(1-((VDK/BVce(TJ))**6))}
.FUNC Iav(IMOS,VDK,VQ,XJ,IXJ,TJ) {(Mav(VDK,TJ)-1)*
+ (Ipc(IMOS,VQ,XJ,IXJ,TJ)+IMOS)+Mav(VDK,TJ)*Igen(XJ,TJ)}

Table 3.3: SPICE analytical functions of Kraus NPT model physical constants and modified equations as function of T_j.

Device models
.model M NMOS(Level=1, VTO={Vth}, KP={Kp})
.model DE D(Is={IsE0}, CJO={Cje})
.model DC D(IS={IsC}, CJO={Cjc}, BV={Bvce0})

Table 3.4: Mosfet and diodes models definition for PSpice NPT IGBT ET model.

Some numerical artifices have been made to enhance model convergence: for example, a multiplication coefficient of 1e-10 is used for intrinsic concentration $n_i(T_j)$ expression in order to avoid numerical overflow. As already mentioned in case of NPT base Kraus model presented in Appendix A, the expressions of both depletion region width x_j and quasi-neutral base region width w must be limited to a value slightly larger than zero (1e-4 cm), to avoid numerical overflow in analytical function such as *tanh(x)* and *sinh(x)* when the argument tends to zero. Although in case of NPT device depletion region never reaches the PNP emitter-base junction J_1 (x_j=W_B) and so w is always greater than zero for all collector-to-emitter V_{ce} voltage values before breakdown voltage, it may happen that a smaller value for W_B is chosen to achieve the best fitting in case of some devices of different technologies (FS or PT devices) and the problem of x_j=0 may occur.

3.3 Model validation

The so-constructed electro-thermal PSpice IGBT model based on the Non-Punch-Through structure is then validated on a commercial device with a rated blocking voltage of 600 V. The main characteristics of DUT are summarized in table 3.5:

Manufacturer	PN	Technology	Electrical ratings	
			$V_{ces}[V]$	$I_{ce,max}[A]$
Infineon	IGP30N60H3	FS trench-gate	600	30

Table 3.5: Electrical and technological characteristics of DUT.

For comparison, a PSpice model of the IGBT, based on Kraus-model too and provided free-available on the web by manufacturer, is considered: it offers the possibility to simulate device static and dynamic characteristics at a certain temperature value, but, since the temperature is simply a parameter and

not an intrinsic network voltage node, the model is not suitable for electro-thermal simulation. Furthermore, the PSpice OrCad emebedded Hefner-based NIGBT model is also used as benchmark for comparison with new model. A summary of characteristics and performances for the three considered models, is reported in fig. 3.17: although model provided by manufacturer is potentially the most accurate model, its implementation in PSpice simulator suffers from many problems, mainly concerning convergence properties and speed. On the other hand, Hefner PSpice NIGBT model is optimized in terms of speed and simplicity but its accuracy is not satisfying, and additions of other physical phenomena is not possible. Whilst, the new proposed Kraus-based model shows the best trade-off between accuracy, speed-convergence and ease of use, so it may represent a very useful tool for circuit simulation users.

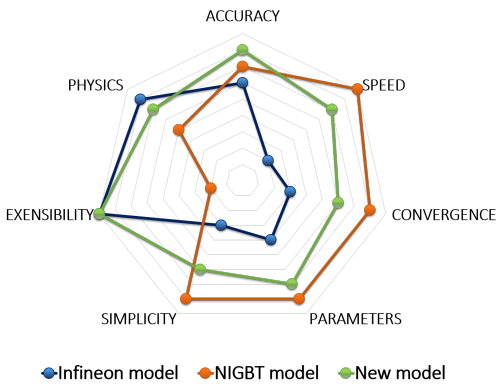


Figure 3.17: Analysis of main characteristics for three IGBT models implemented in PSpice.

As already discussed in chapter 2, authors in [35] suggest an useful and simple technique for Kraus model parameters extraction, from device experimental characteristics. Unfortunately, since the DUT doesn't have the Non-Punch-Through structure on which Kraus model is based, extracted values for some parameters may be not correct or physically consistent: it follows that a proper calibration of parameters is needed to fit experimental curves with simulated ones. In this work an automated calibration procedure based on curve-fitting method is proposed and discussed in Appendix B. Hence, the calibrated set of model parameters for DUT are reported in table 3.6.

In order to match device experimental characteristics at different temperatures, the thermal coefficients of Mosfet threshold voltage and transconduc-

Parameter	IGP30N60H3	Unit
A	0.15	cm^2
A_{gd}	0.11	cm^2
V_{th}	5.6	V
K_p	4.7	A/V^2
K_f	2.6	$none$
C_{ox}	7.5n	F
C_{gs}	2.5n	F
R_g	1	Ω
R_s	24.5m	Ω
W_B	65e-4	cm
N_B	2.2e15	cm^{-3}
τ_B	6e-8	s
I_{sE0}	1.5e-14	A
I_{sC}	1.35e-14	A
C_{jE}	450p	F
C_{jC}	450p	F
BV_{ce0}	770	V

Table 3.6: Model parameters for Kraus NPT model of IGP30N60H3.

tance, diode *DE* built-in voltage and carriers lifetime have been slightly adjusted.

3.3.1 Experimental test equipment

The experimental measurement of devices static and dynamic characteristics are performed using a laboratory automated tool designed ad-hoc for IGBT device characterization. The development of such a system, which is a custom tool, has been carried out in synergy with its manufacturer: starting from a list of requirements and design rules, all steps for system development have been verified and tuned to achieve the best trade-off between low measurement errors and used-friendly capability. The core of the system is the power stage, that is optimized in order to drastically reduce the value of parasitic elements: connection with DUT is realized by means a matrix output terminals configuration that is based on an half-bridge topology [6], shown in figure 3.18.

Hence, three output power terminals and two gate terminals are externally available, so module Half-bridge configuration can be tested: neverthless, it's possible to select only a single-stage configuration if the DUT is a single IGBT device.

[6] The half-bridge topology is "half" of an H-bridge, and it's formed by two cascaded power switches (IGBT, Mosfet, etc.) with both an anti-parallel freewheeling diode.

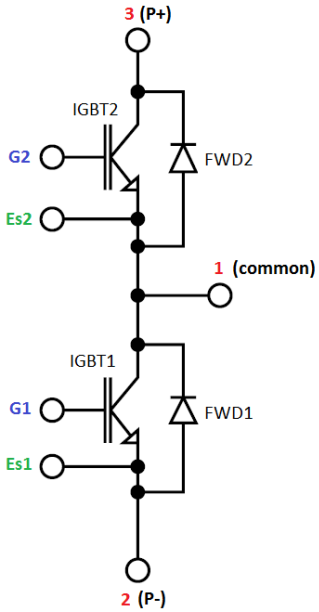


Figure 3.18: Schematic of the half-bridge configuration.

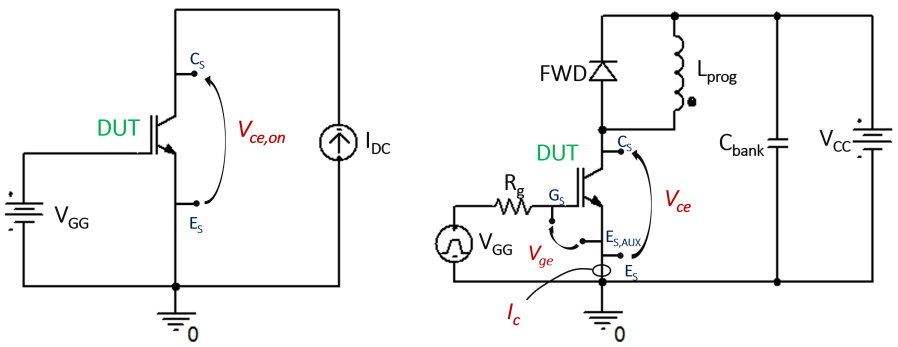


Figure 3.19: Simplified schematics of test circuits for a) IGBT on-state voltage-drop measurement and b)transient parameters measurements with single or double-pulse dynamic test.

The simplified schematics of measurement test circuits in case of static IGBT on-state voltage-drop measurement and dynamic parameters measurement with single or double-pulse test on a single IGBT DUT are depicted in fig. 3.19a-b: note that connection to DUT provides also sense terminals for voltage kelvin detection, in particular an auxiliary emitter terminal with its sense ($E_{S,AUX}$) is available for tests on module configuration which have a dedicated emitter terminal for gate-drive. The current probe is mounted on emitter side of IGBT that is grounded so the node experiences only little voltage variation during transient conditions and noise on current probe is reduced. System equipment includes:

- Low-Voltage (LV) source generator 30V max (for V_{ge} bias voltage);
- High-Voltage (HV) source generator 5kV max (for blocking mode);
- 2 High-Current (HI) source generators (200A max and 1kA max) (for conduction mode);
- a bank of power diodes for freewheeling;
- a capacitor bank and programmable inductor for dynamic test;
- a gate-driver (4A-30V) circuits;
- a 0.1 V/A (5kA max) 100MHz probe current;
- 1Gs 12-bit DSO (Digital Storage Oscilloscope).

The high-current (HI) source generators are designed to operate also as constant voltage generators in order to perform static measurement of device saturation current at high collector-to-emitter voltage (e.g., IGBT trans-characteristic). Voltage and current probes are all connected to the DSO on which a designed user-friendly interface is installed for system management: in particular software allows to set the layout of connection to DUT, to define test programs with a list of sequential electrical tests and to set the test conditions for each measurement. Definitively, system is capable to measure the following IGBT parameters:

Static parameters:
$I_{ces},\ I_{ges},\ V_{geth},\ V_{ce,on},\ g_m,\ V_{ges,ox}$;

Dynamic parameters (single-pulse or double-pulse test):
$E_{off},\ V_{ce,max},\ t_{d-off},\ t_f, E_{on},\ I_{ce,max},\ di/dt,\ t_{d-on},\ tr$;

Short-circuit parameters:
$V_{ce-sc,max},\ I_{ce-sc,max}$.

As concerns IGBT static parameters, bias-point measurement are performed once all test circuit conditions are set: user interface software offers also the possibility to perform parametric test, in which one of the test condition is varied. For instance, in case of on-state voltage drop measurement, the value of I_{dc} source generator pulse can be incremented from 0 to a desired max value by a defined step, in order to obtained the entire DC device output characteristic at certain V_{ge}. The pulse-width needs to be accurately chosen according to device ratings, thermal and package characteristics, in order not to increase device junction temperature at high current value. The time interval between two consecutive pulses is defined by design, and it assures isothermal conditions during multiple tests. On the other hand, device voltages and current waveforms during dynamic single or double-pulse test, are detected by probes and displayed on DSO: the triggering is performed in real-time according to measurements set conditions. A dedicated module of system software processes the acquired waveforms and evaluates device dynamic parameters. An external view of the overall system is depicted in fig. 3.20 and two main parts can be distinguished for user interface:

i) safety door for device fixture installation and drawer for device placement;

ii) LCD touch-screen with Digital Storage Oscilloscope (DSO) view.

According to the particular package in which DUT is assembled, there is a dedicated fixture which allows connection to the circuit output terminals matrix with package output pins by means spring contacts. In fact, once device package has been placed on the metal plate, the automatic drawer "pushes" the device against the spring contacts, ensuring low-resistance link. As regards the DUT, it's assembled in T0220 package, so an adapter is needed (fig. 3.20) too, between fixture contacts and plate. In order to perform measurements of device electrical characteristics at high temperature, the temperature of metal plate, on which device is placed, is regulated via a thermostat.
Although system is a powerful and effective optimized tool for IGBT electrical characterization, the accuracy of measurement results must be analyzed

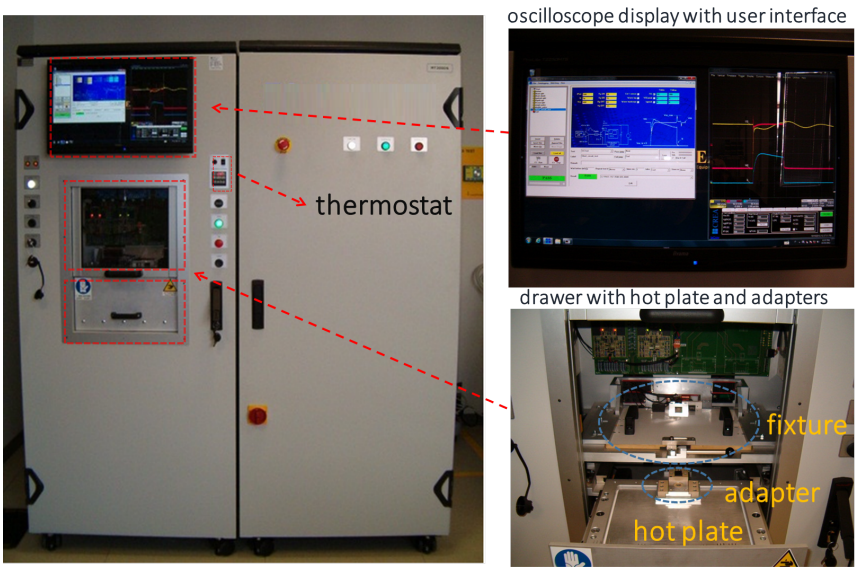


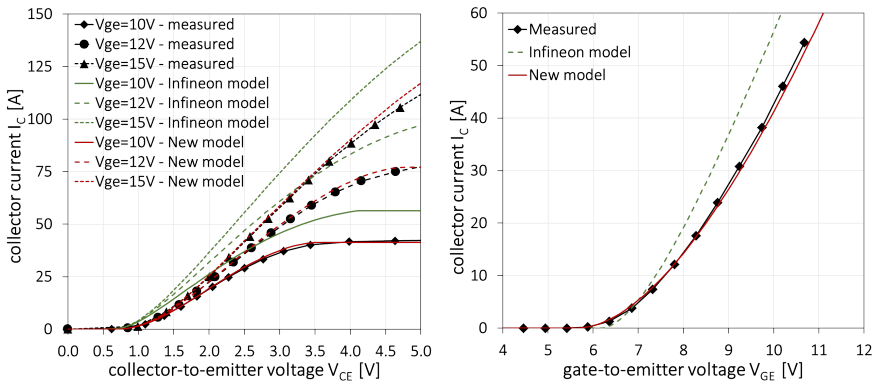
Figure 3.20: Overview of laboratory tester used for IGBT experimental characterization.

and verified by means a comparison with measures acquired on reference instruments. Hence, a complex and detailed procedure for system accuracy definition and evaluation of measurement errors is prepared, which is based on statistical *gage study* analysis.

3.3.2 IGBT characteristics at $T_j = 27\ ^\circ\mathrm{C}$

The effectiveness and accuracy of optimized PSpice electro-thermal NPT IGBT model is demonstrated by comparing simulated device characteristics with experimental curves. The experimental test circuits shown is fig. 3.19a-b are replicated in SPICE OrCad schematic environment and all circuit parasitic inductances, capacitances and contact resistances, properly evaluated, are considered in order to reproduce, in simulation, the same circuit conditions device experiences in real circuit. As already mentioned, simulation of IGP30N60H3 device characteristics with PSpice model provided by manufacturer are also considered for comparison. On the contrary, simulation results obtained with Hefner model are further from device experimental behaviour, so it's not considered in plots. In fig. 3.21a the IGBT DC output character-

istics at different gate-to-emitter voltage values and at ambient temperature T_j=27 °C are plotted: the new proposed model shows better accordance with experimental results, both in linear region and near the saturation region than the Infineon model. In particular the activation of PNP emitter-base junction is well-modeled by SPICE diode DE model and parameter I_{sE} (reverse saturation electron current). At high gate-to-emitter bias voltage, the non-linearity with current of PiN injection effect isn't taken into account with the constant parameter K_f: anyway, the difference with device experimental behaviour is negligible, even for model applications in short-circuit conditions where the device operates near the saturation region.



(a) (b)

Figure 3.21: Simulated and experimental IGBT a) DC output characteristics @V_{ge}=10-12-15V and b) transfer-characteristic @V_{ce}=10V, at ambient temperature for IGBT IGP30N60H3: comparison between PSpice model provided by manufacturer and new proposed model.

In fig. 3.21b, the experimental and simulated IGBT transfer-characteristics at V_{ce}=10V (T_j=27 °C) are depicted: the use of only two parameters, V_{th} and K_p for SPICE Level 1 Mosfet model is enough to assure a good fitting with the experimental curve. Note that maximum collector current value for experimental curve measurement is close to I_c=60A, since the high power delivered to device in this test is such that isothermal condition cannot be assumed for larger current values. On the contrary, although in the Infineon model a SPICE Level 3 Mosfet model is used with more physical parameters, results are very far from device real behaviour and DUT 1 saturation current is overrated even

at very low gate-to-emitter voltage values.

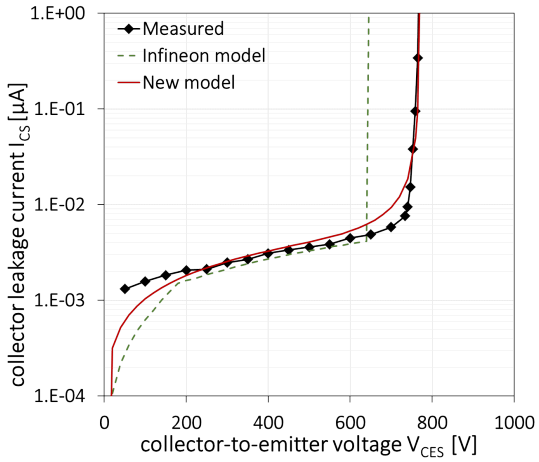


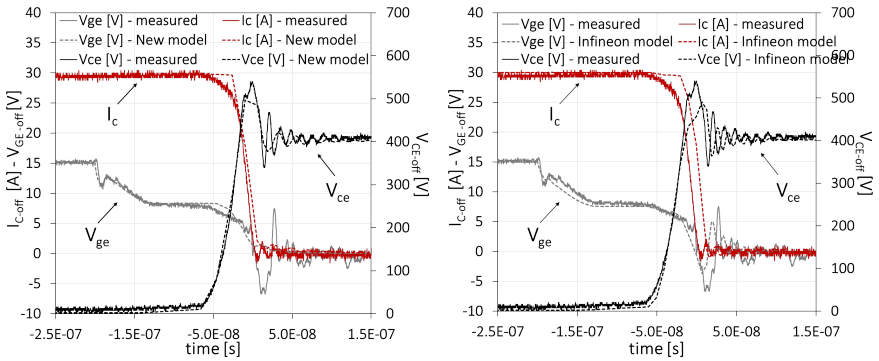
Figure 3.22: Comparison between Infineon model and the new model of DUT on simulated IGBT blocking characteristics ($T_j = 27$ °C), respect to experimental curve.

The device experimental DUT blocking characteristic (V_{ge}=0V) at ambient temperature is plotted in fig. 3.22: as happens for most of semiconductor devices, effective device breakdown voltage ($BV_{ce} \simeq$770V) is much larger than rated blocking voltage (600V for this DUT): this value must be correctly evaluated for device PSpice model because it represents a precious information for circuit designers who must guarantee device operation far from avalanche conditions, especially when hard-switching turn-off transient causes high overvoltages. Furthermore, the avalanche typical behaviour near the breakdown voltage is properly reproduced by new model respect to Infineon model, where conversely the avalanche modeling, assigned to the SPICE diode model *DC*, is obtained with a simple exponential function.
The DUT behaviour during experimental measurement of inductive turn-off transient is depicted in fig. 3.23. Circuital conditions for single-pulse test are:

- steady-state collector current before turn-off I_{cc}=30A (rated current);
- DC link voltage V_{cc}=400V (2/3 of rated blocking voltage);
- gate-to-emitter driver voltage V_{gg}=0-15V;

- gate turn-off resistance R_{g-off}=10 Ω (recommended in device datasheet);

device is assumed to be at T_j=27 °C during the entire transient (isothermal conditions).



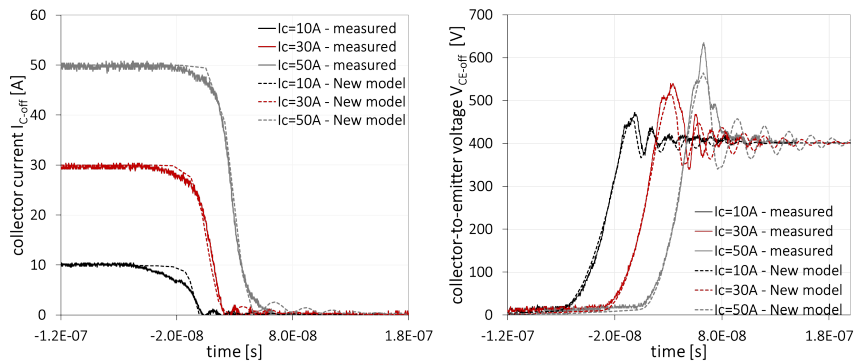
(a) Measured VS new-model.

(b) Measured VS manufacturer model.

Figure 3.23: Current and voltage waveforms during turn-off transient on inductive load with I_{cc}=30A, V_{cc}=400V and R_{g-off}=10 Ω: comparison between experimental and simulated curves.

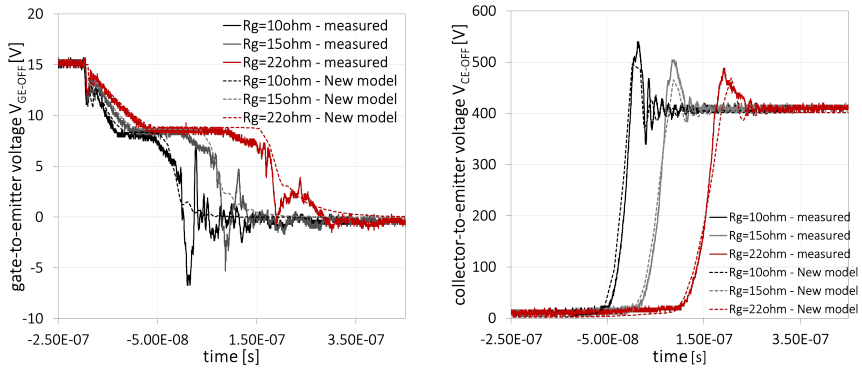
The new proposed model (fig. 3.23a) assures a good accordance with experimental results as well as Infineon model (fig. 3.23b): the only significant difference concerns the behaviour of gate-to-emitter voltage V_{ge} waveform after Miller's plateau, that is influenced by C_{oxd} and C_{gs} parameter values. Unlike the new model in which a constant value is used for both capacitances, in Infineon model C_{oxd} and C_{gs} are modeled as non-linear function of respectively Mosfet gate-to-drain and gate-to-emitter voltages. Nevertheless, this small increase in model accuracy is paid with a significant reduction of model speed and convergence properties: in fact, one of the main issue for Infineon model regards its convergence capability, especially when device is operating in complex circuits or hard switching conditions. Furthermore, it's clear from device V_{ge} experimental waveform that the non-linearity of device MOS gate-to-drain capacitance C_{gd} causes two regions of different slopes during Miller's plateau and produces a slow initial decay of device collector current: hence, the modeling of C_{gd} by means the function *Vdep* in both models is not capable of reproducing this behaviour. However, the decay rate of device collector

current is very fast and doesn't show the typical IGBT current tail, according to the low value of evaluated carrier lifetime τ_B parameter: in case of Infineon model, the variation of collector-to-emitter votlage dV_{ce}/dt just before it reaches the DC link voltage V_{cc}, results in a larger turn-off delay time t_{d-off}, that causes a delay also on current waveform.
The capability of new proposed Kraus-based model to reproduce DUT electrical characteristics, is also demonstrated by considering device operation in other device circuit conditions: for example, in fig. 3.24a-b DUT collector current I_c and collector-to-emitter voltage V_{ce} are plotted during device turn-off transient at different initial inductor current values and same DC link voltage V_{cc}=400V and gate resistance R_g=10 Ω. The slow initial collector current decay previously observed, is more pronounced at low current values: in fact, the effect of C_{gd} capacitance doesn't depend on carriers charge rate, so its contribution is constant with injection level. In addition, fig. 3.25a-b depicts the DUT gate-to-emitter and collector-to-emitter voltage waveforms during inductive turn-off by varying the gate resistance R_g value: new model properly reproduces the Miller's plateau effects, except for the issues related to nonlinear C_{gd} and double-slope, discussed before.



(a) (b)

Figure 3.24: Waveforms of a) collector current I_c and b) collector-to-emitter voltage V_{ce} during turn-off on inductive load with V_{cc}=400V, R_{g-off}=10 Ω and different initial inductor current value: comparison between IGP30N60H3 experimental and simulated (with new model) curves.



(a) (b)

Figure 3.25: Experimental-simulated DUT waveforms of a) collector-to-emitter voltage V_{ce} and b) gate-to-emitter voltage V_{ge} during turn-off on inductive load with I_{cc}=30A, V_{cc}=400V and different values of R_{g-off}.

3.3.3 Behaviour VS junction temperature

The device isothermal static and dynamic characteristics at different junction temperatures T_j are experimentally measured with the laboratory test setup: once the temperature of metal base on which device is placed is set to the required value, the drawer pushes the device against the spring contacts, assuring a good thermal contact between the metal basis (acting as an ideal heatsink at constant temperature) and the device metal plate. Moreover, a thermocouple is properly mounted to verify, before running the test, that thermal transient is extinguished and device junction has reached the required temperature value. The range of set temperature values is from ambient temperature T_j=27 °C to T_j=175 °C, that is the maximum device junction temperature declared in datasheet. On the other hand, device characteristics are simulated in PSpice OrCad environment for different junction temperature conditions in case of both new proposed model and Infineon model: the temperature is considered as a constant circuit parameter and, since the new model is arranged for electro-thermal simulation and temperature is a network voltage node, a voltage DC source of value equal to T_j must be connected to the external device temperature terminal, as shown in fig. 3.26.

The isothermal steady-state output characteristics at gate-to-emitter volt-

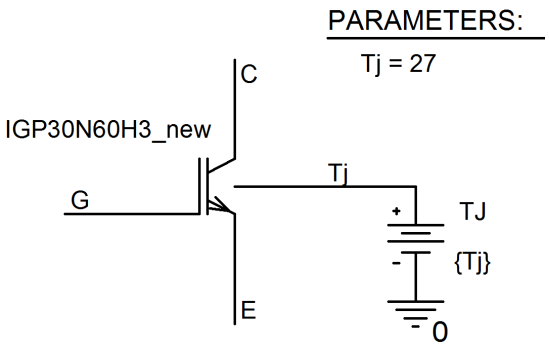
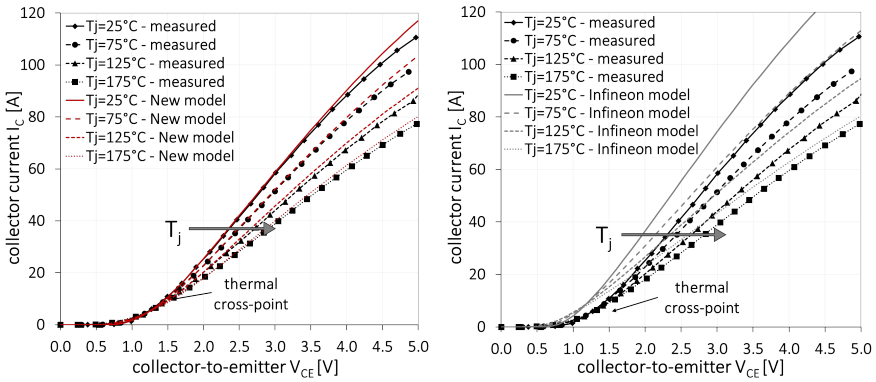


Figure 3.26: Setting of constant temperature T_j for new-model PSpice simulation.

age V_{ge}=15V and increasing device junction temperatures, experimentally measured on DUT IGBT, are compared with results obtained in PSpice simulations using respectively the new model and the Infineon model (fig. 3.27a-b). The new model shows good compliance in reproducing collector-to-emitter voltage drop behaviour with temperature throughout the linear region: in particular the typical *thermal cross-point* that is responsible for thermal slightly positive coefficient of IGBT on-state voltage drop close and beyond to the device rated current [7] is successfully achieved. The main lack shown by Infineon model, as already pointed up, regards the activation of base-emitter junction J_1 and thus its built-in voltage: this is properly fit in new model using the parameter I_{sE} and its temperature dependence together with controlled voltage source *dVDE*. The behaviour of IGP30N60H3 collector current with temperature in the saturation region is well-described by experimental measurement of transfer-characteristic at collector-to-emitter voltage V_{ce}=10V depicted in fig. 3.28a: the thermal negative coefficients of MOS threshold voltage V_{th} and MOS transconductance K_p result in a thermal cross-point too. Since the DUT transfer-characteristic at different temperature are very close, PSpice simulated curves using both new and Infineon models are plotted in fig. 3.28b in order to make them clearer: while Infineon model, that even incurs convergence problems for simulation at temperature above T_j=75 °C, is not capable of reproducing the device experimental behaviour, the new model shows an

[7] A positive thermal coefficient of IGBT on-state voltage drop in a wide range of DC collector current values is strongly desired by module and converter designers since it prevents thermal runaway when same devices are mounted in parallel.

optimum accordance with experimental results, even at high collector current values.

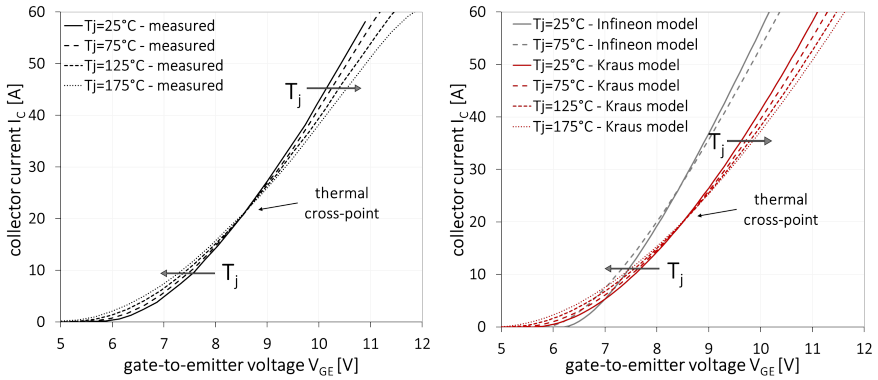


(a) New PSpice model. (b) Manufacturer model.

Figure 3.27: Experimental and simulated DUT DC output characteristics @V_{ge}=15V and different junction temperature T_j.

A correct modeling of device avalanche behaviour with temperature at high collector-to-emitter V_{ces} voltage (with V_{ge}=0V) up to breakdown voltage is crucial for a first investigation of device electrical performances in avalanche conditions aimed to circuit design. Moreover, the thermal behaviour of IGBT leakage collector current may be a heavy constraint for converter designers in calculation of device losses, influencing the choice of a device rather than another. Hence, by using the new optimized PSpice IGBT model, the DUT experimental blocking characteristics at different temperature values are properly reproduced in simulation (fig. 3.29), assuring high speed and convergence rate too. On the contrary, in Infineon model, the use of a PSpice diode model does not give a realistic behaviour of avalanche effect at ambient temperature and therefore with increasing temperature: the DUT blocking characteristic at T_j=75 °C is even overlapped on that at room temperature and the obtained values for leakage current at rated blocking voltage 600 V are considerably lower than experimentally measured ones. Furthermore, since diode model parameter BV used for IGBT breakdown voltage modeling is not considered as temperature dependent, the typical slightly positive coefficient of IGBT breakdown voltage observed on experimental curves is not taken into account.

As concerns IGBT dynamic characteristics, the phenomenon which is



(a) Measured. (b) Simulated.

Figure 3.28: IGP30N60H3 IGBT transfer-characteristic at @V_{ce}=10V and different junction temperature T_j.

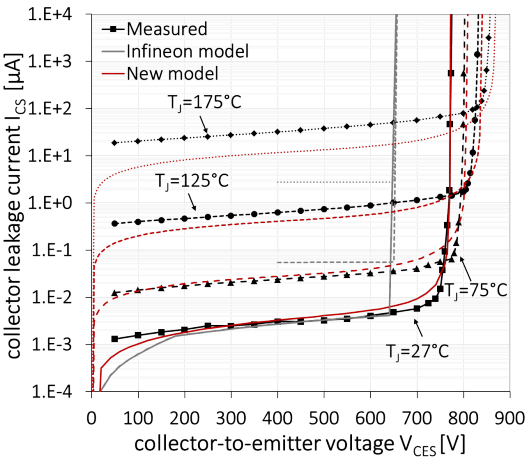
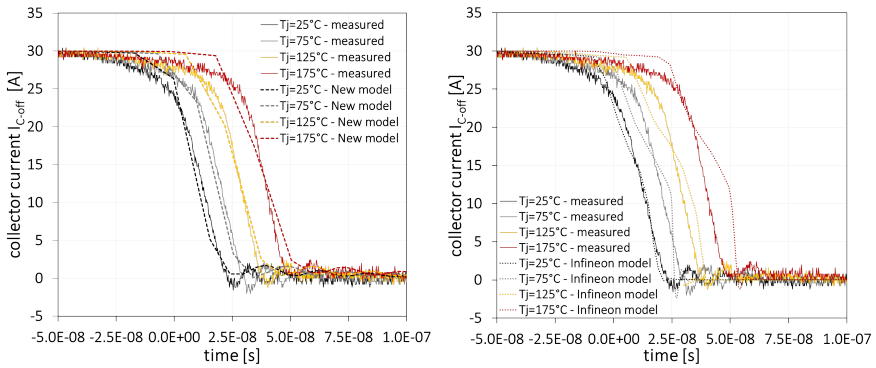


Figure 3.29: Comparison between new model and Infineon model simulated blocking characteristic @T_j=27-75-125-175 °C respect to experimental curves for DUT IGBT.

more affected by the variation of device junction temperature is the behaviour of current tail, mainly due to the increase of base carrier lifetime τ_B with temperature. From experimental measurements of DUT collector-current acquired during turn-off transient at V_{cc}=400V, I_{cc}=30A, R_{g-off}=10 Ω and at different temperatures on inductive load (fig. 3.30), it's clear that thermal coefficient of carriers lifetime is almost negligible, and current waveforms remains the same in the range of temperature from 27 °C to maximum device temperature 175 °C.



(a) New PSpice model.

(b) Manufacturer model.

Figure 3.30: Simulated and experimental IGBT collector current waveforms obtained during DUT turn-off switching on inductive load at different constant temperature values and V_{cc}=400V, I_{cc}=10A R_g=10 Ω.

In conclusion, the improved and optimized version of electro-thermal NPT IGBT model based on Kraus model and implemented in PSpice OrCad simulator shows a better trade-off between accuracy and speed-convergence properties compared to models such as Hefner model and Infineon one, which are currently the most widespread tools adopted by users of SPICE circuit simulators. In fact, although model is based on the simple IGBT Non-Punch-Through structure, excellent results are achieved also in case of more complex device structures, as, for example, the Field-Stop trench-gate IGBT used as DUT for model validation: this is also fulfilled, thanks to a proposed efficient automated parameters calibration procedure implemented in MATLAB environment [5], which allows to define a set of model parameters applying a

curve-fitting method. In the next chapter some case-studies of IGBT circuital application will be presented and the effectiveness of the new model to predict device behaviour in several operating conditions will be demonstrated with reference to experimental measurements.

Chapter 4

Effective circuit design using ET IGBT model

The availability of a reliable, flexible and fast compact model may be very important for both IGBT device designers and circuit engineers, since it can be a useful tool for predictive investigation of device behaviour in certain operating conditions, for optimization of converters design and for simulation analysis of more complex device physical phenomena by means a combined CAD methodology. In this chapter some case-studies of IGBT circuit applications are presented in order to demonstrate the effectiveness of PSpice IGBT model to reproduce real device behaviour at different operating conditions: the aim is, as usual, to confirm some experimental results and extends the analysis to other conditions by using the validated simulation tool in place of experimental measurements, which are often heavy, long and difficult to perform. Furthermore, in some cases, a simulation analysis may be carried out on device physical phenomena which can't be even experimentally measured or detected, and this may provide lot of precious information for further device improvements and future developments.

4.1 Short-circuit test ET simulation

The first circuit application considered as a case-study for new PSpice ET model validation, is the standard Short-Circuit (SC) test, that is usually performed by device users in order to verify its capability to sustain both high-voltage and high-current values during a certain time interval, before thermal runaway occurs, which brings the device to the destruction. Indeed, the in-

vestigation of device short-circuit capability, provided by manufacturers on the datasheet in terms of maximum SC time interval τ_{SC} and maximum SC collector current $I_{c,SC}$ at certain conditions [1], is performed by devices designers with combined analysis of TCAD simulations and experimental results, because of the complex electro-thermal physical phenomena occuring within device structure during a short-circuit event [67]. Therefore, IGBT compact models are not suitable for this kind of analysis and neither the addition to the model of a NPN bipolar transitor responsible for latch-up at high collector current, as proposed in [42], is exhaustive for an accurate description of physical effects which determine the device failure. However, IGBT compact models are an effective tool for evaluation of device electro-thermal behaviour during short-circuit events below the critical conditions given on datasheet: for instance, it's possible to investigate in simulation the effects of device self-heating on short-circuit collector current slope, the transient device junction temperature behaviour, as well as the maximum collector-to-emitter voltage peak during device turn-off at high SC currents [68]. These information may be crucial for circuit designers who have to select the right device in order to achieve the optimum design.

4.1.1 SC test configuration

For new PSpice model validation analysis under SC test conditions, some experimental measurements on a DUT commercial IGBT device have been performed in laboratory by using the automatic tester equipment presented in chapter 3, in which the hardware and the software requirements for standard short circuit test execution are properly implemented: once the SC test conditions, summarized in table 4.1, are defined, it's possible to acquired device voltages and current waveforms during short-circuit test by means the embedded digital storage oscilloscope (DSO). The system user interface also returns information about maximum collector current $I_{c,SC}$ and collector-to-emitter voltage $V_{ce,SC}$ peak value.

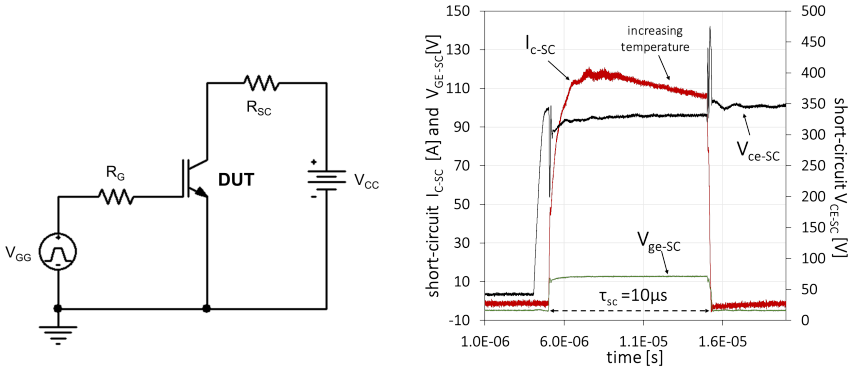
The simplified schematic of experimental short-circuit test setup is depicted in fig. 4.1b. An example of typical experimentally measured IGBT gate-to-emitter voltage V_{ge}, collector-to-emitter voltage $V_{ce,SC}$ and collector current $I_{c,SC}$ waveforms during a short-circuit event of τ_{SC}=10 μs time duration at V_{cc}=350V, V_{ge}=-5/15V, R_g =10 Ω and T_j=27 °C conditions, is reported

[1] The short-circuit test conditions are related to gate-to-emitter V_{ge} voltage, DC link voltage V_{cc}, gate resistance R_g and device junction temperature T_j values: sometimes also the value of stray inductance L_σ is given.

τ_{SC}	V_{ge-}, V_{ge+}	V_{cc}	R_g	T_j
$[\mu s]$	$[V, V]$	$[V]$	$[\Omega]$	$[^\circ C]$
$1 \div 50$	$-30 \div 0/0 \div 30$	$10 \div 1k$	$1 \div 63$	$27 \div 175$

Table 4.1: Test conditions for SC measurement on tester equipment.

in fig. 4.1a: it's possible to appreciate two major effects which are important for circuit designers, which are the device self-heating, that is deduced from negative slope of IGBT collector current with time, and the V_{ce} voltage overshoot due to circuit stray inductance.



(a) (b)

Figure 4.1: a) SC test measurement setup; b) experimental IGBT voltages and current short-circuit waveforms at τ_{SC}=10 μs, V_{cc}=350V, V_{ge}=-5/15V, R_g=10 Ω and T_j=27 °C.

The device used as DUT for SC measurements is the same adopted for model validation in chapter 3, that is the Infineon IGP30N60H3 Field-Stop trench-gate IGBT, rated 25 A-600 V. The equivalent schematic of short-circuit experimental test-circuit implemented in PSpice OrCad for simulations, is depicted in fig. 4.2a: stray inductances due to wire connections to IGBT gate, emitter and collector terminals are considered as well as the series resistance R_{SC} used in real circuit to limit the short-circuit current in case of device failure, which are the most important and critical parasitic parameters in this kind of test.

Moreover, since during a short-circuit event the IGBT experiences a huge power dissipation caused by high-voltage and high current conditions, the Fos-

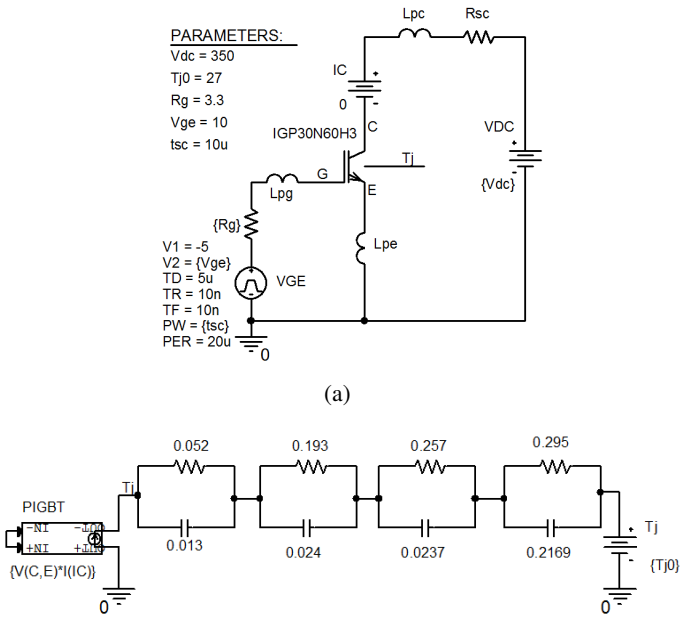


Figure 4.2: PSpice OrCad equivalent schematics of a) short-circuit test experimental setup and b) Foster DUT IGBT thermal network.

ter equivalent thermal network provided by the device manufacturer on the device datasheet, is also taken into account in PSpice simulation in order to investigate the transient behaviour of junction temperature due to device self-heating. The equivalent thermal network is given in datasheet for junction-to-case thermal description, so no heatsink is considered in case of the experimental measurements. In order to perform SC measurements at different initial IGBT junction temperature values, the device is arranged on an hot metal plate, whose temperature is set via an embedded control unit: thus, a thermocouple is mounted inside an hole made through the device package to verify that steady-state junction temperature is actually at desired value. As concerns the set of parameters defined for new PSpice ET model of DUT IGBT, they are listed in table 3.6.

4.1.2 Experimental and simulation results

Hence, experimental measurements are compared with simulation results obtained using the new electro-thermal PSpice model at different SC test conditions in order to verify model capability to reproduce real IGBT behaviour and to predict transient junction temperature, according to device power dissipation and thermal network accurate model. The experimental IGBT voltages and current waveforms taken as reference for calibration of SC test setup parasitic elements, has been acquired during a test performed at τ_{SC}=10μs, V_{cc}=350V, V_{ge}=-5/15V, R_g =10 Ω and T_j=27 °C conditions, which are below the maximum critical conditions suggested in the DUT datasheet: the comparison between experimental and simulation results, reported in fig. 4.3, shows the good accuracy of new model in reproducing the IGBT saturation current even at very high values of collector-to-emitter V_{ce} (350V) and at certain gate-to-emitter voltage value. Furthermore, simulated IGBT collector current $I_{c,SC}$ curve also properly matches the experimental one, which is influenced by the effects of device self-heating: in fact, since fast and large variations of junction temperature during short-circuit transient is very difficult to be experimentally measured, the information on collector current slope may be precious to determine the device temperature behaviour, by means an accurate model of thermal network.

Note that the experimental IGBT collector-to-emitter voltage waveform remains equal to zero before the voltage pulse is applied across gate-emitter IGBT terminals because of a series switch connected between DUT and DC power supply: the switch serves to protect other components of circuit in case of DUT failure event, and it's not directly included in PSpice implementa-

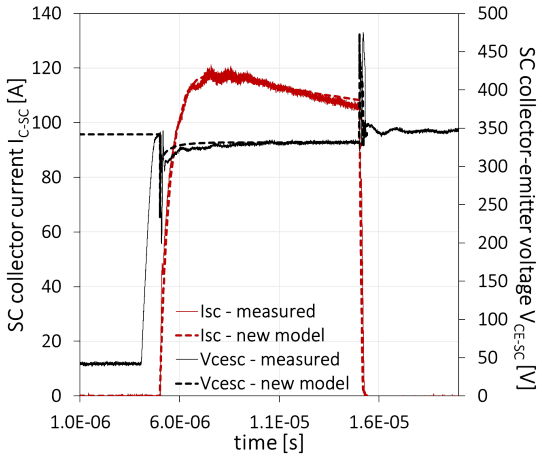
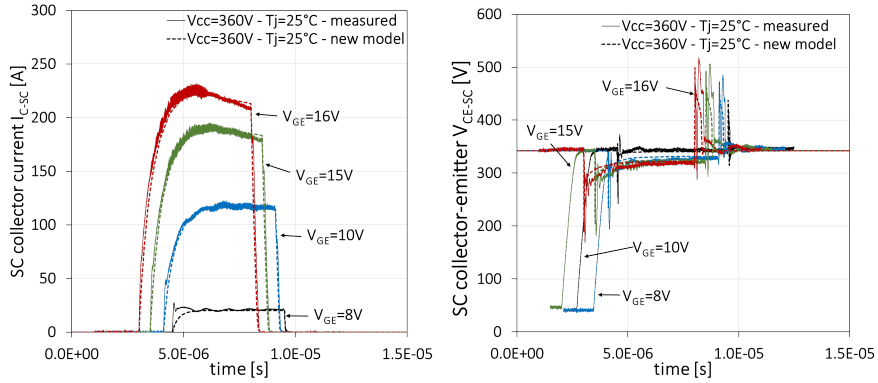


Figure 4.3: Comparison between experimental and simulated $V_{ce,SC}$ and $I_{c,SC}$ short-circuit waveforms at τ_{SC}=10 μs, V_{cc}=350V, V_{ge}=-5/15V, R_g=10 Ω and T_j=27 °C.

tion of circuit, though its influence on IGBT electrical behaviour during τ_{SC} time interval is taken into account within the calibrated L_{pc} and R_{sc} values. Once parasitic elements of equivalent PSpice schematic that models the laboratory SC test setup have been properly calibrated, test conditions are varied to investigate the device response and to verify if the proposed PSpice model still maintains its good properties in terms of accuracy even when device is stressed with SC current-voltage conditions close to the critical ones. Although one of the most important parameters for SC reliability test usually performed by device or circuit designers is the DC link voltage V_{cc}, that is equal to the collector-to-emitter voltage IGBT should sustain when it experiences a short-circuit event in a particular application, there are only a few cases of circuital applications in which it exceeds the previously considered value of 350V. On the contrary, the gate-to-emitter V_{ge} voltage value strongly depends on the particular converter application and it may vary in the range from 8V to 20V. Therefore, some experimental measurements of DUT short-circuit collector current (fig. 4.4a) and collector-to-emitter voltage (fig. 4.4b) waveforms have been performed at different positive V_{ge} voltage values and V_{cc}=350V, V_{ge}=-5/15V, R_g=10 Ω and T_j=27 °C: the SC pulse width is τ_{SC}=5 μs, since it's guaranteed on the datasheet as the maximum short-circuit time interval before device failure.

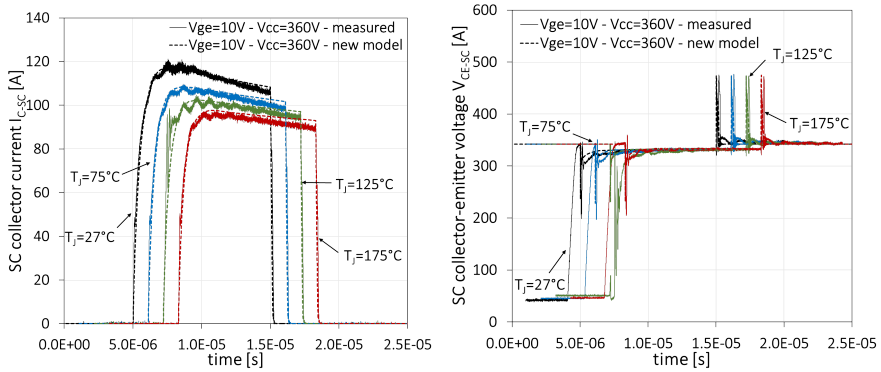


(a) $I_{c,SC}$ waveforms. (b) $V_{ce,SC}$ waveforms.

Figure 4.4: DUT IGBT measured and simulated voltage and current waveforms during SC test at τ_{SC}=5 μs, V_{cc}=350V, V_{ge-}=-5V, R_g=10 Ω, T_j=27 °C and different values of V_{ge+}.

The simulated DUT voltage and current waveforms using the PSpice new model, accurately follow the behaviour of real device at different gate-to-emitter positive pulse voltage values: the increase of IGBT collector current with V_{ge} is well reproduced as well as the effect of device self-heating, which strongly depends on DUT transient power dissipation, and so it's more evident at larger V_{ge} values. Furthermore, the experimental behaviour of both negative and positive $V_{ce,SC}$ voltage overshoots with saturation current occurring respectively during IGBT turn-on and turn-off transient (fig. 4.4b) and mainly due to collector-side stray inductance L_{pc}, is also well reproduced by model, that reveals a useful tool to predict the effects of circuit parasitic elements on device electrical behaviour at certain conditions. Since IGBT operation DC junction temperature in power converter applications may varies from values close to room temperature to maximum temperature declared by device manufacturer on datasheet (usually is $T_{j,DC}$=175 °C) depending on device average power dissipation and on heatsink and cooling strategies adopted by circuit designers, it becomes very interesting to know about IGBT short-circuit electrical and thermal transient behaviour at different steady-state temperature values: as demonstrated in figures 4.5a-b, where a comparison between measured and simulated IGBT short-circuit collector current $I_{c,SC}$ and collector-to-emitter voltage $V_{ce,SC}$ is performed at different steady-state junction temperature T_{j0}

values, the new PSpice model is capable to accurately follow the trend of saturation current with initial IGBT junction temperature. Moreover, this analysis shows how it's possible to effectively use compact ET model such as the new proposed model within PSpice simulator environment, in order to monitor the instantaneous transient IGBT junction temperature during a short-circuit: as depicted in fig. 4.6, since the short-circuit IGBT power dissipation reduces slightly with increasing steady-state temperature conditions, the ΔT_j between initial and final temperature value is actually the same. Hence, in case of SC event, device may reach a critical temperature condition if DC thermal constraints, which are related to IGBT DC power dissipation, heatsink and cooling techniques are not properly taken into account and well designed.



(a) $I_{c,SC}$ waveforms. (b) $V_{ce,SC}$ waveforms.

Figure 4.5: Short-circuit test on DUT IGBT during SC test at τ_{SC}=5 μs, V_{cc}=350V, V_{ge}=-5V/10V, R_g=10 Ω VS T_j: comparison between measured and simulated device voltage and current waveforms.

4.2 Switching losses prediction in DC-DC converter

The PWM (Pulse-Width-Modulation) DC-DC converters have been very popular for the last three decades, and are widely used at all power levels. Advantages of PWM DC-DC converters include:

- low component count;
- high efficiency;

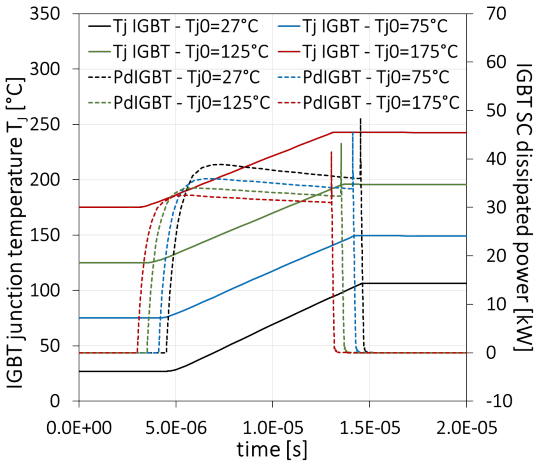


Figure 4.6: Simulation of IGBT transient junction temperature and power dissipation behaviour during short-circuit event at different steady-state T_{j0} values.

- constant frequency operation;
- relatively simple control;
- commercial availability of integrated circuit controllers;
- high conversion ratios (in both step-down and step-up applications).

A drawback is that PWM rectangular voltage and current waveforms may cause high turn-on and turn-off losses in semiconductor devices, which limit practical operating frequencies to hundreds of kilohertz: rectangular waveforms also inherently generate EMI [69]. These constraints make the design of a DC-DC converter very tricky, since the choice of the power device becomes critical to achieve the best performance in terms of efficiency, reliability and EMI compatibility. In particular, nowadays the design of DC-DC converters used for motor-drive medium-power application involving IGBT devices, is mainly done with the aid of simulation tools such as SPICE circuit simulators, so accuracy and reliability of IGBT compact model is critical for the proper evaluation of devices losses and overall performances aimed to the a best choice of the device.

4.2.1 Buck converter design

As a case-study for predictive simulation analysis of IGBT performances in a DC-DC converter using the new PSpice model, a simple step-down or Buck converter is considered [70]: according to design specifics listed in table 4.2, the converter is designed and then realized in laboratory.

Design specific	Value
V_{in}	350 V
V_{out}	150 V
I_{out}	6.5 A
f_{sw}	10 kHz
ΔV_{out}	10%
$I_{L,max}$	10 A

Table 4.2: Buck converter design specifics.

In order to satisfy design specifics and guarantee circuit operation in *Continous Current Mode* (CCM) values for L and C_{out} parameters, which determine respectively the ripple of inductor current and of output voltage are evaluated from equations reported in [70]. The main step-down converter parameter is the duty-cycle D of PWM signal applied to the IGBT gate, and it's related to converter input and output voltages, V_{in} and V_{out}, according to expression:

$$V_{out} = D\, V_{in} \quad \Rightarrow \quad D = \frac{V_{out}}{V_{in}} = \frac{150}{350} \cong 0.429 \tag{4.1}$$

The load is assumed to be pure resistive so the value of load resistor is $R_L = V_{out}/I_{out} \cong 23\Omega$. The value of filter inductor L must be chosen larger than the value L_{min}, which defines the edge between CCM and DCM (*Discontinuous Current Mode*) converter operation modes:

$$L > L_{min} = \frac{D}{2 f_{sw} I_{L,max}} V_{out}(1 - D) \cong 500\mu H \tag{4.2}$$

where $I_{L,max}$ is the maximum inductor current given as design specific. The actual value of L used in laboratory circuit implementation is $1.55mH$. For converter output capacitance C_{out} evaluation, the following equation is used:

$$C_{out} = \frac{1}{8 f_{sw}^2 L} \frac{V_{out}}{\Delta V_{out}}(1 - D) \Rightarrow C_{out} = 4.7\mu F. \tag{4.3}$$

As concerns the IGBT device acting as switch in the step-down converter, the IRG4PC30S Punch-Through planar-gate IGBT rated 25 A with blocking

voltage of 600 V is chosen according to converter current and voltage maximum values. On the contrary, the device 8ETH06, rated 8 A and 600 V, is considered as freewheeling diode. The equivalent schematic of designed step-down converter implemented in PSpice OrCad environment for simulation analysis is depicted in fig. 4.7: parasitic elements are considered to take into account the actual layout of circuit laboratory realization. Note that an alternative version of the standard buck converter with IGBT emitter connected to ground and floating load is realized in order to use a simplified gate-driver (with a grounded power supply) and to reduce the noise on current probe by arranging it on the emitter side of IGBT.

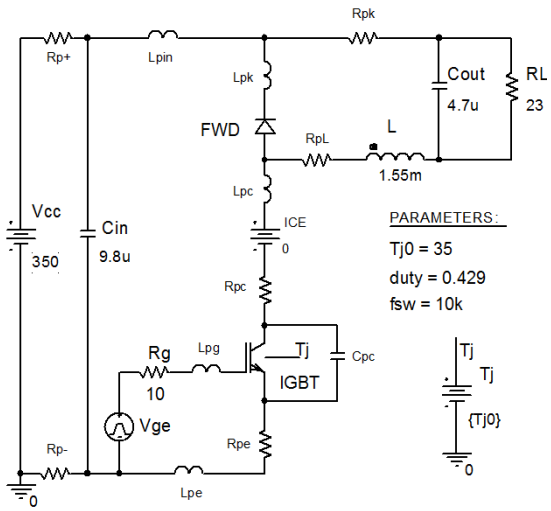


Figure 4.7: PSpice OrCad equivalent schematic of implemented DC-DC buck converter.

An experimental setup is arranged in order to measure IGBT losses and its impact in overall circuit efficiency $\eta = P_{buck,IN}/P_{buck,OUT}$, during DC-DC converter steady-state operating conditions. The test equipment includes:

- TDK Lambda 600V 0÷2.6A DC power supply;
- Agilent E3631A 0÷ 6V.5A/0÷± 25V.1A DC power supply;
- Agilent 33522A 250MSa/s 30MHz Function/Arbitrary Waveform Generator;

- LeCroy Waverunner 44xi 400MHz 5Gs/s Oscilloscope;
- Yogogawa WTP110 20A 600V Digital Power Meter;
- Zimmer LMG95 20A 600V Power Meter;
- LeCroy AP015 Max 50A DC÷50MHz current probe;
- Testec TTSI9110 100MHz 1:100/1:1000 voltage differential probe.

In fig. 4.8 an overview of the laboratory implementation of buck converter is given: since the optimization of converter is not the aim of this analysis and parasitic elements are not critical for circuit performances due to small number of components, a prototype version of circuit is realized, for simplification, on a holed board using "manhattan mount" technique. Both the IGBT and the freewheeling diode are mounted on a larger heatsink in order to assume the heatsink is always at room temperature T_{amb}=27 °C.

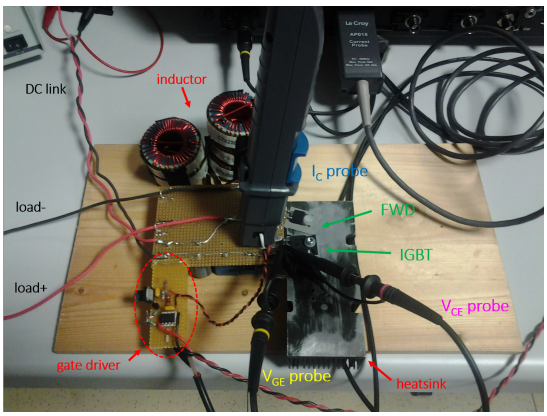


Figure 4.8: PSpice OrCad equivalent schematic of implemented DC-DC buck converter.

Experimental measurements of IGBT voltages and current waveforms (V_{ge}, V_{ce} and I_c) and converter input-output powers ($P_{buck,IN}$ and $P_{buck,OUT}$) are performed at IGBT thermal steady-state conditions, when all thermal transients are extinguished, during converter DC operation mode. The IGBT junction temperature steady-state value T_{j0} is measured by means a thermocouple mounted close to device junction, through an hole made into IGBT package. Hence, isothermal conditions are assured for IGBT and converter simulation is performed assuming constant device junction temperature equal T_{j0}= 35 °C.

New NPT-ET PSpice model: IRG40C30S		
Parameter	**Value**	**Unit**
A	0.171	cm^2
A_{gd}	0.023	cm^2
V_{th}	5.75	V
K_p	3.75	A/V^2
K_f	3.7	$none$
C_{ox}	1.57n	F
C_{gs}	14.5n	F
W_B	55e-04	cm
N_B	3.15e14	cm^{-3}
τ_B	2.3e-07	s
I_{sE0}	1.29e-13	A
I_{sC}	1.57e-13	A
C_{jE}	425p	F
C_{jC}	425p	F
BV_{ce0}	700	V
R_g	0.1	Ω
R_s	11.5m	Ω

Table 4.3: New PSpice model parameters for DUT IRG4PC30S.

4.2.2 Model definition: experimental results

For simulation of designed converter in PSpice OrCad environment, the new proposed optimized Kraus NPT electro-thermal model presented in chapter 3 is considered for the device under test, that is the IGBT IRG4PC30S. By means the calibration procedure discussed in Appendix B, the set of model parameters which provide minimum error between experimental and simulated device characteristics is evaluated and reported in table 4.3.

The experimental acquisition of IGBT characteristics at room temperature which serves as reference for curve-fitting method within the parameters calibration algorithm is performed with tester equipment presented in chapter 3: in fig. 4.9 experimental data are compared with simulated device characteristics obtained at the end of calibration procedure. The improvements in accuracy attributable to the new model, are definitely clear especially from DUT DC output characteristics in fig. 4.9a, where the capability of new model to better reproduce the activation of PNP base-collector junction and its built-in voltage is shown, and from current-voltage waveforms during turn-off on inductive load (fig. 4.9d).

Therefore, the usefulness and effectiveness of new PSpice model to well describe the electrical behaviour of DUT IRG4PC30S are even more evident in

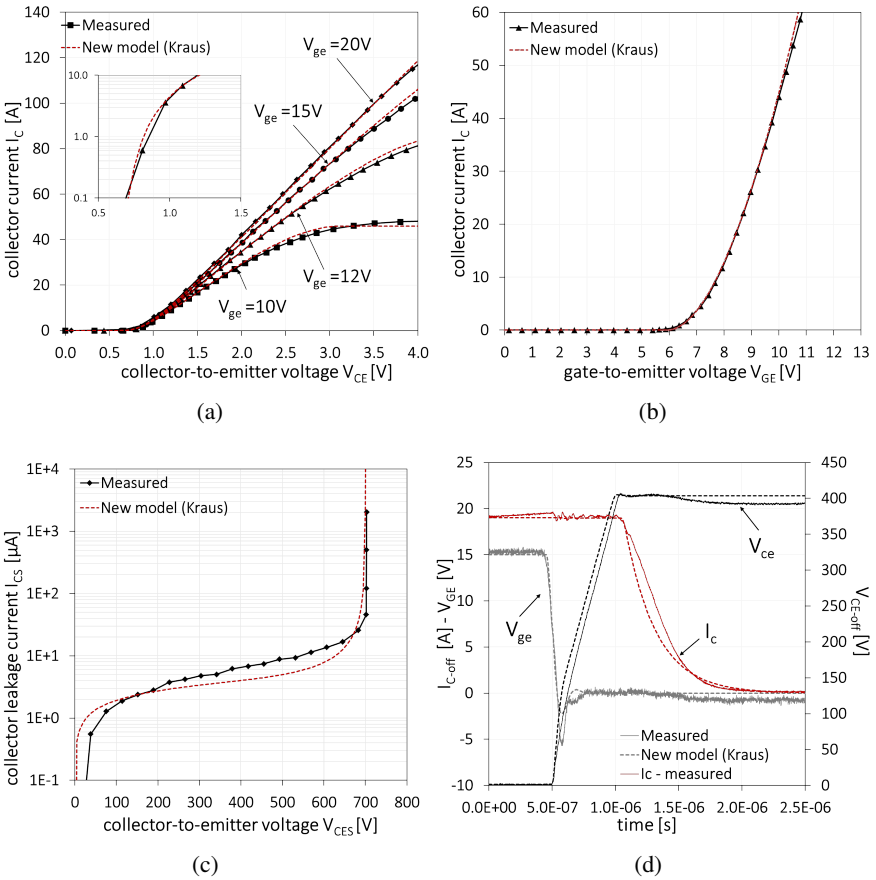
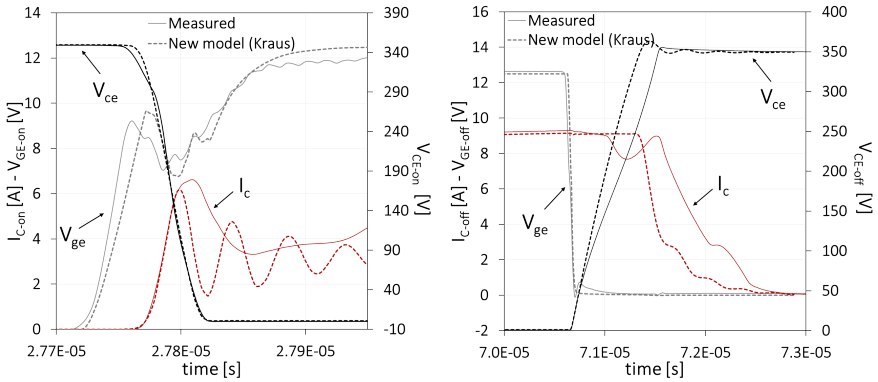


Figure 4.9: Experimental static and dynamic IGBT characteristics at T_j=27 °C for device IRG4PC30S, used as reference for calibration procedure: comparison with PSpice simulated results obtained using the new proposed Kraus-based model.

DC-DC buck converter simulations: in fig. 4.10a-b voltages (V_{ge} and V_{ce}) and current (I_c) waveforms during respectively turn-on and turn-off IGBT transitions at steady-state thermal conditions, that is T_j=35 °C, are shown. In particular, during converter steady-state operation, the IGBT must always handle the input voltage V_{in} in case of both transitions, while it must switch-on the minimum inductor current and switch-off the maximum inductor current, both defined by design. Anyway, simulated curves (continuous line), obtained with new model of DUT, fairly approach the experimental data, except for some differences due to limitation of model itself (discussed in chapter 3) and diode model too: in fact, IGBT turn-on collector current is largely influenced by freewheeling diode reverse-recovery behaviour, and the PSpice embedded model used for diode, doesn't well reproduce the actual long recovery time and softness of device (fig. 4.10a).



(a) Turn-on. (b) Turn-off.

Figure 4.10: IGBT transient voltages and current waveforms at steady-state T_{j0}=35 °C, during converter DC operating conditions.

4.2.3 Prediction of device losses

As a result of accordance on IGBT voltages and current waveforms during buck converter steady-state operation, a good agreement is achieved also on predicting IGBT losses compared to measured values: in table 4.4 the values of experimental and simulated IGBT conduction and switching power losses are reported in case of converter switching frequency f_{sw} equal to 10kHz, that

	P_{cond} [W]	P_{t-on} [W]	P_{t-off} [W]
Measured	10.5	0.238	26.6
New PSpice model	9.1	0.214	25.1
Error [%]	13.3	10.1	5.63

Table 4.4: Buck-converter: IGBT conduction and switching losses at f_{sw}=10kHz.

is a design specific. In particular, IGBT switching energy losses are estimated according to the following expressions, both in experimental and simulation case:

$$E_{t_{off}} = \int_{t}^{t+t_{off}} P_{IGBT}(t, T_j(t)) \ dt \tag{4.4}$$

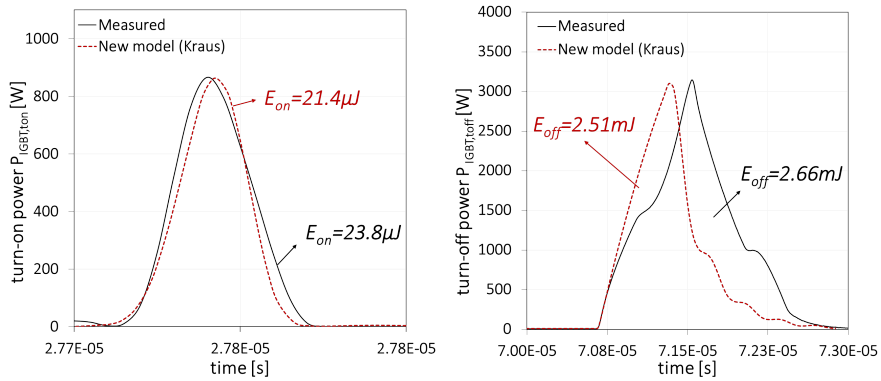
$$E_{t_{on}} = \int_{t}^{t+t_{on}} P_{IGBT}(t, T_j(t)) \ dt \tag{4.5}$$

where t_{on} and t_{off} are the time intervals respectively of turn-on and turn-off transient, defined by the standard *JEDEC*[2], regulation JESD24 1 Oct 1989. The relative percentage error between experimental and simulation data is nearby the 10%, that is a very small value, also considering the error affecting the measurement setup. Moreover, the DUT IGBT represents only a "typical" sample selected within a wide population of devices belonging to the same batch of production: therefore, their electrical performances, such as on-state voltage drop or turn-off switching losses, intrinsically follow a statistical Gaussian profile, whose standard deviation may be even larger than 10% of average value.

In fig. 4.11 the IGBT instantaneous power for turn-on and turn-off transitions during converter DC operation and steady-state IGBT thermal conditions with T_{j0}=35 °C: the device energy losses per-cycle is approximately the area under the curve and it's multiplied by the switching frequency in order to obtained the IGBT turn-off and turn-on dissipated powers. While the simulated waveform of instantaneous IGBT power during turn-on transient is very close to the measured one, the turn-off power behaviour in experimental case is influenced by the change in collector-to-emitter V_{ce} slope during its rise that causes

[2]JEDEC Solid State Technology Division, formerly known as *Joint Electron Device Engineering Council (JEDEC)*, is an independent semiconductor engineering trade organization and standardization body.

a delay on the power peak value respect to simulation result: nevertheless, as proved in table 4.4, the value of simulated turn-off switching energy losses is very close to measured one as well.



(a) Turn-on. (b) Turn-off

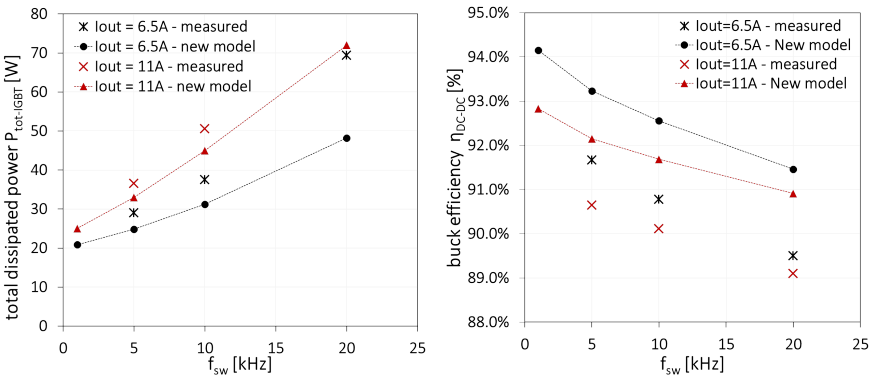
Figure 4.11: IGBT switching dissipated power at DC buck converter operation mode and steady-state temperature value T_j0=35 °C.

Once the effectiveness of new PSpice model for IRG4PC30S device has been validated at buck converter rated operating conditions of f_{sw}=10kHz and I_{out}=6.5A, circuit conditions are changed in order to verify the capability of model to predict IGBT total dissipated power and converter overall efficiency η even at different values of switching frequency and output load current. The converter efficiency is evaluated according to the following expression:

$$\eta_{DC-DC} = \frac{P_{buck,out}}{P_{buck,in}} \tag{4.6}$$

where $P_{buck,out}$ and $P_{buck,in}$ are respectively the power measured at input and output terminals of DC-DC converter.

With reference to design characteristics of buck converter and in particular to the value of filter inductor L, the variation of switching frequency and output current is such that the converter *Continous Current Mode* condition is always satisfied. As expected, IGBT total dissipated power increases with both switching frequency and load current: the error between measured and simulated data becomes larger at higher f_{sw} since the error on turn-off IGBT switching losses becomes more critical. Nevertheless, the overall behaviour of



(a) (b)

Figure 4.12: Measured and simulated a) IGBT total power losses and b) DC-DC buck converter efficiency evaluated in steady-state condition for two values of output load current I_{out} versus switching frequency f_{sw}.

measured IGBT power losses is faithfully reproduced by new model, and the relative difference between parametric curves at different output current value is achieved also in simulation. As concerns the DC-DC converter efficiency η, it's clear in fig. 4.12b that in laboratory circuit implementation there are some sources responsible for power loss not properly modelled or even considered in simulation, such as reverse-recovery of freewheeling diode or inductor iron losses: moreover, the measurement of converter output power $P_{buck,out}$ is performed connecting the power meter across the output capacitance, so, although an average value of 50 measures (acquired every 5 seconds) is considered, the ripples on inductor current and output voltage may still cause an small error. Anyway, the experimental curves of converter efficiency versus switching frequency at two values of output current (I_{out}=6.5A-11A), which tend to approach each other at increasing switching frequency, is well reproduced in simulation, and this further confirms the goodness of new model in predicting real device behaviour in DC-DC converter application too.

4.3 Optimum design of SC protection circuits

The third case-study taken as example for demonstration of new ET PSpice model effectiveness within an IGBT application situation, concerns the optimization of SC protection circuits design, needed in power converters to both detect a short-circuit event and prevent the destruction of device. Nowadays, in fact, a careful choice and design of IGBT SC protection circuits have become crucial [71]-[72] also because in some application device may experience several non-destructive SC events [73], and the abrupt increase of junction temperature may significantly reduce its life expectancy according to the theorized models for power semiconductor devices lifetime [74]. Unfortunately, design of protection circuit parameters is actually performed according to datasheet and application notes, which provide only a general approach and rough design rules, ignoring device technological specificity and SC electro-thermal (ET) effects: therefore, the optimum design cannot be pursued. So an accurate ET simulation of IGBT under SC condition [75] would be very effective for protection circuits design, aimed to the increase of IGBT lifetime and reliability. With reference to a three-phase DC-AC inverter, that is one of the most widespread converter application of IGBT devices, there are basically two cases when short circuits can happen, which are also shown in fig. 4.13:

- *short on the load*: short circuit occurs at the output phases, where the fault current's di/dt depends on the exact location of the fault as the inductance along current path changes;
- *short on a leg (shoot-through)*: one of the inverter legs is short circuited and due to a very small total inductance in the fault current path, the IGBT typically remains continuously in the active region, and the steady-state short-circuit current depends strongly on the applied gate–emitter voltage.

It is also possible to categorize the short circuits based on the timing:

- **HSF** (Hard-Switching-Fault),
- **FUL** (Fault-Under-Load).

In the *HSF* the load is short-circuited before the IGBT is turned on: in this kind of SC the fault current increases maximally the same rate as in a normal turn-on event. Testing the HSF is quite straightforward, and usually manufacturers give the IGBT short circuit withstand data for this type of fault, that is the

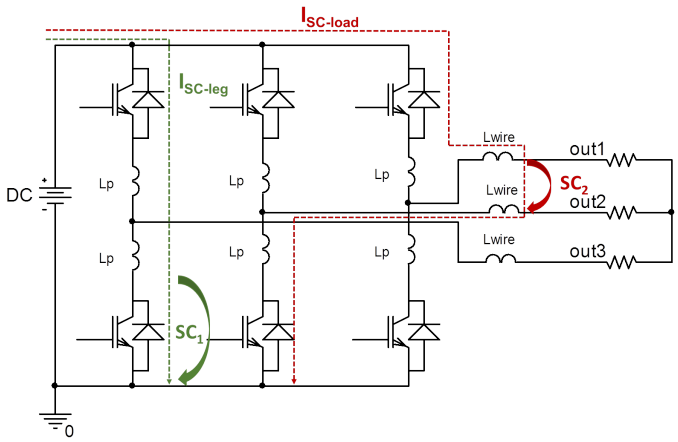


Figure 4.13: Two main typologies of short-circuit event occurring in an inverter: short of the load (SC_2) and shoot-through of the leg (SC_1).

case analysed in section 1. On the other hand, the *FUL* short circuit happens when IGBT is already conducting. In the FUL the IGBT is already saturated when the fault occurs. Therefore di/dt is determined only by the total inductance in the current path and the DC-link voltage. As the current increases, the IGBT moves into the active region which may cause a significant gate voltage rise if the transition is fast. This behaviour is due to the current feedback through the Miller-capacitance and typically the FUL results in a larger peak current than the HSF. There are many techniques used by circuit designers for IGBT short-circuit detection and protection, as discussed in [76]: in this analysis the well-known *desaturation* method is considered, which consists on the sense of device saturation collector-to-emitter $V_{ce,sat}$ voltage. During normal conduction mode in converter applications, IGBT operates in linear region, so its collector-to-emitter voltage is small, equal to on-state voltage drop (2-3V): if a short-circuit events occurs, its collector current I_c abruptly arises till saturation region, where the V_{ce} voltage becomes larger. When the value of V_{ce} exceeds a defined threshold value, the digital control detects a "fault condition" and forces the "soft" turn-off of the IGBT.

The sense circuit is depicted in fig. 4.14 and the logic circuits needed to achieve device protection are all integrated within the IGBT gate-driver. A typical timing diagram of main signals involved into desaturation circuit activation is depicted in fig. 4.15: during IGBT normal operation, the *desat*

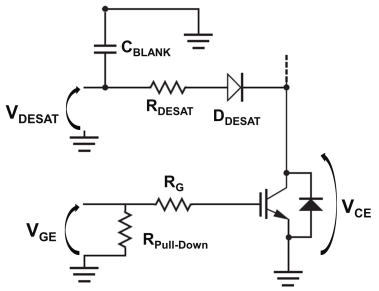


Figure 4.14: Simplified schematic of desaturation circuit V_{ce} detection by means V_{desat} voltage.

circuit voltage V_{desat} follows the behaviour of the sensed collector-to-emitter V_{ce} voltage in on-state, while it's equal to zero when IGBT is in off-state.

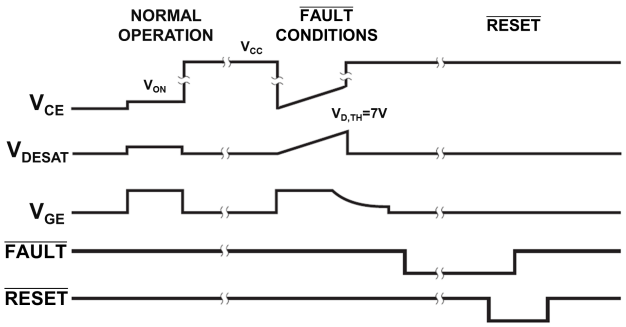


Figure 4.15: Timing diagram for main signals of desaturation protection circuit.

In case of a SC event, the V_{ce} starts to increase causing the V_{desat} to exceed the threshold value (e.g., 7V): the protection circuit $\overline{FAULT}$ signal is brought low until a reset input is activated by a micro to return to normal mode. Without go into details of desat circuit operation, an important aspect for IGBT application circuit designers must be highlight: the choice of a commercial gate-driver circuit with embedded desaturation protection and the design of some external desaturation circuit parameters such as $V_{ce,th}$ (related to $V_{desat,th}$ and to desat diode forward voltage drop), C_{blank} or $R_{pull-down}$ must be properly done according to IGBT characteristics in order to prevent device from critical SC electro-thermal conditions which may affect its reliability and lifetime.

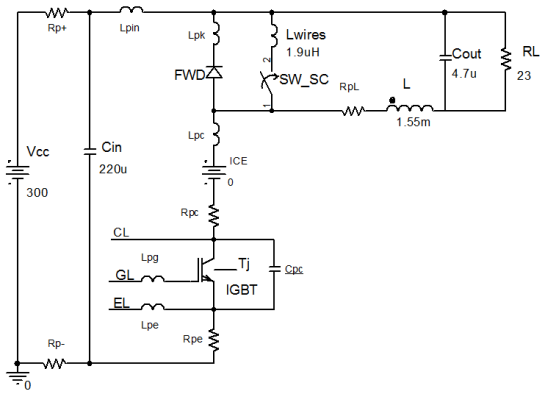
4.3.1 Case-study: test setup

Since experimental characterization of IGBT SC in application is very tricky to deal with, the effectiveness of the new PSpice model to reproduce IGBT electro-thermal behaviour under application converters short-circuit conditions is demonstrated by referring to a simplified case: in fact, an equivalent situation similar to a short occurring at the output phases of a DC-AC inverter (SC_1 case in fig. 4.13) is experimentally obtained by considering the step-down converter presented in previous section, where a short is forced on the load and a SC event occurs on the conducting IGBT, which acts as the second leg low-side IGBT within the inverter shown in fig. 4.13. Hence, the protection of IGBT from destruction is guaranteed by means a commercial gate-driver with integrated logic circuits for desaturation and IGBT "soft turn-off": the driver is the HCPL-316J and it's provided by Avago Technologies. The laboratory test equipment is almost the same as the one described in section 2: the power meters are not used in this test, while a fast electronic relay is used to induce the short across converter output terminals. In particular, the relay has an higher parasitic inductance, L_s=1.9μH, which can be assumed as the total wire inductance of the wiring harness to an AC motor in a real situation. An equivalent-schematic of step-down converter implemented for simulation in PSpice OrCad environment is depicted in fig. 4.16a: as previously said, the model of switch for load short-circuit induction is made of an ideal switch plus a parasitic inductance L_{wires}.

The DUT IGBT used for this test is the Infineon IGP30N60H3, of which the manufacturer provides the Foster equivalent thermal network (fig. 4.16b) for junction-to-package thermal description. Moreover, the model of gate-driver HCPL-316J, is also free available on the manufacturer website: the gate-driver configuration for single IGBT application is recommended on datasheet and it's considered both in laboratory circuit implementation and in PSpice equivalent case (fig. 4.16c). As concerns the design of desaturation circuit parameters, on the gate-driver datasheet a recommended value for some parameters is given:

- R_{desat}=100 Ω, added to avoid large amount of current drawing out of driver due to large negative voltage spikes during IGBT anti-parallel diode transient;

- $R_{pull-down}$=100 Ω, is much larger than R_g, and it's used to turn-off the IGBT in case of driver circuit fault.



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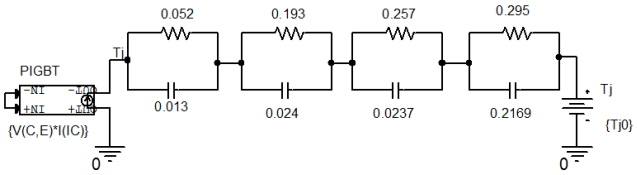
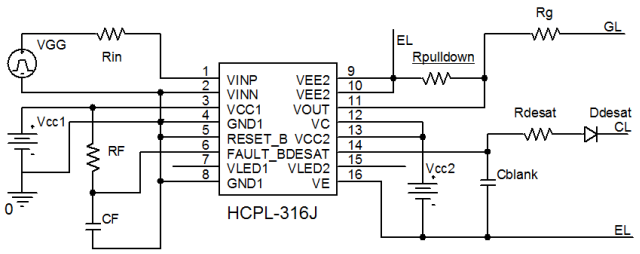




(c)

Figure 4.16: a) Equivalent PSpice OrCad schematic of buck-converter with switch for SC, b) DUT Foster equivalent thermal network and c) HCPL-316J gate-driver model.

On the contrary, some other parameters are designed using approximated expressions provided in gate-driver application notes: the collector-to-emitter voltage threshold $V_{ce,th}$, depends on desat threshold that is usually 7V and on the desat diode D_{desat} forward voltage drop, so it's:

$$V_{ce,th} = 7V - V_f, \tag{4.7}$$

and can be reduced by using a series of diodes with voltage drop equal to V_f. Furthermore, the blanking capacitor C_{blank} is evaluated according to the expression:

$$C_{blank} = \frac{I_{ch} * t_{blank}}{V_{desat}}, \tag{4.8}$$

where I_{ch} is the internal desat charge current (typical value 250μA), V_{desat}=7V and t_{blank} is the blanking time, which must be properly chosen in order to avoid false activation of protection circuit during IGBT turn-on transient. In this case the value of blanking time recommended on gate-driver application note is 2.6μ with a blanking capacitance of C_{blank}=100μF. Anyway, this evaluation do not consider the electro-thermal behaviour of the particular IGBT, which may experiences large ΔT_j during short-circuit time interval, which strongly depends on blanking time. Thus, experimental measurements on buck converter at design operating conditions, have been performed in steady-state converter mode: moreover, since the equivalent thermal network provided by IGBT manufacturer regards the junction-to-case description, the no heatsink is considered for DUT power dissipation and measurements are performed when IGBT reaches the steady-state thermal conditions, at a temperature equal to T_{j0}=55 °C: the device junction temperature is properly monitored by means a thermocouple mounted inside the package, through an hole.

4.3.2 Simulation results

The experimental case-study used for circuit validation is obtained by inducing a short on the load by means the electronic relay: the typology of short is HSF, because IGBT experienced the short-circuit event at turn-on transient. In fig. 4.17 the IGBT experimental V_{ce}, V_{ge} and I_c waveforms during short-circuit device event, after the short occurred on the load, are compared with simulated ones: the good model of gate-driver with embedded desaturation protection assures to reproduce in simulation the sensing of SC desat threshold voltage

and the soft turn-off of IGBT, also thanks to the accuracy of the new ET PSpice model.

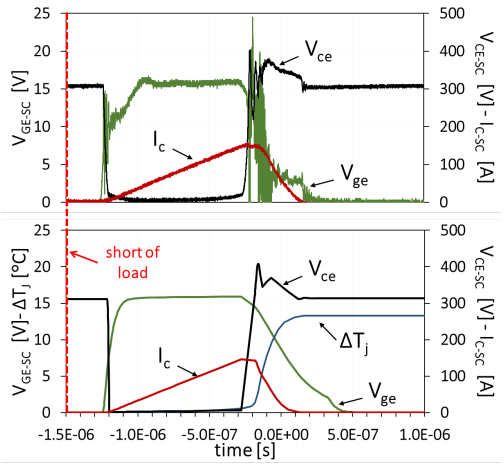


Figure 4.17: Experimental and simulated HSF SC on DUT IGBT, after a short occurred on the load.

The electro-thermal behaviour of IGBT voltages and currents waveforms is also well reproduced, although there are some mismatches with experimental curves mainly due to circuit parasitics and device internal non-linear capacitances, which are not modelled. Nevertheless, being the trend of simulated IGBT voltage and current waveforms very close to experimental curves, the accurate estimation of device transient power dissipation by the model is very important for IGBT maximum junction temperature evaluation during the short-circuit time interval. In this case the simulated IGBT junction temperature reaches a maximum of 65°C (starting from steady-state temperature T_{j0} that is 55°C) during short-circuit event, before protection intervenes. The abrupt increase of IGBT junction temperature due to short-circuit high power dissipation may be even much larger when a shoot-through of the leg occurs in the converter: in fact, since path inductance is significantly lower ($L_{wires} \simeq 100nH$), the high dI/dt may result in delay on protection circuit response, causing a higher device power dissipation and ΔT_j during short-circuit time interval: for instance, in fig. 4.18a-b, simulation of HSF short-circuit due to shoot-though of the leg (L_{wires}=100nH) with C_{blank}=100p is considered. The simulated IGBT current and voltages waveforms during SC event are depicted in fig. 4.18a: the high value of blanking capacitance causes

the protection circuit desat voltage V_{desat} to rise slowly, resulting in high power dissipation and significant increase of device junction temperature (fig. 4.18b).

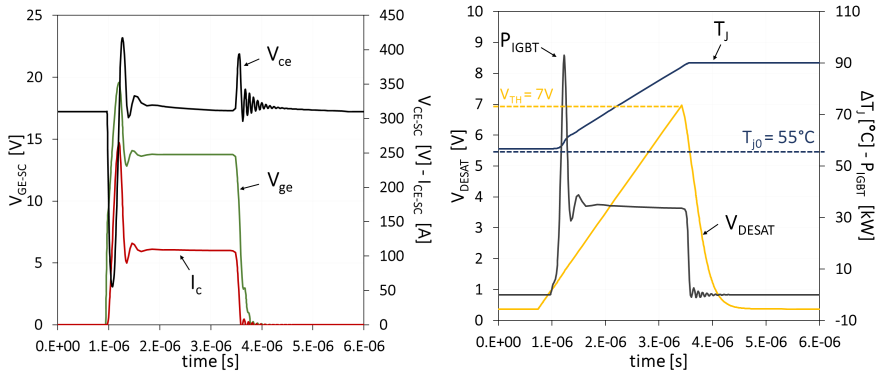


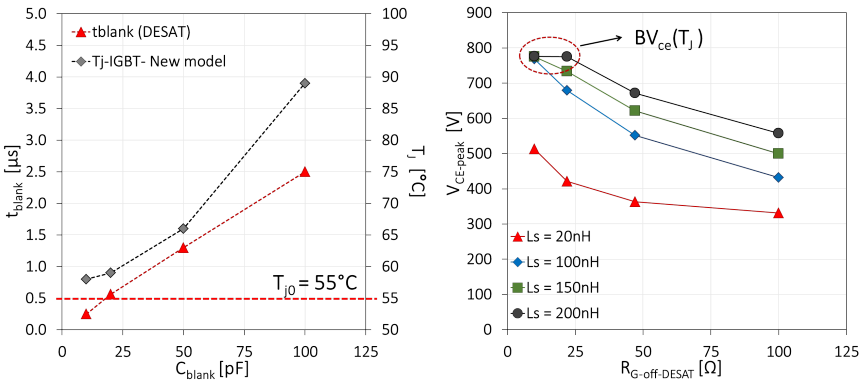
Figure 4.18: Simulation of HSF SC due to shoot-through of the leg (L_{wires}=100nH): behaviour of IGBT a) short-circuit voltages and current waveforms and of b) V_{desat} voltage, IGBT short-circuit dissipated power P_{IGBT} and device junction temperature T_j.

Hence, the circuit designer has to pursue the optimum value for C_{blank}, by avoiding desat circuit false activations in normal operation and also limiting the maximum junction temperature device may reach after a short-circuit event. An ET PSpice model is very useful for this kind of analysis: in fact, in fig. 4.19a, the increase of simulated IGBT short-circuit ΔT_j with C_{blank} is reported in case of HSF SC due to shoot-through of a leg: maximum temperature value of $T_j \simeq 90°C$ obtained with C_{blank}=100pF may be not acceptable by circuit designers.

Whereby, this larger variation of junction temperature during IGBT transient operation may affect its reliability and lifetime expectancy: in fact, the maximum number of thermal cycles a power device can experience during its lifetime is approximately evaluated according to Coffin-Manson model [77], in which the simple formula is given:

$$N_f = a(\Delta T_j)^{-n} e^{E_a/(kT_{j0})}, \tag{4.9}$$

where T_{j0} is the operating device medium temperature and ΔT_j the transient temperature variation during each cycle. Another critical aspect in SC



(a) (b)

Figure 4.19: Electro-thermal simulations of IGBT HSF short-circuit due to shoot-through of the leg (L_{wires}=100nH): a) behaviour of blanking time and device junction temperature with design C_{blank} value and b) behaviour of peak IGBT collector-to-emitter voltage V_{ce} with turn-off protection gate resistance $R_{g,off}$ at different collector stray inductance values.

protection circuits design concerns the wise choice of $R_{g,off}$ when driver circuit doesn't provide an embedded "soft" control of the gate voltage turn-off, as happens in case of HCPL-316J gate-driver. In fact, the R_{g-off} value must be accurately selected in order to limit the collector-to-emitter overvoltages due to stray inductance when turning-off high short-circuit current according to device speed characteristics (tail current and lifetime): with the help of the fast and slightly accurate IGBT ET model we can predict and plot the behaviour of collect-to-emitter peak voltage $V_{ce,peak}$ versus $R_{g-off,DESAT}$ for different values of stray inductance, when a shoot-through occurs to a single leg of an inverter and the desaturation protection circuit is activated to turn-off the IGBT experiencing the short-circuit event(fig. 4.19b): for high values of collector-side stray inductance L_s and small values of $R_{g-off,DESAT}$, for example equal to device normal operation gate-resistance (10Ω), the IGBT may operates at high V_{ce} voltage values, which are far beyond the SOA (*Safe Operating Area*) declared by manufacturer. Although the new improved ET model allows to accurately simulate the behaviour of IGBT steady-state breakdown voltage with temperature, during IGBT turn-off transient more complex electro-thermal physical effects occur, such as "dynamic avalanche" phenomena, in which device breakdown voltage is strongly dependent on collector current. These electro-thermal effects cannot be reproduced by means a compact model, and the use of TCAD models becomes essential.

Chapter 5

Extension of Kraus model to FS devices

As previously discussed, although the enhancements and optimizations brought to Kraus model PSpice implementation which make it more attractive for SPICE simulators users respect to other models, it has not yet been fully investigated and proper adjustments are to be pursued in order to improve its accuracy and to optimize its implementation in SPICE simulators. In this chapter an approximated formulation, evaluated under certain hypothesis, of n^+ Field-Stop layer (FSL) equations are added into Kraus IGBT model to take into account the physical and electrical effects characterizing the modern Field-Stop IGBT technology.

5.1 Field-stop devices modeling

The Kraus PSpice model version so far discussed is based on the IGBT Non-Punch-Through structure so it's properly suitable for modeling NPT devices, where there is no n^+ buffer-layer, and low-doped n^- base region is thick enough to avoid electrical field Punch-Through. Although the trade-off between accuracy of results and model speed, convergence and simplicity may be very satisfying, the need of a proper modeling according to device structural and physical characteristics, becomes necessary, especially for modern Field-Stop IGBT structures. In fact, due to increasingly performances of FS IGBTs which usually operate under circuit hard conditions within modern converters, the effects of buffer-layer (or Field-Stop layer due to different technological characteristic) must necessarily be covered in a compact model too.

5.1.1 FS IGBT advantages

In the last years of the twentieth century both IGBT concepts of PT (Punch-Through) and NPT (Non-Punch-Through) seemed to have been improved vertically to their optimum by mainly some innovations:

- enhancement of the buffer structure and the lifetime killing process on the PT side;
- reduction of wafer thickness on the NPT side.

Nevertheless, some structural drawbacks for both PT and NPT IGBT still remained: in particular, the PT IGBT has an unnecessary high carrier concentration at the back resulting in undesired high turn-off current tail and losses or extremely high lifetime doping leading to a rather high on-state voltage drop. In contrast, the NPT IGBT has the desired low carrier concentration at the back, but the n^- base has to be rather thick due to its triangular electrical field in case of blocking condition: this rather thick n^- base results in higher static and dynamic losses. Obvious is an improvement of the NPT structure to a device with a trapezoidal field distribution under blocking condition as it is typical for the PT IGBT. But the inherent advantages of the NPT concept concerning the low efficient emitter and the high carrier lifetime should not be given up. This is possible in FS devices by implementing a *field-stop layer* (FSL) with a very low dose not influencing the p^+ emitter dose typical of the NPT IGBT but high enough to stop electrical field under blocking conditions: this allows to shrink the thickness of the NPT structure by 1/3, and the doping of field-stop layer is maintained quite low, totally different from typical buffer layer doping of PT devices [78]. The task of FSL is not only to stop the electrical field but also to reduce the enormous p^+ emitter efficiency in PT IGBTs. The technological differences among the three main IGBT structures are reported in table 5.1:

These principles results in drastically improvements of the FS IGBT electrical performances since it's characterized by both reduced of dynamic losses and lower on-state voltage drop than the NPT and also lower turn-off losses than the PT IGBT. Hence, the enhancements brought by Field-Stop IGBT technology must be properly taken into account by compact models too.

5.1.2 Modeling the FSL

In literature a lot of approaches for buffer-layer modeling in IGBT PT structures have been proposed ([38]-[39]-[79]-[45]-[80]-[81]): almost all models

	PT-IGBT	NPT-IGBT	FS-IGBT
p^+ *emitter*	very high efficiency	low efficiency	low efficiency
$n^- base$	thin	medium	thin
additional n layer	buffer layer =high doped -to reduce the very high emitter efficiency -to stop the electrical field	no	field-stop layer =weakly doped -to stop only the electrical field
carrier lifetime	low low (lifetime killing)	high	high

Table 5.1: Comparison of FS concepts with NPT and PT ones.

are based on the solution of ADE in the n^+ buffer-layer, typical of PT IGBT, under certain hypothesis, which are always valid for its characteristics at all normal device operation conditions. The most interesting and simple proposal, that is, instead, specific for Field-Stop IGBTs, is given in [40], in which model is constructed starting from previously theorized NPT and PT models. With reference to fig. 5.1, the addition of the field-stop layer creates two different junctions respect to the NPT structure discussed in chapter 2: the junction J_0 between the p^+ emitter and n doped FSL, and junction J_1 between the FSL and the n^- doped drift region.

In steady-state conditions, the small electron current I_{nE} at junction J_0 is due to electrons reverse injection into the p^+ emitter, which travel through the FSL coming from the drift region. Hole current injected from the p^+ emitter travels mostly by diffusion and, since the FSL is typically fairly thin in comparison to its diffusion length L_{pH}, only little recombination occurs in the FSL and most of the hole current reaches the drift region. This current, called I_{pB} in fig. 5.1, represents hole injection from the FSL into the drift region. The component of hole current lost to recombination is compensated by an increase in the electron current, so that the electron current I_{nb} at junction J_1 is the sum of two terms: the recombination component plus the reverse injection electron current . On the other hand, under dynamic conditions, the additional hole current component due to variations in the stored charge in the FSL must be considered. Therefore, the current continuity equations are always valid at every device operating conditions:

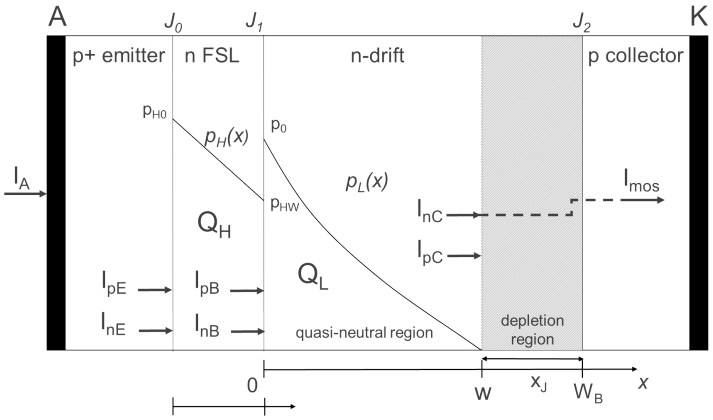


Figure 5.1: Structure of FS IGBT: steady-state base charge carriers distribution.

$$\begin{cases} I_{nC} = I_{nB} + I_{QL} = I_{nE} + I_{QH} + I_{QL}, \\ I_{pC} = I_{pB} - I_{QL} = I_{pE} - I_{QH} - I_{QL}, \\ I_{pE} + I_{nE} = I_{pB} + I_{nB} = I_{pC} + I_{nC} = I_A, \end{cases} \tag{5.1}$$

where electron and hole current components are defined in fig. 5.1 at each junction and I_{QL} and I_{QH} are the diffusion current respectively in n^- drift region and in n FSL [1]. While n^- drift region is always under high-level injection conditions and ambipolar diffusion equation is solved to find the holes density $p_L(x)$ profile, the hypothesis for FSL are:

i) low-level injection in FSL;

ii) FSL thickness $W_H \cong L_{pH}$;

iii) only diffusion component for holes (minority carriers) current;

iv) quasi-static (QS) approximation for FSL carriers charge;

Note that the FSL modeling is based on quasi-static approach, means that the steady-state carriers distribution is assumed for all conditions. Assuming

[1] In the FS structure, parameters of FSL are referred to with subscript *H* (high-doped), while subscript *L* is related to drift region parameters (low-doped): model parameters for drift region are still indicated with subscript *B* used in case of NPT structure.

that FS layer is always under low-level injection, the steady-state excess hole profile $p_H(x^*)$ is:

$$p_H(x^*) = \frac{p_{H0}\sinh\left(\frac{W_H - x^*}{L_{pH}}\right) + p_{HW}\sinh\left(\frac{x^*}{L_{pH}}\right)}{\sinh\left(\frac{W_H}{L_{pH}}\right)}, \tag{5.2}$$

with p_{H0} and p_{HW} the hole densities respectively at p^+ emitter and n^- drift edges of FSL. Due to hypothesis ii), holes profile $p_H(x^*)$ is approximately linear, as shown in fig. 5.1. So it can be simplified and written as:

$$p_H(x^*) = \frac{p_{HW} - p_{H0}}{W_H}x^* + p_{H0}. \tag{5.3}$$

The reverse electron current I_{nE} at junction J_0 can be expressed in terms of hole concentration p_{H0}, if quasi-equilibrium conditions are satisfied, using the well-known junction's law:

$$I_{nE} = I_{sE}\frac{p_{H0}N_H}{n_i^2}, \tag{5.4}$$

where I_{sE} is the emitter electron saturation current (as in NPT structure). For the hypothesis iii) the hole current at emitter edge of FSL is:

$$I_{pE} = -qAD_{pH}\frac{dp}{dx}|_{x^*=0} = qAD_{pH}\frac{(p_{H0} - p_{HW})}{W_H} \tag{5.5}$$

The FSL diffusion current I_{QH} is defined as function of carriers charge Q_H in the FSL, through the current continuity equation:

$$I_{QH} = \frac{Q_H}{\tau_H} + \frac{dQ_H}{dt}, \tag{5.6}$$

which includes a recombination term related to hole carriers lifetime in FSL τ_H and a transient capacitive current due to variations in the charge Q_H stored in FSL. By considering the linear profile of $p_H(x^*)$ in 5.3, carrier charge in FSL is approximated as:

$$Q_H = \frac{qAW_H\,(p_{H0} + p_{HW})}{2}. \tag{5.7}$$

Due to QS approximation (hypothesis iv)) assumed for FSL carriers charge, the expression used for Q_H is always the same in both static and

dynamic case: the dynamic contribution to FSL diffusion current is considered via the $\frac{dQ_H}{dt}$ in equation 5.6. Finally the hole concentration p_{HW} at the boundary between the FSL and the drift region is given by:

$$p_{HW} = \frac{p_{L0}^2}{N_H}, \tag{5.8}$$

since quasi-equilibrium is assumed in both FSL and drift region.
Accordingly, as result of addition of FSL, the solution $p_L(x)$ of steady-state ambipolar diffusion equation 2.8, must be evaluated by considering the new boundary conditions:

$$\begin{cases} p_L(0) = p_{L0}; \\ p_L(w) = 0. \end{cases} \tag{5.9}$$

Since p_{L0} is a function of the FSL parameters through the FSL equations previously reported [2], the steady-state carriers charge Q_{L0} of n^- drift region is influenced by FSL characteristics too, and it must be taking into account for addition of FSL equations within the Kraus-based PSpice model.

5.2 PSpice implementation

In order to synthesize the FSL equations within the PSpice Kraus-based IGBT electro-thermal model previously discussed, some adjustments need to be carried out: the Kraus NPT model implementation discussed in chapter 2 and chapter 3, is essentially based on the evaluation of an explicit expression of the carriers charge Q_{B0} in the drift region (2.22): similarly, an explicit formulation of carriers charge Q_{L0}, in case of FS IGBT model, must be evaluated from the equation:

$$I_{QL} = \frac{Q_{L0}}{\tau_B} + \frac{Q_{L0} - Q_L}{T_D} \tag{5.10}$$

where Q_L is the instantaneous carriers charge of n^- drift region and T_D is equal to 2.20. The analytical calculations performed in Appendix C, result in the following expression:

[2] In case of NPT IGBT structure, the carrier density p_0 at p^+ emitter edge of n^- base is an explicit function of J_1 reverse electron saturation current I_{sE}.

$$Q_{L0} = \frac{2(Q_{LD} - j_{sE}N_H p_T Q_{s0}^2 - T_D I_{QH})}{F_3 + \sqrt{F_3^2 + 4j_{sE}n_i^2(Q_{LD} - j_{sE}N_H p_T Q_{s0}^2 - T_D I_{QH})}} \tag{5.11}$$

One of the main differences affecting the FS IGBT structure is that there are two contributions to base region total carriers charge, which are Q_L and Q_H, respectively related to the n^- drift region and to the n field-stop-layer. As reported in chapter 2 for NPT PSpice model, the evaluation of instantaneous base carriers charge Q_B was made using a NQS (Non-Quasi-Static) approach and it's expressed in terms of the steady-state value Q_{B0} in the equation: therefore, the diffusion current continuity equation 2.12 was synthesized by means a charge sub-circuit. Similarly, in case of FS PSpice model, the n^- drift region carriers charge Q_L, that explicitly appears in 5.11, is defined by the sub-circuit depicted in fig. 5.2, which synthesizes the following current diffusion equation:

$$I_{QL} = I_{nC} - I_{nB} = \frac{Q_L}{\tau_B} + \frac{dQ_L}{dt} \tag{5.12}$$

where tau_B is the high-level injection lifetime in n^- drift region and I_{nB} the electron current at FSL edge of drift region, as defined in 5.1.

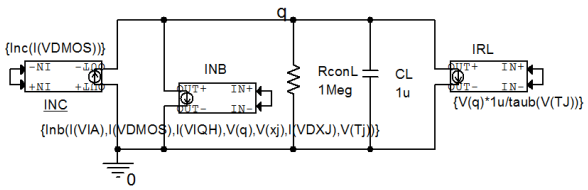


Figure 5.2: Equivalent sub-circuit for Q_L evaluation in FS PSpice model.

The equation 5.6 serves to describe the behaviour of FSL carriers charge Q_H according to a QS (Quasi-Static) approach, so it can be implemented in PSpice with a charge sub-circuit too: since in 5.11 a the FSL diffusion current I_{QH} is used for evaluation of Q_{L0}, the sub-circuit is quite different respect the one used for drift region. The PSpice equivalent schematic, that synthesized the 5.6 is shown in fig. 5.3: here, the voltage across *h* node and ground, is set equal to $Q_H/1\mu$, and the diffusion current I_{QH} is read as output with the zero voltage source generator *VIQH*. Note that the source current generator *IRL* depends on low-level injection lifetime τ_H in FSL, which is the lifetime of minority carriers (holes).

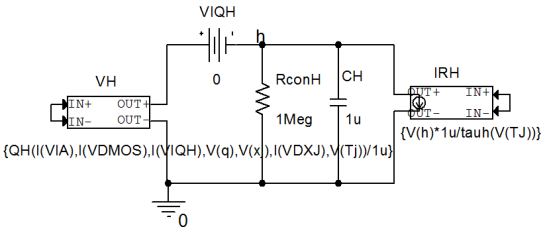


Figure 5.3: Equivalent sub-circuit for Q_H evaluation in FS PSpice model.

Furthermore, some PSpice analytical functions need to be modified in order to take into account the boundary conditions in n^- drift region due to addition of Field-Stop layer. For instance, the PNP collector-side holes current I_{pC} is defined as follows:

$$I_{pC} = \frac{1}{b} I_{nC} + \left(1 + \frac{1}{b}\right)\left(F_1 Q_{L0} + F_2\left(\frac{Q_{L0}}{\tau_B} - I_{QL}\right)\right) = \frac{1}{b} I_{nC} + \left(1 + \frac{1}{b}\right)\left(F_1 Q_{L0} + F_2\left(\frac{-Q_{L0} + Q_L}{T_D}\right)\right) \tag{5.13}$$

where the instantaneous carriers charge value Q_L depends on electron current I_{nB} at FSL side of n^- drift region, as shown in the sub-circuit 5.2 [3]. Of course, the electron current I_{nB} is evaluated from FSL diffusion current I_{QH}, according to the following current continuity equation:

$$I_{nB} = I_{nE} + I_{QH} \tag{5.14}$$

Moreover, the addition of Field-Stop layer results in a further contribution to overall IGBT on-state voltage drop, due to the resistance introduced by the high-doped n layer. Whereby, by assuming low-level injection conditions in FSL (no conductivity modulation occurs) for all device normal operations and considering that the junction J_1 is forward biased (depletion region is negligible respect to W_H), the resistance offered by the FSL is defined as follows:

$$R_H = \frac{1}{qA}\int_0^{W_H} \frac{dx^*}{\mu_{pH} p(x^*) + \mu_{nH} n(x^*)} \approx \frac{W_H^2}{\mu_{nH} Q_{NH} + \mu_{pH} Q_H}, \tag{5.15}$$

[3] In NPT Kraus model, Q_B is related directly to I_{nE}, since FSL is not present.

where $Q_{NH} = qAN_HW_H$ is the background mobile carriers FSL charge, defined in the same way of $Q_{NL} = qAN_BW_B$ for n^- drift region. Nevertheless, since the doping of FSL is some orders of magnitude larger than drift region doping for typical values of FSL thickness adopted in FS device technologies, this resistance is negligible respect to the conductivity modulated resistance R_L that characterizes the low-doped drift region. In fig. 5.4, the behaviour of both drift region and FSL resistances for different values of FSL thickness W_H and doping N_H is plotted for a steady-state operation condition at V_{ge}=15V, V_{ce}=5V and T_j=27 °C: the value of R_L is almost two orders of magnitude larger than R_H in every conditions considered, so it can be neglected within the PSpice model.

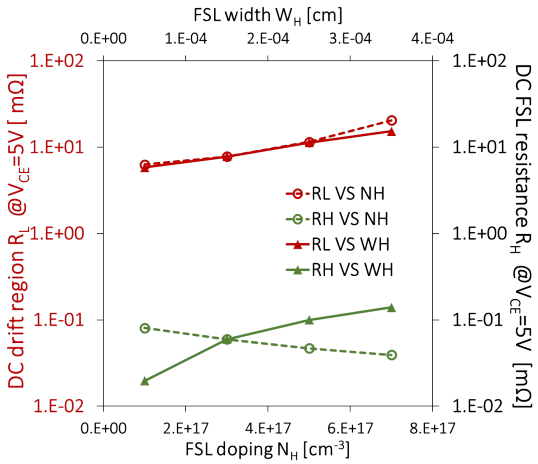


Figure 5.4: Comparison between behaviour of simulated steady-state R_L and R_H resistances with FSL thickness W_H and doping N_H at V_{ge}=15V, V_{ce}=5V.

5.2.1 Model of e-h mobility

One of the main model enhancement performed in parallel with addition of FSL equations, regards the introduction of a physical based model for the dependence of electron and holes mobility on the doping. In fact, since in the Kraus-based FS IGBT model there are three important doped regions, the emitter, the FSL and the drift region, which are considered for internal PNP bipolar transistor modeling, the effect of the different doping concentration on

Coefficient	**Electron mobility** μ_n	**Hole mobility** μ_p	**Unit**
μ_{min1}	52.2	44.9	cm^2/Vs
μ_{min2}	52.2	0	cm^2/Vs
μ_{const}	1417	470.5	cm^2/Vs
P_c	0	9.23e16	cm^{-3}
C_r	9.68e16	2.23e17	cm^{-3}
C_s	3.43e20	6.1e20	cm^{-3}
α	0.68	0.719	$none$
β	2	2	$none$

Table 5.2: Masetti's model coefficients for doping dependence of electron-hole mobility.

	Doping concentration cm^{-3}	**Electron mobility** μ_n cm^2/Vs	**Hole mobility** μ_p cm^2/Vs
N_B	1.5e14	1404	468
N_H	1.0e17	727	319
N_E	5.0e18	138	88

Table 5.3: Values of electron and hole mobility for FS device standard N_B,N_H and N_E doping concentration.

electron and hole mobilities must be properly taking into account. Hence, the well-established Masetti's model [82], which is also included in many TCAD simulators such as *Synopsys Sentaurus*, is effectively implemented in the proposed PSpice FS IGBT model. In particular, the equations used for electron and hole mobility μ_{dop} dependence on net doping concentration $N_A + N_D$:

$$\mu_{dop} = \mu_{min1} exp\left(\frac{-P_c}{N_A+N_D}\right) + \frac{\mu_{const}-\mu_{min2}}{1+\left(\frac{N_A+N_D}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1+\left(\frac{C_s}{N_A+N_D}\right)^{\beta}}, \tag{5.16}$$

where the coefficients μ_{min1}, P_c, μ_{const}, μ_{min2}, C_r, C_s, α and β are reported in table 5.2 for both electron and hole.

The values for electron mobility μ_n and hole mobility μ_p in case of typical IGBT emitter, FSL and drift region doping concentrations are reported in table 5.3.

Furthermore, in Kraus-based model the total reverse saturation current of

junction J_0 needs to be considered within the PSpice model of diode D_E, by means the parameter IS: in case of NPT IGBT model, this parameter is set to the value of model parameter electron reverse saturation current I_{sE0}, since p^+ emitter doping concentration is a few orders of magnitude larger than drift region one and the contribution of reverse hole saturation current I_{sH0} (at T_j=27 °C) can be neglected. On the contrary, in case of FS IGBT model, this contribution to the total reverse saturation current of junction J_0 can no longer be neglected, due to the fact that p^+ emitter and FSL doping concentration may be also very close, according to the particular technology. Whereby, the value of reverse hole saturation current, flowing from FSL to the p^+ emitter when J_0 is reverse biased, needs to be evaluated from the expression:

$$I_{sH} = \frac{qAn_i^2 D_{pH}}{L_{pH} N_H} \tag{5.17}$$

where N_H is the FSL doping concentration and D_{pH}-L_{pH} are respectively the hole diffusivity and holes diffusion length within the FSL n doped region. In order to properly estimate the temperature dependence of reverse electron saturation current I_{sE} given by 3.25, the value of electron diffusivity D_{nE} is needed within the p^+ emitter region, taking into account the small value of electron mobility μ_{nE}. Therefore, since the value of I_{sE0} at room temperature is provided as model parameter, the p^+ emitter doping concentration N_E is given into the model as a constant value to roughly estimate the μ_{nE0} and thus the diffusivity D_{nE0} using Masetti's model.

5.2.2 PSpice complete FS model

Hence, the so-defined electro-thermal Kraus-based model for Field-Stop IGBT devices is implemented in PSpice OrCad environment: the overall model schematic is depicted in fig. 5.5, where it's possible to appreciate the addition of sub-circuit for the evaluation of FSL diffusion current I_{QH} from the expression of FSL carriers charge Q_H. The list of model parameters reported at the side of the schematic includes, of course, parameters regarding the structural and technological characteristics of the Field-Stop layer, which are FSL doping concentration N_H, FSL thickness W_H and FSL low-level injection lifetime τ_H related to minority carriers (holes).

As concerns the implementation in SPICE of analytical equations which govern the physical behaviour of device, they are reported in tables 5.4-5.5-5.6: differently from NPT IGBT PSpice model, here the number of equations

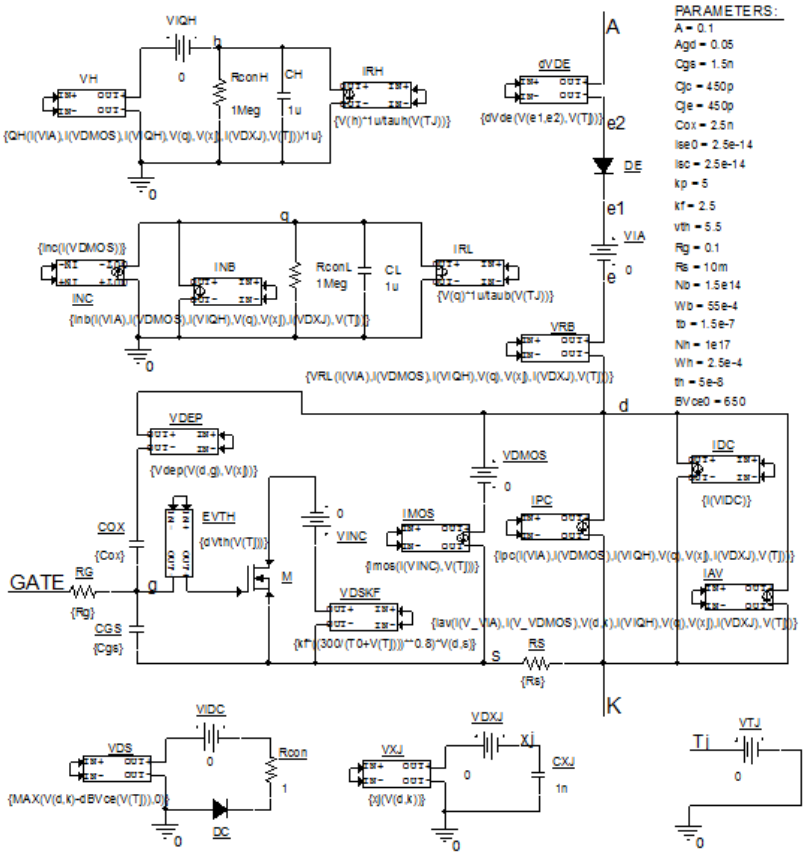


Figure 5.5: PSpice schematic of the Kraus IGBT FS electro-thermal model.

is increased since FSL equations need to be inserted within the model formulation. Moreover, the equations needed to evaluate the physical parameters for each of the considered doped region (n^- drift region, FSL region and p^+ emitter region) as function of doping concentration, are reported in table 5.7, where the Masetti's model is considered for definition of electron and hole mobility. Finally the definition of Mosfet and diodes D_E, D_C PSpice embedded models is shown in table 5.8: note that the reverse saturation current I_S of diode D_E is now set to $I_{sE0} + I_{sH0}$ in order to take into account the effect of hole injection into p^+ emitter region too when the junction J_0 is reverse biased.

Physical constants and silicon properties at $T_j = 300K$
.PARAM q=1.602e-19 eps0=8.85e-14 epsi=11.8 kB=1.38e-23 ni0=1.45e10
+ vnsat0=1.07e7 vpsat0=0.83e7
.PARAM T0=273
.PARAM VN={q*Nb*eps0*epsi*((Agd/Cox)**2)}
.PARAM QNL={q*A*Nb*Wb}
Physical parameter VS T_j
.FUNC taub(TJ) {tb*(((T0+TJ)/300)**1.5)}
.FUNC La(TJ) {SQRT(Da(TJ)*taub(TJ))}
.FUNC tauh(TJ) {th*(((T0+TJ)/300)**2)}
.FUNC Lph(TJ) {SQRT(Dph(TJ)*tauh(TJ))}
.FUNC ni(TJ) {1e-10*3.88e16*((T0+TJ)**1.5)/(exp(7000/(T0+TJ)))}
.FUNC vnsat(TJ) {vnsat0/(0.26+0.74*TJ/300)}
.FUNC vpsat(TJ) {vpsat0/(0.63+0.37*TJ/300)}
.FUNC Ise(TJ) {Ise0*Dne(TJ)*1e20*(ni(TJ)**2)/(Dne0*(ni0**2))}
.FUNC Ish(TJ) {Ish0*Dph(TJ)*1e20*(ni(TJ)**2)/(Dph0*(ni0**2))}

Table 5.4: PSpice Kraus-based IGBT ET model for FS devices: parameters and constants.

5.3 Qualitative FS model simulations

In order to estimate the speed and convergence properties of the electrothermal FS IGBT model implementation in PSpice and to verify its capability to properly reproduce main physical and electrical effects of a FS structure respect to a NPT one, some qualitative simulations of both device static and dynamic characteristics are performed in PSpice OrCad environment. For the purpose, a set of standard model parameters shown in table 5.9 are considered: in particular, the chosen values for n^- drift region and FSL region parameters are intended to be typical of a Field-Stop device structure.

5.3.1 Static and dynamic behaviour

The evaluation of Field-Stop layer equations aimed to PSpice FS IGBT modeling, have been evaluated under certain hypothesis: in particular high-level

Model analytical equations
.FUNC Imos(IVINC,TJ) {LIMIT(IVINC*((300/(TJ+T0))**1.5),0,1e6)}
.FUNC dVth(TJ) {(TJ-27)*5e-3}
.FUNC Inc(IMOS) {LIMIT(IMOS,0,1e6)}
.FUNC Ipc(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT((1/b(TJ))*Inc(IMOS)+
+ (1+1/b(TJ))*(QL0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)*F1(XJ,TJ)
+ +F2(XJ,IXJ,TJ)*(MAX(-QL0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)+
+ QL(VQ),0)/TD(XJ,IXJ,TJ))),-1e6 ,1e6)}
.FUNC Ine(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT(Ise(TJ)*
+ (pH0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)*Nh)/
+ (1e20*(ni(TJ)**2)), -1e6,1e6)}
.FUNC Ipe(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT((q*A*Dph(TJ)/Wh)*
+ (pH0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)
+ -pHW(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)),-1e6,1e6)}
.FUNC Inb(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT(Ine(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)+IQH,
+ -1e6,1e6)}
.FUNC Ipb(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT(Ipe(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)-IQH,
+ -1e6,1e6) }
.FUNC dVdE(VD,TJ) {IF(VD¡-2e-3*(TJ-27),-2e-3*(TJ-27),0)}
.FUNC Vdep(VDG,XJ) {MAX(VDG,0)+VN*(1-SQRT(1+MAX(VDG,0)/VN))}
.FUNC coshyp(XJ,TJ) {(exp((Wb-XJ)/La(TJ))+exp((Wb-XJ)/(-La(TJ))))/2}
.FUNC F1(XJ,TJ) {LIMIT(1/(taub(TJ)*(coshyp(XJ,TJ)-1)),-1e6,1e6) }
.FUNC F2(XJ,IXJ,TJ) { 0.5*(1+tanh(((Wb-XJ)/(6*Da(TJ))) * dxj(IXJ))) }
.FUNC F3(XJ,IXJ,TJ) {LIMIT(1+TD(XJ,IXJ,TJ)/taub(TJ), -1e6, 1e6) }
.FUNC TD(XJ,IXJ,TJ) { LIMIT((0.1*(Wb-XJ)*(Wb-XJ)/Da(TJ))/
+ (1+((Wb-XJ)/(12*Da(TJ)))*dxj(IXJ)), -1e6,1e6) }
.FUNC Qs0(XJ,TJ) {LIMIT(q*A*La(TJ)*1e10*ni(TJ)*
+ tanh((Wb-XJ)/(2*La(TJ))),0,1e6) }
.FUNC QL(VQ) {LIMIT(VQ*1u,-1e6,1e6)}
.FUNC QH(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT(q*A*Wh*(pH0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)+
+ pHW(IA,IMOS,IQH,VQ,XJ,IXJ,TJ))/2,-1e6,1e6)}
.FUNC QLd(IMOS,VQ,XJ,IXJ,TJ) {LIMIT(QL(VQ)+Inc(IMOS)*TD(XJ,IXJ,TJ), -1e6,1e6)}
.FUNC pse(IA,TJ) {Ise(TJ)*Wh/(q*A*Dph(TJ))}
.FUNC pt(IA,TJ) {IA*Wh/(q*A*Dph(TJ))}
.FUNC kse(IA,XJ,TJ) {1/((Qs0(XJ,TJ)**2)*((1e20*ni(TJ)**2)+pse(IA,TJ)*Nh))}
.FUNC jse(IA,XJ,IXJ,TJ) {TD(XJ,IXJ,TJ)*kse(IA,XJ,TJ)*Ise(TJ)}
.FUNC QL0N(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {2*(QLd(IMOS,VQ,XJ,IXJ,TJ)-jse(IA,XJ,IXJ,TJ)
+ *Nh*pt(IA,TJ)*(Qs0(XJ,TJ)**2)-TD(XJ,IXJ,TJ)*IQH)}
.FUNC QL0D(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {F3(XJ,IXJ,TJ)+SQRT((F3(XJ,IXJ,TJ)**2)+
+ 4*jse(IA,XJ,IXJ,TJ)*(1e20*ni(TJ)**2)*(QLd(IMOS,VQ,XJ,IXJ,TJ)
+ -jse(IA,XJ,IXJ,TJ)*Nh*pt(IA,TJ)*(Qs0(XJ,TJ)**2)-
+ TD(XJ,IXJ,TJ)*IQH))}
.FUNC QL0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT(QL0N(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)/
+ QL0D(IA,IMOS,IQH,VQ,XJ,IXJ,TJ),0,1e6)}
.FUNC IL0(IA,IMOS,,IQH,VQ,XJ,IXJ,TJ) {LIMIT(QL0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)/
+ +taub(TJ) ,-1e6,1e6)}
.FUNC pL0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT((1e10*ni(TJ)*
+ QL0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)/Qs0(XJ,TJ)),0,1e20)}
.FUNC pHW(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT((pL0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)**2)
+ /Nh ,0,1e20)}
.FUNC pH0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {LIMIT((pHW(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)
+ +pt(IA,TJ))/(1+pse(IA,TJ*Nh/(1e20*ni(TJ)**2)),0,1e20)}
.FUNC w(XJ) { LIMIT(Wb-XJ,1e-4,Wb)}
.FUNC xj(VDK) { LIMIT(SQRT((2*eps0*epsi*(VDK))/(q*Nb)),0,Wb-1e-4) }
.FUNC dxj(IXJ) {LIMIT(IXJ,-1,1)/1n}

Table 5.5: SPICE analytical functions of PSpice Kraus-based IGBT ET mode for FS devices.

Base resistance equations
.FUNC Neff(TJ) {un(TJ)*Nb/(un(TJ)+up(TJ))}
.FUNC ps0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {pL0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)/sinh((Wb-XJ)/La(TJ))}
.FUNC lambda(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {SQRT(Da(TJ)*QL(VQ)/(Inc(IMOS)-
+ Inb(IA,IMOS,IQH,VQ,XJ,IXJ,TJ))}
.FUNC artanh(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {0.5*log((1+x(IA,IMOS,IQH,VQ,XJ,IXJ,TJ))
+ /(1-x(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)))}
.FUNC x(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {(SQRT(Neff(TJ)**2+ps0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)**2)
+ *tanh((Wb-XJ)/(2*lambda(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)))/
+ (Neff(TJ)+ps0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)*
+ tanh((Wb-XJ)/(2*lambda(IA,IMOS,IQH,VQ,XJ,IXJ,TJ))))}
.FUNC RL(IA,IMOS,,IQH,VQ,XJ,IXJ,TJ) {(2*lambda(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)/(q*A*(un(TJ)+
+ up(TJ))*SQRT(Neff(TJ)**2+ps0(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)**2)))
+ *artanh(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)}
.FUNC VRL(IA,IMOS,IQH,VQ,XJ,IXJ,TJ) {IA*RL(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)}
Avalanche breakdown equations
.FUNC dBVce(TJ) {BVce(TJ)-BVce0}
.FUNC BVce(TJ) {BVce0*(((T0+TJ)/300)**0.3)}
.FUNC Igen(XJ,TJ) {LIMIT((q*1e10*ni(TJ)*A*XJ)/taub(TJ),0,1e6)}
.FUNC Mav(VDK,TJ) {1/(1-((VDK/BVce(TJ))**6))}
.FUNC Iav(IA,IMOS,VDK,IQH,VQ,XJ,IXJ,TJ) {(Mav(VDK,TJ)-1)*
+ (Ipc(IA,IMOS,IQH,VQ,XJ,IXJ,TJ)+IMOS)+Mav(VDK,TJ)*Igen(XJ,TJ)}

Table 5.6: PSpice FS IGBT ET model: equations for avalanche breakdown and base resistance.

Coefficients for mobility model
.PARAM unc=1417 upc=470.5
+ unm1=52.2 upm1=44.9 unm2=52.2 upm2=0
+ un1=43.4 up1=29 Pcn=0 Pcp=9.23e16
+ Crn=9.68e16 Crp=2.23e17 Csn=3.43e20 Csp=6.1e20
+ alfan=0.68 alfap=0.719 betan=2 betap=2
Physical parameters of n^- drift region
.PARAM un0={(unm1*exp(-Pcn/Nb))+(unc-unm2)/(1+((Nb/Crn)**alfan))-un1/
+ (1+((Csn/Nb)**betan))}
.FUNC un(TJ) {un0*((300/(T0+TJ))**1.5)}
.PARAM up0={(upm1*exp(-Pcp/Nb))+(upc-upm2)/(1+((Nb/Crp)**alfap))-up1/
+ (1+((Csp/Nb)**betap))}
.FUNC up(TJ) {up0*((300/(T0+TJ))**1.5)}
.FUNC b(TJ) {un(TJ)/up(TJ)}
.FUNC Da(TJ) {(2*kB*un0*up0/(q*(un0+up0)))*(T0+TJ)*((300/(T0+TJ))**1.5)}
Physical parameters of n FSL region
.PARAM uph0={(upm1*exp(-Pcp/Nh))+(upc-upm2)/(1+((Nh/Crp)**alfap))-up1/
+ (1+((Csp/Nh)**betap))}
.FUNC uph(TJ) {uph0*((300/(T0+TJ))**1.5)}
.PARAM Dph0={kB*(T0+27)*uph0/q}
.FUNC Dph(TJ) {kB*(T0+TJ)*uph(TJ)/q}
.PARAM Lph0={SQRT(Dph0*th)}
Physical parameters of p^+ emitter region
.PARAM Ne=5e18 *given as a constant value
.PARAM une0={(unm1*exp(-Pcn/(Ne+Nh)))+(unc-unm2)/(1+(((Ne+Nh)/Crn)**alfan))
+ -un1/(1+((Csn/(Ne+Nh))**betan))}
.FUNC une(TJ) {une0*((300/(T0+TJ))**1.5)}
.PARAM Dne0={kB*(T0+27)*une0/q}
.FUNC Dne(TJ) {kB*(T0+TJ)*une(TJ)/q}

Table 5.7: PSpice equations for Masetti's model implementation in PSpice.

Device models
.model M NMOS(Level=1, VTO={Vth}, KP={Kp})
.model DE D(Is={IsE0+IsH0}, CJO={Cje})
.model DC D(IS={IsC}, CJO={Cjc}, BV={Bvce0})

Table 5.8: Mosfet and diodes models definition for PSpice FS IGBT ET model.

Parameter	STD value	Unit
A	0.1	cm^2
A_{gd}	0.05	cm^2
V_{th}	5.5	V
K_p	5	A/V^2
K_f	2.5	$none$
C_{ox}	2.5n	F
C_{gs}	1.5n	F
R_g	0.1	Ω
R_s	10m	Ω
W_B	55e-4	cm
N_B	1.5e14	cm^{-3}
τ_B	5e-7	s
W_H	2.5e-4	cm
N_H	1e17	cm^{-3}
τ_H	5e-8	s
I_{sE0}	2.5e-14	A
I_{sC}	2.5e-14	A
C_{jE}	450p	F
C_{jC}	450p	F
BV_{ce0}	650	V

Table 5.9: Standard model parameters for PSpice Kraus-based FS model.

injection in n^- doped drift region and low-level injection in n doped FSL region are assumed for normal device operating conditions, by considering the typical values of doping concentration N_B and N_H. Accordingly, the values of hole density at the edges of both drift region and FSL, which are explicitly calculated within the model, must satisfy the following conditions:

$$\begin{cases} p_{L0} \gg N_B \\ p_{H0}, p_{HW}, \ll N_H \end{cases} \tag{5.18}$$

In figure 5.6 the PSpice simulated behaviour of steady-state hole densities p_{L0},p_{H0} and p_{HW} with collector-to-emitter voltage V_{ce} for a DC IGBT characteristic at V_{ge}=15V and T_j=27 °C, are depicted: even at large saturation current values (V_{ce} >3V), the assumption on injection level is valid.

As discussed earlier, the Kraus model is based on the control of the carriers charge in the PNP n doped region: in the FS IGBT structure the total amount of charge has two contributions, which are the holes charge Q_H in the n FSL region and the both hole-electron charge Q_B in the n^- drift region. Both of them are always acting during IGBT DC forward conduction operation to reduce the overall device on-state voltage, but, due to increase of J_2 depletion

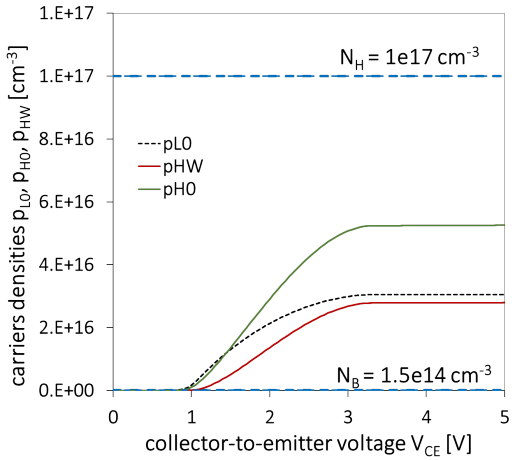


Figure 5.6: Simulated behaviour of hole densities p_{L0},p_{H0} and p_{HW} with steady-state V_{ce} voltage at V_{ge}=15V and T_j=27 °C.

region x_j with collector-to-emitter voltage, the value of Q_B tends to zero as V_{ce} voltage approaches the punch-through voltage defined by:

$$V_{ce,PT} = \frac{qN_B W_B^2}{2\epsilon_0 \epsilon_{Si}}. \tag{5.19}$$

The steady-state qualitative behaviour of $p_L(x)$ and $p_H(x)$, the holes density profiles respectively within the drift region and Field-Stop layer, are reported in fig. 5.7 at different values of collector-to-emitter voltage V_{ce} (until punch-through occurs) and V_{ge}=15V and T_j=27 °C: the simulations have been performed with Synopsys Sentaurus TCAD tool on a single-cell device structure, which has previously been calibrated on a commercial FS IGBT.

From these simulations is possible to appreciate the trend of carriers charge Q_L and Q_H (which are equal to the area above respectively the $p_L(x)$ and $p_H(x)$ doping profiles) with high V_{ce} values, that is well reproduced by the PSpice FS model, as shown in figure 5.8a, where behaviour of steady-state carriers charges is plotted during simulations of DC IGBT characteristic at V_{ge}=10-15-20V and T_j=27 °C.

As we expect, the FSL carriers charge Q_H remains almost constant with increasing collector-to-emitter DC voltage, while drift region carriers charge Q_L falls to zero at punch-through voltage ($V_{ce,PT} \simeq$ 430V), when the electric field reaches the FSL layer edge. Similarly, the trend of hole densities p_{L0},

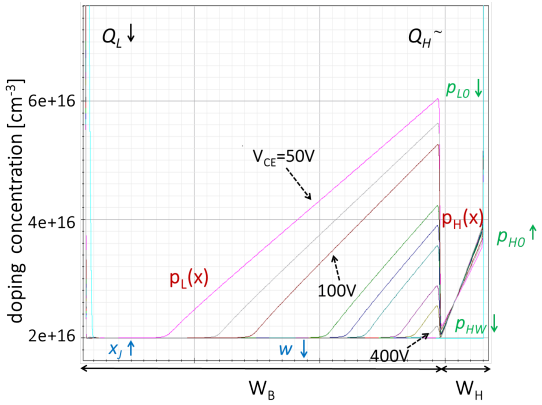
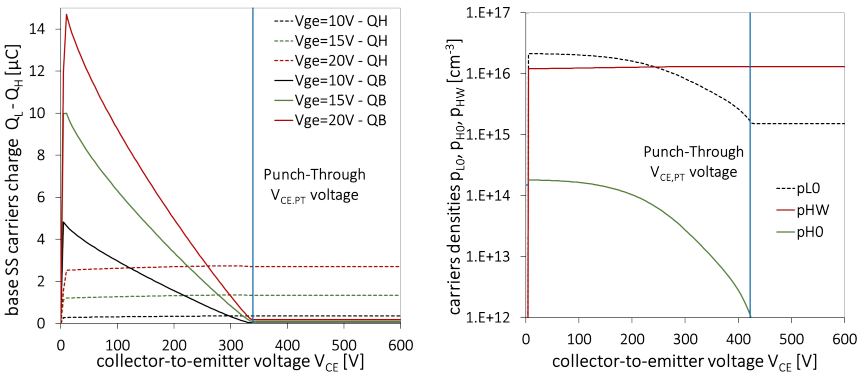


Figure 5.7: TCAD simulations of drift region and FSL DC hole profiles $p_L(x)$ and $p_H(x)$ for different values of V_{ce} voltage (V_{ge}=15V and T_j=27 °C).

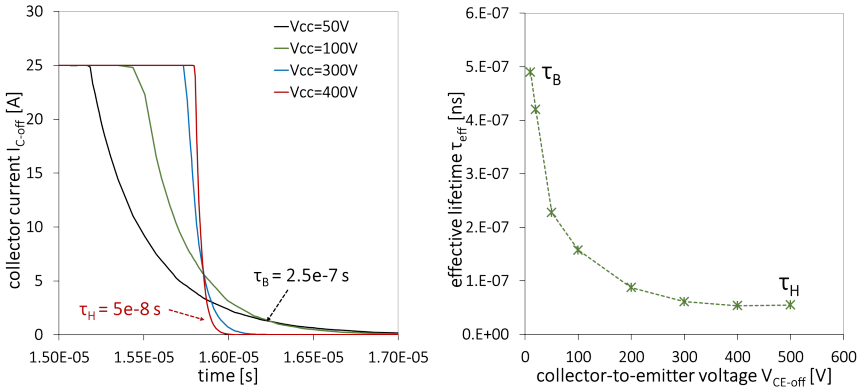


(a) (b)

Figure 5.8: PSpice model simulations of IGBT DC characteristics: a) behaviour of drift region and FSL carriers charges (Q_{L0} and Q_H) at V_{ge}=10-15-20V and of b) hole densities p_{L0}, p_{H0} and p_{HW} at V_{ge}=15V.

p_{H0} and p_{HW} at high values of steady-state collector-to-emitter voltage, until punch-through occurs, is properly outlined by the PSpice model: in particular, p_{Hw} must follow the trend of p_{L0} according to the 5.8, while the p_{H0} must decrease with V_{ce} in order to guarantee that FSL carriers charge remains almost constant. Furthermore, some important features due to the presence of the buffer-layer in the Field-Stop IGBT structure, affect device transient behaviour too. For instance, the turn-off transient collector current tail, is strongly dependent on steady-state current that is turned-off as well as on collector-to-emitter voltage (V_{cc} DC link voltage). In fact, since in the NPT structure the electric field never reaches the p^+ emitter edge for V_{ce} voltage values below the device blocking voltage, there is always a non-depleted region within the n^- drift region in which minority carriers (the charge Q_B) are present and need to recombine during turn-off phase, just after the Mosfet electron current switch-off. This recombination is governed by the high-level injection lifetime τ_B of the drift region at all collector-to-emitter turn-off voltage values. On the contrary, in the FS IGBT structure, the electrical field reaches the FSL corresponding to the $V_{ce,PT}$, so for turn-off V_{cc} voltage values larger than punch-through voltage, the drift region is completely depleted and the carriers charge lies only in the FSL. Hence, minority carriers recombine according to the FSL lifetime τ_H, that is usually smaller than drift region one. This effect is properly reproduced by FS PSpice model: in figure 5.9 simulations of turn-off inductive transient collector current at different V_{cc} (R_g=10 Ω, I_{cc}=25A, L=250 μH and T_j=27 °C) are reported.

It's clear that at low value of turn-off V_{cc} voltage values, the current tail is much more pronounced than at larger voltage values, due to the difference between drift region and FSL region lifetimes, that is one order of magnitude (τ_B=5E-7s and τ_H=5e-8s). This is also confirmed by plotting the effective lifetime τ_{eff}, evaluated as the time constant of turn-off transient current tail, as function of DC link voltage V_{cc} (figure 5.9b): at very low voltage values the minority carriers effective lifetime is actually the lifetime in n^- drift region, since the effect of FSL is negligible, while at V_{cc} values larger than punch-though voltage $V_{ce,PT}$, the effective lifetime tends to FSL region lifetime, since the drift region is completely depleted. These considerations are very useful for the extraction of both lifetime parameters from experimental measurements of turn-off collector current waveforms at different values of turn-off voltage V_{cc}.



(a) (b)

Figure 5.9: a) IGBT simulated I_c waveforms for a turn-off transient on inductive load at I_{cc}=25A, L=250 μH and T_j=27 °C and at different V_{cc} voltage values; b) behaviour of effective lifetime τ_{eff} versus V_{cc} voltage.

Conclusion

This dissertation has presented the development of a PSpice IGBT electro-thermal (ET) model based on the semi-mathematical approach proposed in Kraus model. In fact, it was immediately clear from state of art analysis that an enhancement of the IGBT SPICE modeling approach was actually needed, because both compact models implemented as built-in library model within SPICE circuit simulators (NIGBT in PSpice OrCad, HiSim in SPICE ELDO, etc.) and models provided by IGBTs manufacturers itself still show a drastic trade-off between accuracy and speed/convergence properties. Although initial version of Kraus model suffers of low accuracy and convergence issues when used in PSpice simulators, some improvements have been properly carried out: for instance, the electron injection due to PiN effect into the Mos-gate structure of the IGBT, has been modelled by means a further model parameter, the linear transconductance factor K_F, which contributes to the increase of the Mosfet electron current, as also discussed in Hefner model. Moreover, the steady-state base carriers charge Q_{B0} explicit evaluation together with a substantial modification of model schematic have resulted in an increase of the model speed and convergence. The well-known Miller's impact ionization model has been added to take into account of IGBT avalanche breakdown phenomena, too. Furthermore, the model has been made suitable for electro-thermal (ET) simulation by defining the dependencies on temperature of all the semiconductor physical parameters: some circuital artifices were also needed to take into account the temperature dependence of Mosfet parameters V_{th} and K_p, of the junction J_1 built-in voltage and of the IGBT breakdown voltage which has been experimentally characterized on commercial Punch-Through and Field-Stop devices. Eventually, the temperature has been implemented as a network voltage node, in order to be externally accessible for thermal network connection. The model has been validated on a commercial Field-Stop trench-gate IGBT, rated 30 A, with a blocking voltage of 600 V: the set of model parameters was defined by means an automated parameters calibration

procedure based on curve-fitting method. The proposed calibration strategy first evaluates the incidence of each parameter on a simulated IGBT characteristic, then varies only a few more-relevant parameters to achieve the minimum error between experimental and simulated curve. For this purpose, a laboratory test setup was arranged for the experimental measurement of IGBT DC and transient main characteristics. Thus, obtained results confirm the capability of model to reproduce device static and dynamic behaviour under different electrical and temperature conditions. Since the SPICE compact models are mainly used by circuit designers, it's of significant relevance that they are able to reproduce IGBT electro-thermal behaviour even in circuit applications such as power converters. For this purpose, three different case-studies were considered in order to validate the PSpice ET model in more complex operating conditions: the first situation concerned a standard short-circuit test, performed by both IGBT manufacturer and device users to investigate its capability to sustain high current-voltage conditions for a certain time interval with the aim of defining the short-circuit operation SOA. Moreover, a DC-DC step-down converter was taken as example for simulation predictive analysis of IGBT power dissipation and converter overall efficiency. Finally, the application related to design of SC protection circuit parameters has been analysed: in particular, since the choice of parameters is usually performed according to rough design rules, the availability of an accurate electro-thermal model allows to effectively achieve an optimum design, with particular focus on the characteristics of the adopted IGBT. For each of the three scenarios, test circuits and setup were implemented in laboratory and DUT IGBTs voltage and current waveforms have been acquired during circuits operation at different conditions: on the contrary, PSpice equivalent circuits have been simulated using the proposed model for DUT IGBTs. The electro-thermal simulations performed highlighted the accuracy and efficiency of model in reproducing real device behaviour with excellent results also in terms of speed and convergence. The last part of this work was dedicated to the extension of the PSpice IGBT Kraus-based model to Field-Stop devices, by means the addition of the approximated analytical equations describing the physics of Field-Stop layer under certain hypothesis within the model formulation. In particular, an explicit expression of the n^- drift region steady-state carriers charge Q_{L0} was evaluated taking into account FSL parameters. Finally, some qualitative simulations have been performed to verify model accordance with expected IGBT physical and electrical behaviour, also obtained with TCAD simulations.

Appendix A

Kraus IGBT NPT model PSpice implementation

Hereinafter the PSpice OrCad implementation of Kraus IGBT model for Non-Punch-Through devices: no temperature dependence of physical parameters has been considered, so model it's not capable of reproducing both static and dynamic device characteristics at different temperatures. Hence, model parameters listed in table 2.2 (chapter 2) have to be defined, or extracted from experimental device characteristics, at a specific temperature value.

In fig. A.1 the PSpice schematic of IGBT model is shown: in fact, since PSpice has a circuits drawing CAD (Capture CIS) and an embedded library with models and symbols of electrical elements, the parts of the model which consist of electrical components and devices such as voltage-current controlled sources, resistors, capacitors, diodes, Mosfet, can be simply drawn in the schematic environment in order to better understand model characteristics. On the other hand, it's always possible to write a list of SPICE directives which synthesize the overall circuit itself. In both cases the circuital parts of the model must be combine with model parameters definition in fig. A.1, physical constants and device models definition in table A.1 and analytical functions listed in table A.2 in order to obtain the complete model.

Due to the characteristics of a SPICE simulator, many analytical expression can be synthesized with a circuital implementation: for example, the time-derivative (in transient simulation) of n^- base depletion region width x_j with PNP bipolar transistor collector-to-base voltage V_{bc} (equal to Mosfet drain-source voltage V_{ds}), can be obtained by considering the sub-circuit, in fig. A.1, in which a DC voltage generator of instantaneous value x_j is placed in paral-

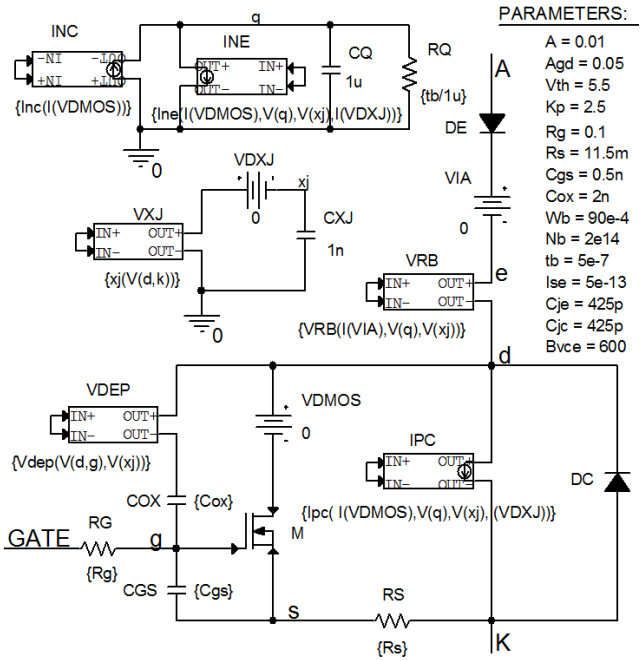


Figure A.1: PSpice schematic of the Kraus IGBT NPT model.

Physical constants
.PARAM q=1.602e-19 ni=1.45e10 eps0=11.8 epsi=8.85e-14 + un=1350 up=450 Dn=36 Dp=11.3 .PARAM b={ un/up} .PARAM Da={2*Dn*Dp/(Dn+Dp)} .PARAM La={SQRT(Da*tb)} .PARAM QN={q*A*Nb*Wb} .PARAM VN={q*Nb*eps0*epsi*((Agd/Cox)**2)}
Device models
.model M NMOS(Level=1, VTO={Vth}, KP={Kp}) .model DE D(Is={IsE}, CJO={Cje}) .model DC D(IS={IsC}, CJO={Cjc}, BV={Bvce})

Table A.1: Model physical constant and PSpice embedded diode and Mosfet models definition.

```
Analytical functions
.FUNC Inc(IMOS) {LIMIT(IMOS,0,1e6)}
.FUNC Ipc(IMOS,VQ,XJ,IXJ) {LIMIT((1/b)*Inc(IMOS)+(1+1/b)
+       *(Qb0(IMOS,VQ,XJ,IXJ)*F1(XJ)+F2(XJ,IXJ)*
+       MAX((-Qb0(IMOS,VQ,XJ,IXJ)
+       -Qb(VQ))/TD(XJ,IXJ),0)) ,0,1e6)}
.FUNC Ine(IMOS,VQ,XJ,IXJ) {LIMIT(IsE*((Qb0(IMOS,VQ,XJ,IXJ)/
+       Qs0(XJ))**2),0,1e6)}
.FUNC I0(IMOS,VQ,XJ,IXJ) {LIMIT(Qb0(IMOS,VQ,XJ,IXJ)/tb,0,1e6)}
.FUNC VRB(IA,VQ,XJ) {IA*Rb(VQ,XJ)}
.FUNC Vdep(VDG,XJ)) {MAX(VDG,0)+VN*(1-SQRT(1+MAX(VDG,0)/VN))}
.FUNC coshyp(XJ) {(exp((Wb-XJ)/La)+exp(-(Wb-XJ)/La))/2}
.FUNC F1(XJ) {LIMIT(1/(tb*(coshyp(XJ)-1)),-1e6,1e6)}
.FUNC F2(XJ,IXJ) {LIMIT(0.5*(1+TANH(((Wb-XJ)/(6*Da))*dxj(IXJ))),
+       -1e6,1e6)}
.FUNC F3(XJ,IXJ) {LIMIT(1+TD(XJ,IXJ)/tb,-1e6,1e6)}
.FUNC TD(XJ,IXJ) {LIMIT((0.1*((Wb-XJ)**2)/Da)/(1+((Wb-XJ)/
+       (12*Da))*dxj(IXJ)),-1e6,1e6)}
.FUNC Qs0(XJ) {LIMIT(q*A*La*ni*TANH((Wb-XJ)/(2*La)),0,1e6)}
.FUNC Qbd(IMOS,VQ,XJ,IXJ) {LIMIT(Qb(VQ)+Inc(IMOS)*TD(XJ,IXJ),0,1e6)}
.FUNC Qb0(IMOS,VQ,XJ,IXJ) {LIMIT(2*Qbd(IMOS,VQ,XJ,IXJ)/(F3(XJ,IXJ)
+SQRT((F3(XJ,IXJ)**2)+4*TD(XJ,IXJ)*IsE*Qbd(IMOS,VQ,XJ,IXJ)/
+       (Qs0(XJ)**2))),0,1e6)}
.FUNC Qb(VQ) {LIMIT(VQ*1u,-1e6,1e6)}
.FUNC xj(VDK) {LIMIT(SQRT((2*eps0*epsi*VDK/(q*Nb)),0,Wb-1e-4)}
.FUNC dxj(IXJ) {LIMIT(IXJ,-1,1)/1n}
.FUNC Rb(VQ,XJ) {(Wb**2)/(un*QN+(un+up)*Qb(VQ))}
```

Table A.2: Analytical functions for model physical variables.

lel with a capacitor C_{xj}, and the capacitative current is exactly $C_{xj}\dfrac{dx_j}{dt}$. One of the main requirements for the SPICE model implementation is to ensure numerical convergence in any simulation conditions: this is pursued by using a limiting function *.LIMIT* in order to restrict the variation domain of each model variable to a define range. Normalization of SPICE variables, which are always nodes of an electrical network, is also needed to avoid both numerical overflow and underflow. An important solution is the use of an explicit expression for *cosh*, in terms of exponential functions: in fact, although function *COSH* is provided in embedded PSpice library, its analytical explicit formulation ensures better convergence, especially in transient simulation.
Respect to Kraus equation for PNP collector-side hole current I_{pC} given in 2.23, the PSpice implemented expression has been slightly modified, in order to make it directly dependent on both steady-state and transient carriers base charge (Q_{B0} and Q_B) , instead of diffusion current I_0 and I_Q. By substituting the 2.21, it becomes:

$$I_{pC} = \frac{1}{b} I_{nC} + \left(1 + \frac{1}{b}\right)\left[F_1 Q_{B0} + F_2\left(\frac{-Q_{B0} + Q_B}{T_D}\right)\right] \qquad \text{(A.1)}$$

Definitively, the IGBT model set of analytical functions and electrical network variables constitutes a system of *linearly dependent differential equations*

with certain initial conditions (the external voltage-current circuit conditions) which are solved by SPICE simulator numerical algorithms for evaluating the DC or transient solution.

In order to explain some features of the model regarding its capability to reproduce the main physical phenomena of an IGBT structure both in steady-state and transient case, qualitative simulations of an ideal Non-Punch-Through IGBT model with standard parameters (reported in table A.1) are performed and the results are shown in fig. A.2. For instance, the steady-state conductivity modulated base resistance R_B (modelled with expression in 2.25) is simulated as function of collector-to-emitter IGBT voltage for different values of gate-emitter voltage (fig. A.2a): as the injection level increases with V_{ge} voltage, the carriers charge Q_{B0} within the quasi-neutral base region becomes larger contributing to the reduction of R_B (conductivity modulation) till Mosfet channel reaches the pinch-off (IGBT collector current approaches its saturation value). Moreover, in fig. A.2b, the behaviour of depletion region width x_j and quasi-neutral region width w (2.5,2.6) with collector-to-emitter voltage (V_{ge}=15V) is simulated: since the considered NPT IGBT structure has a punch-through voltage V_{PT} of about 900 V and the avalanche breakdown should occur almost close to 600 V, the depletion region edge never reaches the base-emitter junction during device operation (electric field doesn't "punch-through" the junction). With regard to transient IGBT characteristics simulated through the Kraus model, the hole recombination of the open-base PNP bipolar transistor during IGBT turn-off transition is represented by carriers charge ΔQ_B equal to:

$$\Delta Q_B = Q_B - Q_{B0}, \tag{A.2}$$

that is the rate of charge remaining within the quasi-neutral region immediately after the gate-emitter voltage goes below the threshold voltage V_{th}, and the Mosfet electron current is set to zero. The behaviour of transient ΔQ_B for different values of steady-state collector current I_c is shown in fig. A.2c: IGBT typical effect of "current-tail" is influenced by ΔQ_B and of course by base high-injection level lifetime τ_B. The Miller effect on collector-to-emitter voltage during both turn-on and turn-off IGBT transient is well modeled by Kraus model via controlled voltage source *VDEP*, that defined a non-linear Mosfet gate-to-drain capacitance: this is demonstrated by plotting qualitative turn-off V_{ce} and V_{ge} waveforms for different values of gate resistance (fig. A.2d).

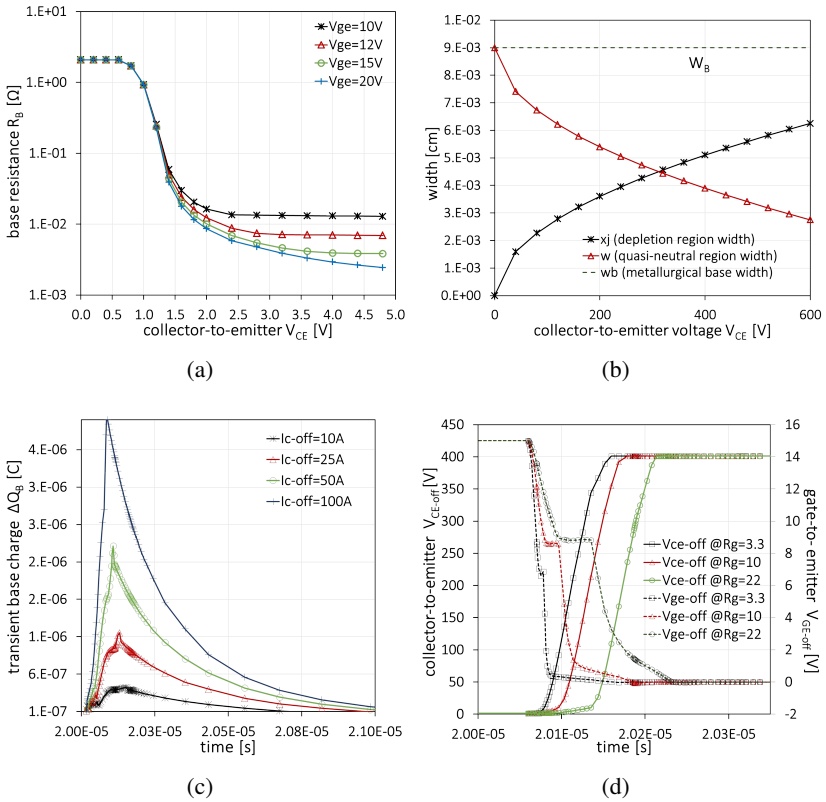


Figure A.2: Qualitative simulation of model physical characteristics for IGBT with standard parameters: a) steady-state conductivity base resistance R_B at different V_{ge} values; b) behaviour of depletion region and quasi-neutral region widths with collector-to-emitter IGBT voltage at V_{ge}=15Vb; c) excess turn-off transient base carrier charge ΔQ_B for different values of steady-state collector current; d) the Miller effect on turn-off V_{ce} and V_{ge} waveforms for different values of gate resistance R_g.

Appendix B

Algorithm for model parameters calibration

As discussed in chapter 1, compact models of IGBT implemented in SPICE simulators are intended to reproduce the static and dynamic device behaviour when used in circuit simulation: they also must guarantee a flexible use in modeling a large number of device technological families, with a good accuracy and high speed performances. For the purpose, a compact model can be roughly considered as a blackbox: in input there is the set of model parameters $(p_0, ..., p_N)$, voltage-current circuit conditions, time and device temperature, in output the static and dynamic device characteristics as depicted in fig. B.1.

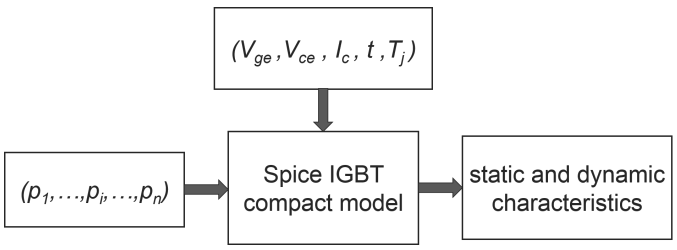


Figure B.1: Simplified scheme of IGBT compact model in circuit simulation.

Usually parameters extraction techniques ([52]-[35]-[83]) are long and complex and often don't return acceptable results, especially when available model doesn't exactly replicate the physics of device. Hence, whatever the model, values of parameters have to be properly chosen in order to fit experimental device electrical characteristics. A feasible solution is to apply a curve-

fitting method, focused on the evaluation of a matrix of differential coefficients which define the impact of each model parameter on an IGBT characteristics: for example by considering an IGBT output DC characteristic $I_c - V_{ce}$ and assuming steady-state and constant temperature (isothermal characteristic) conditions, current expression is:

$$I_{c,DC} = I_c(V_{ge}, V_{ce}, \overrightarrow{p}), \qquad at \quad T_j = 27°C \tag{B.1}$$

where $\overrightarrow{p}$ is the vector of N model parameters $(p_1, ..., p_N)$. Therefore, if $\overrightarrow{p_0}$ is the vector of initial non-calibrated parameters and p_{j-} and p_{j+} are small-deviation (e.g., $\pm 5\%$) values around the $j\text{-}th$ parameter initial value, the differential coefficient of parameter p_j respect to the DC characteristic is evaluated according the following expression:

$$\frac{dI_c\left(V_{ge}, V_{ce}, \overrightarrow{p_0}\right)}{dp_j} = \\ \frac{1}{M}\sum_{i=1}^{M} \frac{I_{c,i}\left(V_{ge}, V_{ce,i}, \overrightarrow{p_0}\left(p_j = p_{j+}\right)\right) - I_{c,i}\left(V_{ge}, V_{ce,i}, \overrightarrow{p_0}\left(p_j = p_{j-}\right)\right)}{I_{c,i}\left(V_{ge}, V_{ce,i}, \overrightarrow{p}_0\right)} \tag{B.2}$$

The so-obtained matrix of differential coefficients allows to introduce a new-idea in the field of calibration techniques, that makes this approach differ from the methods can be found in literature ([84]-[85]) by essentially two aspects: 1) the procedure is suitable for any kind of IGBT PSpice model, 2) calibration of parameters is achieved by substantially reducing the large space of solutions, since only some parameters are to be changed to match the experimental curves. Thus, a procedure for calibrating IGBT PSpice model parameters is developed and then implemented in MATLAB environment. The algorithm flow is shown in fig. B.2 and it can be split in four different parts:

- definition of PSpice model and starting vector of parameters (p_0);
- acquisition of experimental curves;
- evaluation of differential coefficients and assignment of a sub-vector of parameters to each curve;
- variation of parameters to reduce the simulated-experimental curve error.

A MATLAB-to-PSpice interface has been realized in order to automatically launch circuital simulation of the device characteristics and process the acquired data within MATLAB environment [5]; at the input of the entire algorithm IGBT PSpice model has to be defined and a starting vector of model parameters for the DUT IGBT has to be provided (measured, extracted or standard values) together with device experimental curves (DC output characteristics, transfer-characteristic, blocking characteristic, switching voltage-current waveforms at rated conditions).

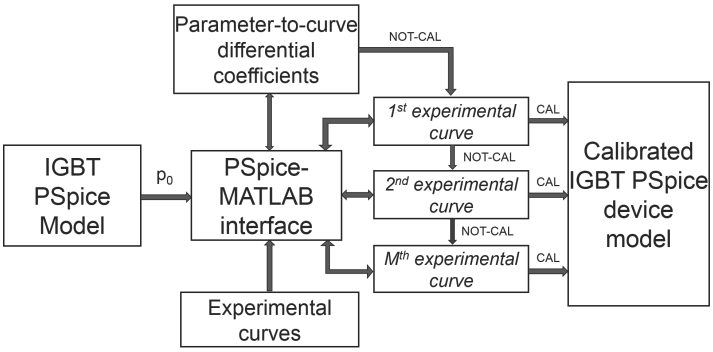


Figure B.2: Algorithm flow for parameters calibration procedure.

According to the evaluated matrix of differential parameter-to-curve coefficients, the main of the program automatically splits the vector of parameters and establishes a sub-vector of most relevant parameters for each simulated device characteristic. So sub-vectors are iteratively calibrated to minimize the error with experimental curve. Hence, if N is the dimension of starting parameters vector and m the number of values to be investigated for each parameters, the dimension of solution space is drastically reduced:

$$m^N \Rightarrow m^{N_1}+, ..., m^{N_R}, \qquad with \quad N_1 + N_2 + ... + N_R \leq N, \qquad \text{(B.3)}$$

where R is the number of considered device characteristics. During the execution, system separately calculates a matrix of error coefficients for each characteristic: for example, in case of first characteristic, combining the m possible values of N_1 parameters, algorithm calculates the error matrix (m^{N_1} coefficients) and returns the parameters sub-vector that minimizes the error between simulated and experimental characteristic (fig. B.3).

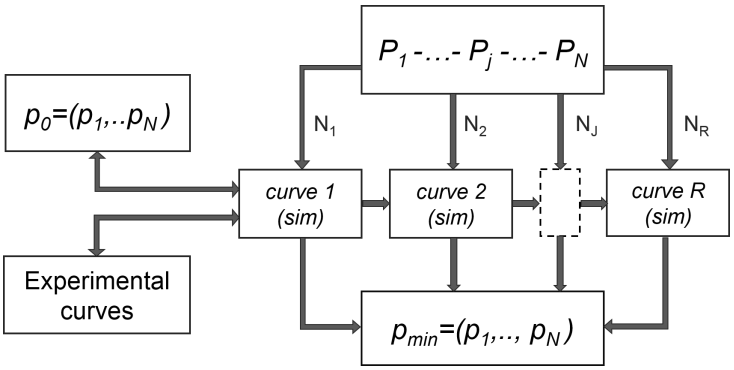


Figure B.3: Splitting of parameters vector and final vector for minimum error.

A further reduction in the computational rate of the calibration procedure is achieved by applying the renowned "bisection method": setting m (number of values for each parameter) equal to three, initial value and two extreme values (initial $\pm$ an X percentage variation around the central value) are considered. The entire cycle is repeated by halving the X percentage parameters variation to achieve a finer solution of the problem. With this expedient the problem is dramatically simplified and final computational rate is reduced to:

$$m^N \Rightarrow m^{N_1} +, ..., m^{N_R} \Rightarrow S \times (3^{N_1} + ... + 3^{N_R}), \tag{B.4}$$

S is the number of cycles (according to desired resolution on parameters values) and $m \gg 3$ to obtain the same variation interval and resolution gained with bisection method.
As a case study, the NIGBT model implemented in PSpice OrCad simulator, presented in chapter 2, is considered. In table B.1 the list of model parameters is reported and parameter-to-curve differential coefficients (estimated on standard parameters values) for some device static and dynamic characteristics are listed.

It can be noticed that some parameters (in bold) are more relevant than others, so they are varied in order to match the particular experimental curve, keeping the other parameters constant. In order to demonstrate the effectiveness of calibration procedure, a PT trench-gate IGBT rated 200 A-600 V is modelled using the previously introduced NIGBT model in PSpice OrCad environment. The extraction procedure proposed in [86] for Hefner'based mod-

Parameter	Standard value	Unit	Differential coefficients		
			DC-chars	Trans-char	V_{ge-off}
AREA	1.0e-05	m^2	4.51	0.08	**3.01**
AGD	5.0e-06	m^2	0	0	**4.5**
WB	9.0e-05	m	**14.27**	1.45	1.54
TAU	7.1e-06	s	3.54	0.62	1.04
THETA	0.01	V^{-1}	0.18	0.05	0.01
JSNE	6.5e-13	A/cm^2	1.8	0	0.03
CGS	1.24e-08	F/cm^2	0	0	**2.03**
COXD	3.5e-08	F/cm^2	0	0	**3.25**
KF	1	$none$	**8.13**	0	0.05
NB	2e+14	cm^2	**7.88**	0.09	1.32
KP	0.38	A/V^2	2.95	**7.63**	0.34
VT	4.7	V	4.06	**14.52**	1.34
VTD	1e-03	V	0	0	**3.75**
MUN	1500	$cm^2/V \cdot s$	**9.15**	0.65	0.15
MUP	450	$cm^2/V \cdot s$	**6.66**	1.36	0.41
BVN	4	*none*	0	0	0.8
BVF	1	*none*	0	0	0.45

Table B.1: List of model parameters and differential coefficients.

els is used for definition of vector of initial parameters p_0: however, the simulated device characteristics using extracted parameters are slightly far from experimentally measured characteristics, so calibration of parameters is needed. The starting S and the set of calibrated parameters are listed in table B.2, and percentage variation between initial and final value for each parameter is estimated.

Final set of parameters is obtained by applying the procedure with a variation of 50% to the initial vector of parameters and decreasing the variation interval through "bisection method" to reach a resolution of 1%. The algorithm involving PSpice OrCad simulations and data processing in MATLAB environment is executed on a laptop and overall computational time is estimated to be few hours. Unlike the DUT NIGBT model with extracted physical parameters that is not capable to properly match the experimental device characteristics, its version using calibrated parameters well approximate, in simulation, experimentally measured device characteristics, as shown in fig. B.4: algorithm searches for minimum error solution but some mismatches can be due to possible other solutions of the problem or to parasitic elements which are not contemplate in reference simulated circuit as collector parasitic inductance that is responsible for high overvoltage on turn-off switching V_{ce} waveform, in fig. B.4d. Furthermore, the major limitation regards the use of a simplified

Parameter	p_0**-extracted**	p**-calibrated**	**Variation**	**Unit**
AREA	1.20e-04	1.31e-04	8.90%	m^2
AGD	8.00e-05	6.48e-05	19.00%	m^2
WB	6.50e-05	7.16e-05	10.18%	m
TAU	2.16e-07	2.70e-07	25.02%	s
THETA	6.40e-03	7.40e-03	15.63%	V^{-1}
JSNE	2.08e-12	1.83e-12	11.95%	A/cm^2
CGS	8.00e-08	5.69e-08	28.91%	F/cm^2
COXD	5.00e-08	6.66e-08	33.10%	F/cm^2
KF	5.42	9.64	77.92%	$none$
NB	3.50e14	2.70e14	22.91%	cm^{-3}
KP	17	17.37	4.90%	A/V^2
VT	8.55	8.72	2.01%	V
VTD	-1.09	-1.20	10.00%	V
MUN	1500	1500	0.00%	$cm^2/V \cdot s$
MUP	450	450	0.00%	$cm^2/V \cdot s$
BVN	4.00	4.00	0.00%	$none$
BVF	1.00	1.75	75.00%	$none$

Table B.2: NIGBT extracted and calibrated model parameters for DUT: percentage of variation.

NPT structure to model a Punch-Through device: in fact, for example, while experimental DUT DC characteristics are influenced by n^- drift high-level injection lifetime and turn-off base charge recombination (current tail) at high V_{ce} values, depends mainly on buffer-layer lifetime, NIGBT model has only one lifetime parameter, *TAU*, for both static and dynamic device behaviour. Therefore a compromise among bipolar parameters such as *TAU*, *JSNE*, *WB* and *NB* is needed to properly fit the device experimental behaviour: anyway it's expected to necessarily incur in some mismatches as happens in case of DUT, on turn-off V_{ce} waveform rise rate and on collector current waveform behaviour.

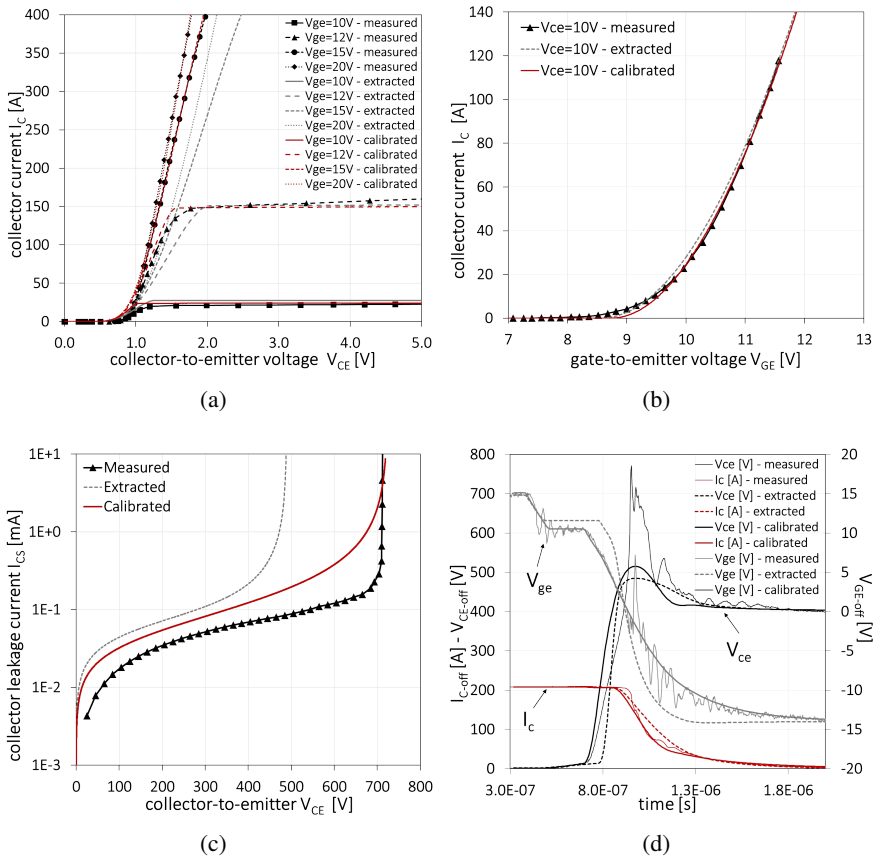


Figure B.4: Enhancement obtained by means the parameters calibration respect to extracted parameters on DUT IGBT simulated characteristics, using NIGBT model: a) DC characteristics @V_{ge}=10-12-15-20V, b) transfer-characteristic @V_{ce}=10V, c) blocking characteristic and d) inductive turn-off transient current and voltages waveforms @ V_{cc}=400V, I_{cc}=200A, R_g=15 Ω and L=250μH.

Appendix C

Evaluation of Q_{L0} in FS Kraus model

The explicit expression for steady-state n^- drift region carriers charge Q_{L0} in case of FS Kraus-based PSpice model, is found by substituting FSL equations reported in section 5.1 into the diffusion current continuity equation given in 5.6. This latter can be also written as:

$$Q_{L0} = \frac{Q_L + T_D I_{QL}}{F_3}, \tag{C.1}$$

where $F_3 = \dfrac{1 + T_D}{\tau_L}$. By substituting in C.1 the relations:

$$\begin{cases} I_{QL} = I_{nC} - I_{nB}, \\ I_{nB} = I_{nE} + I_{QH}, \end{cases} \tag{C.2}$$

taken from current continuity equations 5.1, the Q_{L0} becomes function of MOS electron-current I_{nC} and FSL diffusion current I_{QH} according to the follow expression:

$$Q_{L0} = \frac{Q_{LD} - T_D I_{nE} + T_D I_{QH}}{F_3}, \tag{C.3}$$

with $Q_{LD} = Q_L + T_D I_{nC}$. Since p^+ emitter-side electron current I_{nE} is a function of Q_{L0} through the FSL equations, the purpose is to find this relation to explicitly solve the C.3 in terms of Q_{L0}. As already seen for Q_{B0} in NPT IGBT model, the Q_{L0} is the integral of the steady-state ADE solution for hole density $p_L(x)$ within the n^- drift region, so p_{L0} can be expressed as:

$$Q_{L0} = qAL_a p_{L0} tanh\left(\frac{W}{2L_a}\right) \Rightarrow p_{L0} = n_i \frac{Q_{L0}}{Q_{s0}} \tag{C.4}$$

where the charge $Q_{s0} = qAL_a n_i tanh\left(\frac{W}{2L_a}\right)$ has been defined. By substituting the relation of p^+ emitter electron current 5.4 and the current continuity equation:

$$I_{pE} = I_T - I_{nE}, \tag{C.5}$$

into the p^+ emitter side hole current I_{pE} (5.5), the hole densitiy p_{H0} at emitter side of FSL, is expressed as function of p_{HW} and of IGBT total current I_T:

$$p_{H0} = \frac{p_{HW} + p_T}{1 + \frac{p_{sE} N_H}{n_i^2}}. \tag{C.6}$$

The following quantities have been defined for simplification:

$$\begin{cases} p_{sE} = \dfrac{I_{sE} W_H}{qAD_{pH}} \\ p_T = \dfrac{I_T W_H}{qAD_{pH}} \end{cases} \tag{C.7}$$

The relation between hole densities p_{L0} and p_{HW} at junction J_1 given in 5.8 can be expressed in terms of Q_{L0}:

$$p_{HW} = \frac{p_{L0}^2}{N_H} = \frac{n_i^2}{N_H}\left(\frac{Q_{L0}}{Q_{s0}}\right)^2. \tag{C.8}$$

By substituting expressions C.8 into C.6 and then into 5.4 we obtain:

$$I_{nE} = \frac{I_{sE} N_H \left(\frac{n_1^2}{N_H}\frac{Q_{L0}^2}{Q_{s0}^2} + p_T\right)}{\left(n_i^2 + p_{sE} N_H\right)} \tag{C.9}$$

Now the relation between I_{nE} and Q_{L0} needed to be inserted into the diffusion current continuity equation C.3:

$$F_3 Q_{L0} = Q_{LD} - T_D I_{nE} + T_D I_{QH} =$$

$$Q_{LD} - \frac{T_D I_{sE} n_i^2 Q_{L0}^2}{Q_{sO}^2 (n_i^2 + p_{sE} N_H)} + \frac{T_D I_{sE} N_H p_T}{(n_i^2 + p_{sE} N_H)} + T_D I_{QH} = \tag{C.10}$$

$$Q_{LD} - j_{sE} n_i^2 Q_{L0}^2 - j_{sE} N_H p_T Q_{s0}^2 - T_D I_{QH},$$

where the quantity $j_{sE} = \dfrac{T_D I_{sE}}{Q_{s0}^2 (n_i^2 + p_{sE} N_H)}$ has been defined for simplification. Hence we have the second degree equation of Q_{L0}:

$$(j_{sE} n_i^2) Q_{L0}^2 + F_3 Q_{L0} - Q_{LD} + j_{sE} N_H p_T Q_{s0}^2 + T_D I_{QH}, \tag{C.11}$$

and the solution:

$$Q_{L0} = \frac{-F_3 \pm \sqrt{F_3^2 + 4 j_{sE} n_i^2 (Q_{LD} - j_{sE} N_H p_T Q_{s0}^2 - T_D I_{QH})}}{2 j_{sE} n_i^2}. \tag{C.12}$$

By selecting the positive sign and multiplying/dividing for $F_3 + \sqrt{...}$, finally we obtain the explicit solution for n^- drift region steady-state carriers charge Q_{L0} given in 5.11:

$$Q_{L0} = \frac{2(Q_{LD} - j_{sE} N_H p_T Q_{s0}^2 - T_D I_{QH})}{F_3 + \sqrt{F_3^2 + 4 j_{sE} n_i^2 (Q_{LD} - j_{sE} N_H p_T Q_{s0}^2 - T_D I_{QH})}} \tag{C.13}$$

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