TESI DI DOTTORATO

UNIVERSITÀ DEGLI STUDI DI NAPOLI "FEDERICO II"

DIPARTIMENTO DI INGEGNERIA ELETTRICA
E DELLE TECNOLOGIE DELL'INFORMAZIONE

DOTTORATO DI RICERCA IN
INGEGNERIA ELETTRONICA E DELLE TELECOMUNICAZIONI

A STANDARD CELL BASED HIGH RESOLUTION ALL-DIGITAL PULSED WIDTH MODULATOR WITH SPREAD SPECTRUM CAPABILITY IN 130*nm* CMOS

MICHELE DE MARTINO

Il Coordinatore del Corso di Dottorato
Ch.mo Prof. Niccolò RINALDI

Il Tutore
Ch.mo Prof. Davide DE CARO

A. A. 2014–2015

Contents

List of Figures

List of Tables

Introduction

A pulsed width modulated signal is a square wave signal with a fixed frequency and a digitally adjustable duty-cycle. Digital Pulsed Width Modulators, also called DPWM, are widely used in power delivery applications, where the power transferred to the load is linked to the duty cycle of the input signal. Typical power applications which require a DPWM are DC/DC converters, like step-down (Buck) and step-up (Boost), inverters and class D amplifiers. Pulsed width modulated signals are periodic, and due to their periodicity, the energy of the frequency spectrum is concentrated around the fundamental switching frequency and it's harmonics. Since in power application, these switching signals make large amounts of current commute very fast, the energy peaks in the spectrum can be very high and can overcome limits imposed by international regulations on Electromagnetic Interference (EMI).

EMI is an energy disturbance that affects the performance of electrical/electronic circuits due to conducted power source or radiated electromagnetic fields, that may interfere with the electronic equipment connected to it or other equipment in proximity of it, causing problems like data loss, performance degradation and even equipment damage. In power supplies, the two prominent types of EMI are conducted EMI and radiated EMI. In switched-mode power applications, conducted EMI is primarily caused by fast voltage changes. Unfortunately, this is how all switched-mode power supplies work. The fast edges contain many harmonics and these harmonics are coupled into both inputs and outputs with different damping. The rise and fall times also influence the high frequency content of the noise. Reducing the switching speed improves EMI behavior but reduces efficiency, especially in hard-switched topologies. Radiated EMI issues in switched-mode power supplies are generally related to currents being switched. This usually happens in sync with some clock frequency. Switching a current can trigger resonant tanks in the application, and they then resonate with their characteristic frequency. It is clear that EMI performance can no longer be considered only after the design

is finished. Now days, the EMI reduction has become a major design issue.

Comprehensive regulations provide limitations to radiated and conducted EMI generated when the power supply is connected to the mains. Two considerations of these standards are:

- Limit the amount of emission (radiated/conducted) which a given application generates;
- Define the minimum immunity levels (radiated/conducted) a given application must tolerate without malfunction.

There are various standards e.g. CISPR (Europe), FCC (USA), and military standards that specify the maximum allowable emission levels, and prescribe also precise measurements procedures in order to evaluate compliance with regulations. The common theme is that certain standards define the limit values and their measurement methods and conventions, and additional documents define the regulations for classes of applications in more detail. Additionally, standards can be grouped into local/regional standards, MIL standards, automotive standards, standards for the aircraft industry, for physically large equipment, and for more specialized equipment (e.g. smart meters).

Many methods for reducing the EMI level have been developed. The shielding is a traditional method for preventing EMI emissions. This method consists in covering, fully or partially the emission location with electromagnetic shields, that work by reflecting, absorbing or redirecting electric and/or magnetic fields. However, shielded enclosures are a poor substitute for good EMC design at the board level. Effective enclosures can add significant cost and weight to a product and a single breach of the enclosure (e.g. an unfiltered cable penetration) can completely eliminate any benefit the enclosure would otherwise provide. In many cases, a product in a poorly designed shielded enclosure will radiate more (or be more susceptible) than the same product without the enclosure. Another traditional method that allows to reduce EMI level is line-filtering. This method consists in using low-pass filters in order to eliminate the high-order harmonics. In particular, this method reduces rise and fall times of the signal in order to reduce the radiated EMI. The drawback is that in high-speed systems the filtering reduces critical setup and hold margins and increases the amounts of overshoot, resulting in a worsening of output signal jitter. It is important to note that the EMI filter will work most of the time in an unmatched setup, with the line and load impedances different from the design impedance of the filter, which is therefore reflecting most of the energy. The spread spectrum technique is a well known approach to reduce EMI of

electronic circuits by slowly sweeping (modulating) the frequency of a signal within a given frequency range with a predetermined modulation waveform. This approach allows to spread the energy associated to each clock harmonic over a certain bandwidth mitigating in this way the peak power level which may cause problems to other equipment.

In this work, a high-resolution Digital Pulsed-Width Modulator (DPWM) is presented in all it's aspects: design, simulations and post fabrication measurements. The proposed DPWM is also capable of performing frequency spreading on the generated output waveforms to reduce EMI.

The thesis is structured as follows:

- In the first part, following the electromagnetic interference (EMI) test guidelines, the peak level reduction of the spectrum (modulation gain) achievable by using frequency continuous modulated signals and frequency discontinuous modulated signals is theoretically analyzed.

- In the second part the most common approaches and architectures employed to realize Digital Pulsed Width Modulators are discussed. In literature, several DPWM architectures have been proposed, basically divided into three sub-categories: Counter Based DPWM, Delay-Lines based DPWM, and Hybrid DPWM, that tries to merge the advantages of the two previous categories.

- Finally, the design of an Digital Pulsed Width Modulator is presented. The circuit has an all digital architecture and it's design is completely based on standard cells simplifying porting when technology dimensions scale down. The circuit is capable to perform frequency spreading on the generated output pulsed-width modulated waveforms. First, the whole DPWM architecture is explained in detail, then the circuit sizing details are provided and the major components of deterministic jitter are analyzed. Finally , the results of experimental measurements on the test-chip are provided and discussed, and a comparison with the state of art is done.

Spread Spectrum Technique

Spread Spectrum [1] is a well known technique that allows to spread the energy associated to each harmonic of a square-wave signal over a certain bandwidth, mitigating the peak power level and reducing the EMI. it consists in slowly sweeping the frequency of the signal within a given frequency range and with a given modulation profile. The Modulation Gain is defined as the ratio between the peak power level of the n-th harmonic of the unmodulated signal, and the peak power level of the n-th harmonic of the modulated signal. The Modulation gain that can be obtained with the spread spectrum approach depends on modulation parameters, such as frequency deviation and modulation frequency, and on modulation waveform. Nowadays, a large number of applications like clock generation in high performance digital circuits [2–6], high speed serial links [7, 8] and switching power converters [9–12] use Spread Spectrum clocking technique. The procedures to evaluate the peak power level of frequency modulated waveforms are prescribed by EMI standards [13–16]. They require the analysis of the signal with a spectrum analyzer in swept-frequency mode with a predetermined resolution bandwidth (RBW), depending on the frequency of the waveform, and peak-type detector.

In literature, a Fourier series approach is often used to study the spectrum of frequency modulated waveforms as in [1]. This kind of approach leads in many cases in very different results when compared to experimental data obtained using a spectrum analyzer set with the EMI requirements on measurement [13–16]. This difference is due to the fact that the combined effect of the spectrum analyzer RBW and peak-type detector is not taken in account in the Fourier series analysis. For example, when a modulation profile as the triangular waveform, that is very common in literature, is analyzed using Fourier series, it provides a flat spectrum, resulting the best modulation profile in terms of modulation gain. Things change when the same triangular modulated waveform is analyzed taking in account the spectrum analyzer RBW and detector effects, because the spectrum obtained isn't totally flat anymore. A modula-

tion profile that gives a modulation gain higher than the triangular one when the spectrum analyzer RBW and detector are considered is empirically obtained in [17].

The work in [18] studies the problem of obtaining the spectrum of modulated waveforms analytically considering the combined effect of the spectrum analyzer RBW and detector, also showing for the first time that the optimal modulation frequency is close the spectrum analyzer RBW, when the peak type detector is considered. In [18, 19] the analytical approximation of the spectrum of modulated waveform obtained assumes the continuity of the modulating waveform, but in the case of discontinuous frequency modulated waveforms, only a coarse approximation is provided. The work in [20] extendes to frequency-discontinuous modulating waveforms the analysis of [18, 19]. From the applications point of view, having discontinuous frequency modulated clock signals does not result in any problem in high performance digital circuits clocking and switching power converters. This work also shows that discontinuous modulated waveforms con achive higher modulation gain instead continuous modulated waveform. in [20] is also obtained, in a closed form, the spectrum of a discontinuous frequency modulated signal, considering the effects of the spectrum analyzer RBW and detector.

2.1 Continuous Frequency Modulated Waveforms

Consider the function $u(t)$ as a clock signal with a constant frequency f_0. Using the Fourier series analysis, it can be written as:

$$u(t) = \sum_{k=-\infty}^{+\infty} \frac{I_{0\,k}}{2} \cdot \exp\left[j2\pi k\, f_0 t\right]. \tag{2.1.1}$$

To obtain the frequency modulated signal $u_s(t)$ from $u(t)$, a change of the time variable is needed:

$$u_s(t) = u(t') \tag{2.1.2}$$

where:

$$t' \equiv t + \frac{\delta}{f_m} \int_{-\infty}^{f_m t} V(\tau)\, d\tau \tag{2.1.3}$$

where $V(t)$ is a periodic function of unity period of values in [-1,1]. Merging the previous equations 2.1.1 2.1.2 and 2.1.3, the frequency modulated signal $u_s(t)$ can be written as:

$$\begin{aligned} u_s(t) = \sum_{k=-\infty}^{+\infty} \tfrac{I_{0\,k}}{2} \cdot \exp\left[j2\pi k\, f_0 \left(t + \tfrac{\delta}{f_m} \int_{-\infty}^{f_m t} V(\tau)\, d\tau\right)\right] = \\ = \sum_{k=-\infty}^{+\infty} \tfrac{1}{2} I_k(t) = \tfrac{I_{0\,0}}{2} + \sum_{k=1}^{+\infty} \mathrm{Re}\left[I_k(t)\right]. \end{aligned} \tag{2.1.4}$$

The instantaneous frequency $f(t)$ of this waveform can be easily computed as:

$$\begin{aligned} f(t) = \tfrac{1}{2\pi} \tfrac{d}{dt} \left[2\pi f_0 \left(t + \tfrac{\delta}{f_m} \int_{-\infty}^{f_m t} V(\tau)\, d\tau\right)\right] = \\ = f_0 \left(1 + \delta\, V\left(f_m\, t\right)\right) \end{aligned} \tag{2.1.5}$$

where f_m is the modulation frequency, and δ is the relative frequency deviation of the frequency modulated waveform:

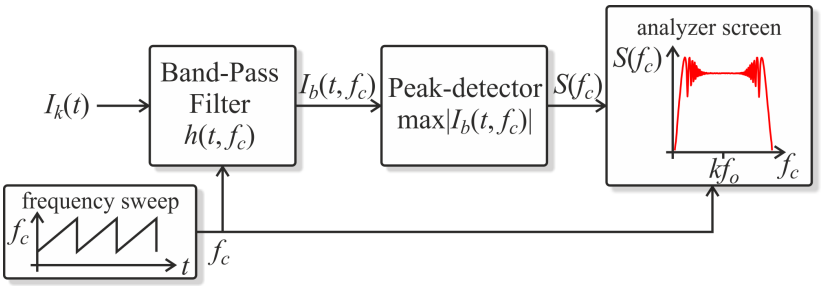

Figure 2.1.1: Model of a swept frequency spectrum analyzer in peak hold mode

$$\delta = \frac{\Delta f}{f_o}. \tag{2.1.6}$$

In the following of this chapter, assuming that $k \cdot \Delta f \ll f_0$ we can put the focus on the spectrum of a single frequency modulated harmonic $I_k(t)$ without considering the effect of the possible frequency overlapping of the modulated spectrums of the neighbor harmonic. The modulation gain is:

$$Gain \equiv \frac{I_{0\,k}}{\max\left[S(f_c)\right]} \tag{2.1.7}$$

where $I_{0\,k}$ is the amplitude of the unmodulated harmonic, that for a perfect square wave of amplitude A is given by:

$$I_{0\,k} = 2A\frac{\sin\left(k\pi/2\right)}{k\,\pi} \tag{2.1.8}$$

and $S(f_c)$ is the spectrum of the frequency modulated harmonic $I_k(t)$, and it's maximum is the spectrum peak value.

EMI measurement standards [13–16] prescribe that the spectrum of a frequency modulated waveform must be measured by a swept-frequency spectrum analyzer in peak hold mode. This instrument can be modeled as shown in Figure 2.1.1. In this model the effect of the spectrum analyzer RBW is represented by a band pass filter with impulse response $h(t, f_c)$ centered around the frequency f_c, followed by a peak detector. The filter impulse response $h(t, f_c)$ can be written as:

$$(ht, f_c) = h_0(t) \cdot \exp\left[j2\pi f_c t\right] \tag{2.1.9}$$

where $h_0(t)$ is a low pass impulse response with -3 dB bandwidth RBW. The output signal of the filter can clearly be written as:

$$I_b(t, f_c) = \int_{-\infty}^{+\infty} I_k(t-\tau) \cdot h(\tau, f_c)\, d\tau. \tag{2.1.10}$$

Considering the effect of the peak-type detector, the spectral component $S(f_c)$ plotted by the spectrum analyzer at frequency f_c corresponds to the maximum absolute value of $I_b(t, f_c)$:

$$S(f_c) = \max\left|I_b(t, f_c)\right|. \tag{2.1.11}$$

The work in [19] introduces the criterion bandwidth defined as:

$$B_{sw} \equiv \sqrt{4k\Delta f \cdot f_m} \tag{2.1.12}$$

In [18, 19] it is demonstrated that no reduction of the peak spectral components can be achieved if $RBW \ll B_{sw}$. Contrariwise, in the hypothesis of $RBW \gg B_{sw}$, it is shown that the output of the pass band filter in Figure 2.1.1 can be approximated as follows:

$$I_b(t, f_c) \cong \sum_n \left(-jk\, f'(t_n)\right)^{-1/2} h(t - t_n, f_c)\, I_k(t_n) \tag{2.1.13}$$

where t_n are the time instants at which the instantaneous harmonic frequency $k \cdot f(t)$ corresponds to the filter center frequency f_c:

$$k \cdot f(t_n) = f_c. \tag{2.1.14}$$

Since we are interested in analyzing the properties of clock waveforms in frequency spreading applications, we will focus on the hypothesis when $RBW \gg B_{sw}$.

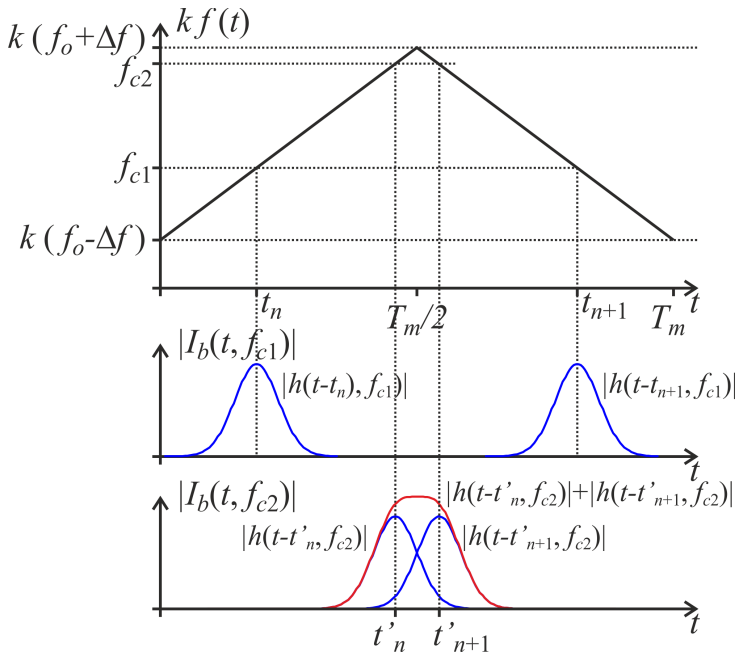

Figure 2.1.2: Schematic illustration of the output of the bandpass filter $I_b(t, f_c)$ considering a triangular modulation for two different filter center frequencies.

In Figure 2.1.2 is shown the output of the band-pass filter of Figure 2.1.1, in case of a triangular modulated waveform for two different frequencies f_{c1} and f_{c2}. The frequency f_{c1} is chosen in the proximity of the harmonic center frequency $k \cdot f_0$, while f_{c2} is chosen close to the upper instantaneous harmonic frequency $k \cdot (f_o + \Delta f)$. The plot of Figure 2.1.2 shows that in the case of f_{c1}, successive terms of the summation in (2.1.13), $h(t - t_n, f_c)$ and $h(t - t_{n+1}, f_c)$ do not interfere. Therefore, the value of $I_b(t, f_c)$, corresponding to $S(f_c)$, is independent from f_c but exclusively depends on the maximum value of $h(t, f_c)$ (approximately equal to RBW) and the first derivative of the instantaneous frequency $f(t)$. In the case of f_{c2} instead, always with reference to Figure 2.1.2, the two consecutive pulses of the summation in (2.1.13) $h(t - t_n, f_c)$ and $h(t - t_{n+1}, f_c)$ overlap. This overlap may lead to constructive or destructive interference, in dependence on the phase of the two pulses and then by the specific value of f_{c2}. These interferences generate an oscillating behavior in the spectrum. When the two pulses mentioned above interfere

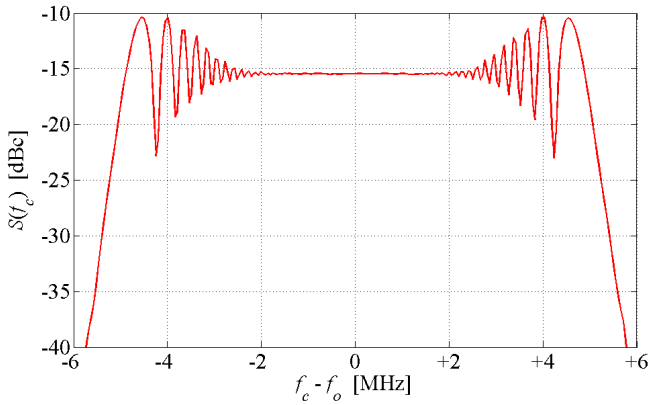

Figure 2.1.3: Spectrum $S(f_c)$ of the first harmonic of a clock signal with triangular modulation (Δf=5MHz, f_m =40kHz, RBW=100kHz)

constructively, the maximum output value of the filter increases, thereby increasing the peak value of the spectrum $S(f_c)$ of the frequency modulated waveform, and reducing the modulation gain achievable according to (2.1.7).

Figure 2.1.3 shows the simulated Spectrum $S(f_c)$ of the first harmonic (k=1) of a clock signal with triangular modulation assuming Δf=5MHz and f_m=40kHz, analyzed with RBW=100kHz. It can be observed that, for f_c close to f_0, as in the case of f_{c1}, the spectrum is almost flat and the modulation gain in this region corresponds to the ratio $RBW/\sqrt[2]{f'(t)}$. Otherwise when the frequency f_c is chosen close to the upper or lower instantaneous frequencies, respectively $f_0 + \Delta f$ $f_0 - \Delta f$, the oscillating behavior is present. When the interference between the two pulses is constructive, the maximum value of the spectrum $S(f_c)$ increases reducing the achievable modulation gain. Considering the same scenario, Figure 2.1.4 shows, just like Figure 2.1.2, the output of the band pass filter in Figure 2.1.1, but with the difference that in this case, the modulating waveform is a sawtooth waveform.

The figure highlights that, regardless of the chosen f_c, the time distance between two consecutive pulses is kept constant, and these pulses never interfere with each other. At this point, according to (2.1.13), we would expect a flat spectrum without any oscillating behavior. In Figure 2.1.5 is shown the simulated spectrum of a sawtooth modulated waveform with the same $f'(t)$ with

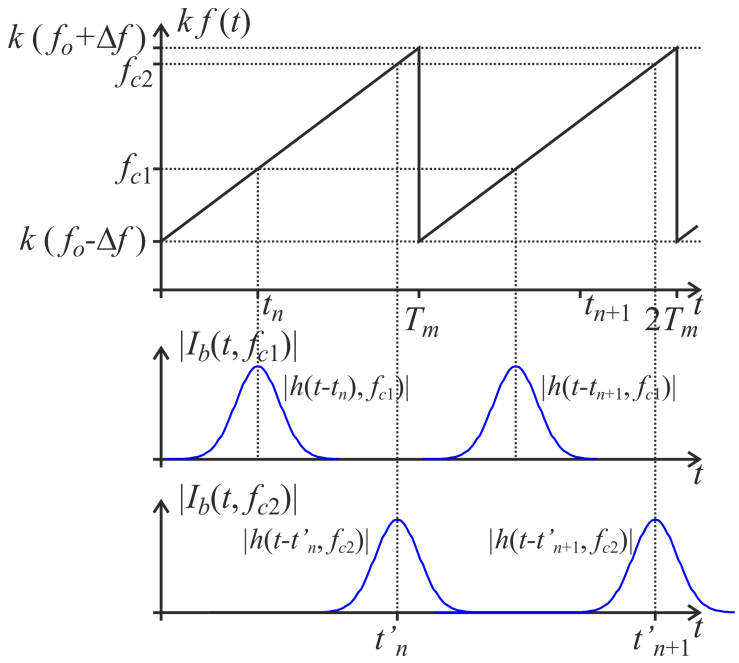

Figure 2.1.4: Schematic illustration of the output of the bandpass filter $I_b(t, f_c)$ considering a sawtooth modulation for two different filter center frequencies.

respect to Figure 2.1.3 (Δf=5MHz, f_m =80kHz). As expected, the modulation gain is much better than the one obtained with the triangular modulation, but surprisingly it is as good as the modulation gain achievable in the flat part of the spectrum because a little oscillating behavior, not predicted in (2.1.13), is still present. However, the nature of the oscillating behavior in Figure 2.1.5 has a different nature than the oscillating behavior in Figure 2.1.3. In this case, the oscillation is due to the discontinuity of the instantaneous modulating frequency. In fact, in the method of stationary phase used in [19] to derive (2.1.13), the continuity of the first and second derivatives of the phase is required [21]. For that reason, in the following subsection, another approximation of $I_b(t, f_c)$ is derived, this time taking into account the discontinuity of the modulating waveform.

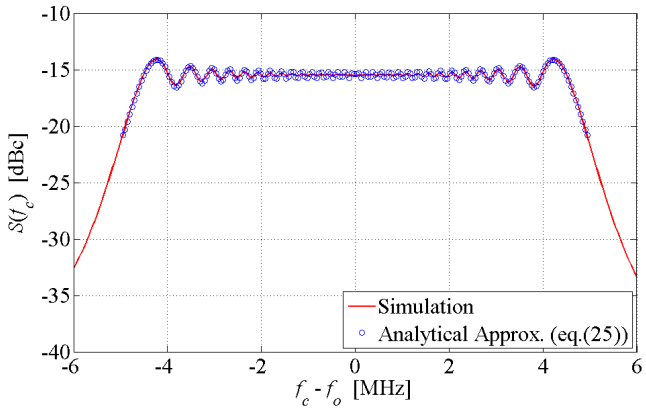

Figure 2.1.5: Spectrum $S(f_c)$ of the first harmonic of a clock signal with sawtooth modulation (Δf=5MHz, f_m =80kHz, RBW=100kHz)

2.2 Discontinuous Frequency Modulated Waveforms

In the previous section, it has been noted that discontinuous modulation profiles can help avoiding the interference at the output of the band-pass filter in Figure 2.1.1, that are the causes of the oscillating behavior, obtaining a better modulation gain with respect to continuous modulated waveforms. This happens because frequency discontinuity allows to realize modulations with a single phase stationary point (t_n) per modulation period, reducing in this way the constructive interference between successive phase stationary points. But it has been also shown that in the spectrum of discontinuous frequency modulated waveforms, an oscillating behavior is still present not predicted in (2.1.13), and this oscillating behavior is due to the discontinuity of the modulating waveform. To overcome this problem in the analytic study of the spectrum of discontinuous modulated waveforms, the number of frequency discontinuous points must therefore be minimized as well. To derive a model of $I_b(t, f_c)$ valid for discontinuous modulated waveforms, the signal described in (2.1.4) must be considered, where $V(t)$ is a monotonic function in $t \in [0, 1]$ with the following constraints:

$$\begin{cases} V(0) = -1 \\ V(1) = +1 \end{cases} \tag{2.2.1}$$

In this way the only frequency discontinuous points are located in $n \cdot T_m$, where T_m is the reciprocal of the modulation frequency f_m. Under this position, the value of $I_b(t, f_c)$ can now be computed as a summation of integrals with continuous integrands:

$$I_b(t, f_c) = \sum_{n=-\infty}^{+\infty} \int_{n \cdot T_m}^{(n+1) \cdot T_m} I_k(\tau) \cdot h(t-\tau, f_c)\, d\tau. \tag{2.2.2}$$

Each integral in the summation in (2.2.2) can now be computed with the method of stationary phase, since it's integrands are continuous as required in [21, 22]. In our asymptotic approximation requires the following conditions:

$$\sqrt{k\Delta f \cdot f_m} \gg RBW, \tag{2.2.3}$$

$$k\Delta f \gg f_m. \tag{2.2.4}$$

The condition in (2.2.3) is the criterion-bandwidth condition already discussed in the previous subsection. The second condition is always verified in spread spectrum application. In fact, under more simpler Fuorier analysis, in a frequency modulated signal where T_m is the modulation frequency, the components in the Fourier spectrum are spaced by f_m. The ratio $k \cdot \Delta f / f_m$ corresponds to the number of frequency components within the frequency modulation range, therefore if $k \cdot \Delta f \ll f_m$ no modulation gain is possible. Merging the condition in (2.2.3) and (2.2.4), with the assumption that the modulation function $V(t)$ is monotonic, each integral in (2.2.2) can be approximated as:

$$\begin{aligned} &\int_{n \cdot T_m}^{(n+1) \cdot T_m} I_k(\tau) \cdot h(t-\tau, f_c)\, d\tau \simeq \\ &\simeq \frac{1}{\sqrt{kf'(t_0)}} I_k(t_n)\, h(t - t_n, f_c)\, e^{j\pi/4} \cdot \Gamma\left(\delta t \sqrt{\pi k\, f'(t_0)}\right) \end{aligned} \tag{2.2.5}$$

where:

$$\Gamma(t) \simeq \frac{1}{2}\left(1 + \mathrm{C}\left[\sqrt{\frac{2}{\pi}} \cdot t\right] + \mathrm{S}\left[\sqrt{\frac{2}{\pi}} \cdot t\right]\right), \tag{2.2.6}$$

$$\delta t = \min\left[t_0, T_m - t_0\right]. \tag{2.2.7}$$

In (2.2.6) $C(t)$ and $S(t)$ are the well known Fresnel integrals. The point $t_n = t_0 + n \cdot T_m$ is the single phase stationary point in the interval $\tau \in [n \cdot T_m, (n+1) \cdot T_m]$. The stationary point in $[0, T_m]$, time instant t_0, as before, can be computed as the point at which the instantaneous harmonic frequency $k \cdot f(t)$ corresponds to the filter center frequency f_c in $[0, T_m]$ interval:

$$k \cdot f(t_0) = f_c \qquad t_0 \in [0, T_m]. \tag{2.2.8}$$

Substituting (2.2.5) in (2.2.2) we have:

$$I_b(t, f_c) \simeq$$
$$\simeq \sum_{n=-\infty}^{+\infty} \frac{1}{\sqrt{k f'(t_0)}} I_k(t_n)\, h(t - t_n, f_c)\, e^{j\pi/4} \cdot \Gamma\left(\delta t \sqrt{\pi k\, f'(t_0)}\right). \tag{2.2.9}$$

According to this equation, the filter response $I_b(t, f_c)$ is a superposition of equally spaced pulses $h(t - t_n, f_c)$, which amplitude is modulated by the Γ function. This function accounts for the effect of frequency discontinuous points. The spectral component $S(f_c)$, which corresponds to the maximum value of the filter output in Figure 2.1.1, can be computed when two pulses do not overlap each other. Since the time spacing between each consecutive pulse is T_m, and the duration of each pulse is approximately the RBW, two consecutive pulses do not interfere when:

$$f_m \ll RBW, \tag{2.2.10}$$

in this hypothesis:

$$S(f_c) \simeq I_0\, k \frac{1}{\sqrt{k f'(t_0)}} \max\left[h_0(t)\right] \cdot \Gamma\left(\delta t \sqrt{\pi k\, f'(t_0)}\right) \tag{2.2.11}$$

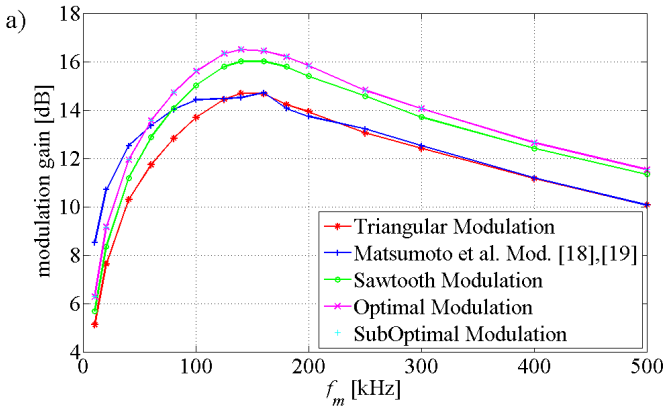

Figure 2.2.1: Modulation gain achieved with different modulations by varying f_m with fixed Δf=5MHz and RBW=100kHz

and the spectrum of a frequency modulated harmonic of the modulated waveform can be written as:

$$S(f_c) \simeq I_0\, k \frac{\max[h_0(t)]}{f_m} \cdot \frac{1}{\sqrt{k\frac{\Delta f}{f_m} V'(f_m t_0)}} \cdot \Gamma\left(f_m \delta t \sqrt{\pi k \frac{\Delta f}{f_m} V'(f_m t_0)}\right). \tag{2.2.12}$$

The Figure 2.1.5 shows how really good is the analytical approximation of $S(f_c)$ in (2.2.11) with respect to the simulation results.

Starting from the approximation in 2.2.11, the work in [20] formulates an optimization problem for the analytical determination of a discontinuous waveform which equalizes peaks in frequency domain and therefore provides an optimal modulation gain. This optimal discontinuous frequency modulation waveform, providing the highest modulation gain, is computed numerically as a solution of a non linear first order, boundary value problem with a Dirichlet boundary condition. In real applications, on the other hand, it is very helpful to have a closed form expression for the modulation waveform. The work [20] in addition provides a sub optimal modulation function that can be obtained as a solution of a linear differential equation, that can easily be solved analytically.

In Figure 2.2.1, different modulation techniques are compared in term of achieved modulation gain, by varying the modulation frequency f_m. It is con-

sidered the case in which Δf=5MHz, RBW=100kHz and f_m is varied between 10kHz and 500kHz. It can be seen that, in accordance with 2.2.12, when $f_m \ll RBW$, the modulation gain increases with f_m. When f_m becomes comparable to RBW, the condition in (2.2.10) is no more verified and the approximation in (2.2.12) becomes less accurate. With $f_m \gg RBW$, the spectrum analyzer filter doeas not have any effect on the spectrum anymore, and the spectrum of the frequency modulated waveform in this condition can be computed with the simple Fourier analysis. In fact, the modulation gain decreases with the increasing of f_m, because in the Fourier analysis the modulation gain is proportional to $\sqrt{\Delta f / f_m}$. The Figure 2.2.1 also shows that the optimal discontinuous modulation derived in [20] also achieves the absolute maximum modulation gain, 16.5dB, that is is 0.5dB and 2dB higher than the highest modulation gains achievable by using sawtooth modulation and frequency continuous optimal modulation, derived in [18, 19], respectively.

2.3 References

[1] K.B. Hardin, J.T. Fessler, and D.R. Bush. “Spread spectrum clock generation for the reduction of radiated emissions.” In: *Electromagnetic Compatibility, 1994. Symposium Record. Compatibility in the Loop., IEEE International Symposium on*. 1994, pp. 227–231.

[2] Jonghoon Kim et al. “Spread spectrum clock Generator with delay cell array to reduce electromagnetic interference.” In: *Electromagnetic Compatibility, IEEE Transactions on* 47.4 (2005), pp. 908–920.

[3] S. Damphousse and M. Mallinson. “All digital spread spectrum clock generator for EMI reduction.” In: *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*. 2006, pp. 962–971.

[4] T. Ebuchi et al. “A 125 1250 MHz Process-Independent Adaptive Bandwidth Spread Spectrum Clock Generator With Digital Controlled Self-Calibration.” In: *Solid-State Circuits, IEEE Journal of* 44.3 (2009), pp. 763–774.

[5] D. De Caro et al. “A 1.27 GHz, All-Digital Spread Spectrum Clock Generator/Synthesizer in 65 nm CMOS.” In: *Solid-State Circuits, IEEE Journal of* 45.5 (2010), pp. 1048–1060.

[6] Sewook Hwang et al. “A 3.5 GHz Spread-Spectrum Clock Generator With a Memoryless Newton-Raphson Modulation Profile.” In: *Solid-State Circuits, IEEE Journal of* 47.5 (2012), pp. 1199–1208.

[7] Sheng-You Lin and Shen-Iuan Liu. “A 1.5 GHz All-Digital Spread-Spectrum Clock Generator.” In: *Solid-State Circuits, IEEE Journal of* 44.11 (2009), pp. 3111–3119.

[8] F. Pareschi, G. Setti, and R. Rovatti. “A 3-GHz Serial ATA Spread-Spectrum Clock Generator Employing a Chaotic PAM Modulation.” In: *Circuits and Systems I: Regular Papers, IEEE Transactions on* 57.10 (2010), pp. 2577–2587.

[9] Feng Lin and D.Y. Chen. “Reduction of power supply EMI emission by switching frequency modulation.” In: *Power Electronics, IEEE Transactions on* 9.1 (1994), pp. 132–137.

[10] K.K. Tse et al. “Analysis and spectral characteristics of a spread-spectrum technique for conducted EMI suppression.” In: *Power Electronics, IEEE Transactions on* 15.2 (2000), pp. 399–410.

[11] J. Balcells et al. “EMI reduction in switched power converters using frequency Modulation techniques.” In: *Electromagnetic Compatibility, IEEE Transactions on* 47.3 (2005), pp. 569–576.

[12] K.K. Tse et al. “An evaluation of the spectral characteristics of switching converters with chaotic carrier-frequency modulation.” In: *Industrial Electronics, IEEE Transactions on* 50.1 (2003), pp. 171–182.

[13] FCC 47 CFR Part 15. *Radio frequency devices*. 2008.

[14] CISPR 22. *Information technology equipment - radio disturbance characteristics - limits and methods of measurement*. 2003-04.

[15] ANSI C63.4. *American national standard for methods of measurement of radio noise emissions from low voltage electrical and electronic equipment in the range of 9 kHz to 40 GHz*. 2003.

[16] ANSI C63.2. *American national standard for electromagnetic noise and field strength instrumentation, 10 Hz to 40 GHz specifications*. 1996.

[17] K. Hardin, R.A. Oglesbee, and F. Fisher. “Investigation into the interference potential of spread-spectrum clock generation to broadband digital communications.” In: *Electromagnetic Compatibility, IEEE Transactions on* 45.1 (2003), pp. 10–21.

[18] Y. Matsumoto, K. Fujii, and A. Sugiura. “Estimating the Amplitude Reduction of Clock Harmonics Due to Frequency Modulation.” In: *Electromagnetic Compatibility, IEEE Transactions on* 48.4 (2006), pp. 734–741.

[19] Y. Matsumoto, K. Fujii, and A. Sugiura. “An analytical method for determining the optimal modulating waveform for dithered clock generation.” In: *Electromagnetic Compatibility, IEEE Transactions on* 47.3 (2005), pp. 577–584.

[20] D. De Caro. “Optimal Discontinuous Frequency Modulation for Spread-Spectrum Clocking.” In: *Electromagnetic Compatibility, IEEE Transactions on* 55.5 (2013), pp. 891–900.

[21] A. Erdelyi. *Asymptotic Expansions*. New York: Dover Publications, 1956.

[22] C. Chapman. “Time-Domain Asymptotics and the Method of Stationary Phase.” In: *Proc. of the Royal Society of London Series A Mathematical Physical and Engineering Sciences*. Vol. 437. 1899. 1992, pp. 25–40.

Digital Pulsed Width Modulators

A digital pulse width modulator (DPWM) produces a fixed frequency clock signal with a digitally adjustable duty cycle, and it is an essential circuit block for fast-emerging digitally-controlled switching regulators used for supplying uniform power to loads. Digital implementations of these controllers for DC/DC converters presents many advantages compared to analog implementation: programmability, flexibility, ability to create complex control laws, immunity to variations in process or operating conditions (PVT), and easy portability when the technology scales down [1–7]. Typical requirements for such DPWM include high resolution, good linearity, and low power dissipation. In addition, in order to cover a wide variety of switching supply applications, it is necessary for the DPWM to support a wide range of operating frequency. The issue of obtaining a high resolution is very important in DPWMs to avoid limit cycling [8, 9]. In literature, several DPWM architectures have been proposed, and a classification is given in [10]. Counter-based DPWM [11, 12], despite the easy implementation and near perfect linearity, are limited by the fact that high input clock frequency is required. In fact, to obtain a N-bits resolution, the switching period $T_s = 1/f_s$ is subdivided in 2^N slots, and a counter clocked by a frequency of $2^N \cdot f_s$ is required. For example, for an output switching frequency of 1MHz and a 8-bit resolution, a 256GHz clocked counter would be necessary. Adding one resolution bit would double the input frequency of the counter. Hence, the power dissipation increases exponentially with the number of resolution bits. Delay-Line based DPWM overcomes this limitation by using a tapped delay-line and a multiplexer [13]. In this architecture, the duty-cycle of the output signal is adjusted by selecting different tap positions on the delay-line. Therefore, the resolution is determined by the unit stage delay rather than by the input clock frequency. Unfortunately, in this

architecture the total delay of the delay-line should be equal to the reference clock period. The resolution in this topology is determined by the delay of the single delay-element unit of the delay-line. For that reason the delay-line is a part of a delay-locked-loop (DLL), that generally requires analog circuits like charge-pump, loop-filter and so on. As a consequence of the presence of analog circuits, area and power increase, and the design is not easy portable with new technology nodes. In this DPWM topology, increasing the resolution demands shorter delays of the single delay-element unit, and consequently a larger number of delay-elements on the delay-line. Reaching N-bit resolution requires $2^N - 1$ delay-elements, and adding one resolution bit requires double the number of delay-elements. All of this means a larger silicon area request. Self-oscillating delay-line [2, 14] do not require neither an external clock frequency nor a DLL to work, sinche the delay-line is closed in a ring-oscillator configuration. This architecture has the advantage of an easy implementation with all-digital hardware, but on the other hand it still requires a large silicon area, and the performances are strongly related to PVT variations. Hybrid architectures try to merge the advantages of both counter based and delay-line based topologies. In this configuration, a counter is used to obtain a coarse resolution, while the fine resolution is obtained through a delay-line and multiplexer architecture. Hybrid DPWM are divided in self-oscillating, [15–17], in which the delay-line is configured as a ring oscillator, and non self-oscillating, [18] [19], where there is no inner clock generation. In the following subsection will be analyzed the most recurrent topologies in DPWM literature.

3.1 Counter Based DPWM

The counter based DPW is the simpliest digital PWM architecture, that can be obtained using an N-bit counter and N-bit comparator as shown in Figure 3.1.1. In this configuration, the digital code K is used to set the comparing value of the comparator.

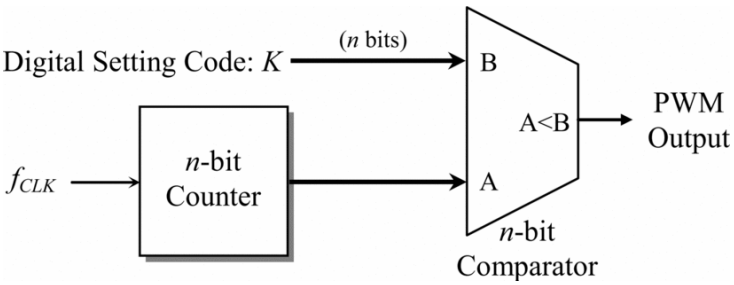

Figure 3.1.1: A simple counter based DPWM architecture

When the counter output is less than the K value, the output of the comparator $A < B$ remains high-level, and it stays high until the counter output becomes equal or higher than the K value, then it goes low-level. The pulse-width generated corresponds to the digital code K. In this architecture, for an N-bit counter based DPWM with an output frequency of f_{DPWM}, the input reference clock required is $f_{CLK} = 2^N f_{DPWM}$, and the modulation rate is:

$$D = \frac{T_K}{T_{DPWM}} = \frac{K \times T_{CLK}}{2^N \times T_{CLK}} = \frac{K}{2^N} \tag{3.1.1}$$

where T_K is the on time of the DPWM pulse controlled by K, and it's value goes from 0 to $2^N - 1$. As seen the resolution in this topology is proportional to the input reference clock. for this reason, this architecture is not suitable for high resolution implementation. The work in [20] tries to provide a new approach for DPWM design, which uses RC charge to perform digital to time conversion and further extend the resolution of the conventional counter-based DPWM. This approach splits the term T_K of (3.1.1) in two elements, T_{K1} and T_{K1}:

$$D = \frac{T_K}{T_{DPWM}} = \frac{T_{K1} + T_{K2}}{T_{DPWM}} = \frac{T_{K1}}{T_{DPWM}} + \frac{T_{K2}}{T_{DPWM}}. \tag{3.1.2}$$

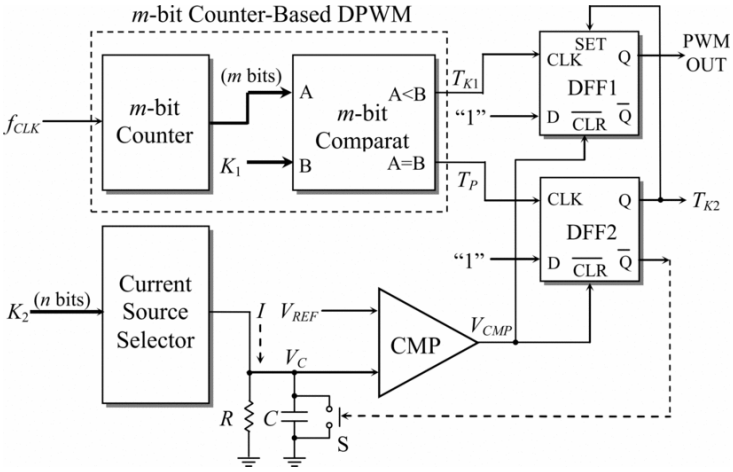

Figure 3.1.2: Architecture of counter-based DPWM using RC charge [20]

When using an m-bit counter-based DPWM with the reference clock f_{CLK} for T_{K1}, therefore, referring to equation (3.1.1), $T_{K1}/TDPWM$ is given by:

$$D = \frac{T_K 1}{T_{DPWM}} = \frac{K_1 \times T_{CLK}}{2^m \times T_{CLK}} = \frac{K}{2^N} \tag{3.1.3}$$

where K1 is the digital setting code from 0 to $2^m - 1$. T_{K2} is an n-bit resolution extention from the m-bit counter DPWM under the same f_{CLK}, and it can be expressed by:

$$T_{K2} = \frac{K_2}{2^n} \times T_{CLK} \tag{3.1.4}$$

where T_{K2} is the digital setting code from 0 to $2^n - 1$. The Duty cycle will become:

$$D = \frac{K_1}{2^m} + \frac{K_2}{2^{m+n}} = \frac{2^n \times K_1 + K_2}{2^{m+n}} \tag{3.1.5}$$

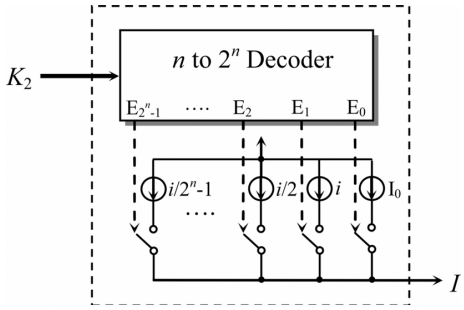

Figure 3.1.3: Structure of current source selector [20]

The architecture of the DPWM proposed in [20] is shown in Figure 3.1.2. Consider V_C as the charging voltage performed by current I charging through R and C after T_{K2} time, and V_C is given by:

$$V_C = I \times R \times (1 - e^{\frac{-T_{K2}}{RC}}) \tag{3.1.6}$$

where I is the current from the current source selector in Figure 3.1.3 with a unit current i for each current source, controlled by $1/K_2$. Let $RC > 1/T_{K2}$, then expanding the exponential of (3.1.6) in a series and ignoring the items with high power, V_C will become:

$$V_C = (\frac{I}{C}) \times T_{K2} = \frac{1}{K_2} \times (\frac{i}{C}) \times T_{K2} = \frac{1}{2^n} \tag{3.1.7}$$

which behaves like capacitor integration. By selecting $i/C = 1/T_{CLK}$, when V_C charges to the reference voltage V_{REF} corresponding to $1/2^n$ at $t = T_{K2}$, the extended pulse output T_{K2} with n-bit resolution will be generated.

With reference to Figure 3.1.2, the current source selector controlled by digital value K_2 uses an n to 2^n decoder (Figure 3.1.3) to select 2^n current sources corresponding to $1/K_2$. Each output of the decoder enable one current source, where the current source I_0 selected by $K_2 = 0$ has a large charging current to make V_C be immediately larger than the reference voltage V_{REF}, such that the Q output of DFF1 (PWM OUT) is almost equal to T_{K1} once $K2 = 0$. This architecture extends the counter based DPWM resolution from

m bits (of the counter), to n+m bits under the same reference clock. On the other hand, this architecture adds hardware complexity with analog components due to RC charge. It results in a greater demand for area, and a reduction in portability when the technology when dimensions scale down. In addition the improvement in resolution isn't still as good as in delay-line based architectures, specially with segmented ones, and hybrid.

3.2 Delay Line Based DPWM

To avoid the high reference frequencies required in counter based DPWM, delay-line based architectures for DPWMs are employed. A classic and simple delay-line based architecture is shown in Figure 3.2.1, constructed by a cascade of delay-cells, a multiplexer, and a SR flip-flop.

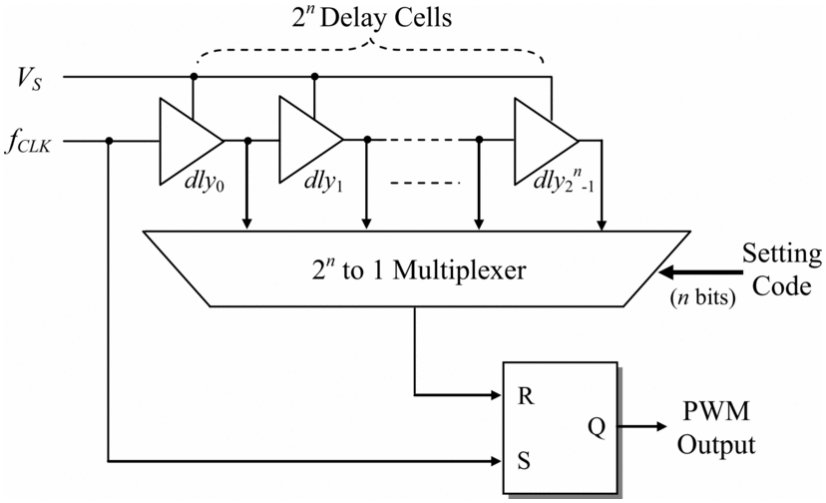

Figure 3.2.1: Delay-Line DPWM architecture

When the reference clock f_{CLK} enters the delay-line, the output of the SR flip-flop is set to the high level. By setting the n-bit code, the desired delay signal is selected at the output of the multiplexer, and it resets the the SR flip-flop until the next clock enters again. In this way, a modulated pulse signal is generated, with a frequency f_{CLK} equal to the reference clock frequency, and a duty cycle related to the number of delay-elements selected by the multiplexer setting code. In this architecture, the total delay of the delay-line must be at least equal to the reference clock period T_{CLK}. The linearity of the delay-line based DPWM is affected by the mismatch of the delay-cells caused by PVT variations [21], and thus more hardware components are required for better performance and linearity [22]. For achieving a better resolution, this DPWM requires a larger amount of delay-cells and a large scale multiplexer.

A segmented binary-weighted delay-line can also be used, as shown in Figure 3.2.2 for a 3-segment, 6-bit DPWM [23]. The additional delay compensation circuit is not shown for simplicity. Each segment has a 4-to-1 multiplexer controlled by two bits of $d[n]$. The delay in each of the four elements of the

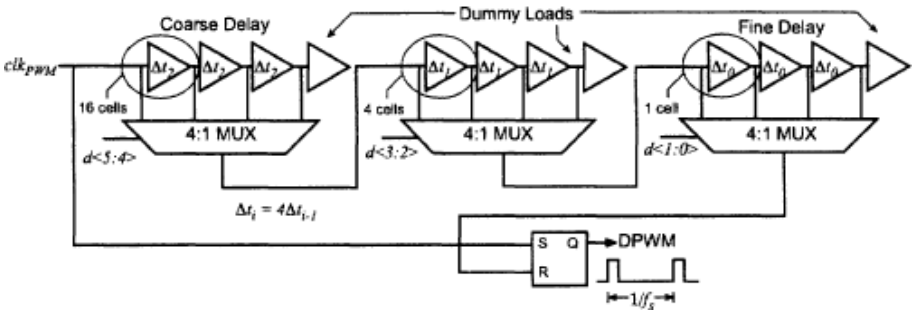

Figure 3.2.2: Simplified block diagram of a 3-segment, 6-bit DPWM [23]

i^{th} segment is given by:

$$\Delta t_i = 4\Delta t_{i-1} = 2^{2i}\Delta t_0 \tag{3.2.1}$$

The Δt_i delays are created by simply replicating the Δt_0 delay-cell, resulting in the same overall number of delay-cells, neglecting the additional dummy load cells. The modest area reduction compared to the traditional non-segmented delay-line DPWM comes from the multiplexer, since a 64-to-1 multiplexer is replaced by four 4-to-1 multiplexers.

To optimize area and power consumption of [23], the work in [24] uses

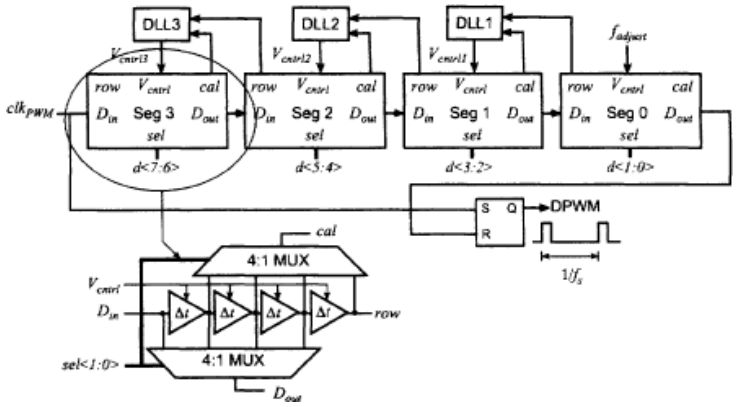

Figure 3.2.3: Conceptual block diagram of an 8-bit self-calibrated segmented DPWM [24]

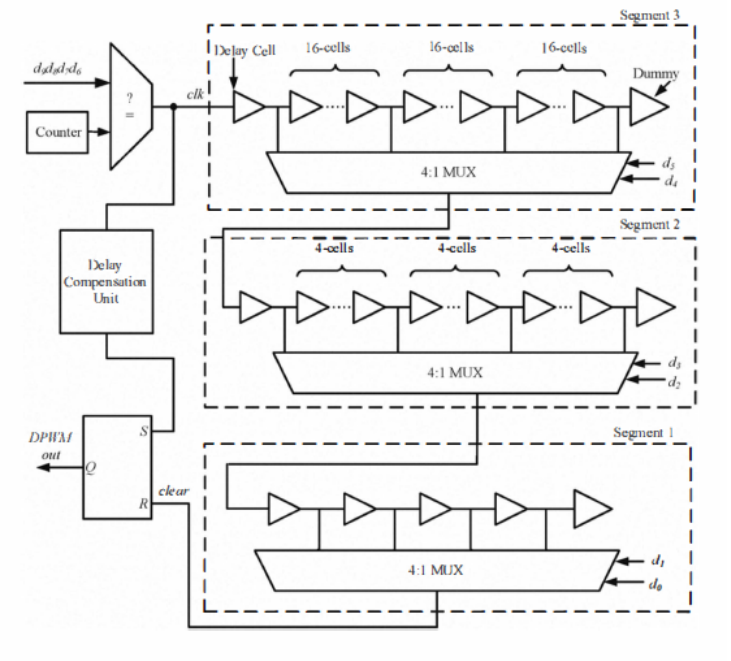

Figure 3.2.4: Self-oscillating segmented DPWM architecture [25]

identical, turnable delay-elements instead of replicating Δt_0. The control voltage of each segment, V_{cntrl} is adjusted to meet (3.2.1) using a delay-locked loop (DLL), as shown in Figure 3.2.3 for an 8-bit DPWM, where the embedded DLL is used to linearize a segmented DPWM. Using this self-calibrated architecture, each segment is identical and differs only in its V_{cntrl}. Each segment's DLL calibrates the delay-cells to be four times longer than the previous segment. While this approach can achieve very good linearity with a minimum number of delay-cells ($2N$ instead of 2^N), the four DLLs consume a large area. The same work [24] then proposes a compromise between the architectures of Figure 3.2.1 and Figure 3.2.3 with single DLL DPWM architecture.

A self-oscillating segmented-hybrid DPWM is proposed in [25], and it is shown in Figure 3.2.4. The counter values are generated by the 4-bit MSBs (d[9: 6]) while the segmented delay-lines are controlled by the 6-bit LSBs (d[5:0]). There are three in total while each segment is controlled by two bits. The three delay-lines unit used are 1-unit, 4-unit and 16-unit delay-cells. The total delay of the delay-line is adjusted so that the total delay is equal to the clock reference which is provided as output from the counter.

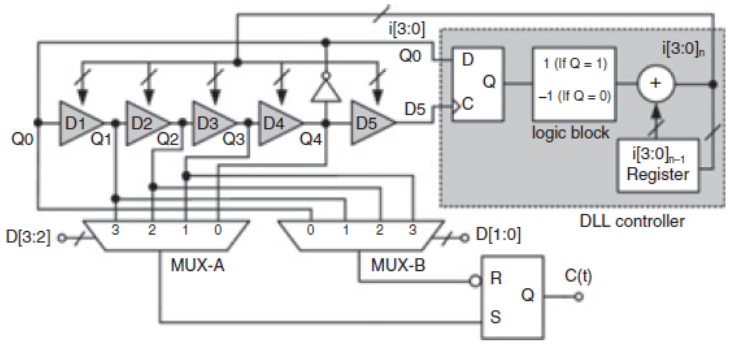

Figure 3.2.5: DPWM architecture based on delay-lines and ring oscillator [14]

In [14] is proposed a DPWM architecture based on delay-lines and ring oscillator, as in Figure 3.2.5 where an example of a 4-bit DPWM is shown. It consists of four digitally programmable delay-cells, D1 to D4, two 4:1 multiplexers and an S-R latch. The intermediate nodes between delay-cells, Q0 to Q3, are connected to the inputs of the multiplexer MUX-B in sequence, while the inputs of the multiplexer MUX-A are connected to the nodes, Q1 to Q4, in reverse order. For coarse resolution of the DPWM, the output of MUX-A is selected by the 2 MSBs of input digital command D. For fine resolution, MUX-B is controlled by the 2 LSBs of D.

The outputs of MUX-A and MUX-B are respectively connected to the set and reset ports of the S-R latch. The S port detects the rising edge of MUX-A output signal and sets the S-R latch. The R port senses the falling edge of the MUX-B output signal and resets the S-R latch. In the architecture in Figure 3.2.5, the 2 MSBs of D select the rising edges of propagated signals, Q1 to Q4, and start the output pulse signal. The falling edges of propagated signals, Q0 to Q3, are selected by the 2 LSBs of D to define the end point of output pulse. The falling delays are four times faster than the rising edge delays. With this architecture, a 4-bit resolution of the PWM signal is achieved with the hardware cost of 2-bit. Since the delay-lines are the main rate of area occupation and power dissipation, the decreasing number of delay-elements required means a considerable power and area saving. However, the delay of delay-cells varies with PVT variations, and to maintain the monotonicity and linearity, programmable delay-cells and a delay synchronization scheme

are required to minimize the non linearity, and a delay-locked-loop (DLL) is presented as illustrated in Figure 3.2.5.

3.3 Hybrid DPWM

The hybrid DPWM architectures provide sensible advantages over both the counter and the delay-line approaches. Hybrid DPWM are introduced to provide high resolution, high frequency DPWM without the need for a very high input clock frequency (as in counter based DPWM), or a very large area as in pure delay-line based DPWM. In the hybrid DPWM, a coarse resolution is obtained using a counter circuit, while fine resolution is gained with the help of a delay-mux architecture. In the approach proposed in [1], an n-bit resolution is achieved using an n_c-bit counter, where $n_c ln$, and the remaining n_d-bits of resolution are obtained from a tapped delay-line, where $n_d = n - n_c$.

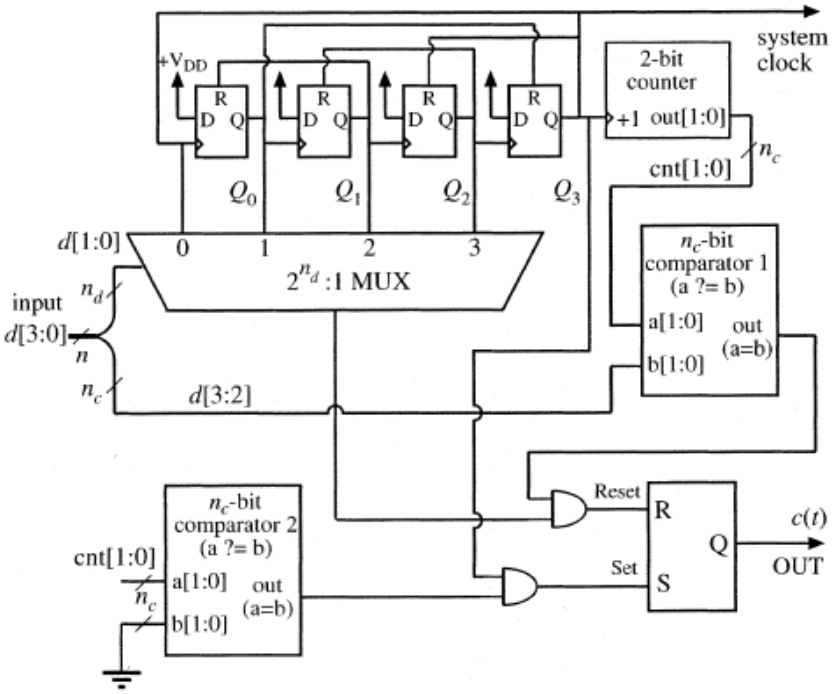

Figure 3.3.1: Simplified diagram of the 4-b hybrid DPWM [1]

A simplified diagram of the hybrid DPWM in [1] is shown in Figure 3.3.1, while in Figure 3.3.2 its operating waveforms are shown. In this case a 4-bit resolution ($n = 4$) is obtained using a 2-bit counter ($n_c = 2$) and a four-cell ring oscillator ($n_d = 2, 2^{n_d} = 4$), in which the delay-cells consists of resettable

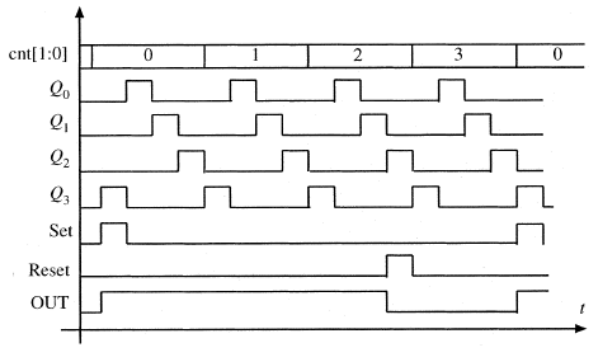

Figure 3.3.2: Operating waveforms of the 4-bit hybrid DPWM [1]

flip-flops. When a switching cycle begins, the output of the SR flip-flop is set, setting to high the DPWM output pulse $c(t)$. The pulse that propagates through the ring at the frequency $2^{n_c} f_s = 4 f_s$ serves as the clock for the counter. The entire switching period is divided into $2^{n_d} \cdot 2^{n_c} = 16$ slots. When the top n_c most significant bits of the digital input d are matched by the counter output, and the tap selected by the n_d least significant bits of d is reached by a pulse, the output flip-flop is reset and the output pulse goes low. To adjust the switching frequency, determined by the number of cells and the cell delay in the ring of Figure 3.3.1, additional elements between flip-flop output and the following delay-cell can be inserted. The additional delay-elements can be standard logic gates, or gates with adjustable delay, if switching frequency tuning or synchronization with an external clock are desired.

In [26] is proposed a hybrid DPWM that uses a phase interpolator (PI) for the fine duty-cycle adjustment instead of the delay-line. The phase interpolator takes two input clocks with different phases and produces a clock with a new phase in-between via interpolation. In Figure 3.3.3 is shown the architecture, consisting in a low-power relaxation oscillator, a programmable digital counter, digital phase interpolators, and a final SR-latch. It is a self-oscillating topology, with the clock generated by a relaxation oscillator. Two clock signals PI_{ROUT} and PI_{SOUT} are generated by the digital counter and phase interpolator stages together, and respectively resets and sets the output clock via the SR-latch. Therefore the duration of the duty cycle of the output clock is determined by the delay between PI_{ROUT} and PI_{SOUT}. First, the digital counter produces $PI_{RIN}[1:0]$ and $PI_{SIN}[1:0]$ according to the coarse control input code $D_{duty_c}[4:0]$, and sets the delay coarsely. The delay spacing between the

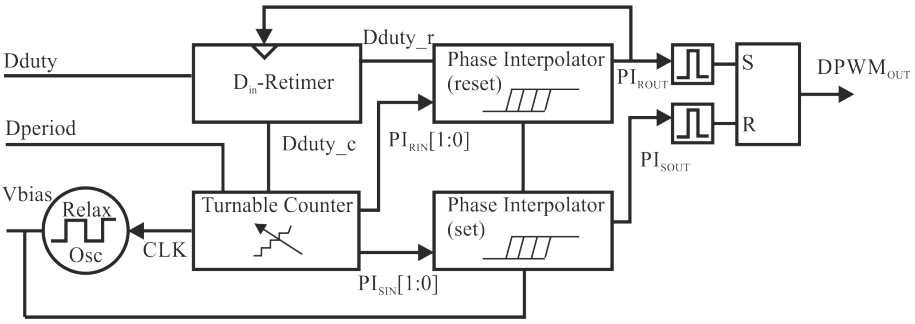

Figure 3.3.3: Architecture of the phase-interpolating hybrid DPWM [26]

two clocks of each counter output, for example $PI_{RIN}[0]$ and $PI_{RIN}[1]$, is equal to one oscillator clock period. To produce a finer resolution, this delay is then interpolated according to $D_{duty_r}[5:0]$ by the phase interpolator stages to generate the PI_{ROUT} and PI_{SOUT} timings. In addition, to uniformly maintain the duty cycle linearity of the DPWM, the operating frequency of the relaxation oscillator and phase interpolators is controlled by one V_{bias} input, that makes phase interpolators operate normally regardless of oscillation frequency change by PVT variation. The drawback of this architecture is that the time resolution isn't the same for all the output frequency range, but it drastically reduces at low frequencies. In addition, it isn't capable to produce frequency spreading on the generated output waveform.

3.4 References

[1] B.J. Patella et al. “High-frequency digital PWM controller IC for DC-DC converters.” In: *Power Electronics, IEEE Transactions on* 18.1 (2003), pp. 438–446.

[2] A.V. Peterchev, J. Xiao, and S.R. Sanders. “Architecture and IC implementation of a digital VRM controller.” In: *Power Electronics, IEEE Transactions on* 18.1 (2003), pp. 356–364.

[3] V. Yousefzadeh and D. Maksimovic. “Sensorless optimization of dead times in DC-DC converters with synchronous rectifiers.” In: *Power Electronics, IEEE Transactions on* 21.4 (2006), pp. 994–1002.

[4] V. Yousefzadeh et al. “A digitally controlled DC-DC converter for an RF power amplifier.” In: *Power Electronics, IEEE Transactions on* 21.1 (2006), pp. 164–172.

[5] Man Pun Chan and P.K.T. Mok. “Design and Implementation of Fully Integrated Digitally Controlled Current-Mode Buck Converter.” In: *Circuits and Systems I: Regular Papers, IEEE Transactions on* 58.8 (2011), pp. 1980–1991.

[6] S. Moon, L. Corradini, and D. Maksimovic. “Auto-tuning of digitally controlled boost Power Factor Correction rectifiers operating in continuous conduction mode.” In: *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on*. 2010, pp. 1–8.

[7] Zhonghan Shen, Na Yan, and Hao Min. “A Multimode Digitally Controlled Boost Converter With PID Autotuning and Constant Frequency/Constant Off-Time Hybrid PWM Control.” In: *Power Electronics, IEEE Transactions on* 26.9 (2011), pp. 2588–2598.

[8] A.V. Peterchev and S.R. Sanders. “Quantization resolution and limit cycling in digitally controlled PWM converters.” In: *Power Electronics, IEEE Transactions on* 18.1 (2003), pp. 301–308.

[9] Hao Peng et al. “Modeling of Quantization Effects in Digitally Controlled DC-DC Converters.” In: *Power Electronics, IEEE Transactions on* 22.1 (2007), pp. 208–215.

[10] A. Syed et al. “Digital pulse width modulator architectures.” In: *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*. Vol. 6. 2004, 4689–4695 Vol.6.

[11] Gu-Yeon Wei and M. Horowitz. “A low power switching power supply for self-clocked systems.” In: *Low Power Electronics and Design, 1996., International Symposium on*. 1996, pp. 313–317.

[12] Gu-Yeon Wei and M. Horowitz. “A fully digital, energy-efficient, adaptive power-supply regulator.” In: *Solid-State Circuits, IEEE Journal of* 34.4 (1999), pp. 520–528.

[13] A.P. Dancy and A.P. Chandrakasan. “Ultra low power control circuits for PWM converters.” In: *Power Electronics Specialists Conference, 1997. PESC ’97 Record., 28th Annual IEEE*. Vol. 1. 1997, 21–27 vol.1.

[14] W.W. Wang et al. “Improved delay-line based digital PWM for DC-DC converters.” In: *Electronics Letters* 47.9 (2011), pp. 562–564.

[15] A.P. Dancy, R. Amirtharajah, and A.P. Chandrakasan. “High-efficiency multiple-output DC-DC conversion for low-voltage systems.” In: *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* 8.3 (2000), pp. 252–263.

[16] R. Foley et al. “Multiphase digital pulsewidth modulator.” In: *Power Electronics, IEEE Transactions on* 21.3 (2006), pp. 842–846.

[17] E. Orietti et al. “Electromagnetic Susceptibility Analysis on a Digital Pulse Width Modulator for SMPSs.” In: *Electromagnetic Compatibility, IEEE Transactions on* 51.4 (2009), pp. 1034–1043.

[18] M. Barai, S. SenGupta, and J. Biswas. “Digital Controller for DVS-Enabled DC -DC Converter.” In: *Power Electronics, IEEE Transactions on* 25.3 (2010), pp. 557–573.

[19] V. Yousefzadeh, T. Takayama, and D. Maksimovic. “Hybrid DPWM with Digital Delay-Locked Loop.” In: *Computers in Power Electronics, 2006. COMPEL ’06. IEEE Workshops on*. 2006, pp. 142–148.

[20] Hsin Chuan Chen. “Design of a Counter-Based DPWM Using RC Charge.” In: *Computer, Consumer and Control (IS3C), 2014 International Symposium on*. 2014, pp. 1267–1270.

[21] Jin-Whi Jung and M.J. Hawksford. “An oversampled digital PWM linearization technique for digital-to-analog conversion.” In: *Circuits and Systems I: Regular Papers, IEEE Transactions on* 51.9 (2004), pp. 1781–1789.

[22] A. Syed, E. Ahmed, and D. Maksimovic. “Digital PWM controller with feed-forward compensation.” In: *Applied Power Electronics Conference and Exposition, 2004. APEC ’04. Nineteenth Annual IEEE*. Vol. 1. 2004, 60–66 Vol.1.

[23] M.G. Batarseh et al. “Window-Masked Segmented Digital Clock Manager-FPGA-Based Digital Pulsewidth Modulator Technique.” In: *Power Electronics, IEEE Transactions on* 24.11 (2009), pp. 2649–2660.

[24] O. Trescases, Guowen Wei, and Wai Tung Ng. “A Segmented Digital Pulse Width Modulator with Self-Calibration for Low-Power SMPS.” In: *Electron Devices and Solid-State Circuits, 2005 IEEE Conference on*. 2005, pp. 367–370.

[25] Ahui Sun, Meng Tong Tan, and L. Siek. “Segmented Hybrid DPWM and tunable PID controller for digital DC-DC converters.” In: *Next-Generation Electronics (ISNE), 2010 International Symposium on*. 2010, pp. 154–157.

[26] Y. Lee, T. Kang, and J. Kim. “A 9-11 bits Phase-Interpolating Digital Pulse-Width Modulator with 1000X Frequency Range.” In: *Industry Applications, IEEE Transactions on* PP.99 (2015), pp. 1–1.

All-Digital DPWM Supporting Multiple Outputs and Spread Spectrum Capability in 130nm CMOS

In the following chapter the proposed all-digital Pulsed-Width Modulator (DPWM) is presented. It exploits an all-digital architecture, without the need of loops to perform frequency synthesis and spreading, avoiding the limitations of analog circuits in implementing frequency discontinuous modulation profiles. The design is based on standard-cells, thus simplifying the porting in new technologies when the technology scales down in dimensions.

The top-level diagram of the developed DPWM is shown in Figure 4.0.1. The proposed DPWM works with an input clock signal CLK having a constant period $T_{CLK} = 1/f_{CLK}$ and a 50% duty-cycle, and the reference clock frequency is assumed $f_{CLK} = 10$MHz. The architecture proposed is based on digitally-controlled delay-lines, dimensioned on the period of an internal Digitally Controlled Oscillator (DCO) and not on the period of the reference clock T_{CLK}. This allows to reduce the dimension of the delay-line maintaining an high resolution. The circuit generates four output pulsed-width modulated square-wave signals, with a programmable duty-cycle value. The output Q_N is generated imposing the desired output period and duty-cycle. The output Q_P is a replica of Q_N, but with a programmable guard time $\Delta\tau_G$ on both edges, as shown in Figure 4.0.2. The guard time programmability of the DPWM provides the opportunity to achieve optimum efficiency in a DC-DC converter including synchronous rectifier. The other two outputs, nQ_N and nQ_P, are respectively the complementary of the outputs Q_N and Q_P. The output signals are produced using the four digitally-controlled delay-lines (DCDL), named

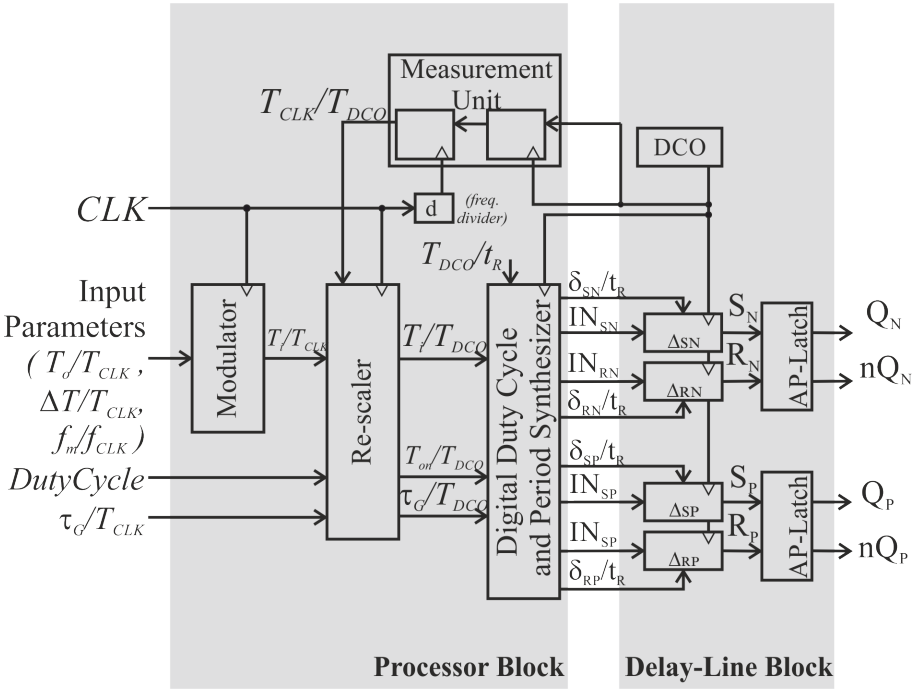

Figure 4.0.1: The proposed DPWM architecture

Δ_{SN} and Δ_{RN} for the outputs Q_N and nQ_N, and Δ_{SP} and Δ_{RP} for the outputs Q_P and nQ_P, digitally controlled by the *Modulator*.

Each delay-line is in charge of generating an output clock edge within a DCO period. The input signals are normalized to the reference clock period T_{CLK}. Those signals, after being processed by the *Modulator*, are normalized to the DCO period T_{DCO} to be processed by the *Duty-Cycle and Period Synthesizer (DCPS)*. The normalization is made employing the output of the *Measurement Unit* T_{CLK}/T_{DCO}. The *Measurement Unit* is included to compensate process, voltage and temperature (PVT) variations, and is realized using a counter and all single-edge triggered flip-flops. The ratio T_{CLK}/T_{DCO} is obtained by counting the number of both rising and falling edges of the DCO within a time window multiple of the reference clock period T_{DCO}. The *DCPS* is able to position output clock edges anywhere within a DCO period, and generates the inputs (IN_{xx}) and the control words (δ_{xx}/T_{DCO}) of the four DCDL. Before entering as an input in the DCDLs, the control words are normalized to the DCDL resolution t_R by the constant ratio T_{DCO}/t_R. The output signals

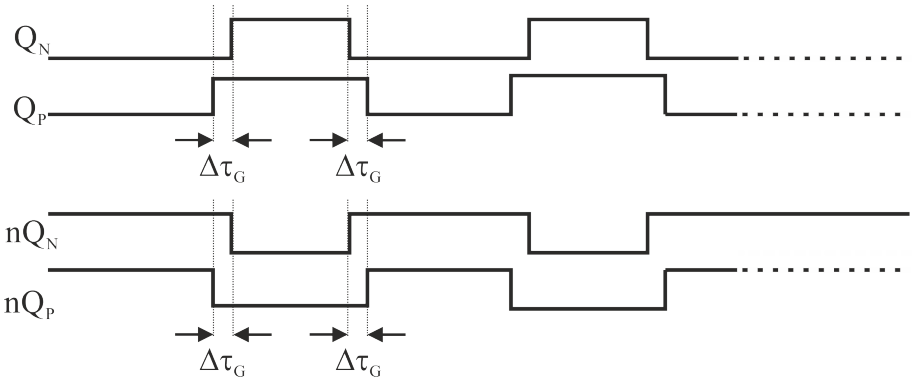

Figure 4.0.2: Outputs and $\Delta\tau_G$ guard time meaning

are generated through two *Auto-Pulsed SR Latch (AP-SR Latch)*. These *AP-SR Latches* have been employed to automatically return in the hold state after a set or reset event, thus avoiding the forbidden state. The developed all-digital DPWM has been implemented by using only standard cells.

A Full-Custom layout has been realized for the Delay-Line Block, including the DCO and the Latches, in order to mitigate the asymmetries components and improve the linearity, while an automatic place & route design is used to design the Processor Block. This chapter is organized as follows. The circuit implementation details are given in § 4.1 4.2 4.3 4.4, while in § 4.5 the circuit sizing is discussed. Finally, § 4.6 reports the test-chip experimental measurement results.

4.1 Modulator Block

The Modulator block determines the shape of the modulation, the modulation depth and the modulation frequency by computing the instantaneous output signal period T_i normalized to the input clock period T_{CLK}.

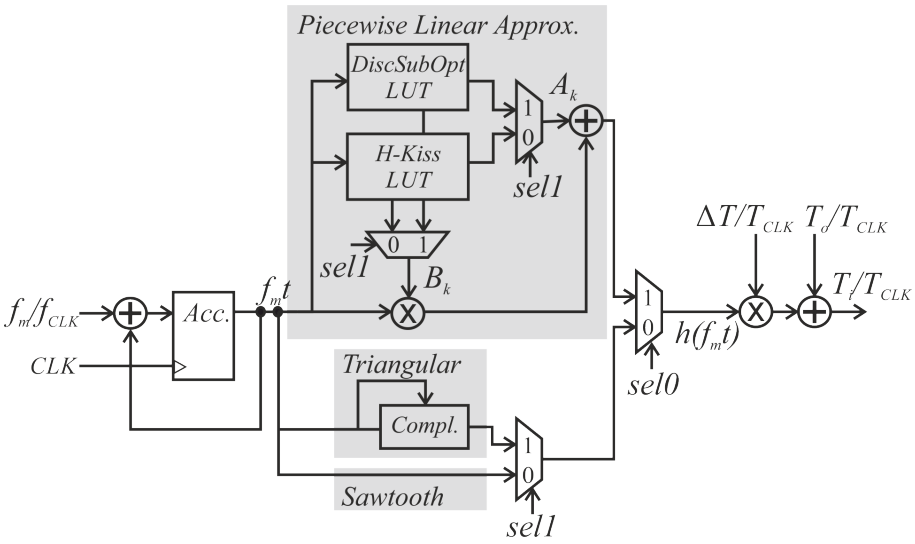

Figure 4.1.1: Modulator Block

The circuit is synchronized by the input clock CLK and includes only positive edge flip-flops. The instantaneous output signal period T_i is computed by adding the desired output period T_0 to the instantaneous period deviation ΔT_i, that can be obtained as:

$$\Delta T_i(t) = h(f_m t) \cdot \Delta T \tag{4.1.1}$$

where ΔT is the maximum period deviation, $h(f_m t)$ is the modulation profile function, whose value $\in [0, 1)$, and f_m is the modulation frequency. In Figure 4.1.2 the definition of modulation parameters ΔT and f_m is explained.

As shown in Figure 4.1.1, an accumulator generates the phase signal $f_m t \in [0, 1)$ by counting the elapsed time normalized to the modulation period $1/f_m$. This signal feeds the blocks which generates the four different modulation profiles. Sawtooth and Triangular profiles are realized respectively directly using the phase signal, or with a 1's complementer at the output of the

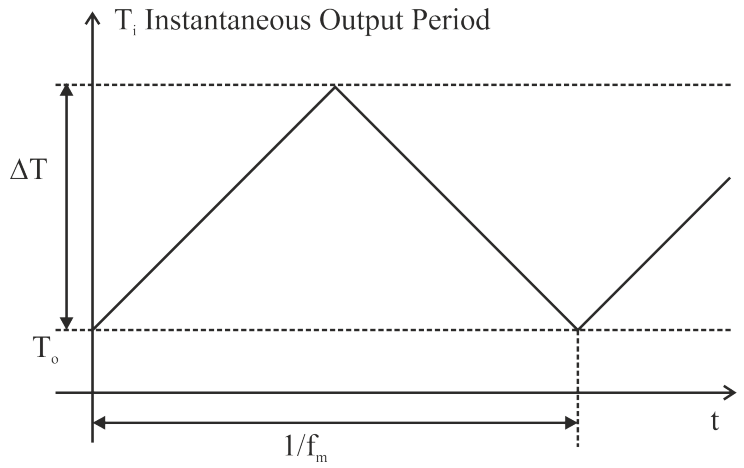

Figure 4.1.2: Modulation parameters for a downspreading modulation (Triangular shape)

accumulator. Hershey Kiss and SubOptimal Discontinuous modulation are implemented by using a piecewise approximation. The argument $x = f_m t$ belongs to the interval $[0, 1)$. This interval is subdivided in 64 segments, and in each segment the waveform is approximated with a straight line, as follows:

$$h(x - x_k) \simeq A_k + B_k(x - x_k) \tag{4.1.2}$$

The coefficients A_k and B_k are obtained from a best-fit of the required modulation profile and are stored in a look up table realized hard wired, that is, with the use of boolean functions and interconnections embedded into the circuit, without the need of an SRAM and therefore with a considerable saving of area.

The desired modulation profile can be chosen by using $sel0$ and $sel1$ signal. The output of the multiplexer, the modulation profile function $h(f_m t)$, is finally multiplied by the maximum period deviation ΔT and added to the desired output period T_o to obtain the instantaneous output period T_i. Please note that both ΔT and T_o are normalized to the input clock period T_{CLK}, and therefore the instantaneous output period itself will be normalized to T_{CLK}:

$$\frac{T_i(t)}{T_{CLK}} = h(f_m t)\frac{\Delta T}{T_{CLK}} + \frac{T_o}{T_{CLK}} \tag{4.1.3}$$

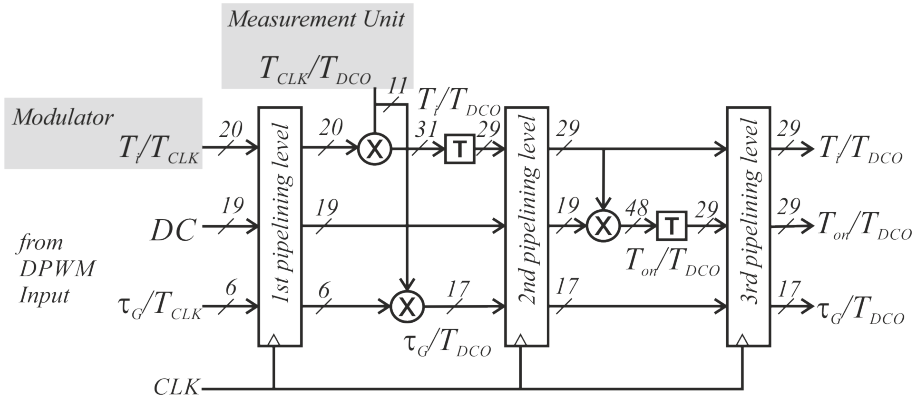

Figure 4.1.3: Rescaling at the end of the Modulator block

Generally a frequency modulation instead of the period modulation 4.1.3 is required. The instantaneous frequency of the output waveform, for an ideal down-spreading modulation, is:

$$f_i(t) = f_o - \Delta f \cdot h(f_m t) \tag{4.1.4}$$

and the ideal instantaneous period is given by;

$$T_i(t) = \frac{1}{f_i(t)} = \frac{1}{f_o} \frac{1}{1 - \frac{\Delta f}{f_o} h(f_m t)} \tag{4.1.5}$$

By expanding (4.1.5) in Taylor series we have:

$$\begin{aligned} &T_i(t) = \tfrac{1}{f_i(t)} = \\ &= \tfrac{1}{f_o} \left[1 + \tfrac{\Delta f}{f_o} h(f_m t) - \left(\tfrac{\Delta f}{f_o} h(f_m t) \right)^2 + \dots \right] \end{aligned} \tag{4.1.6}$$

Comparing (4.1.6) and (4.1.3) we have that, for $\Delta f / f_o$, the period modulation (4.1.3) approximates the ideal frequency modulation (4.1.4), with:

$$f_o = \frac{1}{T_o}; \quad \frac{\Delta f}{f_o} = \frac{\Delta T}{T_o} \tag{4.1.7}$$

In a practical DPWM application the value of $\Delta f / f_o$ is a few percent,

Signal	MSB	LSB	maximum	minimum	resolution
$\frac{T_o}{T_{CLK}}$	2^7	2^{-12}	$T_o \leqslant 256 T_{CLK}$	$T_o \geqslant T_{CLK}$	$2^{-12} \cdot T_{CLK}$
$\frac{\Delta T}{T_{CLK}}$	2^6	2^{-5}	$\frac{\Delta T}{T_o} \leqslant 12800 \frac{T_{CLK}}{T_o}\%$	$\frac{\Delta T}{T_o} \geqslant 0\%$	$3.12 \frac{T_{CLK}}{T_o}\%$
$\frac{f_m}{f_{CLK}}$	2^{-9}	2^{-24}	$f_m \leqslant 40 \cdot 10^{-4} f_{CLK}$	$f_m \geqslant 0$	$5.96 \cdot 10^{-8} f_{CLK}$

Table 4.1.1: Meaning and range of Modulator input signals

and after several system-level simulations, by varying modulation depth, frequency and profile and we found that for $\Delta f / f_o \leq 0.1$ the use of (4.1.3) in place of (4.1.4) does not appreciably modify the spectrum of the output waveform.

The Table 4.1.1 reports the exact meaning of the Modulator block inputs. With a reference clock of $f_{CLK} = 10$MHz, the output frequency T_o could go from 10MHz downto 40kHz, the maximum relative modulation depth $\Delta T / T_o$ is 50 $\%$ in the worst case ($T_o = 256 T_{CLK}$) and the maximum modulation frequency is 40kHz with a resolution of 0.6Hz.

At the end of the Modulator block, the instantaneous output signal period T_i is normalized to the DCO period T_{DCO} by multiplying the output of the Modulator block $T_i(t)/T_{CLK}$ to the output of the Measurement Unit T_{CLK}/T_{DCO}, as shown in Figure 4.1.3. Then the instantaneous output signal on-time is calculated multiplying $T_i(t)/T_{DCO}$ to the input duty-cycle signal DC, whose maximum value is 1, obtaining $T_{on}(t)/T_{DCO}$. Finally, even the guard time τ_G / T_{CLK} is normalized to the period of the DCO.

The Table 4.1.2 reports the exact meaning of the inputs. The duty-cycle DC is given as a fraction of the output desired on-time output period , so its MSB is equal to 2^{-1} and its maximum value is 1. The resolution has been

Signal	MSB	LSB	maximum	minimum	resolution
DC	2^{-1}	2^{-19}	$T_{on} < 100 T_o\%$	$T_{on} > 0\%$	$1.9 \cdot 10^6 T_o$
$\frac{\tau_G}{T_{CLK}}$	2^{-4}	2^{-9}	$\tau_G \leq 12.4 T_{CLK}$	$\tau_G \geq 0$	$1.95 \cdot 10^{-3} T_{CLK}$

Table 4.1.2: Meaning and range of DPWM input signals

chosen 2^{-19} in order to match resolution of the delay-lines even when the output signal period is the maximum available. The guard time, considering a reference clock of $f_{CLK} = 10$MHz, has a resolution of about 200ps and a maximum value of 12.4ns.

4.2 Measurement Unit

As introduced in § 4 and subsequently explained in § 4.1, the Modulator block determines the instantaneous output period $T_i(t)$ normalized to the input clock period T_{CLK}. Before entering the DCPS, $T_i(t)$ is normalized to the DCO period T_{DCO} by multiplying $T_i(t)/T_{CLK}$ to T_{CLK}/T_{DCO}.

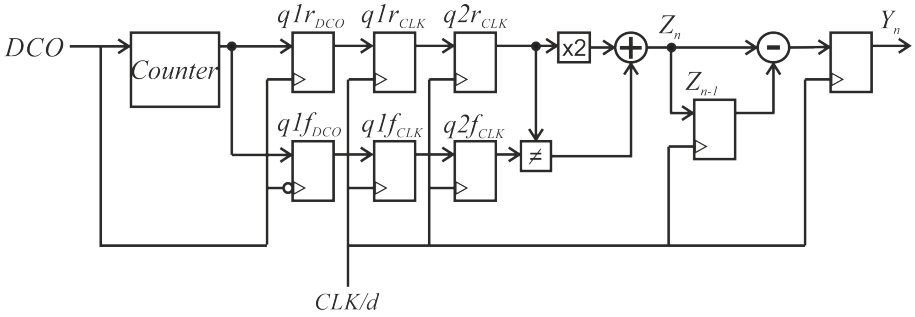

Figure 4.2.1: Measurement Unit

The value of T_{DCO} is strictly related to the delay-lines resolution t_R, because as explained in § 4.4.4 the ratio T_{DCO}/t_R is a constant value. To compensate the variations of t_R with the PVT operating condition of the circuit, the Measurement Unit constantly tracks the value of T_{CLK}/T_{DCO}, by counting the number of DCO clock edges (both rising and falling) in a time window equal to a multiple of the clock period $d \cdot T_{CLK}$, as shown in Figure 4.2.2 where d is an input parameter whose values can be selected between 2, 4, 8 and 16.

In Figure 4.2.1 is shown the circuital scheme of the Measurement Unit. As it can be easily seen, to count both rising and falling edges of the DCO clock no dual-edge triggered flip-flop has been employed, thus reducing the circuit complexity.

The output of the Modulation Block is :

$$Y_n = \frac{d \cdot T_{CLK}}{\frac{T_{DCO}}{2}} \pm \varepsilon_Y \tag{4.2.1}$$

where ε_Y is a quantization error, and it is between -1 and 1. Therefore, the ratio T_{CLK}/T_{DCO} can be computed as:

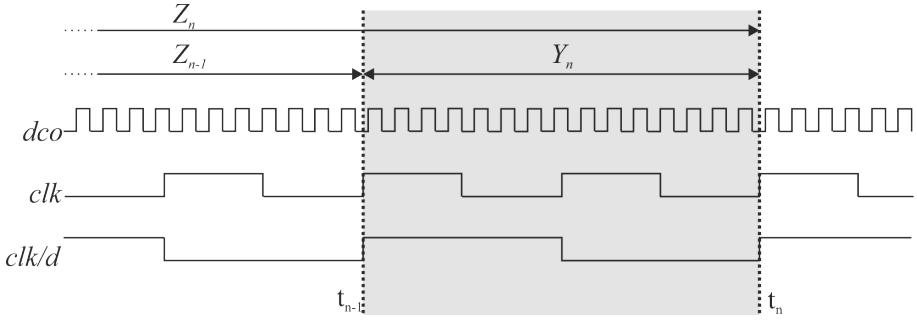

Figure 4.2.2: Example of operation of the Measurement Unit

$$\frac{T_{CLK}}{T_{DCO}} = \frac{Y_n}{2d} \pm \frac{\varepsilon_Y}{2d} \tag{4.2.2}$$

where the measurement error on T_{CLK}/T_{DCO} is:

$$\varepsilon_{T_{CLK}/T_{DCO}} = \frac{\varepsilon_Y}{2d} \tag{4.2.3}$$

By choosing $d = 16$, we can evaluate the maximum error on T_{CLK}/T_{DCO} as:

$$\varepsilon_{T_{CLK}/T_{DCO}} \leq 0.03125 \tag{4.2.4}$$

Please note that the maximum value of the error $\varepsilon_{T_{CLK}/T_{DCO}}$ does not depend neither on T_{CLK} nor on T_{DCO}, and therefore does not vary with the PVT operating conditions of the circuit.

By expanding equation (4.2.3) in Taylor series and truncating at the first order it is possible to evaluate the error on the measured T_{DCO}:

$$\varepsilon_{T_{DCO}/T_{CLK}} = \left(\frac{T_{DCO}}{T_{CLK}}\right)^2 \varepsilon_{T_{CLK}/T_{DCO}} \tag{4.2.5}$$

and therefore:

$$\varepsilon_{T_{DCO}} = \frac{T_{DCO}^2}{T_{CLK}} \varepsilon_{T_{CLK}/T_{DCO}} \tag{4.2.6}$$

Considering the slow corner in which $f_{DCO} = 250$MHz, and a reference clock frequency of $f_{CLK} = 10$MHz, and setting $d = 16$, taking in account equation (4.2.4), we can evaluate $\varepsilon_{T_{DCO}}$

$$\varepsilon_{T_{DCO}} < 5ps \tag{4.2.7}$$

The total measurement time results equal to:

$$T_{meas} = d \cdot T_{CLK} \tag{4.2.8}$$

Parameter	Value	Annotations	
MSB of $\frac{T_{CLK}}{T_{DCO}}$	2^5		
LSB of $\frac{T_{CLK}}{T_{DCO}}$	2^{-5}		
		$\varepsilon_{T_{CLK}/T_{DCO}}$	T_{meas}
d	2	0.25	$2{\cdot}T_{CLK}$
	4	0.125	$4{\cdot}T_{CLK}$
	8	0.0625	$8{\cdot}T_{CLK}$
	16	0.03125	$16{\cdot}T_{CLK}$

Table 4.2.1: Measurement Circuit parameter and performances

The Table 4.2.1 summarizes the meaning and sizing of the parameters of the Measurement Unit. The MSB have been chosen considering the fast corner, in which $f_{DCO} = 625$MHz. In that case, with $f_{CLK} = 10$MHz, the ratio T_{CLK}/T_{DCO} is equal to 62.5, thus the MSB has been chosen equal to 2^5. The LSB is related to the resolution. With reference to the equation (4.2.2), considering that Yn is integer, and the maximum value of d is 16, the LSB must be chosen equal to 2^{-5}. As it can be easily seen, parameter d gives a trade-off between measurement time and accuracy.

4.3 Duty-Cycle and Period Synthesizer

The Duty-Cycle and Period Synthesizer (DCPS) generates the input signals for the four delay-lines Δ_{SN}, Δ_{RN}, Δ_{SP}, Δ_{RN}, as shown in Figure 4.0.1. The behavior of the DCPS can be explained as follows, assuming that the DCPS is triggered on the DCO rising edge. For simplicity, let us consider only the generation of Q_N (nQ_N is the complementary) outputs, as the generation of the other two outputs Q_P and nQ_P is similar. The signal $\Delta t_i(k)$ is the time difference between the next DCO rising edge and the subsequent rising edge of the output waveform Q_N at the k-th clock cycle, while $\Delta t_{on}(k)$ is the time difference between the next DCO rising edge and the subsequent falling edge of the output waveform Q_N at the k-th clock cycle, both signals are normalized to T_{DCO}.

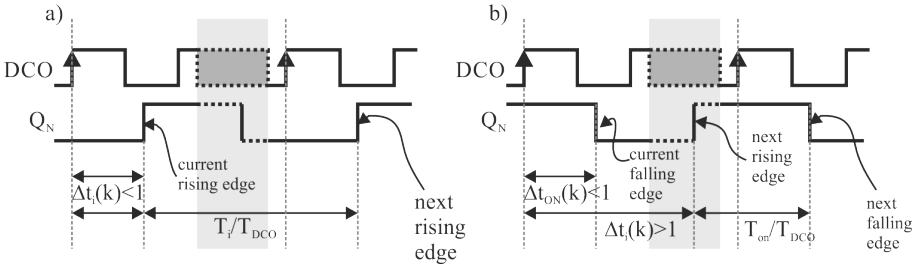

Figure 4.3.1: DCPS signals meaning and timing, only one edge generated in a DCO period

When $\Delta t_i(k)$ and $\Delta t_{on}(k)$ are > 1, no edge is generated for the output waveform within the k+1-th clock period, thus, the signals IN_{SN} and IN_{RN}, feeding the two DCDLs Δ_{SN} and Δ_{RN}, are not switched. The signals $\Delta t_i(k)$ and $\Delta t_{on}(k)$ will be reduced by 1 at the next clock tick (it means that the time interval between DCO rising edge and output waveform edges will be reduced by T_{DCO} at the next clock tick) and therefore $\Delta t_i(k+1) = \Delta t_i(k) - 1$ and $\Delta t_{on}(k+1) = \Delta t_{on}(k) - 1$.

Figure 4.3.1(a) shows what happens when only a rising edge of the output waveform is generated in the k+1-th DCO clock cycle. In this case, $\Delta t_i(k) < 1$ and $\Delta t_{on}(k) > 1$, the signal IN_{SN} is set to high, and the control word of the DCDL δ_{SN}/T_{CLK} is set to $\Delta t_i(k)$. Finally the signals are updated, with $\Delta t_i(k+1) = \Delta t_i(k) + T_i/T_{DCO}$ while $\Delta t_{on}(k+1)$ is decreased by 1 as in the previous case.

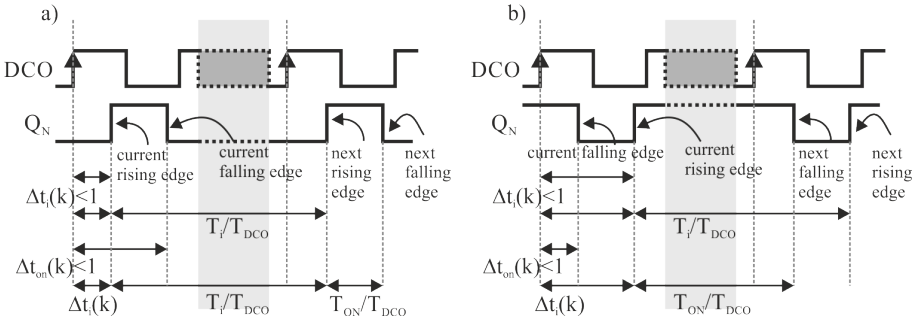

Figure 4.3.2: DCPS signals meaning and timing, both edges generated in a DCO period

The analogue case is when only a falling edge of the output waveform is generated in the k+1-th DCO clock cycle, and it's shown in Figure 4.3.1(b). This time $\Delta t_i(k) > 1$ and $\Delta t_{on}(k) < 1$, the signal IN_{RN} is set to high, and the control word of the DCDL δ_{RN}/T_{CLK} is set to $\Delta t_{on}(k)$. The signal $\Delta t_i(k+1)$ is updated as in the case when no edge is generated, while $\Delta t_{on}(k+1) = \Delta t_i(k) + T_{on}/T_{DCO}$.

Finally, in Figure 4.3.2 is shown the case when both output waveform edges are generated in the k+1-th DCO clock cycle. In this case both $\Delta t_i(k)$ and $\Delta t_{on}(k)$ are < 1, IN_{SN} and IN_{SN} are both set to high, and δ_{SN}/T_{CLK} is set to $\Delta t_i(k)$ while δ_{RN}/T_{CLK} is set to $\Delta t_{on}(k)$. The signal $\Delta t_i(k+1)$ is updated to $\Delta t_i(k) + T_i/T_{DCO}$, while $\Delta t_{on}(k+1)$ could be updated in two different ways, depending on whether $\Delta t_{on}(k)$ is greater or less than $\Delta t_i(k)$. if $\Delta t_{on}(k) > \Delta t_i(k)$ (case ((b)), then $\Delta t_{on}(k+1) = \Delta t_i(k) + T_{on}/T_{DCO}$.

4.4 Delay-Line Block

A fundamental element of the proposed digital pulsed width modulator is the design of the digitally controlled delay-line (DCDL) employed to generate the output modulated-pulse waveforms, as introduced at the beginning of this chapter. The design of the DCDL is a very important issue, since INL of these components translates in duty-cycle jitter. In literature, two main approaches are used to design a DCDL, and they are the MUX-DCDL [1–6] and the delay-elements DCDL (DE-DCDL) [7–11]. In MUX-DCDL approach, to select desired delay a chain of delay-cells and a multiplexer is employed. The main drawback of this topology is that the MUX delay (t_{min}) increases with the increase of the number of cells, resulting in a trade-off between delay-range and minimum delay. In [1], a tree-based multiplexer topology is employed to reduce the large t_{min} of MUX-DCDLs. This however results in an irregular layout that adds an additional severe trade-off between linearity and delay-range. DE-DCDLs are based on a regular cascade of equal delay-elements and include both a forward and a reverse propagation path. In this circuit, the multiplexer of the MUX-DCDL is conceptually spread among all cells, making t_{min} very low and independent of the number of cells. The structure of DE-DCDL is regular, providing an easy design at layout level, and a very good parasitics matching, achieving therefore a good linearity. The DE-DCDL proposed in [12] is based on a forward propagation path composed by a cascade of inverters, and a reverse path of 2-to-1 MUX. This solution, despite its simplicity, presents a very poor linearity due to the imbalances between the cells in forward and reverse path. another drawback of this solution is the large multiplexer delay which worsen the resolution. To overcome this issue and achieve a better linearity, an architecture of DE-DCDL using the same kind of cell in both forward and reverse path could be employed. The TINV topology in [13] for example uses a multiplexed composed by three-state inverters on in both forward and reverse path. The resolution obtained is $t_R = 2 \cdot t_{TINV}$. The NAND based DCDL [7, 8] also present the same gates on both paths, but those elements are composed by only two-inputs NAND gates, obtaining very good linearity and resolution. In this case $t_R = 2 \cdot t_{NAND}$. On the other hand, the NAND based DCDL proposed in [7, 8] may result in severe glitching problems, as shown in [14], where a solution to resolve the glitching problem is given. To avoid glitching problems, The NAND-based DCDL in [14] presents two different control bits for each delay-element. Since each control bits need to be driven by a different flip-flop, the architecture of [14] requires two flip-flops for each delay-element, resulting in a large area and power dissipation.

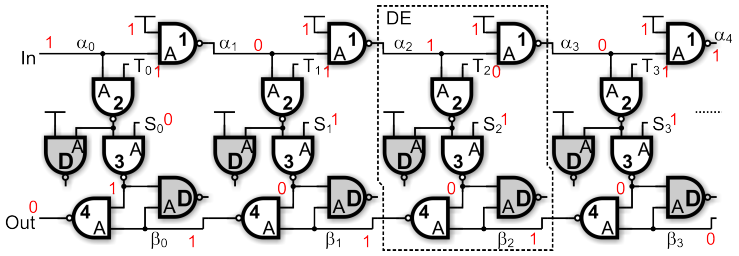

Figure 4.4.1: Digitally Controlled Delay-Line employed in the proposed DPWM

To overcome this issue, in [15] is proposed another glitch-free NAND based DCDL, requiring a single control bit for each delay-element. This architecture introduces an additional inner propagation loop between the delay-elements to eliminate glitching. Unfortunately, the propagation path of the inner loop can result in a very long settling time, by limiting the frequency at which the DCDL can be switched. The DCDL employed in the proposed DPWM uses the delay-element of [14] but changes the encoding of the control bits. In this way a novel driving-circuit, requiring a single flip-flop for each delay-element, can be employed.

4.4.1 NAND-based Digitally Controlloed Delay-Lines

The structure of proposed DCDL [12] is shown in Figure 4.4.1 and it is composed by a cascade of equal NAND based delay-elements (DE). In each DE four NAND gates are employed for the signal propagation, where A is the the fast input, and two dummy NAND gates, highlighted in gray, are employed to obtain the same load for all the NAND gates. Thanks to this architecture, if the DCDL layout is properly arranged, the monotonicity of the delay chain is guaranteed and also the linearity is very good. The delay of the DCDL is controlled by two sets of control bits, named S_i and T_i. Consider c as the control code of the DCDL, S_i bits encode c by using a thermometric code:

$$\begin{aligned} S_i &= 0 \quad \text{for} \quad i < c \\ S_i &= 1 \quad \text{for} \quad i \geq c \end{aligned} \tag{4.4.1}$$

and T_i bits encode c using a one cold code:

S_i	T_i	DE State
0	0	Pass
1	1	Turn
1	0	Post Turn

Table 4.4.1: Logic-States of each DE in proposed DCDL

$$\begin{aligned} T_i &= 0 \quad \text{for} \quad i < c \quad \text{and} \quad i = c+1 \\ T_c &= 1 \quad \text{in remaining cases} \end{aligned} \tag{4.4.2}$$

According to the chosen control bit encoding,, each DE can be in one of possible three states, as shown in Table 4.4.1.

Due to the fact that dummy cells are employed to provide the same load to every NAND gate in Figure 4.4.1, which therefore in a first order approximation present the same delay, we can write the delay δ from IN to OUT as:

$$\delta = 3t_{NAND} + 2t_{NAND} \cdot c = t_{min} + t_R \cdot c \tag{4.4.3}$$

where

$$t_{NAND} = \frac{t_{NAND,LH} + t_{NAND,HL}}{2} \tag{4.4.4}$$

while $t_{NAND,LH}$ and $t_{NAND,LH}$ represent the delay of each NAND gate for low-to-high and high-to-low output transition respectively. Equation 4.4.3 suggests that the resolution of each DE is $t_R = 2t_{NAND}$, while the minimum delay of the DCDL is $t_{min} = 3t_{NAND}$. The logic states of each DE are not independent each other, but the possible logic states of the i+1-th DE are given by the state of the i-th DE, as reported in Table 4.4.2

A common issue that affects system employing DCDL is glitching. As shown in [14] the NAND based DCDL proposed in [7, 8] may result in severe glitching problems that avoid the employ of these topologies in digitally-controlled oscillators (DCO) and in SSCG applications [6, 12]. A NAND based DCDL is glitch free when for every possible switching of the control bits doesn't produce a glitch event. To avoid glitching problems a precise time constraint is required in the switching of the control bits. In [12] two different control bits for each delay-element of the NAND based DCDL are introduced,

i-th DE state	Valid i+1-th DE state	Notes
Pass	Pass	Post-Turn after Pass
	Turn	is not possible
Turn	Turn	Pass after Turn
	Post-Turn	is not possible
Post-Turn	Turn	After Post-Turn only Turn is allowed

Table 4.4.2: Possible i+1-th DE logic states related to i-th DE logic states

and a driving-circuit that computes S_i and T_i with the correct time temporization is presented. Since a different flip-flop is required to drive each control bit, the architecture of [12] presents two flip-flops for each delay-element, as shown in Figure 4.4.2, resulting in a large area and power dissipation.

In order to reduce the number of flip flops in the driving-circuit, using the encoding shown in Table 4.4.1 and the constraints on logic states of two consecutive DE reported in Table 4.4.2, it can obtained that the value of S_i can be computed as:

$$S_i = T_i \; OR \; T_{i-1} \tag{4.4.5}$$

Deriving S_i control bit from T_i and T_{i-1} allows to employ a single flip-flop for the generation of both S_i and T_i control bits of the same i-th DE. According to (4.4.5), a possible driving-circuit is shown in Figure 4.4.3.

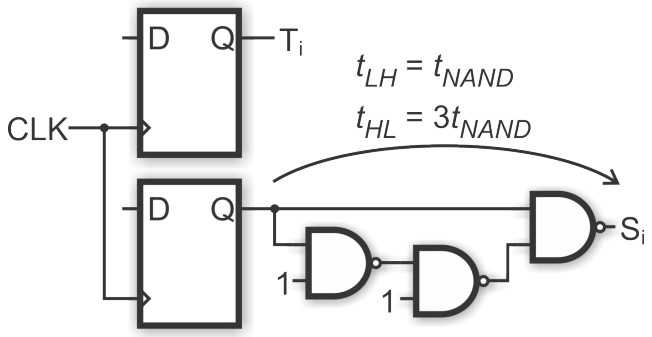

Figure 4.4.2: Double Flip-Flop DCDL Driving-Circuit

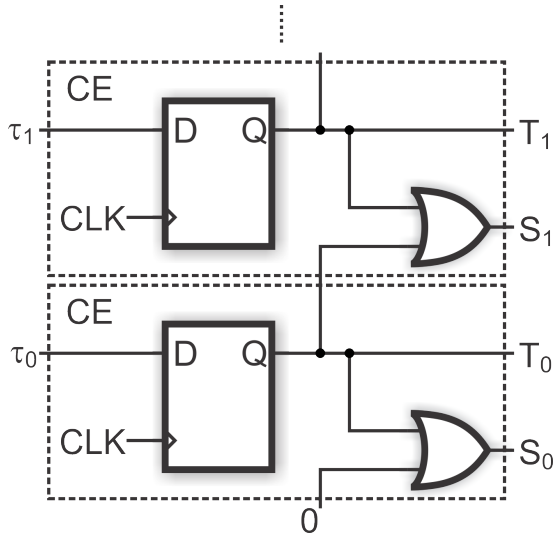

Figure 4.4.3: Single Flip-Flop DCDL Driving-Circuit Topology

4.4.2 Glitch-Free Driving-Circuit

Unfortunately, with the driving-circuit in Figure 4.4.3, glitch events occur. An exhaustive analytical analysis has been performed to find all the possible cases that have to be considered for glitching. In the following analysis, to generalize, the logic state of the input of the i-th DE is indicated as γ, because it can be either 0 or 1. The arrival time of A input and B input of the NAND gates are indicated as t_A and t_B respectively.

The first case is shown in Figure 4.4.4(a), where the i-th DE switches its logic state from pass to turn. A possible glitch can occur in NAND3, due to the fact that both inputs switch: A input switches from 0 to 1 due to the transition of S_i, while B input switches from 1 to $\bar{\gamma}$ due to the transition of T_i. The glitch occur if input A of NAND3 switches earlier than input B. This glitch consists in a transition $1 \rightarrow 0 \rightarrow \bar{\gamma}$ and propagates to input A of NAND4. With reference to Figure 4.4.4(a), $t_A = t_{S_i,LH}$, and $t_b = t_{T_i,LH} + t_{NAND}$. The first constraint to impose to avoid glitching is $t_B - t_A < t_{NAND}$, that therefore results:

$$t_{T_i,LH} < t_{S_i,LH} \tag{4.4.6}$$

The second case is shown in Figure 4.4.4(b), where the i-th DE switches its

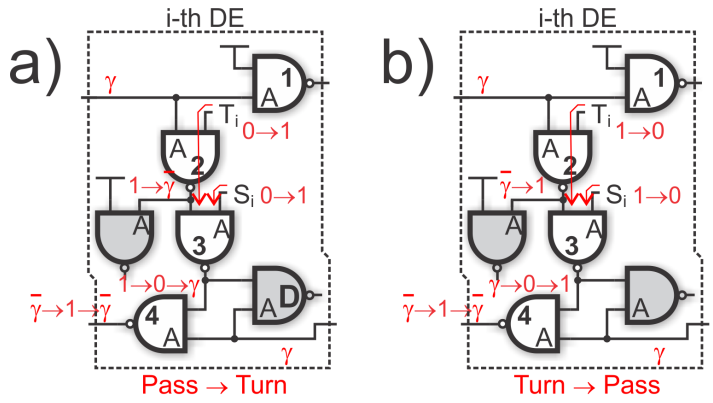

Figure 4.4.4: Possible glitch event of NAND-based DCDL with the driving-circuit of Figure 4.4.3 (1 of 3)

logic state from turn to pass. This is the opposite case of the previous one. The glitch ($\gamma \rightarrow 0 \rightarrow 1$) is located again in NAND3, but this time the glitch occurs if B input switches earlier than A input, thus requiring in this case the condition $t_A - t_B < t_{NAND}$ to avoid the glitch event. From Figure 4.4.4(b) we have $t_A = t_{S_i,HL}$ and $t_B = t_{T_i,HL} + t_{NAND}$, resulting in the following constraint to impose:

$$t_{S_i,HL} - 2t_{NAND} < t_{T_i,HL} \tag{4.4.7}$$

In Figure 4.4.5 is reported the case in witch the logic state of the i-th DE switches from turn to pass, while the logic state of the i+1-th DE switches from post-turn to pass.

This time the glitch may occur in NAND4, because of the switching of both input A, due to the HL transition of S_{i+1}, and input B, due to the HL transition of S_i. if input B switches earlier than input A, at the output of NAND4 the glitching event $\bar{\gamma} \rightarrow 0 \rightarrow \bar{\gamma}$ occurs. The condition to impose to avoid glitching is $t_A - t_B < t_{NAND}$, where $t_A = t_{S_{i+1},HL} + 2t_{NAND}$ and $t_B = t_{S_i,HL} + t_{NAND}$. This leads to the constraint:

$$t_{S_{i+1},HL} < t_{S_i,HL} \tag{4.4.8}$$

The forth case to analyze is shown in Figure 4.4.6, when the i-th DE

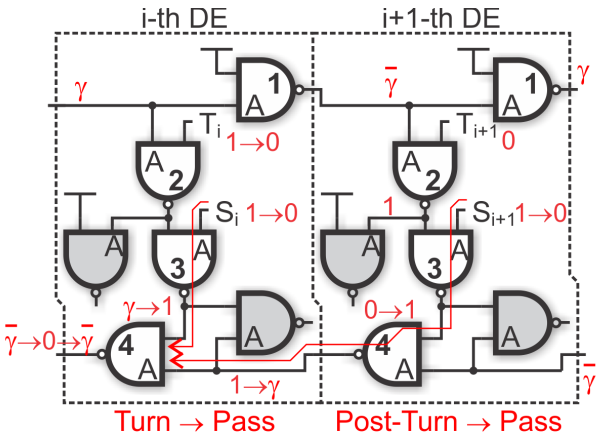

Figure 4.4.5: Possible glitch event of NAND-based DCDL with the driving-circuit of Figure 4.4.3 (2 of 3)

switches from pass to turn state, and the i+1-th De switches from pass to post-turn state. This occurs when the delay control code c is decreased from a value $c > i + 1$ to $c = i$.

In this case, both inputs of NAND4 of the i-th DE and a glitch can occur at its output. Referring to Figure 4.4.6 the A input switches from γ to 1 (because

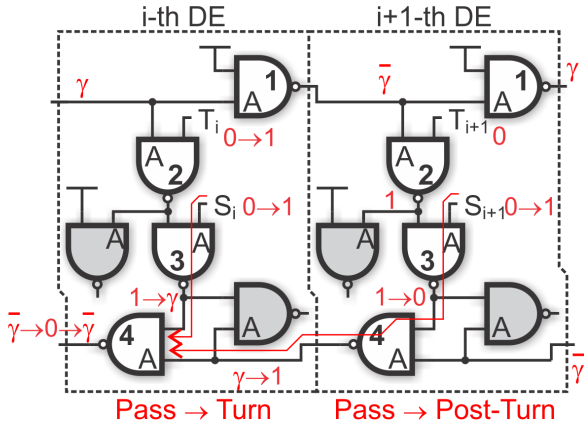

Figure 4.4.6: Possible glitch event of NAND-based DCDL with the driving-circuit of Figure 4.4.3 (3 of 3)

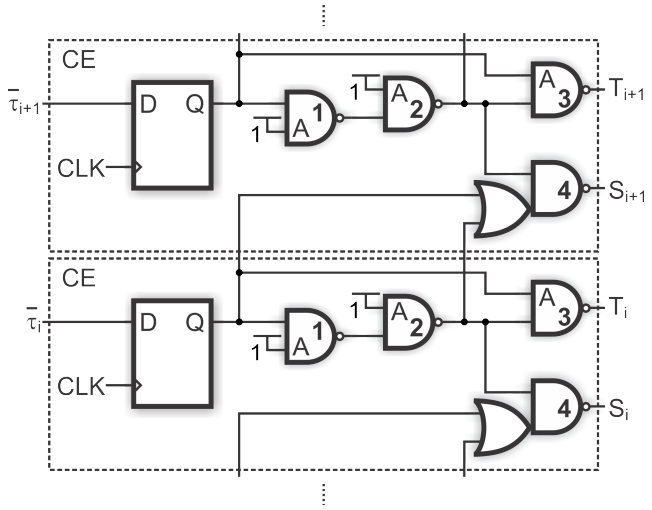

Figure 4.4.7: Single flip-flop glitch-free Driving-Circuit topology

of the low-to high (LH) switching of Si+1) while the B input switches from 1 to γ (because of the LH switching of Si). A glitch ($\bar{\gamma} \rightarrow 0 \rightarrow \bar{\gamma}$) can occur at the output of this gate if the A input switches earlier than the B input. The glitch free operation requires $t_B - t_A < t_{NAND}$. From the figure we note that $t_A = t_{S_{i+1},LH} + t_{NAND}$, while $t_B = T_{S_i,LH} + t_{NAND}$, that leads to the constraint:

$$t_{S_i,LH} - 2t_{NAND} < t_{S_{i+1},LH} \tag{4.4.9}$$

To avoid glitching events, The single flip-flop glitch-free driving-circuit of Figure 4.4.7 has been employed. The circuit is composed by a cascade of identical control-elements (CE), each implemented by using one flip-flop, three NAND gates and one OR-AND-INVERT (OAI) gate to impose the correct timing constraints on S_i and T_i control bits. For simplicity we will consider $t_{OAI} \simeq t_{NAND}$. In the driving-circuit in Figure 4.4.7, the cascade of 3 NAND gates allows to compute different propagation delays for low-to-high (LH) and high-to-low (HL) transitions of T_i. An HL transition of the flip-flop quickly brings the output of the NAND3 T_i to 1, and therefore $t_{T_i,HL} = t_{NAND}$, while the LH transition requires the switching of all the 3 NAND gates, and therefore $t_{T_i,LH} = 3t_{NAND}$. The propagation from the output of the flip-flop to S_i always goes through the cascade of the 2 NAND

and the OAI gate, therefore $t_{S_i,LH} = t_{S_{i+1},LH} = 3t_{NAND}$. The LH transition of the flip-flop output quickly brings S_{i+1} to low through the OAI gate, therefore $t_{S_{i+1},HL} = t_{NAND}$. The opposite propagation instead requires the switching of NAND1 and NAND2 of the i-th CE, and the transition of the OAI of the i+1-th CE, therefore $t_{S_{i+1},LH} = 3t_{NAND}$. By substituting the obtained delays in the constraints in (4.4.6)-(4.4.9), we can see that the contraints are all respected and the time margin is $2T_{NAND}$, similarly to the double flip-flop driving-circuit of [12]. With the driving-circuit in Figure 4.4.7 all the possible switching cases of control bits S_i and T_i have been verified with no glitch occurred. The circuit in Figure 4.4.7 exploits the redundancy of control bits in (4.4.5) with the encoding in Table 4.4.1 with a single flip-flop for each couple of i-th control bits, resulting in a considerable reduction of area and power dissipation in comparison to the double flip-flop driving-circuit proposed in [12] (Figure 4.4.2).

4.4.3 Layout and Performances

The delay-element of the delay-lines employed in the proposed DPWM have been realized full custom, balancing the capacitive loads on each interconnection to improve the delay-line linearity and reduce the INL. In Addition, the delay-elements have been designed to build each the delay-line with a simple juxtaposition of cells in a matrix layout. An example of the delay-line structure is reported in Figure 4.4.8. The control-elements of the driving-circuit have been realized following the same principle, to have a symmetric Layout.

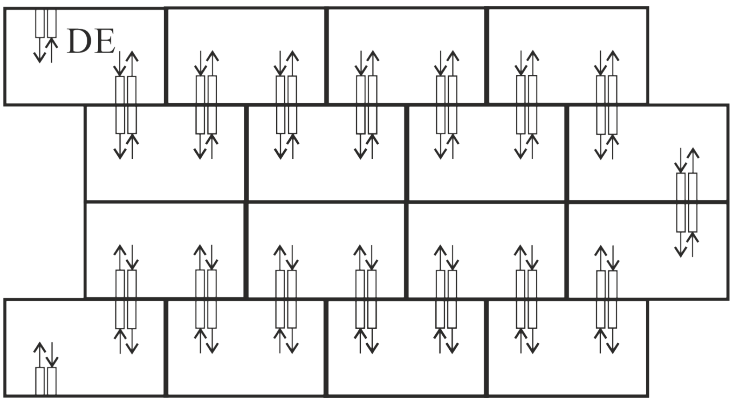

Figure 4.4.8: Delay-Line structure in the proposed DPWM

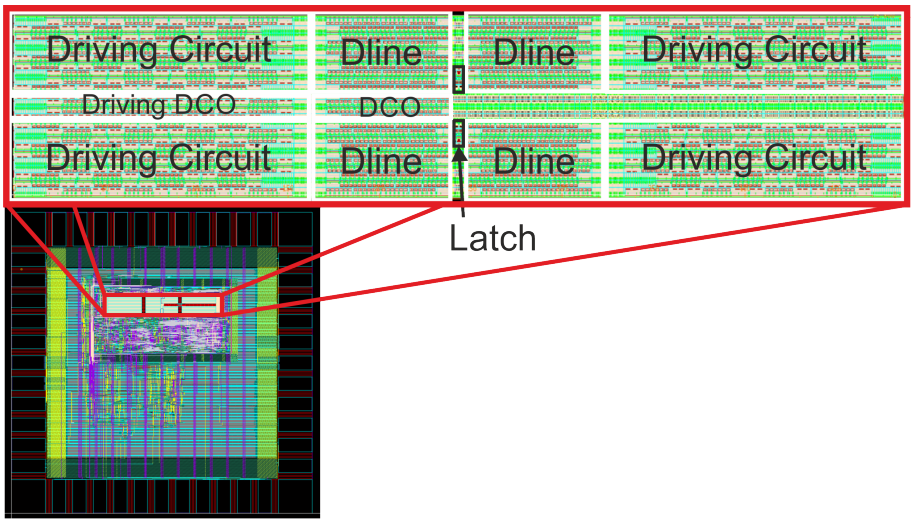

Figure 4.4.9: Full Custom Layout of the proposed DPWM

The four DCDL blocks have been placed in a mirror structure, firstly flipping one DCDL block horizontally, then flipping both vertically to obtain a symmetrical layout, as shown in Figure 4.4.9. The delay-lines and the DCO have been placed as close as possible to each other, in order to match any possible PVT variation of the circuit. Note that the layout of Delay-Line block has been realized in order to equalizes the parasitic, minimizing the differential non-linearity (DNL) of the DCDLs.

To analyze the linearity of the Delay-Line block, the delay-lines have been simulated for all possible control words. The simulations have been done considering a transistor level netlist of the Delay-Line block extracted from the layout with the inclusion of parasitic. The post-layout simulation performance

	LH case			HL case		
	T_{min} ps	T_r ps	Err ps	T_{min} ps	T_r ps	Err ps
Even	103.3	61.3	0.69	110.8	61.3	0.67
Odd	102.5	61.3	1.05	112.2	61.3	1.04
All	102.7	61.3	1.29	111.7	61.3	1.53

Table 4.4.3: Delay-Line block performances obtained by transistor-level simulations

of the Delay-Line block for typical corner are reported in Table 4.4.3 for the Low-to-High case and Table 4.4.3 for the High-to-Low case. The technology is UMC 130nm CMOS.

As discussed in § 4 each delay-line is able to generate a clock edge within DCO time period T_{DCO}, therefore for the choice of the number of delay-elements N, the following constraint must be respected:

$$N \cdot t_R + t_{min} \geqslant T_{DCO} \tag{4.4.10}$$

The choice of number N will be explained in the following section § 4.4.4.

4.4.4 Digitally Controlled Oscillator

The Digitally Controlled Oscillator (DCO) is the core of the proposed DPWM. As discussed in § 4, the delay of the delay-lines is dimensioned on the period of the DCO. With reference to Figure 4.0.1, the output of the DCO is the clock signal of the DCPS and the delay-lines. In addition the DCO is employed ad both input and clock in the Measurement Unit (§ 4.2), where the ratio T_{CLK}/T_{DCO} is measured to track PVT variations.

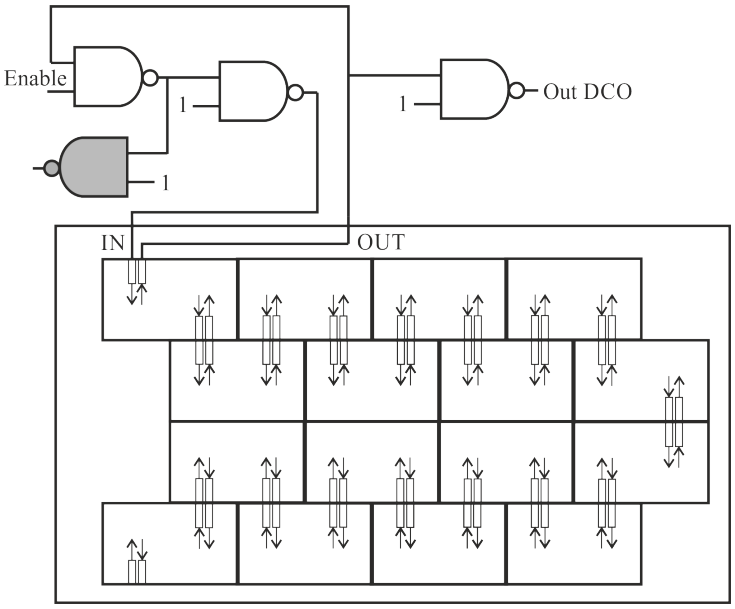

Figure 4.4.10: DCO scheme as a closed loop Delay-Line

Corner	$t_{min,DCO}/t_R$
Slow	2.653
Typical	2.651
Fast	2.652

Table 4.4.4: $t_{min,DCO}/t_R$ value varying the corner

The DCO is composed by a 16-tap DCDL closed in a loop by a NAND circuitry as shown in Figure 4.4.10. The period of the DCO T_{DCO} can be written as:

$$T_{DCO} = 2 \cdot (\delta_{DCO} + t_{loop}) \tag{4.4.11}$$

Where δ_{DCO} is the delay of the delay-line employed in the DCO, and $t_{loop} \simeq 3t_{NAND}$ is the delay introduced by the NAND circuitry closing the loop, referring to Figure 4.4.10. According to equation 4.4.3, and considering $N_{DCO} = 16$, the resolution of each DE $t_R = 2t_{NAND}$, and the minimum delay of the DCDL $t_{min} = 3t_{NAND}$, the period of the DCO can be written as:

$$\begin{aligned} &T_{DCO} = 2 \cdot (t_R \cdot N_{DCO} + t_{min} + t_{loop}) = \\ &= 2 \cdot (t_R \cdot N_{DCO} + t_{min,DCO}) \end{aligned} \tag{4.4.12}$$

where $t_{min,DCO} = t_{min} + t_{loop}$.

As stated in § 4 and shown in Figure 4.0.1, the ratio T_{DCO}/t_R is a crucial parameter in the circuit, due to the fact that it is employed in the DCPS to normalize the control words of the delay-lines to the resolution t_R. This parameter is neither an input, nor calculated inside the circuit, but it is a constant. For this reason, it must not change in presence of process, voltage and temperature variations. According to equation (4.4.12):

$$\frac{T_{DCO}}{t_R} = 2 \cdot (N_{DCO} + \frac{t_{min,DCO}}{t_R}) \tag{4.4.13}$$

Since N_{DCO} is a fixed value equal to 16, the only parameter that could vary is $t_{min,DCO}/t_R$. To ensure the stability of $t_{min,DCO}/t_R$ for PVT variations, extensive simulations have been done considering a transistor level netlist of the DCO block extracted from the layout with the inclusion of parasitic, for slow, typical and fast corner. The post-layout simulation performance of the

DCO block are reported in Table 4.4.4. It can be seen that varying the corner, the value of $t_{min,DCO}/t_R$ varies only on the third decimal number.

Since T_{DCO} have been explained, now we can choose the correct number of the delay-elements N of each delay-line as seen in equation (4.4.10), as anticipated in § 4.4.1. Inserting equation (4.4.12) in (4.4.10), we have:

$$N \geqslant 2 \cdot N_{DCO} + 2 \cdot \frac{t_{min,DCO}}{t_R} - \frac{t_{min}}{t_R} \tag{4.4.14}$$

Extrapolating the values $t_{min}/t_R \leq 2$ and $t_{min,DCO}/t_R \leq 3$ respectively from Table 4.4.3 and 4.4.4, and considering $N_{DCO} = 16$, from equation 4.4.14 we have $N \geqslant 36$. In the realized circuit, in order to optimize the symmetry of the layout of the delay-lines, N is chosen equal to 40.

4.5 Jitter Analysis and Circuit Sizing

The two main sources of jitter are the delay asymmetries introduced by the Delay-Line block, and the jitter sources due to the Modulator block and the Duty-Cycle and Period Synthesizer (DCPS) block. The jitter components in the Delay-Line block are reported in Table 4.4.3. In the following section, a theoretical jitter analysis for the Modulator block the DPS Synthesizer block is discussed. The Figure 4.5.1 shows the portion relevant for the jitter analysis of the Modulator and DCPS blocks. Please note that, when the modulation is turned off, $\Delta T/T_{CLK}$ is equal to 0, and $T_i/T_{CLK} = T_o/T_{CLK}$, therefore in these condition the Modulation Profile block does not introduce jitter.

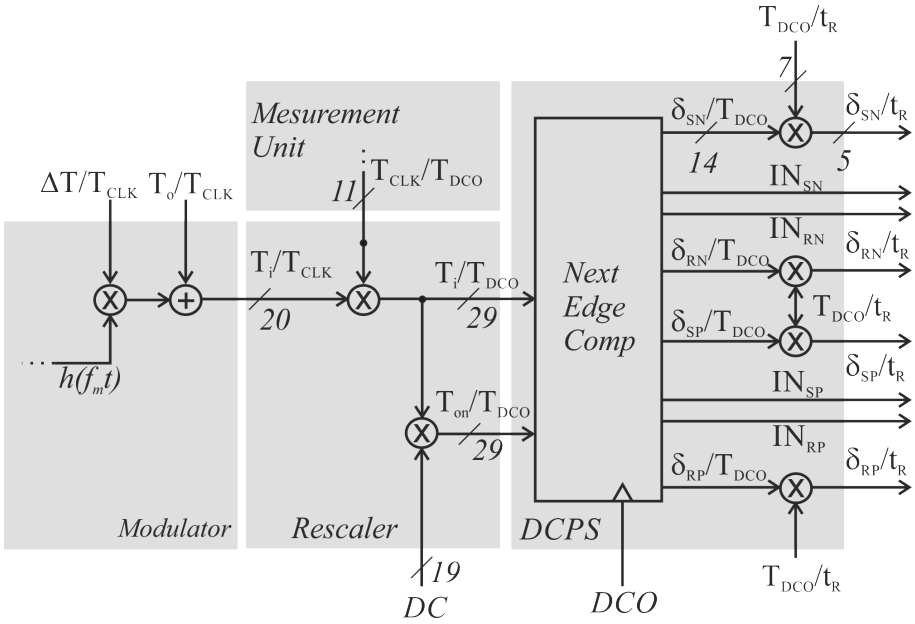

Figure 4.5.1: Portion of the circuit relevant for the jitter analysis (without modulation)

As explained in § 4.3, the DCPS generates the input signals for the delay-lines Δ_{SN}, Δ_{RN}, Δ_{SP}, Δ_{RP}, as showed in Figure 4.0.1. The DCPS block generates the control words δ_{SN}/t_R, δ_{RN}/t_R, δ_{SP}/t_R, δ_{RP}/t_R, and the input signals IN_{SN}, IN_{RN}, IN_{SP}, IN_{RP} with the help of a *Next Edge Computator*, a finite state machine (FSM), as shown in Figure 4.5.1. For simplicity, in the following analysis, the four control words are generalized with δ_{xx}, and

the four input signals with IN_{xx}. The signal δ_{xx}/T_{DCO} represents the ratio between the delay of the generated output edge from the DCO rising edge and the whole DCO period. Its maximum value is 1, due to the fact that each output edge can be positioned in a timing window of one DCO cycle. Therefore the MSB of δ_{xx}/T_{DCO} is 2^{-1}, and since δ_{xx}/T_{DCO} is on 14 bit, the LSB is 2^{-14}. The signals δ_{xx}/T_{DCO} are then scaled to the resolution t_R by a multiplication with T_{DCO}/t_R, that is a fixed value. The first jitter component taken in account is due to the quantization of δ_{xx}/t_R, and it corresponds to the error due to the resolution of the delay-line, and it is independent from the architecture and sizing of the DCPS. Let us call this jitter component $Jabs_{t_R}$:

$$Jabs_{t_R} = 0.5 \cdot t_R. \tag{4.5.1}$$

The second jitter component is due to the error on T_{DCO}/t_R. As discussed in § 4.4.4, this value is fixed, and from equation (4.4.13) and Table 4.4.4, is equal to 37.306 in the worst case. The signal T_{DCO}/t_R is on 7 bit, with an MSB equal to 2^5 and a LSB equal to 2^{-2}. With these specification, the closest value to 37.306 that can be imposed is 37.25, thus the jitter component due to the error on T_{DCO}/t_R is:

$$Jabs_{T_{DCO}/t_R} = 0.056 \cdot t_R. \tag{4.5.2}$$

The third jitter component is due to the quantization of δ_{xx}/T_{DCO} and can be easily written as:

$$Jabs_{Delay/T_{DCO}} = 2^{-14} \cdot \frac{T_{DCO}}{t_R} \cdot t_R = 2.3 \cdot 10^{-3} \cdot t_R. \tag{4.5.3}$$

Let us now analyze the error on the period introduced by the Measurement Unit output T_{CLK}/T_{DCO}. It affects both the generation of the output period through the signal T_o/T_{DCO}, and the generation of the on-period through the signal T_{on}/T_{DCO}. Considering the component of the error related to the output period T_o/T_{DCO} due to the error on T_{CLK}/T_{DCO}, according to equation (4.2.4), we have:

$$\varepsilon per_{T_o/T_{DCO}} = 0.03125 \cdot \frac{T_o}{T_{CLK}}. \tag{4.5.4}$$

With an input clock frequency of 10MHz, we obtain:

$$\varepsilon per_{T_o/T_{DCO}} = 0.0003125 \cdot T_o. \tag{4.5.5}$$

When the output clock frequency is chosen equal to 10MHz, the error becomes:

$$\varepsilon per_{T_o/T_{DCO}} = 31.25ps \simeq 0.5 \cdot t_R. \tag{4.5.6}$$

By generalizing for different values of T_o and d (see § 4.2), the value of the error on the period due to the Measurement Unit is a fixed percentage of the T_o, independent from PVT variations, and it can be written as:

$$\varepsilon per_{T_o/T_{DCO}} = (\frac{0.5}{d}) \cdot T_o\%. \tag{4.5.7}$$

For what concerns the component of the error on the period related to the on-period T_{on}/T_{DCO}, since the maximum value of the DC input signal is 1, we can easily obtain:

$$\varepsilon per_{T_{on}/T_{DCO}} = \varepsilon per_{T_o/T_{DCO}}. \tag{4.5.8}$$

4.6 Test-Chip Measurements

The circuit has been fabricated in UMC 130nm CMOS technology and is included in a 44 pin test chip. The DPWM layout and IC Micrograph are shown in Figure 4.6.1. The total DPWM area is $0.182mm^2$. The block including the delay-lines and their driving-circuits, the DCO and the SR Latch has been designed full custom and its placement has been carried manually, while the remaining parts have been implemented by place&route tools.

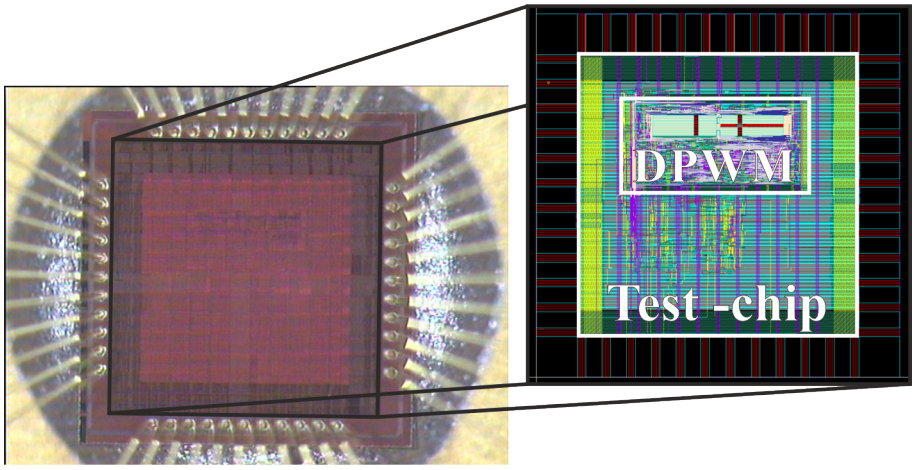

Figure 4.6.1: IC Micrograph and DPWM layout

4.6.1 Measurement Unit Verification

The first performed verification is on the Measurement Unit, since a malfunction of the Measurement Unit compromises the overall functionality of the DPWM circuit. As shown in Figure 4.0.1, and more accurately in Figure 4.1.3, the output of the Measurement Unit is employed to normalize the input signals to the DCO clock period. The verification of the Measurement Unit is possible by using the signal T_{CLK}/T_{DCO} at the output of the test chip, allowing the constant monitoring of the DCO period, since the input clock frequency is known. The parameter T_{DCO}, as seen in § 4.4.4, is directly related to the delay-lines resolution t_R, since the ratio T_{DCO}/t_R is a constant value.

The Measurement Unit performances have been analyzed by evaluating the T_{DCO} measured value varying the supply voltage for different input clock frequencies, as shown in Figure 4.6.2. The parameter d has been chosen equal to

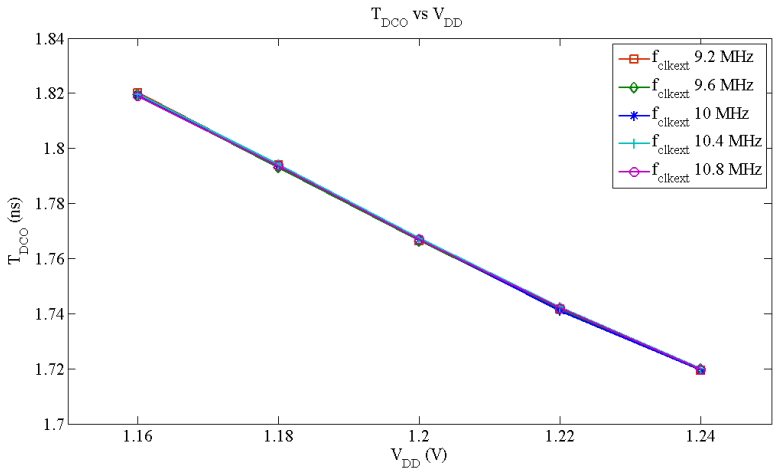

Figure 4.6.2: Experimental T_{DCO} values obtained for different supply voltage and clock frequency

16. In Figure 4.6.3 is displayed the measurement spread ΔT_{DCO} given by the maximum difference between the T_{DCO} values measured at each supply voltage. The data obtained confirm the correct operation of the Measurement Unit.

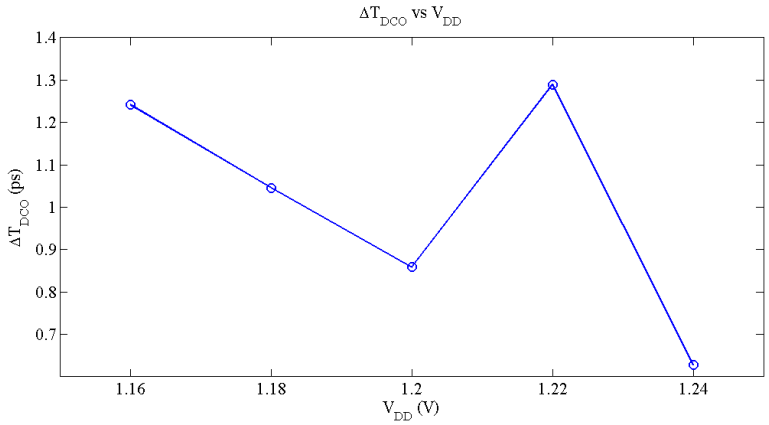

Figure 4.6.3: Experimental ΔT_{DCO} values obtained for different supply voltage and clock frequency

In fact, by varying f_{CLK}, the obtained T_{DCO} value is the same for the same supply voltage, and the maximum value of ΔT_{DCO} is $1.3ps$. From the theoretical analysis made in § 4.2, considering that in these measurements f_{DCO} is in the order of 550MHz, while f_{CLK} is in the order of 10MHz, substituting those values in the equation (4.2.6), we can obtain that $\varepsilon_{T_{DCO}} \simeq 1ps$, and the maximum value of the measurement spread is $\Delta T_{DCO} = 2 \cdot \varepsilon_{T_{DCO}} \simeq 2ps$, according to the obtained measured values of T_{DCO}.

4.6.2 Guard Time Programmability Verification

The guard time ($\Delta\tau_G$) programmability of the DPWM outputs, as said in § 4, provides the opportunity to achieve optimum efficiency in a DC-DC converter including synchronous rectifier.

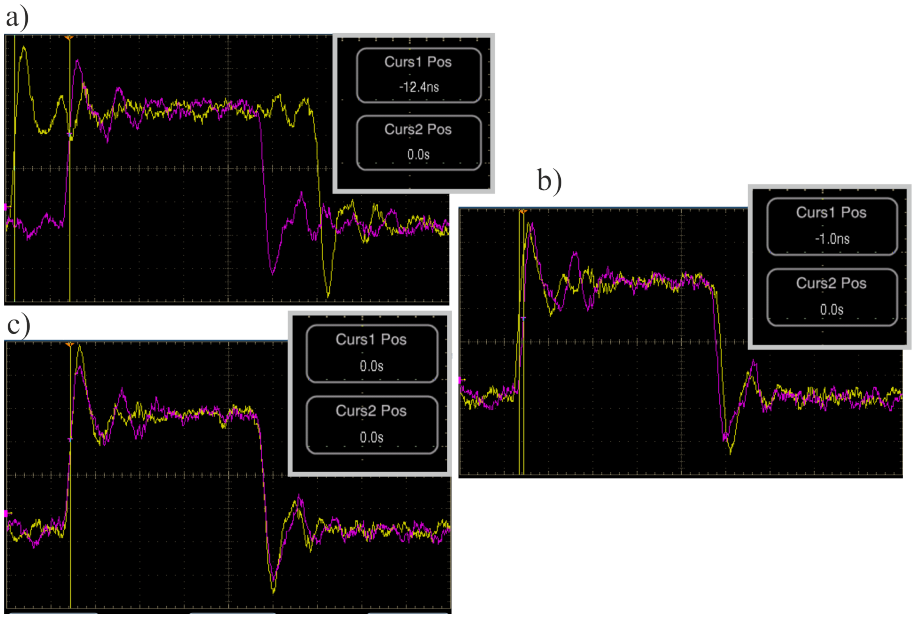

Figure 4.6.4: Guard time programmability verification for a) $\Delta\tau_G = 12.4ns$, b) $\Delta\tau_G = 1ns$, c) $\Delta\tau_G = 0ns$

To evaluate the correct functionality of the DPWM in generating replica output waveform with a programmable guard time on the edges, an extensive set of simulations have been done. According to Table 4.1.2, with an input clock of $f_{CLK} = 10$MHz, the maximum $\Delta\tau_G$ achievable by the circuit is

12.4ns, while the resolution is 200ps. In Figure 4.6.4 are shown the cases in which the imposed $\Delta\tau_G$ is 12.4ns (a), 1ns (b), and no guard time imposed (c).

4.6.3 INL Verification

The analysis on the linearity of the DPWM have been performed by measuring the duty-cycle varying the input duty-cycle code (DC), for different output waveform frequencies. Integral non linearity (INL) error is described as the deviation, in LSB or percent of full-scale range (FSR), of an actual transfer function, that in this case is the measured T_{on} period of the output waveform, from the expected T_{on} period imposed by the duty-cycle code. The expected T_{on} period has been adjusted with information about offset (intercept) and gain (slope) error, as in the best straight line INL approach. This approach yields the best repeatability, and it serves as a true representation of linearity.

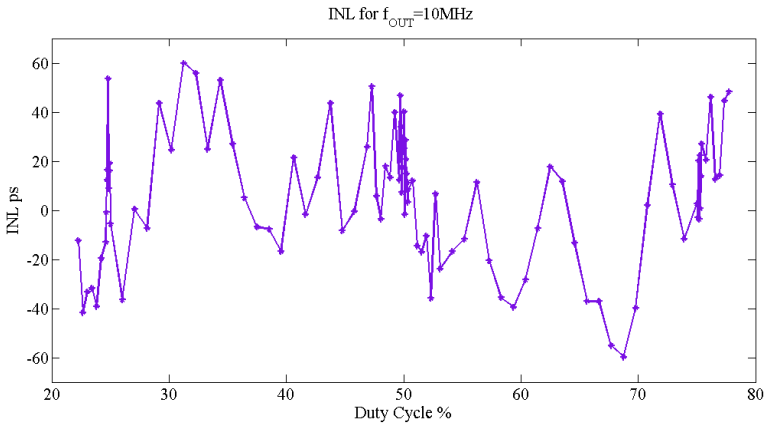

Figure 4.6.5: DPWM INL versus imposed duty-cycle, at $f_{out} = 10$MHz

The Figure 4.6.5 demonstrates the linearity of the DPWM in adjusting the duty-cycle with 11-bit resolution at an output frequency of 10MHz. The INL is less than 1.25 LSB, demonstrating excellent linearity and resulting in a resolution of 60ps. The Figure 4.6.6 instead shows the linearity of the DPWM adjusting the duty-cycle with 18-bit resolution at an output frequency 100kHz. Even in this case, the resolution is maintained 60ps, resulting in an INL less than 1.6 LSB. The results again demonstrate excellent linearity across a wide range of operating conditions, and the resolution doesn't decrease with the decreasing of the output frequency, but it is kept constant (60ps) for a wide output

frequency range. Please note that the resolution obtained is equal to the delay-line resolution obtained with transistor level simulations including parasitics reported in § 4.4.3 and Table 4.4.3.

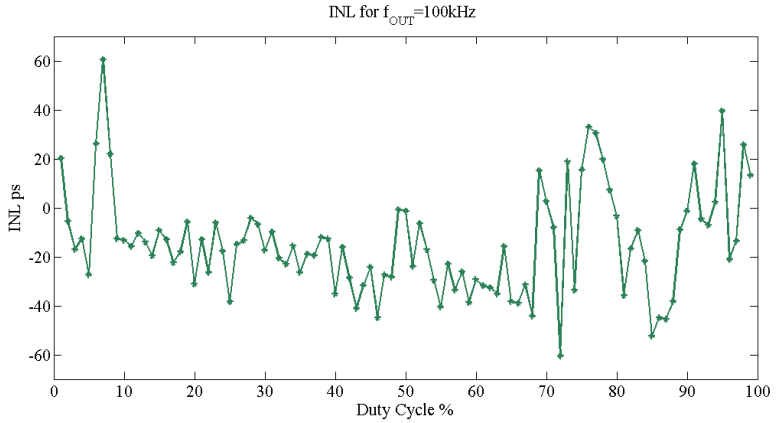

Figure 4.6.6: DPWM INL versus imposed duty-cycle, at $f_{out} = 100$kHz

4.6.4 Verification with Modulation

The following section shows the most significant measurements of the extensive verifications done on the DPWM chip when the modulation is on. The Figure 4.6.7 shows the experimental instantaneous output frequency of the output waveform Q_N of the DPWM obtained with $f_{CLK} = 10$MHz, $f_m = 10$kHz, $f_{out} = 10$MHz and $\Delta f/f_{out} = 9\%$. All the four modulation profiles have been considered: Triangular, Sawtooth, Hershey Kiss and SubOptimal Discontinuous.

The Figure 4.6.7 shows that the desired modulation profile is correctly imposed by the circuit in down-spreading from the imposed output frequency of 10MHz. In addition, it highlights the capability of the circuit to follow

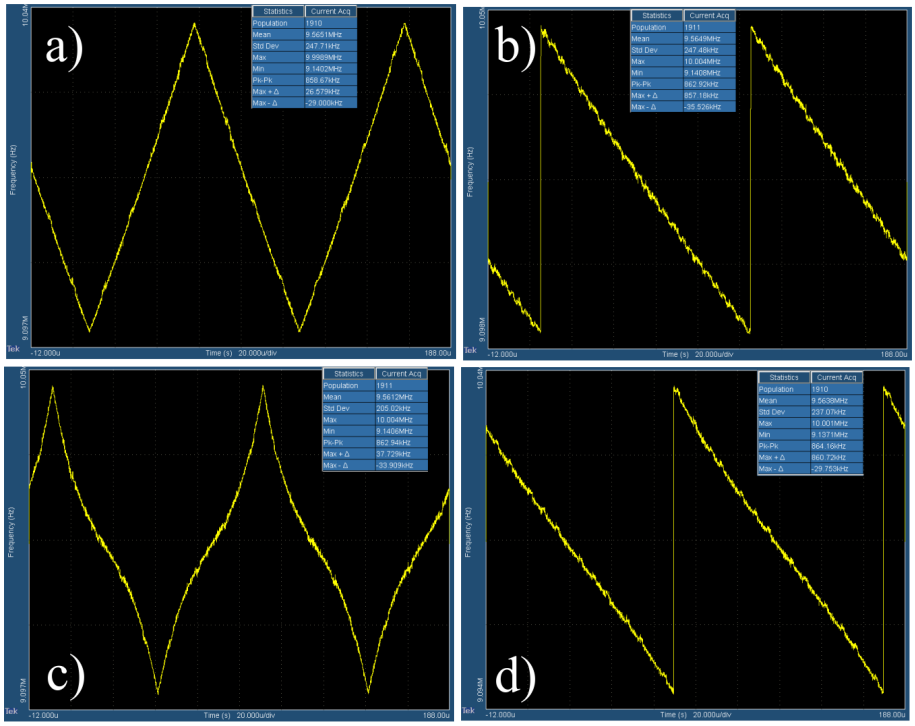

Figure 4.6.7: Experimental Modulation Profiles by TDSJIT software with f_{CLK}=10MHz, f_m=10KHz, f_{out}=10MHz, $\Delta f/f_{out}$=9%, for a) Triangular, b) Sawtooth, c) Hershey Kiss and d) SubOptimal Discontinuous modulation profiles.

perfectly all the desired modulation profiles, whether they be discontinuous as Sawtooth, complex as Hershey Kiss and both discontinuous and complex as the SubOptimal Discontinuous modulation profile.

The Figure 4.6.8 shows the experimental peak power reduction of the spectrum of the modulated waveform compared to the un-modulated waveform measured by Agilent PSA E4445A spectrum-analyzer in Peak-mode and with a resolution bandwidth (RBW) of 9kHz. The DPWM is configured in order to employ Triangular (Figure 4.6.8 a)), Sawtooth (Figure 4.6.8 b)), Hershey Kiss (Figure 4.6.8 c)) and SubOptimal Discontinuous (Figure 4.6.8 d)) modulation profile with $f_m = 10$kHz, $f_{out} = 10$MHz and $\Delta f / f_{out} = 9\%$, with a

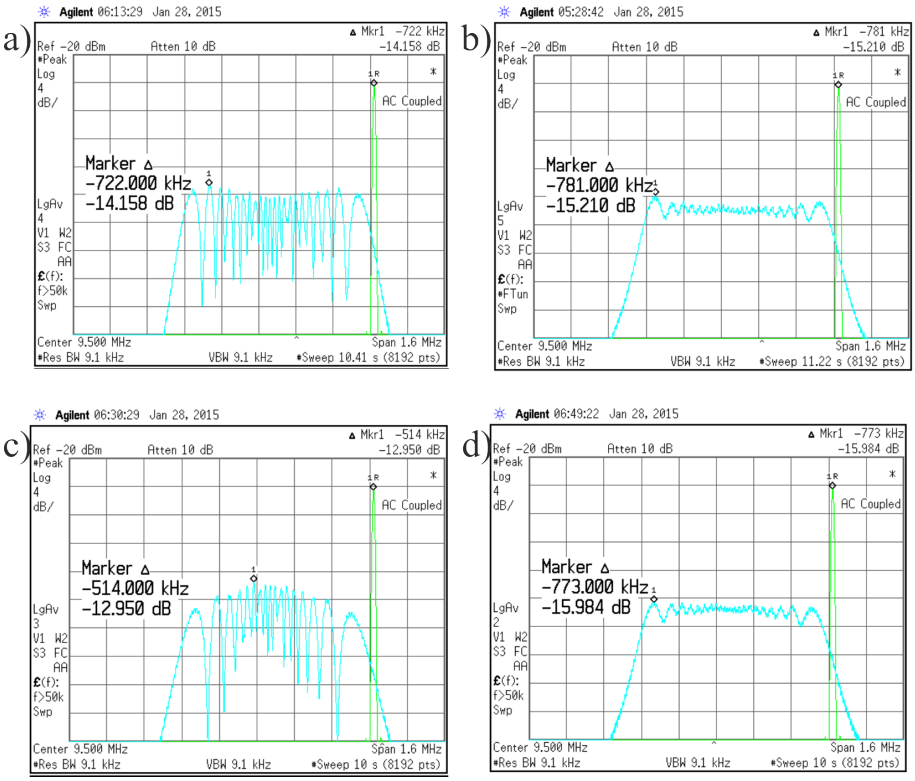

Figure 4.6.8: Experimental Modulation Gain for different modulation profiles: a) Triangular, b) Sawtooth, c) Hershey Kiss and d) SubOptimal Discontinuous modulation profiles (f_m=10KHz, f_{out}=10MHz, $\Delta f / f_{out}$=9%, RBW=9kHz).

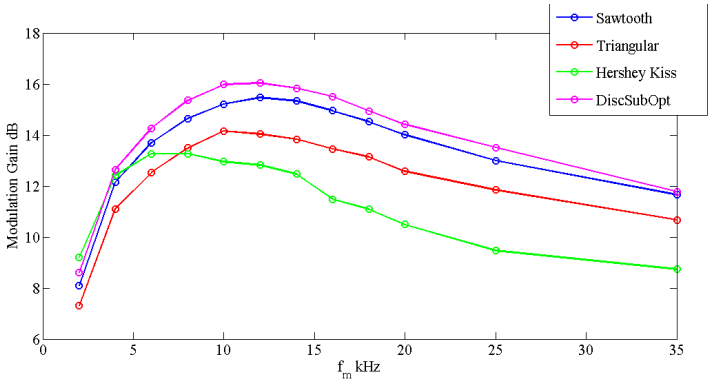

Figure 4.6.9: Experimental Modulation Gain for different modulation profiles and modulation frequencies (f_{out}=10MHz, $\Delta f/f_{out}$=9%, RBW=9kHz).

input clock frequency of 10MHz. The results in Figure 4.6.8 highlights that a considerable improvement in the peak power reduction of the spectrum can be obtained by discontinuous modulated waveforms with respect to the continuous modulated ones.

As reported in Figure 4.6.9, in order to evaluate the modulation gain, the

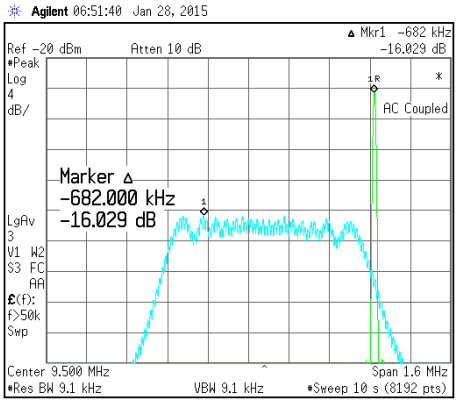

Figure 4.6.10: Experimental Modulation Gain for SubOptimal Discontinuous modulation profile with $f_m = 12kHz$, f_{out}=10MHz, $\Delta f/f_{out}$=9%, RBW=9kHz.

frequency modulated output waveform spectrum is measured by using Agilent PSA E4445A spectrum-analyzer in Peak-mode and with a resolution bandwidth (RBW) of 9kHz, varying the modulation frequency for the four different modulation profiles, with an output frequency of 10MHz and a 9% modulation depth.

The Figure 4.6.9 shows that the highest modulation gain is obtained by using the SubOptimal Discontinuous modulation profile, that achieves a slightly better result than the Sawtooth, while it achieves an improvement in modulation gain larger than 2dB with respect to the continuous modulation profiles (Triangular and Hershey Kiss). The results shown in Figure 4.6.9 are in accordance with the theoretical analysis done in § 2 [16]. The measured spectrum that achieves the best modulation gain is also reported in Figure 4.6.10, and it is obtained with the SubOptimal Discontinuous modulation profile for $f_m = 12$kHz.

4.6.5 Comparison with the state of the art

The performances of the DPWM IC are reported in Table 4.6.1 and compared with the state of the art. The developed circuit improves the resolution with respect to the previous art [17] [18] [19]. Please note that the proposed circuit does not decrease the time resolution with the increase of the period of the output waveform as in [19]. In fact, with a output waveform frequency of 10MHz, the resolution is 11-bits, resulting in a time resolution of $\simeq$ 60ps, while decreasing the output waveform frequency to 100kHz, the time resolution is maintained $\simeq$ 60ps, thus the bit resolution increases to 18-bit. As regards the frequency spreading, in literature this technique is not yet widespread in the realization of the DPWM, as instead for spread spectrum clock generators and high speed serial links. To the best of our knowledge, this represents the first DPWM that can perform frequency-discontinuous modulation. The area and power data can result higher than the previous art, but we can note that when the modulation is considered [20] these values tend to grow. In addition the proposed circuit provides 4 different output signals, requiring twice the number of area relative to the delay-line and a greater logic.

Reference	Approach	Tech	V_{DD}	$f_{out,max}$	Resolution		n of	Freq.	Disc.	EMI Red.		Area	Power
		nm	V	MHz	bits	f_{out}	Phases	Spread	Mod	Params	dB	mm^2	mW
Lukic et al. TPE'07	Self Osc. $+\Sigma\Delta$	180	1.8	12.3	10	12.3MHz	1	No	No	n.a.	n.a.	0.028	1
Barai et al. TPE'10	Non Self Oscillating	350	3.3	1	8	1MHz	1	No	No	n.a.	n.a.	0.07	n.a.
Lee et al. ECCE'2014	Hybrid	250	2.5	10	9 10	10MHz 100kHz	1	No	No	n.a	n.a	0.15	2.36
Pareschi et al. TCS'2014	Analog FM Digital core	180	2	1	n.a.	n.a.	1	Yes	No	$\Delta f = 0.2MHz$ $f_m = 35kHz$ RBW=$9kHz$	10.1	0.1	10.45
This Work	All-Digital Delay-Lines	130	1.2	10	11 13 18	10MHz 1MHz 100kHz	4	Yes	Yes	$\Delta f = 0.9MHz$ $f_m = 12kHz$ RBW=$9kHZ$	16	0.182	14

Table 4.6.1: Circuit performances and comparison with the state of the art

4.7 References

[1] Ching-Che Chung and Chen-Yi Lee. “An all-digital phase-locked loop for high-speed clock generation.” In: *Solid-State Circuits, IEEE Journal of* 38.2 (2003), pp. 347–351.

[2] Pao-Lung Chen, Ching-Che Chung, and Chen-Yi Lee. “A portable digitally controlled oscillator using novel varactors.” In: *Circuits and Systems II: Express Briefs, IEEE Transactions on* 52.5 (2005), pp. 233–237.

[3] Pao-Lung Chen et al. “A clock generator with cascaded dynamic frequency counting loops for wide multiplication range applications.” In: *Solid-State Circuits, IEEE Journal of* 41.6 (2006), pp. 1275–1285.

[4] Byoung-Mo Moon, Chan Hyeong Park, and Deog-Kyoon Jeong. “Monotonic Wide-Range Digitally Controlled Oscillator Compensated for Supply Voltage Variation.” In: *Circuits and Systems II: Express Briefs, IEEE Transactions on* 55.10 (2008), pp. 1036–1040.

[5] T. Matano et al. “A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer.” In: *Solid-State Circuits, IEEE Journal of* 38.5 (2003), pp. 762–768.

[6] S. Damphousse and M. Mallinson. “All digital spread spectrum clock generator for EMI reduction.” In: *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*. 2006, pp. 962–971.

[7] Rong-Jyi Yang and Shen-Iuan Liu. “A 40-550 MHz Harmonic-Free All-Digital Delay-Locked Loop Using a Variable SAR Algorithm.” In: *Solid-State Circuits, IEEE Journal of* 42.2 (2007), pp. 361–373.

[8] Rong-Jyi Yang and Shen-Iuan Liu. “A 2.5 GHz All-Digital Delay-Locked Loop in 0.13 um CMOS Technology.” In: *Solid-State Circuits, IEEE Journal of* 42.11 (2007), pp. 2338–2347.

[9] Shao-Ku Kao, Bo-Jiun Chen, and Shen-Iuan Liu. “A 62.5-625 MHz Anti-Reset All-Digital Delay-Locked Loop.” In: *Circuits and Systems II: Express Briefs, IEEE Transactions on* 54.7 (2007), pp. 566–570.

[10] Lei Wang, Leibo Liu, and Hongyi Chen. “An Implementation of Fast-Locking and Wide-Range 11-bit Reversible SAR DLL.” In: *Circuits and Systems II: Express Briefs, IEEE Transactions on* 57.6 (2010), pp. 421–425.

[11] Youngjoo Lee and In-Cheol Park. “Single-step glitch-free NAND-based digitally controlled delay lines using dual loops.” In: *Electronics Letters* 50.13 (2014), pp. 930–932. ISSN: 0013-5194. DOI: 10.1049/el.2014.0331.

[12] D. De Caro et al. “A 1.27 GHz, All-Digital Spread Spectrum Clock Generator/Synthesizer in 65 nm CMOS.” In: *Solid-State Circuits, IEEE Journal of* 45.5 (2010), pp. 1048–1060.

[13] Kwang-Hee Choi et al. “An Interpolating Digitally Controlled Oscillator for a Wide-Range All-Digital PLL.” In: *Circuits and Systems I: Regular Papers, IEEE Transactions on* 56.9 (2009), pp. 2055–2063.

[14] D. De Caro. “Glitch-Free NAND-Based Digitally Controlled Delay-Lines.” In: *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* 21.1 (2013), pp. 55–66.

[15] Youngjoo Lee and In-Cheol Park. “Single-step glitch-free NAND-based digitally controlled delay lines using dual loops.” In: *Electronics Letters* 50.13 (2014), pp. 930–932.

[16] D. De Caro. “Optimal Discontinuous Frequency Modulation for Spread-Spectrum Clocking.” In: *Electromagnetic Compatibility, IEEE Transactions on* 55.5 (2013), pp. 891–900.

[17] Z. Lukic, N. Rahman, and A. Prodic. “Multibit Sigma-Delta PWM Digital Controller IC for DC-DC Converters Operating at Switching Frequencies Beyond 10 MHz.” In: *Power Electronics, IEEE Transactions on* 22.5 (2007), pp. 1693–1707.

[18] M. Barai, S. SenGupta, and J. Biswas. “Digital Controller for DVS-Enabled DC -DC Converter.” In: *Power Electronics, IEEE Transactions on* 25.3 (2010), pp. 557–573.

[19] Y. Lee, T. Kang, and J. Kim. “A 9-11 bits Phase-Interpolating Digital Pulse-Width Modulator with 1000X Frequency Range.” In: *Industry Applications, IEEE Transactions on* PP.99 (2015), pp. 1–1.

[20] F. Pareschi et al. “Practical Optimization of EMI Reduction in Spread Spectrum Clock Generators With Application to Switching DC/DC Converters.” In: *Power Electronics, IEEE Transactions on* 29.9 (2014), pp. 4646–4657.

Conclusions

In this thesis an all-digital Pulsed-Width Modulator (DPWM) has been presented in all it's aspects: design, simulations and post fabrication measurements. The proposed DPWM is also capable of performing frequency spreading on the generated output waveforms to reduce EMI. The architecture of the proposed DPWM is fully digital, without the need of loops to perform frequency synthesis and spreading, avoiding the limitations of analog circuits in implementing frequency discontinuous modulation profiles. The design is based on standard-cells, thus simplifying the porting in new technologies when the technology scales down in dimensions. The architecture proposed is based on digitally-controlled Delay-Lines, dimensioned on the period of an internal Digitally Controlled Oscillator (DCO) and not on the period of the reference clock, reducing this way the required area of the Delay-Line and maintaining an high resolution at the same time, independently from the chosen output waveform frequency. The circuit generates four output pulsed-width modulated square-wave signals, with a programmable duty cycle value, and a programmable guard time, that provides the opportunity to achieve optimum efficiency in a DC-DC converter including synchronous rectifier. The circuit has been fabricated in UMC 130nm CMOS technology and is included in a 44 pin test chip. The experimental results highlight the capability of the circuit to follow perfectly all the desired modulation profiles, whether they be discontinuous as Sawtooth, complex as Hershey Kiss and both discontinuous and complex as the SubOptimal Discontinuous modulation profile.

Acknowledgments

At the end of my work I want to thank my supervisor Prof. Davide De Caro for his scientific and technical support and encouragement during my research. I would also like to thank all the people of the department of electronics, that have been part of my research time and spare time with their support and friendship. In particular, i would like to thank Michele, who always has an answer for my million questions, Luca for his wise advice, Peppe and Giorgio who started this journey with me, Gianpaolo and Paolo. All of you are good colleagues and even better friends.

Finally, I want to thank my beloved Rossella for the love she gives me and makes me stronger to face any difficulties and to overcome them, and my dear family for their love and their support not only during this work, but during my whole life and their sacrifices throughout my university career that have made this possible.