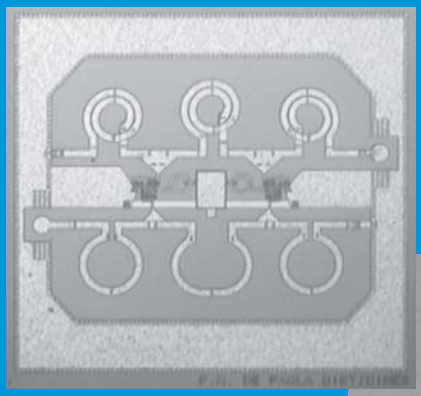
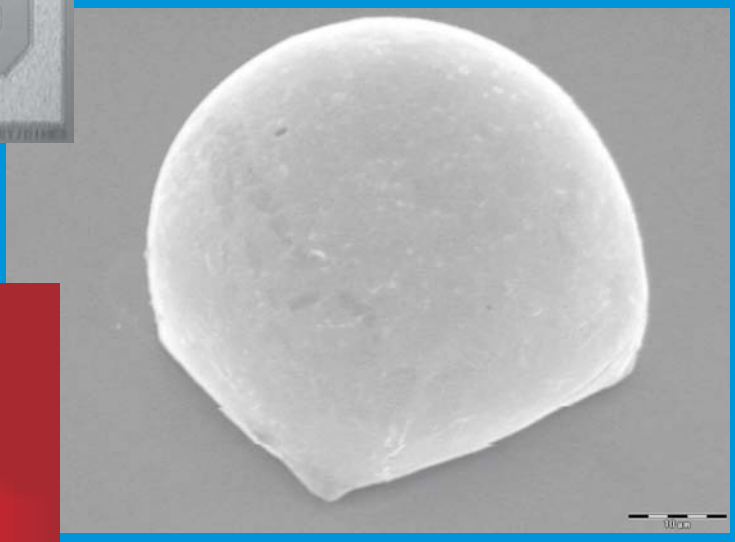
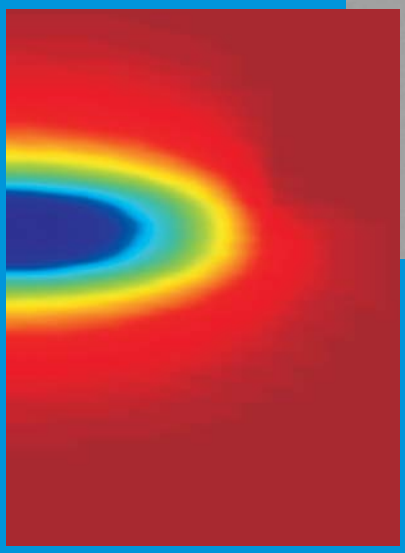
UNIVERSITÀ DEGLI STUDI DI NAPOLI FEDERICO II

Silicon as Smart Package for Photonic ICs

Ph.D. Thesis







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Dipartimento di Ingegneria Elettronica e delle Telecomunicazioni

Silicon as Smart Package for Photonic ICs

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Ph.D. Dissertation

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Chapter 1

Introduction

1.1 The need for a smart package

It is difficult, looking at the world around us, to find something that does not require a package. Even if in some funny futuristic scenario it will also be packaged and sold [1], only the air we breathe is something that we can directly use and consume without opening a package to find it. A package can be needed to improve the handling of a material (i.e. water is shipped enclosed into bottles) or to protect its content (i. e. fruits usually have a removable "protection layer" around them). Sometimes, finding the most suitable package for a specific good is a difficult task. This is because the package should not modify the properties of its contents. Moreover, a successful package must be cheap in order not to impact the manufacturing costs of the product itself. Finally, an important requirement of a good package is that it must be environment-friendly: the package of a food is the only residual so its composition must be optimized not to pollute and to be further re-used.
All these constrains straightforwardly apply to the world of electronics. Unfortunately, also an integrated circuit cannot be operated as is, i. e. a bare chip separated by the hosting substrate. This is because it is mandatory to provide the chip with a mechanical support, with heat removal structures, with protection shells to prevent damages and, finally, with an electrically conductive path to route the signals from the surface of the chip to the printed circuit board. Due to the need of fulfilling all of these requirements at the same time, packaging costs represent the main contribution to the final off-the-shelf price of the product.

In the huge family of electronics, one class of devices that is particularly prone to packaging issues is represented by the optoelectronic integrated circuits (OEICs). OEICs have catched the attention of the market in the very

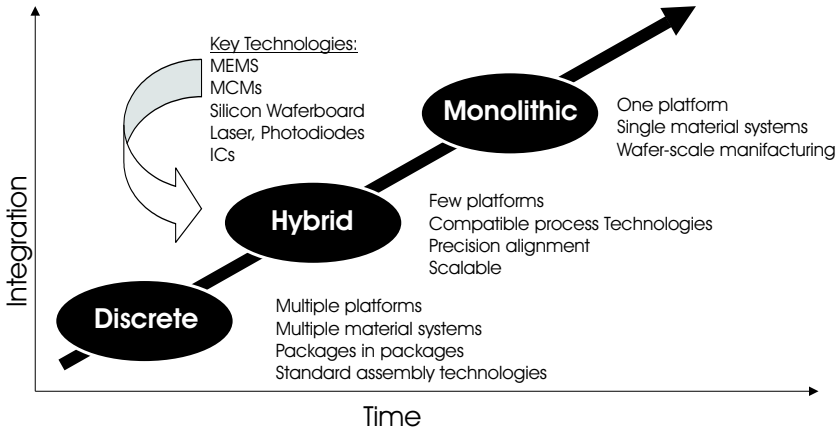


Figure 1.1: Optoelectronic integrated circuits technology trend as highlighted by JDS Uniphase (see text below).

recent years, mainly owing to the impressive growth of information demands related to the Internet and its applications. In order to increase the data-rate and then bring as much information as possible to the end users, several parallel optical channels are used with a relatively short link length. These systems require a large number of optoelectronic, electronic and optical components that introduce cost and size constraints that have not generally been a major issue in the long-haul network. Realization of optical interconnect-based systems will require significant advantages in component integration and packaging technology, since these constitute the most costly elements of present day optical fiber systems. In the technology routemap for OEICs recently sketched by [2] and given in figure 1.1, all the key factors for the selection of a optoelectronic solution are reported.

Optical systems typically employ individually packaged optoelectronic and electronic devices that are assembled on printed circuit boards. This conventional approach is unlikely to fulfill the high density and low cost requirements of these component-rich applications. New optoelectronic component integration and packaging approaches that are capable of accommodating the disparate physical, electrical, thermal and optical characteristics of components such as lasers, photo-detectors, integrated circuits and optical fibers are needed.

One approach to reducing the size and cost of highly parallel photonic systems is represented by the monolithic integration of optoelectronic and electronic devices on a single chip. Although OEICs have the potential for reducing cost through the use of batch processing, they often require complicated multi-step crystal growth and complex fabrication sequence. OEICs are also limited

since non-semiconductor components cannot be incorporated monolithically. A hybrid integration approach, however, offers the option of combining optoelectronic, electronic and optical components that are optimized with the most efficient design in the most appropriate material. Unlike OEICs, hybrid designs do not constrain the subsystem designer to work within one single material system and can incorporate non-semiconductor components such as optical fibers or micro-lenses. The provisioning of fiber input-outputs for optoelectronic devices is particularly important because it constitutes the major cost factor associated with the package of these components. For instance, the cost of a commercial pigtailed laser is dominated by the labor intensive process of actively aligning the fiber to the laser rather than the expense of the laser chip. Thus the benefits derived from an OEIC implementation of an optical subsystem may be overshadowed by the costs associated to the packaging.

1.2 Outline of this thesis

The motivation of this thesis derives directly from the observations outlined above and it is based on the concept of silicon-waferboard introduced by Armiento [3]. It can be briefly summarized as: to use silicon as a package material to enhance, support and interface the functionalities of indium phosphide based photonic ICs. The research project has been carried out through a collaboration between the University of Naples "Federico II", the Technische University of Delft and the Technical University of Eindhoven. The outline of the thesis is as follows.

In *chapter two*, the InP technology that is used through all the experiments is described. Particular attention is devoted to the description of the principle of operation of interferometer-based switches and modulators. In order to model the optical and electrical behavior of the phase shifting in a particular optical modulator, a special simulation strategy, based on the joint use of a device simulator and some custom FEM codes, has been pursued. Therefore the results of the computer-based analysis are compared with the experimental data yielding a good agreement and validating the simulation approach.

Chapter three provides an overview of the different solution for having an InP chip mounted on a silicon carrier. The flip-chip technique is addressed to be the most suitable and the different techniques for the deposition of the

solder bumps are detailed. In the second part of the chapter, the custom in-house developed flip-chip process is described. The process is implemented in the DIMES[1]-TUDelft laboratories. Several examples of successfully bonded InP and Si chips onto a silicon carrier are presented. Finally, some examples of hybrid systems (namely a semiconductor optical amplifiers array and a optical multiplexer-demultiplexer) that are expected to benefit from the integration with silicon are given. The examples are provided with simulations since at the time of writing it has not been possible to have experimental data.

In *chapter four* a scalable lumped equivalent model for coplanar-to-coplanar waveguide transition in flip-chip applications is presented. The model has been derived in order to simulate different topologies of flip-chip transition at high-frequencies directly in circuit simulations without the need of time consuming numerical simulations.

Chapter five describes the design of silicon-based integrated circuits for optical communications. In particular, the design of wide-band amplifiers as drivers for optical modulator is presented. After an overview of the common circuit schemes to achieve the large bandwidth required by digital communication systems, the concept of traveling wave amplification is presented and detailed in the case when the active devices are bipolar devices. Since the major bottleneck for standard silicon technologies at high-frequency is given by the parasitics introduced by the non-insulating substrate, the design and the characterization of a traveling wave amplifier (TWA) for 10 Gb/s optical communication implemented in the surface passivated high-resistivity DIMES03 bipolar process is presented. The TWA shows clearly the need of an high-resistivity substrate achieving a 3dB cut-off frequency of 7.5 GHz even with a device f_T of about 13 GHz. The experience acquired with the first design is then used for the design of a TWA that is optimized for the bonding together with one of the optical modulators characterized in chapter two. The optimization involves the design for high output voltage levels (as required for correctly operate the optical modulator) as well as the design of the layout in order to facilitate electrical and optical characterization of the final assembly.

Chapter six provides a discussion of the research that is described in the preceding chapters and the conclusions that can be drawn from this research, leading to proposals for further developments.

[1]Delft Institute of Microelectronics and Submicrontechnologies

Chapter 2

InP-based Switches and Modulators

Opto-electronic integrated circuits (OEICs) are frequently described as integrated circuits where light waves, instead of electric currents, are used to carry information around. To a certain extent, OEICs are comparable with IC: both use a semiconductor material as substrate and both are usually processed using similar techniques. ICs, however, mainly obtain their functionalities from complex interconnects between similar components whereas OEICs obtain their functionalities from the integration of devices with different tasks. Besides, ICs are fabricated onto a single material (most of the cases silicon), while OEICs require deposited layers of special material, whose composition has to be optimized for electrical, optical and, sometimes, electro-optical properties. Most of the optical network components are today fabricated in the form of OEICs. Being much smaller than their electrical counterparts, their implementation is sometimes much easier. OEICs can be either hybrid or monolithical. Hybrid opto-IC consist of two or more substrate materials and have the advantage of utilizing the best material for each component with existing processing techniques. Their disadvantage is that they introduce severe alignment problems, are less robust and seem less suitable for mass production. Monolithic OEICs, instead, use a single substrate material that makes them suitable for mass production. An additional advantage is the possibility to integrate the different components onto a single chip, avoiding complicated interconnects and then lowering the cost and size of complex circuits. The required integrability of a component depends on its (on chip) size and on the number of additional components that can be realized on the employed material.

The main functionality in a node of an optical network is undoubtedly represented by packet switching. Since switching devices are expected to have

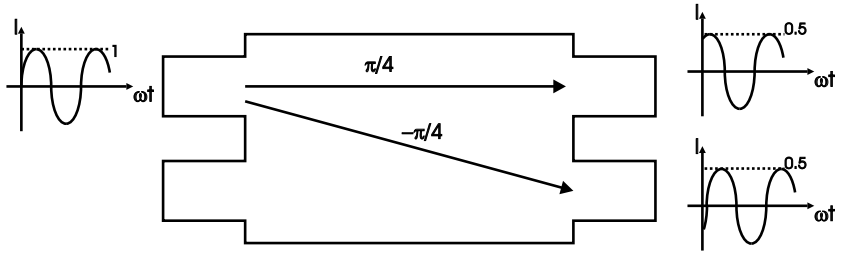


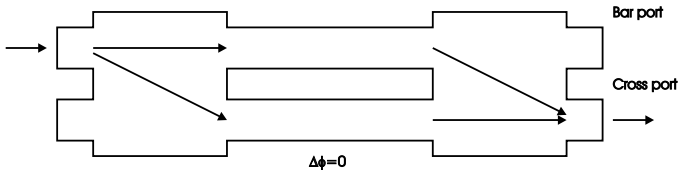
Figure 2.1: Schematic layout of the input MMI coupler. The phase difference between the outputs is 45°.

a large amount of in- and output nodes, scalability of elementary switches is an important property. Further, a high bit-rate transparency and a low power consumption are required for good operation. Optical switching can be accomplished in many ways, depending on the physical properties of the optical material (electro-, acusto- or thermo-optical effects) and on the switching architecture (Mach-Zehnder interferometer, directional coupler, Y-branch or SOA-gate switch [4]).

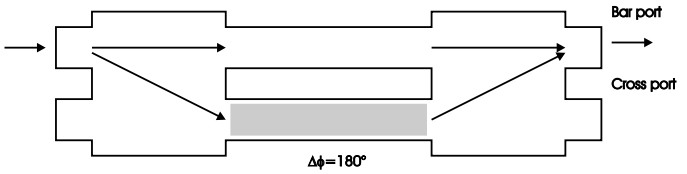
This chapter will be focused on the description of the principle of electro-optical switching and on how a switch can be used also as a light modulator. The description is completed with the results of numerical characterization of the phase-shifting section of a Mach-Zehnder modulator. The results of the simulations, obtained via a combination of finite element solver (ATLAS and FEMLAB) and in-house MATLAB code are validated by comparison with some experimental data.

2.1 Mach-Zehnder Switches

A Mach-Zehnder interferometer based optical switch is composed of three sections, namely a phase modulation section with two multimode-interference (MMI) sections, one at the input and one at the output. In order to fully understand its operation, the single elements need to be described. Since the analytical description of the different optical devices is beyond the scope of this thesis, only a schematic view will be provided. The input MMIs can be considered as a four terminal device that splits the entering light into two signals, with amplitude equal to half of the incoming one and a phase which depends on the access port (see figure 2.1). The outputs of the MMI are then connected to the two arms of a phase modulation section. This section is responsible of adding an extra controlled phase shift to one of the two arms. This is done by changing the refractive index (and then the propagation



(a) Passive state (cross)



(b) Active state (bar)

Figure 2.2: Schematic layout of a 2×2 MZI switch.

constant) of the material by applying an external voltage. This property of the material is known as electro-optical effect and it is different for each material. The overall electrical induced phase shift depends by many complex different phenomena, which will be detailed for InP based compounds in the next sections. Finally, the two optical signals are combined again by the second MMI. By considering as input port of the whole device the same of figure 2.2, and by assuming an externally induced electric field that provides an extra 180° phase shift in the central section, two possible situation can be spotted. In the first case, i.e. for an externally applied voltage equal to zero, the situation is the one depicted in figure 2.2(a). Without any other phase unbalance, the phases of the two beams interfering at the bar port is

$$\begin{aligned}\phi_{beam1} &= \pi/4_{MMI,input} + \pi/4_{MMI,output} = \pi/2 \\ \phi_{beam2} &= -\pi/4_{MMI,input} - \pi/4_{MMI,output} = -\pi/2\end{aligned}$$

resulting in a destructive interference. Conversely, at the cross port,

$$\begin{aligned}\phi_{beam1} &= \pi/4_{MMI,input} - \pi/4_{MMI,output} = 0 \\ \phi_{beam2} &= -\pi/4_{MMI,input} + \pi/4_{MMI,output} = 0\end{aligned}$$

and then the two beams coherently interfere giving arise to an output signal. If, instead, there exists a π -phase shift between the two signals (figure 2.2(b)), the light emerges from the bar port.This can be easily verified by calculating again the phases of the two interfering signals at each port. For the bar port:

$$\begin{aligned}\phi_{beam1} &= \pi/4_{MMI,input} + \pi/4_{MMI,output} = \pi/2 \\ \phi_{beam2} &= -\pi/4_{MMI,input} + \pi - \pi/4_{MMI,output} = \pi/2\end{aligned}$$

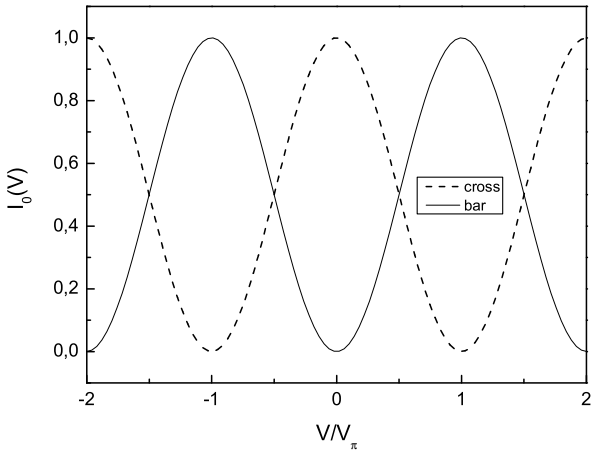


Figure 2.3: Calculated transfer function for the bar and cross port for different values of the external voltage. The lengths of the arms are supposed to be equal (i.e. $\phi = 0$).

and so the two beams are in-phase. Similarly at the cross port:

$$\phi_{beam1} = \pi/4_{MMI_input} - \pi/4_{MMI,output} = 0$$
$$\phi_{beam2} = -\pi/4_{MMI,input} + \pi + \pi/4_{MMI,output} = \pi$$

there is cancelation of the waves. By using this interferometric technique, very high contrast ratios between the bar and the cross state can be obtained. Figure 2.3 shows the intensities at the bar and cross port as a function of the phase shift induced in one of the two phase-shifting sections (as in figure 2.2). By changing the phase, light is gradually transferred from the cross port to the bar port and the switch is in the bar state at an external voltage V_π, corresponding to a 180° phase shift. Neglecting the crosstalk, the intensity at the bar port is:

$$I_{bar}(V) = I_i \sin^2(\pi \frac{V}{2V_\pi} + \phi)$$

where V_π is the voltage required to the device to completely switch from bar to cross state and ϕ is any static imbalance between the interferometer arms. Similarly at the cross port:

$$I_{cross}(V) = I_i \cos^2(\pi \frac{V}{2V_\pi} + \phi)$$

The transfer functions are shown graphically in figure 2.3.
Mach-Zehnder switches are currently used in optical routers for broadband

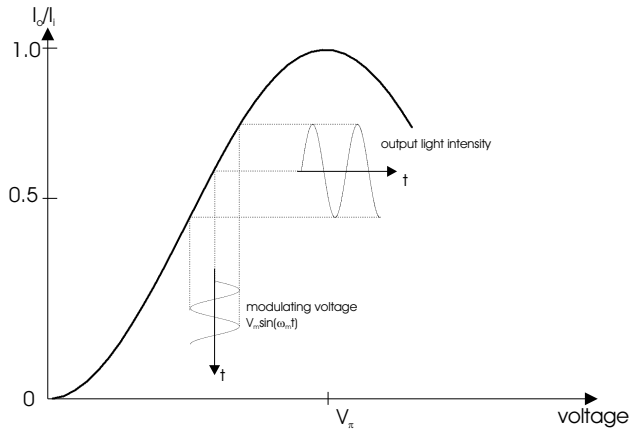


Figure 2.4: Output light intensity versus the modulating voltage.

optical networks. The traditional materials for the realization of such devices are $LiNbO_3$ and III-V semiconductors. The difference between them is the way the electric field interact with the optical signal and the corresponding change in refractive index. InP-based devices are characteristic of a larger phase shift per unit length, making them more suitable for miniaturization. Further, on III-V materials it is also possible to integrate the electronics required to correctly drive and operate the optical device.

2.2 Mach-Zehnder Modulators

It is possible to operate a Mach-Zehnder switch as a analog or digital light modulator. This can be achieved by considering a modulating signal applied to the electrode in the phase-shifting section. If the amplitude of the modulating signal is much lower than V_π (see figure 2.4), the modulator behaves like a linear analog device. Conversely, if the modulating voltage is a square pulse-train with peak-to-peak amplitude equal to V_π, the device works as a broadband modulator. However, in case of broadband modulation, the system has to be designed in order to meet the high-frequency constrains of the utilized modulation scheme. The simplest way to implement a Mach-Zehnder modulator is to use electrodes that can be considered as lumped elements. In most cases the lumped element is the capacitance of a reverse biased p-n junction in InP-based devices or of a Schottky connected diode in the case of $LiNbO_3$ technologies. The advantages of using a lumped electrode solution is that the electrodes are short and easy to drive in the low-frequency regime. Unfortunately, as frequency increases, their speed of operation is limited by the RC time constant of the circuit, with R equal to either the termination

resistance or the generator resistance. It is possible to reduce the capacitance by shortening the device and then increase the operation speed. However, shortening the device results in reduced interaction between the externally generated electric field and the optical signal, so that an higher modulating voltage is required to achieve the same results. Operation speed and low driving voltage are hence contradictory demands and cannot be easily fulfilled at the same time. Finally, also impedance (50 Ω) matching between the source and the modulator cannot be easily realized [5].
A very well-established approach to obtain very wide-bandwidth modulators is the so-called *traveling-wave* design. In such a design the electrode is designed as a transmission line. Therefore, electrode capacitance is distributed and does not limit the modulator speed due to the above mentioned RC time-constant limitations. The modulating voltage wave then propagates in exclusively the same direction and at precisely the same speed as the resultant modulation envelope of the optical wave, permitting the phase modulation to accumulate monotonically, irrespective of frequency. Since the electrode capacitance is not anymore the bandwidth limit, one can make the electrode very long, typically thousand times the wavelength. Therefore, the drive voltage requirements can be significantly relaxed without sacrificing electrical bandwidth [6]. In this kind of design, then, the properties of the electrode determine the main properties (bandwidth and drive voltage) of the modulator. The frequency response of an idealized traveling-wave modulator is [7]:

$$\frac{\sin\left(\frac{\pi f_m |n_o - n_\mu| L}{c}\right)}{\frac{\pi f_m |n_o - n_\mu| L}{c}} \tag{2.1}$$

where f_m is the modulation frequency, n_o and n_μ are the optical and the microwave effective refractive index values, respectively, L is the length and c is the free-space velocity of the light. the optical and the microwave refractive index are in general different and depends on the optical properties of the material and from its dielectric constant respectively. The electrical bandwidth derived from (2.1) is:

$$f_0 = \frac{1.4c}{(\pi\,|n_o - n_\mu|\,L)} \tag{2.2}$$

Based on (2.2), the maximum bandwidth is achieved when n_o matches with n_μ or, equivalently, when the group velocity of the modulating and that of the modulated one have the same value [8]. Obviously, since the electrode is now a coplanar waveguide, its impedance must be matched to the one of the system that provides the modulation voltage. Achieving velocity match usually requires a careful optimization of the electrode layout and dimensions.

In case of $LiNbO_3$ with a Ti in-diffused optical waveguide, the effective index of the optical mode is around 2.15 while a coplanar transmission line running along the same direction has an effective microwave index (calculated as suggested in [9]) larger than four. As a result, an electrical signal applied to the electrode will travel significantly slower than the optical wave.
In III-V semiconductors, the optical index of refraction is about 3.4 and the relative dielectric constant at microwave frequencies is about 13, corresponding to an index of 3.6. Since it is easier to form electrodes on the surface of the crystal, the most commonly used electrode is either a coplanar waveguide or coplanar stripline structure. The optical beam is entirely confined in the semiconductor (typically in a ridge waveguide) and then its optical index is exactly 3.4. The microwave and millimeter-wave electric field, on the other hand, fringes into the air experiencing an effective index between the air and the semiconductor that can be approximated as:

$$\varepsilon_{eff} = \frac{\varepsilon_{III-V} + 1}{2} \tag{2.3}$$

A more accurate modeling would have required the utilization of complex domain transformation to calculate the effective dielectric index [9]. However, for structures like the one considered, with a metal layer sandwiched between only two dielectric layers (substrate and air) and considering the substrate as infinitely thick, equation (2.3) is a good approximation. Therefore the effective dielectric constant is around seven, which corresponds to a microwave index of about 2.65. This reflects in a 38% of index mismatch between the optical and the microwave signals, requiring about 23% velocity reduction. Therefore, in III-V compound semiconductors, velocity matching requires slowing down of the microwave signal. The most commonly used technique to slow the microwave signal is to use a slow-wave transmission line, i.e. a standard transmission line periodically loaded with lumped capacitances. The electrode of the modulator presented in the next section has been designed only for impedance matching, while the refractive index of the material has been optimized to accommodate velocity mismatches.

2.3 InGaAsP Technology

III-V direct-bangap semiconductor materials based on InP are widely used for optical communication device applications. The quaternary (III-V) alloy InGaAsP lattice matched to InP offers the possibility to tune the bandgap from 0.97 μm to 1.65 μm by adjusting its composition. This range easily covers the two wavelength windows 1.3 μm and 1.55 μm for optical communications. By choosing the bandgap wavelength of the quaternary layer

smaller than the signal wavelength, transparent low-loss waveguide structures can be fabricated and by choosing a longer wavelength material a detector can be obtained. Quaternary alloys can also be used to manufacture a laser or a optical amplifier around its emission wavelength. P- or n-type doped regions can be defined by incorporating other elements like Si, Be or Zn, which can be used to fabricate electronic devices in InP-based materials. The properties of the quaternary $In_{1-x}Ga_xAs_yP_{1-y}$ compound, such as the lattice constant and the bandgap energy, are determined by the fractional amount of the binary constituents. A detailed table with the material properties at room temperature can be found in [10].

The basic structure of a photonic integrated circuit is the waveguide. The ridge waveguide structure consists of an InP substrate and buffer layer, an InGaAsP film and an InP cladding [11]. In such a structure, since $n_{InGaAsP} > n_{InP} > n_{air}$, the effective refractive index as experienced by an optical field is the highest inside the film underneath the ridge and the light is confined both in transversal an lateral direction. Since all the materials have a bandgap energy that is larger than than the photon energy, the structure is transparent for the signal wavelengths. More complicated devices such as optical (de)multiplexers, semiconductor optical amplifiers or mumltimode interference coupler can also be realized.
Usually, the calculation of the effective refractive index (and of course its variation when an external voltage is applied) in the guiding section of an InGaAsP device is complicated by the presence of the different layers in the layer stack. In order to facilitate this calculations, in the following subsections is presented an innovative simulation strategy that combines device simulators and customary developed FEM solvers to predict the behavior of complex electro-optic devices, in this particular case a Mach-Zehnder modulator.

2.3.1 Numerical Characterization of the Phase-Shifting Section

With reference to figure 2.5, the electrical device consists of an InP/ InGaAsP p-i-n diode. Starting from an InP substrate, two high-doped buffer layers are grown for optical confinement and ohmic contact purpose. An InGaAsP bulk-layer makes the guiding filmlayer. The cladding layer is non-intentionally doped in order to move the absorbing p-layers away from the waveguide core. The p-doped layer is capped by a thin highly doped layer in order to obtain good ohmic contacts. The difference in refractive index between the film layer and the substrate/cladding guarantees that the optical

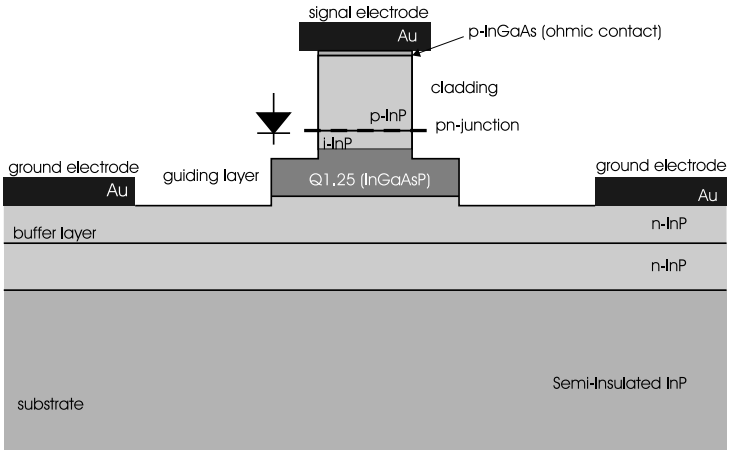


Figure 2.5: Cross section of the device in the phase shifting region. Note the position of the junction that generate the depleted regions.

radiation is all confined where the depletion of the p-i-n diode under reverse bias condition takes place. The principle of operation of this device is very simple: by depleting the guiding layer it is possible to vary its refractive index due to plasma dispersion effect and band-filling effect; moreover, refractive index variation takes also place due to the Pockels and Kerr mechanism inside the material. The relationship between injected (depleted) free carriers, electric field and refractive index variation are summarized in the following.

Pockels effect. In anisotropic semiconductors without inversion symmetry, such as InP/InGaAsP, a linear dependence of the refractive index with the electric field in the substrate can be observed. This effect is anisotropic and gives the TE polarized light a positive $\Delta n_{Pockels}$ for light propagating along $\langle 1\bar{1}0 \rangle$ direction and a negative $\Delta n_{Pockels}$ for the light propagating along $\langle 110 \rangle$ direction. For a wafer grown on a (100) substrate and with an electric field perpendicular to this plane, the negative refractive index change can be written as:

$$\Delta n_{\text{pockels}}(\theta, E) = \frac{1}{2} n_0^3 r_{41} E \cos(2\theta) \tag{2.4}$$

where θ is the angle between the TE-polarized light propagation direction and the [110] direction, E is the applied electric field, n_0 is the unperturbated refractive index and r_{41} is the linear Pockels coefficient. For InP/InGaAsP materials, the Pockels coefficient has been measured to be [12]:

$$r_{41} = 1.4 \times 10^{-10}\ [cm/V] \tag{2.5}$$

TM-polarized light and light propagating in [100] direction are not affected by this refractive index change.

Kerr effect. Together with the linear Pockels effect, a quadratic dependence of the index change on the applied field is observed. This effect is isotropic and polarization independent. The induced refractive index change is then proportional to the square of the applied electric field:

$$\Delta n_{\text{kerr}} = \frac{1}{2} n_0^3 R_{\text{kerr}} E^2 \tag{2.6}$$

The Kerr coefficient $[cm^2/V^2]$ was found to obey to the empirical relation

$$r_{\text{kerr}} = 1.5 \times 10^{-15} e^{-8.85\Delta E} \ [cm^2/V^2] \tag{2.7}$$

where ΔE represents the difference in gap energy (in eV) between the photon energy of the guided light and the material.

Plasma effect. The InP/InGaAsP refractive index can also be changed by intra-band absorption, which is indicated as plasma-dispersion effect. Since it is related to free-carriers concentration in the guiding section, its effect on a reverse biased p-i-n diode is to produce a positive index change:

$$\Delta n_{\text{plasma}} = \left(\frac{e^2 \lambda^2}{8\pi^2 c^2 \varepsilon_0 n_0} \right) \left(\frac{N}{m_e} + P \left(\frac{m_{hh}^{1/2} + m_{lh}^{1/2}}{m_{hh}^{3/2} + m_{lh}^{3/2}} \right) \right) \tag{2.8}$$

where e is the electron charge, λ the wavelength, c the free space light speed, n_0 the refractive index, m_e the electron mass, m_{hh} and m_{lh} the heavy and light hole masses, N and P the electron and hole concentrations.

Band-filling Effect. Because of the carried depletion by reverse biasing the structure of figure 2.5, the absorbtion coefficient α of the depleted region changes as the Fermi level decrease. This modification reflects in an isotropic refractive index change in the depleted regions. The resulting variation is calculated by using Kramers-Kronig formula:

$$\Delta n_{\text{band-filling}} = \Delta n \left(E, N_d \right) = \frac{hc}{2\pi^2} \int_0^\infty \frac{\Delta \alpha \left(E', N_d \right)}{E'^2 - E^2} dE' \tag{2.9}$$

where

$$\Delta \alpha \left(E \right) = \alpha \left(E, 0 \right) - \alpha \left(E, N_d \right) \tag{2.10}$$

is the electro-absorption in a material with a band gap energy of E'. The refractive index change due to band-filling is much stronger than for bulk InP and, at a wavelength of $1.55\mu m$ the variation due to plasma -effect is about four times smaller .
The strongly dependence of plasma and band-filling on the carrier concentrations, clearly stated in (2.8) and (2.9), motivates the need of a simulation tool that can effectively take them into account when calculating the variation of refractive index. Unfortunately, optical simulators are not able to provide this kind of analysis, which can be accomplished by conjugating a simulation of the electrical device with an optical analysis. To correctly characterize complex electro-optic devices, it has been developed a new design strategy, consisting of linked electrical and optical simulations in order to obtain an exact refractive index map in the cross section of the phase shifting section of the device. To convert the variation in refractive index into amplitude modulation of optical radiation, a Mach-Zehnder interferometer (MZI) configuration is exploited. In figure 2.6 the layout of the integrated Mach-Zehnder[1] modulator is shown. It is the same device presented in [13]. The two arms, the central phase shifting region and the input and output waveguide are clearly visible. The electrodes are implemented as coplanar waveguide to allow traveling-wave operation .

DC characterization.
In order to correctly describe the behavior of optoelectronic devices, both the semiconductor equations and the wave equation must be taken into consideration. For the electrical simulations we have used the state of art ATLAS software [14], which solves the continuity and Poisson equations with a finite-element approach. ATLAS allows the evaluation of all relevant quantities (carrier distribution, electric field, energy band etc.) for each biasing condition. When analyzing the input domain, ATLAS automatically activates the BLAZE module, which is a "general purpose" 2D simulator developed for composite semiconductor devices with position dependent band structure and can be applied to III-V, II-VI materials. Note that at the "meshing stage" the doping-based regrid facility option has not been adopted, since the device structure only includes regions of uniform doping. A concentration-independent low-field mobility has been chosen for the overall domain, since the default parameter values for more complex models are still not suitable for compound materials [14]; the mobility degradation at high "parallel" electric field has been accounted for. Au electrodes have been considered by

[1]The Mach-Zehnder modulator has been realized at the laboratories of Technical University of Eindhoven.

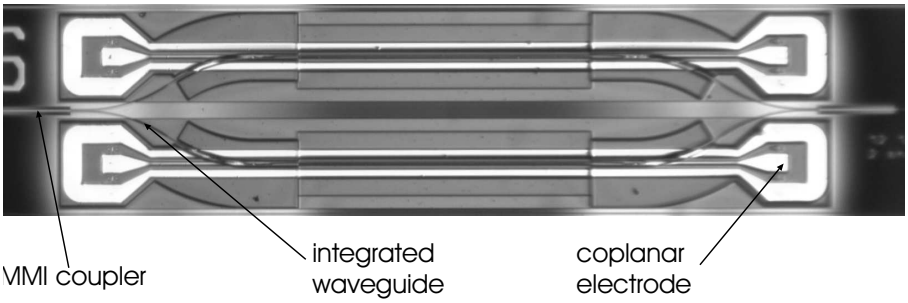


Figure 2.6: Top view photograph of the realized modulator. The phase-shift section length measures 2 mm.

simply forcing a work-function of 5.1 eV. Note that the impact-ionization mechanism is described in ATLAS through the following equation:

$$G = \alpha_n J_n + \alpha_p J_p \tag{2.11}$$

where G represents the total generation rate of electron-hole pairs, α_n and α_p $[cm^{-1}]$ are the ionization coefficients for electrons and holes, respectively, and J_n, J_p $[Acm^{-2}]$ are the current densities. Among the various models available, the formulation proposed by *Selberherr* [15] has been selected. The following expressions are then activated for the electron and hole ionization coefficients:

$$\begin{aligned} \alpha_n &= \mathrm{AN} \exp\left[-\left(\tfrac{\mathrm{BN}}{E}\right)^{\mathrm{BETAN}}\right] \\ \alpha_p &= \mathrm{AP} \exp\left[-\left(\tfrac{\mathrm{BP}}{E}\right)^{\mathrm{BETAP}}\right] \end{aligned} \tag{2.12}$$

being E the electric field in the direction of current flow at a certain position in the domain simulated. Note that a value for a critical electric field, EGRAN, may be defined such as:

$$\begin{aligned} E < \mathrm{EGRAN} \quad (\mathrm{AN}, \mathrm{AP}, \mathrm{BN}, \mathrm{BP}) &= (\mathrm{AN2}, \mathrm{AP2}, \mathrm{BN2}, \mathrm{BP2}) \\ E > \mathrm{EGRAN} \quad (\mathrm{AN}, \mathrm{AP}, \mathrm{BN}, \mathrm{BP}) &= (\mathrm{AN1}, \mathrm{AP1}, \mathrm{BN1}, \mathrm{BP1}) \end{aligned} \tag{2.13}$$

Table 2.1 illustrates the impact ionization parameter values adopted for the electrical simulations. It is noteworthy to observe that, although the depletion region is believed to be confined within the lightly doped ($5 \times 10^{15} cm^{-3}$) N InP region (cathode), it has been proved that, for quite high inverse voltages, it spreads in the $6 \times 10^{16} cm^{-3}$ N InGaAsP region. Therefore, the impact-ionization mechanisms are demonstrated to be relevant also in the quaternary

Table 2.1: ATLAS impact ionization parameter values

Parameter	InP	InGaAsP
AN1	7.03*e*5	7.03*e*5
AN2	7.03*e*5	7.03*e*5
AP1	6.71*e*5	6.71*e*5
AP2	1.58*e*6	1.58*e*6
BN1	0.50*e*6	0.50*e*6
BN2	0.50*e*6	0.50*e*6
BP1	0.50*e*6	0.50*e*6
BP2	0.50*e*6	0.50*e*6
BETAN	1	1
BETAP	1	1
EGRAN	5.00e5	5.00e5

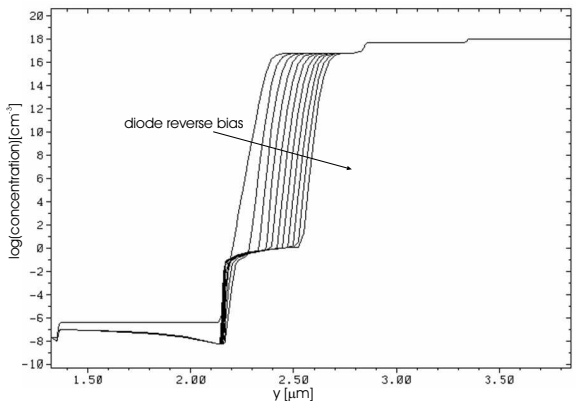
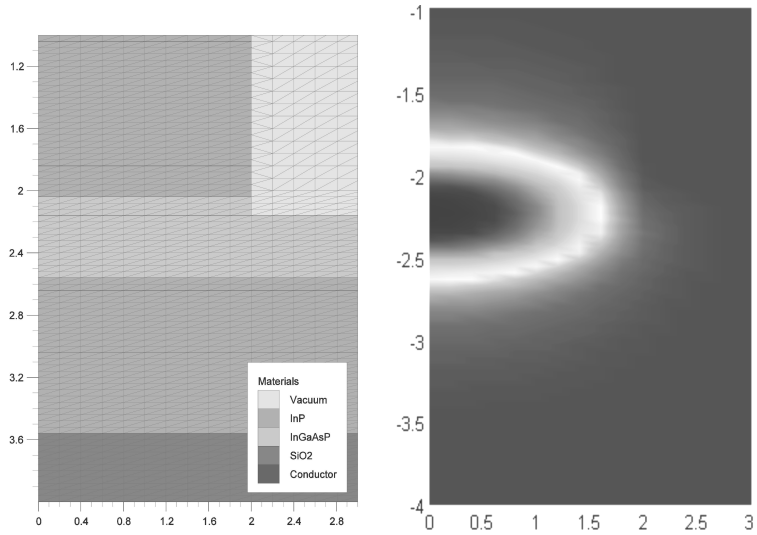


Figure 2.7: Depletion of the electrons in the optical waveguide as a function of the increasing reverse bias.

material when the diode is operating in reverse mode. The calculated electron concentration for different values of the reverse applied voltage is shown in figure 2.7. As expected, as the reverse voltage increases, a depleted region arises at a position corresponding to the guiding layer. In each BLAZE simulation the impact-ionization mechanism has been taken into account.
Once the electrical solution has been obtained in terms of free carriers and electrical field for each bias step (DC analysis) or time step (transient analysis), the refractive index profile is evaluated taking into account free carrier dispersion, band filling and electro-optic effect. The optical wave equation is then to be solved in the cross section to calculate the effective refractive index and therefore the phase shift per unit length. This is the most crucial step in the simulation process because the grid used to solve the electronic problem



(a) Detail of the FEM grid used by BLAZE.

(b) propagating fundamental mode in the waveguide as calculated by FEMLAB.

Figure 2.8: Simulation results.

is usually not suitable for the solution of the optical wave equation. On the other hand, interpolation from one grid to the other can lead to significative numerical errors. Moreover, it is advisable to make use of the same numerical scheme and strategy for Partial Differential Equation (PDE) solution in both the electrical and optical domain. We have developed a suitable numerical code to solve the wave equation using FEMLAB [16] and considering exactly the same grid that ATLAS/BLAZE uses to solve the semiconductor equations. In this way any source of error due to the need of interpolating the FEM grid to a Finite Difference rectangular grid (as used by many commercially available optical simulators) is eliminated; this has proved to be very helpful for both stability and reduction of computational time. In figure 2.8 the grid used during BLAZE analysis is shown together with the refractive index calculated by our in-house code. It is possible to observe that the fundamental mode spot is located exactly in the depleted region (see also figure 2.7) and is laterally confined by the sidewalls of the ridge waveguide. Figure 2.9 illustrates the light phase-shift at the output of one modulator arm as a function of the applied reverse bias voltage obtained through the proposed approach. In order to better appreciate the different physical phenomena involved in the whole phase-shifting effect for the TE-polarized wave, all the four components are provided. The curves confirm what was enunciated in section 2.3.1,

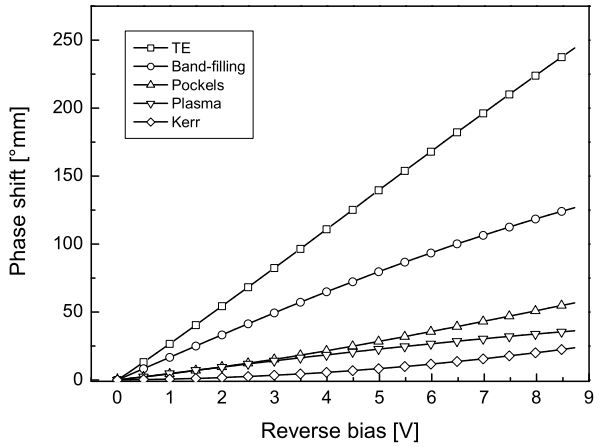


Figure 2.9: Predicted phase shift as a function of the applied voltage for different physical effects.

demonstrating that for compound technologies the effects related to carriers' concentration play an important role on the device operation and cannot be neglected in favor of a simpler linear or quadratic model. It is possible to note that, for a 1 mm-long device and 5.5 V applied reverse bias, a 90° phase shift is obtained. Hence, in order to guarantee a complete switch-off of the light for this bias, a 2 mm-long device or alternatively a higher voltage level is required. However, increasing the driving voltage is a strategy that cannot always be pursued due to limitations in breakdown voltage of high-speed electronic devices. We have also simulated a switching voltage of 11 V for a 1 mm-long phase-shifters and 5.5 V for 2 mm-long phase-shifters. The modulator shown in figure 2.6 has been characterized to compare experimental and numerical results. The measured I-V curve is reported in figure 2.10 while the optical switch curve is depicted in figure 2.11. The latter plot plainly shows an excellent agreement with the predicted switching voltage.

Transient analysis.
In order to verify whether the proposed modulating structure is suitable for fast switching, a transient pulse has been applied and the phase shift has been evaluated. Transient analyses have been performed in inverse operating mode, with and without impact-ionization effects. The analysis has been first performed for a 5 V, 1 ns-long pulse. As can be seen in figure 2.12, the desired phase shift is obtained, while a slight overshoot in the phase shift is observed 400 ns after the driving pulse. Also the observation of turn-on and turn-off times suggests that a much shorter pulse can be applied. The

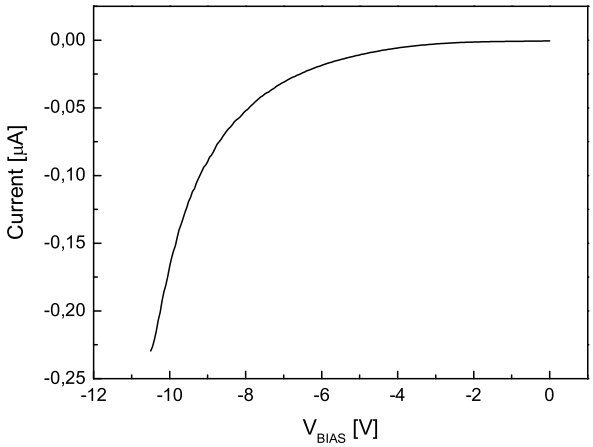


Figure 2.10: Experimental IV curve of the p-i-n diode in reverse bias condition.

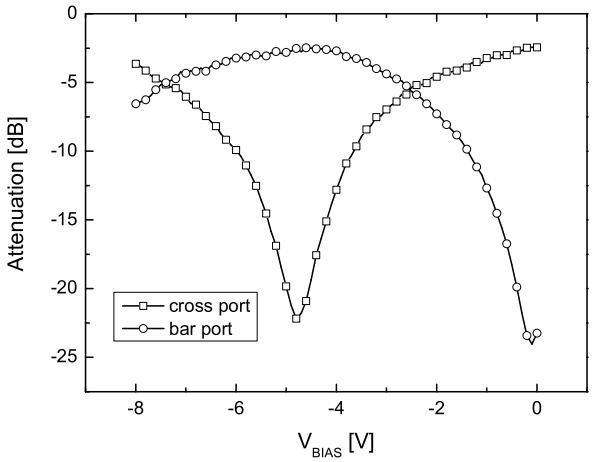


Figure 2.11: Experimental switch curve for a 2 *mm*-long modulator. The voltage corresponding to a complete switching is in good agreement with the predicted one.

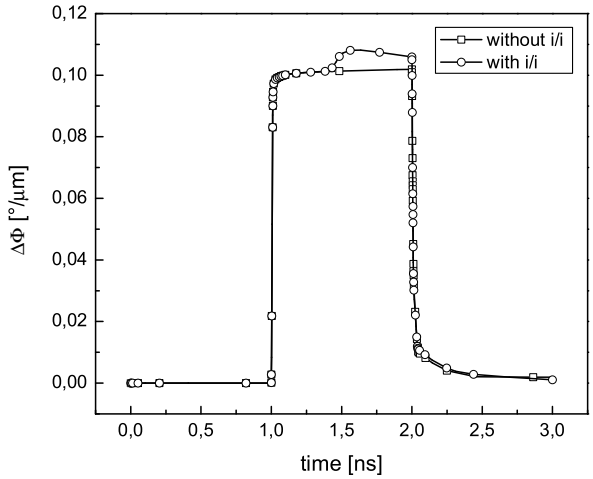


Figure 2.12: Transient phase shift obtained for a 5V - 1 ns-long applied pulse, which corresponds to a data-rate of 1 Gb/s.

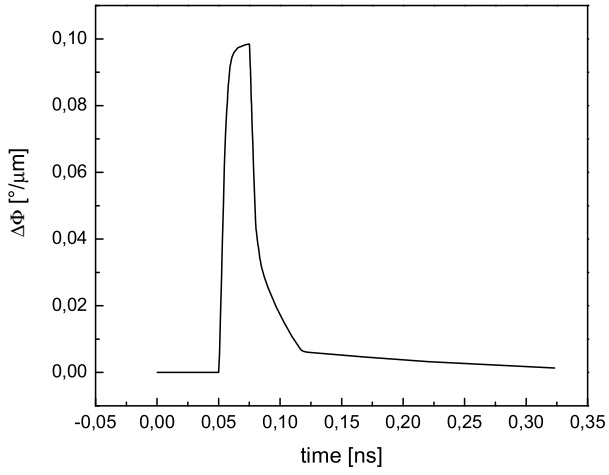


Figure 2.13: Transient phase shift obtained for a 5V - 25 ps-long applied pulse, indicating that the modulator is suitable for 40 Gb/s operaion.

pulse width has been reduced to 25 *ps* while keeping its amplitude constant. The obtained phase shift is reported in figure 2.13, where we again observe that the modulator is still capable of shifting the light beam phase with the required speed, thus resulting suitable for 40 Gb/s operations.

2.3.2 A New Concept Architecture for Mach-Zehnder Modulator

As mentioned, the Mach-Zehnder interferometer is the most commonly used configuration for integrated electro-optic modulators. In order to improve the device speed, Mach-Zehnder modulators (MZM) are often implemented in a traveling-wave configuration, with the electrode designed as a transmission line, namely a coplanar line, with the same characteristic impedance of the driving system. In this way, the electrode capacitance is distributed along the transmission line and does not limit the bandwidth of the driver, thus alleviating the driver design requirements. However, a proper design of the electrode is of paramount importance for high modulation efficiency. By recalling the expression of the phase modulation depth:

$$\frac{\sin\left(\frac{\pi f_m |n_0 - n_\mu| L}{c}\right)}{\frac{\pi f_m |n_0 - n_\mu| L}{c}} \tag{2.14}$$

where f_m is the modulating frequency, n_0 and n_μ are the optical and the microwave refracting index, respectively, L is the length of the phase shifting section and c is the free-space velocity of light [7], it is possible to note that the maximum of the modulation depth, and hence of the electrical bandwidth, is achieved when the optical refractive index matches the microwave one. Depending on the properties of the optical material, the matching of the refractive indexes, and then of the group velocities, can be pursued in two ways, namely increasing or decreasing the velocity of the microwave modulating signal [6]. However, it is rather troublesome to obtain simultaneously an impedance and a velocity match. Furthermore, the intensity of the modulating signal decreases as it travels along the electrode. The solution proposed to tackle these problems is based on the replacement of the traveling wave electrode with a series of lumped electrodes, each of them providing a limited value of phase shift. The electrodes are then plugged at the current injection nodes of a distributed amplifier (see section 5.1.2) and are connected by the artificial output transmission line of the amplifier (figure 2.14). The electrode can be modeled as a lumped capacitor and the value of the inductance for the artificial collector line needs to be modified in order to keep constant the

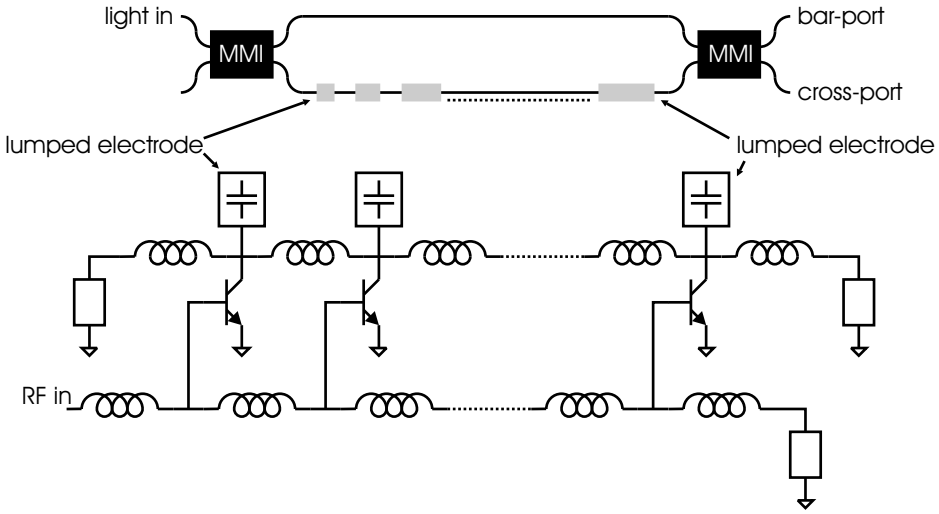


Figure 2.14: Proposed architecture of an hybrid flip-chip module. The 50 Ω matching and velocity matching constrains can be alleviated by using a distributed approach for the electrodes.

delay between each stage of the amplifier. Since the phase shift in the guiding section under each electrode is proportional to its applied voltage and the voltages on the electrodes are not equal, it is important to carefully optimize their number and spacing in order to achieve a correct phase shift between signals propagating on the arms of the modulator. The phase shift can be roughly approximated as:

$$\Delta\phi = \beta_0 L - \beta_0 x N - \sum_{i=1}^{N} \beta_i l_i \tag{2.15}$$

where L is the total phase shift section length, l is the electrode length, x is the distance between two electrodes and N is the number of electrodes. Since $\beta_i = \left(\frac{2\pi}{\lambda}\right) n_{effi}$, it is important to exactly evaluate n_{effi} of the wave-guide section lying under each electrode. This can be accomplished by using the simulation strategy presented here. As detailed in the following of this thesis, it is important to remark that this strategy can alleviate the design of the driver since its load impedance is no longer set by the modulator electrode characteristic impedance. The termination of the collector line could, in principle, be optimized to achieve the same modulating voltage with a reduced number of stages.
As a final step, the photonic device can be directly flip-chip mounted (see section 3.1) on a silicon substrate to realize a fully packaged optical transmitter.

Chapter 3

A Technology for Packaging of Opto-IC Systems

It is not hard to be impressed with the progress that has been been achieved in optoelectronics over the last few years. Optical fiber is now the transmission medium of choice throughout the telecommunication systems in the world. It is also rapidly penetrating many other fields that have hitherto been the domain of conventional electronics, for example microwave systems, computer interconnects and local area networks. Given the enormous benefits of optical technology (including superior electromagnetic compatibility, low loss, highly flexible fibers, low mass, wide temperature range, wide bandwidth and low dispersion), a critical issue in the mass-production of all-optical systems is represented by the difficulties in interfacing such systems to optical fibers (or as well to other systems) in a convenient way and within a recognized package practice.

In designing the package of an optical device, all the factors that affect conventional electronic devices need to be considered: mechanical integrity, hermeticity, electrical parasitics, thermal impedance and so on. Indeed, some of these criteria can be quite stringent. Package parasitics are of utmost importance for an integrated optical modulator operating at 20 GHz, while the thermal impedance is critical for a semiconductor laser chip where the injection current density in the laser junction can be several $kAcm^{-2}$. The optical device is, however, unique in that extremely tight physical alignment tolerances are mandatory. In order to achieve high coupling of optical power from an integrated optical waveguide, i. e. from a matrix switch or an high-speed modulator to an optical fiber, the lateral or vertical displacement from the optimum position must be less than $\sim 1\ \mu m$. For a semiconductor laser with a near field spot size of $\sim 1\ \mu m$, the tolerance is only $\sim 0.2\ \mu m$ [17]. These tolerances are much tighter than in other field of electronics and they

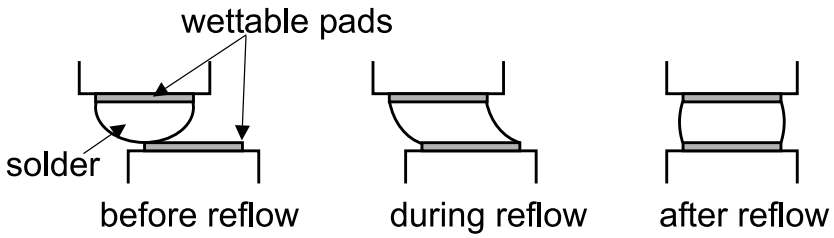


Figure 3.1: Sketch of the self-alignment mechanism during the bonding process.

are responsible for the large part of the relatively high cost of modern high-performance optoelectronic parts. To achieve high coupling efficiency, a substantial degree of manual adjustment is needed during final assembly, which leads to high costs. Furthermore the device typically has to be operational during the final assembly. If machine vision equipment and sophisticated robotics are used to assist or replace the operator, the number of production units needed to justify the capital investment can be very high. Fortunately, an alternative method of assembly for optoelectronic components is capable of achieving tight assembly tolerances ($< 1\ \mu m$) without manual adjustment during finally assembly. This method is the flip-chip solder-bump bonding.
In this chapter, after a brief overview of flip-chip technology, the custom technology developed at DIMES-TUDelft laboratories will be detailed, together with some examples of silicon-indium phosphide hybrid modules for optoelectronic applications.

3.1 Flip-Chip Technology

Flip-chip solder was introduced in the mainstream of electronics by IBM more than thirty years ago [18] under the name of C4 (Controlled Collapse Chip-Connection). The solder bond technique makes use of a precise volume of solder confined between wettable metal pads of known area on each side of the bonds (figure 3.1), these pads being surrounded by regions that the solder does not wet. When the temperature is raised to the melting point of the solder, surface tension tends to bring the structure into alignment. Several hundred of pads can readily be used to join the two chips with tight self alignment. The final position is the one that minimizes the total energy of the system, i.e. the position of greatest symmetry. On cooling, a very secure and precise unit is formed, with excellent mechanical and electrical properties. The critical step in the process is the formation of the solder bumps,

because the bump alloy sets the melting temperature of the metal connections.
Before detailing the different deposition techniques, it is important to describe the importance of the under-bump-metallization (UBM). A proper UBM should provide good adhesion to the wafer passivation and good adhesion to the IC final metal pad. At the same time, it has to behave as a solder diffusion barrier in order to avoid contaminations. Finally, the metal combination must have a low resistance in order to reduce the electrical losses. Several processes have been demonstrated to deposit solder bumps on wafer or substrate. The most common are [19]:

- evaporation
- electroplating
- printed solder bump formation
- solder wire bumping (or "stud bumping")

The choice of the technology is influenced primarily by the bump dimensions and pitch, composition and costs.

Evaporated bumps. Evaporation can provide bumps with the best uniformity in composition and volume. The most commonly used evaporated bumps are those based on the PbSn (e.g. IBM C4 process) deposited on a wafer through a molybdenum metal mask. The molybdenum metal masks are first aligned to the bond pads on the wafer and clamped. The assembly is then mounted into an evaporator to deposit the bond pads. For interconnection systems such as C4 this metallization consists of chromium, copper and gold. Following the metallization, the wafers along with the shadow mask assembly are transferred into a solder evaporation system. Here a known composition and volume of solder is evaporated onto the bond pads. The shadow mask is then removed. Obviously, the metal mask technology influence the minimum size and pitch capability of evaporated solder bumps. Typical values are 100 μm diameter and 250 μm pitch.

Electroplated bumps. The electroplating process involves the following steps. First, the wafer with devices is metalized in such a way to provide a current path to the individual bond pads. Two approaches are commonly used for this purpose. In the first, metallization traces are patterned between the die to the bond pad. In order to electrically isolate the bumps after the plating process, these traces are cut during the dicing operation. This

method of metallization typically provides uniform plating heights with relatively good process control. However, such a method requires an additional patterning step, and it might not be desirable for chip designs with bumps in the interior of the die. The alternative approach is to deposit a blanket metallization on the entire wafer. This metallization is called the *bus* ot the *seed* metal. After the plating step, the seed metal is etched away to isolate individual bumps.
Following the deposition of the seed layer, the wafer is patterned with photoresist in such a way that the seed metal is exposed in the regions where the bump is desired. The photoresist process often determines the geometry and pitch limitations of plated bump technology. The wafer is then mounted in a plating bath and a static or pulsed current is applied with the wafer as cathode. The time for which the current is applied generally determines the thickness of the plated bump. If the bump contains more than one material, the electroplating process can be repeated for each metal in the bump. The typical pitch and diameter range for electroplated bumps spans from 200 μm down to 25 μm.

Printed bumps. Printing of bumps using either stencil and screens has traditionally being used in the surface mount industry. More recently, advances in the stencil technology and pastes have extended this technology to flip-chip applications, particularly to coarse pitch (> 600 μm) applications. Applications of this technology to finer pitches require further refinements in stencil and screen technologies, and solder paste development. Printing processes typically involve three steps. The paste is first pushed into the holes in the stencil or screen by a squeegee. It then makes contact with the bond pads on the substrates. Then the paste is transferred to the substrate while the stencil retracts. Finally, the paste bump is pre-baked in order to retain its shape during handling. The rheology of the paste, the print speed and the separation between the stencil (or screen) and the substrate are some factors that affect the printed bump geometry and uniformity.

Solder wire bumping. Wire bumping is a relatively low-cost alternative for low-volume prototyping applications. In this approach, a thermosonic bonder is used to deposit solder wire bumps directly on aluminum. The wire is then broken to form a tailed bump. In this approach, the bond pad metallization step can be eliminated reducing the number of process steps required. Furthermore, this wire bump may be reflowed and processed as any other solder interconnect. The size and pitch capabilities of the wire-bumping process are limited by the diameter of the wire and the alignment capabilities of the wire-bumping equipment.

Regarding the reflow process, in general solder bumps are reflowed twice during the process flow. The first reflow step occurs immediately following the bumping process. The second reflow occurs after the die placement during flip-chip bonding process. During the reflow process the solder bump is heated to a temperature above the melting point of the solder alloy. When the solder melts, it forms a metallurgical bond with the bond pad metallization. For lead-tin solders, this operation can be performed in a reducing atmosphere such as hydrogen or nitrogen-hydrogen. For other solders, such as those based on indium, a flux may be required.
In bumping operations such as plating or evaporation, the surface of the bump is often oxidized: the reflow operation reduces the oxide from the surface. In addition, the reflow processes promote uniformity in the solder composition and heights. The reflow temperature profile can influence the kinetics of the reaction of the solder composition with the metallization. Typically a peak temperature between 10 and 50 $°C$ above the melting point is used. At low temperatures the rate of melting of the solder can be slow, resulting in poor ball formation and height nonuniformity. At very high temperatures, the solder might react extensively with the bond pad metallization, resulting in intermetallics and even dewetting. Extensive intermetallic formation can be deleterious to the reliability of the interconnect. The choice of the environment or the flux for bump reflow is determined by the composition of the solder bump. Fluxes commonly contain three constituents: a solvent (e. g. alcohol), a vehicle (e. g. a highly boiling point solvent) and an activator (e. g. carboxylic acids). The solvent facilitates uniform spreading of the flux on the bond pads.
The reflow process usually consists of preheat step where the solvent is vaporized. This promotes a uniform coating of the flux on the solder and bond pad metallization. The flux also becomes more viscous and tacky. Further increase in temperature causes the vehicle to flow along with the activator. The activator reduces the oxides, while both the vehicle and the activator volatilize. Flux residues commonly contain residues from the carrier, the wetting agent and reaction by products of the reduction agent. These can be cleaned using a variety of organic and inorganic solvents. Environmental concerns[1] and cost factors has resulted in the development of some fluxless processes.

[1]Montreal protocol of November 25, 1992 [20]

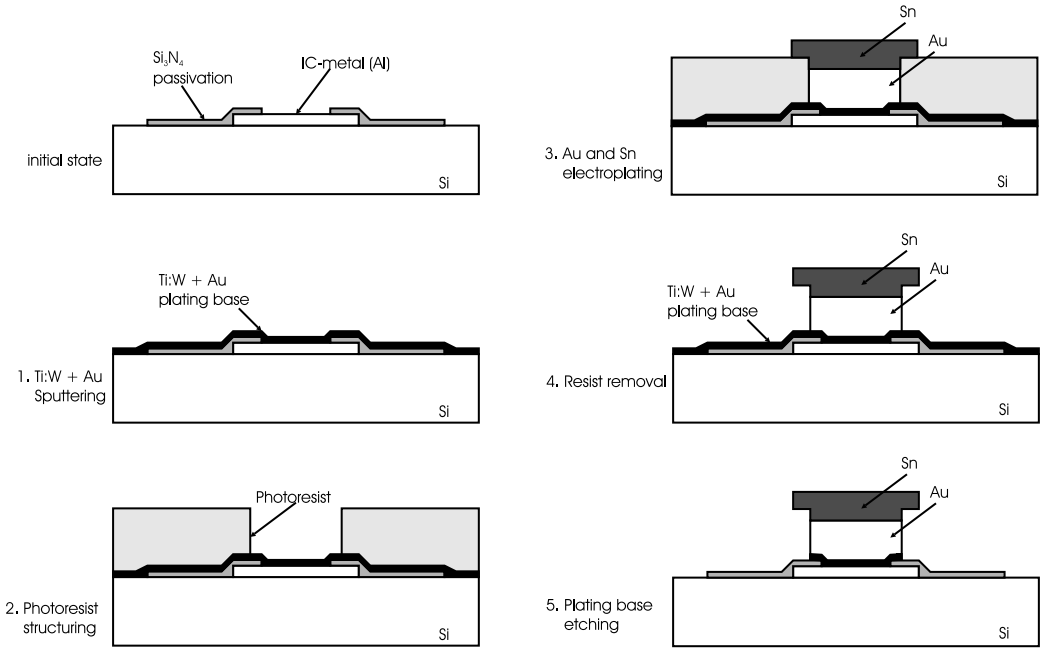


Figure 3.2: Flow-chart of the bumping process developed at DIMES laboratories.

3.1.1 The DIMES electroplating process

In order to bond indium-phosphide chips onto a silicon substrate, a custom deposition process has been developed at DIMES laboratories at the Technical University of Delft, in the Netherlands. The main issue in the development of the process was related to the need of achieving very low diameters and pitches for the solder bumps in order to be compatible with the pre-existing metal pads on the optical chip. Moreover, the photonic chips were already diced and therefore they were not suitable for further processing, so the bumps have to be realized on the silicon carrier. Regarding the metallization alloy, the silicon wafers have aluminum pads and an inorganic (Si_3N_4) passivation opened over the pads. InP photonic chips are covered with gold as pad metal so a bump alloy that is able to wet gold was mandatory. Due to all those constrains, an eutectic 80/20 tin-gold has been selected. The flow-chart of the process is given in figure 3.2.
By an initial sputter etching step, the wafer surface is cleaned to remove contamination and metal oxides. Without braking the vacuum, an adhesion layer of Ti:W with a total thickness of $50nm$ ($10nm$ Ti followed by $40nm$ of W) is sputtered on the whole wafer, followed by a second layer of 300 nm

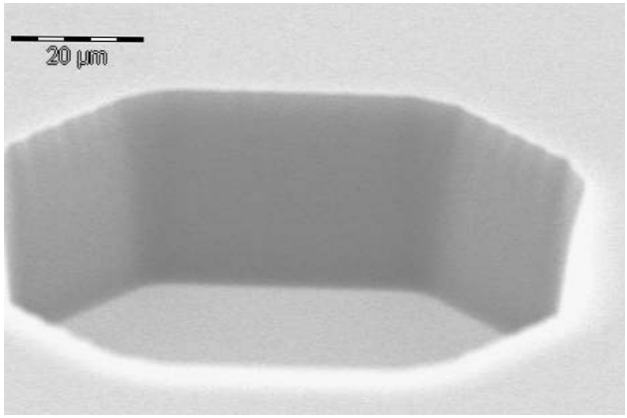


Figure 3.3: Openings in the photoresist for straight-wall bumps.

Au as a plating base [2] (step one in figure 3.2). The Ti:W layer has a double function: it serves as an adhesion promoter to the Al pad and as a diffusion barrier avoiding aluminum-gold interdiffusion. It also presents high thermal stability, low contact resistance and good adhesion properties to the adjoining layers. After the UBM deposition, an high viscous photoresist has been used to produce resist layers of 5 μm up to 30 μm. As in solid state technology, spin-coating is used to deposit the photoresist onto the wafer in the desired layer thickness. After treating the silicon wafers with HMDS vapor to improve the adhesion on the surface, a layer of 30 μm has been realized by multi-spin-coating AZ4562 photoresist at 400 rpm. The positive AZ resist system was used due to its high transparency in the near UV spectrum. Therefore, a high depth-to-width aspect ratio and steep slopes of the generated structures are possible even in thick films. To dry the coated resist film, stabilize it mechanically on the wafer and reach its final photosensitivity, the photoresist is pre-baked at 90 $°C$ for $\sim$ 30 min before exposure. To prevent drastic thermal stress, the temperature is ramped down in 45 min. The pad mask is then exposed with energy of $\sim$ 3600 mJ/cm^2. The exposed area dissolves during the development in an alkaline solution and the resist pattern appears (step two, figure 3.2). A final one hour postbake at 110 $°C$ is made to fix the photoresist so that it will get through the following electroplating process. Figure 3.3 shows a SEM photograph of the walls of the openings, where it is possible to note the steep sidewalls. This sequence of exposing, developing and baking steps is crucial to get a high lithographic performance.

[2]This process step has been done at the Thin Film Facilties (DTS) Philips Research Labs in Eindhoven, The Netherlands, since the gold target for the sputter machine was not available at DIMES.

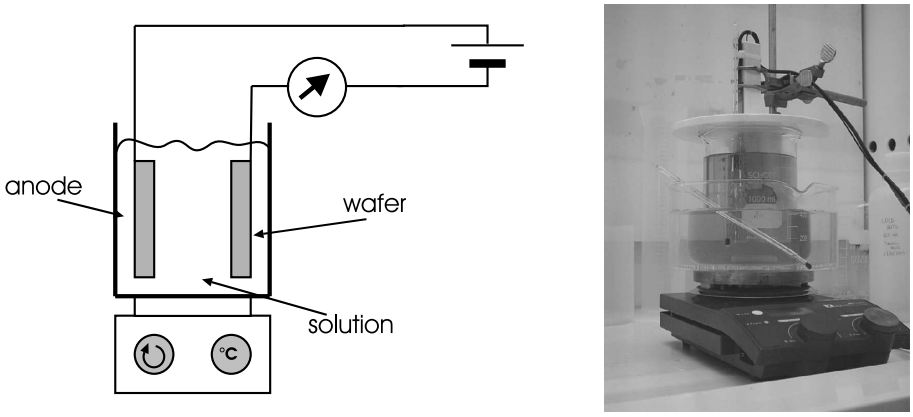


Figure 3.4: Au-plating setup: schematic and picture. The anode is made by platinum while the cathode is the wafer.

Obviously, besides the structurability, another important aspect for the suitability of the photoresist for bumping is its easy removal after the metal deposition. Before electroplating, the wafer are cleaned in a weak acid solution to remove possible resist residues, which may cause a reduced adhesion of the bumps, an increased contact resistance and an inhomogeneous growth of the electroplated gold layer.
The plating equipment for the gold deposition is given in figure 3.4. The Au-plating solution in the bath, namely *MICROFAB AU-100* [21], is a sulfite-based electrolyte [22]. Plating is done from the solution, which eliminates the need for a gold electrode. However a Pt anode is used to apply the potential, as seen in figure 3.4(a). In order to achieve an uniform growth of the bumps, an optimal current of 4 mA/cm^2 has been found. At this current density plating rate is 1 μm in 4 minutes. The thickness required is ~ 25 μm, which leads to a total plating time of 100 minutes. Other process parameters are the temperature of the plating solution and the speed of the magnetic stirrer inside the bath. Also these parameters have been optimized, resulting in 60 $°C$ and 400 rpm, respectively. During the plating, special precautions, like gently shaking the wafer, have been used in order to facilitates the removal of bubbles at the seed layer - solution interface. In this way reproducible gold pillars of 25 μm have been realized. The tin plating is performed after the gold plating by using the same seed layer. The Sn-plating solution, namely *STANNOSTAR A300* [21], operates at room temperature. Sn is plated from the anode through the electrolyte solution in this case and therefore an Sn block is used as the anode. Current density for plating is 8 mA/cm^2 and

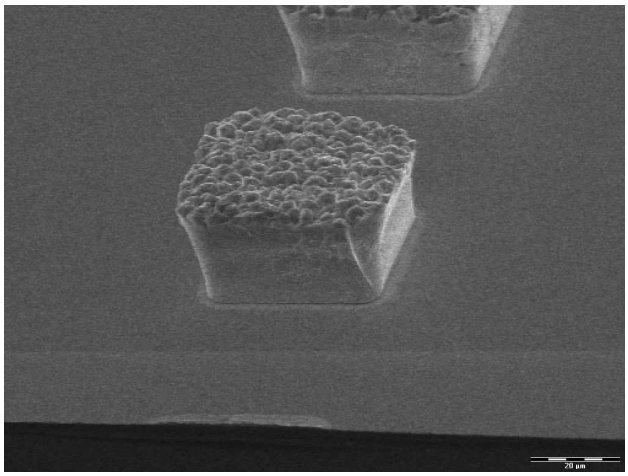


Figure 3.5: SEM image of $40 \times 40 \mu m$ pillars.

plating rate is 0.3 $\mu m/minute$. The thickness is desired to be ~ 10 μm, resulting in a plating time of 1 minute. Total thickness of the plated pillar is ~ 35 μm. This is ~ 5 μm more than the photoresist thickness, leading to a mushroom like shape as depicted in the process flow (step three, figure 3.2). However the shape changes to a hemisphere. Therefore initial shape of the pillar is not so important.
After electroplating, the photoresist is removed in acetone (step four, figure 3.2). The plating base of Au and Ti:W are then selectively etched by using a wet-etching technique. First, Au is etched in a $KI : I_2$ solution that has $7g : 1g$ of KI and I_2 respectively in 1 liter deionized water. Etching time is approximately 3 minutes. Then Ti and W are etched at the same time in 30% H_2O_2 solution heated up to 40 $^\circ C$ in 90 seconds. A SEM picture of one of the resulting pillars, which are the end product of silicon wafer process, is given in figure 3.5. It is worth to mention that in our situation, the top wafer is the InP chip most of the times. However, in order to perform some initial test, silicon chips were realized to be flip-chip mounted on the silicon carrier. General requirement was a gold coated pad. Gold is preferred for its wettability and oxidation free surface. In this case, gold can be very thin compared to the carrier wafer. Generally a layer thicker than 1 μm is sufficient. The layer should also be provided with an adhesion layer and a diffusion barrier. We used again sputtered Ti:W/Au seed layer with a $5 - 10$ μm thick photoresist mold and $3 - 5$ μm Au pads. Also for the dummy silicon chips, photoresist and seed layer were removed with the process described above.
Bonding can be done in two ways. A first way is to bond directly during reflow. The second one is to perform an additional heating process for bonding

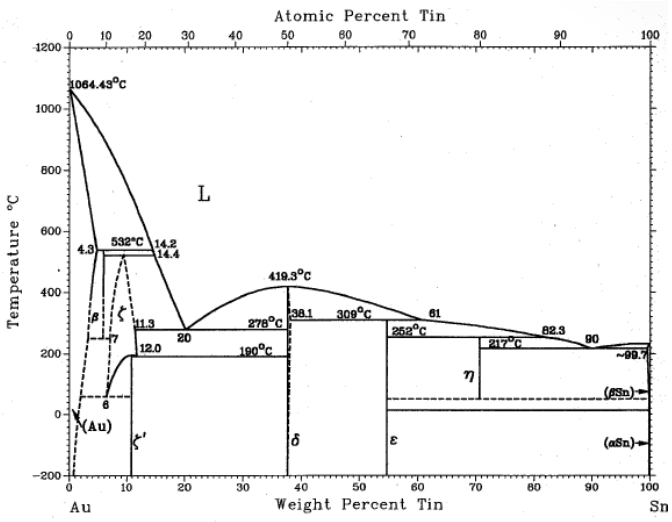


Figure 3.6: Equilibrium phase diagram of Au/Sn system.

after the reflow process. The second method improves the height uniformity of the bumps. This ensures a better bonding quality throughout the wafer. Both steps include a reflow step. In this step the carrier wafer is heated up to 310 $°C$, which is $\sim 20\ °C$ higher than the eutectic Au/Sn 80/20 alloy melting temperature of 290 $°C$, as can be seen in the the equilibrium phase diagram of the Au/Sn system (figure 3.6). From the equilibrium phase diagram of the Au/Sn system, it is possible to identify two eutectic points, each corresponding to a precise reflow temperature [23]. The heating process must be performed in a very short time to prevent premature diffusion of Sn into gold without melting that would prevent the bump taking the hemisphere shape that is the crucial point in improving uniformity. Therefore a rapid thermal annealing (RTA) oven with a controlled nitrogen atmosphere was used. The temperature profile of the RTA is given in figure 3.7. The whole reflow process is performed in a few seconds. By melting, the deposited mushroom-like shape of the pillars changes into a hemispherical form. The result of the reflow step is given in figure 3.8(a). The bump size is $40 \times 40\ \mu m$ with a thickness equal to 30 μm as desired. The good uniformity along the wafer can be appreciated by looking to one dimensional arrays of bumps (figure 3.8(b)) or to a bump matrix (figure 3.8(c)). All the bumps are $40 \times 40\ \mu m$ in size, and a pitch of 90 μm has been proven to be large enough to avoid short circuits. The alignment between the chip and the substrate has been done in a normal pick-and-place machine. This machine was adapted to flip-chip bonding and then it did non allow for a very precise alignment. The final bonding has been performed again in a RTA oven, with a temperature profile similar that

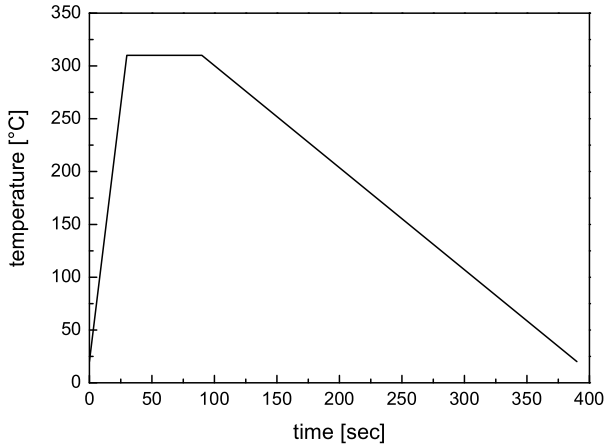
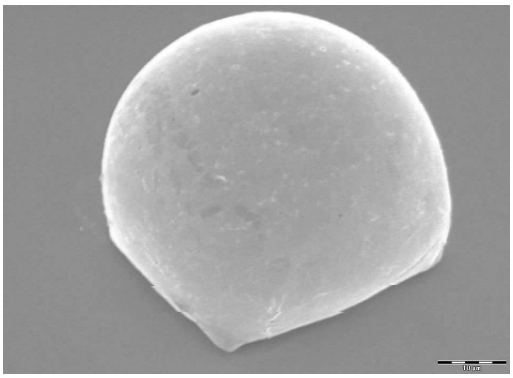


Figure 3.7: Temperature variation in the reflow cycle in rapid thermal annealing device.

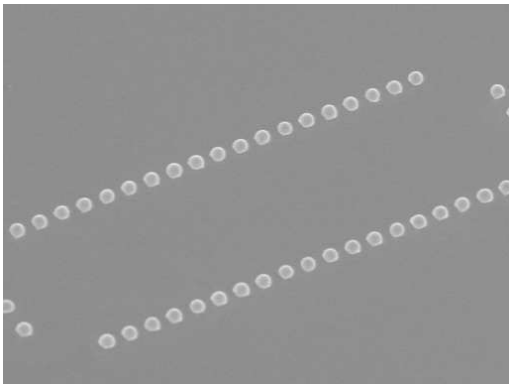
shown in figure 3.7.
To test the process with real chips, a test substrate has been designed. Figure 3.8(d) shows a picture of the bumped silicon substrate with metal traces on it. The resulting bonding is given in figure 3.9. In the next section, examples of successful bonding of InP photonic chips on a proper silicon carrier will be presented, together with some simulation results and suggestions for future applications.

3.2 Flip-chip Packaging of Photonic Devices

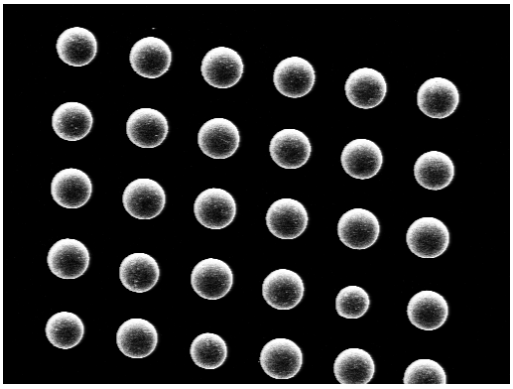
Flip-chip bonding permits an efficient combination of device technologies to be employed in creating high-performance components. GaAs, InP and Si can all be employed, thus permitting, for example, VLSI circuits to have direct optical interfaces, or long wavelength optical component on InP to use high performance GaAs or Si interface chips. In many case, only minor additions to the standard foundry processes are needed in order to make use of this technique. The flip-chip technique has excellent characteristics for being used in high-speed systems, since the parasitics inductance and capacitance of the bonds is much lower compared to conventional wire bonds (and it is also more reproducible). It represents therefore a natural choice for high-speed applications such as photodetectors and modulators. The solder bond technique is also particularly favorable when an array of devices is to be bonded, because electrical connections can be made everywhere on the device surface rather than being limited on the edge.



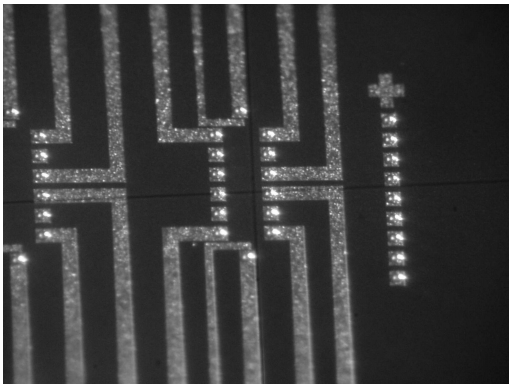
(a) SEM image of a Au/Sn bump after the reflow process.



(b) SEM image of 1D bumps arrays. The good uniformity is clearly visible.



(c) SEM image of a square bump matrix. The pitch is 90 μm.



(d) Microphotograph of the bumped silicon test substrate.

Figure 3.8: Realized eutectic Au/Sn bumps.

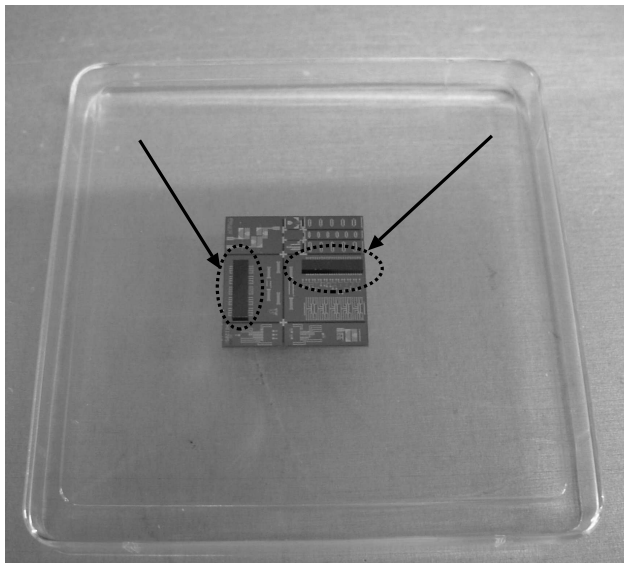


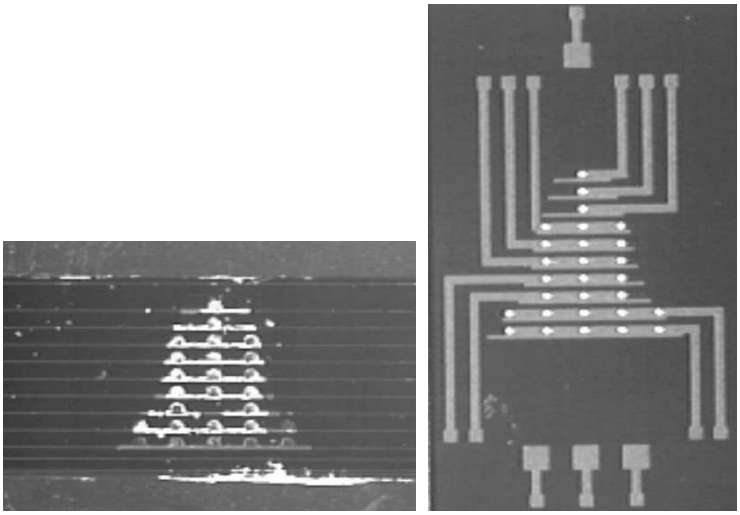
Figure 3.9: Realized silicon dummy carrier with flip-chip mounted silicon chips.

As previously mentioned, the solder bumper approach is compatible with a wide range of different device technologies and materials. It is therefore an attractive means of constructing hybrid assemblies involving silicon integrated circuits, GaAs MMICs and optoelectronic devices based on GaAs or InP. This flexibility opens up a range of new possibilities, particularly in the application of optoelectronics to short-distance interconnections between electronic subsystems (at chip or board level). This is because a very large amount of power is often dissipated in the interface circuits of high-performance computers, in particular in driving data bus lines at very high bit rates. Optoelectronic interconnects can reduce this dissipation considerably and also alleviate the bandwidth limitations of conventional interconnects schemes: practically, it is possible to add optical ports directly to a silicon IC.

By applying the process described in the previous section, two photonic chips [3] have been successfully integrated on a silicon carrier [4]. The two chips contain some integrated semiconductor optical amplifier (SOA) and some optical demultiplexer (PHASARS). These samples represent an attempt of supporting the photonic functionalities from the silicon carrier: in the first case, a chip containing several SOAs of different length (the layout of the

[3]The InP chips have been produced by the Opto-Electonic Device (OED) group of the Eindhoven University of Technology, The Netherlans

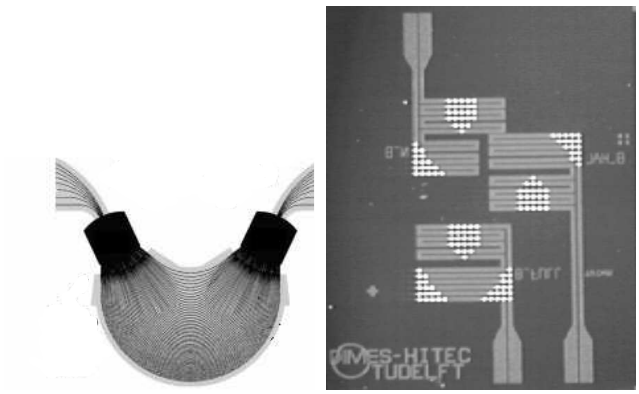
[4]The silicon samples and the flip-chip bonding has been made possible at DIMES laboratories at the Technical University of Delft, The Netherlands



(a) layout of the optical chip (b) layout of the silicon carrier

Figure 3.10: Sketch of the thermally enhanced SOA module

chip is given in figure 3.10(a)) has been mounted on a proper designed silicon substrate (figure 3.10(b)) in order to improve its thermal stability. This is because the thermal impedance of the bumps-silicon system is lower than that of a III-V substrate. Also, the InP chip fragility causes difficulties in probing the SOAs with DC needles. By mounting the test chip on the silicon carrier is possible to overcome this practical problem because all measurements can, in principle, be done by probing the metal pads.
In the second case, the goal is to compensate the offset in the wavelength selectivity of a PHASAR by controlling its temperature. The heat is generated on the silicon carrier by DC biasing a metal resistor and then transferred to the optical chip via the metal bumps. The optical chip and the carrier layouts are given in figure 3.11(a) and 3.11(b) respectively. Pictures of the realized flip-chip hybrid modules are shown in figures 3.12 and 3.13.
Since at the time of writing this thesis it was not possible to have the support of measured data, in the next section the proposed experiments will be detailed and motivated by a theoretical analysis and by simulation results. However, the investigation presented below is to be regarded as a starting point for future developments.



(a) layout of the optical chip

(b) layout of the silicon substrate

Figure 3.11: Sketch of the temperature controlled wavelength demultiplexer.

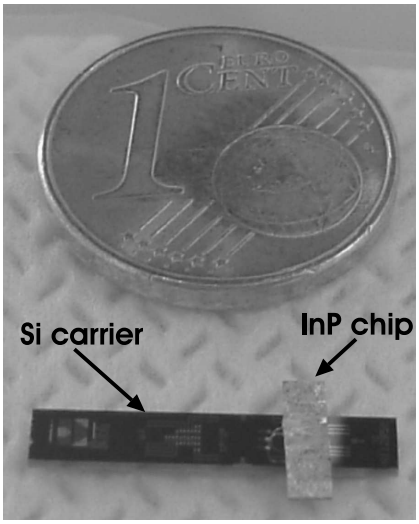


Figure 3.12: Photo of the realized SOAs module.

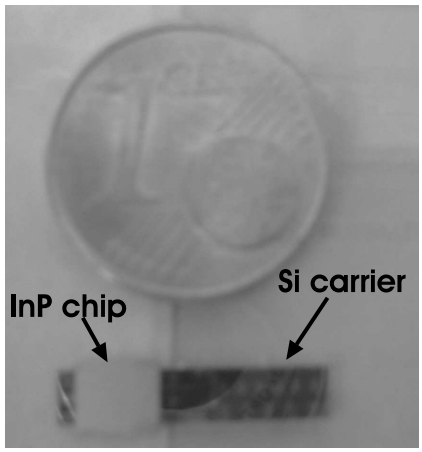


Figure 3.13: Photo of the realized SOAs module.

3.2.1 Thermal Management of Integrated SOAs

Semiconductor optical amplifiers are key components for the monolithic realization of complex lightwave functionalities, being widely employed as high speed gates for all-optical routing and switching in dense wavelength division multiplexing (D-WDM) networks, as well as integrated light sources or amplifiers. The implementation of a variety of functions requires the integration of multiple SOAs on the same chip. One shortcoming lies in SOAs' performance and reliability limitations due to thermal effects. The most critical issue is the increase in the operating wavelength with temperature [17]; other temperature-sensitive parameters include the threshold current of semiconductor lasers and amplifier gain [24], along with the mean time between failures (MTBF). The mentioned effects are exacerbated by the close proximity of many optical amplifiers, which makes thermal management an important aspect to account for when designing a photonic system package. A viable low-cost solution is to flip-chip package the photonic device onto a low-thermal impedance substrate like silicon [25], via metal bumps: this provides mechanical support as well as the possibility to integrate complex electronic driving circuitry. This section focuses on the thermal analysis of flip-chip mounted semiconductor optical amplifiers. Wi will present a brief overview of how flip-chip technology can be used to reduce the thermal impedance of a photonic chip. Next it will be detailed a semi-analytical approach for evaluating heat distribution in flip-chip systems. Based on the Green's functions method, it yields an exact solution of the heat transfer equation in each subdomain, while continuity conditions between adjacent subdomains are numerically imposed. This procedure is advantageous compared to rude-force

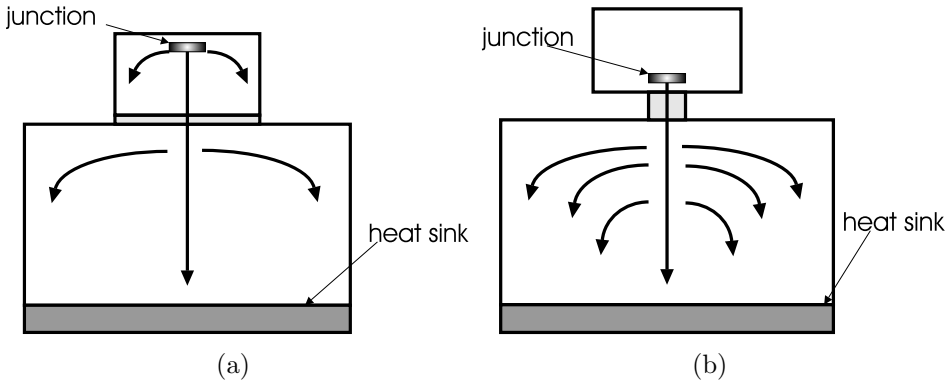


Figure 3.14: Different heat flows for the (a) junction-up and (b) flip-chip mounting techniques.

finite element (FE) simulations, which requires considerable effort and adequate skills in order to properly generate a convenient mesh [26], owing to the very thin geometries of photonic devices, like laser junctions, whose thickness is negligible compared to their planar dimensions and to the substrate size. Besides, FEM simulators require a long computation time to perform 3-D transient analysis on a wide time span with numerous time discretization points. In order to efficiently calculate the derived equations, a MATLAB routine has been developed for the 3-D transient simulation of flip-chip structures. Different geometric layouts and bump materials are accounted for, and the dependance of the thermal behavior on geometric parameters is clearly displayed and discussed. This analysis points out some design rules, which provide useful guidelines for flip-chip design improvement.

Two ways are currently used for mounting a chip onto a heat sink, i.e., the junction-up and the flip-chip [27] techniques. As displayed in figure 3.14(a), in the junction-up configuration the SOA is bonded onto the carrier by means of an eutectic alloy (usually gold-tin) and the active layer is located opposite to the heat sink. Thus, heat conduction occurs mainly through the III-V (InP or GaAs) substrate, whose poor thermal conductivity results in a relatively high thermal resistance of the structure; the thermal resistance is further increased by the proximity of the heat source to the top adiabatic surface. Nevertheless, due to its simplicity, this scheme is widely used in low power laser device industry. Conversely, the flip-chip technique, as illustrated in figure 3.14(b), has the advantage that the junction is much closer to the heat sink, which favors the excess heat removal. Moreover, the thermal conductance of the metal bonds is lower than that of the thick bulk III-V substrate, whence a lower overall thermal resistance. The interconnects between the

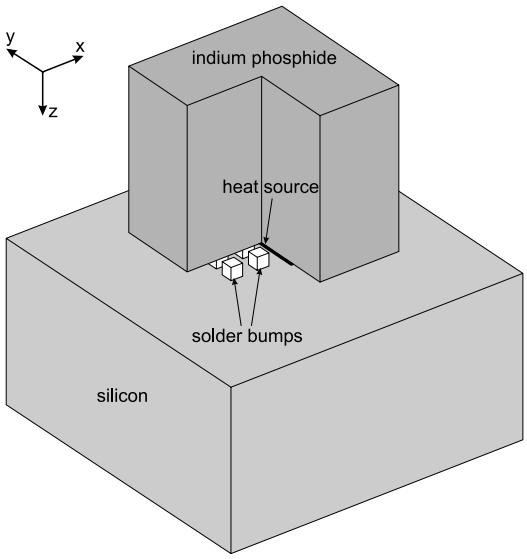


Figure 3.15: Flip-chip schematic structure drawn to scale.

chip and the submount are usually fabricated by electroplating soft gold-tin alloy bumps. Besides the good heat conduction characteristics, this material is preferred since it allows a precise height control during the bonding process, and because it absorbs the mechanical stress related to the difference in thermal expansion coefficients of the substrates. By means of this technology, InP based SOAs have been successfully integrated on a silicon platform [28, 29].

The analytical formulation

As a first step, due to the inherent symmetries we can restrict our analysis to only one quarter of the structure shown in figure 3.15; considering adiabatic conditions (i.e., with zero heat flux) at the symmetry planes virtually restores the missing parts. The resulting domain is then subdivided into four blocks, namely the InP layer containing the heat source, two bumps (taken as rectangular parallelepiped), and the silicon substrate. Four interfaces can be spotted between the InP block and each bump, and between each bump and the silicon substrate. A time-dependent formulation of the temperature field has been derived by means of the Green's functions approach for each subdomain. One can conveniently refer to the temperature increase above ambient, defined as

$$\theta\left(\vec{r},t\right) \triangleq T\left(\vec{r},t\right) - T_{AMB} \tag{3.1}$$

The temperature distribution in the InP substrate can be expressed as [30]

$$\theta_{InP}\left(\vec{r},t\right)=\theta_{InP,g}\left(\vec{r},t\right)-\theta_{InP,b.c.}\left(\vec{r},t\right) \tag{3.2}$$

Being $\theta_{InP,g}\left(\vec{r},t\right)$ the contribution due to the volumetric heat source (VHS) arbitrarily embedded within the top InP layer, and $\theta_{InP,b.c.}\left(\vec{r},t\right)$ the term related to the non-homogeneous boundary conditions (b.c.) and due to the heat flowing through the interfaces between the InP layer and the bumps. The temperature field in the bumps is expressed as the sum of two b.c. terms

$$\theta_{bumper}\left(\vec{r},t\right)=\theta_{bumper,b.c.,in}\left(\vec{r},t\right)-\theta_{bumper,b.c.,out}\left(\vec{r},t\right) \tag{3.3}$$

where the first term represents the contribution due to the incoming heat flux from the top interface, while the second is related to the flux through the silicon substrate interface. In a similar fashion, the temperature distribution in the silicon substrate is due to the fluxes entering from both bumps, that is

$$\theta_{substrate}\left(\vec{r},t\right)=\theta_{substrate,b.c.1}\left(\vec{r},t\right)+\theta_{substrate,b.c.2}\left(\vec{r},t\right) \tag{3.4}$$

All boundaries are adiabatic except the bottom, assumed isothermal at $T=T_{AMB}$. In (3.2)-(3.4) the terms corresponding to non-homogeneous boundary conditions of the second kind (i.e., assigned heat flux) at surface S are generally expressed as

$$\theta_{b.c.}\left(\vec{r},t\right)=\frac{\alpha}{k}\int_{0}^{t}\iint_{S}G\left(\vec{r},\vec{r}',t,\tau\right)\cdot f\left(\vec{r}',\tau\right)d\vec{r}'\,d\tau \tag{3.5}$$

being $G\left(\vec{r},\vec{r}',t,\tau\right)$ a three-dimensional Green's function and $f\left(\vec{r},t\right)$ the heat flux distribution at time t. In order to solve the thermal problem in the overall structure, one should evaluate the non-uniform flux distribution that satisfies the temperature continuity condition at each boundary between adjacent materials. The presented approach can be summarized as follows: each interface is first partitioned into a given number of elementary rectangles, and the flux is then assumed uniform in each rectangle; a 3×3 interface, together with the corresponding fluxes, is reported as an example in figure 3.16. The adopted discretization allows expressing (3.5) in the simplified form

$$\theta_{b.c.}\left(\vec{r},t\right)=\frac{\alpha}{k}\sum_{i=1}^{Nx}\sum_{j=1}^{Ny}f_{ij,t}\int_{0}^{t}\iint_{S}G\left(\vec{r},\vec{r}',t,\tau\right)d\vec{r}'\,d\tau \tag{3.6}$$

where R_{ij} is the generic elementary rectangle. The uniform heat flux matrix $f_{ij,t}$ related to the generic rectangle at time t is the unknown of the problem. Note that the integral

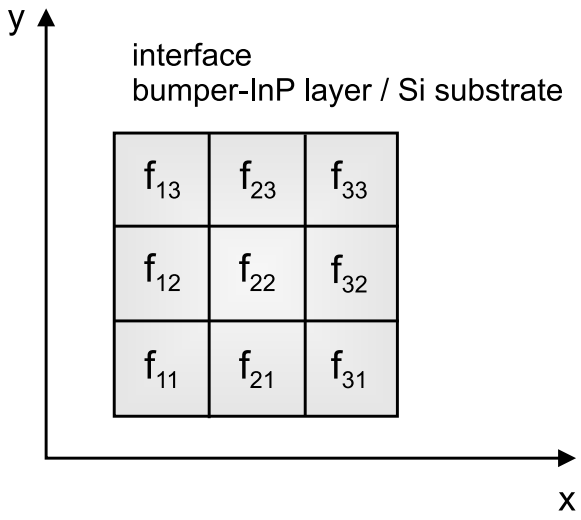


Figure 3.16: A 3×3 sample interface discretization.

$$\int_0^t \iint_{R_{ij}} G\left(\vec{r}, \vec{r}', t, \tau\right) d\vec{r}' \, d\tau \tag{3.7}$$

easily evaluates to an analytical form.
The MATLAB code is made up of two basic blocks, namely a pre-processing code that computes the heat flux matrix and a tool for calculating the temperature field once the heat fluxes are known, as schematically illustrated in figure 3.17. The first part operates as follows: imposing the temperature continuity on the barycenters of the rectangles at the interfaces yields a system of $N = N_{1x} \times N_{1y} + N_{2x} \times N_{2y} + N_{3x} \times N_{3y} + N_{4x} \times N_{4y}$ equations (one for each barycenter on the four interfaces) and N unknowns (the uniform heat fluxes in rectangles). Both coefficients and known terms are calculated from the pre-processing code on the basis of the Green's functions theory at each time instant. Once the heat flux matrix is known, the second block evaluates the temperature distribution over the desired domain within the structure. Clearly, the level of accuracy is an increasing function of the interface discretization step. Note, however, that an extremely fine grid leads to unacceptable computational requirements. Therefore, a proper trade-off should be determined prior to simulation.

Simulation results

A set of transient thermal resistance curves, corresponding to different design

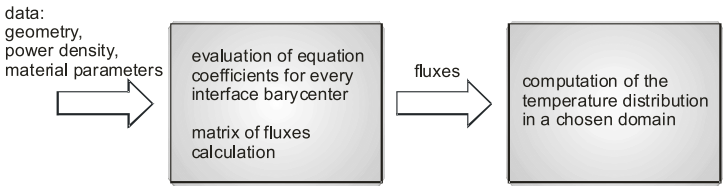
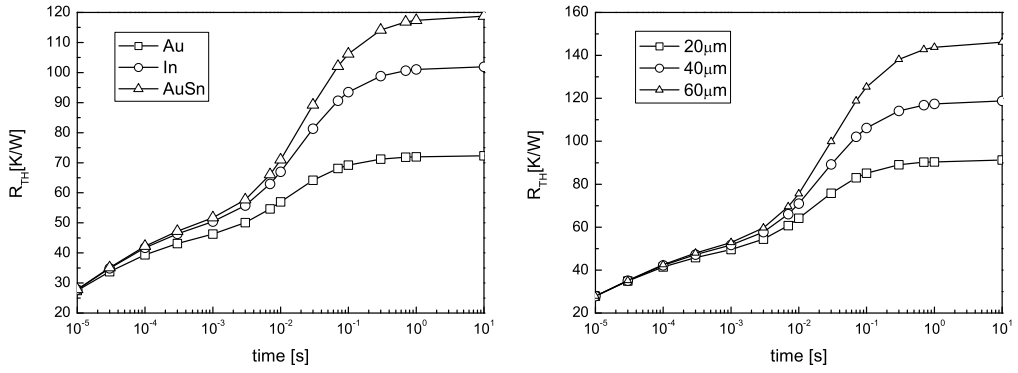


Figure 3.17: Schematic structure of the MATLAB code.



(a) (b)

Figure 3.18: Calculated dynamic thermal resistance. (a) Comparison between structures with bumps of different materials. The thickness of the bumps is 40 μm. (b) Comparison between structures with AuSn bumps of different heights.

features, result from FATS [5] simulations performed by applying a power step to one quarter of the flip-chip structure shown in figure 3.17. A discretization of 4×4 tiles was adopted for the interfaces of the bump closer to the heat source, and of 3×3 for the farer one; finer interface partitioning could only marginally improve accuracy. Figure 3.18(a) displays the effect of varying the bump material for a fixed 40 μm bump height: the soft AuSn alloy, although mechanically convenient, is less thermally conductive and causes thermal impedance to grow significantly higher than the other materials; by converse, pure gold bumps drastically improve thermal management at the expense of assemblage stability. The thermal resistance values resulting from different AuSn bump heights are compared in figure 3.18(b). As apparent from the curves, shorter bumps lead to a better thermal behavior: 20 μm tall bumps nearly halve the structure's steady-state thermal resistance value with respect to 60 μm ones. In both figures, a time instant around 3×10^{-5} s, from

[5]Flip-chip Thermal Analytical Simulator

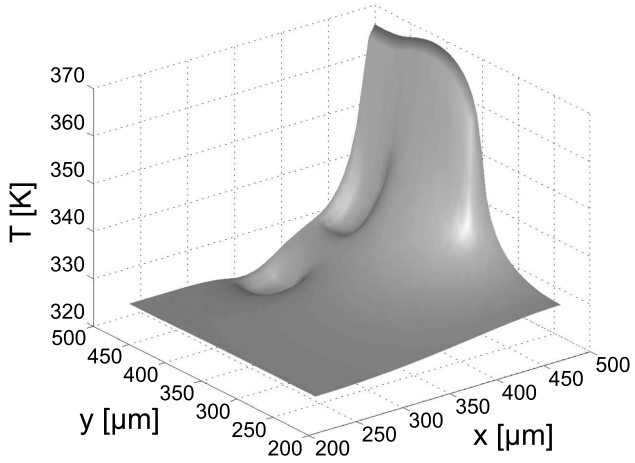
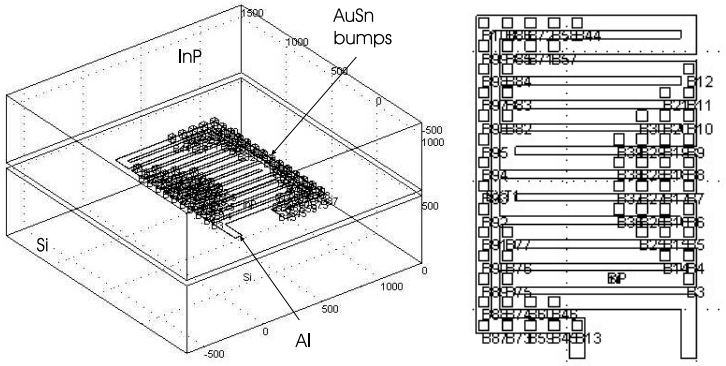


Figure 3.19: Temperature map taken at heat source height and time $t = 7 \times 10^{-3}$ s for 0.25 W power dissipation over one quarter structure.

which the curves split apart, can be neatly spotted: at this point, heat has just reached the closer bump and the flux and temperature distributions can be therefore affected by the difference in material or height. At an early time stage, before this "sensing" point, heat only flows within the indium phosphide layer, which is the same in all the considered structures, and the curves consequently overlap.
As a visual support to the above considerations, figure 3.19 displays a temperature map over the plane containing the heat source at time $t = 7 \times 10^{-3}$ s for one quarter structure, assuming a 1 W power dissipation in the overall domain. It is apparent that the peak temperature (slightly below 370 K) is reached within the heat source, while the two pits are caused by heat flowing down through the bumps, thus reducing temperature in their close proximity.

3.2.2 Thermal Management of Integrated Phasars

Wavelength (de)multiplexers are clearly key components in WDM networks. Phased-array demultiplexer were proposed for the first time in 1988 by Smit [31], while the extension to wavelength routers is due to Dragone [32]. As phasars are manufactured according to conventional waveguide technology and do not require the vertical etching step needed in grating based device, they appear to be more robust and product tolerant. Monolithic integration of an InP based MUX/DEMUX allows then a reduction in size, cost, and an increase of functionality for mass production of more complex devices. Due to this, multiwavelength lasers [33, 34], integrated add-drop multiplexers



(a) 3-D view (b) top view

Figure 3.20: Different views of the structure modeled within FEMLAB. The trace width is 60 μm and the distance between adjacent traces is 30 μm.

[35] and optical cross connect [36] are examples of integrated system where phasars play a central role.
Intuitively, a phasar is a bidirectional optical device that can be used as a multiplexer, and then it combines multiple input channel into a single one at the output, or as a demultiplexer, and conversely it splits the different wavelength, and then the different information load, into different waveguides in the output. A detailed description of the phasar physics is presented in [37]. One important aspect of integrated phasars is that it is possible to tune the wavelength selectivity by changing the operating temperature [38]. The phasar considered for the experiment has been provided by TUEindhoven. The fabrication and characterization of the device are described in great detail in [39]. The device is an eight-channel phasar using 400-GHz channel spacing (corresponding to 3.2 nm at 1550 nm) and a free spectral range of 35 nm. The central wavelength of the device is 1550 nm. Taking advantage of the above mentioned dependence of the behavior of the phasar with temperature, the proposed module is composed by a silicon carrier, which hosts an heat source, and by an indium phosphide chip with an integrated phasar on it. The module has been modeled by means of the finite element solver FEMLAB. In figure 3.20, two different views of the hybrid module are given. As visible in figure 3.20(b), the heating element is represented by a metal serpentine and realized on the top of the silicon carrier. By using the bumps as thermal pipes, it is possible to transfer the heat generated by the voltage biased serpentine to the surface of the InP chip. In this way the temperature of the phasar can be kept as constant as possible. The thermal properties of the different material involved, including the thermal conductivity of the

Au/Sn alloy, have been modeled according to [40]. All the boundaries of the model are adiabatic, except for the bottom of the silicon carrier that is supposed to be isothermal at room temperature of 300 K.
Due to the very different thicknesses of the elements in the model (the Si block is 525 μm thick while the metal trace is only 3 μm), it was not possible to run a complete multiphysic simulation to couple the electrostatic problem to the heat conduction one. However, since all the phenomena are considered in steady-state conditions, the two simulation were performed in sequence according to the following algorithm:

1. from the DC simulation, the resistance of the metal trace is found. Under DC operation, only the metal serpentine has been considered due to the very poor conductivity of the InP block and to the presence, in the real module, of a thin oxide layer between metal and silicon (that is not modeled)

2. with the exact value of resistance, the amount of power generated at each voltage level has been calculated as $W = V^2/R$

3. the power has been divided by the total volume of the serpentine in order to obtain a power per unit-volume

4. heat conduction simulation has been run with the calculated unit-power as heat source.

As a result of the modeling procedure, the temperature map at the phasar plane is given in figure 3.21. The mean temperature simulated over the phasar area as a function of the applied control voltage V is given in figure 3.22(a). The standard deviation has been calculated as

$$SD = \frac{1}{n-1} \sum_{i=1}^{n} \left[X_i - \bar{X} \right]^2 \tag{3.8}$$

where $\overline{X}$ is the mean value of the temperature over the phasar area and n the number of mesh points on the InP surface. From figure 3.22 it is clear that it is easy to control the temperature of a critical InP area by changing the DC voltage across the serpentine terminal. Also, a very small deviation of the temperature is observed. The change in temperature, as mentioned, impacts the central wavelength of the phasar. By considering a temperature coefficient of 0.13 nm/K, the shift in wavelength as a function of the temperature increase can be approximated with:

$$\lambda(T) = 0.13(T - T_{AMB}) + \lambda_{AMB} \tag{3.9}$$

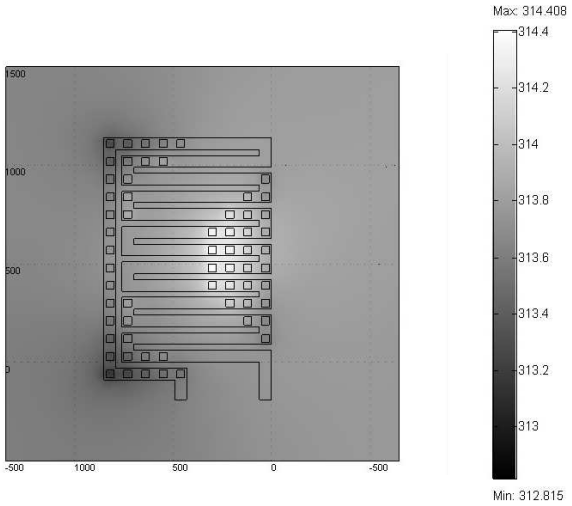
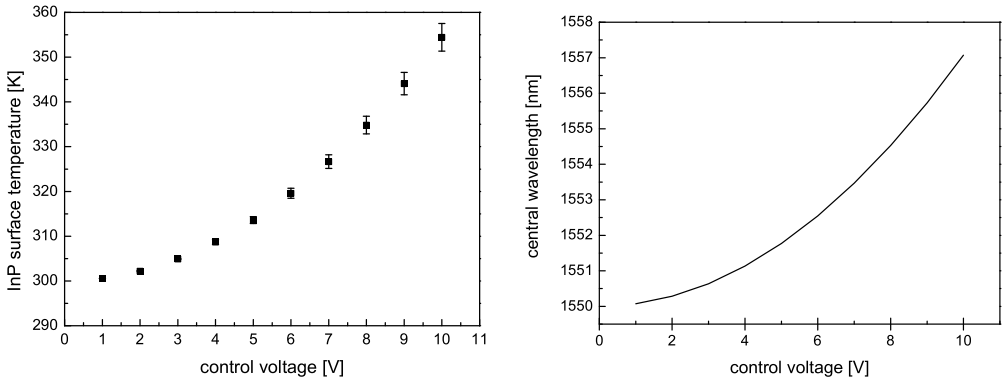


Figure 3.21: Simulated temperature map of the InP surface for a control voltage V = 5 V.

where $T_{AMB} = 300\ K$ and $\lambda_{AMB} = 1550\ nm$. It is then possible to plot the central wavelength of the phasar when heating up the chip (figure 3.22(b)) through the control voltage.
It is clear than it is possible to tune and control the wavelength selectivity of the phasar though its operating temperature. Moreover it is possible to exploit this property to compensate process fluctuations by post-fabrication tuning.

The heat transfer efficiency from the serpentine to the phasar can be further improved. Looking at figure 3.22(a), it is clear that a high voltage can be required to stabilize the temperature on the InP chip. Such a high voltage may damage the metal wire due to electromigration. We can solve this problem by increasing the thermal impedance of the silicon block: in this way the heat is ”forced” to flow into the InP chip instead that moving toward the bottom of the silicon wafer. This can be done by selectively removing the bulk material underneath the serpentine in the silicon carrier (figure 3.23). In this way, the only isothermal surfaces are those external to the cavity, which is now filled with air. Selective etch of the bulk silicon substrate can be done by micromachining [41]. Obviously the substrate cannot be completely removed in order to avoid a degradation of the mechanical stability of the final assembly. The resulting wavelength tunability plot is given in figure 3.24. It is evident that, due to the higher thermal coupling between the metal serpentine and the phasar, with a lower voltage it is possible to generate larger wavelength shifts. A demonstrator module with normal silicon carrier



(a) (b)

Figure 3.22: (a) Phasar mean temperature for different control voltage values. The standard deviation bars have been multiplied by a factor of four for better visibility. (b) Wavelength dependence on the control voltage.

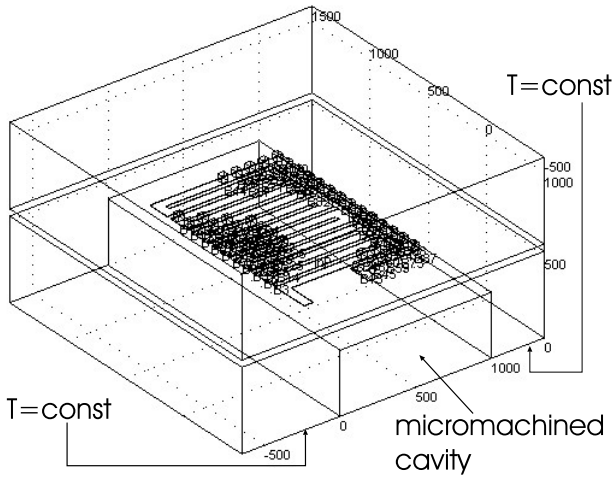


Figure 3.23: Micromachined silicon carrier.

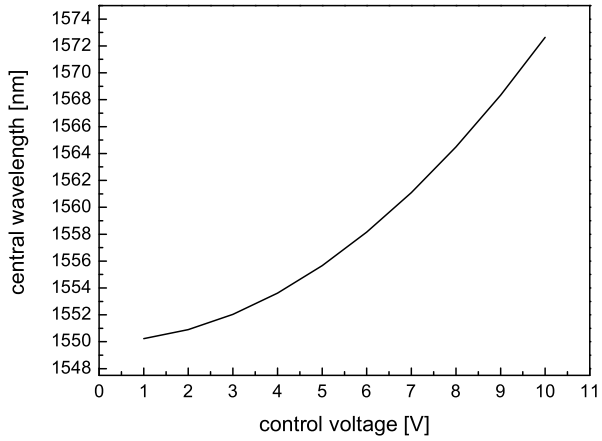


Figure 3.24: Wavelength dependence on the control voltage.

thickness ($\sim 500\ \mu m$) has been fabricated (figure 3.13).

Chapter 4

Microwave modeling of flip-chip interconnects

In this chapter we discuss the electromagnetic characterization of coplanar to coplanar flip chip transitions through a new scalable electrical lumped model. The model is developed by reducing the well-known electrical model of two coupled coplanar waveguides. Electromagnetic simulations of the structure are used to generate circuit models for various bump configurations. Regression models are then used in order to scale the values of the lumped elements with physical dimensions of the system. Based on the agreement between fast circuit simulations and time-consuming finite element analysis, the model is well suited for modeling flip-chip CPW in the high-GHz range.

4.1 Flip-chip Interconnects

Transitions in a flip-chip package involve the use of metallic bumps to transmit the signal between the substrates. These bumps represent the main discontinuity to a signal propagating on the lines, resulting in partial loss and possibly distortion of the signal. All these issues need to be then properly considered in the design of the flip-chip system. Many studies involve a comparison between using coplanar and microwave flip-chips. Even if many chips are today designed in a microstrip fashion (figure 4.1(a)), a coplanar structure (figure 4.1(b)) is believed to be more efficient. As can be seen in the figures, it is expected that the substrate will have a more marked influence on the field in the microstrip structure than in the coplanar one [42]. It is then important to develop equivalent lumped element models of the bump transition in order to understand and predict the electrical behavior of the flip-chip assembly and to develop proper design rules. Moreover a scalable

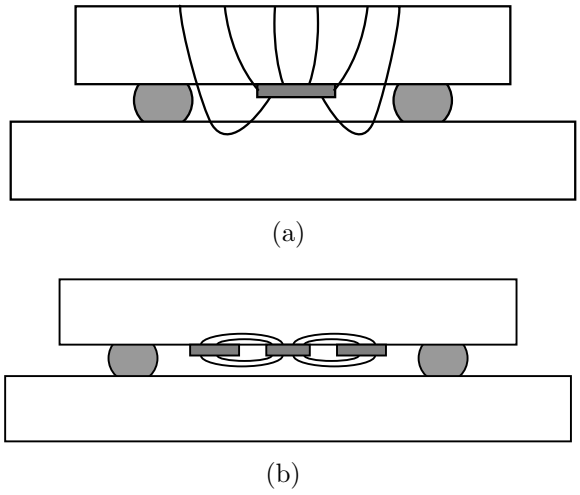


Figure 4.1: Typical transmission lines in flip chip modules: microstrip (a) and coplanar waveguide (b).

equivalent circuit model for flip-chip transition is an helpful tool to use in circuit simulators to predict the performance of the overall system including the package. Scalability of circuit elements with physical parameters of the transition is required in order to overcome the use of time-consuming 3D electromagnetic simulations. The variation of the physical parameters has to be reflected in the values of the elements of the circuit.
Some works presented equivalent circuits extracted from electromagnetic simulations. In figure 4.2 [43], a simple L-C ladder network is used, but all resistive losses were neglected and a symmetric (both substrates are composed of the same material) model was assumed. In [44], a simple capacitance is used to model the interconnect. Moreover, parasitic modes propagating through the silicon motherboard are addressed to account for crosstalk effects. In [45] (figure 4.3), an accurate pi-model including series and substrate losses is proposed, but it is an equivalent model that does not provide any physical insight.
The lumped model proposed here is an extended version of the one described in [43]. The improvement is represented by resistive losses, both metal- and substrate-related, which are now included in the model. Moreover, the substrates are assumed to be different, as required in many opto-IC applications. Regression models are also developed to relate variations of equivalent circuit elements with geometrical parameters of the transition in order to provide the model with prediction and scalability capabilities.

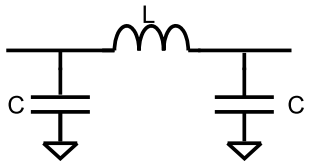


Figure 4.2: Equivalent circuit proposed in [43].

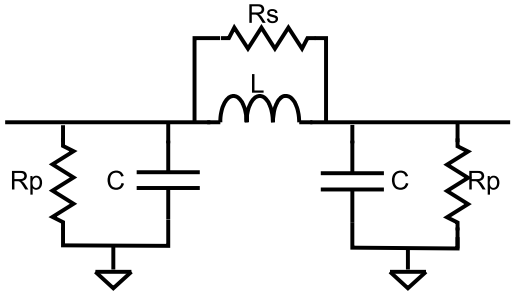


Figure 4.3: Equivalent circuit proposed in [45].

4.2 Model development

A view of the simulated structure is given in figure 4.4, together with physical parameters of interest, namely the conductors overlap o, the distance of the ground bump center from the edge of the ground plane d, the bump height h, the bump diameter a and the launching coplanar signal lines width w. The media under consideration are assumed uniform, isotropic, homogeneous and without magnetic properties, i. e. $\mu_r = 1$. In order to model the RF behavior of the transition, an equivalent lumped circuit is required.
As a starting point for the model development, figure 4.5 shows the equivalent circuit of two coupled transmission lines. To represent the coplanar lines the classic T-model has been preferred and electric circuits have been superimposed to the CPW-to-CPW transition. The two lines are magnetically coupled by L_{SS1}, L_{SS2}, L_{SC1} and L_{SC2}, while the electrical coupling is represented by C_{Min}, C_{Mout} and C_{MB}. Metal losses are represented by R_{SC1},R_{SC2}, R_{SS1}, R_{SS2} while substrate losses are included in R_{PS}, C_{PS}, R_{PC} and C_{PC}. Note that grounding is provided by the ground lines of the coplanar waveguides on both the substrate and chip. By inserting a bump interconnecting the two lines, the circuit reduces to that depicted in figure 4.6, where the capacitance C_M has been shorted by the bump and has been thus removed.
After inspection of the circuit, it is also possible to neglect impedances $R_{SC1}+$

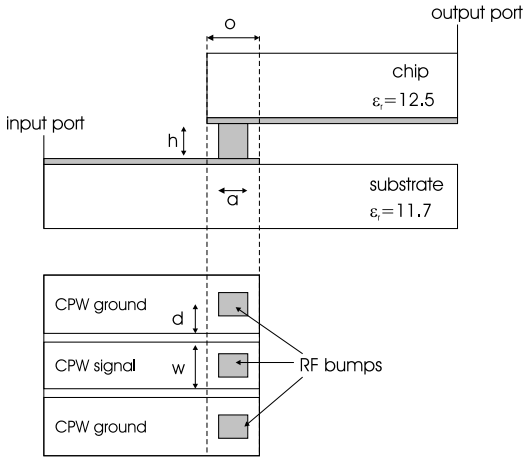


Figure 4.4: Modeled flip-chip structure.

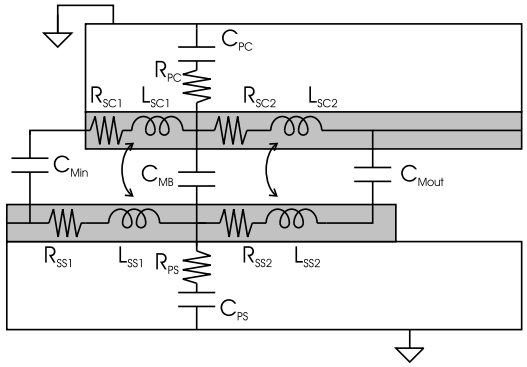


Figure 4.5: Equivalent circuit of two stacked coupled CPWs.

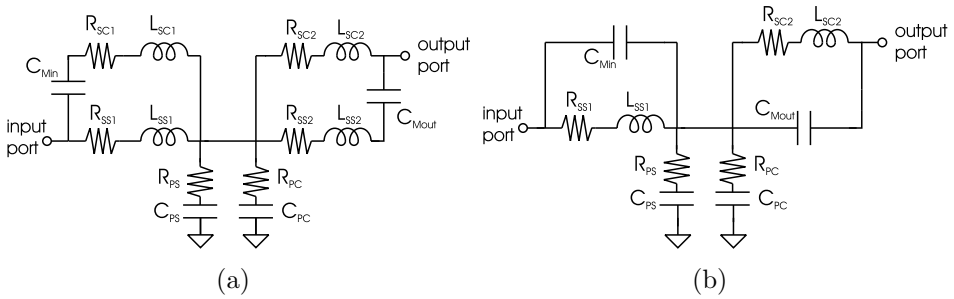


Figure 4.6: Equivalent circuit of two stacked coupled CPWs before (a) and after reduction (b).

$j\omega L_{SC1}$ and $R_{SS2} + j\omega L_{SS2}$ with respect to $1/(j\omega C_{Min})$ and $1/(j\omega C_{Mout})$. This can be done without introducing significant errors since the metal lines exceeding the edge of the bump are usually characterized by a short length and thus small values of resistance and inductance. It is important to note that the approximation of considering the bump itself as a short circuit does not affect the results since we are modeling the whole transition rather than the single bump, which has been demonstrated to depend mainly on the overlap between the two coplanar lines (here represented by C_{Min} and C_{Mout}) and on the height of the bump [43].
The final circuit configuration is shown in figure 4.6. The equivalent circuit considered here accounts for all the losses related to the transition and, contrary to other models ([43]-[45]), it considers different electrical properties for the substrates. This is needed when considering hybrid systems with silicon as a substrate for the monolithic integration of III-V devices, namely indium phosphide. It is also important to note that the model considers the whole transition rather than the bump itself and then all the phenomena, like parasitic modes due to close proximity of two substrates [46], are embedde in the EM simulations required to generate the model itself.
To find the value of the elements in the circuit of figure 4.6(b), a best fit algorithm has been developed. In this algorithm, the scattering parameters of the transition obtained from a 3D FEM simulator are converted to Z-parameters. The Z-parameters are then used to find the elements of the equivalent circuit at a single frequency point (namely the mid-band frequency). The values of the elements of the equivalent circuit are used as an initial guess for further fitting the result of the electromagnetic simulation over all the range of frequencies of interest. In this way values for the circuit elements that best fit the simulation are found.
Note that the input and output launching coplanar lines dimensions have

Table 4.1: Parameter range for model development.

	min	max
h	$20\mu m$	$100\mu m$
o	$120\mu m$	$200\mu m$
a	$30\mu m$	$100\mu m$
w	$40\mu m$	$120\mu m$
d	$30\mu m$	$100\mu m$

been separately optimized for 50Ω characteristic impedance and then de-embedded up to the transition area from the result of electromagnetic simulations.

4.3 Model scalability and simulation results

In the development of a scalable model, all factors related to the geometry of the bump, to its placement and to the launching coplanar lines configuration are expected to directly affect the value of model parameters. In order to enhance the proposed model with such capability, regression techniques can be developed for the elements of the equivalent lumped circuit of figure 4.6(b). The geometrical parameters o, d, h, a and w of the transition have then been varied to build up a statistical base for the regression analysis. In Table 4.1 the range of parameters values for each variable is reported. For a total of 20 variable combinations, model parameters have been first extracted from FEM simulations using the procedure described before. The whole circuit has then been tuned to optimally fit the electromagnetic simulation results using the extracted values as an initial guess.
To model the dependance of lumped elements on geometrical parameters, a linear regression equation with one level interaction has been used:

$$\begin{aligned} R, L, C &= c_0 + c_h \cdot h + c_a \cdot a + c_w \cdot w + c_d \cdot d \\ &+ c_o \cdot o + c_{ha} \cdot h \cdot a + c_{hw} \cdot h \cdot w \\ &+ c_{hd} \cdot h \cdot d + c_{ho} \cdot h \cdot o + c_{aw} \cdot a \cdot w \\ &+ c_{ad} \cdot a \cdot d + c_{ao} \cdot a \cdot o + c_{wd} \cdot w \cdot d \\ &+ c_{wo} \cdot w \cdot o + c_{do} \cdot d \cdot o \end{aligned} \tag{4.1}$$

Please note that the coefficients c_{xx} in the right hand side of equation (4.1) are different for each component in the equivalent circuit. To verify the proposed approach, the results of circuit simulations have been compared with full 3D FEM simulations. Excellent agreement has been observed for all configurations. Figure 4.7 shows s_{11} as a function of frequency, as obtained from

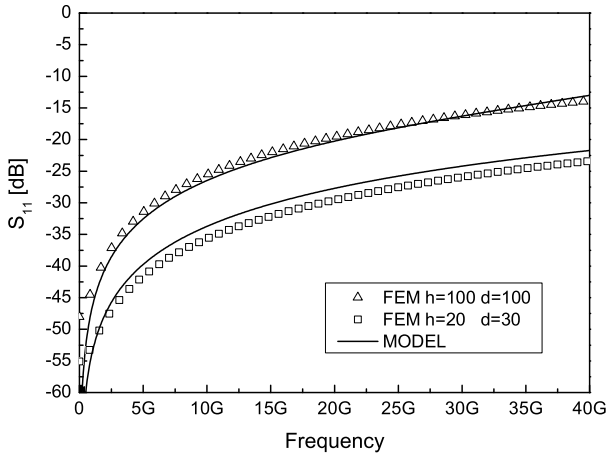


Figure 4.7: Reflection of the CPW-to-CPW transition for different height(h) and diameter(d) of the bumps.

FEM simulations and from circuit simulations for two configurations, namely a thin and short bump and a wide and high one. It is evident that smaller dimensions lead to a lower reflection of the signal wave. Figure 4.8 shows the frequency behavior of s_{21} for the same structures. Contrary to what depicted in figure 4.7, it is possible to note how, mainly due to series resistance, small dimensions yield higher losses. The slight deviation for a thick bump can be regarded as the result of the simplifications. It is then possible to conclude that a trade-off exists between low reflections and low insertion loss for the same geometry.

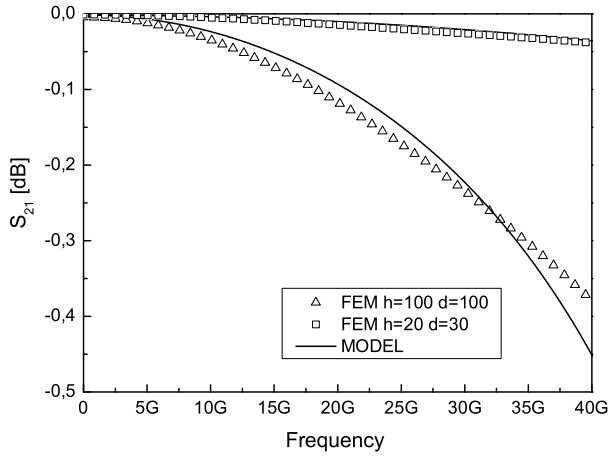


Figure 4.8: Transmission of the CPW-to-CPW transition for different height(h) and diameter(d) of the bumps.

Chapter 5

Silicon Bipolar IC's for Optical Communications

The rapid-growing volumes of data processed in telecommunication networks have rekindled interest in high-speed optical and electronic devices and systems. With the proliferation of the Internet and the rise in the speed of microprocessors and memories, the transport of data continues to be the bottleneck, thus motivating work on faster communication modules. Moreover, besides performance considerations, the manufacturing costs of a technology that enables the co-existence of electronics and photonics functionalities on the same chip, other than in the same package, pushes research efforts toward hybrid opto-IC solutions.
This chapter, after a brief overview of an optical communication architecture and of the techniques for broadband amplification, details the design and the characterization a of a silicon Mach-Zehnder modulator driver. This driver operates in traveling wave mode. An improved version of the amplifier that has been designed for multi-chip implementation with an InP-based modulator will be also presented.

5.1 Wide-Band Amplifiers

In recent years, the unappeasable development of multimedia communications has created a strong demand for high-speed and high-capacity transmission systems. Wavelength-division multiplexing (WDM) and time-division multiplexing (TDM) techniques have been developed to realize the next generation of transmission systems. In order to achieve the multi-Gb/s data rates for WDM and TDM systems, very high performance ICs are required [47]. In figure 5.1 a block diagram of a fiber-optic transmission system is given [48].

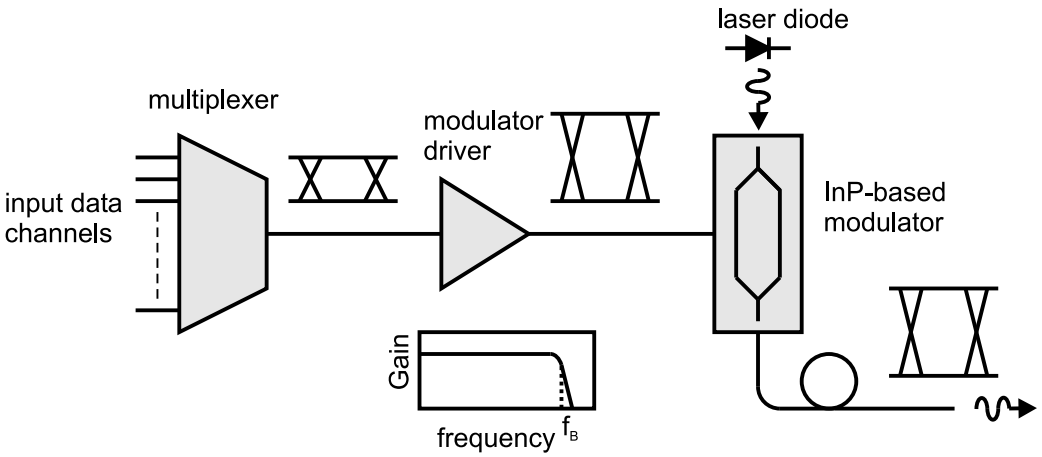


Figure 5.1: A typical optical transmitter.

The different data streams are mixed together by a multiplexer into a single data-stream. In order to achieve the proper voltage level to correctly operate the optical modulator, a broadband amplifier is required. Finally, the amplified bit-stream is impressed on the optical signal generated by a optical source by means of a light modulator. Two laser modulation schemes can be used: the direct laser modulation and the external laser modulation. The earlier approach employed in lightwave communication was direct modulation of the laser (see figure 5.2(a)). In this configuration, the electrical signal is combined with a bias current and applied to the laser diode. The electrical signal thereby directly modulates the laser gain and consequently the optical output intensity. In spite of its simplicity, direct modulation fails at data rates beyond about 2.5 Gb/s, since the change in charge density associated with the transition in the input current not only affects the optical gain of the material but also change the real part of the index of refraction within the laser cavity [49]. The latter change shifts the lasing frequency[1] and thereby broadens the optical spectrum of the transmitted pulses. When combined with the chromatic dispersion of standard single-mode silica fibers, the pulses spread and interfere as they propagate along the fiber leading to shorter distance links.
An alternative approach to the direct modulation of the laser is the external modulation (figure 5.2(b)). The laser is used in a continuous wave mode (CW) and thus presents no frequency chirp. Data are then encoded onto the optical carrier by applying the modulating signal to the modulator that is

[1]This phenomenon is know as frequency chirp

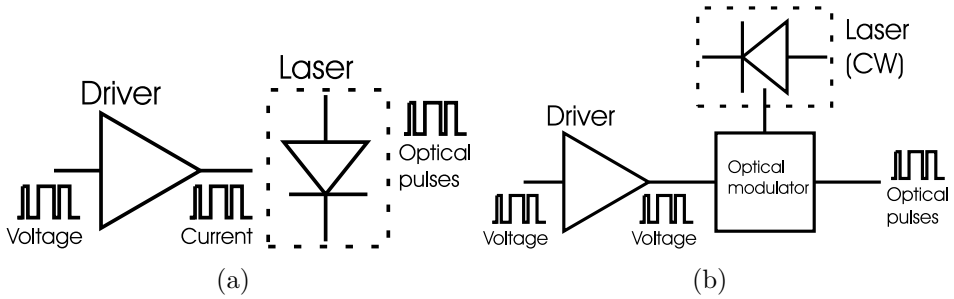


Figure 5.2: Methods of information encoding in lightwave systems. (a) Direct modulation of the laser. (b) External modulation of the laser.

external to the laser cavity. External modulators can be further classified in two main groups, namely electroabsorption modulators (EAM) and Mach-Zehnder interferometers (MZI). Electroabsorption modulators need a lower voltage swing compared to Mach-Zehnder interferometers and may, therefore, be more suitable to be driven by monolithic integrated circuits (rather than expensive hybrid amplifiers).
However, as one disadvantage, the EAM presents a capacitive load, in contrast to the 50Ω input of a MZI. As a consequence, at very high bit-rate it would be extremely difficult to drive the modulator via a 50Ω transmission line. In this case, due to insufficient matching, double reflections would occur increasing the time-jitter and so deteriorating the quality of the signal.
Even by using external modulation, the severe bottleneck in the electronics of an optical transmitter system is still represented by the modulator driver [50], because of the contradicting demands on high voltage swing and high operation speed [51]. Moreover, as previous stated, one other important characteristic of the modulator driver is its frequency behavior. This is because random signals are usually characteristic of a wide spectrum. To get more insight with this aspect of the design of an amplifier for optical communications, it is instructive to examine how a random binary (without coding) sequence looks like in the frequency domain.
Let us represent a bit as a rectangular pulse with duration $T = 1/f_b$:

$$W(t) = rect(t/T) \tag{5.1}$$

where f_b is the bit-rate. An infinite sequence of bits where each bit has a probability p_k to be "1", otherwise it is "0" can then be expressed as

$$x(t) = \sum_{k=-\infty}^{\infty} W(t - k \cdot T)\, p_k \tag{5.2}$$

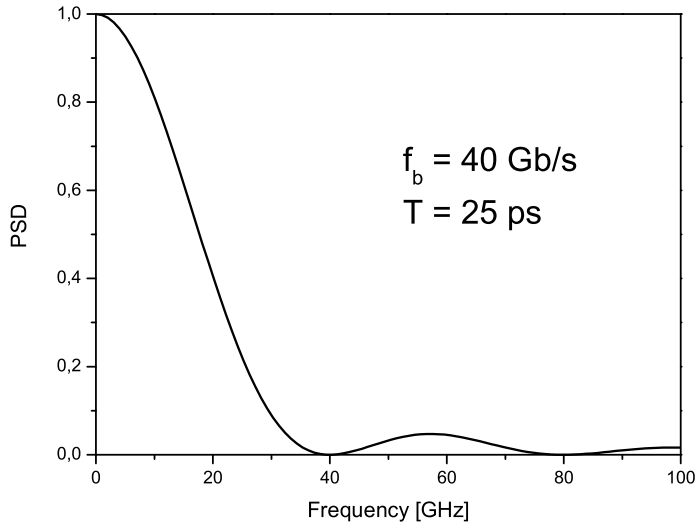


Figure 5.3: Normalized PSD of a 40Gb/s random data signal.

The resulting *power spectral density* (PSD) of $x(t)$ is defined as the magnitude of the Fourier transform of the *autocorrelation function* $r_{xx}(t)$:

$$r_{xx}(t) = \lim_{T\to\infty} \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t-\tau)\, x(\tau) d\tau \tag{5.3}$$

that, for a rectangular pulse shape of a random data signal is a triangular function [52]. The Fourier transform of a triangular pulse is a $sin(x)/x := sinc(x)$ function:

$$PSD(f) = \frac{T}{4} \cdot \left| \frac{\sin(\pi f T)}{\pi f T} \right|^2 \tag{5.4}$$

In figure 5.3, the PSD of a random sequence is normalized to its maximum value and plotted for a 40 Gb/s signal (T=25ps). From the above analysis, many important attributes of random binary sequences can be outlined.
For a bit-rate of f_b, the spectrum exhibits no power at frequencies equal to f_b, $2f_b$, etc. Moreover, the spectrum extends down to DC ($f = 0$). This should not surprise since a long sequence of "1" or "0" is considered by the amplifier as a DC signal that has to be correctly processed.
Amplifiers designed for fiber-optic links must then have the following characteristics:

- bandwidth from f_l to f_u, with $f_l \approx DC$ and $f_u \approx 0.75 f_b$ to cover approximately 75% of the spectrum of the data signal

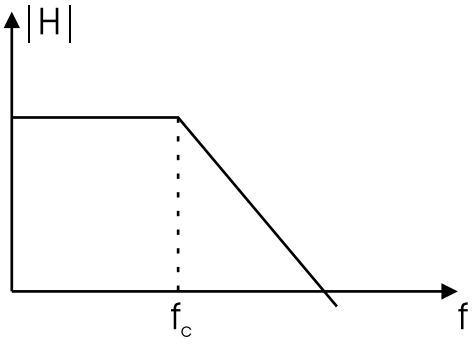


Figure 5.4: Desired amplifier transfer characteristic for digital data transmission, $f_c \approx 0.75 f_b$.

- the phase response has to be as much linear as possible to guarantee the same propagation velocity to each impulse, independently from its duration.

The magnitude of the amplifier transfer function must therefore be flat as indicated in figure 5.4.
The above reported analysis can be used to quantify the bandwidth demand of most communication standards. It has been estimated that a bandwidth of at least 75% for the bit-rate is needed to equalize non-return-to-zero (NRZ) signals. This means that a bandwidth higher than 7 GHz is required for transmission at synchronous-transport-module level 64 (STM-64), and that the 60 GHz bandwidth should be a milestone that corresponds to 80 Gb/s (eight time that of the STM-64) [53]. On the other hand, the lower limit is determined by the section length in the bit-stream. Most data are scrambled and have a mark density of one-half. However, if we use the ITU-T SDH standard, the section overhead involving some special data comes out every 125 μs, corresponding to a frequency of 8 kHz [54]. Actually, there is a margin that depends on many factors such as the roll-off characteristics of the amplifier, the performance of the DC regeneration circuit and the sensitivity of the subsequent circuit. Overall, the required lower frequency limit is estimated to be less than 100 kHz. Therefore, the bandwidth has to be broaden without affecting the lower frequency limit.

5.1.1 Classic Broadband Amplifiers

As mentioned in the previous section, amplifiers in broadband communications must be operated up to quite high frequency. The most significant limitation of high-frequency performance of standard amplifier stages is the

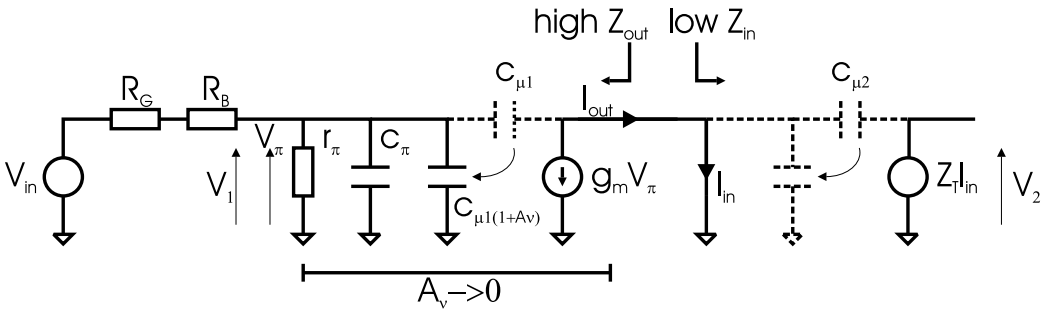


Figure 5.5: Avoidance of the Miller-effect by extreme mismatch.

presence of feedback capacitance due to the Miller effect. One solution that is quite often exploited is the reduction of the Miller effect by "extreme mismatch": since the Miller effect is based on *voltage gain* between two nodes, one way to alleviate its effect is to reduce the gain of the circuit to zero by short-circuiting its output, or in practice by providing a very-low impedance load. Unfortunately, the circuits based on this method are not useful for practical applications.

A more effective approach is to transfer the output current to a second voltage- or current source (figure 5.5). In this way, the bandwidth of the amplifier is increased. This approach has been proven to be also effective in reducing the capacitive noise coupling at the interface point due to its low impedance.

As a typical example of this technique, a chain of alternating transadmittance stage (TAS) and transimpedance stage (TIS) can be used [55]. Due to this mismatching, the critical poles in the transfer function of one stage are compensated by the zeros introduced by the other stage. The transfer function of the overall stage is equal to

$$H_{tot} = Y_T Z_T \tag{5.5}$$

with $Y_T = I_{out}/V_1$ and $Z_T = V_2/I_{out}$. H_{tot} remains approximately constant up to relatively high frequencies, resulting in a high cutoff frequency. This again is because of the drastically reduced influence of the strongly frequency-dependent input and output impedances of the different stages. As another advantage of mismatching, all the nodes in the circuit are low-ohmic. This reduces the influence of parasitic capacitances and thus further increases the bandwidth.

In figure 5.6 the original double-stage proposed by Cherry and Hooper [56], consisting of a TAS and a TIS, is extended by (one to three) emitter followers

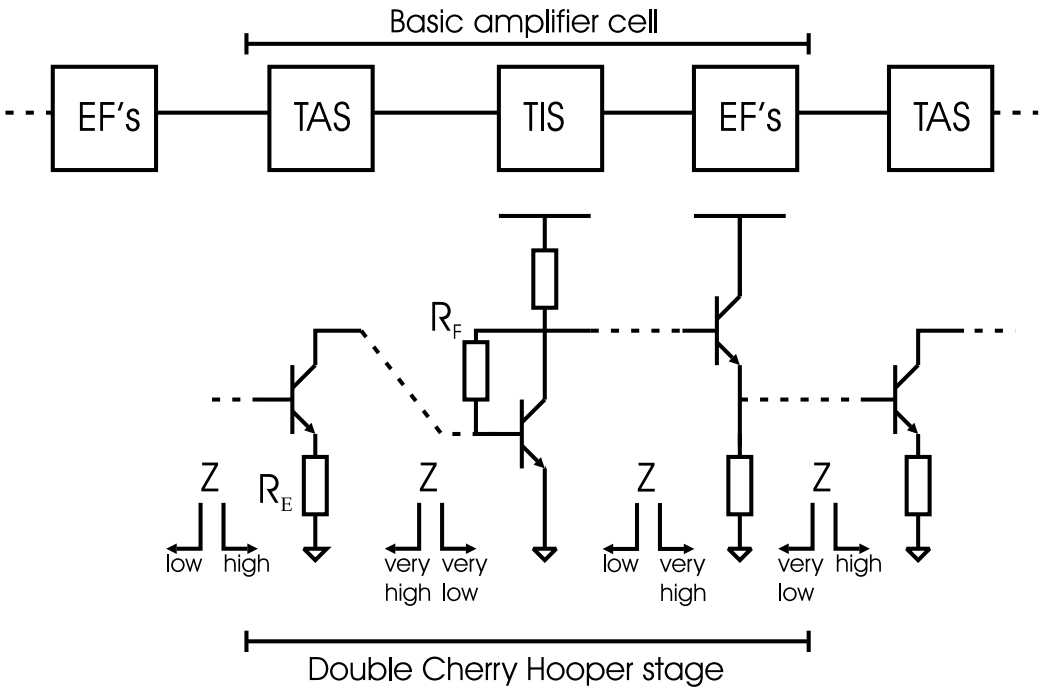


Figure 5.6: Principle of impedance mismatching in broadband amplifiers. Z stands for the input and output impedances, respectively.

(EF) between the output of the TIS and the input of the TAS. These EF's are required for improving the insufficient mismatching at this interface, for levels shifting and for gain peaking near the upper frequency limit. At high frequencies, where mismatching is degraded, conjugate complex input and output impedances can be observed at the interface between different stages, which can further increase the bandwidth. One important thing to note is that also the *cascode* (see section 5.1.2) configuration can be considered as an approximation to the TAS/TIA principle of figure 5.5.
Obviously all mentioned circuits can be operated in the advantageous differential mode, in order to improve noise ruggedness and output voltage level. However, single-ended operation is usually required, at least in the output stage, for the modulator drive because of its interface to the optoelectronic component, which normally is implemented in single-ended configuration [57].
Regarding the IC-technology, it should be noted that historically optical communications have been considered a domain for III-V materials due to the higher maximum voltage BV_{CEO} (zero base current collector emitter breakdown voltage) of III-V bipolar transistors compared to silicon or to SiGe counterparts. This large breakdown voltage need is needed to accommodate

the high output swing required by external modulators (i.e. 3 to 6 V_{pp}). Conversely, for high-speed operation, the device parasitics and delays must be kept to the minimum, resulting in very small transistor dimensions. In addition, in high-speed bipolar devices, the current density is improved by using a relatively highly doped and thin collector. These trends result in relatively low breakdown voltages for the active devices. This trade-off cannot be easily handled in state-of-art SiGe technologies, which are characterized by an f_T and a BV_{CEO} of 200 GHz and 1.5 to 2 V respectively [58]. InP-HBT's instead, due to the higher band-gap of InP compared to Si, can reach f_T of 150 GHz [59] and support BV_{CEO} of 4 to 8 V. Similar numbers can be found for GaAs.
One last consideration is in order, as to the choice of the devices used for the design of circuits for optical communications. In addition to voltage and bandwidth specifications, high-speed optical communications require also a low-phase jitter to support the monolithic integration of clock and data recovering modules that follow the optical detection. HEMT-based amplifiers have, in principle, low threshold voltage uniformity and high phase jitter. This may hinder HEMT's from providing optimum system performance in a single integrated chip. On the other hand, heterojunction bipolar transistors are analog devices that possess excellent threshold uniformity, low $1/f$ noise characteristics and high output impedances [60] and have been the preferred technology for high-speed digital and analog application.

The techniques presented in this section allow the design of amplifiers with a gain that extends theoretically down to DC and up to a very high bandwidth. But, even if the gain bandwidth of the presented circuits can be considered fairly wide, the upper limit is empirically known to reach only 30% of the transition frequency f_T of the transistors [61]. This is because the gain is unfortunately limited by the device and circuit parasitics that cause premature roll-off or excessive peaking response. In addition, it is not trivial to realize a broadband high order matching network to compensate these parasitics. To increase the gain-bandwidth product, one solution might be cascading more lumped amplifiers. However, since the total gain of a cascaded amplifier is given by the product of the gain of the single stages, the high-frequency gain does not benefit (if the gains of the individual stages are as close to one as frequency increases, also the total gain will) [62]. An alternative approach is based on a distributed amplification approach as will be discussed in detail in next section. As an example, using the same technologies, a 50% improvement with respect to the lumped implementation has been reported [63].

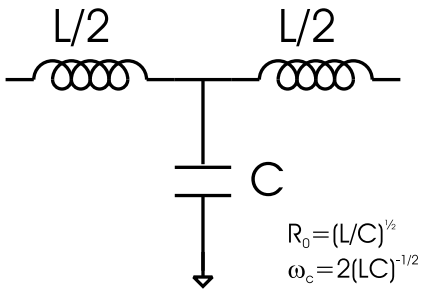


Figure 5.7: Ideal constant-k line. The nominal characteristic impedance R_0 and the radian cut-off frequency ω_c are calculated assuming image characteristic impedance terminations at both sides.

5.1.2 Traveling-Wave Amplifiers

As mentioned in the previous section, feedback amplifiers with a flat gain from DC are routinely used in current systems. Unfortunately, high frequency performance is limited by parasitic capacitances of the transistors. Broad bandwidth can be achieved by absorbing the transistor parasitics into synthetic input and output transmission lines, which are coupled by the transistor transconductance. Such an amplifier is known in literature as distributed amplifier (DA) or traveling wave amplifier (TWA) and its operation principle was originally suggested in the attempt to increase the gain-bandwidth product of an amplifier by separating the individual tube inter-electrode capacitances while adding their transconductance [64].
The most traditional implementation of a TWA is based on the use of (MES)FET devices. An analytical discussion of the TWA amplifier design has been presented in [65, 66], showing a maximum achievable operational frequency equal to $0.8 f_{MAX}$[2]. A schematic representation of a three-stage traveling wave amplifier is shown in figure 5.8. The principle of operation is based on the absorption of input and output impedances in the input and output line in order to create two artificial lines. Each stage can then be considered as a T-section network (see figure 5.7) with a cut-off frequency given by [68]

$$f_c = \frac{1}{\pi\sqrt{LC}} \tag{5.6}$$

The basic traveling wave amplifier consists of two transmission lines, namely the input line, the output line and the transistors, which provide the signal amplification, as shown in figure 5.8. The forward (coming from the right of the figure) wave on the input line is amplified by each transistor. The incident

[2] f_{MAX} is defined as the maximum oscillation frequency of the active device [67].

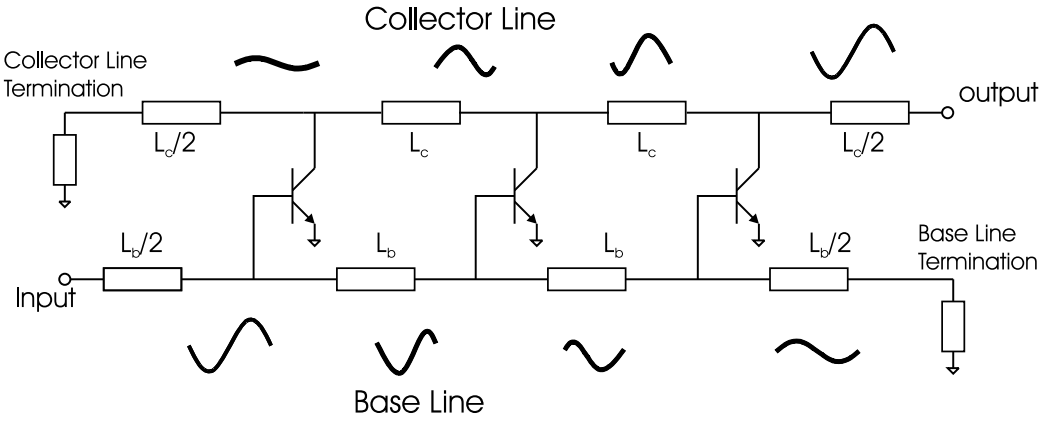


Figure 5.8: Three-stage bipolar-based TWA schematic.

wave on the output line travels forward in synchronization with the traveling wave on the input line. Each gain stage adds current in phase to the signal at each tap point on the output line. The forward traveling wave on the input line and the backward (traveling to the left) wave on the output line are absorbed by terminations matched to loaded characteristic impedance of the input line Z_{in} and output line Z_{out}.
Assuming that the number of transistor on the line is large and that their spacing is much smaller than half-wavelength, their input and output capacitances may be considered distributed. The input impedance of a loaded artificial line (which will be referred to as base line in the following) is then given by [68]:

$$Z_b \approx \sqrt{\frac{j\omega L_b + R_b}{j\omega\left(C_b + \frac{c_{in}}{l_b}\right) + G_b}} \tag{5.7}$$

where L_b, R_b, C_b, G_b are the series inductance and resistance the parallel capacitance and conductance of the base transmission line per unit length l_b, respectively. The small signal input capacitance of the amplifying stage is represented by C_{in}. A similar expression can be obtained for the output impedance (which will be referred to as collector line in the following):

$$Z_c \approx \sqrt{\frac{j\omega L_c + R_c}{j\omega\left(C_c + \frac{c_{out}}{l_c}\right) + G_c}} \tag{5.8}$$

where L_c, R_c, C_c, G_c are the series inductance and resistance , the parallel capacitance and conductance of the collector transmission line per unit length l_c, respectively, while c_{out} is the small signal output capacitance of the amplifying stage. The complex propagation constants of the transmission lines are also changed due to the transistor loading

$$\gamma_b \approx \sqrt{(j\omega L_b + R_b) \cdot \left[j\omega \left(C_b + \frac{c_{in}}{l_b} \right) + G_b \right]} \tag{5.9}$$

$$\gamma_c \approx \sqrt{(j\omega L_c + R_c) \cdot \left[j\omega \left(C_c + \frac{c_{out}}{l_c} \right) + G_c \right]} \tag{5.10}$$

It can been seen from equations (5.7) - (5.10) that device parasitic capacitances are absorbed into the capacitive component of the transmission line and therefore contribute manly to the real part of Z_0 and the imaginary part of γ, which do not induce loss.
The gain of the distributed amplifier can be calculated as follows. Note that the voltage at the k_{th} tap of the base line is related to the base segment length l_b and complex propagation constant of the loaded base line γ_b through

$$v_{bk} = v_1 e^{\left(k-\frac{1}{2}\right)\gamma_b l_b} \tag{5.11}$$

where v_1 is the voltage at the input node of the amplifier. We have assumed that the base line is terminated to Z_b on the right end. Also, by assuming the collector line terminated to Z_c on the left end, the voltage wave going out of each gain stage sees an impedance of $Z_c/2$, which is the parallel combination of the two Z_c seen on the left and on the right. The generated voltage wave at the k_{th} collector tap traveling to the right is therefore given by

$$E_{ck} = -g_m \frac{Z_c}{2} v_{bk} = -g_m \frac{Z_c}{2} v_1 e^{-\left(k-\frac{1}{2}\right)\gamma_b l_b} \tag{5.12}$$

where g_m is the small signal transconductance of each transistor. A simple first order approximation for g_m can be used since the transistor parasitic capacitances are primarily absorbed into the real part of Z_0 and the imaginary part of γ [69]. The assumption of considering the load impedance of each stage equal to half of the impedance of the load line can be misleading. This is because the analysis does not consider the role of the current injected by the remaining stages on the effective load impedance of each stage. This as been accounted for in [70], where it is shown that for optimal design the characteristic impedance of the line has to be properly taper for each stage. However, for the sake of simplicity, we will consider the characteristic

impedance of the line to be uniform.
The total wave traveling to the right at the output is given by superposition

$$E_{i,out} = \sum_{k=1}^{n} E_{ck} e^{-\left(n-k+\frac{1}{2}\right)\gamma_c l_c} \tag{5.13}$$

$$\begin{aligned} E_{i,out} &= \sum_{k=1}^{n} E_{ck} e^{-\left(n-k+\frac{1}{2}\right)\gamma_c l_c} \\ &= -g_m \frac{Z_c}{2} v_1 \cdot \sum_{k=1}^{n} e^{-\left(k-\frac{1}{2}\right)\gamma_b l_b} \cdot e^{-\left(n-k+\frac{1}{2}\right)\gamma_c l_c} \\ &= -g_m \frac{Z_c}{2} v_1 \cdot e^{-(\gamma_c l_c + \gamma_b l_b)/2} \cdot \frac{e^{-n\gamma_c l_c} - e^{-n\gamma_b l_b}}{e^{-\gamma_c l_c} - e^{-\gamma_b l_b}} \end{aligned} \tag{5.14}$$

In the last calculation use has been made of the identity

$$a^n - b^n = (a-b) \cdot \underbrace{\left(a^{n-1} + a^{n-2}b + \cdots + b^{n-1}\right)}_{\sum_{i=0}^{n-1} a^{n-1-i}b^i} \tag{5.15}$$

where n is the number of transistors. Since in general the load impedance is different from Z_c, part of the incident wave will be reflected. The reflected wave $E_{r,out}$ is related to the to the incident wave $E_{i,out}$ through the reflection coefficient

$$\Gamma_{out} \triangleq \frac{E_{r,out}}{E_{i,out}} = \frac{Z_{out} - Z_c}{Z_{out} + Z_c} \tag{5.16}$$

The voltage in the output is thus related to the incident wave by

$$v_{out} = E_{i,out} + E_{r,out} = E_{i,out} \cdot \frac{2Z_{out}}{Z_{out} + Z_c} \tag{5.17}$$

Combining 5.14 and 5.17, the general expression for the voltage gain of a traveling amplifier can be obtained:

$$A_v = \frac{v_2}{v_1} = -g_m \left(Z_{out} || Z_c\right) \cdot e^{-(\gamma_c l_c + \gamma_b l_b)/2} \cdot \frac{e^{-n\gamma_c l_c} - e^{-n\gamma_b l_b}}{e^{-\gamma_c l_c} - e^{-\gamma_b l_b}} \tag{5.18}$$

In the special case of synchronization between base and collector line ($\gamma_c l_c = \gamma_b l_b = \gamma l$), the voltage gain can be written as

$$A_v = -n \cdot g_m \left(Z_{out} || Z_c\right) \cdot e^{-n\gamma l} = -n \cdot g_m \left(Z_{out} || Z_c\right) \cdot e^{-n\alpha l} e^{-jn\beta l} \tag{5.19}$$

where $\gamma = \alpha + j\beta$ and α and β are the attenuation and phase constants of the transmission lines, respectively. In the analysis above, we neglected the base access resistance. It is interesting to note that, in equation (5.19), the gain shows a linear dependance on the number of stages n. However, it will be shown that the line attenuation, especially when bipolar devices are used, is responsible of the limitation in the number of stages that can be successfully added. This is because the power received by the n_{th} will be sufficient to excite its output and it will simply behave as a passive rather than active device.

Bipolar-based Traveling Wave Amplifier Design

The HBT distributed amplifier gain-bandwidth performance is limited by several factors compared to HEMT and MESFET design. The three main limiting factors are [71]:

1. input capacitance C_{be}
2. the input transmission line attenuation factor, dominated by device input losses
3. the output transmission line attenuation factor.

The first factor limits the cut-off frequency of the resulting TWA, while the last two factors limit the number of section that can be beneficially cascaded to increase the output power and the gain-bandwidth performance. The base-emitter capacitance, together with the inductance used to construct the synthetic transmission line of the amplifier, sets the maximum input line cut-off frequency (equation 5.6).
The input transmission line attenuation is caused by the losses due to passive microstrip lines as well as device input impedance characteristics. For bipolar transistors, the losses related to the finite base resistance dominate the attenuation on the base line. This attenuation reduces the number of sections that can be beneficially added. Output line attenuation is affected by the finite output conductance of the device.
Bipolar transistors are characterized by a very low output conductance in comparison to FET's, leading to low attenuation for the collector transmission line. However, in spite of their higher f_{MAX}, bipolar-based distributed amplifiers have been demonstrated a maximum operation frequency equal to $60\% f_{MAX}$ [71]. Figure 5.9 shows the synthesized input and output transmission lines using bipolar devices. The input transmission line is periodically loaded by the base and is represented by a series base resistance $R_{bb'}$ and

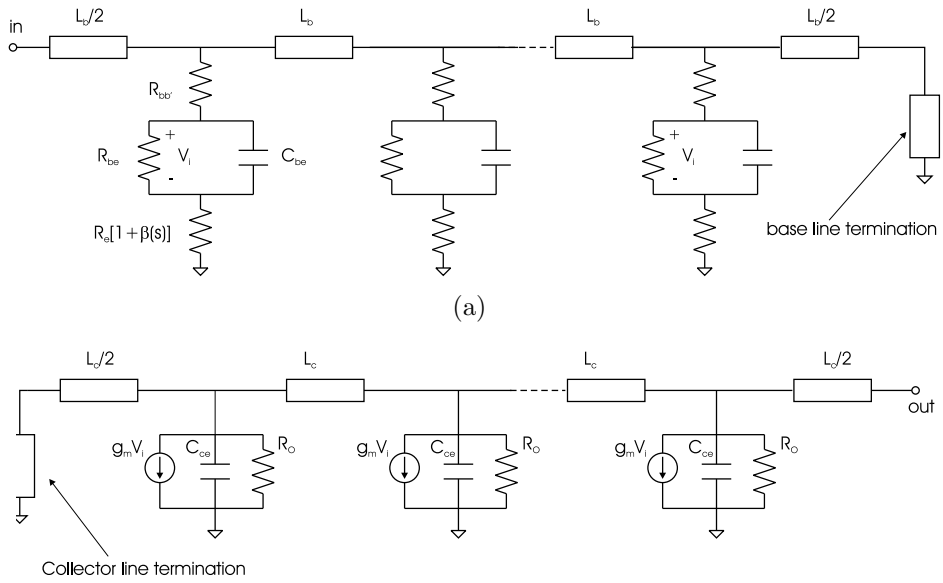


Figure 5.9: Synthesized distributed input (a) and output (b) transmission lines using bipolar devices.

shunt R-C network consisting of resistance R_{be} and capacitor C_{be} in series with an emitter resistance $R_e(1+\beta(\omega))$. The output load line is loaded by the collector output conductance $g_0(=1/R_O)$ of the transistor. The transconductance g_m couples input and output lines. The attenuation factor can be calculated by using a simple lossy line model and is given by [71]:

$$\alpha_i \approx \frac{1}{2}\left[\frac{Z_0}{R'_e + R'_{bb'} + \left[|\beta(\omega)| \cdot \left(\frac{1}{g'_m + R'_e}\right)\right]} + \frac{R'_i}{Z_0}\right] \cdot \frac{N}{m} \tag{5.20}$$

where

$$|\beta(\omega)| = \left[\frac{\beta_0}{\sqrt{1+\omega^2 R_{be}^2 C_{be}^2}}\right] \tag{5.21}$$

is the magnitude of the frequency dependent forward AC current gain of the transistor, β_0 is the current gain at low frequencies, R'_i is defined as the input transmission line series resistance per unit length and all primed variables are normalized (per unit length) quantities. From the expression of α_i it is evident that the attenuation strongly depends on the parasitic resistances of the transistor. The last term is the series resistive contribution of the artificial transmission line. The output attenuation can also be expressed in

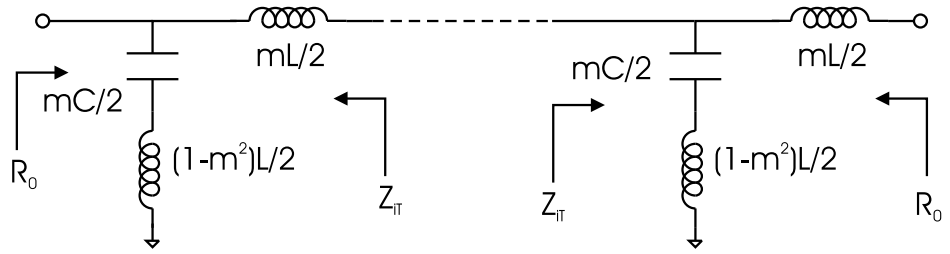


Figure 5.10: Half-Pi termination of the base and collector line. The parameter m is usually equal to 0.6. Z_{IT} is the image impedance of standard L-C tee-section.

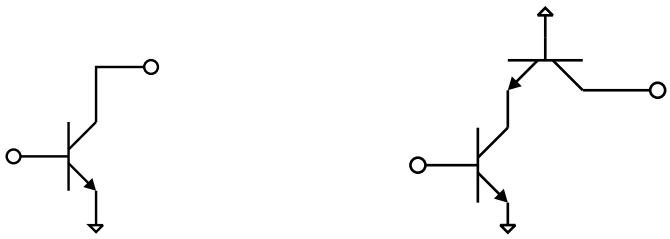
a similar manner, except that it has only contributions due to transistor output conductance that is relatively small:

$$\alpha_o \approx \frac{1}{2}\left[g'_o Z_0 + \frac{R'_o}{Z_0}\right] \cdot \frac{N}{m} \tag{5.22}$$

Also in this last equation the first term represents the loss due to the device output conductance while the second one represents the loss due to resistance attenuation of the output line.
Although the output attenuation is relatively small compared to the input one, it still affects on the performance of the system. Please note that the above expressions do not consider the base-collector capacitance of the bipolar transistor. It worth to note that in the above analysis we consider each artificial constant-k line terminated with its own image impedance. This is not a realistic scenario due to the dependence of the characteristic impedance with frequency. However, it is still possible to have a flat characteristic impedance of the line from DC to the cut-off frequency of the line by terminating it with a so called "half-pi" circuit (figure 5.10).

Gain Cell Topologies

The most traditional topology of the gain cell is represented by a common-emitter transistor (figure 5.11(a)). This configuration, as claimed many times, is prone to high-frequency gain degradation due to the Miller effect related to the base-collector capacitance. Moreover, the reduced emitter-collector breakdown voltage does not allow for large output voltage swing. These problems can be circumvented by using a *cascode* configuration (figure 5.11(b)).
In a cascode amplifier, due to the small input resistance of the common base stage, the base collector capacitance is not affected by the Miller effect. The voltage on the output node is now limited by the BV_{CBO} breakdown voltage, which normally is about two times BV_{CEO} and the output losses are



(a) Common emitter

(b) Cascode

Figure 5.11: Gain cell topologies.

reduced due to the higher output impedance of the common-base stage. The last advantage of the cascode configuration is that it can be considered as a single-pole stage.
Unfortunately, the standard cascode configuration is not unconditionally stable for the whole frequency range of interest. This is because the real part of the output impedance of a cascode stage can become negative in some frequency range, so that proper stabilizing networks have to be designed in order to avoid spurious oscillations. The common-emitter design and the cascode configurations were found to provide limited values of gain due to the access resistance of the transistor base terminal. The reduction of this resistance could help to improve the gain-bandwidth characteristics of distributed amplifiers using common-emitter or cascode active cell design. This reduction is based on the attenuation compensation technique [71, 72], namely a common collector stage followed by a cascode transistor pair. Figure 5.12(a) illustrates a common-collector device, which actively transforms a capacitive impedance at the emitter in order to generate a negative impedance at the base (input). The bipolar transistor transforms the capacitor at the emitter to an impedance at the base, which can be represented as a capacitor C in parallel with a series negative resistance $-R_{be}C_{be}/(\beta_0 C)$ and a negative capacitance $-\alpha_0 C$. Proper attenuation compensation can be obtained when the base and emitter resistances of the device are canceled out by the negative resistance generated by the transformation. This results in an effective input impedance that has no real part.
The equivalent circuit of the input impedance is illustrated in figure 5.12(b). By inspection it is possible to see that the capacitances C and $-\alpha_0 C$ cancel each other. The attenuation of the series resistive losses due to R_{be} and R_e can be directly canceled by the negative resistance $-R_{be}C_{be}/(\beta_0 C)$: by equalizing the resistive losses with the negative resistance it is possible to calculate the proper value of the compensating capacitance C. In practice, however,

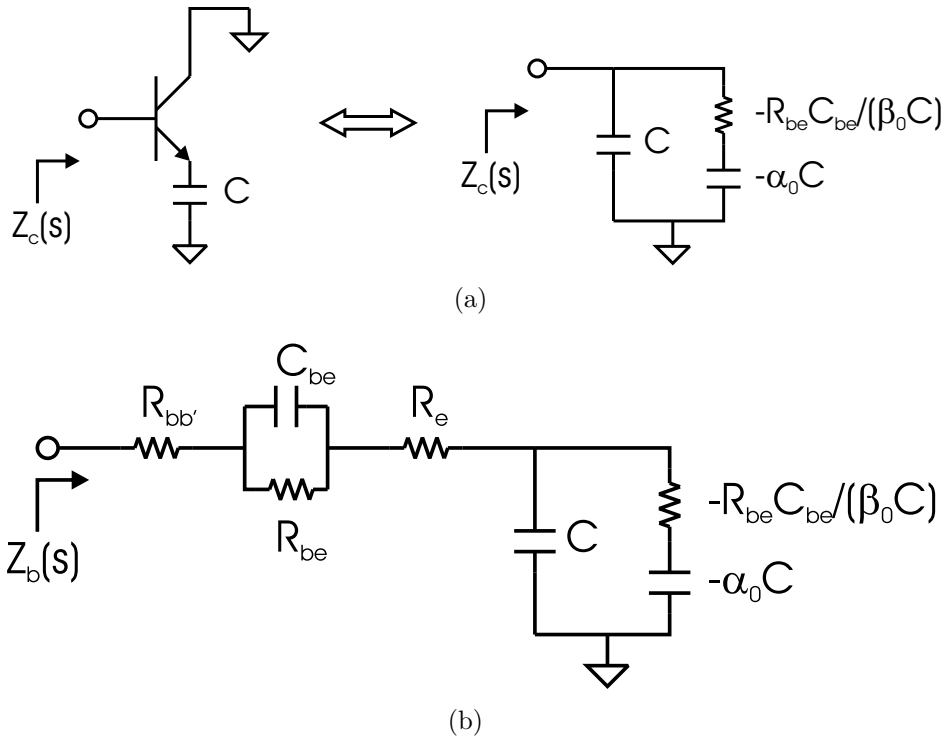


Figure 5.12: Active impedance transformation of a capacitance C at the emitter of a common collector stage.

since this common-collector stage is present at the input of the amplifier, a more complex R-C network must be considered at its emitter (Figure 5.13). Therefore the above calculated compensation capacitance is overestimated and computer simulations are needed to optimize the size and bias of transistor Q for a broad-band loss-less input impedance.

The last factor that affects the design of a distributed amplifier is the lower band limit. This is currently attributed to the DC-blocking capacitors of the load terminations and to the AC-coupling capacitors at the input and output of the amplifier, which are often monolithically integrated using MIM (Metal-Insulator-Metal) capacitors. The input and output AC-coupling capacitors, in combination with the 50Ω system impedance, provide a high-pass pole whose frequency is given by $1/(2\pi R_{system} C_{coupling})$. The dc-blocking capacitors also form a frequency pole. In order to achieve lower frequency operation, large value of MIM capacitors are required, which may not be practical to implement on chip. A convenient solution is to incorporate active loads to terminate the input and output transmission lines [73]. The active load

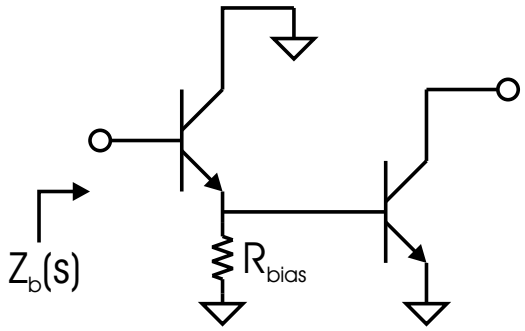


Figure 5.13: Practical configuration of common-collector input transistor.

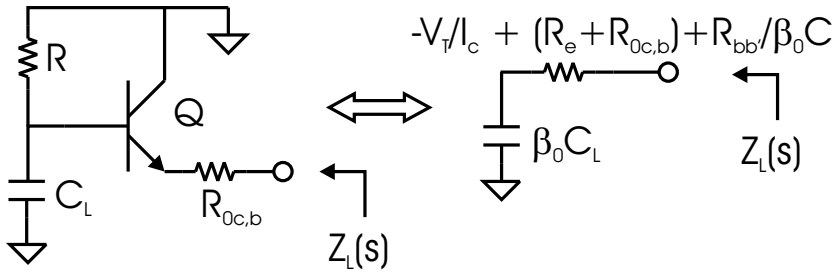


Figure 5.14: Active transmission line load transformation and its low-frequency equivalent circuit.

consists of a common-collector device that transforms a shunt load capacitance on the base to an effectively larger load capacitance when looking into the emitter. Figure 5.14 conceptually illustrates the active load impedance transformation. The active load extends the low frequency limit by effectively multiplying the capacitance value of the MIM capacitor C_L by β_0. Since the capacitance value is proportional to the area of the passive component, this technique corresponds to a significant saving in chip-area.

5.2 Traveling wave amplifier examples

As often stated, broadband distributed amplification is traditionally considered a domain for III-V technologies. This has been found to be partially due to the inherent higher operating frequency of GaAs- and InP-based devices compared to their silicon counterparts [74]; moreover, the semi-insulating nature of III-V substrates facilitates the realization of low-loss transmission lines and inductors, which are essential for the design of a traveling wave amplifier (TWA). However, the goal in all circuit design efforts is to reduce the manufacturing costs without compromising the performances: the silicon technology that enables the realization of high speed circuits with performance about comparable to the expensive III-V counterparts then represents the ideal solution. With the recent improvements in SiGe bipolar technologies (f_T and $f_{MAX} > 200$ GHz [58]), one can conclude that the bottleneck for the implementation of silicon TWAs is no longer to be attributed to the active devices, but lies in the low-Q passives related to the lossy silicon substrate. Owing to this, to the author best knowledge, the few successful distributed circuit implementations in silicon are represented by a 12 GHz distributed voltage controlled oscillator [69], by a $0.5 - 8.5$ GHz differential [75] and by a $0.5 - 5.5$ GHz CMOS amplifier [76]. In [77], instead, the artificial transmission lines have been implemented by using package inductances. Recently, a 50 GHz bandwidth but with a modest in-band gain has been reported in [78] using a sophisticated IBM BiCMOS SiGe process together with half-pi terminations. The design presented here is a traveling wave driver for 10 Gb/s optical communication systems. This circuit is intended as a technology demonstrator for the surface-passivated high-resistivity silicon (pHRS) DIMES03 technology. It will be shown that through the use of additional processing steps, including an argon implant, it becomes possible to integrate the high Q (> 20) inductors required for a TWA design and hence achieve broad band operation even with an in-house laboratory process.

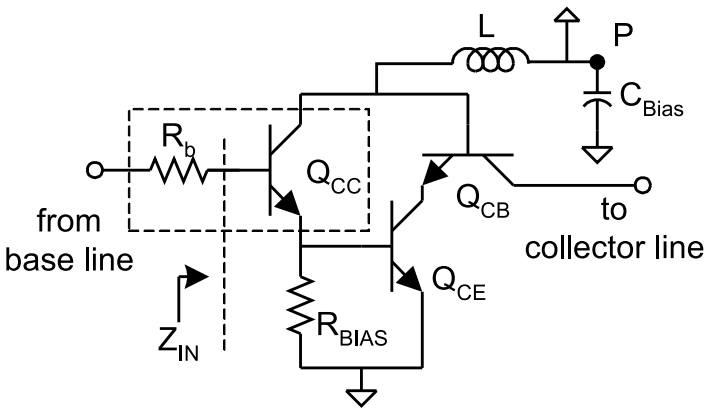


Figure 5.15: Modified emitter-follower cascode gain cell for higher MAG (Maximum Avaailable Gain) at high frequencies.

Active stage design

The traveling wave amplifier is composed of two gain stages. Each stage is implemented in a modified emitter follower-cascode configuration (figure 5.15), with the input transistor Q_{CC} capacitive loaded by the common emitter stage of the cascode Q_{CE} [79]. By proper dimensioning of the transistor sizes we can attain a capacitor-like input impedance compensation, while at the same time compensating for R_b through the negative real part of the Z_{IN} of the emitter follower yielding an effectively shunt loss-free base line. The cascode stage, on the other hand, reduces the output shunt conductance. This is because, with respect to the common emitter configuration (see eq. 5.22), the output shunt conductance of a cascode is reduced by the AC beta of the transistor:

$$g_{ocascode} = \frac{2}{\beta_o} g_{oce} \tag{5.23}$$

that directly results in a reduced attenuation at the collector line. At the same time a cascode stage increases the bandwidth by eliminating the Miller effect for the transistor Q_{CE}. Moreover, higher output voltage levels are permitted since we are restricted by B_{VCBO} rather than BV_{CEO} [80].
In this design we further lower the losses related to base and collector lines by inserting an inductor (L in figure 5.15) between the base-collector connection of $Q_{CB} - Q_{EF}$ and the bias point P. As a result, the real part of the input and output impedances can be made slightly negative and the imaginary parts behave as pure capacitors at the frequencies of interest. In this way the series resistive losses on the lines are compensated. Note that the improved transistor stage has a significantly higher gain at high frequencies

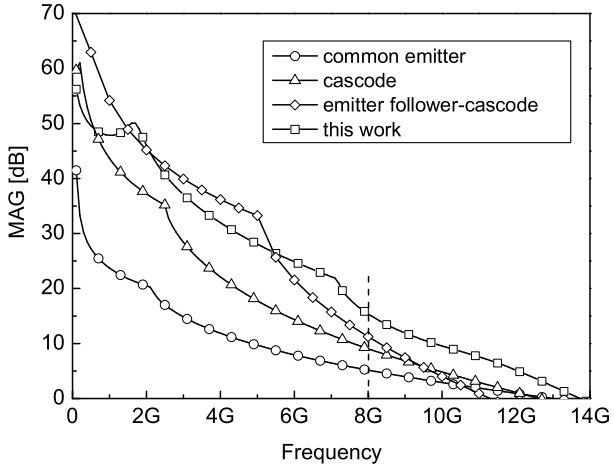


Figure 5.16: Simulated maximum available gain for different gain topologies. At high frequencies the proposed stage provides an higher MAG in comparison to other circuit schemes.

compared to more conventional stages (figure 5.16).
Following the gain stage optimization, the artificial transmission lines need to be optimized. Note that, even with a high-resistivity substrate, the circuit design is quite complicated since layout parasitics can easily lead to unexpected amplifier performance. To overcome these problems we extensively used Agilent Momentum EM simulator. By careful simulating the required inductors and, finally, the whole layout in combination with active devices, the overall TWA design was optimized [81]. The simulated S_{21} after this layout-schematic-layout optimization is given in figure 5.17.

Circuit fabrication and technology considerations

The two-stage traveling amplifier of figure 5.18 has been fabricated using DIMES03 bipolar silicon technology developed at University of Delft laboratories. The measured f_T of the active device is given in figure 5.19. The devices used for this measurements were located on the same wafer and in proximity of the full circuit in order to reduce the effect of process spreading. To implement the artificial transmission lines, lumped inductors have been preferred to transmission lines, as in III-V based technologies. This is motivated by the excessive length of lines needed to synthesize the required inductance. When implementing these inductors in conventional silicon technology, however, poor quality factors result, due to the low resistance of the

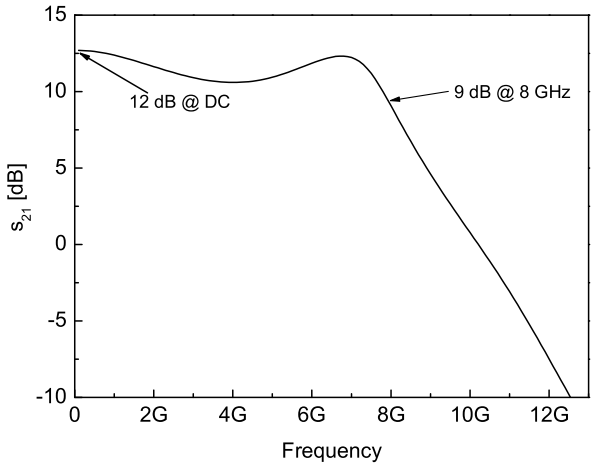


Figure 5.17: Simulated small signal gain of the DIMES03 traveling wave amplifier including layout effects. The layout has been simulated with MoMentum EM solver.

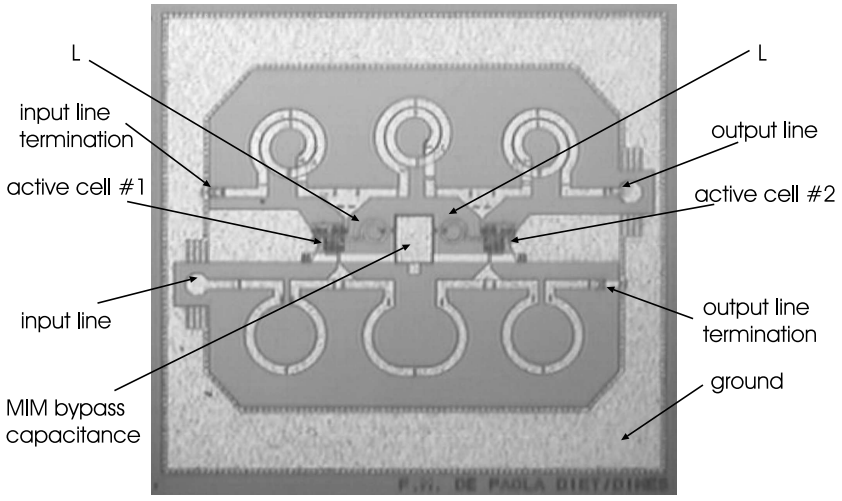


Figure 5.18: Photo of fabricated distributed amplifier. The chip size is $2242 \times 2099 \mu m^2$.

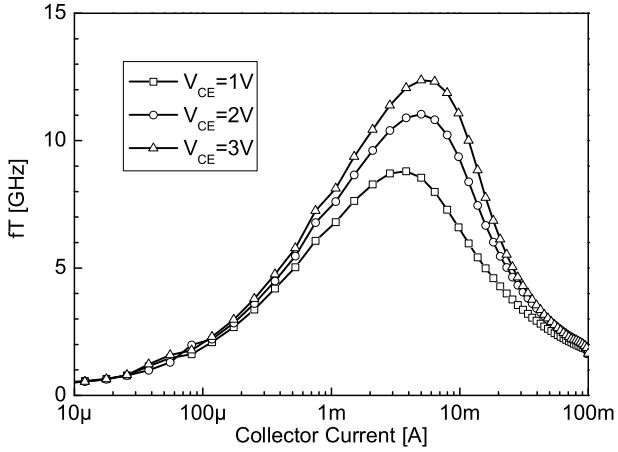


Figure 5.19: Measured f_T of a DIMES03 NPN32x1 device. The f_T is measured as a function of collector current at a given collector-emitter voltage.

bulk silicon substrate. To reduce this undesired effect, it is possible to introduce high ohmic substrates in the IC-fabrication process.
Unfortunately, in spite of what stated above, passive components integrated on a high-resistivity substrate still suffer from much higher losses than predicted by EM simulators like Momentum. This can be related to the presence of a surface charge layer at the silicon-insulator interface. This charge layer is responsible of additional eddy currents, and therefore deteriorates the high-frequency performance.
In order to reduce the effect of this surface charge, argon has been implanted underneath the integrated passives [82]. This implantation completely amorphizes the silicon substrate, reducing the effective mobility and, consequently eddy currents. Although the Ar-implant technique was successfully applied

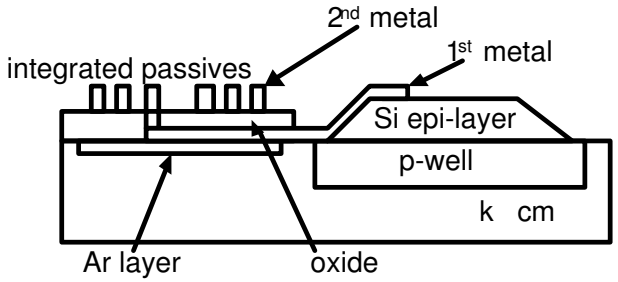


Figure 5.20: Schematic cross section of the passive and active device structures in DIMES03 on SP-HRS.

Table 5.1:

Characteristics of fabricated inductors. Metal thickness is 3 μm.

	L $[nH]$	W $[\mu m]$	n	outer R $[\mu m]$	Q_{SIM}	Q_{MEAS}	f_{MAX} $[GHz]$	s $[\mu m]$
	0.8	40	1	180	**21**	**21**	4	-
	1	40	1	230	**29**	**27**	3.8	-
	1.6	40	2	180	**24**	**24**	4.2	6
	2	40	2	180	**22**	**27**	4	6

for the improvement of the quality of integrated passive devices [82], it has been never combined with active devices before. Three extra step are required to extend the normal silicon process to that required for a high-resistivity substrate (figure 5.20), namely:

1. deep p-well to realize a junction isolation of the silicon devices (NPNs, resistors and diodes)

2. trench-etching to remove the epitaxial layer in which silicon devices are made, together with an extra-planarization

3. argon implantation through surface SiN_x passivation layer.

Note that the creation of the amorphous silicon layer must be one of the final steps of the wafer processing in order to avoid the recrystallization of the amorphous regions at high temperatures. More details about technology are given in Appendix A.
Table 5.1 shows the dimensions, simulated and measured loaded maximum quality factors for the different inductors in the design. The frequency corresponding to the maximum measured Q is also reported. Inductors in different zones of the wafer have been measured and no spread of data was noticed. The good agreement between simulations and measurements together with the uniformity of results clearly indicates the need of the argon implant.

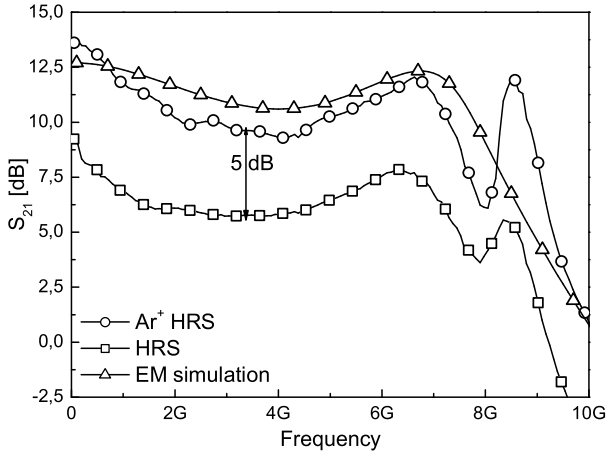


Figure 5.21: On-wafer measured characteristics of the DIMES03 traveling wave amplifier. Ar+ HRS clearly yields an increase of the in-band gain.

Experimental results

A HP8510C vector network analyzer was used to measure the integrated TWA. For calibration we have used the line-reflect-reflect-match (LRRM) method in combination with GSG coplanar probes. An extra DC needle was applied in conjunction to a large MIM integrated capacitor to provide the additional bias of the common-base stage on the chip (P in figure 5.15). With a collector line bias of 8 V, a base line bias of 1.8 V and a bias of 5 V for the base voltage of the cascode, we achieved a 10 dB flat gain and a 7.5 GHz bandwidth (5.21). A clear improvement of 5 dB of the in-band gain when using argon implant is observed. Note that the gain peaks again beyond 8 GHz. This is due to some misplacement of one of the pole pairs. We will not refer to this peaking in the rest of our discussion, but it clearly indicates the gain-bandwidth potential of the proposed design technique as well as of the technology. Note that the gain roll-off at 7.5 GHz of this amplifier is quite smooth, which is important for digital applications, since the sharp gain roll-off often seen in distributed amplifiers will cause excessive in-band group-delay peaking, thus deteriorating the eye diagram of the system [59]. The group delay deviations were within 0.15 ns up to 8 GHz (figure 5.22).
In order to compare the performance of our amplifier with other works, it is possible to introduce a figure of merit [83] defined as the ratio of the -3dB cutoff frequency of the amplifier to transistor f_T. Table 5.2 shows a comparison between our amplifier and state-of-the-art devices realized in III-V technologies. From this table it is obvious that, despite the much lower f_T,

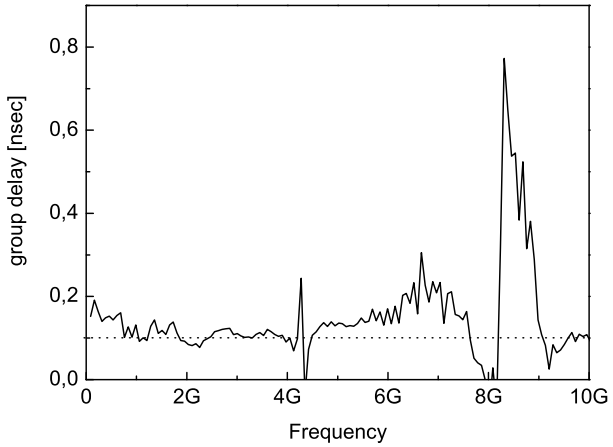


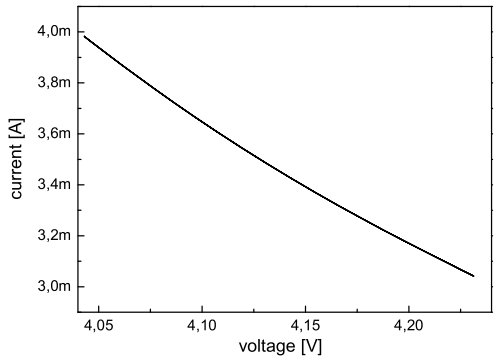
Figure 5.22: Group delay of the DIMES03 TWA as calculated from measured s-parameters.

Table 5.2:

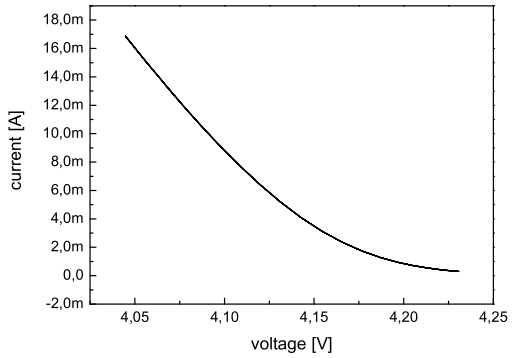
COMPARISON OF DIFFERENT TECHNOLOGIES

Technology - device	f_{-3dB} $[GHz]$	f_T $[GHz]$	Gain $[dB]$	f_{-3dB}/f_T
InP - HEMPT [83]	92	130	13	0.70
InP - HBT [59]	74	150	13	0.49
SiGe - HBT [78]	50	120	6	0.42
SOI - CMOS [84]	91	150	5	0.60
this work	**7.5**	**13**	**10**	**0.57**

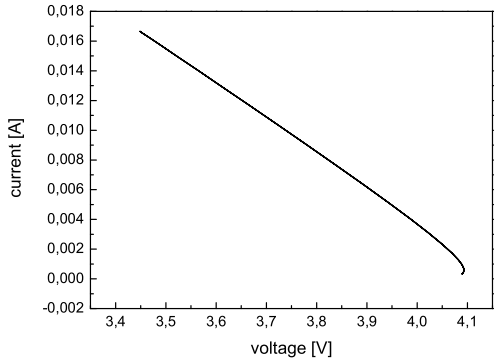
our design is still able to achieve a considerable bandwidth.
This circuit, however, presents some drawbacks. As can be seen in figure 5.15, both the gain stages require a bias voltage at the point P. In order to reduce the parasitics associated with the bias line, the layout of the first stage was mirrored. Unfortunately, this solution practically did not allow more than two stages. Furthermore, in an hypothetical flip-chip module, accessing the mentioned bias pad would have posed serious problems. Another problem was found to be the limited output power gain of the circuit as the input power increased (figure 5.24). This was found to be due to the low current capability of the common emitter and common base transistors that yields clipping effects in the load line (figure 5.23), even with very low input power levels (i. e. -10 dBm). In order to overcome the above mentioned problems and to accomplish the output power levels to correctly operate the InP-based optical modulator described in section 2.3.1, a new driver has been designed.



(a) Emitter follower stage.



(b) Common emitter stage.



(c) Common base stage.

Figure 5.23: Simulated load line for the stages of the gain cell. The input power to the TWA is -10 dBm. In (b), the common emitter stage, a clipping effect can be noticed.

Improved TWA for flip-chip module

In order to provide more power to the load (that can be considered a 50Ω resistor), the number of stages must be increased. Also the artificial base and collector lines need to be optimized to better absorb gain stages capacitances. By recalling transmission line theory, a transmission line loaded with two capacitances (one at the input and one at the output) can be designed to present a given characteristic impedance Z_c and electrical length $\Theta = \pi/2$ (figure 5.25). This can be easily verified by equating the $ABCD$ representation of the two transmission lines:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{cases} \begin{bmatrix} 0 & jZ_c \\ \frac{j}{Z_c} & 0 \end{bmatrix} \text{ unloaded} \\ \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ\sin\theta \\ \frac{j\sin\theta}{Z} & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \text{ loaded} \end{cases} \tag{5.24}$$

with $Z > Z_c$, yielding

$$\begin{aligned} \cos\vartheta &= \omega C Z_c \\ Z &= \left(\frac{Z_c}{\sin\vartheta}\right) \end{aligned} \tag{5.25}$$

If C is the input or output capacitance of each gain stage, it is possible to extract the values of Z and Θ to achieve a 50Ω, $\lambda/4$ transmission line. However, the capacitance C cannot vary in a very wide range, since it must always be limited to $Z_c\omega C < 1$.
Once the input and output capacitance have been optimized (by changing the size and the bias of the emitter follower and common base stage) the power requirements of the load have to be accomplished. Since an output voltage swing of $6V_{PP}$ is required on a 50Ω load [3], corresponding to 19 dBm output power, more stages have been used (i.e. five). Also, in each stage, the transistors in the common emitter and common base stage have a larger area (see figure 5.26) with respect to the emitter follower stage. Since DIMES03 transistor models are not scalable, several transistor in parallel have been used to increase the current capabilities of the stage. In this way it has been possible to improve the current handling capabilities of the 2^{nd} TWA design in respect to the original design.

[3]The goal is to operate the optical modulator presented in section 2.3.1 as an analog modulator. Since $V_\pi = -6V$, the bias has been set to $V_\pi/2$ when the superimposed modulating signal has a peak-to-peak value of 6V.

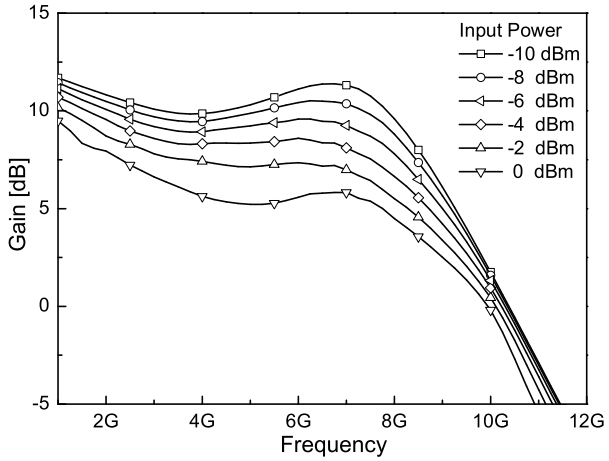


Figure 5.24: Simulated power gain for different input powers. As the input power increases, a clear reduction of the output power is visible, indicating clipping effect in some of the active devices.

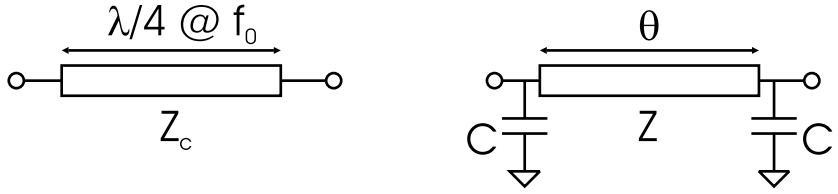


Figure 5.25: Principle of capacitance absorbtion into transmission line.

The effective active emitter area is different for the CE stage and the CB stage in order not to load the output line with an excessive capacitance. Further, the CB stage can tolerate higher current densities since the frequency behavior is not critically dependent on the collector current as for a CE stage. However, the minimum number of transistors is set by the current density, since a high current density can easily burn the device. The circuit topology of figure 5.26 has only two bias points, corresponding to the RF input and output ports, so the probing and the flip-chip mounting is facilitated. The capacitance C_{bypass} is used to AC-ground the common base transistor and to improve the cascode isolation. Resistor R_E is used to further decrease the capacitive loading of the of the output cell on the input artificial transmission line [85]. Resistor R_2 is used for biasing purpose and for dumping the unwanted resonances that may arise from the combination of the bypass capacitor C_{bypass} and the parasitic ground inductance.

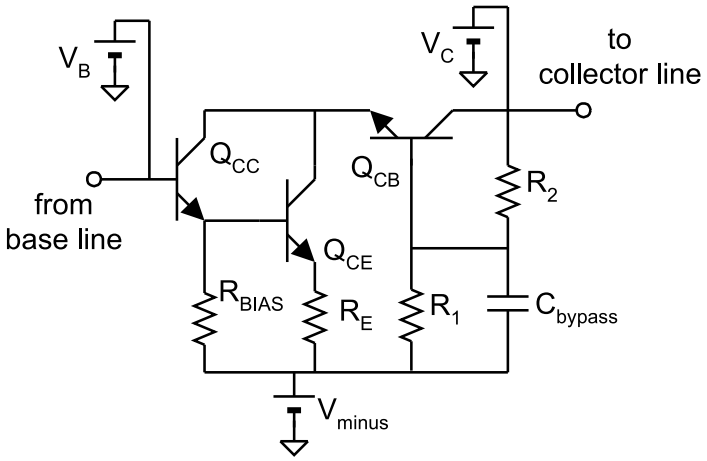


Figure 5.26: Improved gain cell: Area $Q_{CC} = 1$, Area $Q_{CE} = 4$, Area $Q_{CB} = 2$, $R_{BIAS} = 200\Omega$, $R_E = 25\Omega$, $R_1 = 3k\Omega$, $R_2 = 6k\Omega$, $C_{bypass} = 8pF$, $V_{minus} = -18V$, $V_B = -15.84V$, $V_C = -3V$.

The DC voltage levels have been set to negative values, to allow high voltage swing in the output while keeping the quiescent DC point of the Mach-Zehnder modulator in the output at $-3V$. The simulated input and output reflection coefficients of the improved gain cell are given in figure 5.27. It is possible to note the capacitive behavior of the output impedances up to the design band (7 GHz). The output impedance presents a slightly negative real part to compensate for resistive losses on the collector line.
In order to calculate the optimum values for the loading capacitances and the corresponding characteristic impedance of the unloaded line (or equivalently its electrical length), a five-stage traveling wave amplifier with the active stage substituted by an ideal voltage controlled current source has been studied by means of circuit simulations. The input and output capacitances effects were included by adding two capacitors at the input and the output of the controlled source. The resulting output voltage for a 7 GHz signal together with the values of the capacitances are given in figure 5.28. It is evident that the output voltage is suitable for driving the optical modulator at the design frequency.
The active stage has been then designed to present identical input and output capacitances and with a value as close as possible to that obtained from the "ideal" simulation. This is required when aiming for 50Ω base and collector transmission lines, which are matched for their phase velocity. Figure 5.29 shows the input capacitance extracted from circuit simulations of the gain stage. Figure 5.30 shows a circuit schematic of the 5-stage traveling wave

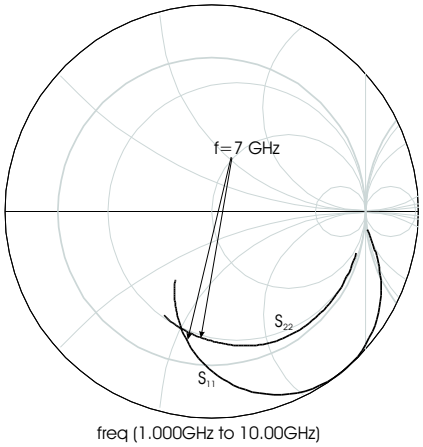


Figure 5.27: Simulated input and output impedances. s_{11} moves on the edge of the Smith chart, indicating a capacitive-like behavior up to high-frequencies. s_{22} shows a negative real part, that can be used to compensate further losses on the output line.

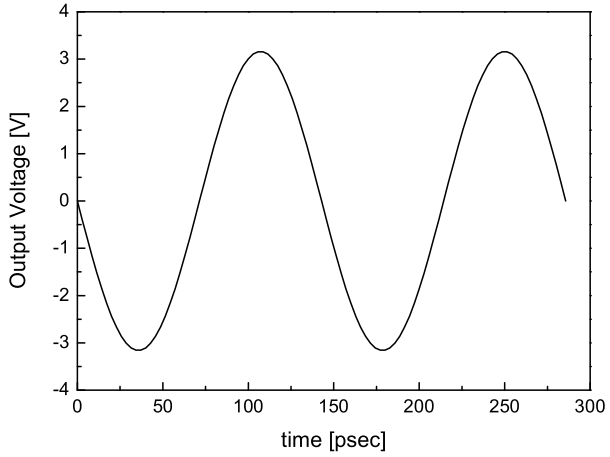


Figure 5.28: Simulated voltage at the output node of an ideal five-stage traveling wave amplifier. The value of capacitances and the corresponding characteristic impedances of the unloaded line that optimize the voltage level are $0.56pF$ and 63Ω.

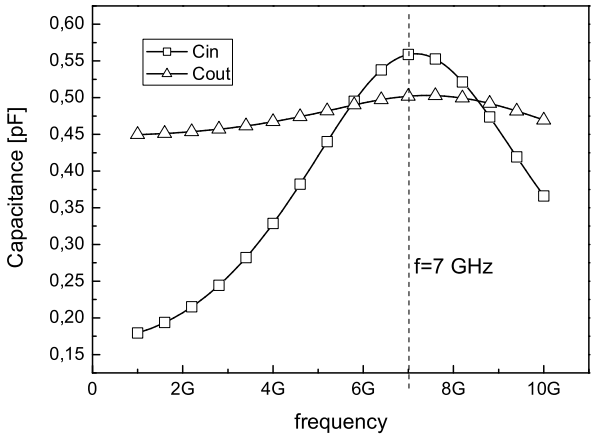


Figure 5.29: Extracted frequency-dependent capacitance of the improved gain cell. At the marked frequency $C_B = 0.55pF$ and $C_C = 0.50pF$.

amplifier. Bypass MIM capacitors C_t are used to avoid drawing DC current in the 50Ω input and output matching resistors. However, the C_t capacitors give a bandpass structure to the amplifier. In theory, C_t can be chosen arbitrarily high to satisfy any low-frequency system requirement. Practically, the C_t size is limited by its resonant frequency as well as area consumption.
The base and the collector lines are biased through the network analyzer bias-tees. Finally, the layout of the five-stage TWA is given in figure 5.31. The artificial lines are clearly visible, together with the capacitances added at the input, output and at the terminations. The simulated small signal parameters of the 5-stage TWA are given in figure 5.32, where the results of MoMentum simulations are compared to the ideal case, i.e. with the transmission lines implemented as ideal loss-free elements. The layout has been completely EM-characterized by extensive MoMentum simulations. The low frequency peaking of the small-signal gain is explained by the fact that, at such frequencies, the transmission lines behaves like short circuits and then the five-stage are effectively in parallel, causing the output currents to add in phase. Moreover, the capacitor C_t cannot block this low frequency peak because the effective load of the five parallel stage is the output 50Ω termination.
Large signal analysis has been performed by means of harmonic-balance simulations. Figure 5.33(a) shows the output power for different input power levels. The decrease in the output power that was affecting the previous design is not present here, allowing a higher input power swing. An appropriate output power is reached with a 5 dBm input, see figure 5.33(b), where also

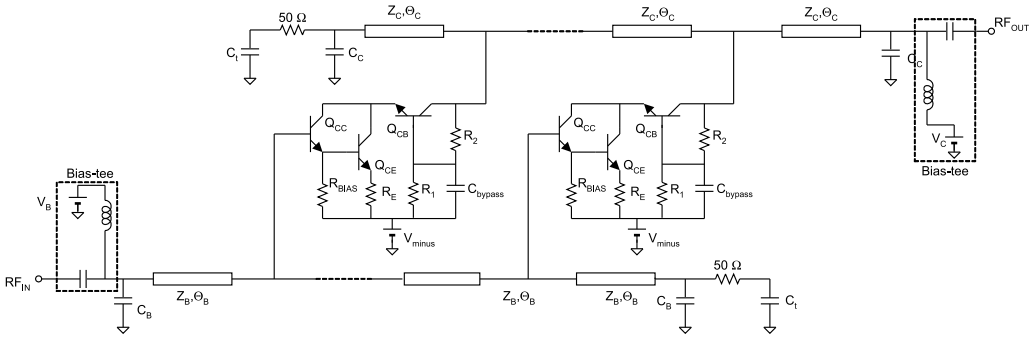


Figure 5.30: Five-stage traveling wave amplifier circuit schematic. The DC blocking capacitance C_t has been set to 8 pF.

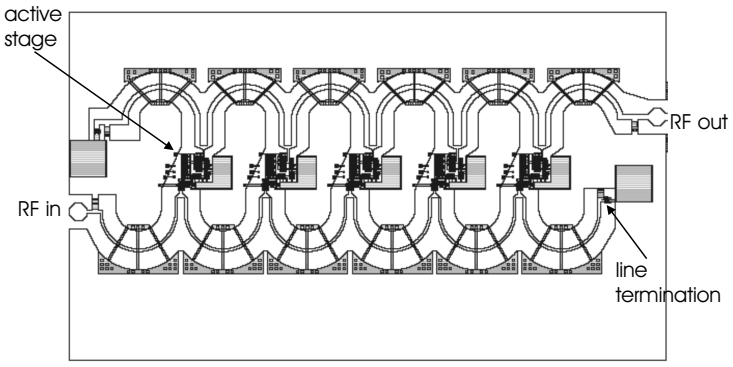


Figure 5.31: Layout of the improved five-stage DIMES03 TWA. The layout size is $3444 \times 2005 \mu m^2$.

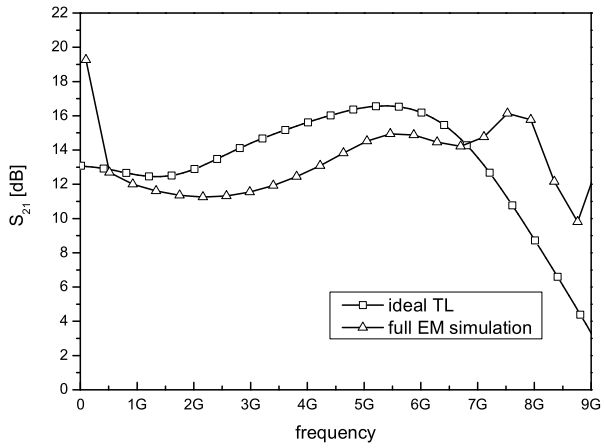
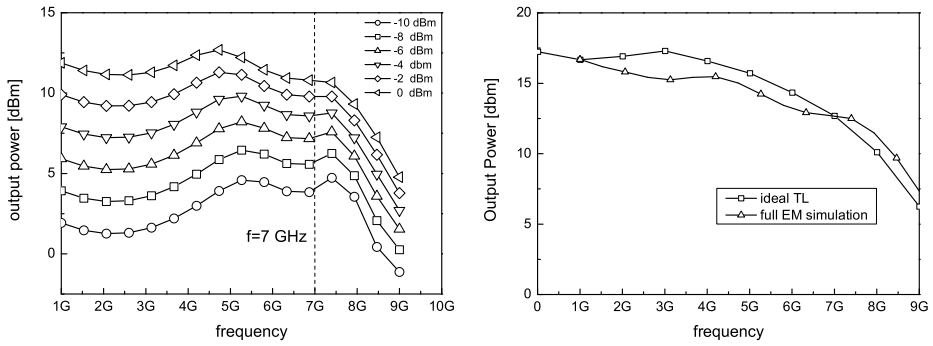


Figure 5.32: Comparison between simulated small-signal gain S_{21} of the ideal five-stage amplifier, implemented with loss-free transmission lines, and the result of MoMentum EM simulation.

the result of the ideal simulation with loss-less transmission lines is given for comparison. The good agreement between EM simulations and expected performances clearly indicates the potentialities of the circuit. In view of a final flip-chip bonding with the optical modulator, the layout of the silicon substrate has been optimized to facilitate optical probing while providing, at the same time, the modulating RF signal. It is worth nothing that the position of the micro-manipulators in the probing station is fixed. A low loss 50Ω coplanar access line, with air-bridges on the first metal layer, has then been designed at the output of the modulator. The DC decoupling capacitors are mandatory to DC isolate the lowest potential paths of the driver and the modulator. By placing the capacitors only on the ground path it is then possible to transmit the RF signal and, at the same time, to shift the reference DC points. Finally, saw lines above and below the module are laid-out to facilitate the coupling of optical fibres via a fiber-boat for testing. At the time of writing, the module is under processing.

Before concluding this overview of design techniques and examples, it is worth to spend few word to summarize the design trade-offs that are behind the design of a traveling wave amplifier to get simultaneously high output power levels and wide bandwidth. First of all, the power requirements and the impedance of the load typically set the current that must be provided by the driver to accomplish them. Since the load impedance could not be controlled in our design (even if some suggestions for removing this restrictions



(a) (b)

Figure 5.33: Simulated output power for the improved DIMES03 driver. (a)Output power of the five-stages DIMES03 TWA for different input powers: the TWA is not suffering the power limitations of the previous design. (b) Output power for an input power level equal to 5 dBm: the result of the ideal simulation is given for comparison.

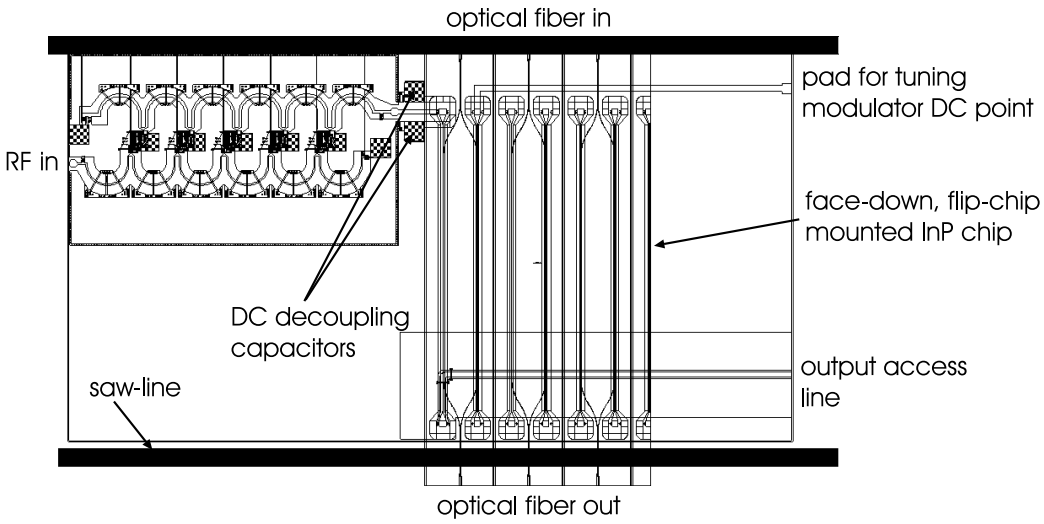


Figure 5.34: View of the final hybrid module Si-InP. Note the routing of the metal trace and the position of the face-down optical chip to facilitate electrical and optical probing.

have been provided in section 2.3.2), the only way to reach the proper current levels seemed to be laddering more stages. However, this solution is not always suitable, due to the fact that, as explained, more stages can be ineffective if the wave traveling on the base line has been too attenuated to excite them. It is possible, then, to increase the current that is provided by each stage by using large transistors. This solution, instead, limits the maximum bandwidth of the amplifier, since it has been demonstrated that the maximum cut-off frequency of the loaded transmission lines is dependent on the capacitance that must be absorbed, for a given electrical length (and then phase shift) of the line. This is the main reason of the bandwidth limitation of the improved amplifier design, since higher frequencies would have required smaller capacitances, smaller transistors and then lower current densities.

Chapter 6

Conclusions and Recommendations

Summary

Low cost optoelectronic modules can be fabricated combining the optical capabilities of III-V components with the superior performances of silicon technologies in terms of mechanical stability, very large scale integration and manufacturing costs. The electrical and mechanical properties of III-V base photonic ICs, namely InP device, can then be enhanced by means of a technology that allows their mounting onto a carrier with better thermal, electrical and manufacturing characteristics. Proposing and motivating technology demonstrator for such a hybrid packaging technology has been the scope of this thesis.
Several aspects have been considered to pursue this goal. Observing the backbone of the thesis, the different topics related to the the design and fabrication of the above mentioned demonstrators can be easily spotted.

Following a short introduction, in *chapter two* the InP-based photonic devices, which essentially represent the devices that must be packaged a/o enhanced with silicon support, are described. Due to the extreme high cost of productions of these device, an important point has been the prediction, at simulation level of their behavior, so that alternative solutions can be studied with reliable tools before real fabrications. An efficient simulation strategy has been developed to take into account, also in the optical simulations, the semiconductor-like nature of the optical devices. This is because it has been proven that for complex InP compounds, like the one used in the processing of the optical devices, the exact distribution of the carriers in the device, and then its influence of the effective refractive index variation, cannot be neglected in favor of classic linear and quadratic electro-optic effects. The core

of this strategy is represented by solving the wave equations for the determination of the optical index profile in the cross section exactly on the same grid produced by a device simulator. Simulated results of knows structures have been validated by comparisons with measured data.

In *chapter three*, a key problem for the realization of the hybrid modules has been tackled: a technology to allow the coexistence of InP chips ont a Si carrier. The most promising solutions is the flip-chip mounting technique and an important role of the research here presented is played by the quest for the best solution to create the metal interconnects that are the base for a successful flip-chip bonding. The solution described, and practically implemented within the DIMES laboratories, is based on electroplating eutectic gold-tin bumps on the carrier and then reflow them. By using such a technique, first Si-to-Si bonding and, finally, InP-on-Si samples have been fabricated. The InP-on-Si samples, consisting of a semiconductor optical amplifier array chip and a phasar chip, have been studied by means of FEM simulations.

In *chapter four*, in view of the design and realization of a module consisting of a silicon driver and an optical RF modulator, an equivalent scalable model of coplanar-to-coplanar transitions in flip-chip systems has been derived. The circuit is suitable for circuit simulators and can be used to foresee the impact of the discontinuities (i. e. the bumps) on the signal path. The circuit is furnished with regression models for each of its component and is derived from a limited number of 3D EM simulations of different structures. The model is validated by comparing the results of circuit and 3D EM simulations of different (and not included in the database generated for the regression analysis) structures.

In *chapter five* the problems related to the design of a wideband driver for optical data transmission are addressed. After an overview of standard circuit schemes, the design of a traveling wave amplifier is detailed. The amplifier is implemented with DIMES03 transistors and, in spite of a relatively low f_T of about 13 GHz, it is able to achieve a flat bandwidth of about 60% of the f_T of the active devices. This result has been made possible by modifying the standard process to include also high-resistivity substrates to reduce the substrate parasitics that lower the quality factor of the integrated passives. A second version of the amplifier has been designed to be bonded with one of the RF modulators described in chapter two. Also, the silicon space around the amplifier has been optimized to host the InP chip by routing the interconnections to facilitate the electrical and optical probing.

Conclusions and Recommendation for Future Works

In this thesis, it is described the research for realizing hybrid modules where silicon can be used to effectively improve different functionalities of the photonic device. Through simulations and experiments it has been demonstrated how it is possible to successfully combine in a single hybrid module a circuit operating in the optical domain and a substrate that provide support and interface circuitry. Moreover, attention has been payed to the technology that enables the realization of these modules. From the technology point of view, if from one hand great benefits, both on manufacturing costs and level of integration, can be obtained, on the other hand the difficulties in achieving a reliable technology for the bonding cannot be neglected.
It has been found that the most critical step in the process is the reflow of the solder bumps, provided that a reliable under-bump-metallization is available. A reliable under-bump-metallization is mandatory to ensure good adhesion of the bumps to the metal pads on the silicon wafer and to protect silicon from diffusion of metal particles from the bumps. Also, the metal combination must be selected in view of its removal after the formation of the bumps. For a good bonding and alignment it is crucial to have access a pick-and-place machine that allows for precise positioning and, at the same time, provides a controlled heated chuck to reflow the solder in-situ. Finally this last step must be performed in an inert ambient to prevent the oxidation of the solder.
From the application point of view, it has been demonstrated how it is possible to enhance some photonic devices, such as integrated optical amplifiers and phasars, by means of packaging them onto a silicon carrier. For instance, it is possible to compensate technology fluctuation, which reflects in selectivity variation, of a phasar by controlling its temperature via a heat generator on the silicon chip while it is possible to cool down an integrated optical amplifier by realizing some kind of metal pipe (the bumps) to remove the excess heat and route it to a heat sink without passing through the optical material (typically characterized by a high thermal impedance).
Finally, from the circuit design aspects, a distributed driver seems to be the ideal solution to overcome the limitation in frequency of the common amplifying schemes. However attention must be payed to the design of the artificial transmission lines, since a trade-off has been spotted between the maximum capacitance that can be effectively absorbed and the characteristic impedance of the resulting loaded transmission line. Within this project, two amplifiers have been designed. The first has been used as a case study for gain-bandwidth trade-off and technology consideration. The second design has been optimized for flip-chip mounting with a optical modulator.

The mounting of the chips will be performed within another frame in a future project.

A final topic for further studies is the optimization of the impedance of the optical modulator that is the load of the amplifier. This is because the electrode of the modulator is designed as a perfect 50 Ω in order to reduce reflections. A possible solution is represented by the segmentation of the electrode into a finite number of pieces with different length. In such a way each segment of electrode can be considered as a capacitor that can be lumped into the artificial transmission line together with the output capacitance of the gain cell. As suggestion for future work, the design of such a modulator (which has not been not possible during this project) and of a proper drive to it seem to be feasible topics.

Appendix A

The Surface Passivated HRS DIMES03 Process

The in-house university DIMES03 process ($f_T \sim 15GHz$) and has been used here for the fabrication of the traveling wave amplifier. In the table A.1the main process parameters are reported.

Table A.1:

DIMES-03 TRANSISTOR PARAMETERS

$A_E(\mu m^2)$	20x1
β	100
BV_{CEO} (V)	8.0.
V_A (V)	38
C_{EB} (fF)	85
C_{BC} (fF)	60
C_{Sub} (fF)	200
f_T@$3V$(GHz)	13

The bipolar active NPN device in DIMES-03 is fully-implanted with less than 10% spread in the main device parameters over the wafer. The often observed higher spread in current gain associated with polysilicon emitter processes is thus avoided. The active circuits presented in this thesis are therefore fabricated in a technology that exhibits excellent parameter control. The fabrication process, which was designed for low-resistivity p-type LRS ($2-5\Omega cm$) substrates, has been transferred to p-type HRS substrates having a resistivity of 2000-4000 Ωcm. Since the very high silicon resistivity results in excessively wide space-charge regions (in the $20\mu m$ range) of the

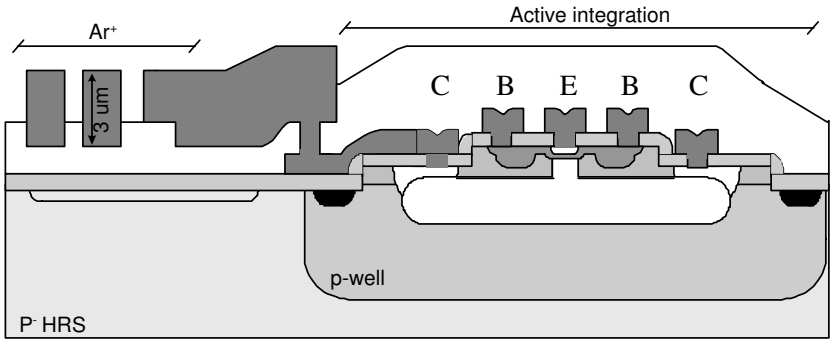


Figure A.1: Schematic cross section of the passive and active device structures in DIMES03 on SP-HRS.

collector-substrate junctions and low integral p-type doping between neighboring n-type regions placed in the substrate, a special p-well isolation structure has been developed for dense integration of the transistors. A $3\mu m$ deep boron doped p-well with a peak doping concentration of $2 \cdot 10^{15} cm^{-3}$ is created by implantation and thermal annealing prior to the implantation of the n^+ sub-collector regions and blanket deposition of the n-type layer, in which the active devices are built [86]. Outside the silicon device regions, this n^{--} silicon layer is removed by trench etching so that the passive components can be placed directly on the HRS substrate. where substrate losses are the lowest. The p-well provides a vertically increased p-type doping level under each transistor and narrow collector-substrate space-charge regions, while laterally a p^+ channel stopper is implanted after removal of the lightly-doped n-type layer. A schematic of the active and passive integration structure is shown in figure A.1. Since the well doping is comparable to that of the LRS substrate for which the DIMES03 process was originally designed, all transistor characteristics including the collector-substrate capacitance remained virtually unchanged (Table A.1). For the integration of passive components a two-level aluminum (Al) interconnect process with a $3\mu m$ thick top Al layer is used, as also shown in figure A.1. Without special surface passivation the substrate losses were still considerably above the theoretical minimum values due to the presence of conductive channels that build up at the wafer surface right beneath the silicon/silicon-dioxide interface. These channels result from positive (ion) charges in the isolating oxide, from (positive) states at the silicon/silicon-dioxide interface, or from a bias between a metal layer and the substrate [87]. According to the metal-oxide-semiconductor (MOS) theory either a majority carrier accumulation layer or an inversion layer in combination with a depletion region can be formed, depending on the specific conditions. With the low silicon doping level the flatband voltage is very

low so that the bias difference between the cases of accumulation and inversion/depletion is very small. That means that the chances for the presence of an accumulation or inversion surface channel are high and more losses than those associated with the bulk silicon are present. Given the local variations of both the oxide contamination level and the distribution of interface states, such additional losses also vary considerably across the wafer. It was therefore essential to apply a surface passivation technique in order to suppress these effects for minimum loss and best possible parameter control. Surface passivated high-resistivity silicon (SP-HRS) can be achieved by forming a thin silicon layer having a very high density of traps within the bandgap of silicon. This leads to a very high recombination rate and a reduced rate of impurity ionization. Consequently, accumulation, depletion, and inversion layer formation will be prevented and the additional source of loss will be eliminated. Such a high trap density can be achieved through a high-dose implantation of a neutral impurity, such as argon , into the silicon surface region or by depositing a thin, highly defective silicon layer, such as poly-crystalline silicon or amorphous silicon , onto the wafer. For the run used for this thesis it has been used an implantation of argon at a dose of $10^{15} cm^{-2}$ to form the SP-HRS.

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List of publications

1. F. M. De Paola, L. C. N de Vreede, L. K. Nanver, B. Rejaei, N. P. Pham, N. Rinaldi and J. N. Burghartz, "A Single Chip 1.8 GHz LNA and Power Amplifier with Improved Isolation Using Micromachining", 5th Annual Workshop on Semiconductor Advances for Future Electronics (SAFE), November 2001, Veldhoven (The Netherlands)

2. F. M. De Paola, L.C.N de Vreede, L. K. Nanver, B. Rajaei, N. Rinaldi and J.N. Burghartz, "A 1.8 GHz Integrated LNA Using Novel RF Si Technology" 6th Annual Workshop on Semiconductor Advances for Future Electronics (SAFE), November 2002 Veldhoven (The Netherlands)

3. F. M. De Paola, V. d'Alessandro, A. Irace, J.H. den Besten and M.K. Smit, "A Novel Simulation Strategy for Ultrafast InP/InGaAsP Optoelectronic Modulator Analysis", ROMOPTO 2003, 7-th International Conference on Optics 8-11 Settember 2003 Constanta (Romania).

4. F. M. De Paola, L.C.N de Vreede and N. Rinaldi "Optimised Design of a Si-based Wideband Amplifier by Including Layout High-Frequency Parasitic Effects", Workshop on Optimization and Coupled Problems in Electromagnetism , 22-23 Settember 2003 Naples (Italy)

5. F. M. De Paola, L. C. N. de Vreede, N. Rinaldi and J. N. Burghartz, "A Wideband Distributed Silicon Driver for 10 Gb/s External Modulators", 14th Workshop on Circuits, Systems and Signal Processing (ProRISC), 26-27 November 2003 Veldhoven (The Netherlands)

6. F. M. De Paola, V. d'Alessandro, A. Irace, J. H. den Besten and M. K. Smit, "Numerical Simulations for the Analysis of the Dynamical Behaviour of an Ultra-Fast InP/InGaAsP Optoelectronic Modulator", Photonics Europe 2004, 26-30 April 2004 Strasburg (France)

7. F.M. De Paola, V. Aliberti, B. Rajaei, N. Rinaldi and J. N. Burghartz, "A Scalable Physical Model for Coplanar Waveguide Transition in Flip-Chip Applications", 24th International Conference on Microelectronics,

16-19 May 2004, Nis (Serbia - Montenegro)

8. F. M. De Paola, V. d'Alessandro, F. Tamigi and N. Rinaldi, "Analytical Thermal Modeling of Flip-Chip Mounted Semiconductor Optical Amplifiers", European Microelectronics And Packaging Symposium (EMPS), 16 - 18 June 2004, Prague (Czech Republic)

9. F. M. De Paola, L. C. N. de Vreede, L. K. Nanver, N. Rinaldi and J. N. Burghartz, "Design and Characterization of a High-Resistivity Silicon Travelling Wave Amplifier for 10 Gb/s Optical Communication Systems", Digest of 2004 IEEE Topical Meeting on Si Monolithic ICs in RF Systems, 8 - 11 September 2004 Atlanta (USA)

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A. Manzoni, The Betrothed , ch. XXXVIII

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A. Manzoni, I Promessi Sposi, cap. XXXVIII

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About the Author

Francesco Maria De Paola was born in Salerno, Italy, on November 26 1976. He received the *Laurea* degree in Electronic Engineering from the University of Naples "Federico II" in 2001. In 2002 he joined the Department of Electronics and Telecommunications Engineering of the same university as a Ph. D. student, where he performed the research presented in this thesis. Currently he is working on pre-amplifiers integration for μdrive and mobile applications under an ST-Microelectronics grant. His research interests include analog design and microwave characterization.

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In this thesis, the research is described for realizing hybrid modules where silicon can be used to effectively improve different functionalities of the photonic device. Several aspect are detailed, spanning from the techology to implement the hybrid modules to the description of some particular photonic devices that might improve their performance when mounted onto a silicon carrier.

Also,some considerations about different amplifier architectures for optical communications are presented and completed with practical implementations in an advanced university bipolar process.