

Università degli Studi di Napoli *Federico II*

DOTTORATO DI RICERCA IN
FISICA

Ciclo XXXI

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Investigation of graphene as electrode in n-type OFETs and its use in nanometric devices

Settore Scientifico Disciplinare FIS/01

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Anni 2015/2018

"Ignoranti quem portum petat nullus suus ventus est."

-Seneca, Lettere a Lucilio-

CONTENTS

Introduction	1
1 Organic-Field-Effect-Transistors	4
1.1 Organic Semiconductors	5
1.1.1 n-type and p-type organic semiconductors.....	7
1.1.2 PDIF-CN2 and PDI8-CN2 as n-type organic semiconductors.....	9
1.2 Working principles	11
1.2.1 Current-Voltage characteristics	12
1.3 Contact resistances and electrode/organic interfaces in OFETs.	16
1.3.1 Contact Engineering in OFETs	19
1.3.2 Measuring techniques for contact resistances.....	21
1.4 Transistor operation in dynamic regime	23
1.5 Short channel effects in nanometric architectures	26
1.6 Graphene.....	29
1.6.1 Electronic Properties.....	30
1.6.2 Charge Transport	32
1.6.3 Quantum capacitance.....	34
1.6.4 Doping effects.....	36
1.6.5 Production methods of graphene	37
1.7 Graphene as novel electrode material for organic electronics.....	39
2 Device Fabrication	43
2.1 Electron Beam Lithography.....	43
2.1.1 The EBL experimental set-up	44
2.1.2 Enhanced sensitivity of PMMA 950K as positive e-resist using amyl acetate-based developers.	46
2.2 Reactive Ion Etching.....	48
2.3 HMDS deposition from vapor precursor	49

2.4	Bottom-contacts/Distributed-bottom-gate nano-OFET layout.....	50
2.4.1	Gold-based nano devices	54
2.5	Bottom-contacts/Local-gate nano-OFET layout	55
2.6	Micrometric bottom-contacts/distributed-bottom-gate interdigitated architectures.....	58
2.7	Organic thin film growth	59
2.7.1	Perylene diimides thin films by Organic Molecular Beam Deposition	62
3	Graphene Electrodes in nanometric Architectures	64
3.1	PDIF-CN2 based bottom-contacts/distributed-bottom-gate OFETs	65
3.1.1	Morphological characterization	65
3.1.2	DC electrical Characterization	66
3.1.3	Gold electrodes Vs Graphene electrodes in nanometricarchitectures	68
3.1.4	Doping conditions of CVD-Graphene Electrodes.....	72
3.2	PDI8-CN2 based nanometric OFETs with Local gate and ultra-thin Hafnium Dioxide as dielectric	75
3.2.1	CVD-Graphene on ultra-thin HfO ₂	75
3.2.2	Current-Voltage characteristics	79
3.2.3	AC characterization.....	82
3.2.4	Capacitance contribution of graphene electrodes	83
3.2.5	Calculated Cut-off frequencies for short channel OFETs	87
3.3	Final Discussion.....	88
4	The Graphene/Organic interface	91
4.1	Scanning Kelvin Probe Force Microscopy	92
4.2	Contact effects in gold-based micrometric devices.....	95
4.3	micrometric devices with CVD-Graphene Electrodes.....	101
4.3.1	Transport properties of CVD-graphene electrodes	102
4.3.2	Electrical characterization.....	103

4.3.3	Surface Voltages Profiles and Contact Resistances via SKPFM	106
4.4	Surface Spectroscopy via UPS/XPS.....	110
4.4.1	X-ray photoelectron spectroscopy	111
4.4.2	XPS analysis of PDI8-CN2 and PDIF-CN2 reference films	112
4.4.3	UV photoelectron spectroscopy.....	116
4.4.4	UPS analysis of the organic/graphene interfaces	117
4.5	Final Discussion.....	122
5	Conclusions	124
	Bibliography.....	126

Introduction

In the last years, scientific attention has been actively focused on the possible technological breakthrough of organic electronics and on the effective application of its paradigms, consisting in the production of flexible, low cost and easy-to-process devices for mass consumer electronics. Rapid advancements in the field prompted the development of a wide number of organic devices such as light-emitting diodes (OLEDs), solar cells, memories, light emitting field-effect transistors (OLETs) and organic-field-effect-transistors (OFETs). Specifically, OFETs have significantly improved in the past decade with nowadays benchmark devices competing with amorphous silicon thin-films-transistors (TFTs) in terms of electrical performances. However, further improvements are still necessary to maximize output currents and switching frequency, with a significant reduction of the required supply voltages at the same time. All these assessments are typically addressed in terms of the enhancement of charge mobility. A different approach for improving OFET performances is to intervene on the device architecture rather than on transport properties of the organic semiconductors, with the downscaling of channel lengths L , which are typically in the micrometer scale, into the sub-micrometer regime. On the other hand, the reduction of lateral dimension is typically accompanied by the rising of short-channel effects heavily interfering with a proper functioning of the organic devices.

Moreover, in the last years scientific community witnessed the relentless rise of the graphene: a carbon-based one-atom-thick material that combines high electronic and thermal conductivities, and extreme mechanical strength. Huge effort has been spent in the solid-state research to develop new technological applications of such a material. Among them, graphene has been recently considered as an interesting electrode material in organic field-effect devices, taking advantages from its work function tunability, permeability to the transversal electric field, and overall chemical stability.

The aim of this thesis concerns the investigation of graphene as electrodes in OFETs based on perylene tetracarboxylic diimides derivatives as n-type organic semiconductors. In particular, the role of graphene has been explored in relation with the downscaling of the lateral dimensions of the devices towards nanometric architectures. The electronic and morphological peculiarities of graphene electrodes have been demonstrated to play a key role in the mitigation of short-channel effects, typically encountered in gold-based devices. High quality transistor operation is observed for channel lengths down to $L \approx 150 - 200\text{nm}$ while long-channel (micrometric) devices shows substantially state-of-the-art performances if directly compared to gold-based layouts with similar architectures.

The thesis is divided in four chapters. In the 1st chapter, a brief introduction to the semi-conductive properties of π -conjugated molecules will be reported. A digression on the organic compounds will stress the differences between n-type and p-type conduction giving particular attention to the properties of two electron-transporting organic molecules: PDIF-CN2 and PDI8-CN2. The operating mode of the organic thin film

transistor will be discussed, borrowing the theoretical considerations from inorganic MOSFETs and outlining the main differences. The discussion will continue describing the contact effects occurring at the organic-semiconductors/electrode interfaces as well as the widely employed technique for the measurements of contact resistances. The downscaling of lateral dimensions of OFETs will be addressed by discussing the main theoretical considerations on short-channel effects and their influence in nanometric architectures reported in literature. The role of the channel length L will be highlighted in the description of the dynamic regime of operation in OFETs. The second part of the chapter is devoted to the introduction to graphene and its properties, with particular attention to the experimental techniques typically employed for the estimation of its transport properties, the quantum capacitance contribution in state-of-the-art graphene-based devices and the procedures commonly employed for its production. In the last section, the use of graphene as novel electrode material in organic devices will be addressed.

The 2nd chapter is devoted to the description of the experimental set-ups employed for the fabrication of both nanometric and micrometric architectures based on graphene electrodes by means of Electron-Beam-Lithography (EBL). A brief digression will be presented on the observed enhanced sensitivity of standard PMMA950K through amyl-acetate developers. The detailed fabrication recipes of three main architectures will be given. The discussion will move to the deposition methods for the organic semiconductors via the Organic Molecular Beam Deposition (OMBD) technique, describing the employed experimental set-up and focusing the attention on the deposition of perylene diimides thin films.

The 3rd chapter focuses on the experimental results obtained from the characterization of the nanometric channel n-type PDIF-CN2 OFETs based on graphene electrodes. In the first paragraph, by a thorough comparison with short channel transistors made with reference gold electrodes, an overall suppression of short-channel effects will be demonstrated for the graphene-based counterpart. The lack of current saturation in the output characteristics, due to the presence of a relatively thick distributed gate electrode of this architecture (SiO_2 300nm), is overcome in the second paragraph of the chapter, where the results will be reported for an alternative optimized layout with local gate electrodes and ultra-thin hafnium dioxide as high-k dielectric. The mitigation of short channel effects will be proved to still hold in the case of PDI8-CN2 thin films. Moreover, the AC characterization of devices will highlight the contribution of the quantum capacitance of graphene electrodes on the overall switching capabilities of the nano OFETs in dynamic regime.

The 4th chapter will give further insights on the organic/graphene interfaces, particularly in the case of long channel (micrometric) OFETs with graphene electrodes. Particular attention will be given to the contact resistances and their measurement by means of Scanning Kelvin Probe Force Microscopy (SKPFM). A brief description of the technique and of the experimental set-up will be given. The analysis will focus on the comparison between the contact effects in graphene-based layouts and their state-of-the-art counterpart with gold electrodes. The last section concerns on surface spectroscopy of

the organic/graphene interfaces, investigated by means of UV Photoelectron Spectroscopy (UPS) and X-ray Photoelectron Spectroscopy (XPS).

1 ORGANIC-FIELD-EFFECT-TRANSISTORS

The discovery of the first highly conducting polymer (chemically doped polyacetylene) in 1977 [1] resulted in a huge research effort on organic materials that led to the firstly reported p-type Organic-Field-Effect-Transistor (OFET) in 1986 [2].

Nowadays, the unique processing characteristics and demonstrated performance of OFETs suggest that they can be competitive candidates for existing or novel thin film transistor applications requiring large area coverage, structural flexibility, low temperature processing, and especially low production cost. Despite the potential technological applications, several bottlenecks still restrict their miniaturization towards the nanometric scale.

This first chapter will introduce to the scientific topic with a brief digression on the definition of organic semiconductor, with particular attention to the difference with the inorganic counterparts in terms of electronic structure of organic solids and transport mechanisms. Once introduced to the working principles of OFETs, contact effects affecting organic devices and their implication in terms of electrodes engineering will be discussed. The second part of the chapter is intended to briefly introduce to the utterly vast topic concerning graphene and its application. The digression will focus mostly on the experimental aspects that are preparatory for the discussion of experimental results reported in the following chapters.

1.1 ORGANIC SEMICONDUCTORS

Organic semiconductors (OSCs) are usually hydrocarbon molecules or polymers with a core of sp^2 hybridized carbon atoms. In sp^2 configuration, the $2s$, $2p_x$ and $2p_y$ atomic orbitals form three pairs of in-plane bonding (σ) and antibonding (σ^*) molecular orbitals. The remaining p_z atomic orbital forms a pair of π and π^* hybrid orbitals, perpendicular to the plane individuated by the σ bonds. The π - π^* couple is delocalized over the entire organic molecule that is thus referred to as π -conjugated. In the ground state, all the molecular orbitals are filled by an antiparallel-spin electron pair up to the highest occupied molecular orbital (HOMO). The antibonding orbitals, from the lowest unoccupied molecular orbital (LUMO) onwards, are empty (Figure 1.1 a). In organic semiconductors, the energy difference between HOMO and LUMO acquires the role of the bandgap of the inorganic counterpart. For increasing molecular mass, the confinement effects on electrons are weakened and the HOMO-LUMO gap is reduced.

In conventional inorganic semiconductors, strong covalent bonds between the atoms lead to significant overlaps of the electronic orbitals, resulting in broad energy bands. In organic solid, on the contrary, the magnitude of the interactions between molecules is limited to weak van der Waals forces. Wave functions of the HOMO and the LUMO are mainly localized in each molecule resulting in narrow gaussian-shaped energy bands, typically only few hundreds of meV wide [3] (Figure 1.1 b).

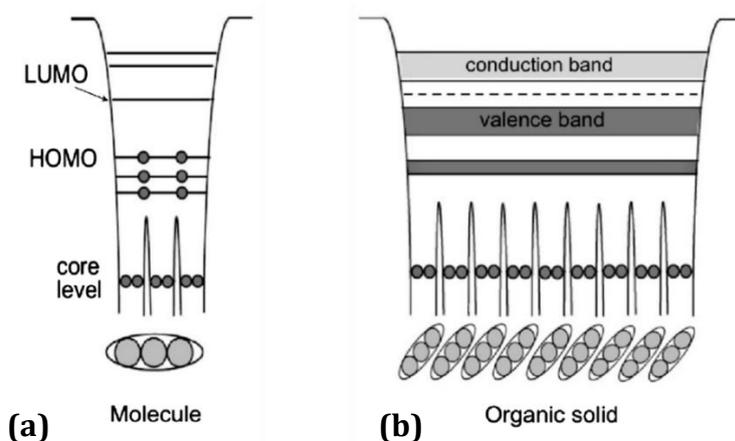


Figure 1.1 (a) Electronic structure of a single molecule and (b) band structure for an organic solid. Adapted from [4].

The more complicated geometry of organic molecules compared with the simple, spherical atoms and ions that constitute the inorganic semiconductors render most of the organic semiconductors rather disordered. All these factors limit the ability of intermolecular charge transfer in the organic solid and consequently influence the charge carrier mobility μ . Since the huge variety of organic compounds and in great number of extrinsic parameters influencing μ , there is no model that comprehensively describes the charge transport in all organic semiconductors.

In conventional inorganic semiconductor charge carriers move freely in a wide band as propagating Bloch waves. In organic semiconductors, this charge transport mechanism

has been observed only at low temperatures for which $\mu \propto T^{-n}$, with $n > 0$. A band model description has been proved to be suitable in describing charge transport at very low temperatures for naphthalene single crystals [5,6]. In general, organic semiconductors are in the form of polycrystalline films or even amorphous solids. Charge transport in organic semiconductor devices is therefore usually determined by localized states in the forbidden energy gap. These states can be created by energetic and positional disorder, which includes impurities, defects, grain boundaries and interface states. For example, for organic solids in which disorder is not dominating, it is possible to apply the so-called Multiple-Trap-and-Release model (MTR) [7]. MTR has been used to account for gate voltage dependent mobility in hydrogenated amorphous silicon [8] and then extended successfully to polycrystalline oligothiophene thin-films [9]. The model assumes the presence of localized states in the HOMO-LUMO bandgap. The shallow trap can exchange carriers with the extended band states through the competing processes of trapping and thermal excitation (Figure 1.2a), thus reducing the effective carrier mobility with an Arrhenius-like behavior of the form:

$$\mu_{\text{MTR}} = \mu_0 \Theta_t \exp\left(-\frac{E_C - E_t}{k_B T}\right) \quad (1.1)$$

where μ_0 indicates the intrinsic trapping-free mobility of the organic semiconductor, Θ_t is the ratio between the density of transport free states and the trapping states while E_C and E_t individuate the conduction and the trapping level, respectively.

Variable-Hopping-Range (VHR) models, on the other hand, can be applied when disorder can be considered as dominating [10]. Localized charge carriers may travel through the material by hopping from one localized state to the next by phonon-assisted tunneling (Figure 1.2b). The transition probability (W_{ij}) between an occupied state with energy E_i and a free state E_j , separated by a hopping distance R_{ij} , can be described by the Miller-Abrahams expression [11,12]:

$$W_{ij} = v_0 \exp(-\gamma |R_{ij}|) \begin{cases} \exp\left(-\frac{E_j - E_i}{k_B T}\right) & \forall E_j > E_i \\ 1 & \text{else} \end{cases} \quad (1.2)$$

where v_0 is a characteristic vibration frequency of the material while γ is defined as an the inverse of the localization radius.

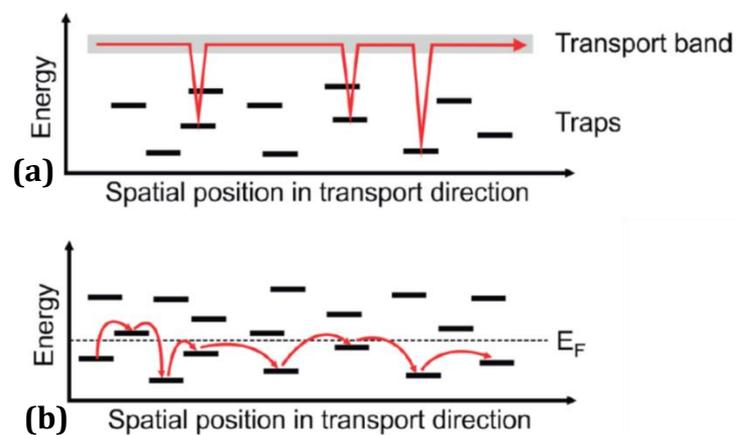


Figure 1.2 Schematic illustrations of disorder-based transport models in organic semiconductors. (a) In Multiple-Trap-and-Release model (MTR), charge carriers trapped in localized states in the forbidden band are thermally released towards the conduction band. (b) In Variable-Range-Hopping (VRH) models, phonon assisted tunneling between localized states dominates the transport in the organic semiconductors.

Furthermore, in organic semiconductors electron-phonon coupling no longer plays the role of a perturbation, as in the case of covalently bound inorganic semiconductors, but rather leads to the formation of polarons for which mobility results strongly temperature dependent [13]. At this regard, the dynamic interaction between the traveling charges and the molecular vibrations has been recently measured in rubrene single crystals via angle resolved UV photoelectron spectroscopy [14].

1.1.1 n-type and p-type organic semiconductors

For organic semiconductors, the common p-type or n-type classification does not apply since organic compounds can be considered as intrinsic. It rather expresses the ease with which one of the charge carriers can be injected through the metal electrodes. One of the most important aspects of charge injection is, indeed, the energy levels alignment at the interfaces.

Lowering energetic barriers facilitates efficient injection resulting in enhanced electrical performances. The energy levels matching at electrode/organic interface can be achieved through the proper selection of the metal in comparison with HOMO or LUMO levels of the organic semiconductors. In particular, referring to the Fermi energy (E_f) of the metal electrode, low E_f -LUMO barrier yields to an assisted electron injection; on the contrary, low E_f -HOMO barrier is characterized by hole injection (Figure 1.3).

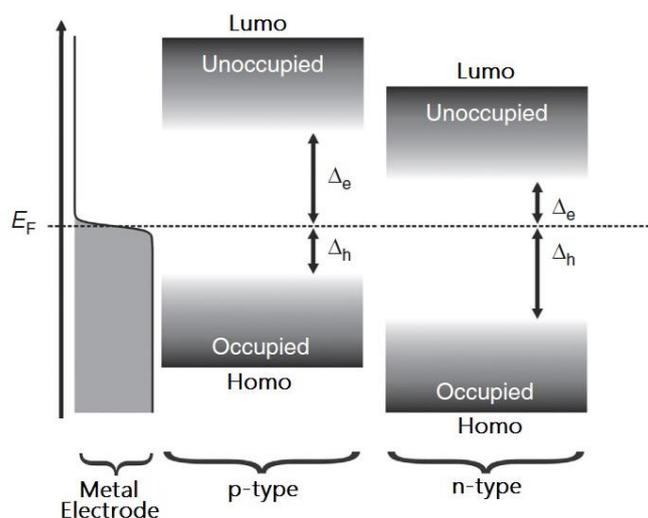


Figure 1.3 Schematic showing the Fermi-Dirac occupation function with Fermi level E_F for the metallic side of the interface. The difference in energy between E_F and the onsets of occupied and unoccupied density of states (DOS) on the organic semiconductor side are the charge injection barriers Δ_h for holes and Δ_e for electrons, respectively.

However, a simplistic energy-band diagram only provides a guide for selecting contact materials and the use of an electrode with a properly selected work function does not guarantee efficient hole or electron transport and improved device performances. As it will be further discussed in the next sections, charge injection and extraction at the OSC/electrode interface are not trivial phenomena and numerous parameters must be taken into account when estimating the energy barriers.

In the past few years, remarkable improvements have been made in enhancing the charge carrier mobility of p-type OSCs thanks to the development of new materials, and device architecture optimization. Charge carrier mobility values exceeding $40 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ have been achieved for both p-type small molecules [15–17] and highly oriented nanocrystalline hole-transporting polymers [18], in OFETs configurations. On the other hand, the overall development of n-type organic semiconductors still lags behind their p-type counterparts in terms of ambient stability and mobility which is still confined in the order of few $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ [19]. To move ahead with organic electronics, nevertheless, research activity on n-type OSCs is of vital importance for the development of complementary logic for digital applications. One of the main challenges for n-type organic semiconductors is the injection of electrons from a suitable electrode to the LUMO level of the organic compound. In the p-type counterparts, HOMO levels in the range between 4.8eV and 4.3 eV are typically observed. These values are easily aligned with the work function of the most widely used metallic electrodes, as for example gold which has a work function ranging between 4.8eV and 5.1eV. For n-type OSCs, LUMO levels are in the range of 3-4eV. Observation of n-type behavior is thus severely limited due to the extremely high injection barrier in the case of Au/OSC interfaces. Increasing electron affinity (i.e. lowering the LUMO level) of the organic compound is thus a valuable route for enhancing electron-transporting properties. This is usually achieved by taking a known semiconducting core molecule and adding strong electron withdrawing groups

such as fluorine, cyano, or imide moieties [20]. Another strategy for the reduction of the metal/OSC energy barrier would imply the use of high work function metals such as Aluminum, Calcium, Chromium. In this case, major drawbacks are clearly due to the high oxidizing nature of those materials, degrading the reliability of the contacts and the overall performances of the organic device.

Even if the chemical tailoring of the molecule and the choice of the electrode material ensure the electron transporting properties, the susceptibility of n-type organic semiconductors to atmospheric oxidants is usually an open issue. Organic radical anions, in particular carbanions, react with O₂ and H₂O molecules under operating conditions, thus providing devices with dominant electron trapping effects [21]. Usually, a LUMO energy of -4.0 eV or lower is assumed to be connected to a certain level of ambient stability.

1.1.2 PDIF-CN₂ and PDI8-CN₂ as n-type organic semiconductors

Among all the n-type OSCs under investigation, in the last years perylene tetracarboxylic diimides (PDI) have been reported showing high electron affinities, good electron-transporting properties and excellent ambient stability [22–24]. The organic molecules employed throughout this work are two moieties belonging to this class of semiconductors: PDI8-CN₂ and PDIF-CN₂, commercialized by FlexTerra as ActivInk™ N1200 and N1100 [25].

As shown in Figure 1.4, both molecules are based on a perylene core decorated by electron-withdrawing cyano (-CN) and imide (-N) groups insertion on the aromatic scaffold.

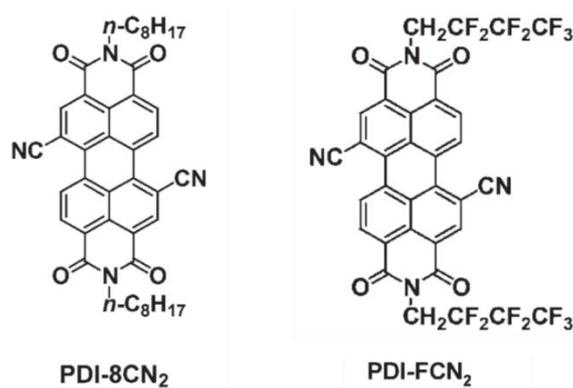


Figure 1.4 Molecular structures of PDI-8CN₂ and PDI-FCN₂.

Such substitutions act as “ π -acceptors” increasing the conjugation length and lowering the LUMO level minimizing in such a way the energetic offset with the electrodes for enhanced electron injection [26].

The PDI8-CN₂ and PDIF-CN₂ differ solely by their imides substituents: PDI8-CN₂ is characterized by an alkyl chain, while PDI-FCN₂ features a fluorocarbon chain. Both impact on the energy of the σ orbitals of the aromatic core, lowering the electron density

at the nuclei of the carbon atoms in the π -conjugated system. Consequently, LUMO levels result further lowered with final values of -4.3eV for PDI8-CN2 and -4.5eV for PDIF-CN2. Parameters characterizing the two materials under investigation are summarized in Table 1.

In PDIF-CN2 the fluorinated functionalities provide a more robust morphological screening of the aromatic core that can be explained in terms of a larger van der Waals radius of fluorine atoms if compared to hydrogen in the alkyl chains of PDI8-CN2. This leads to a reduced available spacing between the chains of co-facial stacked molecules from 4 \AA to 2 \AA , preventing to a greater extent O_2 intrusion [27]. The specific chemical tailoring of these two organic compounds has a valuable impact on their electrochemical reduction potentials (E_{red}) as well. Values of -0.13V and -0.06V (Table 1) ensure an enhanced thermodynamic stability towards oxidation by water contamination for which $E_{red} > -0.67\text{V}$ are usually indicated as hindering considerably electron trapping phenomena [21].

The crystal structure for both the organic compounds, inferred from x-ray diffraction measurements on single crystals [28–30], show similar results. A slip-stacked face-to-face molecular packing (Figure 1.5a) with a minimum interplanar spacing of 3.4 \AA between the adjacent aromatic planes of the flat perylene cores (Figure 1.5b) is reported.

	E_{HOMO} [eV]	E_{LUMO} [eV]	E_{gap} [eV]	E_{red} [V]
PDI8-CN2	-6.7	-4.3	2.4	-0.06
PDIF-CN2	-6.8	-4.5	2.3	+0.03

Table 1 Energy levels, bandgap and reduction potentials (determined vs Saturated Calomel Electrode) for PDI8-CN2 and PDIF-CN2. Adapted from [25].

The tight interplanar packing demonstrates the good overlap of π -orbitals between neighboring molecules that promotes an efficient intermolecular charge transfer.

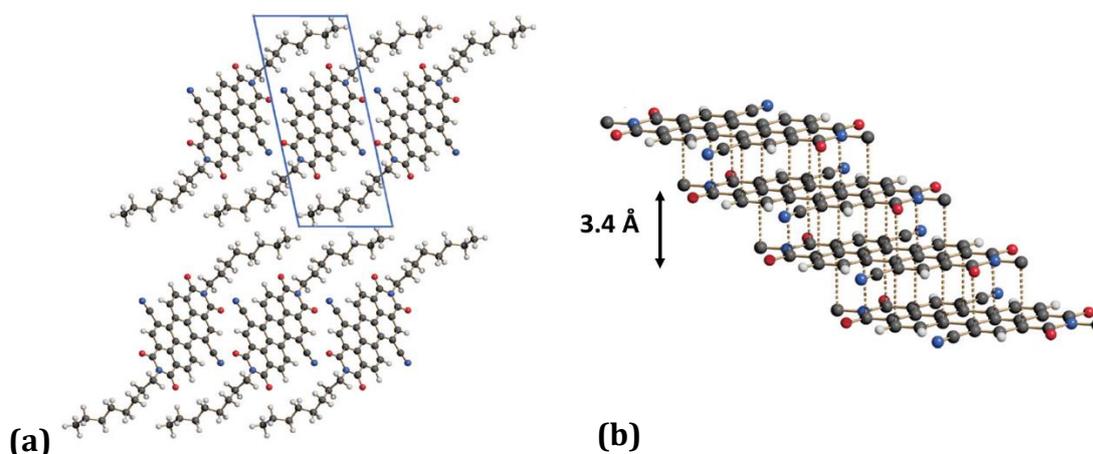


Figure 1.5 (a) Schematic drawing of the crystal structure of PDI-8CN2, viewed from the [100] axis. (b) π - π stacking of the flat perylene cores in the slip-stacked face-to-face molecular packing (side chains are omitted for clarity). A similar crystal structure is observed for the PDIF-CN2. Adapted from [30].

PDI8-CN2 has been proved to be a suitable material for complementary circuits [31] and has shown to yield high-performance devices by sublimation [32,33] or from solution methods [34] with typically observed field-effect mobility of $\sim 10^{-2} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$.

Similarly, PDIF-CN2 has been used for the fabrication of n-type transistors based on highly ordered vapor-deposited thin films [35], solution-processed devices [36], with state-of-the-art mobility values around $10^{-1} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. High performing transistors based on single crystals with mobility values largely exceeding $1 \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ have been reported as well [37].

1.2 WORKING PRINCIPLES

An OFET is analogous to its inorganic counterpart in design and function. It can be schematically represented as a three-terminal device composed by a gate electrode, separated from the OSC by a dielectric interface forming a Metal-Insulator-Semiconductor (MIS) structure, and a source-drain electrodes pair from which charge carriers are injected and extracted, respectively. Organic Thin Film Transistors (OTFT) are a subclass of organic transistors for which the conduction channel is made by a thin strip of semi conductive material (with a thickness $< 1 \mu\text{m}$) deposited over the insulating interface. A schematic depiction of a typical OTFT with channel length L and width W is reported in Figure 1.6. The basic operating principles discussed below are referred to a n-channel device. In the case of p-type operation all the biases must be reversed.

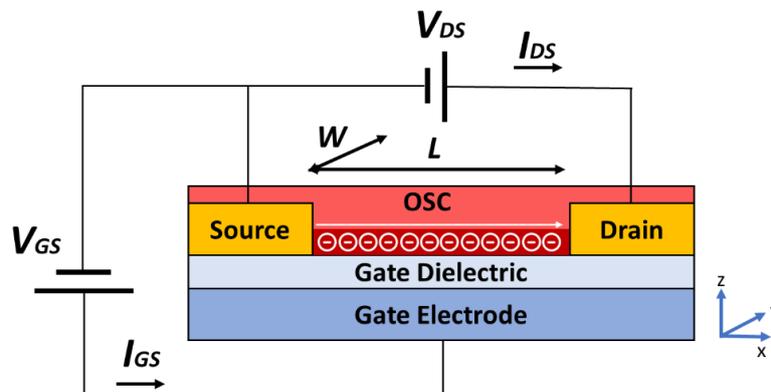


Figure 1.6 Schematic depiction of an Organic-Thin-Film-Transistor (OTFT) with channel length L and width W . The device consists of three contacts (source, drain and gate). The organic semiconductor is usually deposited on a dielectric interface, insulating the active channel from the gate electrode. In the case of a n-type channel, the application of a positive gate voltage (V_{gs}) induces charge accumulation on the insulating interface. A perpendicular V_{ds} bias causes the charge carriers drift between source and drain (I_{ds}). An unwanted gate-source current (I_{gs}) may leak from the transistor active channel towards the gate electrode.

In n-type OTFTs, the application of a positive voltage between the gate and the source electrodes (V_{gs}) induces the accumulation of a large number of charges at the MIS interface, if a threshold value (V_{th}) is exceeded. Conversely, they are depleted from the channel if a negative V_{gs} is applied. This is in contrast with conventional inorganic

MOSFET in which the conductive layer is formed by population inversion within the active channel rather than by accumulation. A positive voltage applied between the source and the drain electrodes (V_{ds}), then, drives the channel current (I_{ds}) across the charge-accumulated layer. Unwanted leakage current (I_{gs}) may flow from the organic channel to the gate electrodes breaking through the dielectric interface. The variation of the gate potential modulates the amount of accumulated interfacial charge influencing the conductivity of the organic thin film between the source and the drain electrodes. In these terms, OFET operates as a gated current switch.

1.2.1 Current-Voltage characteristics

The current-voltage characteristics of OTFTs can be described analytically assuming the gradual channel approximation. That is, the field perpendicular to the current flow generated by the gate voltage is much larger than the electric field parallel to the current flow created by the drain-source voltage [38]. On the MIS structure, for a given gate potential, the accumulated charge density n can be expressed in terms of V_{gs} and of the potential $V(x)$ along the longitudinal path connecting the biased source-drain pair. Namely [39]:

$$n(x) = C_{ox} (V_{gs} - V_{th} - V(x)) \quad (1.3)$$

Where C_{ox} is the capacitance per unit of area of the dielectric while V_{th} is a threshold gate voltage that can originate from several effects and depend strongly on the semiconductor and dielectric used. Built-in dipoles, impurities, interface states, and, in particular, charge traps contribute to the deviation of V_{th} from zero [40]. In a simplified Drude model for charge conduction, it is possible to express the drain-source current induced by mobile carriers according to the following formula:

$$I_{DS} = W \mu_{FET} n(x) E_x \quad (1.4)$$

Where W is the channel width, μ_{FET} is the field-effect mobility and $E_x = dV/dx$ is the longitudinal electric field at position x along the channel. Making use of (1.3) and (1.4), and integrating from the source electrode ($x = 0, V = 0$) to the drain electrode ($x = L, V = V_{ds}$) the following relation is obtained:

$$I_{ds} \int_0^L dx = I_{ds} L = W \int_0^{V_{ds}} \mu_{FET} \left[C_{ox} (V_{gs} - V_{th} - V(x)) \right] dV \quad (1.5)$$

In first approximation, it is possible to consider the field-effect mobility as an intrinsic parameter, i.e. independent of charge carrier density distribution, applied gate voltage and transversal electric field. Given those assumptions, the final expression for the drain-source current is given by the following relation:

$$I_{ds} = \frac{W}{L} \mu_{FET} \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (1.6)$$

From (1.6), two distinct regimes can be specified, according to the relative magnitude of V_{ds} compared to the effective applied gate potential ($V_{gs} - V_{th}$).

For $(V_{gs} - V_{th}) \ll V_{ds}$, the accumulated charge density is uniform, and the active channel can be modeled as a resistor. This is the linear regime, in which the current flowing through the channel is directly proportional to V_{ds} . Thus, (1.6) can be rewritten as:

$$I_{ds}^{lin} = \frac{W}{L} \mu_{FET} [(V_{gs} - V_{th}) V_{ds}] \quad (1.7)$$

A typical transfer characteristic (I_{ds} - V_{gs}) in linear regime is reported in Figure 1.7a. If the drain-source bias is increased until $V_{ds} = (V_{gs} - V_{th})$, the difference between the local potential $V(x)$ in correspondence of the drain electrode and the gate voltage is below the threshold voltage; charge carrier are thus depleted and the channel is “pinched-off”. Further increase of the drain-source bias ($V_{ds} \gg (V_{gs} - V_{th})$) leads to an expansion of the depleted region towards the source electrode. In this case, the device is referred as in saturation regime. I_{ds} becomes independent from V_{ds} and quadratic in $(V_{gs} - V_{th})$ as reported in Figure 1.7b and Figure 1.7c, namely:

$$I_{ds}^{sat} = \frac{W}{2L} \mu_{FET} (V_{gs} - V_{th})^2 \quad (1.8)$$

Field-effect mobilities for linear and saturation regimes can be operationally defined from I - V curves. The first can be obtained considering the transconductance defined as $g_m = \partial I_{ds} / \partial V_{gs}$ for a fixed V_{ds} . Referring to (1.7), μ_{FET}^{lin} can be written as:

$$\mu_{FET}^{lin} = \frac{L}{WC_{ox}} \frac{1}{V_{ds}} \frac{\partial I_{ds}}{\partial V_{gs}} \quad (1.9)$$

Similarly, the differential mobility in saturation regime can be extracted from the $\sqrt{I_{ds}}$ curve of (1.8):

$$\mu_{FET}^{sat} = \frac{2L}{WC_{ox}} \left(\frac{\partial \sqrt{I_{ds}}}{\partial V_{gs}} \right)^2 \quad (1.10)$$

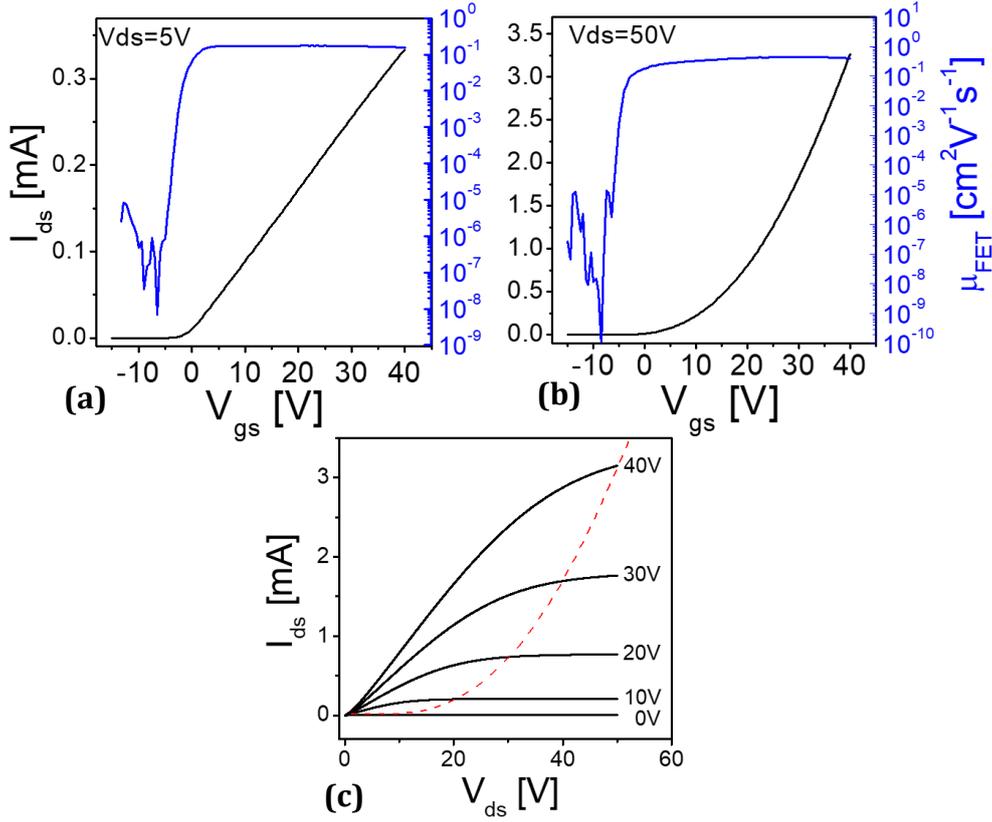


Figure 1.7 Typical current-voltage characteristics for a PDIF-CN2 based OTFT. For the device under consideration, $L=20\ \mu\text{m}$ and $W=1.1\text{cm}$. The gate insulator is formed by a 200nm thick SiO_2 interface. (a) and (b) are the transfer characteristics (I_{ds} - V_{gs}) in linear and saturation regime, respectively. The blue curves represent the point-wise field effect mobilities calculated using (1.9) and (1.10). (c) Typical output curves (I_{ds} - V_{ds}) for different gate voltages in the range between 0V and 40V. It is possible to observe the saturation of the channel current for drain-source biases greater than the effective gate voltage ($V_{gs}-V_{th}$), delimited by the saturation curve (red dashed line).

1.2.1.1 Parameters influencing the field effect mobility

Charge carrier mobility in FET configuration, defined by (1.9) and (1.10), are extrinsic quantities whose reliability in defining the performance of the OFET is strictly related to the linearity of the I_{ds} and $\sqrt{I_{ds}}$ curves [41]. In real-world devices, the field-effect mobility is often observed as a point-wise quantity strongly influenced by the applied gate-voltage according to a semi-empirical form of the type [9]:

$$\mu_{FET}(V_{gs}) = \alpha(V_{gs} - V_{th})^\beta \quad (1.11)$$

In a MTR theoretical framework, the gate voltage dependence of the mobility relies on the amount of released charge, with respect to the trapped fraction that does not contribute to the charge transport, which in turn depends on the Fermi level at the insulator semiconductor interface.

Measured field-effect mobility values in OFETs are strictly related to the morphology of the organic thin film in the active channel, as well. Vapor-deposited films of small

molecules are usually composed by interconnected crystalline domains in which the semiconducting molecules are uniformly arranged with optimized π - π stacking. The efficiency of charge transport across the organic channel is thus mainly limited by the charge transfer phenomena in correspondence of the grain boundaries. The effect on the mobility of the OTFT can be modeled straightforwardly dividing the polycrystalline material into high (the crystalline grains) and low (the boundaries) conductivity regions. Considering grains with length L_G and mobility μ_G in series with grain boundaries with length L_{GB} and mobility μ_{GB} , the effective mobility μ_{eff} is thus given by [42]:

$$\frac{L_G + L_{GB}}{\mu_{eff}} = \frac{L_G}{\mu_G} + \frac{L_{GB}}{\mu_{GB}} \quad (1.12)$$

Tunneling, thermionic emission or MTR models [43] specifically address the transport across adjacent crystalline domains in which grain boundaries act as trapping centers. At high temperatures, carriers tend to be driven over the grain barriers by thermal activation. Therefore, an Arrhenius-like behavior of the form $\mu_{GB} \propto \exp(-E_A/k_bT)$ is usually considered, with activation energy given by E_A .

Lastly, the dielectric interface of the organic transistors plays a major role in several aspects. The presence of an atomically flat surface enhances in first approximation the morphological order of the organic semiconductor, maximizing the grain size and limiting trapping phenomena at the boundaries. Typically, SiO_2 (thermally grown on Si or sputtered), Al_2O_3 , and Si_3N_4 , or polymeric insulators, such as, for example, poly(methyl methacrylate) (PMMA) or poly(4-vinylphenol) (PVP) [44] are commonly employed depending on the OFET architecture. In the case of the most widely used SiO_2 , moreover, trapping of electrons at the semiconductor–dielectric interface by hydroxyl groups, present in the form of silanols, strongly limits the electron transport over the OFET channel [45]. Self-Assembling-Monolayer are often employed to chemically passivate the dielectric interface, in order to minimize charge trapping and to optimize the overall performances of the device (Figure 1.8).

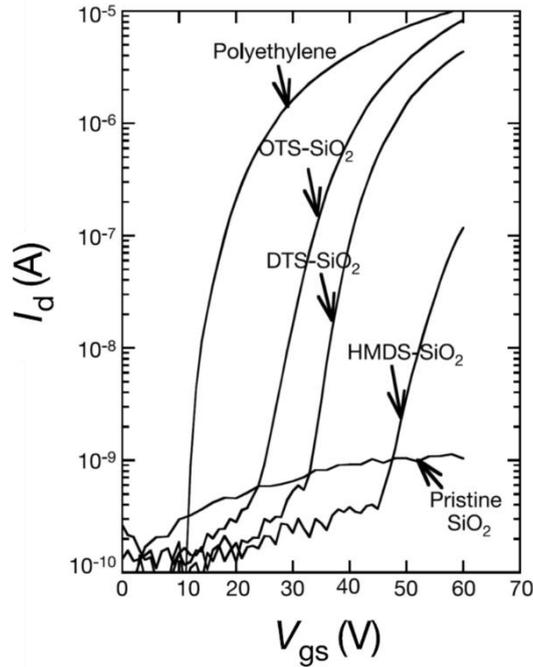


Figure 1.8 Transfer characteristics for n-channel OFETs with various siloxane self-assembled monolayer (SAM) on SiO₂ as dielectric or with polyethylene as buffer dielectric. From [45].

1.3 CONTACT RESISTANCES AND ELECTRODE/ORGANIC INTERFACES IN OFETs.

In traversing an OFET channel from source to drain, charge carriers are injected from the source contact into the semiconductor channel, transported across the length of the channel and extracted into the drain electrode. These processes can be roughly thought of as three resistors in series, as schematically depicted in Figure 1.9.

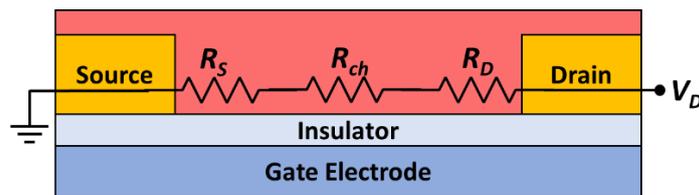


Figure 1.9 Schematic depiction of the contacts contribution to the total resistance of an OFET.

The total device resistance $R_{tot} = V_{ds}/I_{ds}$ can be thus written as the sum of two contributions: one from the conduction channel (R_{ch}) and one from the contacts (R_C) [46]:

$$R_{TOT} = R_{ch} + R_C = R_{sheet} \frac{L}{W} + R_S + R_D \quad (1.13)$$

Where R_{sheet} indicates the 2D resistance of the active channel while R_S and R_D are the contribution due to the source and drain electrodes, respectively. In order to compare the contact resistance of transistors with different device geometries they are typically reported in their width-normalized form ($R_C W$ expressed in Ωcm). In an ideal OFET, contact effects can be neglected in comparison to the channel contribution. However, in real devices they can considerably consume voltage drop across the active channel, generate Joule heating, and decrease charge injection and extraction efficiency, limiting a proper working condition of the device and invalidating the description of current-voltage characteristics given by (1.7) and (1.8). Field effect mobility individuated by equations (1.9) and (1.10) become effective parameters that contain intrinsically the parasitic effects and that may deviate considerably from an actual quantification of charge carrier mobility of the organic semiconductor [47]. Moreover, referring to (1.13), R_S and R_D are length-independent parameters and can be a severely limiting factor in short channel devices [48], as it will be further discussed in the next section. The role of the organic/electrode interface is crucial in understanding the origin of R_C . Contrary to the case of inorganic FET, the contacts in organic field-effect transistors rely on a direct metal-semiconductor junction without any doping. In the former case, the metal-semiconductor interface is usually treated as a Mott-Schottky barrier, where the injection barrier height (ϕ_b) is given by the difference between the metal work function (ϕ_m) and the semiconductor electron affinity (EA), in the case of a n-type semiconductor (Figure 1.10a). Namely:

$$\phi_b = E_F - E_{LUMO} = \phi_m - EA \quad (1.14)$$

However, many metal-organic semiconductor interfaces do not follow the Mott-Schottky rule and the electronic structure may significantly deviate from the description given by (1.14). Interfacial charge transfer between the electrodes and the organic molecules, the formation of metal-induced mid gap states and the push-back effect on the electron density of the electrode modify the energetics of the barrier, affecting both the actual work function of the electrode and the band width of the LUMO or HOMO of the OSC [49,50]. These effects are usually summarized in an additional interfacial dipole Δ in the estimation of ϕ_b (Figure 1.10b):

$$\phi'_b = \phi_m - EA \pm \Delta \quad (1.15)$$

The contribution of delta can lower or increase the effective interface barrier according to its sign.

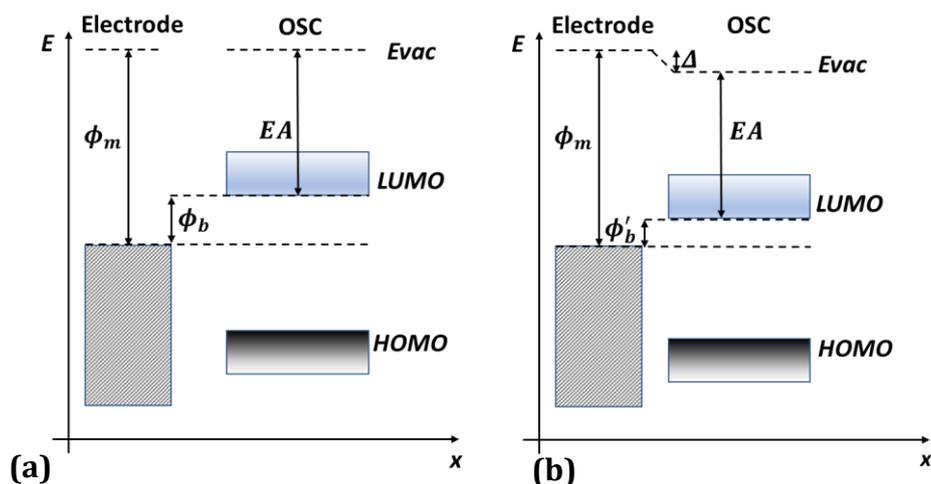


Figure 1.10 (a) Schematic band line-up at a metal/organic interface following the classical Mott-Schottky rule. In this case the vacuum levels of the electrode and of the organic semiconductor are aligned. (b) Band alignment in the presence of an additional term Δ causing a shift of the vacuum level of the organic semiconductor and a consequent lowering of the interfacial barrier ϕ'_b .

In the classical case of an inorganic semiconductor/metal contact, Mott-Schottky thermionic emission and Fowler–Nordheim tunneling are usually invoked in the modeling of charge injection phenomena when the interface is biased [38]. For both mechanisms, the crucial condition is that there is strong electronic coupling among the constituting lattice elements that leads to wide valence and conduction bands. In organic solids this condition is violated because electronic coupling between molecules is of weak van der Waals type. Several models have been developed in the last years addressing the physics of the charge injection in organic semiconductors [51–53]. However, since the complexity of the topic and the hugely assorted variety of molecular compounds, scientific community has not yet accredited one of the proposed models as main theoretical framework. Experimentally, charge injection in organic semiconductors is observed as a thermally activated process in accordance with a thermionic process, although with activation energies that are lower than those predicted by (1.14) [54]. Moreover, the order of magnitude of contact effects at the injective (Source) and extractive (Drain) electrode are usually comparable [55], in contrast with a classical picture according to which the reverse-biased barrier at the source should give the major contribution to the overall R_C . Lastly, contact resistances are observed to decrease for increasing gate bias [56–58], indicating that transport properties and both energetical and positional disorder near the contacts are of crucial importance in the injection and extraction phenomena. Given the aforementioned experimental evidences, it is possible to assume that charge injection occurs as a thermally activated phenomenon that raises an electron from the Fermi level of the electrode to a tail state of the gaussian density of states distribution of the organic semiconductor. At this stage, the promoted carrier can continue its motion away from the interface or recombine with its image charge in the electrode (drift-back). Injection and drift-back can be assumed to cancel out once the thermal equilibrium is reached. Conversely, injection is favored upon the application of an external electric field

E that reduces the effective injection barrier ϕ_b by Frenkel-Poole effect [38]. The injected carrier is thus considered to execute a diffusive random walk in the combined coulomb potential of the image charge and the externally applied potential, towards the conduction band (Figure 1.11a). The resulting injected current density can be described, in first approximation, following the model proposed by Scott and Malliaras [59]:

$$J_{INJ} = e\mu_0EN_0\exp\left(-\frac{\phi_b}{k_bT} + \frac{\gamma\sqrt{E}}{k_bT}\right)\psi^2(E) \quad (1.16),$$

where N_0 is the total density of states, γ is a material-dependent coefficient related to the barrier lowering and ψ individuates a slowly varying function of electric field accounting for the drift-back of charge carriers. It is worth noting that in (1.16), the energetical disorder is neglected and the barrier is determined solely by the theoretical Schottky barrier given by (1.14). Referring to Figure 1.11b, a more realistic picture in which a statistical distribution of occupied states (ODOS) centered at $-\sigma^2/k_bT$ with respect the nominal LUMO (HOMO) gaussian DOS must be taken in account [49]. The temperature dependence of the barrier lowering is given by $\Delta\phi_b = -\sigma^2/2k_bT$ according to which lower temperatures or higher energetic disorder may correspond to a decreased injection barrier. However, the reduction effect is counterbalanced by the reduction of the overall charge carrier mobility that is strictly dependent on both parameters.

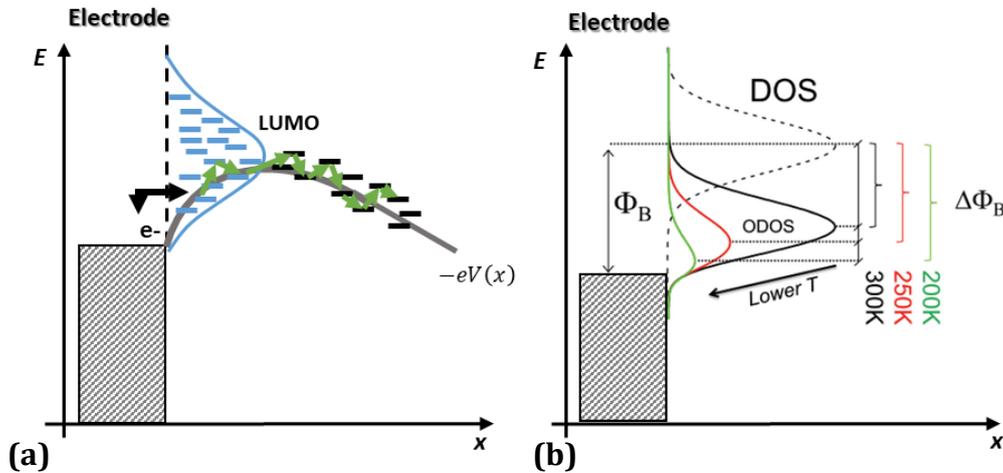


Figure 1.11 (a) Schematic depiction of the thermal hopping-assisted charge injection at the electrode/OSC interface. Thermally excited electron is injected in a tail state of the gaussian density of state of the organic semiconductor, in the vicinity of the electrode. It is promoted in the transport band after a diffusive random walk in the localized state following the potential profile due to the applied bias. (b) Effect of disorder and temperature on energetic barrier at the metal/organic interface. At room temperature the density of occupied states (ODOS, black curve) closely resembles a Gaussian, and its center lies close to the metal Fermi level: the effective energetic barrier is lower than the nominal DOS (black dashed line) by $\Delta\phi_b = -\sigma^2/2k_bT$. Upon lowering the temperature, the barrier reduction is even larger. Adapted from [49]

1.3.1 Contact Engineering in OFETs

According to the sequence on which all the transistor components are deposited, four different TFT architectures can be distinguished, as reported in Figure 1.12. They can be

divided in two main classes: coplanar and staggered. In the former, the accumulation layer and the source/drain pair lie in the same plane. Conversely, in staggered architectures, the OSC is in between the dielectric layer and the plane containing the source and drain electrodes. Each class is characterized by top-contacts (Figure 1.12b,d) or bottom-contacts (Figure 1.12a,c) layouts, depending on the relative position of the source/drain electrodes with respect to substrate. Contact resistances and the overall performances of the device are indeed influenced by the architecture. Staggered top-contacts, generally, exhibit lower contact resistance values if compared to coplanar layouts [60]. This can be explained in terms of geometrical consideration on the injection and extraction surface. In coplanar architectures the injection surface is usually defined by the height of the electrodes (usually tens of nanometers) and to the organic thin film morphology at the contacts [61]. In staggered configurations, all the contact area facing the gate dielectric is prone to charge injection and extraction. Nevertheless, charge carriers must cover a longer distance separating the injection interface and the accumulation layer, resulting in additional interface barrier referred as “access-resistance” that strictly depends on the organic thin film thickness.

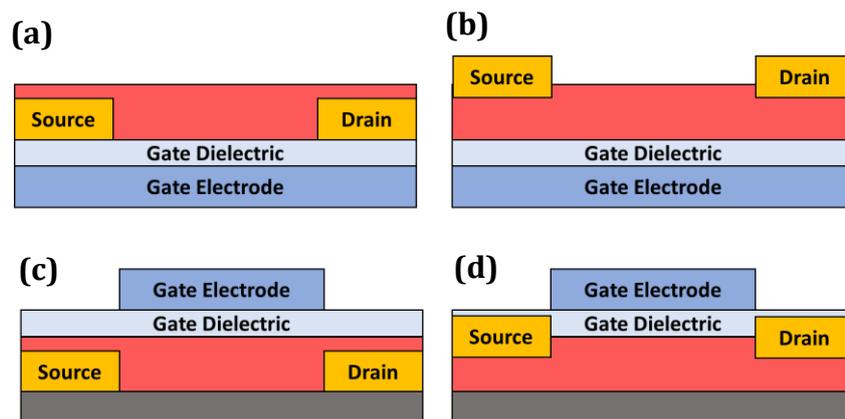


Figure 1.12 Typical OTFTs architectures. (a) Bottom-contacts/Bottom gate. (b) Top-contacts/bottom-gate. (c) Bottom-contacts/Top-Gate and (d) Top-contacts/Top-gate.

However, major drawbacks in staggered architectures rely in the fabrication processes. Top metal contacts are typically patterned by means of shadow-masks, evaporated directly on to the deposited organic thin film with minimum achievable channel lengths that are typically limited in the micrometric scale with few exceptions [62,63]. Conversely, in coplanar layouts the device architecture is defined before the organic thin film deposition. In this case, the dimensionality of the device is thus only limited by the resolution of the employed patterning technique.

The control over the contact resistances is not dictated solely by a thoughtful choice of the device architecture. More general approaches aiming to the contacts engineering by the direct tuning of the interfacial barriers ϕ_b have been widely investigated in recent years [64]. Especially in coplanar architectures, fine modulation of both hole and electron injection barriers can be achieved by molecular dipole-induced modifications of the

electrode work function via thiol-based SAMs [65], or by interfacial doping through the insertion of Charge Injection Layers (CILs) consisting of both inorganic [66,67] and organic [68,69] buffer interlayers. Moreover, a valuable alternative to metallic electrodes has been individuated in highly conductive polymers or, more in general, carbon-based electrodes. Poly(3,4-ethylenedioxythiophene):poly(4-styrenesulfonate) (PEDOT:PSS) has been widely reported as a promising electrode material, enabling the fabrication of cost-effective and flexible organic devices as well as printing-based production [70,71]. Many reports have demonstrated good device performances of p-type OFETs based on PEDOT:PSS electrodes due to its high work function ranging between 4.75 and 5.15 eV [72–74]. Conversely, photo-patternable highly conductive tosylate-doped PEDOT:Tos electrodes, characterized by a very low work function of 4.3eV, have been reported as highly suitable for electron injection in n-type organic devices [75].

As conclusive remarks, given their high conductivity, carbon nanotubes (CNTs) are another class of interesting candidates as electrodes for solution-processible and flexible organic devices [76]: OFETs were demonstrated both for the case of single-walled CNTs and the case of multi-walled CNTs

1.3.2 Measuring techniques for contact resistances

Several techniques can be employed for both direct and indirect measurements of contact resistances in organic transistors: Transmission Line Method (TLM), Gate Four Probes measurements (GFP) and Scanning Kelvin Probe Force Microscopy (SKPFM).

The TLM technique takes advantage of the linear relationship between the channel resistance R_{ch} and the channel length L , expressed by (1.13). Considering the total resistance $R_{tot} = V_{ds}/I_{ds}$ for several devices with different values of L and a fixed gate-source bias, linear extrapolation of the plot to $L = 0$ effectively eliminates the channel resistance and yields indirectly the contact resistance as the y-intercept (Figure 1.13).

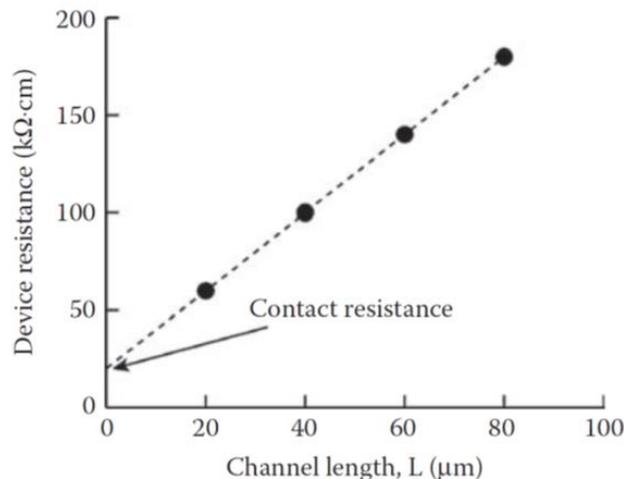


Figure 1.13 Example of a transmission line ($R_{tot} \cdot W$ vs. L) plot at a given V_{gs} value. Extrapolation of the data to a channel length of zero yields the specific contact resistance R_c' as the y-intercept. From [13].

The procedure can be repeated for different values of V_{gs} and V_{ds} in order to investigate the functional trend of R_C with the applied biases [57]. With this straightforward technique, however, drain and source contribution cannot be estimated separately. Moreover, the functional trend R_C Vs L often appears not to be monotonically defined for L approaching 0, resulting in a wide discrepancy between the calculated and the actual R_C values.

The GFP technique overcomes the limitations of the transmission line method by estimating the individual contributions of contact resistances in terms of voltage drops in correspondence of the electrodes. This method utilizes two voltage-sensing probes situated in between the source and drain electrodes, that slightly overlap with the channel area (Figure 1.14a). The local potentials (V_1 and V_2) are thus measured via high-impedance electrometers during transistor operation. Assuming a linear potential drop across the active channel in linear regime ($V_{ds} \ll V_{gs}$), it is thus possible to estimate the voltage drops at the source (ΔV_S) and at the drain electrode (ΔV_D) by comparison with an ideal linear profile induced by the externally applied bias V_{ds} (Figure 1.14b).

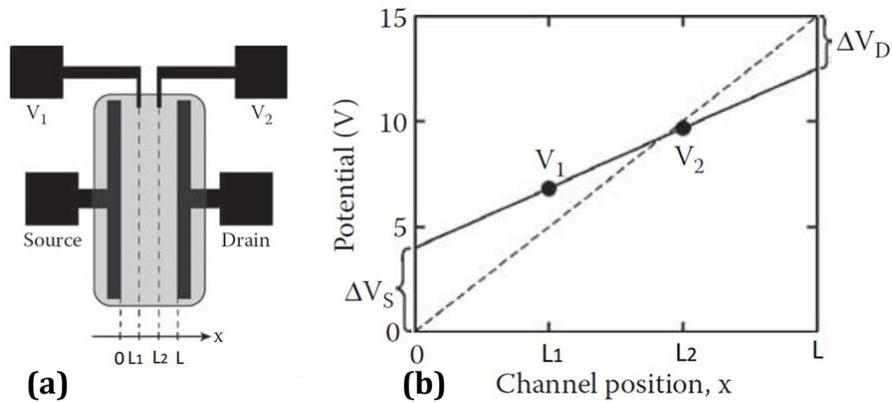


Figure 1.14 (a) Top-view schematic depiction of a device layout for gated four probes measurements. Two narrow voltage-sensing probes protrude into the active channel measuring the local potentials V_1 and V_2 at positions L_1 and L_2 . (b) In linear regime, it is possible to estimate individually the contact resistances at the electrodes by comparing the interpolated profile (solid-line) with the nominal linear profile (dashed-line). Adapted from [13].

Therefore, R_S and R_D can then be simply obtained from Ohm's law as $\Delta V_S/I_{ds}$ and $\Delta V_D/I_{ds}$ for source and drain respectively. However, this method is clearly not valid in the saturation regime, where pinch-off is reached at the drain side and the field profile is highly non-linear.

Point-wise information's on the surface potential profile of the entire active channel, with no limitation on the bias conditions, can be obtained by means of scanning kelvin probe force microscopy. SKPFM is a non-contact potentiometry technique by which the work-function difference between the biased device and an oscillating AFM tip is acquired. The potential profile, for each point, is determined minimizing the electrostatic force building up between the sample and the conductive tip. The potential drop at the contacts can be thus directly visualized with achievable lateral resolutions below 50 nm.

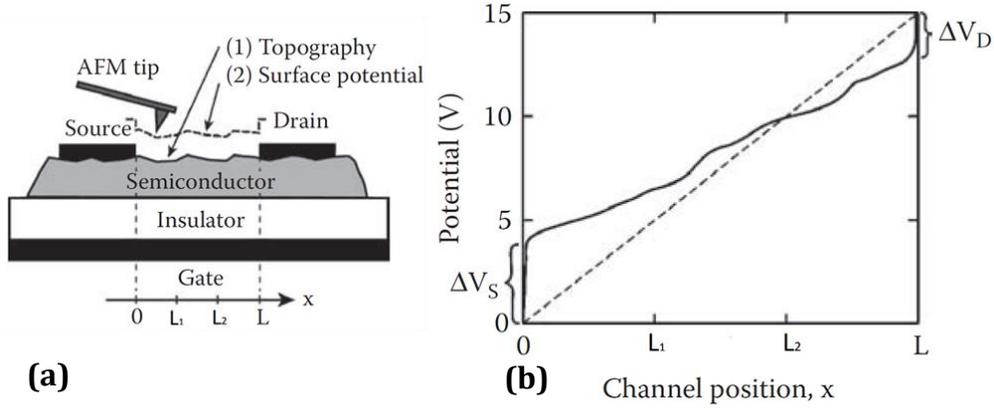


Figure 1.15 (a) Application of SKPFM to characterize an OFET. (b) Hypothetical channel potential profile measured by the SKPFM technique; voltage drops at the source and drain contacts are measured directly. The dashed line is the ideal (no contact resistance) linear potential profile for an applied drain voltage of 15 V. Adapted from [13].

In this work, SKPFM will be employed for the direct evaluation of contact resistances in graphene-based micrometric channel devices with a direct comparison with analogous gold-based devices. Further details on the technique and its applications will be given in Section 4.1.

1.4 TRANSISTOR OPERATION IN DYNAMIC REGIME

For their technological application in complex circuitry, OTFTs must be capable to operate in a dynamical switching regime between a digital on and off state, at high frequencies. The application of an AC signal to the gate electrode results in a rapid charge and discharge of the equivalent capacitor individuated by the MIS structure of the transistor, resulting in a displacement gate current i_G given by [77]:

$$i_G = C_G \frac{\partial v_{gs}}{\partial t} = 2\pi i f C_G v_{gs} \quad (1.17)$$

Where C_G is the equivalent gate capacitance, i is the imaginary unit and f is the switching frequency of the applied gate bias. The AC current gain of the transistor is given by the ratio of the modulus of the frequency-independent drain current (i_D) and the displacement gate current i_G . Since the latter parameter is directly proportional to f , the current gain decreases for increasing frequency. The frequency at which the current gain is equal to unity is therefore defined as the cut-off frequency, also called transfer frequency, f_T :

$$f_T = f \left(\frac{|i_D|}{|i_G|} = 1 \right) = \frac{g_m}{2\pi C_G} \quad (1.18)$$

In (1.17) and (1.18) the gate equivalent capacitance can be assumed as the sum of the channel capacitance (C_{ch}), and the parasitic overlap capacitance (C_o) due to the source and drain electrodes, as schematically depicted in Figure 1.16.

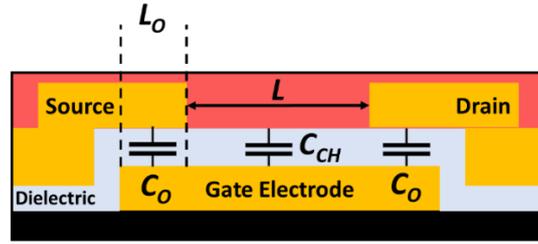


Figure 1.16 Schematic depiction of the channel and overlap capacitances in an OTFT.

Considering the overlap length of the electrodes (L_o), it is possible to directly express the cut-off frequency, in both linear and saturation regimes, in terms of the intrinsic mobility μ_0 and of the channel length L [62]:

$$f_T^{lin} = \frac{\mu_0 V_{ds}}{2\pi L(L + L_o)} \quad (1.19)$$

$$f_T^{sat} = \frac{\mu_0 (V_{gs} - V_{th})}{2\pi L(2/3L + 2L_o)} \quad (1.20),$$

according to which, in the case of negligible contact overlaps, the cut-off frequency scales by $f_T \propto \mu_0/L^2$, so that a reduction of the channel length by one order of magnitude leads to an increase of the transfer frequency by two orders of magnitude. The operational frequencies in OTFTs is thus strictly related to the electrical performances and the lateral dimensions of the devices. Consequently, high transconductances values are needed to ensure maximization of the driving capabilities of the organic transistor, i.e. the maximization of the output i_D , while the influence of parasitic capacitance must be controlled via the optimization of the architectures and the reduction of the overlap between the source/drain and the gate electrode (Figure 1.17a). For devices with reduced dimensionality, the contribution of the contact resistances in linear regime must be taken in to account in the evaluation of the cut-off frequency (Figure 1.17b).

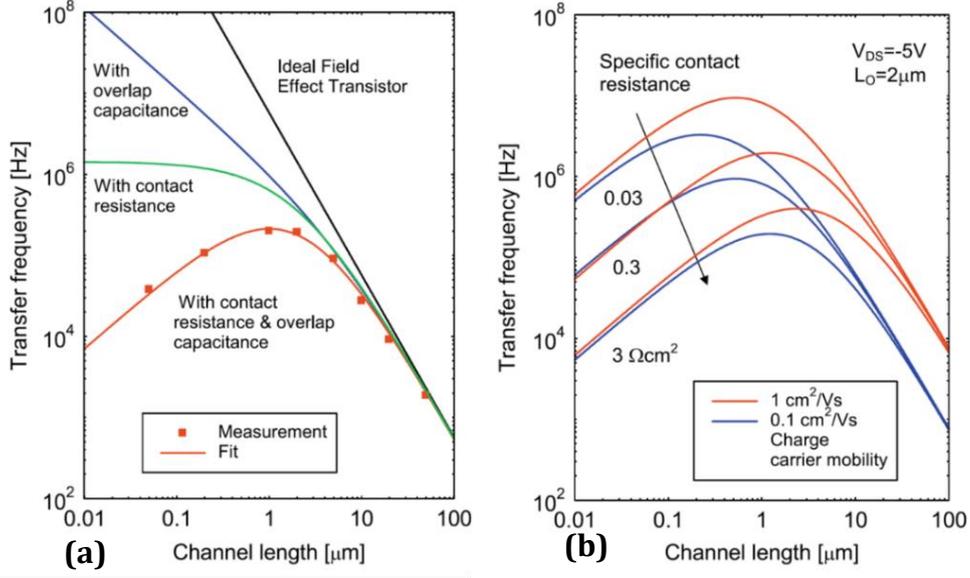


Figure 1.17 (a) Measured cut-off frequency of a dihexyl-7-thiophene (DH7T) staggered top-contacts/bottom-gate thin film transistor as function of the channel length. The data are fitted by taking contact resistances and overlap capacitances between drain/source and gate electrode into account. (b) Influence of the charge carrier mobility and the specific contact resistance on the transfer frequency of devices as function of the channel length with a fixed contact overlap $L_o = 2 \mu\text{m}$. Adapted from [48].

The relation for f_T can be thus reformulated in terms of the contact resistance R_C and the intrinsic charge carrier mobility μ_0 [48]:

$$f_T = \frac{1}{2\pi} \frac{\mu_0 V_{ds}}{[L + C_G R_C W \mu_0 (V_{gs} - V_{th})]^2} \quad (1.21)$$

1.5 SHORT CHANNEL EFFECTS IN NANOMETRIC ARCHITECTURES

OFETs with reduced lateral dimensions are highly desirable for integrated digital circuits since operational frequencies and minimum supply voltages are strictly dependent on the channel length L . However, short-channel devices usually show strong non-idealities that manifest, already at the micrometer scale [78], in the form of supra-linear current-voltage characteristics dominated by Space Charge Limited Current (SCLC) [79], the absence of current saturation for high drain-source biases and high off-state currents related to Drain Induced Barrier Lowering (DIBL)[80,81].

Short-channel effects are primarily due to the presence of highly intense lateral electric fields ($E_x = V_{ds}/L$) building up at the organic channel, which may easily exceed 10^6 Vcm^{-1} for L in the sub-micrometer scale. The presence of high fields can be considered to influence the charge carrier mobility since it reduces the effective depth of trapping states in the organic semiconductor by the Poole-Frenkel effect [82,83]. In the presence of shallow traps in thermal equilibrium with the conduction band, the SCLC contribution in the thin film, enhanced by the Frenkel-Poole effect can be described according to [84]:

$$I_{SCLC} \propto \mu_0 \epsilon_s \epsilon_0 \frac{V_{ds}^2}{L^2} f_{FP}(\sqrt{V_{ds}/L}) \quad (1.22),$$

where μ_0 indicates the intrinsic mobility, ϵ_s is the dielectric constant of the organic semiconductor while $f_{FP}(\sqrt{V_{ds}/L})$ is the Frenkel-Poole contribution given by:

$$f_{FP}(\sqrt{V_{ds}/L}) = \exp\left(\gamma \frac{\sqrt{V_{ds}/L}}{k_b T}\right) \quad (1.23),$$

with γ as material-dependent numerical parameter. The SCLC flows in the entire region of the organic semiconductor, as a bulk contribution, resulting in parabolic I_{ds} - V_{ds} characteristics. Moreover, the space charge contribution shifts the pinch-off towards the source electrode, further reducing the effective length of the accumulated channel. If the effective accumulated length approaches zero, the current flow is dominated solely by the lateral electric field. Channel depletion is hindered by the limited gate modulation, resulting in low on/off current ratios.

In the last years, several studies addressed the influence of short-channel effects in OFETs with sub-micrometric and nanometric architectures [62,85–90], giving numerous insights on the possible strategies to limit their influence on the working condition of the devices.

In their work, Fujimori et al. [63], investigated the systematic contact doping by FeCl₃ in $L=400\text{nm}$, staggered top-contacts/bottom gate pentacene OTFTs. Experimental results suggest that the parabolic increase of drain current is suppressed in devices with undoped contacts (Figure 1.18a). Conversely, a theoretical reduction of the injection barrier

due to the molecular doping in the proximity of the contacts appears to enhance the SCLC contribution and the poor gate tunability of the transistors (Figure 1.18b and c). Similar conclusions can be inferred from the work of Hirose et al. [91]. In this case, the injection barrier is controlled by the ionization potential (or the HOMO level) of various polymeric p-type semiconductors (P3HT, pBTTT and F8T2), in coplanar short-channel devices with channel lengths as small as 30nm. Counterintuitively, the suppression of parabolic drain-source currents and the maximization of on/off ratios are observed for the highest mismatches between the work function of gold-based contacts and the HOMO level of the F8T2. Both the results have been rationalized considering the presence of robust contact resistances in series with the organic channel as a healing factor that prevents the direct application of an intense electric field for increasing V_{ds} and limits the SCLC contribution, although at the expense of a reduced effective charge carrier mobility.

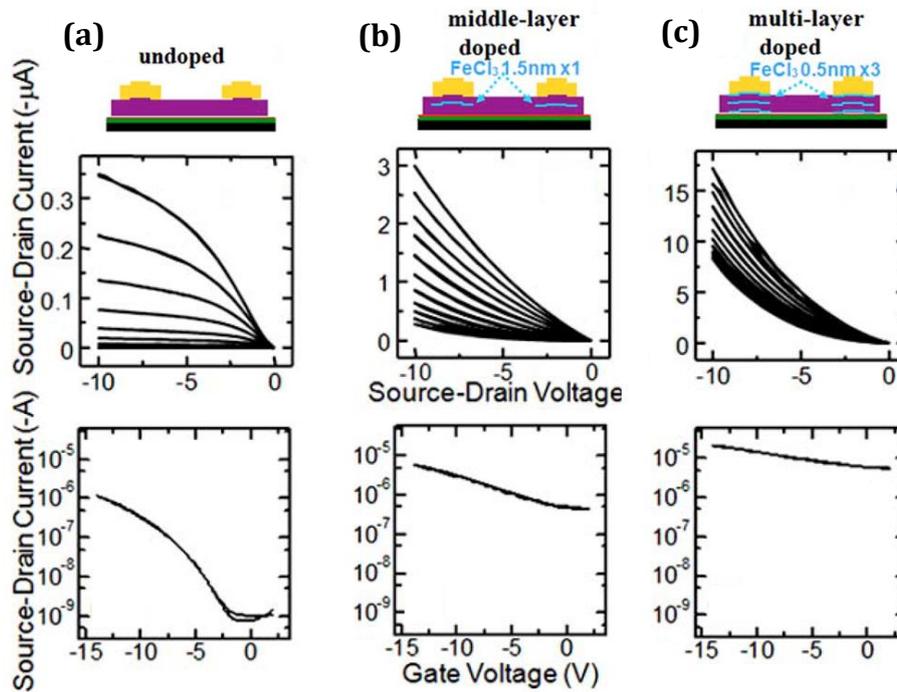


Figure 1.18 Device schematic (upper panels), output characteristics (middle panels) and transfer curves (lower panels) for staggered top-contact/bottom-gate pentacene-based short channel OFETs ($L=400\text{nm}$) with (a) un-doped contacts and with middle-layer (b) and multilayer doping (c) via FeCl_3 . Adapted from [63].

As a final remark, when scaling down the lateral dimensions of an organic device, the gate dielectric thickness (t_{ox}) must be scaled accordingly. As a common rule shared with inorganic MOSFETs, a minimum ratio $L/t_{ox} \approx 20$ must hold [92]. The fulfillment of this constraint typically restores a proper gate-induced modulation of charge carrier density in the accumulation layer and, consequently, the saturation of the output current for increasing V_{ds} (Figure 1.19).

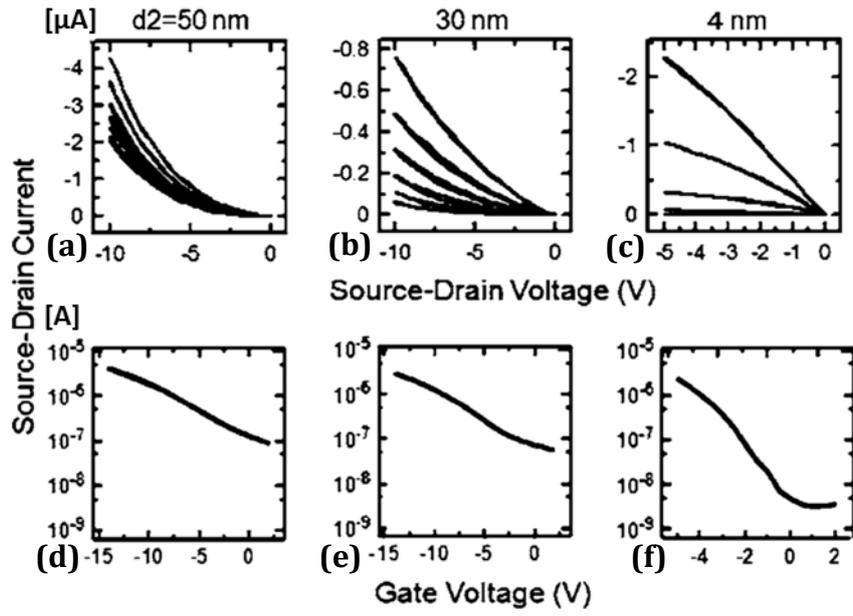


Figure 1.19 Variation of electrical characteristic with dielectric (SiO_2) thickness d_2 . (a)-(c) Output characteristics and (d)-(f) transfer characteristics for short channel OFETs based on pentacene organic thin films with a fixed channel width $2\mu\text{m}$ and channel length $L=200\text{nm}$. From [93]

1.6 GRAPHENE

Graphene is the lastly discovered, and more interesting, allotropic form of carbon. It is the 2D basic constituent of other graphitic systems such as the 1D carbon nanotubes [94] and the 0D fullerenes [95] (Figure 1.20).

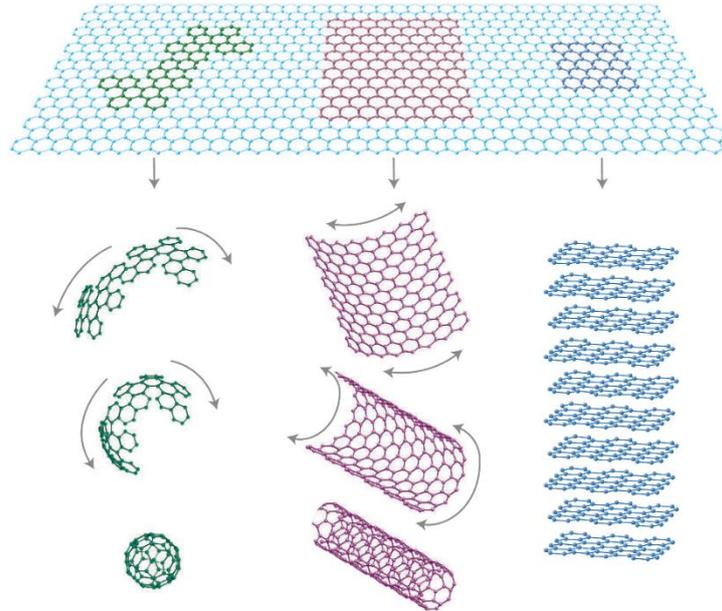


Figure 1.20 : Graphene (top) can be considered as the fundamental 2-dimensional form for all the graphitic derivatives: the 0-dimensional fullerene (left), the 1-dimensional carbon nanotube (central) and the 3-dimensional graphite (right). From [96].

Although graphene properties have been investigated theoretically starting from the late 1940s [97–99], for decades its production in stable-form under ambient conditions was presumed impossible to obtain due to the so called Mermin-Wagner theorem [100,101] according to which long wavelength fluctuations destroy the long-range order for 2D crystals.

Despite the adverse theoretical background, stable graphene flakes were firstly isolated in 2004 by mechanical exfoliation of Highly-Ordered-Pyrolytic-Graphite (HOPG) by Geim and Novoselov [102], both awarded with Nobel Prize in 2010. Since then, the scientific community has seen a restless growth of published papers having graphene as main topic. This huge scientific attention is dragged since, as a material, graphene harbors some remarkable qualities. In the first place, graphene exhibits high electronic quality such that charge carriers can travel ballistically at micrometer scale at room temperature with charge carriers mobility as high as $2.5 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [103]. Moreover, graphene is able to sustain current densities of six order of magnitude higher than copper [104] while showing mesmerizing mechanical and thermal properties: a Young Modulus of 1TPa and intrinsic strength of 130 GPa have been observed [105], as well as a record high thermal conductivity in the range of 1500-5000 WmK^{-1} has been reported [106,107]. The 2-dimensional nature of graphene, furthermore, yields to wavelength-independent optical

absorptions of only $\pi\alpha \approx 2.3\%$ (where α is the fine structure constant) for normal incident light below 3 eV [108].

1.6.1 Electronic Properties

The aforementioned characteristics of graphene are directly related to its electronic band structure whose theoretical framework will be briefly discussed here. Graphene consists of a flat monolayer of sp^2 hybridized carbon atoms which form a hexagonal lattice. Each carbon atom is at $a = 1.42 \text{ \AA}$ from its three neighbors with which it shares three electrons forming in-plane inner thigh σ bonds. The out-of-plane p_z atomic orbitals form a π and π^* hybrid orbital couple, delocalized on the whole layer. The honeycomb lattice of graphene consists of two interleaving triangular sublattices (atoms labeled as A and B in Figure 1.21a), invariant under 120° rotation, that results in an hexagonal first Brillouin zone in the reciprocal lattice (Figure 1.21b)

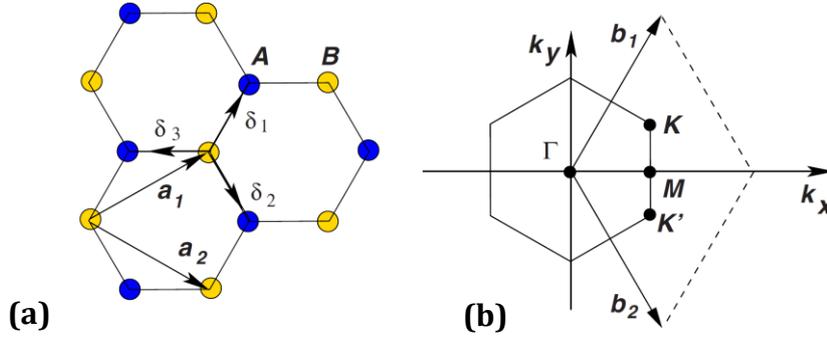


Figure 1.21.: (a) Bravais lattice of graphene is composed by two interleaving triangular lattices. Each unit cell contains two carbon atoms with a_1 and a_2 as base lattice vectors. δ_1 , δ_2 and δ_3 are the vectors in the real space individuating the nearest neighbors. (b) The reciprocal lattice is defined by b_1 and b_2 base vectors. The first Brillouin zone is a hexagon. From [109].

The energy band dispersion of graphene can be solved analytically, following the theoretical framework successfully employed by Wallace in 1947 investigating a single graphite sheet in the tight-binding approximation [97,110], according to which $E(\mathbf{k})$ can be expressed in the form:

$$E_{\pm}(\vec{k}) = \pm t \sqrt{3 + f(\vec{k})} \quad (1.24),$$

with

$$f(\vec{k}) = 2 \cos\left(\sqrt{3}k_y a\right) + 4 \cos\left(\frac{\sqrt{3}}{2}k_y a\right) \cos\left(\frac{3}{2}k_x a\right)$$

where off-diagonal factor t ($\approx 2.7\text{eV}$) individuates the nearest-neighbor hopping energy between the two sublattices A and B , and the plus sign applies to the conduction (π) band while the minus sign is referred to the valence band (π^*). Conduction and valence bands

touch in correspondence of the six corners of the hexagonal first Brillouin points, composed by two series of three equivalent points (K and K' in Figure 1.23a), called Dirac Points.

Energy dispersion (1.24) can be expanded, in terms of the momentum k in the proximity of the Dirac points, obtaining a linear dependence of the form [109]:

$$E_{\pm}(\vec{k}) \approx \pm v_f |\vec{k}| \quad (1.25)$$

Where the fermi velocity $v_f = 3ta/2$ assumes a value of $1 \times 10^6 m/s$. Due to the linear dispersion expressed in (1.25), charge carriers in graphene mimic pseudo-relativistic particles with zero effective mass in correspondence of the Dirac points (Figure 1.23b) and with momentum-independent velocity v_f . For undoped graphene, the Fermi level lies at the apex of these cones which gives its semimetal (or zero band-gap semiconductor) character, according to which the nature of a charge carrier changes at the Dirac point from an electron to a hole or vice-versa.

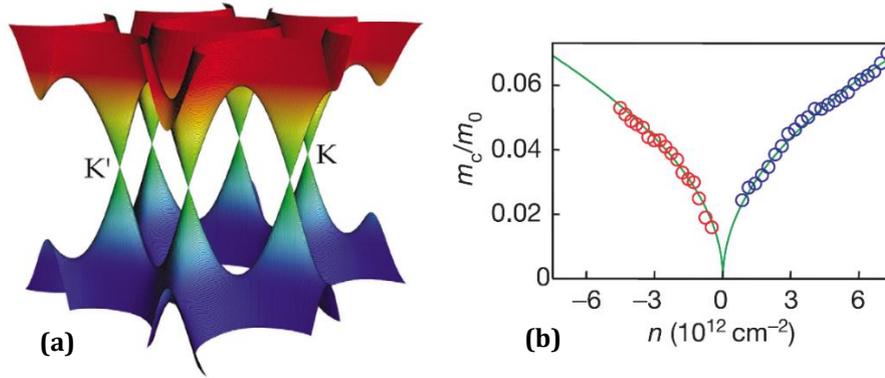


Figure 1.22.: (a) Band structure of graphene. The conduction and valence bands touch in correspondence of the Dirac Points (K and K'). From [111]. (b) Ratio between the cyclotron mass and the rest mass of charge carriers in graphene as function of the charge concentration.

Lastly, in graphene, the density of states ($\rho(\epsilon)$) appears to be characterized by the presence of van Hove singularities far from the Dirac point while it reflects the semi-metallic nature of graphene approaching a degenerate zero value in correspondence of the neutrality point (Figure 1.23), following the relation [109]:

$$\rho(\epsilon) = \frac{2A_c}{\pi} \frac{|\epsilon|}{v_F^2} \quad (1.26)$$

where $A_c = 3\sqrt{3}a^2/2$ indicates the unit cell area. This is in substantial contrast with both graphene nanoribbons and carbon nanotubes for which $\rho(\epsilon)$ follow the geometrical quantization of states in confined nanometric structures and finite energy band gaps are observed.

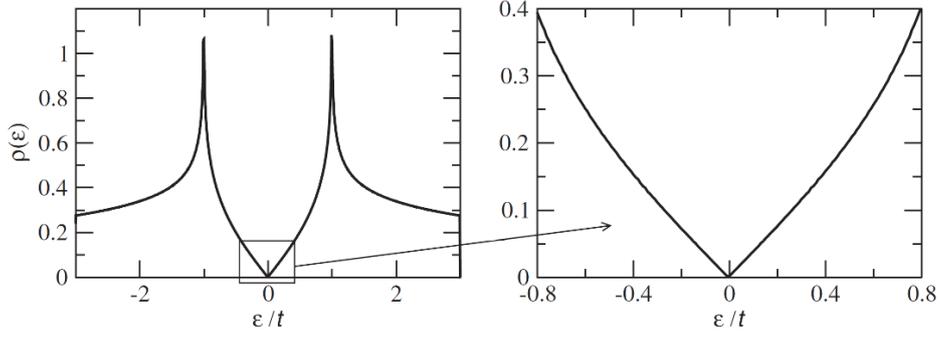


Figure 1.23.: Density of states of graphene for unit cell as function of energy expressed in unit of the hopping energy t . The density of states close to the Dirac point (right panel) is well approximated by $\rho(\epsilon) \propto |\epsilon|$. Adapted from [109].

1.6.2 Charge Transport

Concerning the charge transport properties of graphene, those are usually inferred from graphene-field-effect-transistor (GFET) configuration. Referring to Figure 1.24.a, in a GFET, graphene is transferred on a dielectric surface with metallic contacts acting as the Drain-Source electrodes. The three-contacts configuration is completed by the conductive substrate (usually Si^{++}) acting as bottom gate electrode. The considerations around the working principles of a GFET can be considered analogous to those inferred for an ambipolar OFET. Far from the Dirac point (also called neutrality point), the gate voltage (V_g) induces a surface charge density $n = \epsilon_0 \epsilon_r \Delta V_g / t_{ox} e$, where $\epsilon_0 \epsilon_r$ is the permittivity of the dielectric, e is the electron charge, t_{ox} indicates the dielectric thickness and $\Delta V_g = V_g - V_D$, with V_D indicating the gate voltage at which the Dirac point is located. The charge density n shifts the Fermi level of the graphene between the valence and conduction bands switching accordingly between a hole- and electron-dominated transport, as depicted in the insets of Figure 1.24.b. As result, graphene exhibits a pronounced ambipolar behavior so that charge transport can be continuously tuned between p- and n-type. Approaching the neutrality point, however, the presence of both thermally generated carriers [112] and electrostatic spatial inhomogeneity [113] limit the minimum charge density (n_0) to residual values as high as 10^{12}cm^{-2} , deviating from theoretical models according to which charge density n should vanish as suggested by (1.26). Considering the functional trend of resistivity ρ as function of the applied gate voltage (Figure 1.24.b), it rapidly increases as the Fermi level approach the Dirac Point, where it reaches its maximum value.

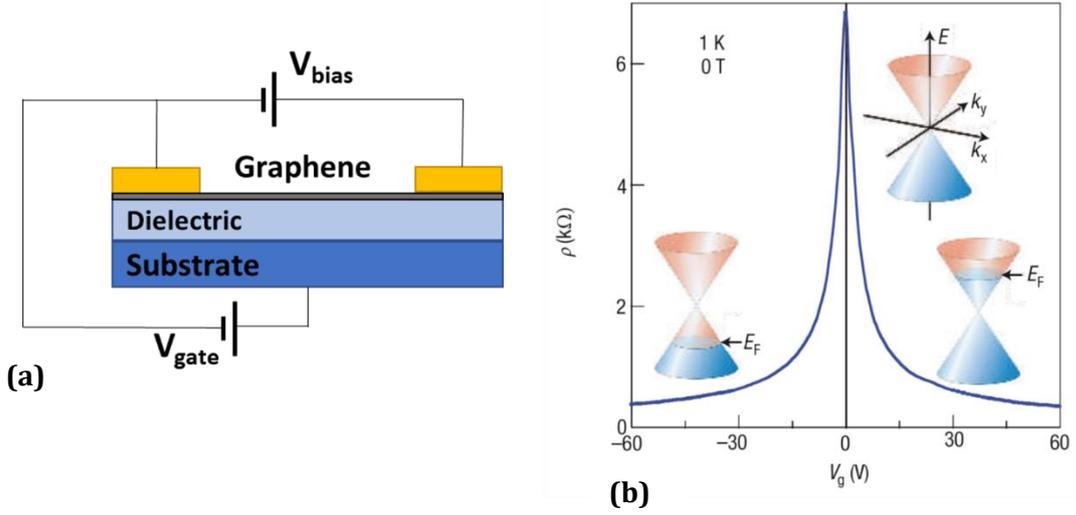


Figure 1.24. (a) Schematic depiction of a Graphene-Field-Effect-Transistor (GFET). (b) GFET resistivity as function of the applied gate bias. The insets highlight the ambipolar nature of the charge carrier transport switching between a hole-dominated regime ($V_g < 0$ and E_f located in the valence band) and an electron-dominated transport ($V_g > 0$ and E_f located in the conduction band). The resistivity approaches a maximum value in correspondence of the Dirac point. From [114].

Experimentally, the ambipolar transport reflects on the total sheet resistivity of the GFET that can be expressed in terms of the gate-modulated charge n density as [115]:

$$\rho_{sheet}(V_g - V_D) = \frac{1}{\mu e n (V_g - V_D)} = \frac{1}{\mu e \sqrt{n_0^2 + (C_g |V_g - V_D|)^2}} \quad (1.27),$$

where e is the elemental charge, n_0 is the residual charge density, $C_g = \epsilon_r \epsilon_0 / t_{ox}$ is the capacitance per unit of area of the dielectric interface and μ indicates the charge carrier mobility. The latter can be considered as a pivotal parameter for estimating the quality of the graphene sample under investigation. Several methods can be employed in determining μ : Transmission Line Method (TLM), Fitting Method (FTM) and Direct Transconductance Method (DTM).

TLM is a standard method to measure the contact resistance of graphene/metal junction [116], as well as of organic-semiconductor/metal-electrode interfaces. It can be further expanded to extract carrier mobility of graphene by considering the total resistance of the graphene sheet as the sum of two contributions due to the contact resistances and the sheet resistance, namely:

$$R_{total}(L) = \rho_{sheet} \frac{L}{W} + \frac{2R_C}{W} \quad (1.28),$$

Where L and W indicate the GFET length and width, respectively, while R_C is the length-independent contribution of the contact resistances per unit of width. By fitting (1.28), of multiple GFETs with different channel length L , biased with the same net gate voltage ($V_g - V_D$), contact resistance R_C and charge carrier mobility μ_{TLM} can be then individuated as the intercept and the slope, respectively.

The FTM method takes advantage of the explicit formula for ρ reported in (1.27), by direct fitting of the total resistivity R_{total} of a single GFET with known channel length L . Namely [115]:

$$R_{total} = \frac{R_C}{W} + \frac{L}{W} \frac{1}{\mu_{FTM} e \sqrt{n_0^2 + (C_g |V_g - V_D|)^2}} \quad (1.29)$$

From which the FTM charge carrier mobility can be extracted as fitting parameter for the n- and p-branches separately.

Lastly, in the DTM methods, charge carrier mobility can be evaluated in total analogy with the procedure described in Section 1.2.1 for determining the charge carrier mobility of the OFETs in linear regime:

$$\mu_{DTM} = g_m \frac{L}{W V_{ds} C_g} \quad (1.30)$$

Where $g_m = \partial I_{ds} / \partial V_{gs}$ is the transconductance of the GFET, μ_{DTM} is the field-effect-mobility and V_{ds} is the applied Drain-Source bias.

1.6.3 Quantum capacitance

Similarly to the scaling strategies for inorganic and organic transistors, in graphene devices the gate-induced charge modulation imposes the ultimate boundary to the lateral dimension in short channel architectures. To maintain sufficient control, the distance between the gate and channel must be simultaneously scaled down by employing thinner gate oxides with higher dielectric constants k , required to improve the field-induced charge accumulation. Despite this, in analogy with other FET system based on two-dimensional electron gas, the total gate capacitance in a GFET is ultimately limited by the rising of the quantum capacitance contribution originated from the finite density of states of the channel and the extra energy needed for filling states with higher momentum [117]. Theoretical considerations on the quantum capacitance contribution of graphene (C_{gr}) are typically inferred from two-dimensional free-electron gas models, providing a quantitative description in terms of Fermi velocity, carrier density, temperature and fundamental physical quantities [118]:

$$C_{gr} \approx e^2 \frac{2eV_{ch}}{\pi(\hbar v_F)^2} = \frac{2e^2}{\hbar v_F \sqrt{\pi}} \sqrt{n(E_f)} \quad (1.31),$$

where v_F is the Fermi velocity of the Dirac electrons, $V_{ch} = E_f/e$ is the graphene channel potential while $n(E_f)$ is the field-effect-induced charge density. Comparing equation (1.31) with equation (1.26), it is clear that the density of states in graphene is directly related to the quantum capacitance by $C_{gr} = e^2 \text{Dos}(E_f)$. According to that, in pure perfect graphene, C_{gr} should vanish in correspondence of the neutrality point. In reality, charged impurities have a key role in the transport properties of graphene near the Dirac point, causing local potential fluctuations and electron/hole puddles in graphene: equation (1.31) must be thus reformulated accordingly, taking in account the residual carrier density n_0 in correspondence of V_D [118] (Figure 1.25a):

$$C_{gr} = \frac{2e^2}{\hbar v_F \sqrt{\pi}} \sqrt{|n(E_f)| + |n_0|} \quad (1.32),$$

Where $n(E_f)$ can be expressed as [119]:

$$n(E_f) = n(eV_{ch}) = \left(\frac{eV_{ch}}{\hbar v_F \sqrt{\pi}} \right)^2 \quad (1.33),$$

Experimentally, quantum contribution in graphene sheet has been successfully measured from capacitance measurements in three-electrode electro-chemical configuration, as reported by Xia et al. [115] (Figure 1.25a).

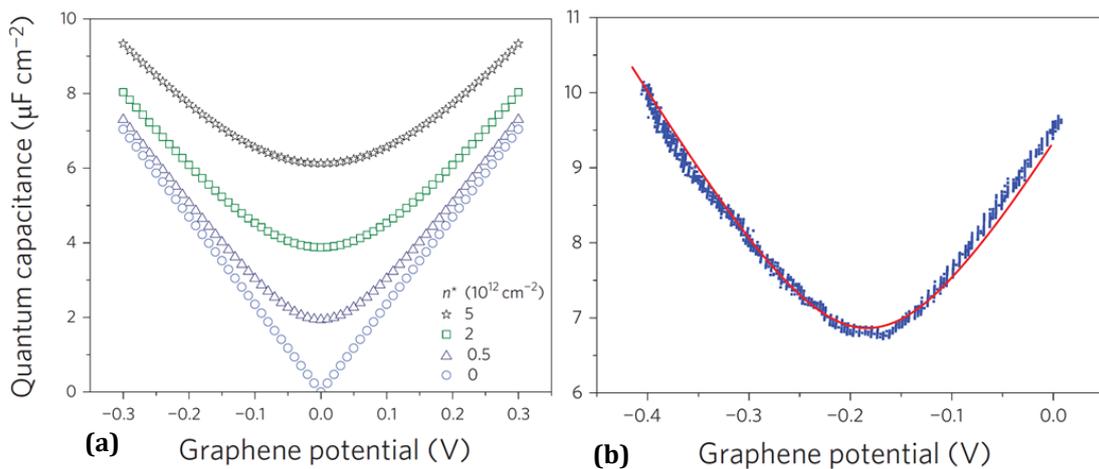


Figure 1.25 (a) Simulated capacitance at different effective charged impurities n^* . (b) Fitting of the measured capacitance (blue symbols) with theory (red line), for electrolyte gate configuration. Adapted from [118].

Additional studies have been focused on double gate architectures based on ultra-thin Y2O3 [120,121] or AlO2 top contacts [122], from which additional information on the residual density of states at the neutrality point and on gap states formation in bi-layer structures can be retrieved.

1.6.4 Doping effects

Being a two-dimensional material, graphene is extremely sensitive to surface adsorbates and its electronic properties can be effectively modified by chemical doping upon exposure with different atoms and molecules. The doping state of graphene reflects directly on the relative position of the neutrality point in GFETs that manifests itself in terms of a rigid shift of the resistivity maximum (or conductivity minimum) towards negative (n-type doping) or positive gate values (p-type doping). Chemical doping can be categorized in surface transfer doping and substitutional doping [123]. The latter refers to the substitution of carbon atoms in the honey-comb lattice of graphene by atoms with different number of valence electrons [124]. In surface transfer doping, on the other hand, graphene properties are modified by electron exchange with atomic or molecular adsorbates. N-type doping of graphene has been observed with exposure of GFETs to potassium atoms [125] while p-type shifts have been reported to NO₂ [126].

Unintentional doping of graphene is quite commonly observed as well. The presence of resist residues due to lithographic processes, the exposure to atmospheric contaminants [127] as well as substrate surface treatments prior to the graphene transfer [128], usually results in p-type doping. Thermal annealing or hard cleaning procedure by means of organic solvents are usually employed in order to restore both the morphological and electrical properties typically encountered in intrinsic samples.

Both n-type and p-type doping of graphene through charge transfer processes can also be controllably induced by surface functionalization with molecular layers. Indeed, aromatic molecules can stably bind to single-layer-graphene films through strong π - π interactions between their aromatic scaffold and the graphene lattice [129]. Experimental evidences on graphene-based devices suggest that the aromatic molecules with electron-donating groups, such as 1,5-naphthalenediamine (Na-NH₂) [129] or vanadylphthalocyanine (VOPc) [130], enhance charge density on the graphene layer inducing n-doping. On the contrary, organic moieties with electron-withdrawing groups, such as tetrasodium 1,3,6,8-pyrenetetrasulfonic acid (TPA) [129], para-hexaphenyl (6P) [131] and tetrafluorotetra-cyanoquinodimethane (F4-TCNQ) [132], are reportedly inducing p-doping. An explicative example is reported in Figure 1.26.

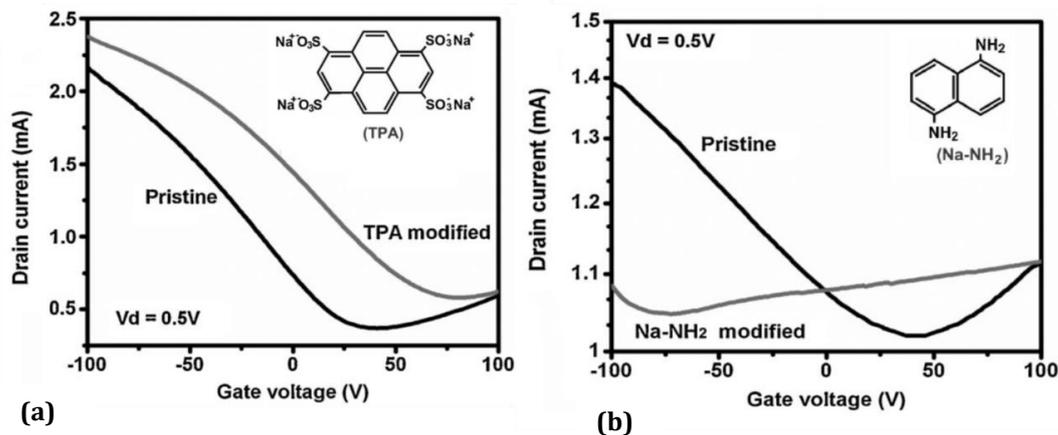


Figure 1.26: Transfer curves (Current vs. gate voltage) for single-layer GFETs (a) before and after TPA doping and (b) before and after Na-NH₂ doping. Adapted from [129].

1.6.5 Production methods of graphene

Up to now, a large number of methods have been proposed for the production of graphene of various dimensions, shapes and quality. These can be categorized into top-down and bottom-up approaches. The former relies on the exfoliation of bulk multi-layered graphite, for example by the mechanical cleavage of bulk HOPG surface by means of simple adhesive tape [66] or by liquid phase exfoliation [133,134].

In the bottom-up approaches, the graphene production is based on the chemical reaction of molecular building blocks to form covalently linked 2D networks. At this category belong the epitaxial growth by graphitization of crystalline silicon Carbide (SiC) [135,136] or the surface-assisted cyclodehydrogenation of linear polyphenylenes from molecular precursors [137].

Lastly, molecular beam deposition [138] as well as laser ablation [139] have been used for the growth of chemically pure graphene, although with huge differences in terms of costs and overall process easiness with respects to other growth processes such as the widely employed chemical-vapor-deposition (CVD) method.

The CVD growth of graphene involves the thermal decomposition of a hydrocarbon source (usually methane CH₄) on a heated substrate on which the process is catalytically enhanced [140]. Transition metals such as Ni, Pd, Ru, Ir or Cu are the most widely used substrates in graphene synthesis [141]. During the reaction, the metal substrate not only works as a catalyst, lowering the energy barrier of the reaction between the carbon atoms, but also determines the graphene deposition mechanism according to its carbon solubility. With transition metals characterized by high carbon solubility (like Ni or Fe), atoms produced from the hydrocarbon precursor dissolve into the metallic substrate during the catalytic decomposition at high temperatures. As the substrate cools down, the dissolved atoms segregate from the metallic bulk forming the graphene layer [142,143]. On the opposite, for low carbon solubility metals, such as copper, carbon atoms nucleate directly on the surface and expand laterally in the form of multiple crystalline domains whose growth process terminate once the substrate is fully covered [144], as

schematically depicted in Figure 1.27a.

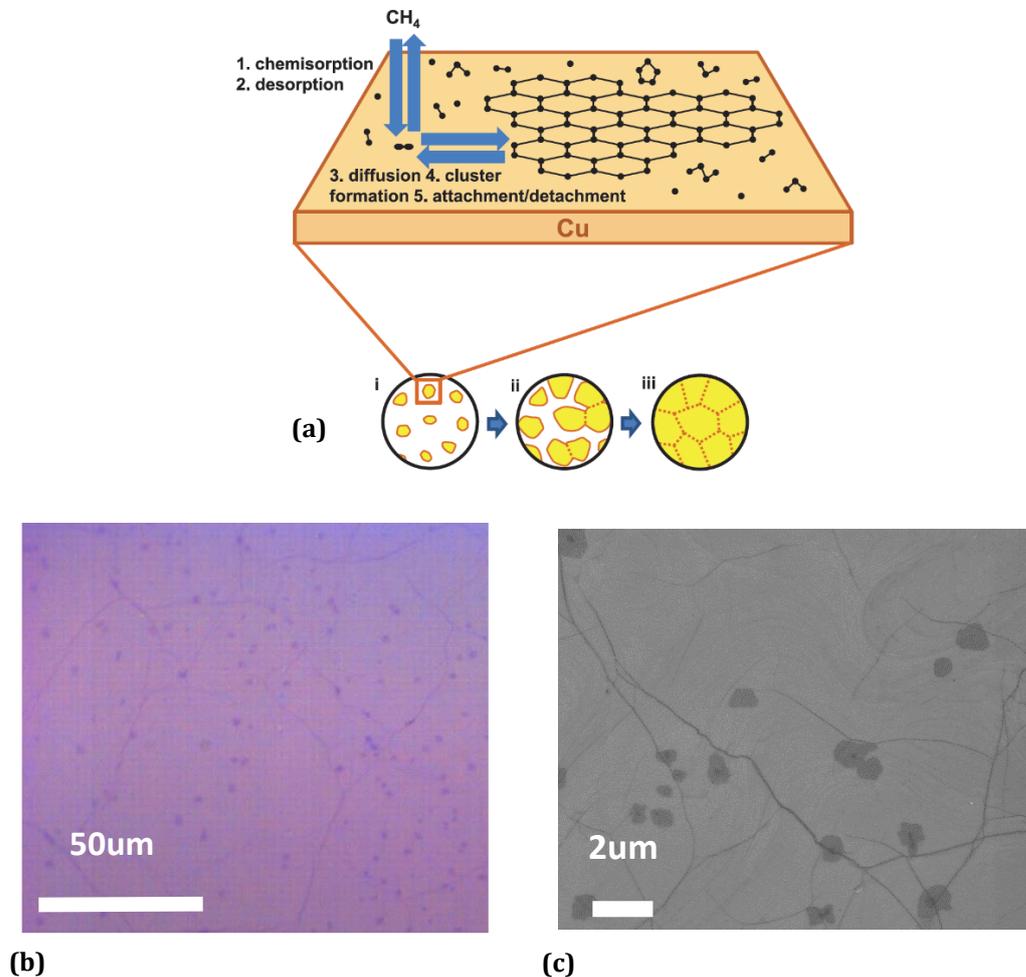


Figure 1.27 (a) Overall illustration of the nucleation and growth mechanism of graphene on Cu. Adapted from [144]. (b) Optical and (c) SEM images of CVD-Graphene transferred on 300nm thick SiO_2 substrate. Multilayered nucleation sites (darker spots) and graphene wrinkles (dark lines) are clearly observable.

Large-area uniform graphene can be then grown by CVD on copper foils with crystal dimensions that are virtually limited solely by the size of the substrate [145]. After the growth process, the graphene sheet is usually transferred on a different substrate to be further processed. A layer of Poly Methyl MethaAcrylate (PMMA) is then spin-coated on the graphene-on-copper surface. The Cu foil is etched by means of iron nitrate and the graphene-on-PMMA stack is then transferred to another substrate. Organic solvents are then used to remove the PMMA, completing the graphene transfer [146].

1.7 GRAPHENE AS NOVEL ELECTRODE MATERIAL FOR ORGANIC ELECTRONICS

Graphene has some remarkable characteristics that justify undoubtedly the scientific attention spent in the last fourteen years. Against this background, the scientific rush often loses sight of one of the major obstacles for graphene applications in integrated circuits as potential Si replacement: graphene should be more conveniently referred as a zero-overlap semimetal rather than a zero-bandgap semiconductor. As a result, low on/off current ratio due to its ambipolar nature, usually observed in GFETs configurations, still limit its application in CMOS technology. Numerous approaches aiming to graphene bandgap engineering have been proposed in the last years [147–150]. Despite that, all the reported methodologies are at their infancy, and uniform and reliable graphene doping over a large area has not been achieved yet.

Nevertheless, graphene applications are not limited to its use as semiconductor in FET technology. It has been demonstrated to be reliably employed in the fabrication of ultra-broadband polarizer for photonic applications [151] and plasmonic meta-surfaces [152], or in the energy harvesting and storage field the development of supercapacitors [153]. Numerous other uses ranging from biosensing [154] to targeted drug delivery [155] have been investigated in the biomedical field, as well.

Among all the promising applications cited so far, recent research has coincided with increased interest in the use of graphene as an electrode material in transistors, light-emitting diodes, solar cells and flexible devices [156–158]. Taking advantages of its intrinsic semi-metallic nature in addition to its excellent mechanical and optical properties, graphene films are promptly closing the technological gap with more common transparent electrodes, such as ITO and other carbon-based alternatives, in terms of sheet resistance and transparency (Figure 1.28).

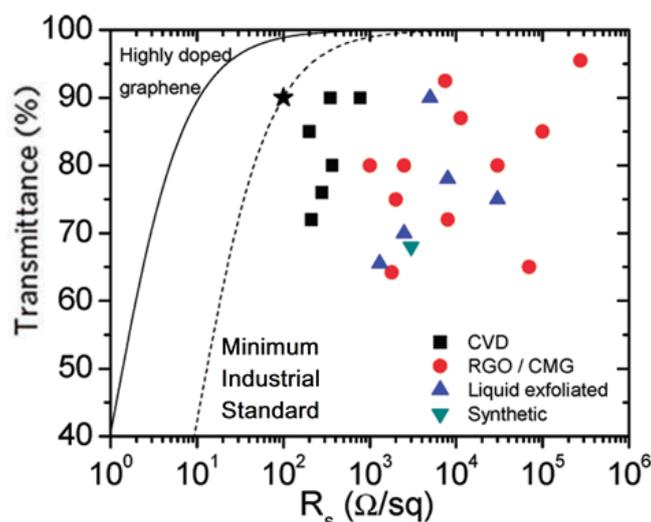


Figure 1.28 Transmittance (%) Vs. sheet resistance (R_s expressed in Ω/sq) data reported in the literature for graphene films prepared by various fabrication methods. The dash line represents the minimum industry standard for transparent electrodes for solar cells. Adapted from [159].

Particular attention has been given to its application as Source-Drain electrodes in organic transistors. Several experimental works have exploited yet the advantages obtained by the use graphene in micrometric architectures. Pentacene OFETs with graphene electrodes, for example, have been reported to exhibit higher current than those with standard Au electrodes [160] (Figure 1.29a and b). In this case, interface dipoles (Δ) measured by Kelvin Probe Microscopy are 0.09 eV for pentacene/graphene and 0.44 eV for pentacene/gold interfaces resulting in a hole-injection barrier (ϕ_b) of 0.29 eV, in the former case, and of 0.54 eV for standard gold electrodes. In addition, morphological changes can also play critical roles in using graphene electrodes, especially when there are significant polymeric residual due to the graphene transfer and patterning, as reported by Lee et al. [161]. Contaminants appear to determine the molecular assembly in correspondence of the electrodes, promoting the stand-up orientation of the pentacene molecules and favoring the interfacial charge transport. In contrast, epitaxial growth of pentacene having molecular assembly of lying-down structure is observed between pentacene and the thermally treated graphene electrode without polymer residues, which adversely affects lateral charge transport at the interface between electrode and channel (Figure 1.29c and d).

Beside its use in p-type organic devices, more recently CVD-graphene monolayer has been successfully employed for high-performance n-channel polymeric OTFTs. In the work of Zhou et al. [162], via a facial spin-coating process, they took advantages of Cs_2CO_3 engineered single layer CVD-graphene, exhibiting a heavy and stable n-doping with a decreased work function of 3.9 eV. Polymeric FETs based on the electron-transporting P(NDI2OD-T2) thin films showed an enhancement of electron mobility by a factor of 10 as well as a reduction of contact resistance compared to the devices using pristine undoped graphene.

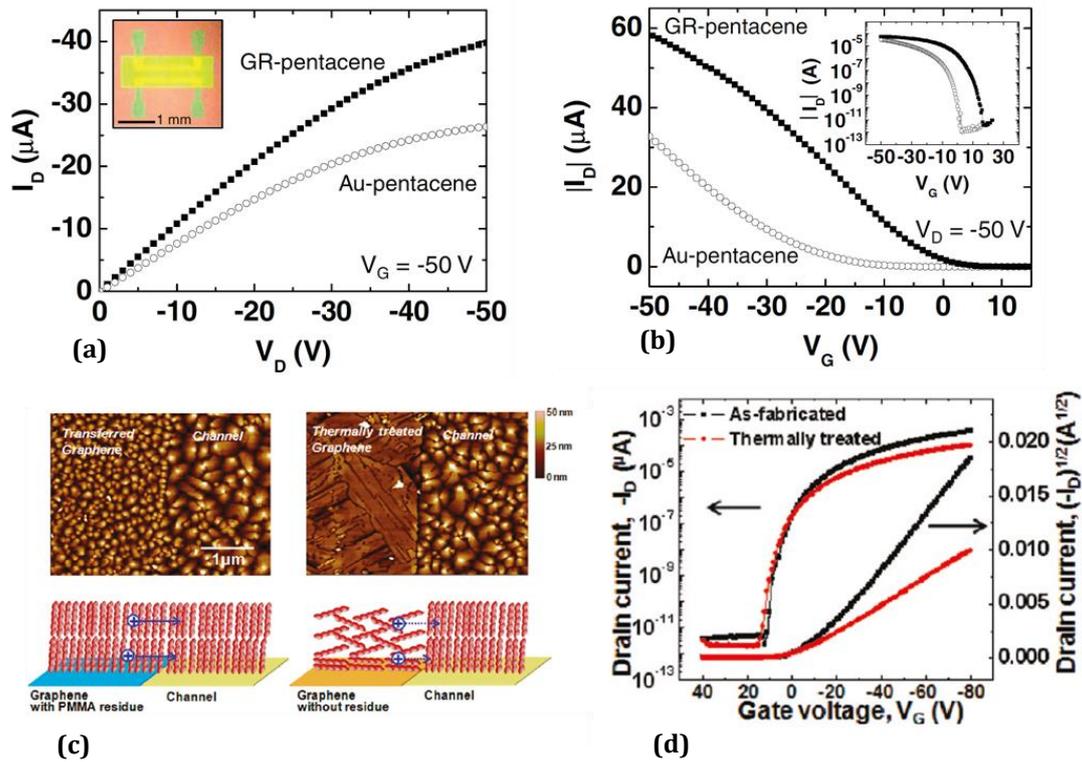


Figure 1.29 (a)-(b) Enhancement of hole injection in coplanar pentacene OFETs with graphene electrodes. Adapted from [160]. (c)-(d) Graphene electrodes with/without residual PMMA affect the morphology of pentacene growth and thus injection. Adapted from [161].

The weak electrostatic screening of the graphene as electrode, due to its degenerate thickness, has been exploited for the same solution processed n-type organic semiconductor in the work of Parui et al. [163]. In this case, the penetration of the gating electric field through the graphene layer modulates the energy levels of the organic semiconductor in vertical diode architectures for which the tunneling contribution appears to play a strong role in the transistor operation.

The use of graphene electrodes for enhancing contact injection in OFETs has mainly been attributed to the tuning capability of graphene work function and its role in determining the injection barrier at the interfaces. As reported by Kim et al. [164], in fact, applying scanning Kelvin Probe Microscope to back-gated GFETs, it has been observed that the graphene work function (W_f) can be effectively tuned by the gate voltage within the range 4.5-4.8 eV for single layer and 4.65-4.75 eV for bi-layer exfoliated graphene flakes (Figure 1.30). In addition, the intrinsic work functions were estimated to be 4.57 ± 0.05 eV and 4.69 ± 0.05 eV for undoped single-layer and bilayer graphene films, respectively.

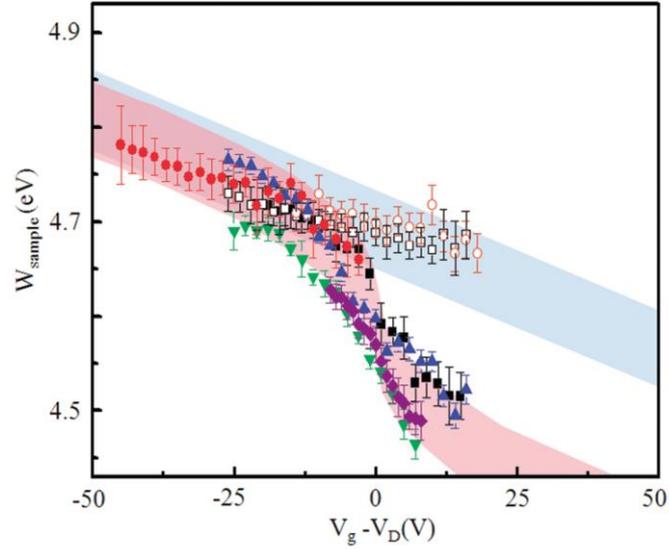


Figure 1.30.: Measured work function of single layer graphene samples (filled symbols) and bilayer graphene samples (open symbols) as a function of effective gate bias ($V_g - V_D$). Single layer samples show larger work function changes (shaded in red) while the bi-layer samples exhibit fewer changes (shaded in blue), where shaded areas indicate the uncertainty for the work function offset due to the adsorbate induced surface dipole layers. From [164].

In the light of this, it is possible to assume the organic/graphene energetic barrier as directly driven by the application of the gate field. In the case of organic transistors based on n-type OSCs, the functional trend of W_f is concordant with charge accumulation: a widening of the interfacial barrier ϕ_b is expected for negative gate biases, hindering at a greater extent the current flow for $V_g - V_D \ll 0$. Conversely, injection barrier lowering is likely to occur for W_f approaching its intrinsic value of $\sim 4.5\text{eV}$ with $V_g - V_D > 0$. These phenomena will be considered as key factors in the observed mitigation of short channel effects in graphene-based OFETs with nanometric architecture, as it will be exhaustively described in the experimental section of this work.

2 DEVICE FABRICATION

In this chapter, the employed techniques and procedures for the fabrication of both nanometric and micrometric graphene-based layouts will be discussed. Three different device architectures will be described:

- Coplanar bottom-contacts/distributed bottom-gate nanometric layouts with graphene-based and gold-based electrodes.
- Coplanar bottom-contacts/local-bottom-gate graphene-based nanometric layout with Hafnium Dioxide as high-k dielectric.
- Micrometric coplanar bottom-contacts/bottom-gate interdigitated architectures with both graphene electrodes or with hybrid structures (one gold-based and one graphene-based electrode)

In the conclusive sections, the principles behind organic thin film growth will be briefly discussed, focusing the attention on the experimental set-up employed for the thermal evaporation of the perylene diimides thin films.

2.1 ELECTRON BEAM LITHOGRAPHY

Electron Beam Lithography (EBL) is a widely employed process in nanotechnology in which a user-defined pattern is engraved on an electron-sensitive material, defined as resist [165]. Usually, the e-beam resists are high molecular weight polymers dissolved in a liquid solvent. The EBL process consists of three main steps: resist coating, exposure and development. A schematic depiction of the main processes involved is shown in Figure 2.1.

As a first step, the resist liquid is dropped onto the substrate and then spun at high speed to form a thin coating. The thickness of the layer is precisely defined by the viscosity of the solution and the rotating speed of the substrate. Afterwards, the substrate is usually annealed at a moderate temperature (typically between 100°C and 200°C) in order to eliminate the casting solvent and to obtain an overall uniform layer. The lithography is then achieved by the inelastic collisions of electrons of the beam with the polymeric chains of the resist that are split in smaller and more soluble fragments for positive tone resists, such as the Poly MethylMethaAcrylate (PMMA) [166]. Conversely, in a negative tone resist, the electrons transforms the material into a low solubility medium by cross-linking of smaller polymer chains into larger and less soluble fragments, as in the case of hydrogen-silsesquioxane (HSQ) [167]. After the exposure, the sample is then immersed in a liquid developer that selectively dissolves the exposed (positive tone) or the non-exposed (negative tone) complementary pattern. The sample is further processed by growing an external material on the top of it or by etching the substrate in correspondence of the patterned surface, where the resist has been removed. The residual resist is thus removed by plunging the processed sample in organic solvents (Lift-off).

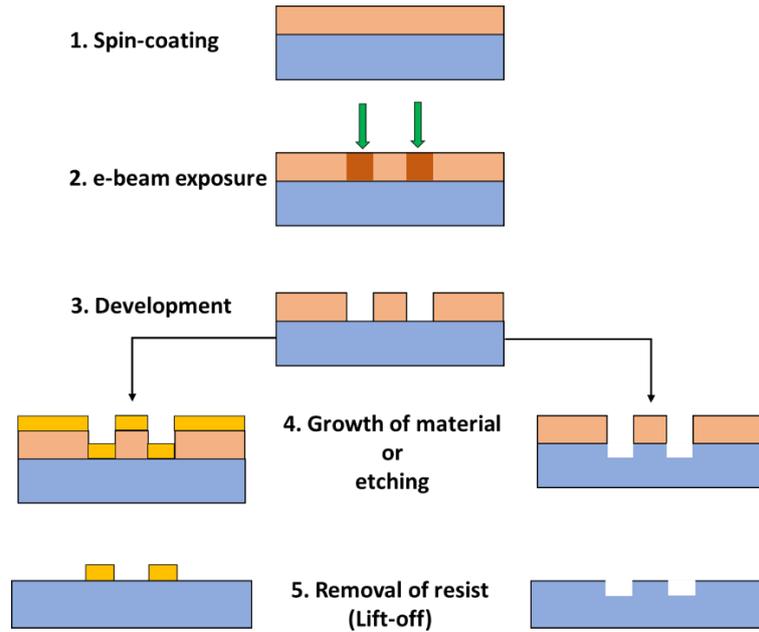


Figure 2.1 Schematic depiction of the different steps of electron beam lithography.

The primary advantage of EBL is that it overcomes the diffraction limit imposed on conventional UV-Vis lithographic processes, allowing the patterning of arbitrary structures with minimum features below 10nm. The resolution limits are achieved by the optimization of several parameters such as the physical dimension of the electron beam, its energy, the pattern density, the resist material as well as its thickness, the development time and temperature, and the fine tuning of the area dose D to which the polymeric resist is subjected. The latter parameter is defined as the electric charge impinging on the sample per unit of surface, usually expressed in $\mu C/cm^2$. Namely:

$$D = \frac{I t}{S^2} \quad (2.1),$$

where I is the beam current, t is the exposure time and S is the step-size of the electron beam. In addition to that, proximity effects due to forward- and back-scattered electrons usually limit the actual lateral resolution causing pattern distortion and overexposure of the resist [168].

2.1.1 The EBL experimental set-up

In the EBL process, the column of a Scanning Electron Microscope (SEM) is typically exploited for the generation of a highly focused electron beam rastering on the resist layer. The EBL system employed for the manufacturing of the samples throughout this work is a Carl Zeiss Sigma-Gemini SEM system equipped with a Raith Elphy Quantum pattern generator, controlled via the NanoSuite software interface (Figure 2.2).



Figure 2.2 EBL facility based on a Carl Zeiss Sigma-Gemini SEM system equipped with a Raith Elphy Quantum patterning unit. The set-up is located in the NanoFab laboratories at the CNR-NANO-S3 institute of Modena, Italy.

The system is schematically depicted in Figure 2.3. Electrons are produced by thermal field emission from a tungsten needle coated with zirconium oxide, in ultra-high vacuum conditions ($P \approx 10^{-10} \text{ mbar}$). They are consequently accelerated through a series of anodes by the application of voltages with values in the range between 0.2kV and 20kV. The beam is then injected in the column where it is skimmed via a micrometric aperture whose diameter can be selected from a rotating metallic plate. The choice of the aperture defines the current I of the beam: diameters of 7.5 μm , 10 μm , 30 μm , 60 μm and 120 μm can be selected. The e-beam thus passes through a blanking stage in which a system of electrostatic plates can controllably hinder the electrons from impinging on the substrates, so that only the desired resist area is exposed to the irradiating beam. A deflector control unit at the bottom of the SEM column deflects the beam accordingly with a user-defined CAD file. Finally, a series of electronic lenses permits the focusing of the beam and the correction of defects such as astigmatism.

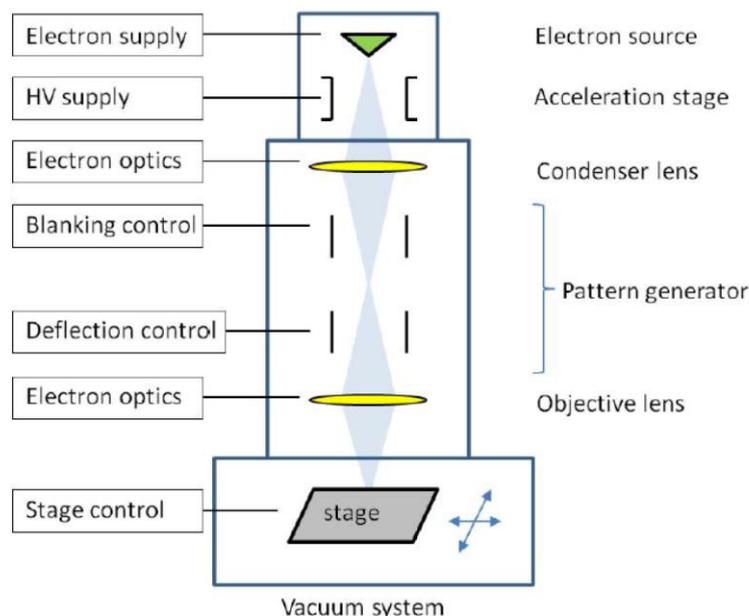


Figure 2.3 Schematic depiction of the EBL experimental set-up. The electrons generated by field-emission are accelerated at high voltages. The electron beam is then focused by a system of electrostatic lenses while the blanking and deflection units control the generation of the nanometric pattern on the sample.

2.1.2 Enhanced sensitivity of PMMA 950K as positive e-resist using amyl acetate-based developers.

According to (2.1), the exposure time is inversely proportional to the beam current I . Since this latter parameter is fixed by the set-up specifications, it is thus clear that the writing time is primarily governed by the material-dependent dose to clear D_0 , i.e. the minimum required dose in order to dissolve the exposed resist area for its entire thickness. The EBL can be thus a time-consuming method whose process speed relies exclusively on the interplay between the developer solvent and the chemical properties of the polymer upon irradiation. Many resists have been developed over the years suitable for attaining required resolutions in lesser EBL writing time [169]. PMMA was the first resist of the methacrylate family and is still regarded as the most widely used high-resolution EBL polymer. Throughout this work, the resist employed for the nano-fabrication of the devices is a solution of PMMA 950K with 4% of solid content in ethyl-lactate (All-Resist, AR-P-679.04). The standardized procedure suggested by the manufacturer indicates the development of the exposed areas in the AR600-56 developer (a methyl isobutyl ketone MIBK and IPA solution specific for PMMA resists) for 2 minutes at 20°C. In this case, observed doses to clear are in the range of 250-300 $\mu\text{C}/\text{cm}^2$ at 20kV. Lower values can be obtained by using more expensive derivatives of the methacrylate family, such as the ZEP520 [170] or the chemically semi-amplified CSAR62 [171] for which doses in the range of 60-100 $\mu\text{C}/\text{cm}^2$ are typically indicated. However, switching from AR600-56 to AR600-54/6 (an amyl acetate-based developer, specific for CSAR62 resist), a reduction of 2/3 in terms of nominal exposure doses has been observed for standard PMMA 950K. Particularly, a nominal dose of $D_0 \approx 80 \mu\text{C}/\text{cm}^2$ can be employed, achieving yet the same

lithographic resolutions obtained with higher doses and the standard PMMA-specific developing procedure, while reducing the proximity effects in high-resolution nano structures. A qualitative analysis has been performed in order to have a preliminary insight on the observed sensitivity enhancement of PMMA. Dosal arrays have been patterned on a SiO₂ (300 nm)/Si substrates with both a 220nm and 280nm resist layers, spun at 4000 rpm and 6000 rpm respectively. A nominal dose of 100 $\mu\text{C}/\text{cm}^2$ has been chosen as reference value. Referring to Figure 2.4a and b, it is possible to observe under-exposure for patterned areas with $D \leq 50 \mu\text{C}/\text{cm}^2$. Single pixel lines with a nominal dose of 300 pC/cm has been investigated as well: nano trenches with a width of 70nm and 50nm can be easily obtained for both PMMA layer thicknesses (Figure 2.4c and d).

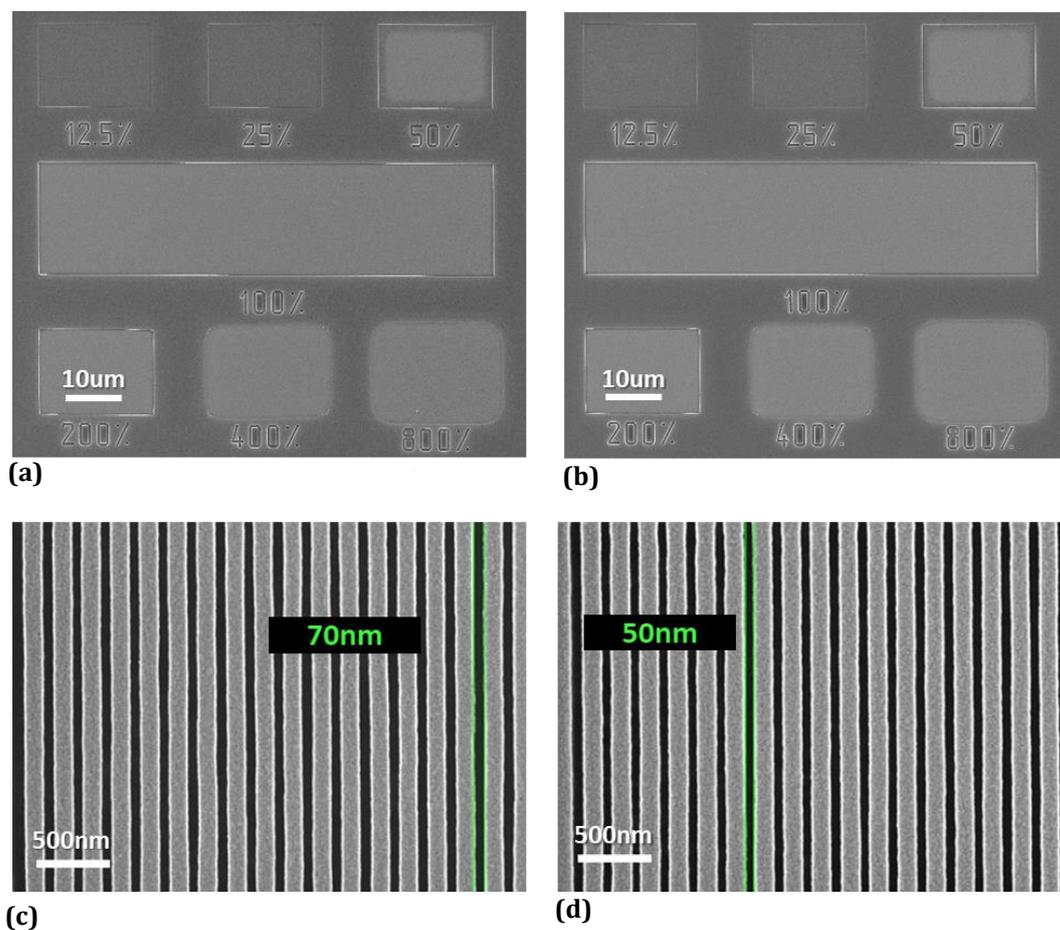


Figure 2.4 (a) Dose test on the 280 thick PMMA 950K layer (spun at 4000rpm for 60s). The nominal dose (referred as 100%) is of 100 $\mu\text{C}/\text{cm}^2$. (b) Equivalent test pattern for a 220nm thick layer (6000rpm for 60s). (c)-(d) Nanometric trenches with a 200nm pitch, patterned by means of single pixel lines with a nominal dose of 300pC/cm for a 280nm and a 220nm thick PMMA950K layers, respectively.

The development process appears to be highly selective in terms of the molecular weight of the exposed PMMA, as can be observed in Figure 2.5a and b. By immersion in the AR-600-56 (PMMA-specific) for 90s, the areas exposed to a dose of 85 $\mu\text{C}/\text{cm}^2$ appears to be poorly dissolved. Adding a subsequent development step in AR-600-54/6 (CSAR-62-

specific), PMMA residues are totally cleared. Moreover, the unexposed complementary surfaces appear not to be affected by the amyl-acetate-based developer in any way. From profilometry measurements, in fact, the nominal resist thickness appears to be unaffected by the AR-600-54/6 (Figure 2.5c and d).

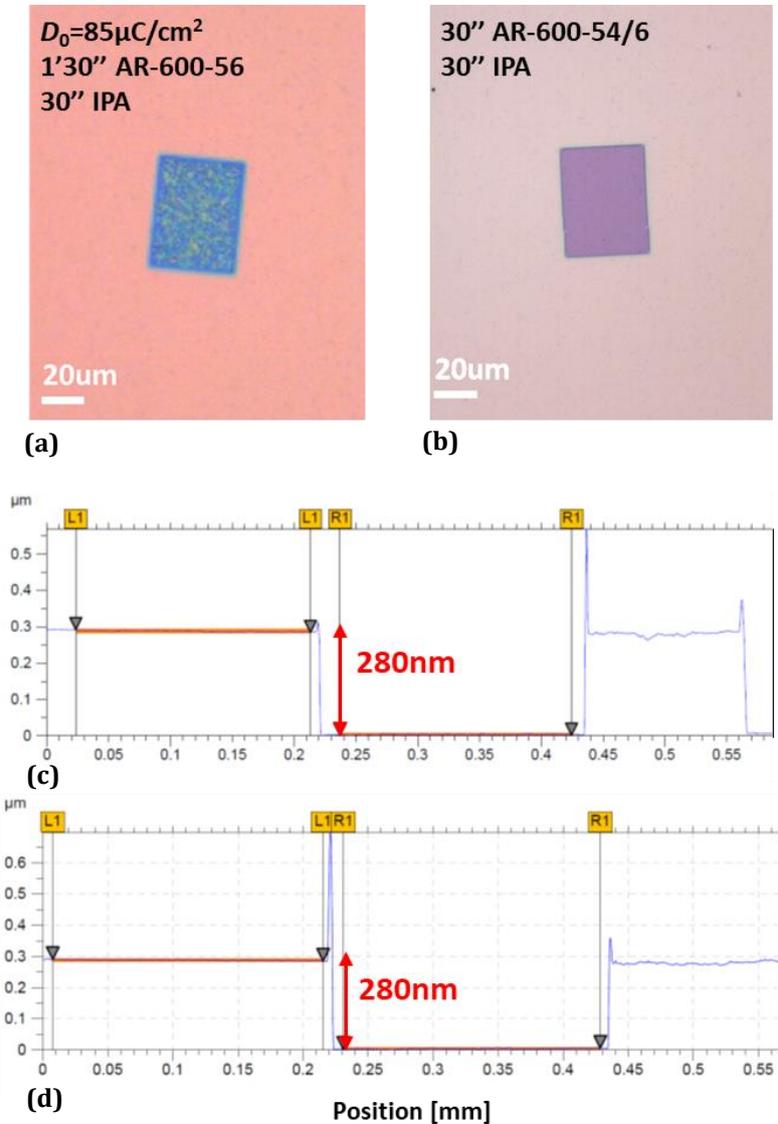


Figure 2.5 (a) Optical image of a micrometric surface exposed to an area dose of $85\mu\text{C}/\text{cm}^2$ and developed by means of the PMMA-specific AR-600-56 developer. In this case, the resist results under-exposed. (b) The area is observed to be totally cleared by subsequent immersion of the same sample in the AR-600-54/6 developer for 30'', indicating its high dissolution selectivity in terms of molecular weight of the exposed resist. (c)-(d) Profilometry measurements on a 280nm thick PMMA950K layer before and after the immersion in AR-600-54/6, respectively.

2.2 REACTIVE ION ETCHING

The reactive ion etching (RIE) is a dry etching technique based on a chemical reactive plasma generated by an electromagnetic field, in low-pressure conditions. An Advanced

Vacuum Vision 300 RIE system (Figure 2.6) has been employed throughout this work for the graphene etching. The set-up is composed by a graphite-coated sample platen enclosed in a cylindrical vacuum chamber from which is electrically isolated. A gas diffuser injects a selected gaseous species in the chamber with a controlled flux (expressed in sccm). The system is equipped with four different gas lines: Ar, O₂, CH₃ and CF₄. Since O₂ reacts with graphene to form graphene oxide and volatile byproducts, it is a natural choice as an etching gas. The plasma is generated by the application of a strong radio-frequency ($f=13.56$ MHz) electromagnetic field with a maximum power of 600W. Electrons removed from the ionized gas molecules are partially absorbed by the grounded chamber walls, inducing a strong potential difference between its upper section and the sample platen located in the lower section which acts as cathode. Positive ions are thus drifted towards the cathode surface where they react chemically with the material of the sample.

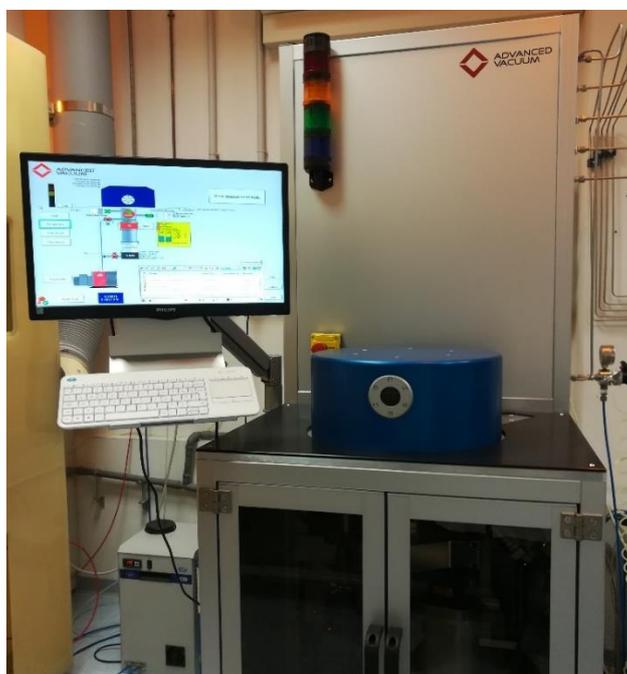


Figure 2.6 Advanced Vacuum Vision 300 RIE system located at the departments of physics of the university of Modena and Reggio Emilia.

2.3 HMDS DEPOSITION FROM VAPOR PRECURSOR

As reported in Section 1.2.1.1, the dielectric interface in OFETs is typically passivated by means of Self Assembling Monolayers (SAMs) in order to mitigate trapping phenomena at the gate interface and to improve the overall morphology during the organic thin film growth. In this work, SiO₂ substrates have been functionalized by means of Hexamethyldisilazane (HMDS provided by Sigma-Aldrich) from vapor precursor. The experimental set-up is shown in Figure 2.7a. Samples are placed inside the oven kept at 150°C and then annealed in dynamic vacuum ($P < 1$ torr) for 1 hour to ensure the removal

of ambient moisture from the surface and to promote the HMDS adhesion. A three-fold purging process of the HMDS gas line is performed by repeatedly injecting N₂ gas inside the oven and pumping down to restore a pressure of 10 torr. The HMDS vapor is produced by the sublimation of the liquid precursor contained in an external reservoir. The samples are then exposed to the HMDS-saturated atmosphere at a constant pressure of 8 torr for a time interval ranging from 1 to 4 hours. HMDS molecules react primarily with the silanol groups (-OH) on the SiO₂ surface while non-polar methyl groups (-CH₃) self-assemble on the surface, providing a hydrophobic monolayer with correspondingly low surface energy features (Figure 2.7b). The deposition is completed by a further purging cycle by N₂.

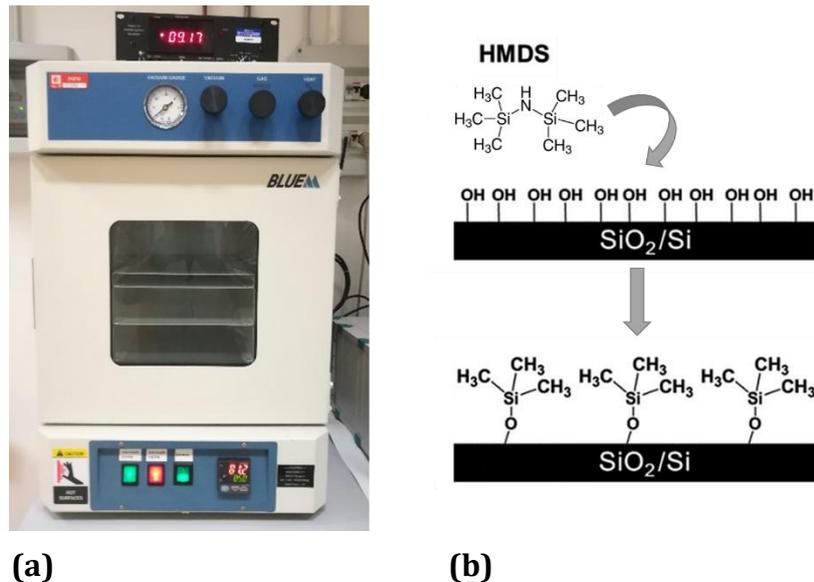


Figure 2.7 (a) Vacuum oven employed for the HMDS deposition from vapor precursor. (b) Schematic depiction of the self-assembling of the HMDS molecules interacting with the silanol groups at the SiO₂ interface.

2.4 BOTTOM-CONTACTS/DISTRIBUTED-BOTTOM-GATE NANO-OFET

LAYOUT

Graphene electrodes are patterned by a three-steps EBL procedure starting from a large area CVD-graphene sheet, transferred on a multi-layer wafer (5x5 mm²) consisting of a 300 nm thick thermal SiO₂ dielectric buffer on the top of a p⁺⁺ doped Si substrate. The latter acts as distributed gate electrode in the final layout. Graphene substrates were prepared in collaboration with Dr. N. Mishra and Dr. C. Coletti (Istituto Italiano di Tecnologia, Pisa, Italy) following the wet-transfer approach described in [172]. In the following section, the fabrication procedures are reported in detail.

- **First fabrication step: graphene contacting and alignment markers.**

The first EBL session is aimed to the fabrication of gold contacts on the graphene and dedicated markers used for the electron beam alignment in the following lithographic sessions. The graphene substrate is firstly cleaned in acetone, rinsed in isopropanol

(IPA) and blow-dried with N₂ gas in order to eliminate possible contaminants and to improve a uniform resist adhesion. The sample is thus covered by a liquid solution (4% in ethyl-lactate) of PMMA 950K (All-Resist AR-P-600.79). A 270nm thick resist layer is obtained by spin-coating at 4000 rpm for 60 s. The substrate is annealed afterwards at 115°C for 15 minutes in order to remove the residual solvent. The contacts array is patterned by EBL within a 50μm² write-field using a beam aperture of 7.5μm and an area dose D= 320 μC/cm² with an acceleration voltage of 20kV. A further set of alignment markers is patterned in a larger write-field (1000 μm², 30 μm aperture and D=260 μC/cm²). The process is then repeated over a matrix of 16 areas of 1 mm² tiling the entire substrate. The exposed pattern is developed by immersion in a MIBK:IPA solution (All-Resist AR-600-56) for 2 minutes at 20°C and then rinsed in IPA for 30s to stop the dissolution process. A bi-layer of Cr/Au (3nm/30nm) is thermally evaporated on the sample with a deposition rate of 0.8 Å/s. This procedure was performed in a thermal evaporation system under vacuum (base pressure of 10⁻⁷mbar) monitoring the film thickness and deposition rate by means of a quartz microbalance. The lift-off is performed by immersion of the sample in acetone at 65°C for 4 hours. The obtained gold pattern is shown in Figure 2.8.

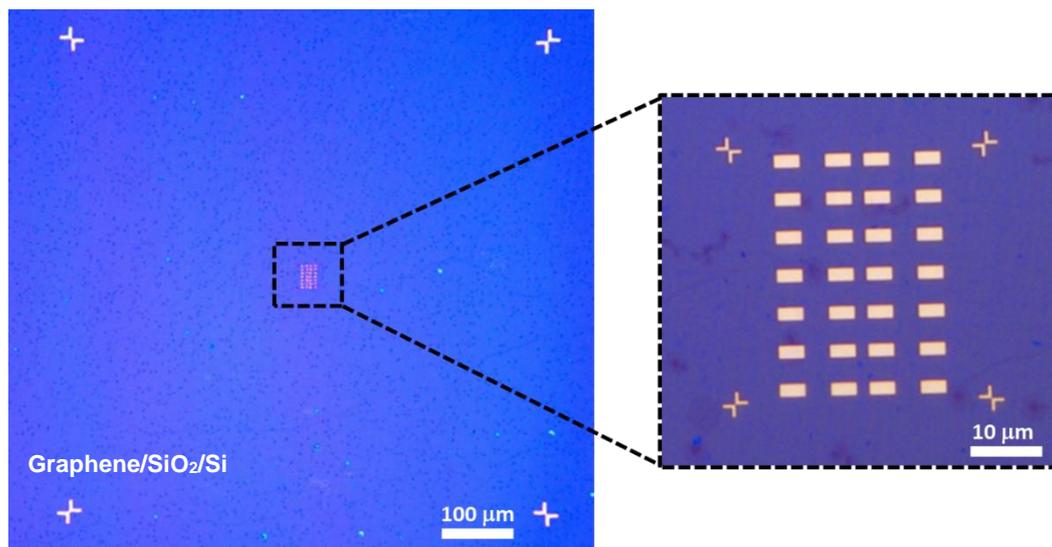


Figure 2.8 Optical images of the first array of gold contacts (Cr/Au 3nm/30nm) and alignment markers (crosses) over-imposed on the graphene substrate.

- **Second Fabrication Step: probe pads and electrical interconnections**

For the electrical characterization of the nano devices, an easily accessible array of probe pads (150 μm x 150 μm) and electrical interconnections is over imposed on the pre-patterned gold contacts. The sample is spin-coated with PMMA using the same parameters of the previous fabrication step. Electrical interconnections and contact pads are patterned through a second EBL process by repeatedly aligning a 100 μm²

write-field ($7.5\ \mu\text{m}$ aperture, $D=280\ \mu\text{C}/\text{cm}^2$ at 20kV) and a $1000\ \mu\text{m}^2$ write-field ($120\ \mu\text{m}$ aperture, $D=280\ \mu\text{C}/\text{cm}^2$), on each of the 16 areas containing the pre-deposited contact arrays, through the dedicated markers. The exposed patterns are developed in AR-600-56 for 2 minutes at 20°C . Graphene is thus removed in correspondence only of the exposed areas by means of the oxygen plasma RIE ($P=10\text{mTorr}$, 20sccm at 50W for 20 s). Figure 2.9 shows the gold layout obtained after the thermal evaporation of a Cr/Au ($5\text{nm}/50\text{nm}$) layer followed by the lift-off in acetone at 65°C for 4h.

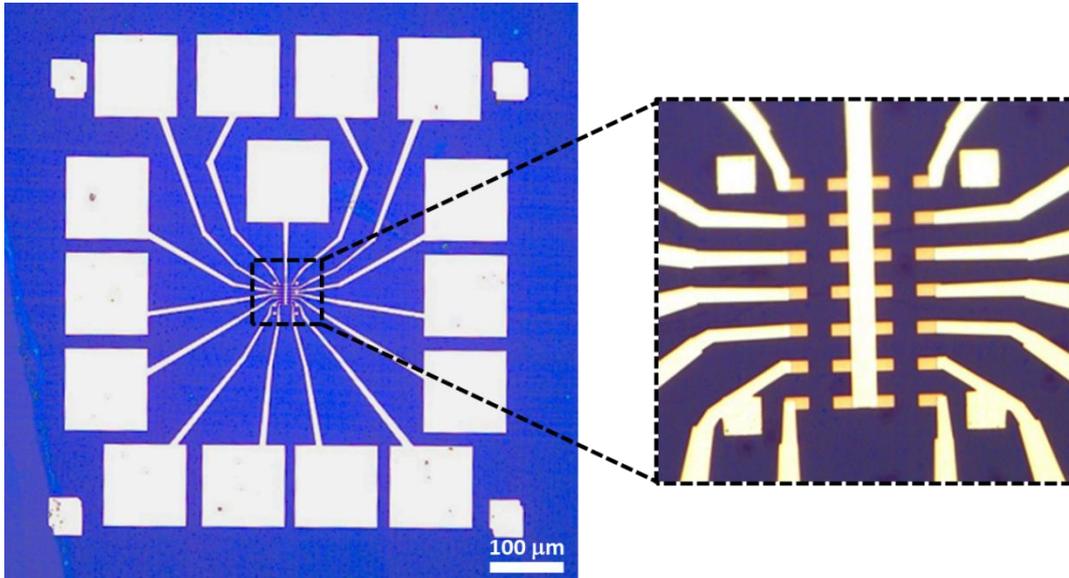


Figure 2.9 Optical images of the gold pads and electrical interconnection ($5\text{nm}/50\text{nm}$ Cr/Au) over-imposed on the graphene contacts.

- **Third Fabrication Step: nano-patterning of the graphene electrodes.**

In the last fabrication step, the sample is spin-coated with PMMA at $6000\ \text{rpm}$ for 60 s, resulting in a $220\ \text{nm}$ thick layer. The resist deposition is followed by a thermal annealing at 180°C for 5 minutes. The third EBL session is aimed to the removal of graphene over the entire device area (1mm^2) except for the electrode surfaces. Resist is exposed throughout the $1000\ \mu\text{m}^2$ write-field with an area dose $D=280\ \mu\text{C}/\text{cm}^2$ ($120\ \mu\text{m}$ beam aperture at 20kV). The smaller write-field ($50\ \mu\text{m}^2$) centered on the graphene contacts is thus nano-patterned following the CAD drawing reported in Figure 2.10. For decreasing lengths, proximity effects must be taken in account. At this regard, a difference of 100nm between the actual channel length and the CAD dimensions is considered. Moreover, lower area doses ($D=240\ \mu\text{C}/\text{cm}^2$) are employed for the rectangular graphene nanogaps in addition to the presence of a thinner resist layer in comparison with the previous fabrication steps. Shortest channels are produced by means of single pixel lines transversally cutting the graphene surface with varying linear doses of $950\text{pC}/\text{cm}$ and $1100\text{pC}/\text{cm}$.

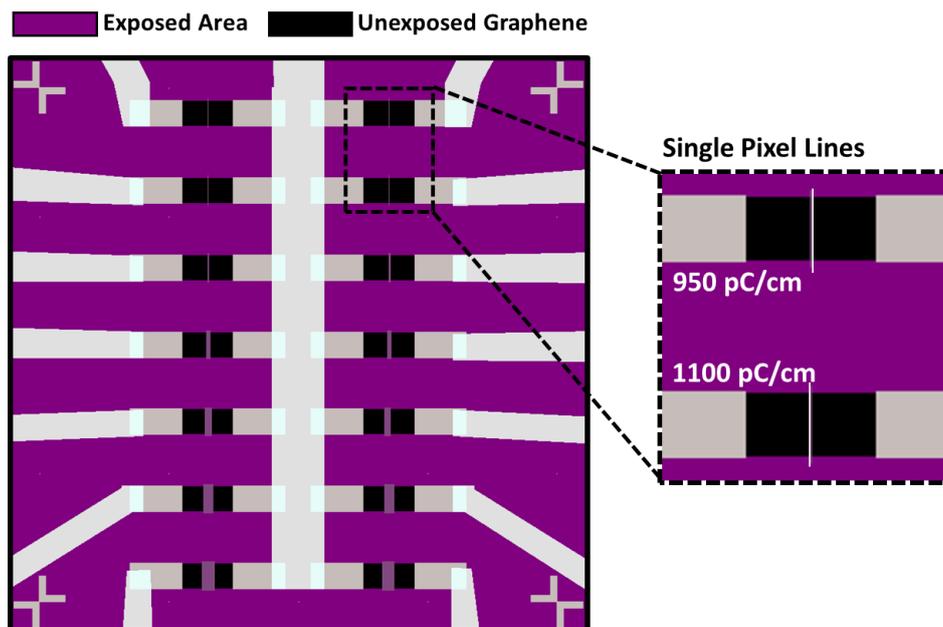


Figure 2.10 CAD drawings of the final nano-patterning for the graphene electrodes. The two shortest channels are made from transversal cutting via single pixel lines with linear dose of 950pC/cm and 1100pC/cm.

The exposed resist is thus removed by development in AR-600-56 for 2 minutes at 20°C and IPA for 30s. Graphene is etched by oxygen plasma RIE using the same process parameters reported for the second fabrication step.

After the fabrication, the sample undergoes a hard cleaning procedure by organic solvents: an acetone bath at room temperature for 1 hour is followed by the immersion of the sample for 4 hours in N-Ethyl Pyrrolidone (NEP) at 65°C and rinsing in IPA. This procedure is observed to be crucial in removing the resist residues, improving the organic thin film morphology and the overall electrical performances of the nano-OFETs. Afterwards, SiO₂ is chemically functionalized by means of HMDS, following the procedure described in Section 2.3.

The resulting layout is showed in Figure 2.11. Each area of 1mm² contains an array of two series of 7 devices sharing a common source electrode. Channel lengths (L) vary between 140nm and 1 μ m while the channel width (W) is fixed at 2 μ m.

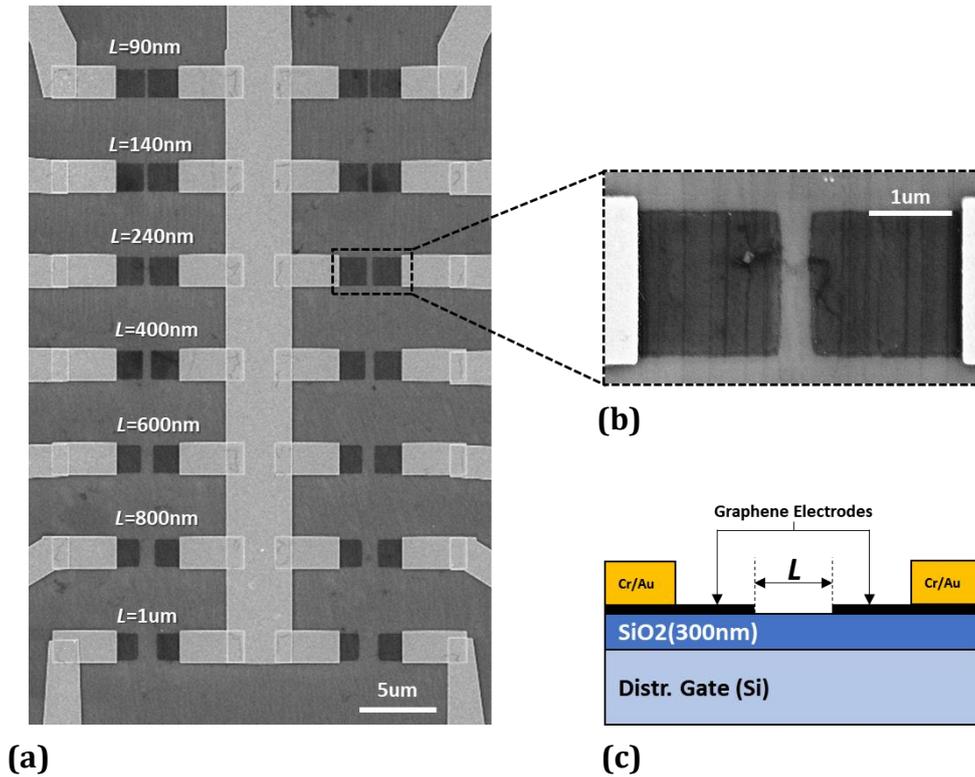


Figure 2.11 SEM image of the bottom-contacts/distributed-bottom-gate layout with graphene electrodes. The array consists of two series of 7 devices sharing a common source electrode. Channel lengths vary between 140nm and 1 µm while the channel width is fixed at 2 µm. (b) SEM image of a single device with $L=240\text{nm}$. (c) Schematic depiction of the lateral section of the graphene-based nanodevices.

2.4.1 Gold-based nano devices

An analogous fabrication procedure has been used for devices based on gold electrodes. In this case, the nanometric channels are outlined directly in the first EBL session. A 220nm thick layer of PMMA 950K is deposited on a SiO₂(300nm)/Si substrate by spin-coating (6000rpm for 60s) followed by a thermal annealing at 180°C for 5 minutes. Proximity effects for channel lengths $L < 600\text{nm}$ are addressed using the layout reported in Figure 2.12c. A nominal dose of 280 µC/cm² (with an aperture of 7.5µm at 20kV) is used for the patterning of the micrometric rectangles defining the contacts. A reduction of 10% in terms of D , in the vicinity of the nano-gaps, counterbalances the possible overexposure of PMMA in the surrounding areas, hindering the two contact fingers from fusing together for L approaching 90 nm. Metal deposition, lift-off and the fabrication procedure for the gold pads and supply lines are exactly the same as for the case of graphene-based devices. The final layout is shown in Figure 2.12a and b. After the fabrication, the sample underwent the same hard cleaning procedure and HMDS functionalization of the graphene-based devices.

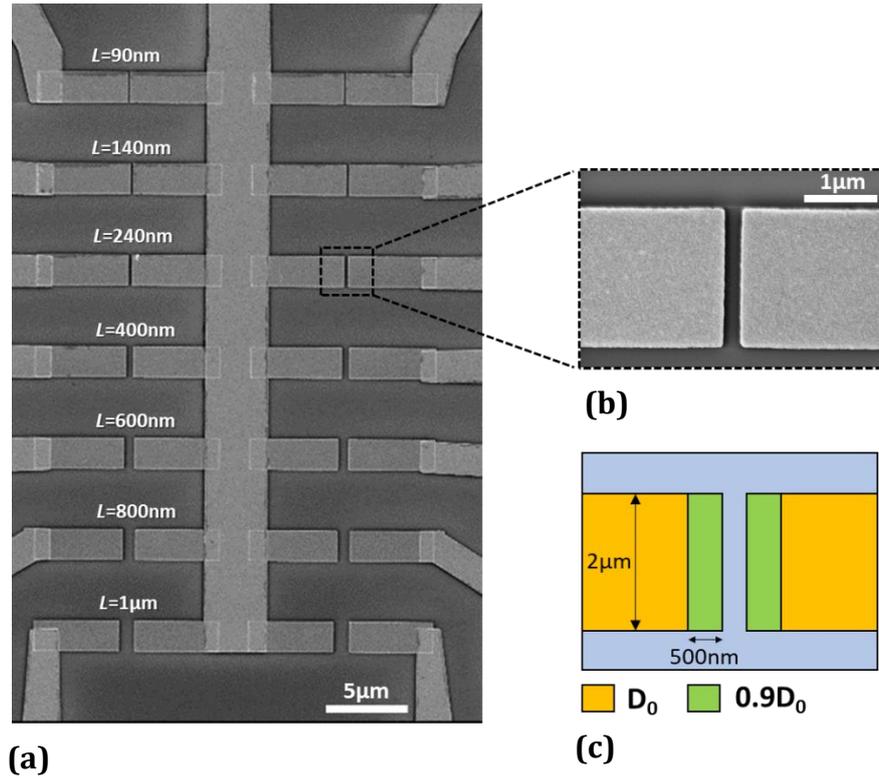


Figure 2.12 (a) SEM image of the bottom-contacts/distributed-bottom-gate layout with gold electrodes. (b) Insight on the $L=240\text{nm}$ gold gap. (c) Proximity effects are limited by a reduction of 10% in terms of the nominal dose D_0 in the vicinity of the gaps.

2.5 BOTTOM-CONTACTS/LOCAL-GATE NANO-OFET LAYOUT

As described in Section 1.5, the miniaturization of lateral dimensions in OFETs must be followed accordingly by the down-scaling of the dielectric buffer layer. At this regard, a bottom-contacts/local-gate layout with an ultra-thin HfO_2 layer as high-k dielectric has been developed. The design is an adaptation of the layout previously employed for the fabrication of single molecular spin transistors based on electro-burned gold nano-junctions [173]. In this work, samples have been fabricated in collaboration with Dr. S. Lumetti (University of Modena and Reggio Emilia, Italy).

A diapason-shaped local gate electrode (3nm/35nm, Ti/Au), characterized by two prongs, is patterned on a SiO_2/Si substrate by means of deep-UV lithography (Figure 2.13a). The prongs have a width of 2µm and 5µm, respectively. The gate electrode is thus insulated by the growth of 8 nm of Hafnium Dioxide (HfO_2) by Atomic Layer Deposition (ALD) which ensures a capacitive coupling of $\sim 2 \mu\text{F}/\text{cm}^2$. The electrical supply lines departing from the center of the device, where the actual nanopatterned graphene electrodes will be located, and the contact pads (Figure 2.13b) are patterned on top of the oxide layer through deep-UV lithography and the deposition of a Ti/Au metallic bilayer (3nm/80nm).

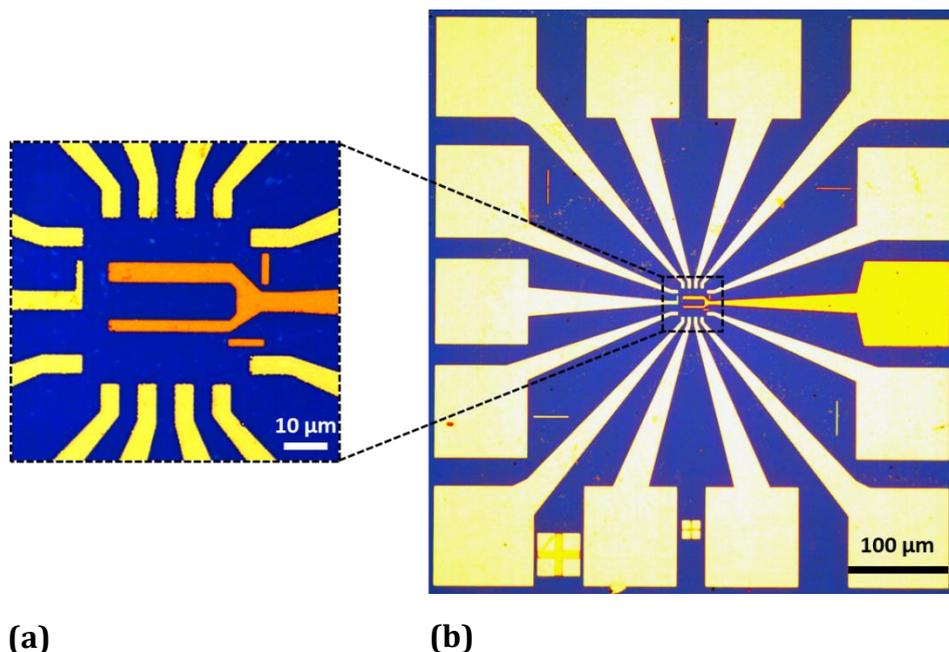


Figure 2.13 (a) Optical micrograph of the diapason-shaped gate electrode for the bottom-contacts/local-bottom-gate layout. The two progs have a width of 2μm and 5μm, respectively. (b) Optical image of the pre-patterned array consisting of 13 micrometric gold pads (100μm×100μm) and as many supply lines.

Further details on the fabrication of the diapason-like gate electrode, the oxide layer and the supply lines can be found in [174]. A large area CVD-Graphene sheet is thus transferred on the pre-patterned substrate. It follows a three-stages EBL process outlining the graphene-based nanometric channels:

- **First fabrication step: graphene contacting.**

A 280 nm thick resist layer of PMMA 950K (All-Resist AR-P-600.79) is spun, at 4000 rpm for 60 s, on a 5x5 mm² sample containing a matrix of 16 pre-patterned arrays of Figure 2.13. Resist layer is dried on the hot plate at 150°C for 15 minutes. Given the lack of dedicated markers, 1000μm² and 100μm² write-fields are aligned by taking advantage of four micrometric pad corners, at the extremities of the pre-fabricated array, and of the metallic interconnections in proximity of the local gate electrode. In view of the observed PMMA sensitivity enhancement discussed in Section 2.1.2, micrometric electrodes are patterned by exposing the resist to an area dose approximately four time lower respect to the previously reported values for the bottom-contacts/distributed-bottom gate layout of Section 2.4: in this case, a value of 75 μC/cm² (7.5 μm aperture at 20kV) has been employed. Enhanced sensitivity is exploited by the development of exposed areas in amyl acetate-based developer AR-600-54/6 for 1 minute at 20°C then rinsed in IPA for 30 s. Electrodes are thus fabricated by thermal evaporation of 3nm/30nm of Cr/Au followed by the lift-off in acetone bath at 65°C.

- **Second fabrication step: graphene etching**

In the second EBL session, a 220 nm thick layer is deposited at 6000 rpm for 60 s followed by a thermal annealing at 180°C for 5 min. The entire array area of 1mm² is exposed with $D= 80 \mu\text{C}/\text{cm}^2$. The nano-channels are patterned in an aligned 100 μm^2 write-field by means of an area dose of 90 $\mu\text{C}/\text{cm}^2$. The two smallest channels are outlined by a single pixel line with a linear dose of 1000pC/cm whereas two devices, out of a total of 8 for each array, are left uncut in order to evaluate the electronic transport characteristics of graphene in GFET configuration (Figure 2.14a). The sample is developed in AR-600-54/6 for 1 minute at 20°C. The exposed area is thus etched by an oxygen plasma RIE following the same recipe as Section 2.4. It is worth noting that proximity effects appear to be largely suppressed since the use of lower area doses: in this case, the CAD design and actual pattern dimensions showed a 1:1 matching within 10nm.

- **Third fabrication step: PMMA sinkholes.**

The last fabrication step is aimed to the creation of PMMA sinkholes in correspondence of the nanometric channel areas. This in order to insulate the external gold interconnections from the organic thin film, that will cover the whole sample, hindering in such a way the contribution from fringing currents in the final OFETs (as it will be discussed in the following sections). Before the EBL session, the sample undergoes the same hard-cleaning procedure and HMDS deposition from vapor precursor, as described in the previous section. A 280nm thick PMMA layer is then deposited on the sample (4000rpm for 60s) and cured on the hot plate at 115°C for 15 minutes. Eight micrometric sinkholes are patterned in the central area with an area dose $D=105 \mu\text{C}/\text{cm}^2$ then developed in AR-600-54/6 for 1 minute at 20°C (Figure 2.14b)

The final layout is schematically depicted in Figure 2.14c. Each array contains 8 devices sharing a common source electrode. Three different channel lengths $L=200 \text{ nm}$, 550 nm, 750 nm are considered while the channel width W is fixed at 4 μm .

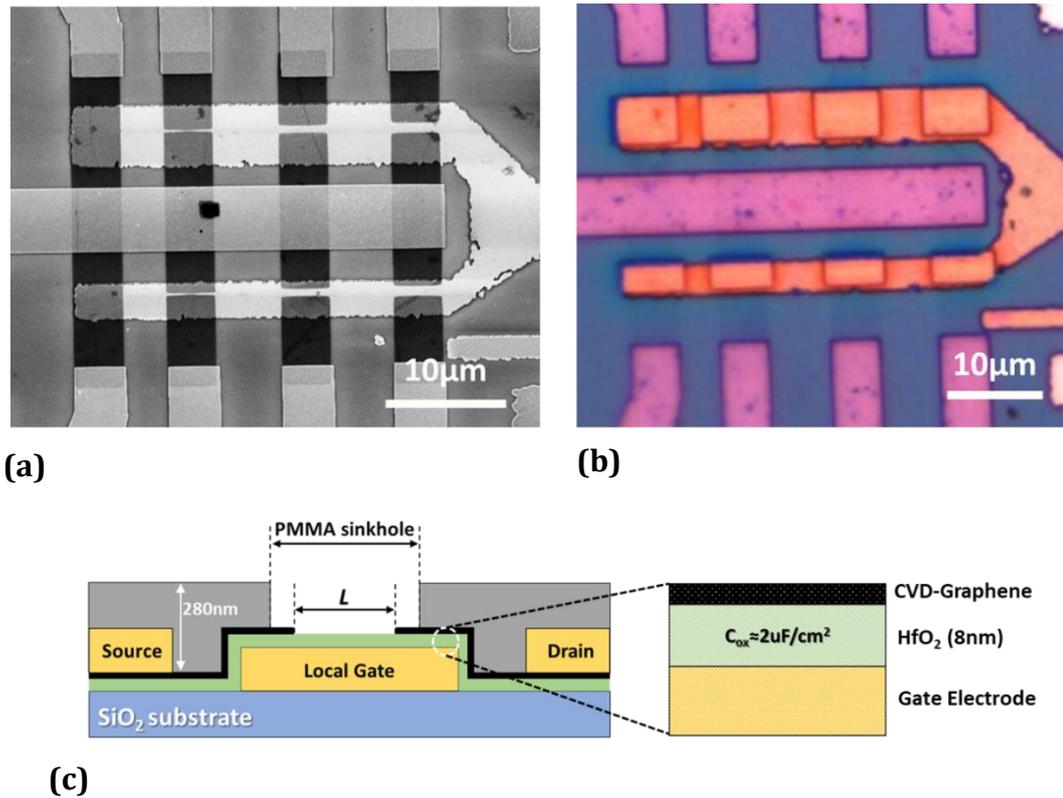


Figure 2.14 (a) SEM image of the nano-patterned graphene electrodes in the bottom-contacts/local-bottom-gate configuration. The diapason-shaped gate electrode has two prongs, 2 μm and 5 μm wide. The dielectric layer is an 8nm thick HfO_2 buffer layer grown by Atomic Layer Deposition. (b) Optical image of the central area after the third fabrication step. It is possible to observe the presence of sinkholes, in the 280nm thick PMMA layer, in correspondence of the nano-gaps. (c) Schematic depiction of the layout under investigation.

2.6 MICROMETRIC BOTTOM-CONTACTS/DISTRIBUTED-BOTTOM-GATE INTERDIGITATED ARCHITECTURES

Micrometric test-patterns have been developed in order to directly compare the electrical characteristics of graphene-based OFETs with the state-of-the-art devices reported in literature and to perform a direct estimation of the contact resistances at the Organic/Graphene interface by Kelvin probe microscopy. At this regard two different layouts have been considered. The first micrometric test-pattern consists of a comb-like interdigitated architecture characterized by a channel length L of 10 μm (Figure 2.15a-b). Samples have been fabricated starting from commercially available substrates ($\text{Si}/\text{SiO}_2(300\text{nm})/\text{CVD-Graphene}$) provided by Graphenea, Inc. [175], using the process parameters of the first two steps reported in Section 2.5. The devices have a channel width of 3 mm resulting in a W/L ratio of 300. In a second architecture (Figure 2.15b-c), an asymmetrical layout consisting of one metallic (Cr/Au , 3nm/40nm) and one graphene electrode, with analogous L and W , has been considered.

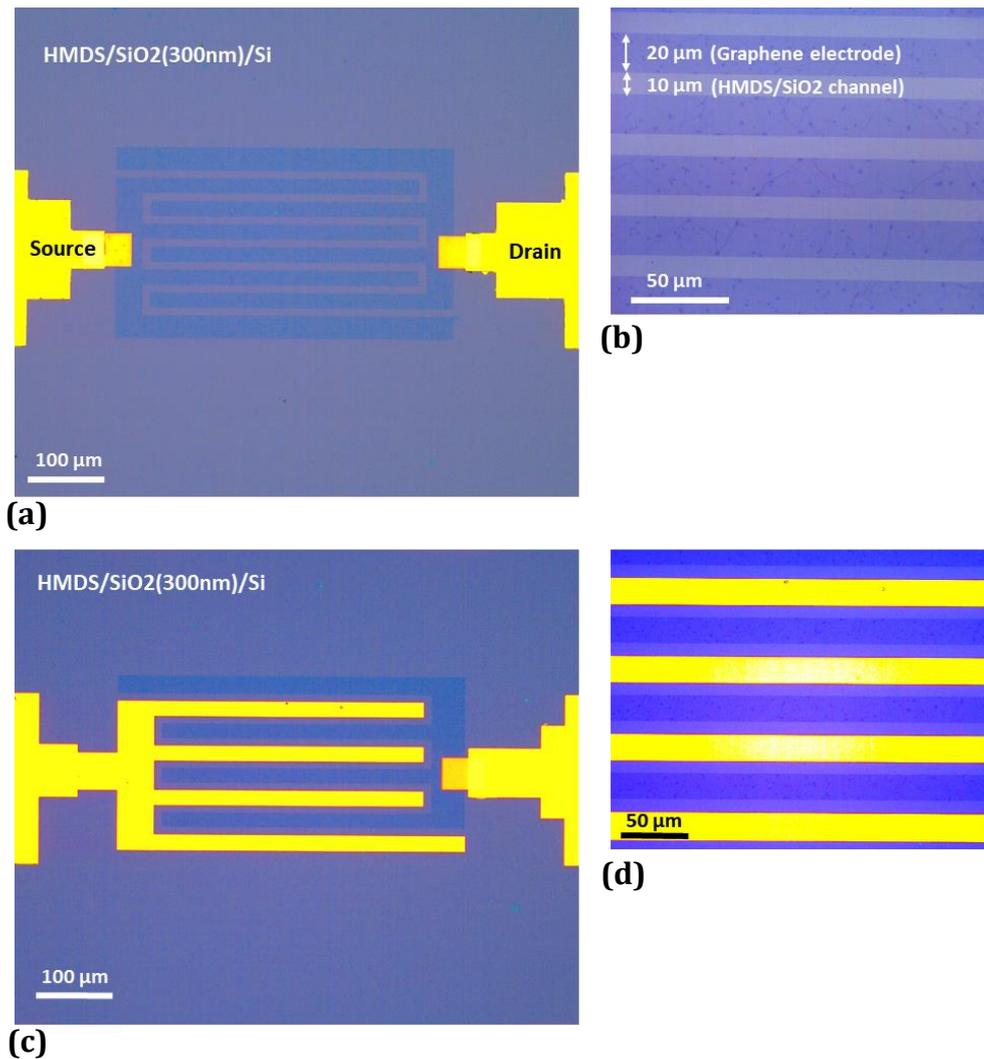


Figure 2.15 Optical micrographs of the bottom-contacts/distributed-bottom-gate interdigitated micrometric layouts. (a) and (b) shows the architecture characterized by two comb-like graphene electrodes with $L=10\ \mu\text{m}$ and $W=3\ \text{mm}$. (c) and (d) Asymmetrical layout with a metallic electrode (Cr/Au, 3nm/40nm) and a graphene electrode. The channel length and width are the same as the all-graphene architecture.

Organic devices based on the latter architecture are still under analysis at the time this work is in preparation. Further discussion on the results is thus missing throughout the thesis.

2.7 ORGANIC THIN FILM GROWTH

After the realization of the nano and micro patterned graphene electrodes and the deposition of the metallic contact arrays, described in the last sections, the fabrication procedure is terminated by the deposition of thermally evaporated organic thin film by Organic Molecular Beam Deposition (OMBD) technique. In this section, a brief digression on the basic theoretical insights of organic thin film growth as well as details on the employed experimental set-up will be given.

Theoretical considerations of organic thin film growth are traditionally exported from inorganic crystal growth even if several exceptions and assumptions are clearly needed. In inorganic Molecular Beam Epitaxy (MBE), the substrate is a clean single crystal and the adsorbates are usually single atoms or dimers that chemisorb on the surface from vapor state. Atoms are assumed to have an isotropic shape (sphere) so that the orientation of the adatom relative to the substrate or to other atoms is irrelevant for the strength of the interaction. Inorganic crystal growth relies on the rather strong covalent or ionic bonds of the adsorbates to the substrate. For the same reason, lattice matching is usually a requisite for crystal growth, because it avoids stress buildup.

In an ideally atomistic framework, the precursor species are deposited onto a perfect substrate surface with a deposition flux F , from gas state. The relevant processes during the process are schematically depicted in Figure 2.16. Once atoms are on the surface as adatoms, they can diffuse with a diffusion constant D or reevaporate without contributing to the film growth. Adatoms can nucleate to form a dimer or attach to existing islands. Once adatoms are attached to an island, they can detach and diffuse along the island edge, rearranging on the same layer or trespassing the layer boundaries by interlayer diffusion.

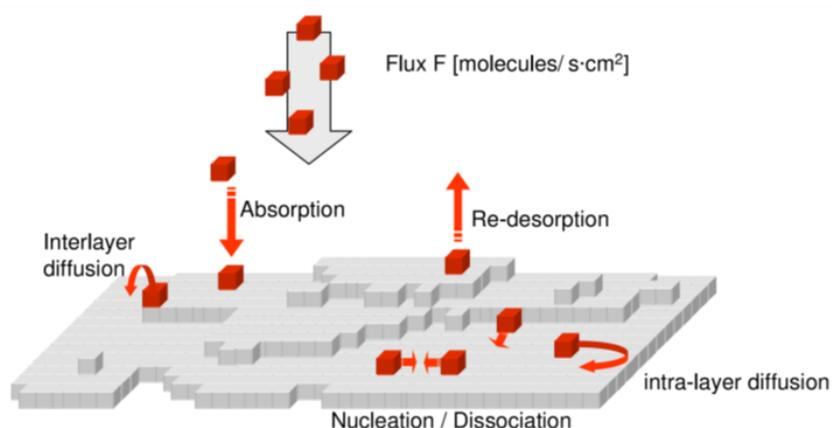


Figure 2.16 Atomistic processes in both organic and inorganic thin film deposition. From [167].

The general considerations above apply both to organic and inorganic materials, but several aspects specific to organic materials can lead to distinctively different growth behavior. For example, the vibrational degrees of freedom of molecules can impact the interaction with the substrate and also the thermalization upon adsorption on the surface by conversion of the translational energy into internal vibrational energy [176]. Conformational degrees of freedom may trigger change molecular assembly within the film, for example by bending to accommodate stress [177]. Furthermore, molecular orientational configurations can give rise to tilt domains and thereby an additional source of disorder that may induce ‘lying down’ and ‘standing up’ structures, influencing the final thin film morphology [178].

In addition to these considerations, a major contribution to the organic growth is determined by contributions to the surface free energy given by the substrate (γ_{sub}), the deposited film (γ_f) and the interplay between the two at the interface (γ_i). In general, one can distinguish three growth scenarios: layer-by-layer growth (Frank–van der Merwe),

layer-plus-islands (Stranski–Krastanov), and island (Volmer–Weber) [179]. The interplay between the surface energies γ_{sub} , γ_f , and γ_i are related to these growth modes (Figure 2.17) that can be wisely controlled by the use of self-assembled monolayers.

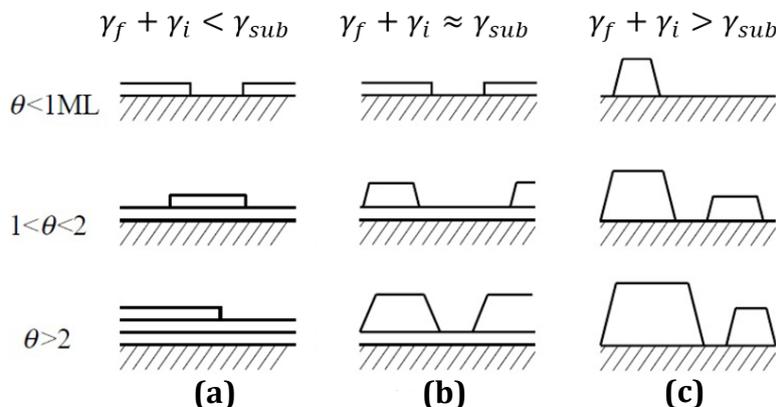


Figure 2.17 Schematic representation of the three growth modes, as a function of the coverage θ in ML (Mono Layers): (a) layer-by-layer, or Frank–van der Merwe growth; b) layer-plus-island, or Stranski–Krastanov growth; c) island, or Volmer–Weber growth. Adapted from [179].

In addition to the interface thermodynamics, polycrystalline order in organic thin film growth relies experimentally also on the interplay between the substrate temperature and on the deposition rate. Perylene diimides appears to be particularly influenced by deposition parameters with huge impacts on the overall electrical performances of the final devices. In particular, PDIF-CN2 based organic transistors exhibit dramatic Ion/Ioff and μ enhancements with increasing substrate temperature: field-effect-mobility variations of five order of magnitude, between substrates kept at room temperature and at 100°C, are typically observed [32]. More recently, it has been reported that thermal energy can be reliably replaced by high translational energy in PDIF-CN2 thin films deposited by Supersonic Molecular Beam Deposition technique (SuMBD) on substrates kept at room temperature [180]. In this case, post-deposition spontaneous wetting phenomena induce a transition from an initial Volmer-Weber growth, characterized by the presence of three-dimensional nanopillars, to a final terraced layer-plus-island morphology (Figure 2.18a-c). The observed time scales of the transition, from few hours to months, as well as the lateral dimensions and density of the nanopillars are related to the deposition rate and have been theoretically investigated by invoking non-linear stochastic models [181]. As shown in Figure 2.18d and e, field-effect-mobility in micrometric channel OFETs is observed to increase according with the spontaneous molecular reassembly, with final values comparable to those obtained in state-of-the-art devices fabricated by standard OMBD and with higher substrate temperatures ($\mu_{max} \approx 10^{-1} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ with $T_{sub} = 100^\circ \text{C}$).

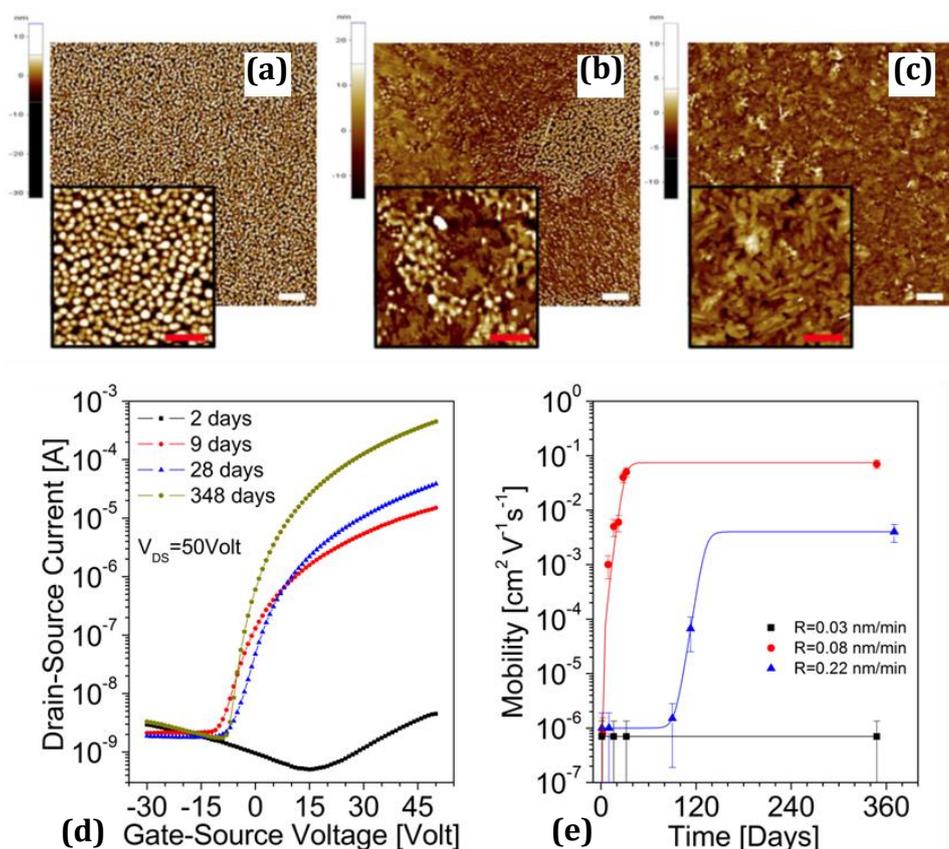


Figure 2.18 AFM topographies of PDIF-CN2 thin films deposited via Supersonic Molecular Beam Deposition (SuMBD) with kinetic energy of 17eV per molecule on substrates kept at room temperature: the as-grown surface after few hours from the molecular beam switch off (a), a mixed surface (b) and a terraced surface after 1 year (c) are shown. The white markers are of size 1 μm . In the insets, images of $2 \times 2 \mu\text{m}^2$ zoom of the images (a-c) are shown. The red markers are of 0.5 μm . Adapted from [181]. (d) Semi-log plot of the transfer curves measured in the saturation regime for OFETs based on PDIF-CN2 thin films (20nm) deposited via SuMBD. (e) Mobility time dependence extracted from the transfer curves in the saturation regime for different deposition rates. Adapted from [180].

2.7.1 Perylene diimides thin films by Organic Molecular Beam Deposition

Perylene diimides thin films, employed throughout this work, are fabricated by means of the home-made OMBD set-up shown in Figure 2.19. The system consists of two stages comprising a UHV deposition chamber and a load-lock section. The molecular beam sources are individuated by two DN35CF-UHV Knudsen cells (Organic Spintronics, S.r.l.) equipped with quartz crucibles in which PDI8-CN2 and PDIF-CN2 are placed in the form of powder. The cells are heated via Joule effect while a PID automatically controls the sublimation temperature. The deposition rate (expressed in nm/min) is monitored via an IL150 Quartz Crystal Growth Rate Monitor by Intellemetrics. A set of three heating bands envelopes the entire deposition chamber controlling its temperature (T_{ch}) via a PID driven feedback loop. By the calibration of the internal chamber temperature and that of the heating elements, the selected substrate temperature T_{sub} is indirectly set when the whole system is at the thermal equilibrium. This configuration allows maximum achievable T_{sub} values of about 150°C.

The deposition procedure is quite straightforward. Substrate are secured into the load-

lock chamber on a copper sample-holder. Once the equilibrium is obtained between the load-lock pressure and the UHV main chamber kept at high temperature, substrates are thus inserted in the deposition stage by means of a magnetic manipulator, facing up towards the top of the chamber. The system is let thermalize overnight in order for T_{sub} to equal the surrounding T_{ch} . The Knudsen cell is then heated up to temperatures ranging from 220°C and 260°C, depending on the molecular precursor, and the corresponding deposition rate is measured via the quartz microbalance. Once the designated deposition rate R is obtained, the sample holder is turned over in order for the substrates to orthogonally intercept the organic beam. Typical deposition pressures range between $3\text{-}7 \times 10^{-7}$ mbar depending on the deposition rate. The deposition stops when the nominal film thickness is reached (typically 25nm). Sample are then retrieved back in the load-lock stage and let cool down for at least one hour, in dynamic vacuum, after which the chamber is vented with N_2 gas. This in order limit the exposition of the freshly deposited organic films to ambient contaminants.

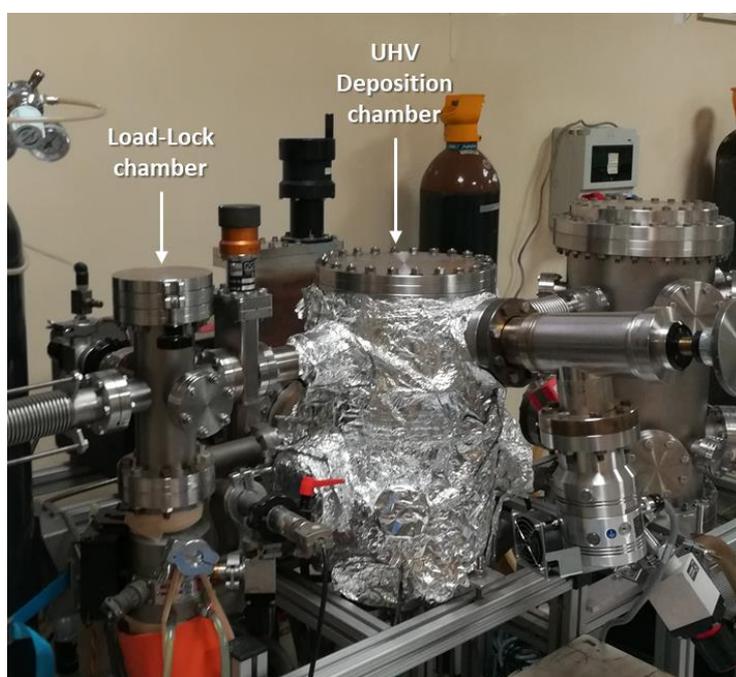


Figure 2.19 OMBD experimental set-up for the deposition of organic thin films situated at the department of Physics of the university of Naples “FedericoII”.

Optimized deposition parameters, for PDIF-CN2 and PDI8-CN2, have been found by testing both the morphological properties and electrical performances of organic thin films (25nm) deposited on numerous micrometric test-patterns, by both varying T_{sub} and R , based on HMDS-treated, 200nm thick thermal SiO_2 ($W=1.1\text{cm}$, $L=20\mu\text{m}$ with interdigitated gold-based architecture similar to that reported in section 2.6). An optimized deposition rate value $R=0.3\text{nm}/\text{min}$ and $T_{\text{sub}}=104^\circ\text{C}$ for PDIF-CN2 results in excellent transport properties with $\mu_{\text{sat}} = 4 \times 10^{-1} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. State-of-the-art electrical performances, with field effect mobility in saturation regime $\mu_{\text{sat}} \approx 5 \times 10^{-2} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, are obtained for $0.5\text{nm}/\text{min} < R < 0.7 \text{nm}/\text{min}$ and $T_{\text{sub}}=95^\circ\text{C}$ for PDI8-CN2 thin films.

3 GRAPHENE ELECTRODES IN NANOMETRIC ARCHITECTURES

In this chapter, the experimental results for the nanometric n-type OFETs fabricated following the procedure of section 2.4 and 2.5 will be reported. In the first part of the chapter, a preliminary investigation will be focused on the comparison between the use of standard gold and CVD-graphene as electrodes in nanoarchitecture based on PDIF-CN2 as n-type organic semiconductor. The quality of the organic thin films has been tested by Non-Contact Atomic Force Microscopy in order to compare the morphologies with those obtained in standard micrometric test-pattern devices with gold electrodes and state-of-the-art performances. DC electrical characterization has been performed on an average of 180 devices for each substrate. In the following sections, the results have been rationalized considering the most commonly observed electrical behavior among the entire dataset. An average mitigation of short-channel effect will be demonstrated. The encouraging results obtained have prompted the development of a second optimized device layout, comprising ultra-thin hafnium dioxide as dielectric in a local-bottom-gate architecture. The second part of the chapter is thus devoted to the experimental results obtained in this case. Local gate electrodes and high capacitive coupling appear to be well suited for the characterization of graphene electrodes in dynamic regime by impedance spectroscopy, from which the quantum contribution of graphene to the total capacitance of the nano devices will be addressed. Experimental results will be discussed taking into account the morphological and electronic characteristics of graphene electrodes which have been investigated both by electrical characterization in GFET configuration and by a direct estimation of their work-function by SKPFM.

3.1 PDIF-CN2 BASED BOTTOM-CONTACTS/DISTRIBUTED-BOTTOM-GATE OFETs

For both graphene-based and gold-based nanoarchitectures of section 2.4, a 25nm thick PDIF-CN2 thin film has been deposited via OMBD (section 2.7.1), on a substrate pair kept at 104°C. A deposition rate of about 0.3 nm/min in high vacuum conditions ($P_{dep} \approx 5 \times 10^{-7} \text{ mbar}$) has been employed obtaining the final layouts depicted in Figure 3.1.

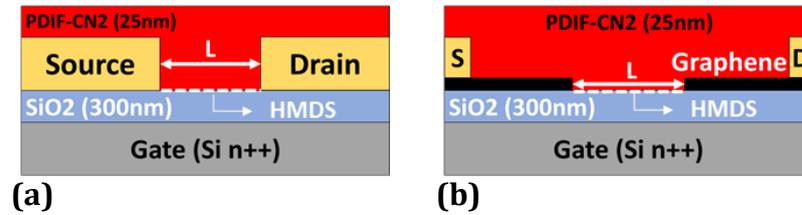


Figure 3.1 Schematic depiction of the coplanar bottom-contacts/distributed-bottom-gate layouts based on evaporated thin films (25nm) of PDIF-CN2 with nanometric channels and (a) gold-based or (b) graphene-based electrodes.

Over an average of 180 measured devices for each architecture, more than 80% of the entire dataset showed a proper transistor operation. For shortest devices ($L=90\text{nm}$) and particularly for graphene-based nanoarchitectures, scarcely reproducible results have been obtained. In this case, the fabrication step through EBL appears to be critical due to proximity effects: unwanted fused source/drain graphene electrodes are observed in the vast majority of the samples. For these reasons, the analysis for the nanometric transistors with $L=90\text{nm}$ has been neglected in the following discussion.

3.1.1 Morphological characterization

Morphological characterization of the deposited organic thin films has been performed by means of a Park Xe-100 AFM equipped with a $50\mu\text{m} \times 50\mu\text{m}$ x-y scanner stage, in Non-Contact configuration.

The commonly observed morphologies for both graphene-based and gold-based devices are reported in Figure 3.2, for three out of a total of six different channel lengths L . From AFM analysis, the organic thin films appear to cover uniformly the nanometric gap dividing the electrodes. The samples manifest a typical Stransky-Krastanov growth characterized by the mixed presence of homogenous molecular layers and three-dimensional island formations inside the active channel. The step height of the molecular terraces is estimated in about 2nm, in good agreement with crystallographic d-spacing reported in literature and an overall thin film morphology similar to state-of-the-art devices is observed [35]. Despite that, a direct comparison of the images indicates higher granularity and a smaller average island size in graphene-based architectures (Figure 3.2(a)-(c)). This reflects on the root-mean-square roughness (σ_{rms}) determined in correspondence of the active channels: values of 1.4 nm are extracted for graphene-based

layouts, whereas values of about 1.2 nm are observed in the gold case. In both the geometries, the presence of electrodes affects clearly the organic thin film morphology at a different extent. Graphene-architectures may be considered as truly coplanar structure in the sense that graphene thickness is neglected by the molecular ordering during the thin film growth. Organic molecules assemble in a tilted upright position in which the conduction plane is orthogonal to the graphene sheet. Conversely, in the case of gold-based nano devices, contacts and the organic thin film share approximately the same thickness (33nm and 25nm respectively). In such a way, it is possible to assume that gold has a not negligible three-dimensional extension with respects to the 25nm thick organic thin film. The interface is thus dominated by an abrupt discontinuity between the organic solid and the electrode edges which, in this case, are in registry with the molecular transport plane in the active channel.

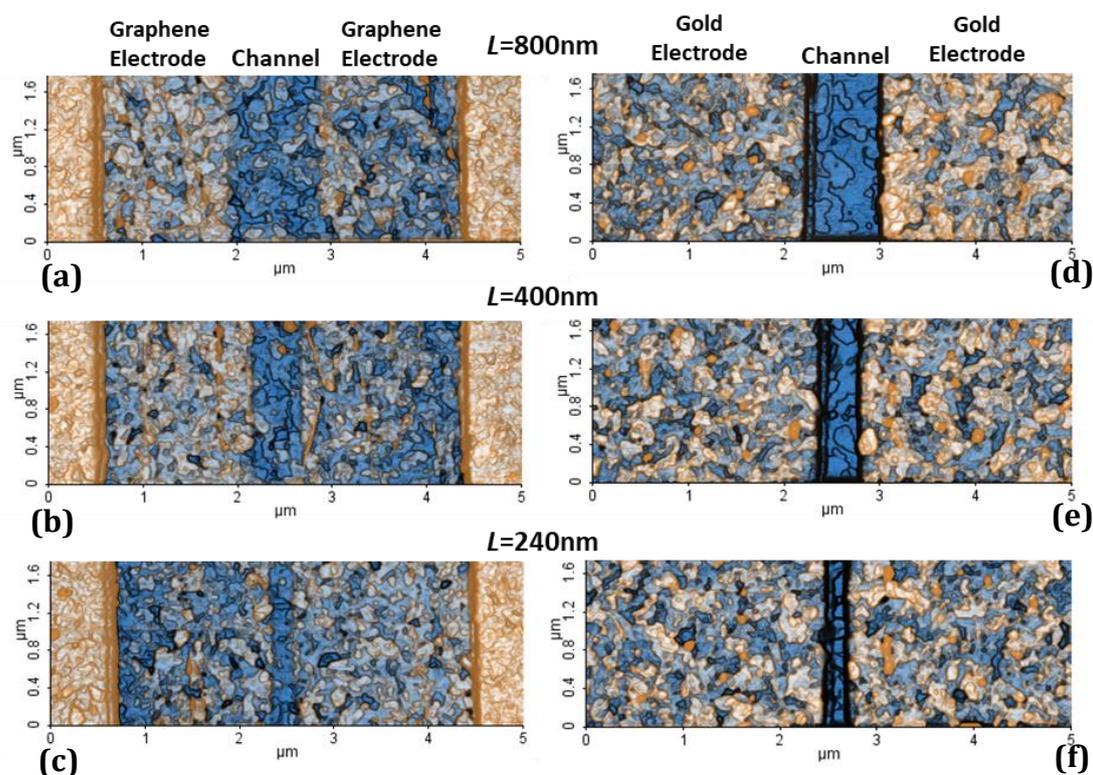


Figure 3.2 Enhanced color NC-AFM topographies of the graphene-based transistor (a)-(c) and gold-based devices (d)-(f) with $L=\{240\text{nm}, 400\text{nm}, 800\text{nm}\}$.

3.1.2 DC electrical Characterization

The electrical characterization of the devices has been carried out inside a Janis ST500-Family Cryogenic Probe Station (Figure 3.3a). The probe station is a four-armed apparatus: three are typically employed for the electrical characterization while an additional arm is equipped with an optical fiber for local optoelectronic measurements. It is able to perform electrical measurements in cryogenic conditions, with temperatures as low as 77 K, and in a high vacuum environment. Each arm is provided with a moving probe tip whose translational degrees of freedom are explored by means of independent x-y-z

sliders; the fine tuning along the y and z axis is provided by micrometric knobs with typical resolution of 5 μm .

Transfer (I_{ds} - V_{gs}) and output (I_{ds} - V_{ds}) characteristics have been acquired by means of a dual-channel Keithley-2612A System SourceMeter®. A schematic depiction of the experimental set-up is reported in *Figure 3.3b*. For each channel of the multimeter, a voltage value is set and the current is acquired. The first channel (CH-A) is related to the gate current-voltage measurements, i.e. for each gate voltage V_{gs} the leakage current I_{gs} is measured. The second channel (CH-B) controls the current-voltage measurements on the drain electrode, namely the drain-source current I_{ds} for a fixed V_{ds} . The source terminal acts as shared reference ground level for both the channels. The measurement routines are remotely controlled by custom-designed LabView™ interfaces. In this section, all the electrical characterizations reported have been conducted in a high vacuum environment ($P < 10^{-5}$ mbar) and in dark conditions.

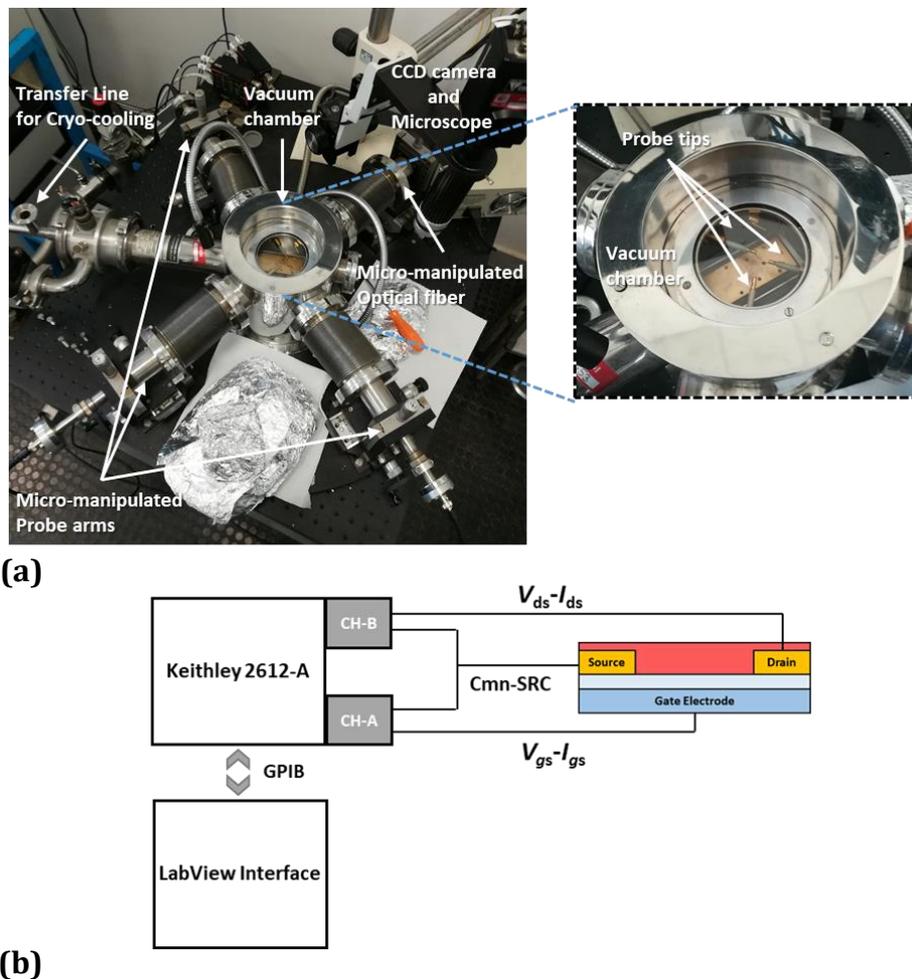


Figure 3.3 (a) External view of the Janis ST500-Family Cryogenic Probe Station. (b) Schematic depiction of the experimental set-up for the DC electrical characterization of the OFETs.

3.1.3 Gold electrodes Vs Graphene electrodes in nanometric architectures

Typical output curves of nano devices with graphene electrodes are shown in Figure 3.4. The drain-source current (I_{ds}) appears to respond linearly to the drain-source bias (V_{ds}) in the range $0 V < V_{ds} < 20 V$. An obvious current modulation is observed in the case of graphene electrodes for increasing gate-source bias ($-80V < V_{gs} < +40V$), independently on the channel length L . Increasing L from 140nm to 1000nm, the maximum I_{ds} values are observed to decrease accordingly. A comparative analysis with the output curves for gold electrodes reported in Figure 3.5 shows substantial differences between the two systems. In the case of gold electrodes, a supra-linear behavior is evident in the same V_{ds} interval, while the gate-source current-modulation deteriorates for L approaching the minimum value of 140 nm where the contribution over the transport due punch-through current starts to dominate. It should be pointed out that in both architectures current saturation is not achieved for any L due to the relatively thick gate dielectric (300 nm) and its effective charge accumulation. In this configuration, indeed, a capacitance per area of 17.25 nF/cm^2 is present at the dielectric interface. Moreover, despite PDIF-CN2 organic thin films show similar morphologies inside the active channel, maximum I_{ds} values was observed to differ by a factor of 5, indicating a major contribution of the contact resistances for the case of graphene electrodes.

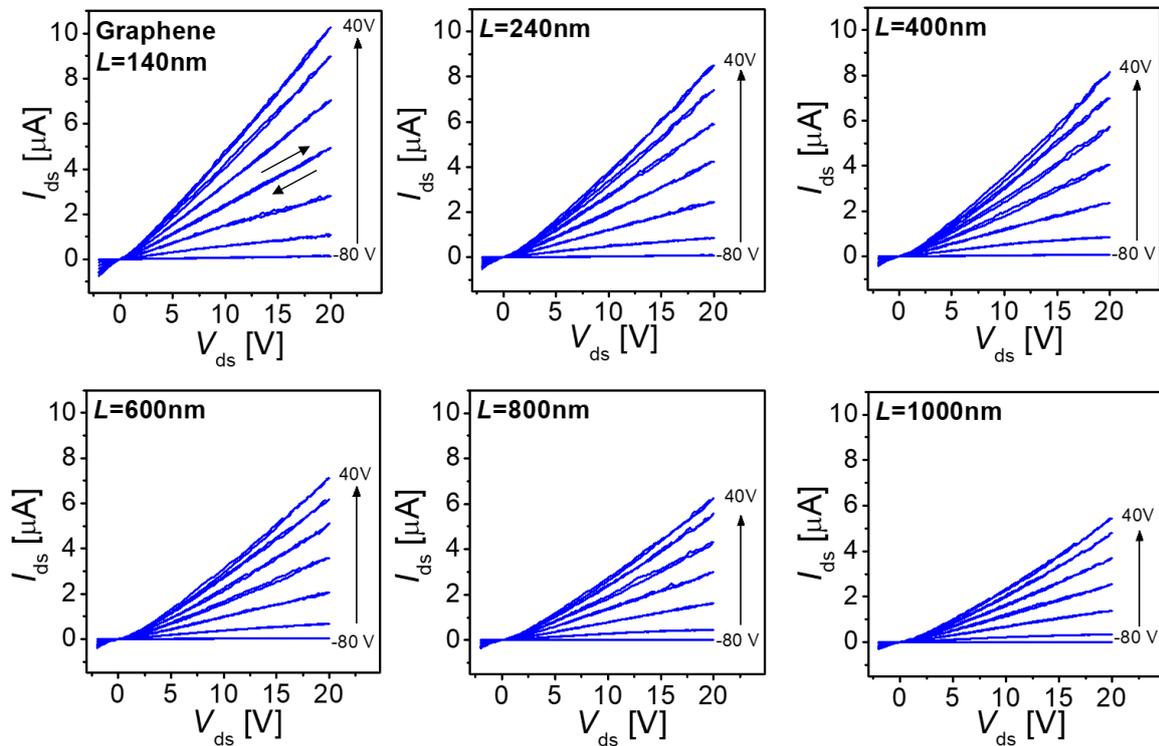


Figure 3.4 Output curves obtained in vacuum for different channel lengths L for the graphene-based devices ($-80V < V_{gs} < +40V$ with $+20V$ steps). The black arrows indicate the sweeping direction of the drain-source bias.

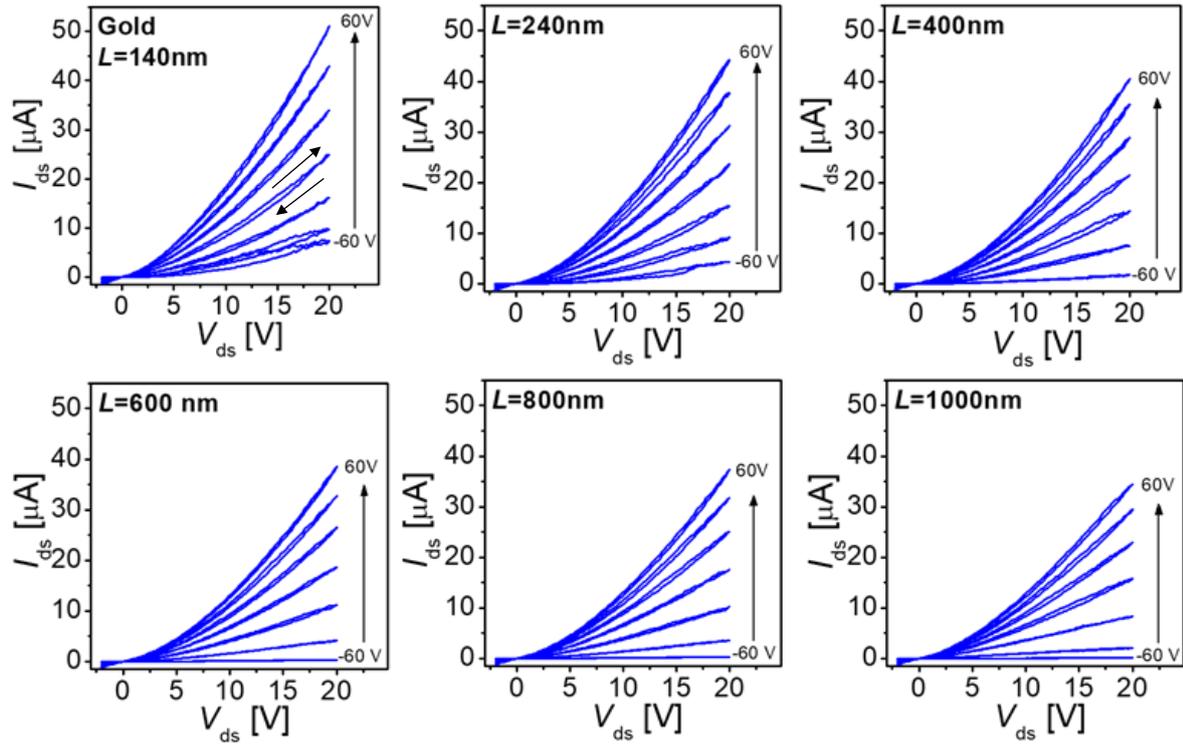


Figure 3.5 Output curves obtained in vacuum for different channel lengths L for nano OFETs with gold electrodes ($-60V \leq V_{gs} \leq +60V$ with $+20V$ steps). The black arrows indicate the sweeping direction of the drain-source bias.

Output characteristics can be further analyzed considering the ln-ln scale in order to investigate in deeper details the power-law characteristics $I_{ds} \approx V_{ds}^n$ in both the architectures (Figure 3.6a). For graphene-based transistors, I_{ds} has a quasi-linear dependence on the entire drain-source interval with $n \approx 1.2$ even in the case of the shortest channel ($L=140$ nm). On the other hand, the power law for the gold-based devices with a comparable channel length appears to be characterized by two distinct regimes, depending on the applied bias, with a slope value $n \approx 1.5$ diverging from the linearity for $V_{ds} > 2$ V. This is a typical signature from a SCLC contribution that becomes more evident for decreasing V_{gs} , as can be seen in Figure 3.6b. In particular, the exponent n for $V_{ds} > 2V$ approaches values exceeding 2 for gate-source bias near $-60V$ where punch-through currents start to dominate over the charge carrier transport. For $V_{ds} < 2V$, gold-based devices show slope values similar to those obtained for graphene-based transistors, with n asymptotically approaching 1.2 for increasing V_{gs} biases.

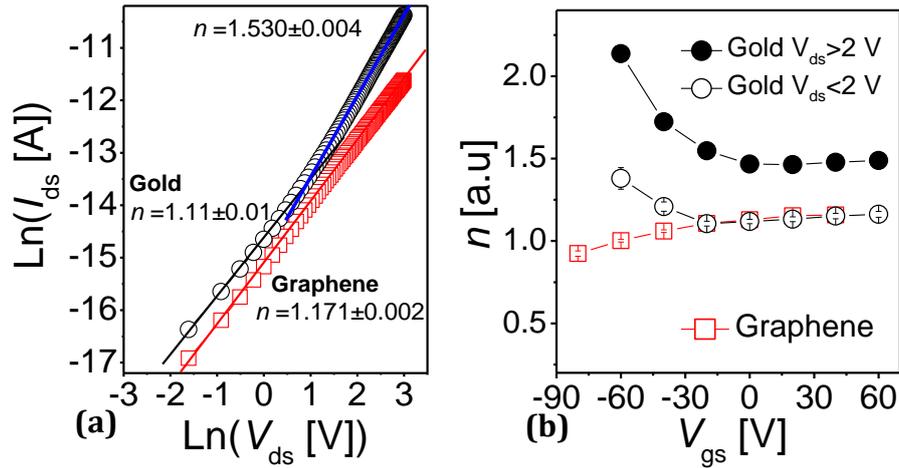


Figure 3.6 (a) Ln-Ln plot of the output curves for $V_{gs}=20V$ of the graphene-based device (red squares) and for the gold-based transistor (black circles) with $L=140$ nm. The n values indicate the slope of the Ln-Ln curves extracted from the linear best fit. (b) Slopes n extracted as a function of the applied gate-source bias for $L=140$ nm in both the architectures. For gold electrode devices, the responses for $V_{ds} < 2V$ (empty circles) and $V_{ds} > 2V$ (filled circles) are reported.

The advantages in terms of the overall performances of devices with graphene electrodes can be further inferred comparing the transfer curves for a fixed drain-source bias $V_{ds}=+5$ reported in Figure 3.7a and b. In particular, punch-through currents due to drain-induced barrier lowering are evidently suppressed in graphene-based devices. Indeed, in the case of gold-electrode devices, approaching V_{gs} values near to the onset voltages (V_{on}), off-state currents (I_{off}) for a fixed V_{ds} bias deteriorate progressively for decreasing L : increasing I_{off} values from $\approx 10^{-9}A$ for $L=1000nm$ to $\approx 10^{-6}A$ for channel lengths approaching 140 nm are observed. Conversely, off-state currents in graphene-based devices appear to sustain the shrinking of the channel length down to $L = 140$ nm with values fixed in the nA scale. Different behaviors in terms of off-state currents are even more evident for increasing drain-source biases for $L=140nm$, as can be observed in Figure 3.7c and d. Drain induced barrier lowering is clearly mitigated in graphene-based architectures with off state current again pinned in the nA scale for V_{ds} as high as 10V.

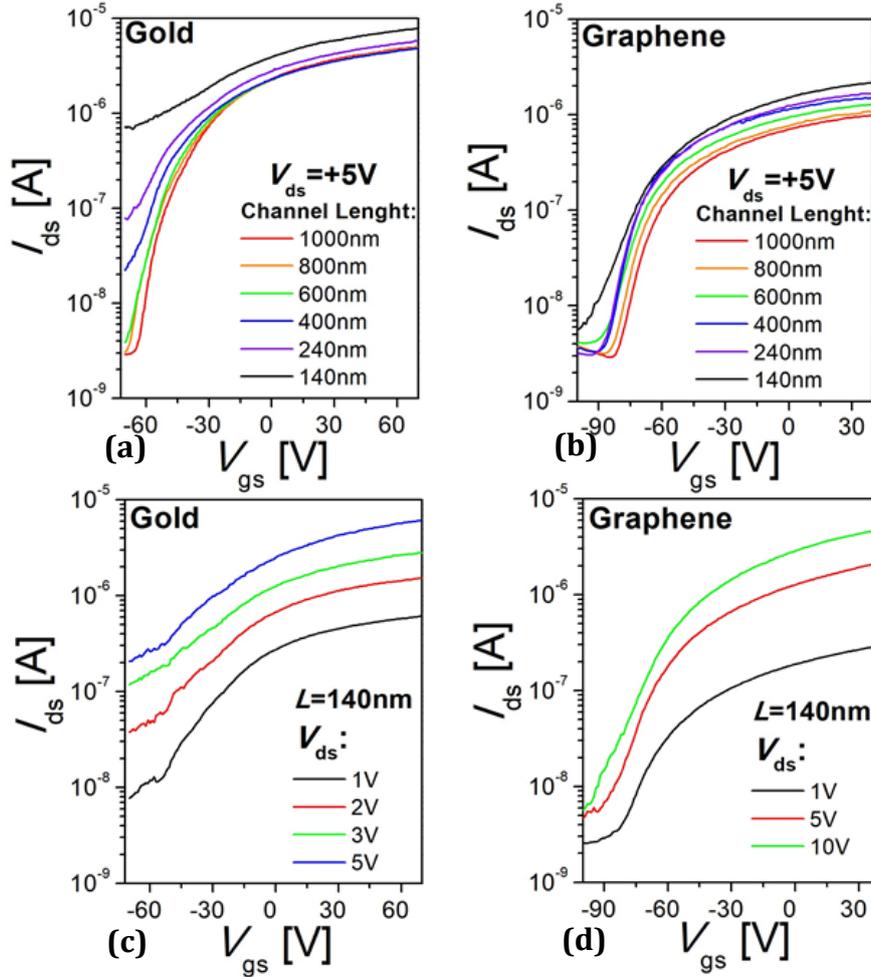


Figure 3.7 Transfer curves acquired in vacuum for a fixed drain source bias ($V_{ds}=5V$), at different channel lengths for (a) gold and (b) graphene-based devices. (c) Transfer curves for $+1V < V_{ds} < +5V$ in gold-based devices with a fixed channel length $L=140nm$. (d) Transfer curves in a graphene-based device with $L=140nm$ and V_{ds} ranging between 1V and 10V.

As a common feature, highly negative onset voltages (V_{on}) are observed with values of about -60 V in the case of gold electrodes and -80 V for graphene electrodes. Large negative threshold values are commonly observed for perylene diimides and especially for PDIF-CN2 when deposited on “bare” (i.e. not passivated) SiO₂ substrates, where the presence of charge traps also induces hysteresis in the current characteristics and affects negatively the overall morphology of the organic thin film. These issues are usually overcome by the HMDS functionalization [182]. Despite that, the effectiveness of the functionalization procedure, in the device under analysis, is confirmed by the ordered polycrystalline morphology of the organic thin film and the presence of limited hysteresis phenomena in the electrical characteristics. Therefore, it is possible to ascribe the highly negative on-set voltages to a partially un-passivated surface, where, likely, a fixed parasitic surface charge density at the SiO₂/HMDS interface is still present [183]. Importantly, the negative threshold values do not influence the direct comparison between the graphene and gold-based devices.

Figure 3.8 displays the on/off ratios ($R_{ON/OFF}$) trends as a function of the channel length L .

Here, the ratios are evaluated taking in account the different on-set voltages observed between the two architectures, i.e. considering on-state currents for equivalent effective gate bias $V'_{gs} = V_{gs} - V_{on}$. Graphene-based transistors essentially show constant $R_{ON/OFF}$ values of the order of 10^2 in contrast with gold-based devices for which V_{gs} current-modulation decreases towards 10^1 for $L < 400\text{nm}$ (Figure 3.8a). This is further supported by the results shown in Figure 3.8b where $R_{ON/OFF}$ as a function of the applied V_{ds} is plotted for $L=140\text{nm}$ and for comparable $V'_{gs}=100\text{V}$. Graphene-based transistors show increasing $R_{ON/OFF}$ for increasing V_{ds} , as a consequence of the steadily low I_{off} values while. On the other hand, drain-induced barrier lowering degrades $R_{ON/OFF}$ for increasing longitudinal electric fields in gold-based transistors.

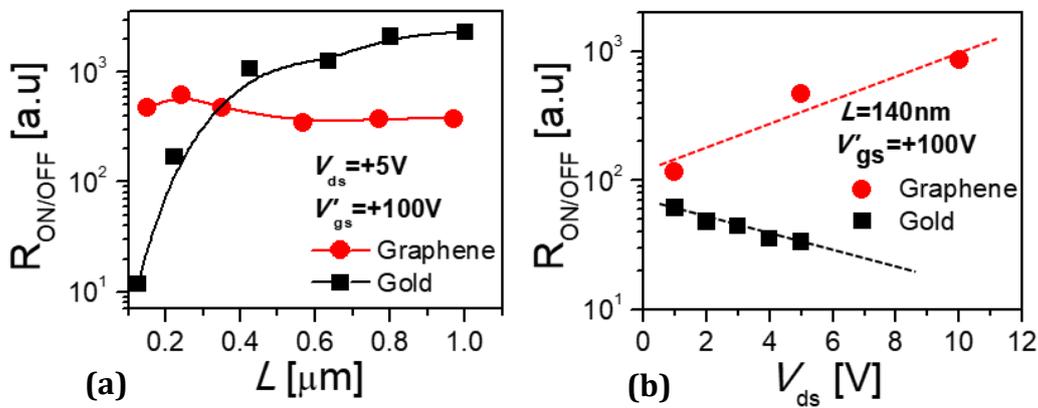


Figure 3.8 (a) Comparison of on/off current ratios for the two architectures as a function of the channel length (L) and (b) as a function of the applied drain-source voltage V_{ds} for $L=140\text{ nm}$. In (a) and (b), equal $V'_{gs} = V_{gs} - V_{on} = 100\text{ V}$ has been considered.

3.1.4 Doping conditions of CVD-Graphene Electrodes

Transport properties of the CVD-graphene electrodes have been inferred from electrical characteristics of micrometric strips ($W=2\ \mu\text{m}$, $L=4\ \mu\text{m}$) in GFET configuration, used as a benchmark test devices (Figure 3.9a and b). In particular, transfer curves have been acquired, before the organic thin film deposition, for pristine graphene and then compared to electrical characteristics obtained after a thermal annealing of the sample for one hour at 373K in vacuum conditions (Figure 3.9c). As inferred from current-voltage characteristics, graphene appears to be heavily p-doped with neutrality point that are shifted towards positive values out of the considered gate-source voltage interval ($-60\text{V} < V_{gs} < +60\text{V}$).

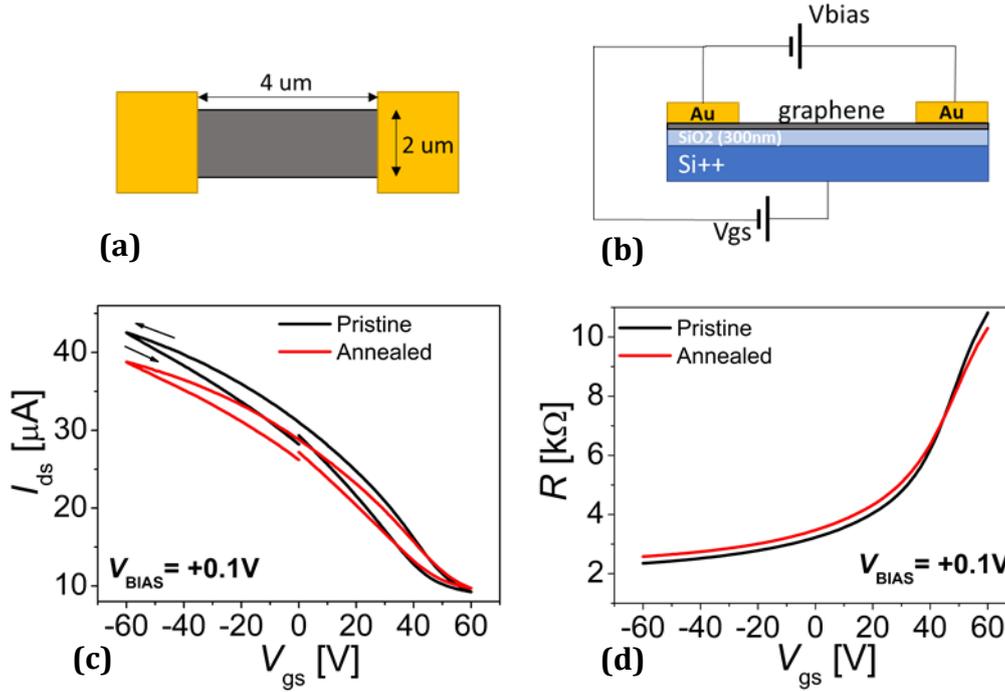


Figure 3.9 (a) Top and (b) lateral-view schematic depiction of micrometric strip of CVD-graphene in GFET configuration. (c) Transfer curves of graphene strips ($W=2 \mu\text{m}$, $L=4 \mu\text{m}$) acquired in vacuum before and after the thermal annealing (1 hour at 373K). Arrows indicate the gate-source voltage sweep directions. (d) Device resistance inferred from (c) as function of the gate-source bias in the range between -60V and +60V.

Considering the total resistance of the device evaluated as $R = V_{bias}/I_{ds}$, sheet resistance values ($R_{sh} = R W/L$) ranging between $1.1 \text{ k}\Omega/\text{sq} < R_{sh} < 5.4 \text{ k}\Omega/\text{sq}$ are observed for a varying gate-source bias in the interval between -60V and +60V.

SKPFM measurements performed in air on the graphene surface confirms quantitatively the arguments deduced from the electrical characterization by the direct determination of the graphene work function in absence of gate-source bias. For further details on the SKPFM technique and the experimental set-up refer to section 4.1. Scanning probe tip, gold contacts and back-gate have been placed at a same reference potential of 0V during the acquisition of both the topography and the surface voltage of a gold/graphene interface (Figure 3.10a and b). Under these conditions, it is possible to observe a negative contact-potential difference (ΔV_{CPD}) building up between the gold and the graphene surface, as shown by the line scan reported in Figure 3.10c. An average difference of $\Delta V_{CPD} \approx -160 \text{ mV}$ is calculated from the statistical analysis of the surface potential map reported in Figure 3.10d. Considering the Cr/Au coted SKPFM tip as characterized by a reference work function value $W_{tip} \approx 4.9 \text{ eV}$, the graphene work function W_{gr} is obtained from the difference between the W_{tip} and the measured contact-potential-difference, namely $W_{gr} \approx W_{tip} - e\Delta V_{CPD}$. For the graphene sample under investigation, an approximate work function of $\approx 5.1 \text{ eV}$ can be deduced, resulting in a difference of approximately 0.6eV with respect un-doped graphene for which values of $W_{gr}^0 \approx 4.55 \text{ eV}$ are typically reported [164,184].

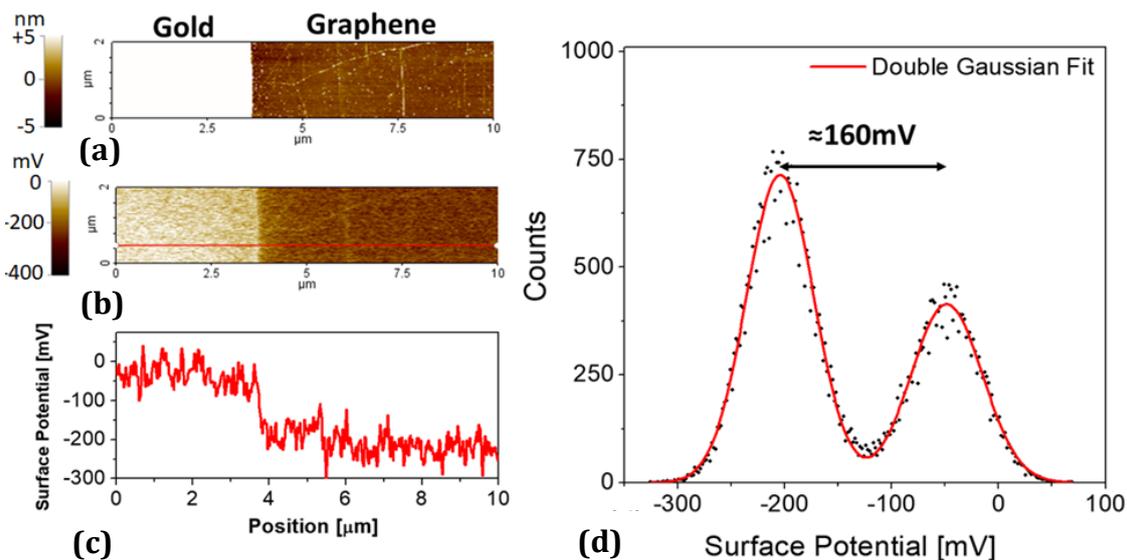


Figure 3.10 (a) AFM topography of the interface between the gold electrode and the bare graphene surface. (b) Surface Potential determined via Kelvin Probe Microscopy of the same portion and (c) correspondent line profile. AFM tip, gold contact and back-gate are placed at the same reference potential during the acquisition of the surface voltage. (d) Histogram of the surface potential values mapped in (b) from which an average contact-potential-difference of 160mV is obtained.

From the previous analysis it is thus possible to give a rough estimation of the energetic mismatch building up at the graphene/OSC interface. In particular, considering the measured work function of p-doped graphene at zero bias ($W_F \approx 5.1$ eV) and the LUMO level of PDIF-CN2 (4.5 eV, as reported in Table 1), a theoretical barrier of 0.6 eV builds up at the heterointerface. A similar mismatch can be assumed even in the case for the gold electrodes for which theoretical values of 5eV are commonly considered, regardless of the possible presence of interfacial dipoles described in Section 1.3.

3.2 PDI8-CN2 BASED NANOMETRIC OFETS WITH LOCAL GATE AND ULTRA-THIN HAFNIUM DIOXIDE AS DIELECTRIC

In this section, the experimental results for nanometric OFETs with locally patterned gate contacts, fabricated following the procedure of Section 2.5, will be presented. A 25 nm thick PDI8-CN2 organic thin film is deposited via OMBD ($R=0.7$ nm/min, $T_{\text{sub}}=95^{\circ}\text{C}$) on the HMDS passivated HfO_2 gate dielectric. The effective device area is outlined by micrometric sink-holes in a 280nm thick PMMA layer (Figure 3.11). This in order to minimize the possible presence of fringing currents affecting the measured current-voltage characteristics. Those contributions appeared as detrimental since the gate-induced accumulation layer is expected to form only in correspondence of the gate tracks. Since perylene diimides typically show negative threshold voltage between 0V and -10V [185], in absence of a proper insulating layer, unwanted current may flow through the interstitial areas between the metallic pads and interconnections where the conductivity of the organic thin film is not modulated by an effective gate voltage.

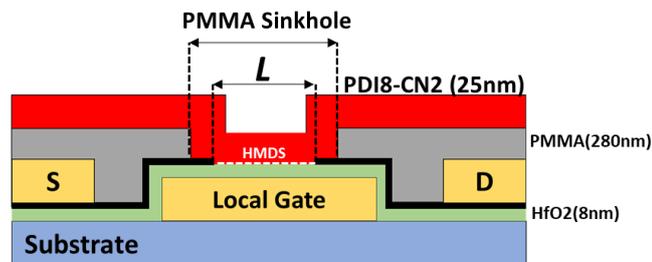


Figure 3.11 Schematic depiction of the PDI8-CN2 based bottom-contacts/local-bottom-gate nanometric OFETs with Hafnium Dioxide as dielectric and CVD-graphene electrodes.

3.2.1 CVD-Graphene on ultra-thin HfO_2

As described in Section 2.5, each transistor array contains a pair of un-cut micrometric graphene strip in GFET configuration, with a fixed channel length of $L=9$ μm and channel width $W=4$ μm . Electrical characterization of GFETs has been performed in order to study the transport properties and the doping state of the electrodes before and after the organic thin film deposition. A schematic depiction of the devices under analysis is shown in Figure 3.12.

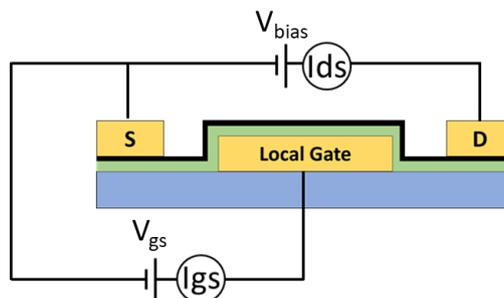


Figure 3.12 Schematic depiction of the micrometric graphene strip ($W=4$ μm , $L=9$ μm) in GFET configuration

As opposed to the device layout of Section 3.1, the 8 nm thick hafnium dioxide layer provides a much stronger capacitive coupling with a capacitance per surface area as high as of $2 \mu\text{F}/\text{cm}^2$. As a consequence, the analysis in terms of applied gate potentials can be limited to few volts. Typical transfer characteristics and correspondent R - V_{gs} curves, for both the $2\mu\text{m}$ and the $5\mu\text{m}$ wide gate tracks, are reported in Figure 3.13.

In this case, both geometries share similar neutrality points centered around $V_{\text{D}} \approx +0.15\text{V}$ while differences in current modulation can be observed. Enhanced charge density modulation is present in wider gate tracks resulting in lower conductivity minimum values (or higher resistance maximum values) in correspondence of the neutrality point. Moreover, a more rapid saturation of the current occurs in the p-type transport branch ($V_{\text{gs}} < V_{\text{D}}$) in the case of $2\mu\text{m}$ wide gate tracks.

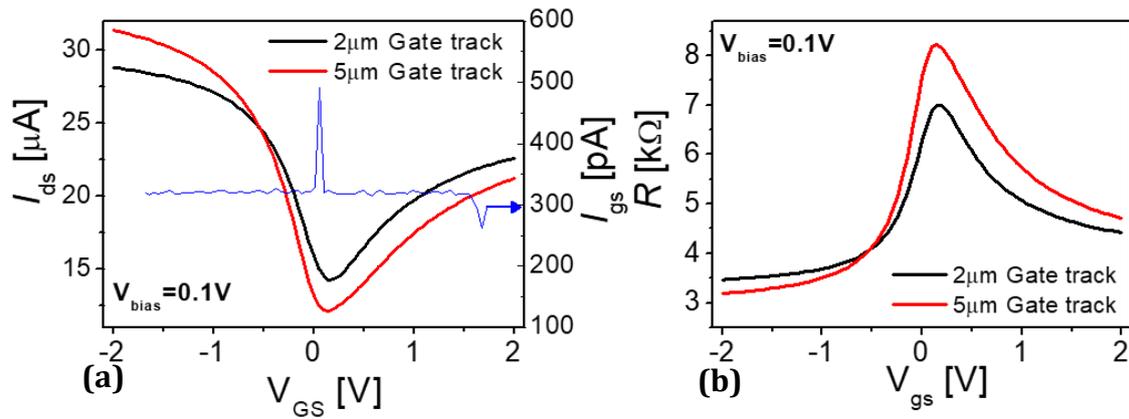


Figure 3.13 (a) Transfer characteristics, acquired in vacuum conditions and at room temperature, of micrometric GFETs ($W=4 \mu\text{m}$, $L=9 \mu\text{m}$) with a 8nm thick HfO_2 as dielectric layer. (b) Resistance as function of the applied gate-source bias of the same devices. The black and red curves are referred to a $2\mu\text{m}$ and $5\mu\text{m}$ wide local gate track, respectively. The applied drain-source bias is 0.1V .

Electron and hole mobility were evaluated from transfer characteristics and R - V_{gs} curves by means of the FTM and DTM methods reported in Section 1.6.2. Results for the $5\mu\text{m}$ wide gate are reported in Figure 3.14. By the application of equation (1.30), gate-dependent field effect mobility (μ_{FET}) can be inferred from the transfer curve (Figure 3.14a). Maximum values of the order of $\approx 10^2 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and $\approx 10^1 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ are obtained for hole and electron-transport, respectively. It must be pointed out that this method clearly underestimates the actual charge carrier mobility since it completely neglects the presence of contact resistances at the gold/graphene interfaces. A more reliable estimation is obtained by fitting separately the n and p-branch of the R - V_{gs} curve by means of (1.29), as shown in Figure 3.14b.

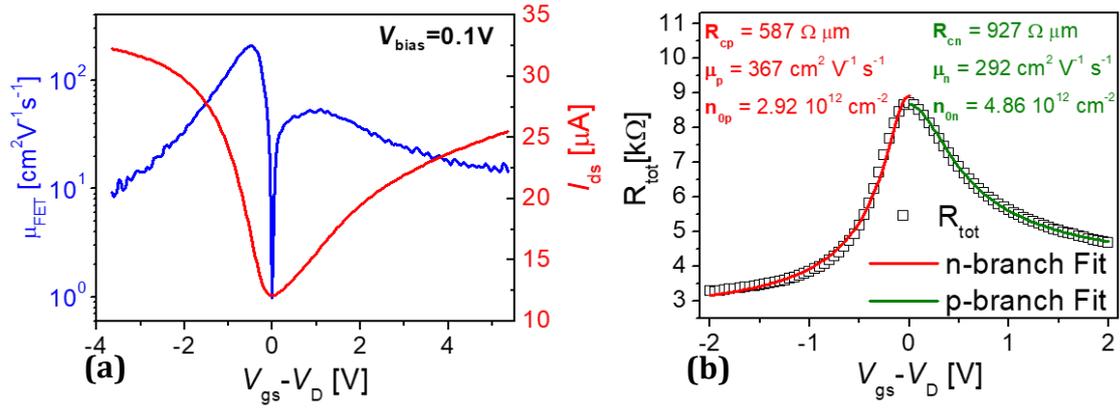


Figure 3.14 (a) Transfer curve (red line) of graphene transferred on 8nm HfO₂. The local gate track has a width of 5 μm . The blue curve individuates the field effect mobility calculated by equation (1.30). (b) Total resistance of the same device as function of the applied gate voltage. Applying the fitting curve of equation (1.29) for the n-branch and the p-branch separately, contact resistances of the GFET, electron/hole mobility and the residual charge density can be determined.

In this case, despite that the fitting procedure provides gate-independent values, hole and electron mobilities are $367 cm^2 V^{-1} s^{-1}$ and $292 cm^2 V^{-1} s^{-1}$ respectively. Contact resistances of $\approx 10^2 \Omega$ and residual charge density in the order of $\approx 10^{12} cm^{-2}$ are extracted as well. This latter parameter appears to be quite larger than those usually observed in both CVD and exfoliated graphene for which values of $10^{11} cm^{-2}$ are typically reported for state-of-the-art samples [186].

The effect of the individual stages of the OMBD deposition procedure, on the doping state of the graphene electrodes, have been simulated by observing the changes in the electrical performances of the devices after a thermal annealing of the substrate in vacuum for one hour at 373K and after the deposition of a 25nm PDIF-CN2 organic thin film. N-type doping is observed by exposing the sample to the thermal treatment, with neutrality points shifting towards $V_{gs} \approx -0.4V$. Conversely, the presence of the PDIF-CN2 thin film manifests as molecular p-doping on the graphene surface with an average shift of the neutrality points centered around $V_{gs} \approx +1V$ (Figure 3.15), indicating doping concentrations as high as $1.25 \cdot 10^{13} cm^{-2}$.

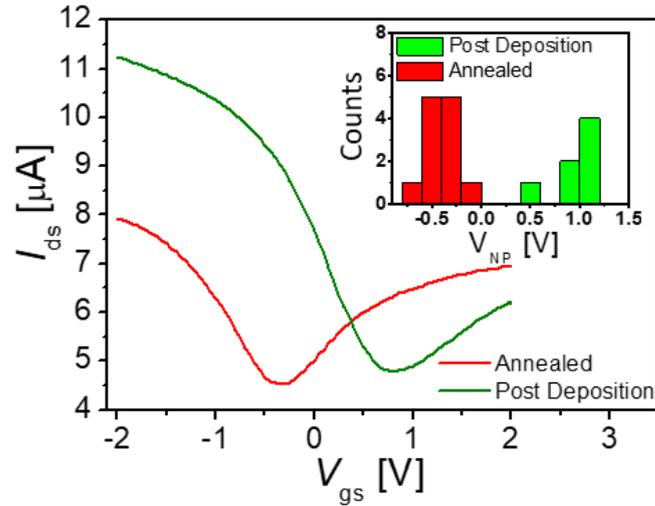


Figure 3.15 Transfer curves acquired in vacuum after a thermal annealing at 373K for 1 hour (red curve) and after the deposition of 25 nm thick PDIF-CN2 organic thin film. The inset shows the average of neutrality points after the thermal annealing and after the organic thin film deposition.

As it will be described in the ongoing discussion, PMMA sinkholes are crucial to ensure proper functioning of the nanometric OFETs. On the other hand, the presence of a thick layer of polymeric resist may influence substantially the transport properties of the graphene electrodes. At this regard, transfer characteristics of GFETs characterized by bare and PMMA-covered graphene microstrips have been investigated. The effect of charge transfer occurring at the PMMA/graphene interface is clearly visible in Figure 3.16a in terms of a positive shift of V_D towards +0.5V for transfer curves acquired in vacuum. Doping effects are observed to be even larger comparing I_{ds} - V_{gs} curves acquired in air, as plotted in Figure 3.16b: in this case the influence of the PMMA layer is similar to that observed in the presence of the organic semiconductor, with a neutrality point shift of $\Delta V_D \approx +1V$.

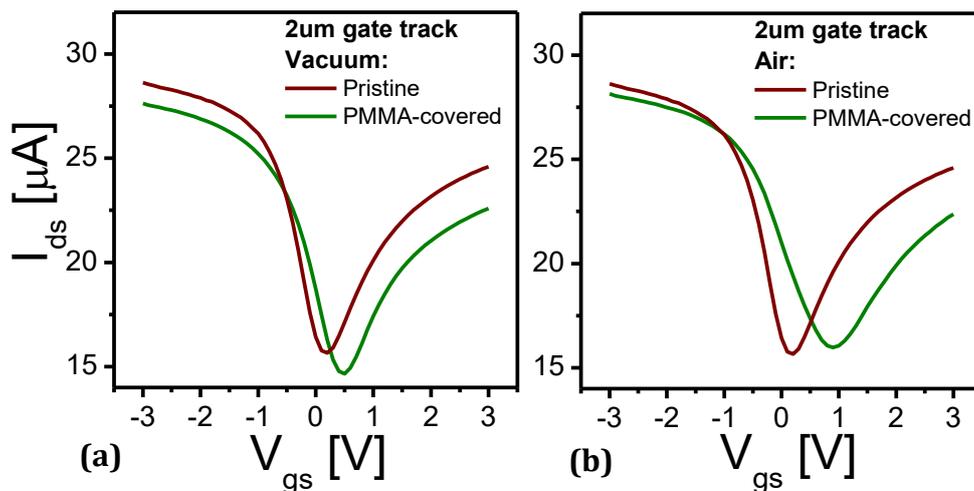


Figure 3.16 (a) Transfer curves acquired in vacuum for pristine and PMMA-covered graphene microstrip in GFET configuration. (b) Same analysis performed in air.

3.2.2 Current-Voltage characteristics

After the organic thin film deposition, electrical characterization of nanometric OFETs has been performed in vacuum at room temperature by means of the same experimental set-up of Section 3.1.2. Typical transfer curves in saturation regime, as function of the channel length, are reported in Figure 3.17 for both 2 μm and 5 μm wide local gate tracks. The phenomenology encountered in short channel devices presented in Section 3.1.3 still holds in the case of local gate architectures and PDI8-CN2 thin films. Off-state currents are limited between 1×10^{-9} A and 3×10^{-9} A with on/off ratios reaching values of $\approx 10^2$ for $L=200\text{nm}$. In the case of 2 μm wide gate track (Figure 3.17a), excellent current modulation with channel length is observed for $-2\text{V} \leq V_{\text{gs}} \leq +3\text{V}$, with maximum I_{ds} values scaling accordingly with the lateral dimensions of the active channel.

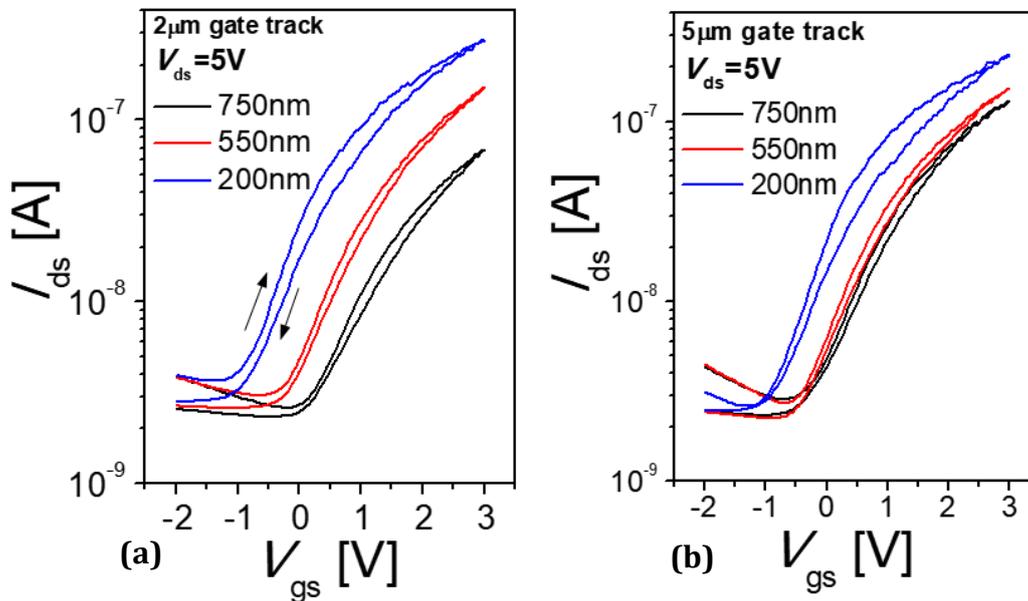


Figure 3.17 Transfer characteristics in saturation regime ($V_{\text{ds}}=+5\text{V}$) at room temperature acquired in vacuum of PDI8-CN2 based nanometric OFETs with local gate electrode and channel length $L=\{200\text{nm}, 550, 750\text{nm}\}$ (for a fixed channel width of 4 μm). (a) and (b) refer to the 2 μm and 5 μm wide local gate track.

Threshold voltages undergo to a progressive shift towards negative voltages, with values ranging from $V_{\text{th}}=-0.25\text{V}$ for $L=750\text{nm}$ to -0.60V and -1.4V for $L=550\text{nm}$ and $L=200\text{nm}$, respectively. Moreover, referring to Figure 3.17b, the confined active area given by the PMMA sinkholes is observed to influence the overall response of the devices. Current appears to be poorly modulated by L in the case of wider gate track, especially for decreasing W/L ratios for which fringing current may result from conduction paths that are not purely delimited by graphene edges.

From transfer curves of Figure 3.17a, it is possible to extrapolate the width-normalized transconductance from which the field-effect-mobility in saturation regime are retrieved via equation (1.10). As depicted in Figure 3.18a, increasing maximum transconductance values ranging between $8 \times 10^{-3}\text{S/m} \leq g_m W^{-1} \leq 2 \times 10^{-2}\text{S/m}$ are observed for

decreasing channel lengths, corresponding to gate-dependent mobilities with maximum values $\mu_{sat} \approx 10^{-3} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. A loss of about one order of magnitude is thus inferred for the nanoarchitectures, if directly compared to state-of-the-art long channel devices for which μ_{sat} usually range in between $10^{-2} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$.

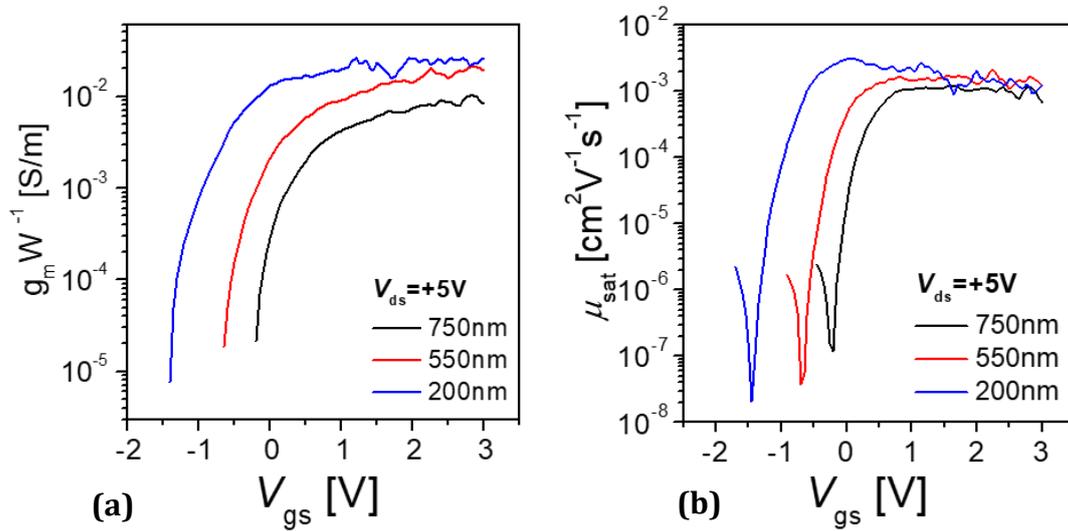


Figure 3.18 (a) Width-normalized transconductance of nanometric PDI8-CN2 OFETs calculated by differentiating the transfer curves of Figure 3.17a. (b) Field-effect-mobilities in saturation regime for the same dataset.

Focusing the attention on shortest channel devices, transfer curves acquired for $+1V \leq V_{ds} \leq +5V$ are reported in Figure 3.19. Considering the linear bias regime ($V_{ds} < V_{gs}$), contact resistances affects clearly the transport for lower drain biases, with a steep variation of the I_{ds} slope in correspondence of $V_{gs} \approx +1V$ (Figure 3.19a). As a result, field-effect-mobility values, calculated by means of equations (1.9) and (1.10), are observed to be significantly dependent on the applied V_{ds} or, alternatively, on the extremely dense electric fields building up at the electrodes ($E_{field} = V_{ds}/L$). Averaged values ranging from $2 \times 10^{-4} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ to $7 \times 10^{-4} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ are reported in Figure 3.19b for $5 \times 10^6 \text{V/m} \leq E_{field} \leq 2.5 \times 10^7 \text{V/m}$.

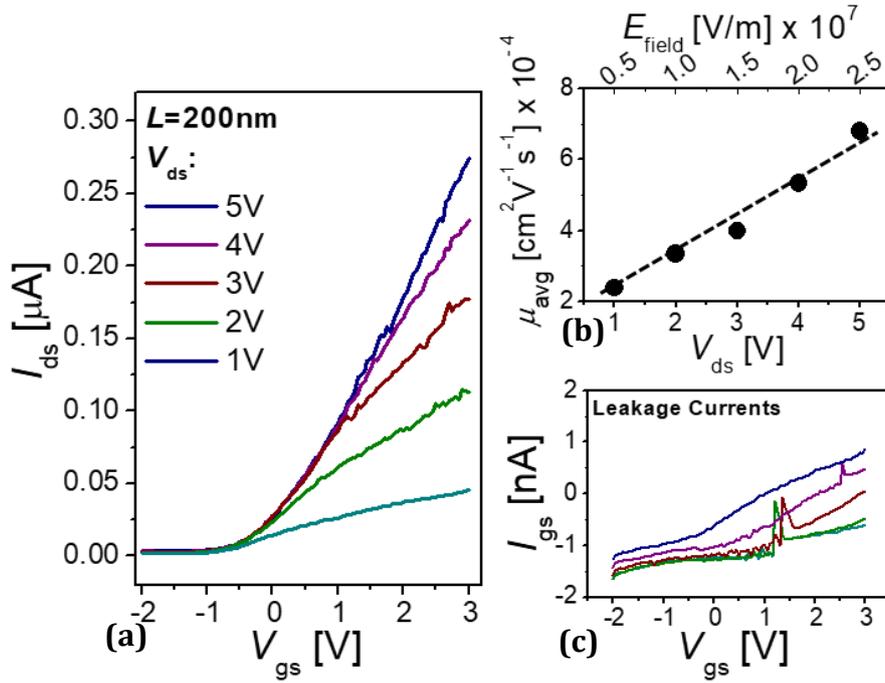


Figure 3.19 (a) Transfer characteristics as function of varying V_{ds} bias for an $L=200\text{nm}$ and $W=4\ \mu\text{m}$ PDI8-CN2 based OFET with local gate and CVD-graphene electrodes. Curves were acquired in vacuum conditions at room temperature. (b) Average field-effect mobility (μ_{avg}) as function of the applied drain-source bias. Top x-axis individuates the equivalent electric field applied at the electrodes ($E_{field}=V_{ds}/L$). Data are obtained considering the mean value of the gate-dependent mobility for $V_{gs}\geq V_{th}$. (c) Gate-source currents (I_{gs}) for drain-source bias $+1\text{V}\leq V_{ds}\leq +5\text{V}$.

Measured leakage currents (I_{gs}) are negligible if compared to the channel current I_{ds} , with values limited within 1 nA for every V_{ds} considered (Figure 3.19c).

Output curves, acquired in vacuum, are observed to take great advantages from the increased capacitance per surface area given by the ultra-thin HfO_2 layer, if compared with the 300nm thick SiO_2 employed for PDIF-CN2 based transistors of Section 3.1. Current saturation is achieved independently of the channel length within $V_{ds}=3\text{V}$ and $-2\text{V}<V_{gs}<+2\text{V}$, as it can be observed in Figure 3.20. The scaling behavior of maximum currents follows the $I \propto 1/L$ trend according with the previously observed phenomenology for transfer curves. Considering the device with $L=200\text{nm}$, for both the 2 μm and 5 μm wide gate tracks, current noise is observed for $I_{ds}>0.1\ \mu\text{A}$. This can be likely ascribable to the non-negligible presence of grain boundaries that influence the transport path within the drain-source pair for high biases.

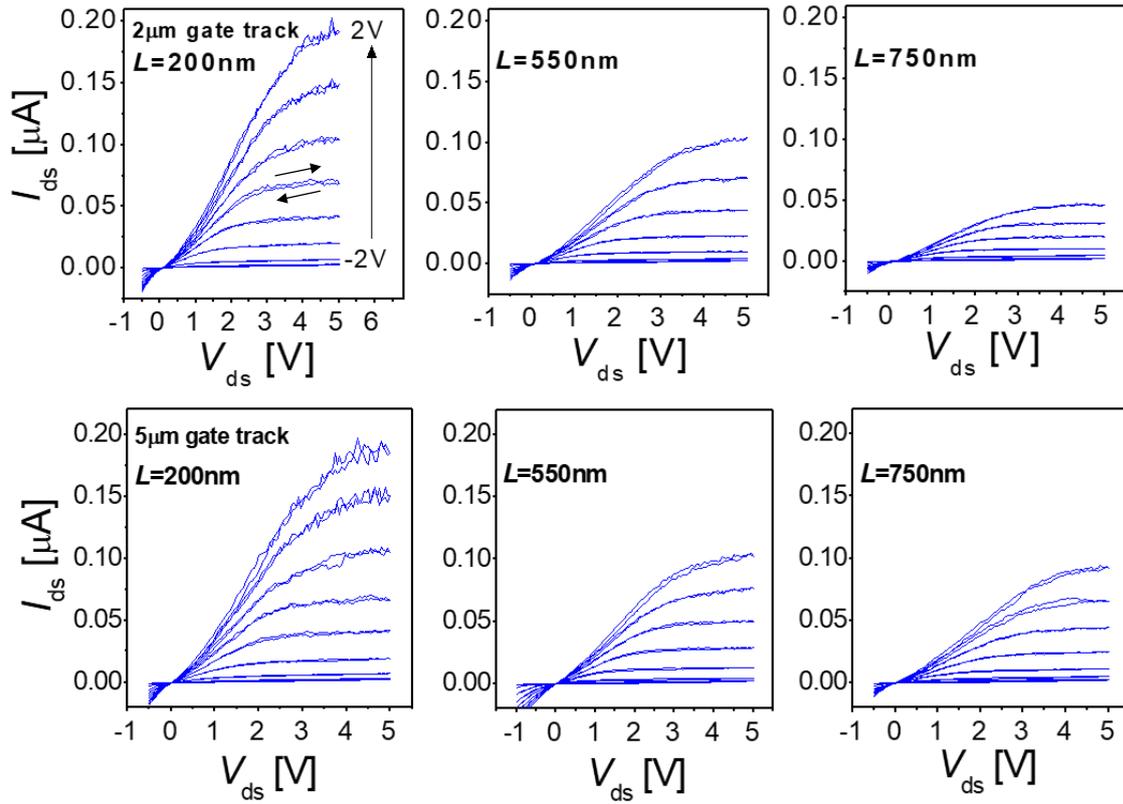


Figure 3.20 Output curves for the bottom-contacts/local-bottom-gate nanoarchitectures with CVD-graphene electrodes and PDI8-CN2 as organic semiconductors. The acquisition has been performed in vacuum. Top panels are referred to the 2 μm wide gate track for varying channel length L . Channel width is fixed at 4 μm . Lower panels show experimental results for wider gate track (5 μm) and equal channel lengths and widths.

3.2.3 AC characterization

In contrast with the distributed-gate layout, for which unavoidable parasitic capacitances may dominate over the dynamic response of the device, the local gate architecture under investigation is particularly well suited for AC analysis, due to its limited overlap length between the electrodes and the gate interface. In this case, AC characterization aims to the investigation of the quite exotic graphene/HfO₂ interface and to the estimation of the equivalent capacitance of the nanometric channels of the final OFETs, with the indirect determination of the cut-off frequency as final goal.

Measurements have been performed by mean of an Agilent™ 4284A Precision LCR Meter, in vacuum conditions. The instrument has a DC bias capability (V_{bias}) of $\pm 40\text{V}$ and a wide frequency range of 20 Hz - 1 MHz. The amplitude of the sinusoidal probing signal (V_{rms}) can be tuned between -2V and 2V. The experimental set-up is schematically depicted in Figure 3.21. The automated acquisition is driven externally by means of user-defined LabView interfaces. In the following discussion, both C - V_{bias} analysis and impedance spectroscopy (C -freq) acquired in vacuum will be shown.

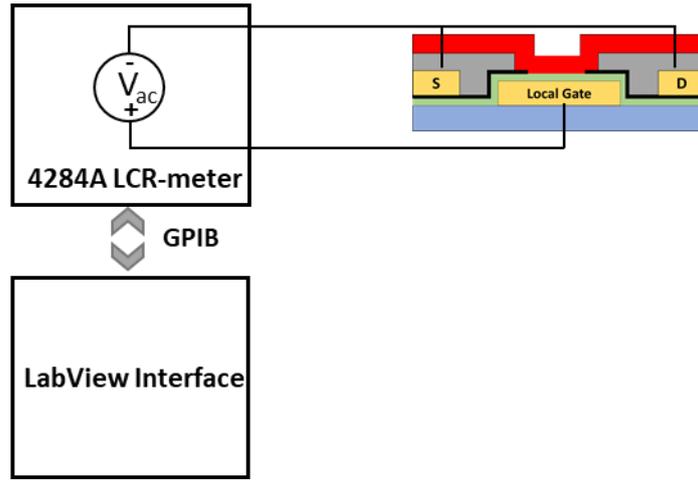


Figure 3.21 Schematic representation of the experimental set-up for the AC characterization of the OFETs

3.2.4 Capacitance contribution of graphene electrodes

As preliminary investigation, impedance spectroscopy of graphene electrodes has been performed before the organic deposition. In Figure 3.20 the device configuration and the equivalent circuit are reported.

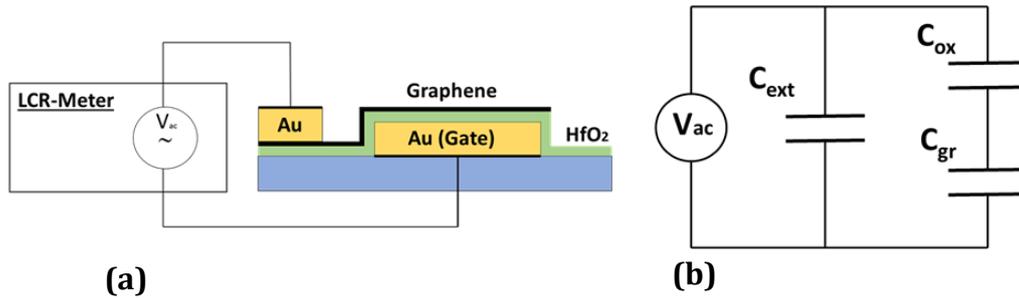


Figure 3.22 (a) Schematic depiction of the graphene-based capacitor under analysis and (b) Equivalent circuit. C_{ext} indicates the parallel contribution given by the experimental set-up (LCR-meter and coaxial cables) while C_{ox} and C_{gr} forms the capacitance series individuated by the oxide layer and the graphene sheet acting as counter-electrode.

The LCR meter is connected to the metallic gate track while the graphene sheet act as counter electrode in a equivalent architecture characterized by parallel planes where the 8nm thick HfO₂ layer acts obviously as dielectric buffer. The system can be thus assumed as composed by a capacitance series (C_{tot}) including the geometrical contribution of the oxide layer (C_{ox}) and of the graphene surface (C_{gr}), namely:

$$C_{tot}^{-1} = C_{ox}^{-1} + C_{gr}^{-1} \quad (3.1)$$

A spurious contribution, due to the experimental set-up, comprising the LCR-meter and the connection cables, must be taken in account as a parallel term named C_{ext} (Figure

3.20b).

The total capacitance of the system (C_{tot}), as a function of the frequency, has been measured in the interval between 1kHz and 1MHz, using a sinusoidal probe signal with $V_{rms}=+0.05V$. Several curves have been acquired adding a fixed DC (V_{bias}) component to the AC-signal. The considered DC biases range from -2V to +2V with 0.2V steps. For each V_{bias} value, the effective contribution of the sample is singled out by subtracting a reference curve acquired in open circuit configuration, i.e. in absence of electrical connection with the sample, eliminating in such a way the spurious contribution of the experimental set-up. Data are thus normalized considering the effective surface of the graphene strip in contact with the gate track. According to the functional trends plotted in Figure 3.23a, normalized capacitance appears to be dependent on both the frequency and applied bias.

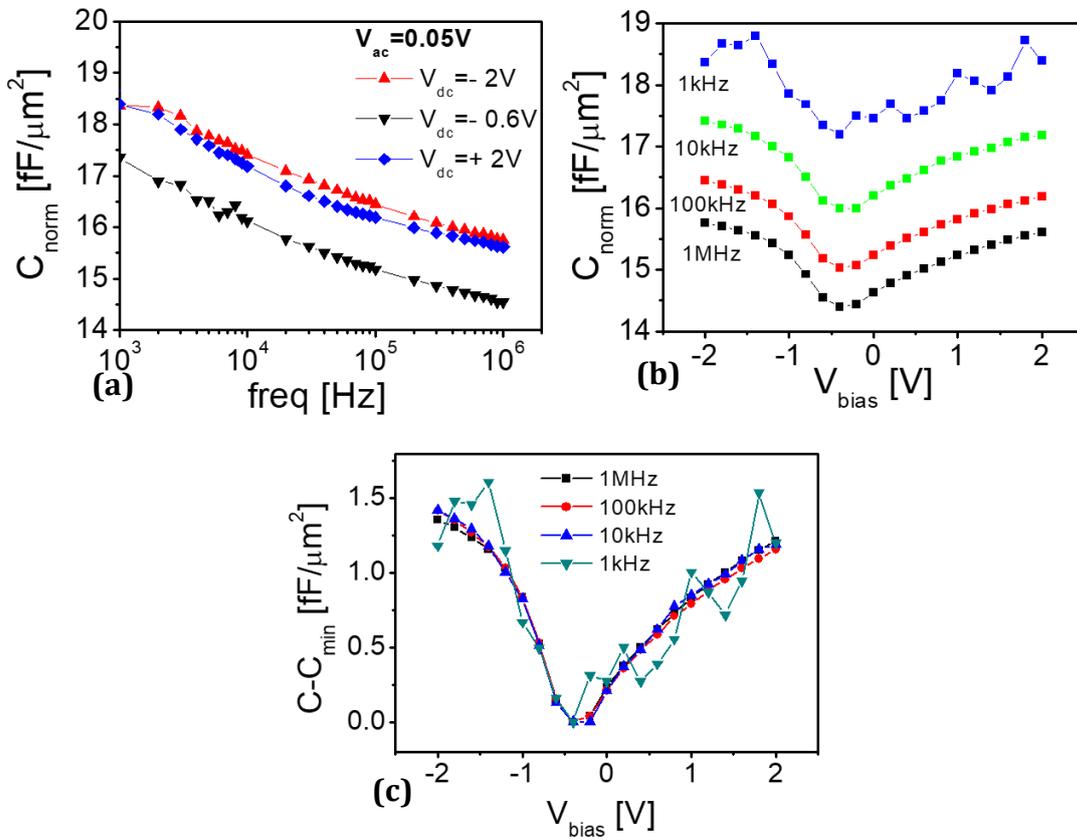


Figure 3.23 (a) Normalized capacitance (C_{norm}) as function of the frequency, for various DC biases $-2V < V_{bias} < 2V$ with a 0.2V step. Here, only the interval boundaries and a single central value are reported for the sake of clarity. (b) C_{norm} as function of V_{bias} extracted from data reported in (a) for various frequency values (1kHz, 10kHz, 100kHz and 1MHz). (c) Average capacitance modulation for various frequency values, obtained by subtracting capacitance minima in correspondence of the neutrality point ($V_D \approx -0.4V$).

The latter feature has been further analyzed extracting the $C-V_{bias}$ curves at different frequency values fixed at 1kHz, 10kHz, 100kHz and 1MHz, respectively. Results are reported in Figure 3.23b where $C-V_{bias}$ trends suggest a clear signature from the quantum capacitance of graphene. The measured capacitances have a minimum value at the Dirac point ($V_D \approx -0.4V$ as reported in Section 3.2.1) which decreases for increasing frequencies.

An average modulation of $\approx 1.4 \text{ fF}/\mu\text{m}^2$ is observed, independently from the considered frequency (Figure 3.23c).

3.2.4.1 Quantum Capacitance of Graphene

From the C-V data of Figure 3.23, quantum contribution of graphene can be extracted straightforwardly from equation (3.1), considering:

$$C_{gr}(V_{ch}) = \frac{C_{ox}C_{tot}(V'_{gs})}{C_{ox} - C_{tot}(V'_{gs})} \quad (3.2),$$

Where $V'_{gs} = V_{gs} - V_D$ is the effective applied gate bias while V_{ch} individuates the graphene channel potential (inset of Figure 3.24). This latter parameter can be calculated for any V'_{gs} using the following relation [187]:

$$V_{ch} = V'_{gs} - \int_0^{V'_{gs}} \frac{C_{tot}}{C_{ox}} dV'_{gs} \quad (3.3),$$

which is the integral form of $C_{tot}dV'_{gs} = C_{ox}d(V'_{gs} - V_{ch})$, resulting from charge conservation. The observed trends of V_{ch} as function of the effective gate bias V'_{gs} are reported in Figure 3.24. Considering that the graphene channel potential is directly related to the fermi energy since $V_{ch} = E_f/e$, it is possible to observe a symmetric modulation around 0V and induced variations as high as 0.5eV in correspondence of $V'_{gs} \approx +2V$. Again, the behavior is directly influenced by the considered frequency with a more efficient interfacial coupling for 1MHz.

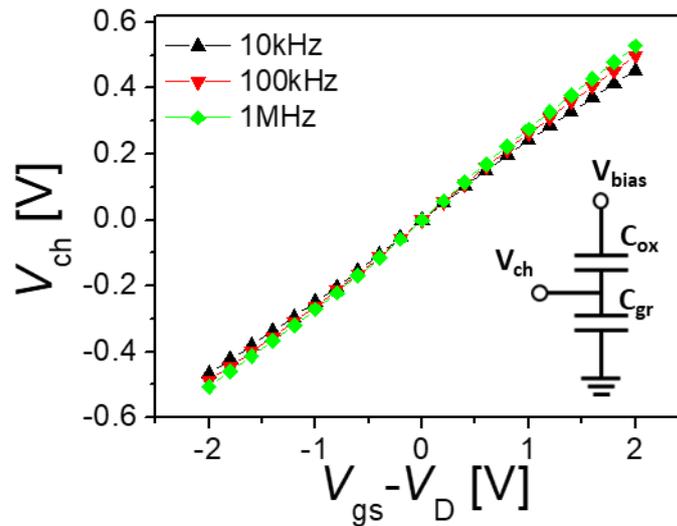


Figure 3.24 Calculated graphene channel potential V_{ch} as function of the effective applied gate $V_{gs}-V_D$. The inset shows the equivalent circuit considered for the estimation of V_{ch} .

Combining the V_{ch} data obtained via equation (3.3) and C_{gr} values calculated through equation (3.2), and considering a constant oxide capacitance $C_{ox} = 2.21\mu F/cm^2$, it is possible to compare directly the experimental curves with the theoretical values for quantum capacitance obtained through equation (1.32), considering different residual charge densities n_0 . In Figure 3.25, C_{gr} data are plotted as function of the Fermi energy E_f . Apparently, the theoretical model fails in describing the behavior of the samples under analysis and agreement is found uniquely in proximity of the neutrality point for the 100kHz and 1MHz curves. The comparison let to estimate a residual charge density of $4 \times 10^{12} \text{ cm}^{-2}$, in accordance with values obtained from electrical characterization reported in Section 3.2.1.

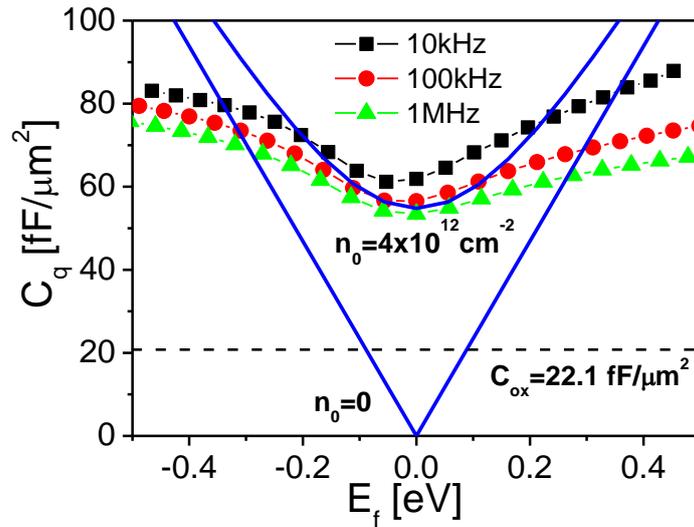


Figure 3.25 Measured quantum capacitance of graphene as function of the Fermi energy E_f , for different frequency values (symbols). Data are acquired at room temperature and in high vacuum. Experimental values can be compared with theoretical curves (blue solid lines) obtained using equation (1.32) for different residual charge density n_0 . The black dashed line indicates the nominal oxide capacitance given by the 8nm thick HfO_2 layer, considering a dielectric constant of $k=20$.

The observed discrepancies, at this stage of the investigation, can be mainly ascribed to the HfO_2 layer or, more specifically, to the HfO_2 /graphene interface. Dipolar effect, for example, could be induced by the presence of organic contaminants, such as resist residues, resulting in an additional capacitive term that might strongly depend on the probing frequency. Moreover, the employed C_{ox} value, for the calculation of both V_{ch} and C_{gr} , is not directly measured and it is assumed to be constant both with the frequency and the applied bias. A theoretical value of $\approx 2.21\mu F/cm^2$ is taken in account, considering the nominal oxide thickness (8nm) and a quite conservative estimation of its dielectric constant, $k=20$ (in comparison with reported values ranging typically from 18 to 24). For this analysis, this might be an overly strong assumption since the measured total measure capacitance appears to be clearly dependent on the frequency with a rigid shift observed between different C - V curves in Figure 3.23b. Dielectric relaxation of the HfO_2 thin film [188,189] could lead thus to a systematic error in the estimation C_{ox} resulting in the observed differences with the theoretical model of Figure 3.25. In addition to this, it

cannot be excluded that CVD-graphene may be characterized by the presence of structural defects or nucleation sites in correspondence of the considered areas for the C-V characterization. In this case, the theoretical model must be replaced in order to take in consideration a bi- or multi-layer structure [190].

3.2.5 Calculated Cut-off frequencies for short channel OFETs

The estimation of the electrode capacitance allows the indirect calculation of the cut-off frequency introduced in Section 1.4. In particular, it is possible to assume the equivalent gate capacitance C_G as the parallel including the gate-dependent contribution given by the graphene overlap $C_{gr}(V_{gs})$ and the channel contribution C_{ch} . The latter will be considered in first approximation correspondent to the gate oxide capacitance C_{ox} . Under these assumptions, equation (1.18) thus becomes:

$$f_T = \frac{g_m}{2\pi C_G} \approx \frac{g_m}{2\pi [C_{gr}(V_{gs})S_{ov} + C_{ox}S_{ch}]} \quad (3.4),$$

where S_{ov} indicates the overlap area between the graphene electrodes and the gate track, $S_{ch} = W L$ is the channel area and g_m is the electrical DC transconductance acquired in saturation regime ($V_{ds}=+5$). Results are depicted in Figure 3.26 for the transistor array presented in Figure 3.17a. Data have been obtained considering the graphene capacitance obtained at 100kHz and its gate dependence observed in Figure 3.23. As previously discussed, a correct evaluation of C_{ox} is undoubtedly critical. At this regard, both capacitance terms in equation (3.4) have been considered as affected by a 20% uncertainty, this in order to include the observed frequency dependence of the nominal oxide capacitance. As a general remark, cut-off frequencies follow the corresponding trend of the transconductances as function of the gate voltage; the latters range from maximum values of $g_m \approx 10^{-8} S$ for $L=750nm$ to $g_m \approx 10^{-7} S$ for channel length approaching $L=200nm$. In this case, a maximum cut-off frequency $f_T \approx 100$ kHz is obtained when g_m saturate towards a steady value ($V_{gs}>+1V$).

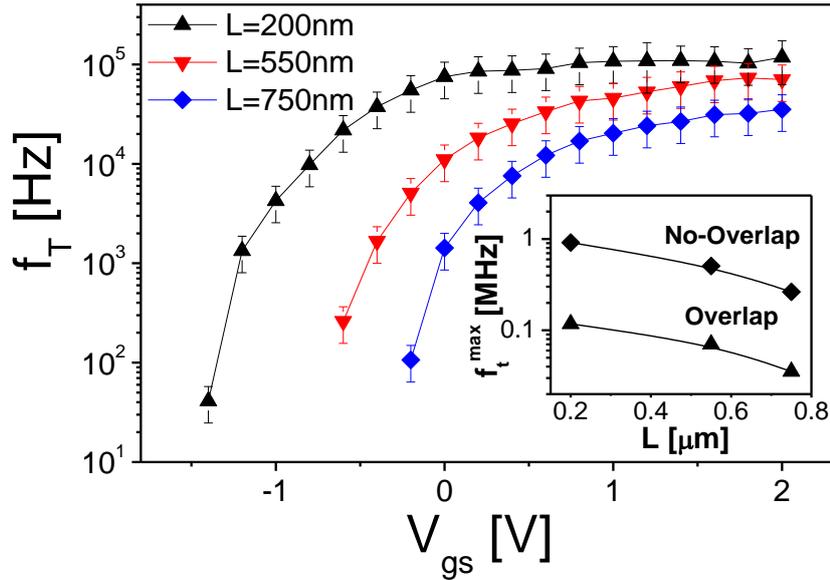


Figure 3.26 Calculated cut-off frequencies (f_T) for the PDI8-CN2 based nano OFETs with HfO₂ as local gate dielectric, for the three different channel lengths. Data are acquired in high-vacuum conditions and at room temperature. The applied drain-source voltage is $V_{ds}=+5V$. The inset shows the influence of the overlap contribution over the maximum f_T values.

The magnitude of the influence of the overlap contribution is clearly visible from the inset of Figure 3.26 where maximum frequency including the contribution of the graphene electrodes (overlap) are compared to values obtained taking in account only the channel contribution (no-overlap). In the latter case, theoretical maximum values $0.2MHz \leq f_T^{max} \leq 1MHz$ are estimated, with deviations of one order of magnitude with respect to the actual devices.

3.3 FINAL DISCUSSION

The phenomenological picture that stems from the experimental results suggests that nano OFETs with graphene electrodes show great advantages in terms of electrical performances with respect the gold-based architectures. Short channel effects are considerably suppressed in distributed-bottom-gate architectures based on PDIF-CN2 thin films: enhanced response for high longitudinal drain-source electric fields are demonstrated for L down to 140 nm.

In particular, we found that the output characteristics of the graphene-based devices, in the distributed-bottom-gate configuration, respond linearly to the applied bias, in contrast with the supra-linear trend of gold-based transistors. Despite this, the magnitude of the currents appears to be limited in the graphene case suggesting a major contribution of contact resistances.

Contacts effects are indeed known to be not uniquely dictated by the energetic alignment at the electrode/organic Schottky interface, but morphological and geometrical contributions must be also considered. In particular, different crystalline orientations, namely when the molecules sit on the substrate with the edge (stand-up) or the face (lay-

down), play a major role in the final properties of the system [191]. In our case, when one-atom thick graphene is used as the electrode, charges are likely to be injected perpendicularly with respect to the molecular layer in contrast with the 30nm thick gold contacts where the transport of the charge carriers takes place mostly in the parallel direction, resulting in lower contact resistances, as discussed in 3.1.1. Nevertheless, the high resistive but still-ohmic region at the electrodes can be considered as a healing factor that hinders the creation of an intense electric field (of the order of MV/cm in 100nm long channels for $V_{ds}=+20$ V), limiting the space charge transport in the bulk of the organic channel. This last assumption is strengthened by considering the exponents calculated from the log-log plots of Figure 3.6. The SCLC contribution, whose signature can be referred to exponents diverging towards $n=2$, is clearly observable in the case of gold electrodes, especially for V_{gs} approaching on-set values. A similar analysis on graphene-based devices, on the contrary, suggest a linear proportionality between the electric field, building up at the electrodes, and the current.

Graphene electrodes appears to have a noticeable influence also on the drain induced barrier lowering typically affecting the off-state currents of nano OFETs. Current on/off ratios independent of L and enhanced response for increasing V_{ds} have been observed. These results can be explained taking into account the gate-tunability of the work function in monolayer graphene. In particular, considering the measured work function of p-doped graphene at zero bias ($W_F=5.1$ eV) and the LUMO level of PDI8-CN2 (4.5 eV) theoretical barrier of 0.6 eV builds up at the heterointerface. This value depends directly on the applied V_{gs} since W_F for graphene decreases (i.e., becomes more negative) for negative gate voltages, as Kelvin Probe measurements reported in literature suggest. As a result, an increasing barrier is expected for decreasing gate-source voltages towards negative onset threshold values, counterbalancing in such a way the drain induced barrier lowering and suppressing the punch through currents otherwise observed in gold-based transistors, as reported in Figure 3.7.

Moving to the experimental results obtained for the local-bottom-gate architecture with ultra-thin HfO_2 as high-k dielectric, the aforementioned phenomenology still holds for PDI8-CN2 thin film devices. Again, off-current sustains the downscaling of channel length L down to 200nm, with off-state current values pinned in the nA scale. Differently from the distributed-gate layout, the increased gate capacitance allows a proper current saturation of the devices within V_{ds} : excellent low voltage transistor operation has been thus demonstrated. Despite this, the evaluation of field-effect-mobility indicates a loss of one order of magnitude with respect to long-channel counterparts, based on gold electrodes. For short channel PDI8-CN2, maximum values $\mu_{FET} \approx 10^{-3} cm^2 V^{-1} s^{-1}$ are obtained while $\mu_{FET} \approx 3 - 4 \times 10^{-2} cm^2 V^{-1} s^{-1}$ are typically reported in state-of-the-art devices with $L=10-20 \mu m$ ($W/L > 100$). It is thus possible to assert that contact resistances still remain the main bottleneck in terms of electrical performances. It should be pointed out, however, that their presence is in any case unavoidable and yet fundamental for the suppression of short-channel effect, in addition to the electronic peculiarities of graphene electrodes.

AC characterization, reported in Section 3.2.3, highlights the role of quantum capacitance

of graphene (C_q) that, since the peculiarities of the HfO₂ MIS structure, start to contribute considerably to the equivalent capacitance series given by the electrodes and by the oxide layer. In particular, $C_q \approx 6 \mu F/cm^2$ is typically observed in comparison with $C_{HfO_2} \approx 2.21 \mu F/cm^2$ given by the 8nm thick dielectric. This clearly influence the cut-off frequency calculated by accurately estimating the overlap surface of the electrodes and the DC-transconductance of the nano OFETs: a maximum cut-off $f_t=10^5$ Hz is obtained for $L=200$ nm. This value is strictly related to the spurious contribution of graphene electrodes to the total channel capacitance and it is directly dictated by the intrinsic transport properties of the PDI8-CN2 thin films, since $f_t \propto \mu/C_g$. It is thus clear that a further optimization of both the architecture and of the organic thin film could imply an enhancement in terms of the cut-off frequency towards the MHz or above, with huge technological implications.

4 THE GRAPHENE/ORGANIC INTERFACE

This last chapter is devoted to the specific investigation of the graphene/organic interfaces via photoemission spectroscopy and Scanning Kelvin Probe Force Microscopy (SKPFM). Particular attention will be spent to the study of contact effects in the micrometric graphene-based architectures presented in Section 2.6. In this case, PDI8-CN₂ has been selected as organic semiconductor. Despite this material has lower reported performances with respect to PDIF-CN₂, its choice here is motivated by the easiness by which it can be deposited via OMBD. Experimentally, in fact, this organic material appears to be much less influenced by both the deposition parameters (such as the deposition rate R and the substrate temperature T_{sub}) and by the initial conditions of the bare substrate. Contact interfaces are thus expected to be almost totally unaffected by the presence of the atomically thin graphene sheet and, consequently, the analysis can be aimed to the investigation of the pure electronic properties at the electrode/semiconductor boundaries.

In the first section of the chapter, a detailed description of SKPFM technique and its working principles will be provided. In the following discussion, a recently reported analysis of contact effects at the gold/organic interfaces in state-of-the-art PDIF-CN₂ based micrometric devices will be presented as frame of reference for the results obtained for PDI8-CN₂ thin films with equivalent architectures. In this case, the effect of different film thicknesses will be assessed. Hence, similar analysis will be performed in the case of CVD-graphene electrodes, giving insights on the charge injection and extraction phenomena at the organic/graphene interfaces. This in addition to a standard electrical characterization of the organic transistor and, individually, of the graphene electrodes in GFET configuration.

In the last section of the chapter, further details on the interface energetics will be provided by analyzing photoemission spectra of bare organic/graphene interfaces. Ultra-thin layers, with sub monolayer or 1-2 monolayer coverages of both PDI8-CN₂ and PDIF-CN₂, grown on large area CVD-graphene sheets, will be investigated by means of Ultra-violet Photoelectron Spectroscopy (UPS). Elemental analysis of 25nm thick films, used as reference samples, and of pristine graphene sheet will be provided via X-ray Photoelectron Spectroscopy (XPS).

4.1 SCANNING KELVIN PROBE FORCE MICROSCOPY

Scanning Kelvin Probe Force Microscopy, firstly introduced by Nonnenmacher et al. in 1991 [192], is a reliable and versatile tool to directly measure a local potential difference between the sample and a conducting AFM tip, thereby mapping the work function or the surface potential, with high spatial resolution, over a relatively large area. In recent years, SKPFM has been widely used in determining surface voltage characteristics and contact resistances in various organic devices, such as pentacene [193], P3HT [55] and TPD:PS [194] based OTFTs, exploiting the advantage to estimate separately the contributions of source and drain electrodes to the overall contact resistances, in contrast with alternative techniques such as the transmission line method and gated four-probe configurations (Section 1.3.2).

The working principle of SKPFM is exquisitely simple. The metallic AFM tip, characterized by a work function ϕ_t , is brought in close contact with the sample having a work function ϕ_s (Figure 4.1a). Upon electrical contact, a net current would flow between them until the Fermi levels are aligned and the system reach an equilibrium state, as depicted in Figure 4.1b. In this condition, the difference between the vacuum levels manifests itself as a contact potential difference (V_{CPD}) given by:

$$V_{CPD} = \frac{\phi_t - \phi_s}{-e} \quad (4.1)$$

An electrical force is thus generated between the tip and the sample because of the electric field determined by V_{CPD} . By direct application of an external DC bias (V_{DC}) with the same magnitude as V_{CPD} and opposite polarity, the work function difference is counterbalanced, and the electric force is thus nullified (Figure 4.1c). In the light of equation (4.1), therefore, ϕ_t can be retrieved directly from V_{CPD} measurement, when the tip work function ϕ_t is known.

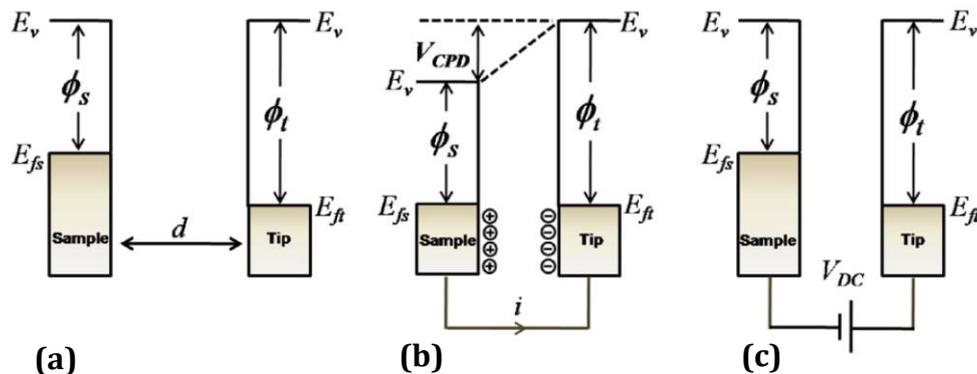


Figure 4.1 Energy levels of the sample and AFM tip for three cases: (a) tip and sample are separated by distance d with no electrical contact, (b) tip and sample are in electrical contact, and (c) external bias (V_{DC}) is applied between tip and sample to nullify the contact potential difference. From [195].

SKPFM is primarily based on the instrumentations of an AFM system which is known to operate either in contact, tapping or non-contact modes [196]. In contact mode, the AFM tip touches the sample surface and the repulsive tip-sample interaction is acquired as a deflection of a laser beam impinging on an optical lever, the so-called cantilever, on which the tip is bonded. The cantilever deflection is monitored and used as a feedback signal that adjusts the relative height of the cantilever in order to leave the magnitude of interaction constant. Point-wise scan data are thus processed to retrieve the topography of the surface. Non-Contact AFM, on the contrary, operates at a relative distance from the sample for which the tip-surface interaction is attractive, while the cantilever is forced to oscillate mechanically at its resonant frequency. The force related to the local interaction between the tip and the surface leads to a variation of the amplitude (Amplitude Modulation or AM-mode) or of the frequency of the oscillation (Frequency Modulation, FM-mode) with respect a reference value. Those variations are used as feedback signals for the z-height control of the cantilever from which the topographical informations of the surface are obtained.

In SKPFM the AFM system operates in non-contact mode and V_{CDP} is typically acquired concurrently with surface topography by applying an AC signal ($V_{ac}(\omega, t)$) plus a DC bias to the oscillating cantilever. The corresponding electrostatic force, acting between the AFM tip and the sample, is given by [188]:

$$F_{es}(z, t) = -\frac{1}{2} \frac{\partial C(z)}{\partial z} [(V_{DC} \pm V_{CPD}) + V_{ac} \sin(\omega t)]^2 \quad (4.2),$$

where z is the direction normal to the sample surface and $\partial C(z)/\partial z$ is the capacitance gradient between the tip and the sample. The \pm depends whether the DC bias is applied to the tip or to the sample, respectively. Equation (4.2) can be decomposed in three different contributions:

$$F_{DC} = -\frac{\partial C(z)}{\partial z} \left[\frac{1}{2} (V_{DC} \pm V_{CPD})^2 \right] \quad (4.3)$$

$$F_{\omega} = -\frac{\partial C(z)}{\partial z} (V_{DC} \pm V_{CPD}) V_{ac} \sin(\omega t) \quad (4.4)$$

$$F_{2\omega} = -\frac{\partial C(z)}{\partial z} \frac{1}{4} V_{ac}^2 [\cos(2\omega t) - 1] \quad (4.5)$$

In these expressions, F_{DC} results in a static deflection of the cantilever, F_{ω} is the term related to the actual surface potential measurements while $F_{2\omega}$ can be employed for a direct estimation of the capacitance. It should be pointed out that equation (4.1) relies on assumptions valid uniquely in the case of a metal/metal system. For a semiconductor surface, the particular behavior of the force versus tip-surface distance variation is linked to the crossover of the characteristic inversion/depletion regimes and to the formation of a space charge layer affecting the effective capacitance of the tip/sample system [197]. In this case, the measured V_{CPD} can be related specifically to the surface potential and it

cannot be directly employed in the determination of the work function of the semi-conductive surface area.

Experimentally, both the topography signal and the electrical force F_{ω} are typically demodulated by means of two separate lock-in amplifiers, as depicted in Figure 4.2. In particular, the V_{CPD} value, for each point on the sample surface, can be measured by applying V_{DC} to the AFM tip, such that the output signal of the lock-in amplifier is nullified and $F_{\omega} = 0$. The AC frequency ω is usually set far away from the main mechanical resonance, at either a second resonant peak of the cantilever or a lower frequency, in order to avoid the cross-talk between the topographic and electrical signals.

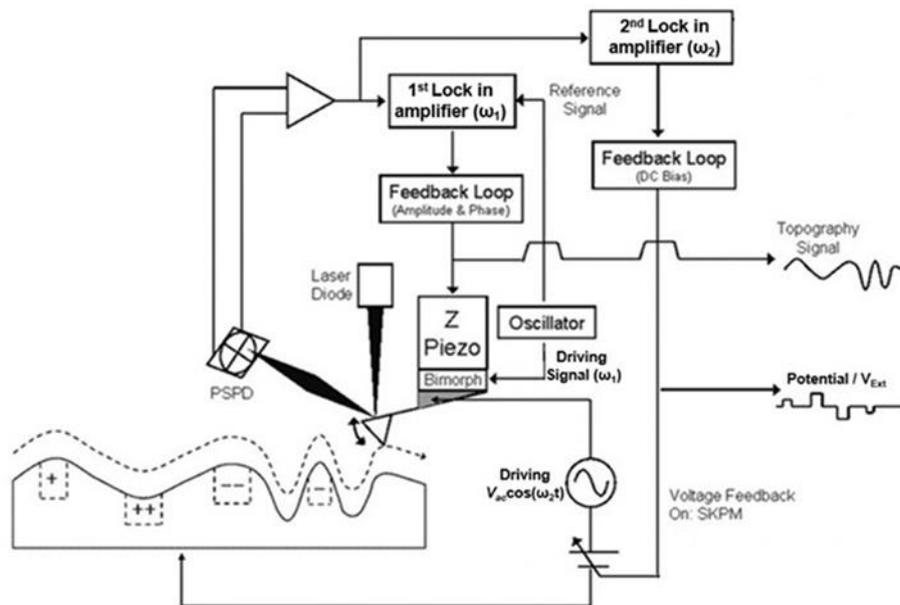


Figure 4.2 Schematic depiction of a typical SKPFM set-up. From [198].

For the determination of contact resistances in perylene diimides OTFTs, reported in the following sections, Amplitude Modulation Scanning Kelvin Probe Force Microscopy (AM-SKPFM) measurements have been performed by a XE-100 Park AFM, equipped with Cr/Au-coated conducting cantilevers (NSC14 Cr/Au MicroMask™). Surface potential profiles were acquired, both in air or in Argon-saturated atmosphere, in dual frequency mode: i.e. acquiring simultaneously both the height profile and the potential profile of the OTFT active channel. The height profile signal is processed by the internal lock-in amplifier of the instrument, demodulating the AC signal received from the oscillating AFM tip locked on its mechanical resonance frequency of ≈ 100 kHz. The potential profile-signal is singled out by means of an external Stanford Research System SR830 DSP Lock-in amplifier using a sinusoidal reference signal with a frequency of 17 kHz and a V_{AC} amplitude between 1 V and 1.5 V. Typical acquired line scans of 512 pixels along 30 μm or 20 μm (depending on the device architecture) result in an approximate dwell time of 39 ms per point (considering a scan frequency of 0.1 Hz per line). Concerning the scan direction, surface voltage profiles under analysis have been acquired with the fast scan

axis always perpendicular to the electrodes edge. This in order to have a symmetric overlap between the cantilever and the electrodes.

4.2 CONTACT EFFECTS IN GOLD-BASED MICROMETRIC DEVICES

Recently we reported a throughout investigation of contact effects in state-of-the-art bottom-contacts/distributed-bottom-gate OTFTs, based on thermally evaporated thin films (25nm) of PDIF-CN2 deposited on HMDS-treated SiO₂ (200nm) substrates [199]. The gold-based architecture is the same as the test-pattern used for the optimization of the organic thin film growth, described in Section 2.7.1. During the acquisition of the surface potential profiles, the OTFTs are biased by means of a Keithley 2400 and Keithley 6517A source-meters that apply the gate-source and drain-source voltages while measuring the corresponding drain-source and gate-source currents, respectively. Typical potential profiles, acquired in linear regime ($V_{gs}=30V$, $0.2V < V_{ds} < 5V$) are reported in Figure 4.3a.

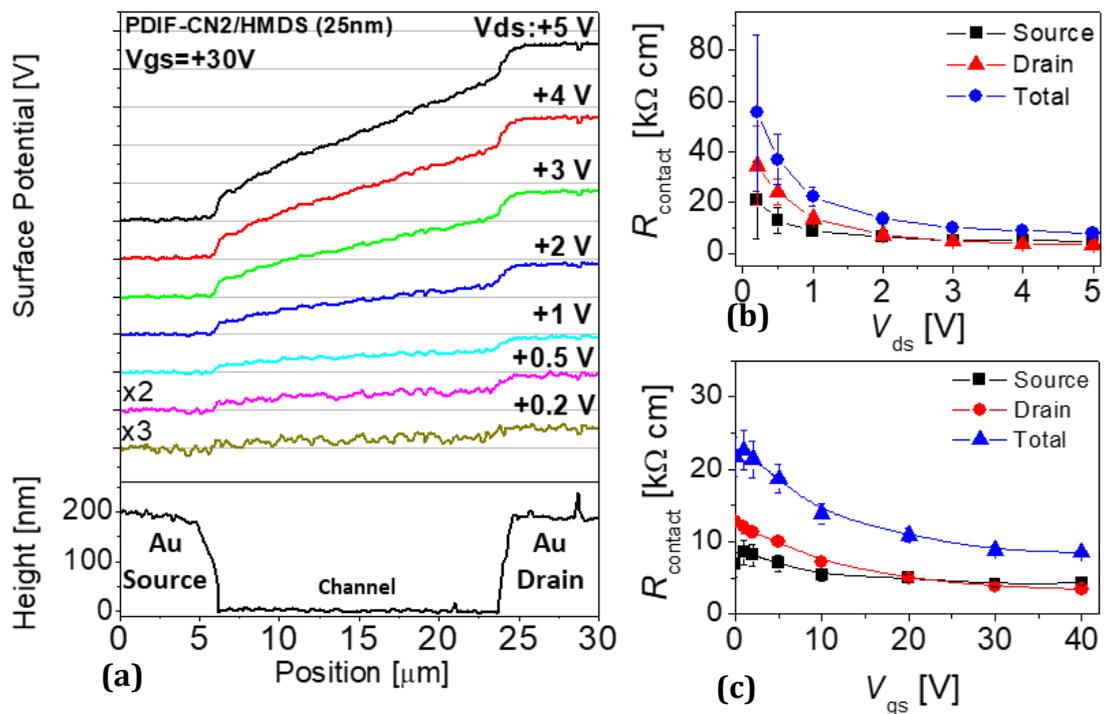


Figure 4.3 (a) Surface potentials for different applied V_{ds} and $V_{gs} = 30$ V, acquired at room temperature and in Argon saturated atmosphere (upper panel), for a PDIF-CN2 micrometric OTFT with gold electrodes. The correspondent topography of the channel is showed in the lower panel where Source electrode is located on the left and Drain electrode on the right. Surface potential profiles in (a) are shifted (and scaled for $V_{ds} = 0.5$ and 0.2 V) for clarity. Major ticks spacing along the y-axis in the upper panel is of 1 V. (b) Behavior of the contact resistances as function of V_{ds} voltage for a fixed gate- source bias ($V_{gs} = 30$ V) and (c) as function of the gate bias for a fixed drain-source potential ($V_{ds} = 5$ V).

Surface voltage distributions reveal that the active channel of the investigated OTFT can be electrically described as the series of three different resistive regions, as discussed in

Section 1.3. The two voltage drops at the metal/organic interfaces (ΔV_s , ΔV_d) manifest the presence of contact effects, while the active channel responds linearly to the externally applied V_{ds} accordingly to the MOSFET model.

After acquiring the voltage profiles, the contact resistance values at the source (R_s) and drain (R_d) electrodes, expressed in $k\Omega \cdot cm$, have been evaluated by simply dividing the corresponding voltage drops (ΔV_s , ΔV_d) by the width-normalized current density I_{ds}/W . The latter is always estimated following the I_{ds} reduction over time caused by the bias stress effect [185,200]. The acquisition of the surface potentials is launched only after the initial rather fast decrease of the current involving about the first 100 seconds and a mean value between the initial and final current is considered: typical variations of $\approx 2\%$ are observed in air for PDIF-CN₂ devices. Hence, the overall $R_{contact}$ contribution is achieved through the sum of the two terms ($R_{contact} = R_s + R_d$).

Results as function of the drain-source and gate-source bias are plotted in Figure 4.3b and Figure 4.3c, respectively. The contact resistance values for the devices under investigation have been found to display a strongly increasing behavior when V_{ds} is decreased. In particular, for $V_{ds} \leq 1V$, the Drain appears to be more affected by the contact resistance phenomenon with $R_d > R_s$. Conversely, for V_{ds} values ranging between 3 V and 5 V, R_s and R_d exhibit comparable values of few $k\Omega \cdot cm$ resulting in $R_{contact} \approx 10 k\Omega \cdot cm$. Beyond the V_{ds} impact, a rather weak dependence of $R_{contact}$ on V_{gs} is found, with typical changes by about 40% for $10V \leq V_{gs} \leq 40V$.

In order to gain further knowledge about the local variability of contact resistances, ΔV_s and ΔV_d have been mapped over 85 different locations of the device, while keeping a fixed polarization ($V_{gs} = +30 V$ and $V_{ds} = +5 V$). The statistical distributions of the voltage drops are reported in Figure 4.4. An average value of 0.6 V and 0.82 V can be inferred for the source and drain electrode, respectively.

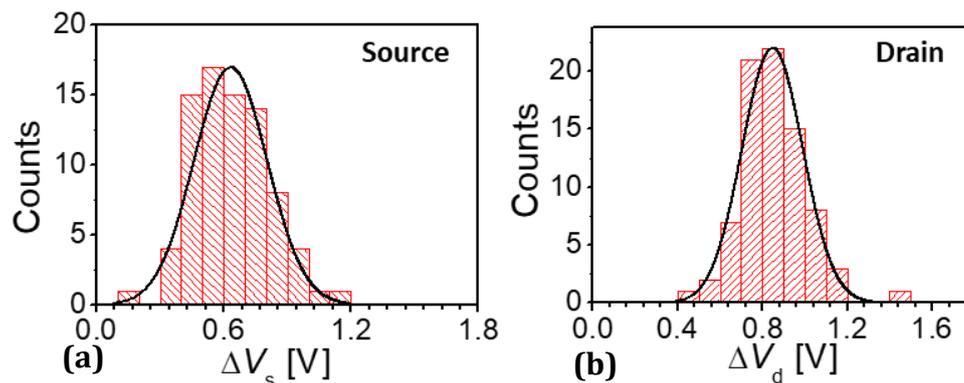


Figure 4.4 Statistical distribution of the voltage drops at (a) the source and (b) drain gold electrodes for a micrometric channel OTFT based on PDIF-CN₂. Fixed applied voltages are $V_{gs} = 30 V$ and $V_{ds} = 5V$.

The effect of the temperature on the contact effects, acquired in linear regime ($V_{gs}=30$; $V_{ds}=+5V$), is reported in Figure 4.5. For $300K \leq T \leq 350K$ a mild decaying behavior for increasing T , with decrements of the order of 18%, is observed for both the source and drain electrodes (Figure 4.5a). On the other hand, the effect of the temperature is much

more evident when referring to the charge transport of the overall active channel. The I_{ds} current undergoes to a rapid growth due to the role of thermally assisted transport properties of PDIF-CN2 (Figure 4.5b). Consequently, the R_c trends are mainly dictated by the Arrhenius-like increment of the current, with an activation energy estimated at 107 meV , giving birth to a general decrement of R_c up to $\approx 50\%$ for temperatures approaching 350K (Figure 4.5c)

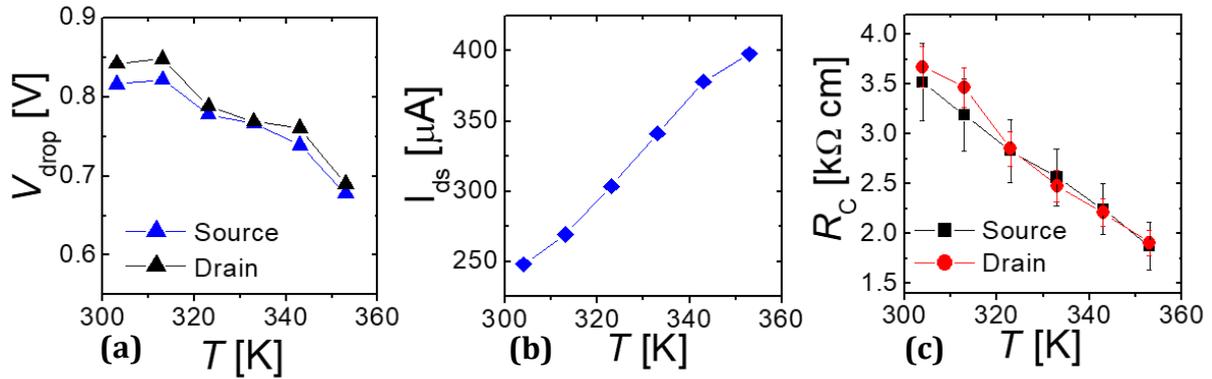


Figure 4.5 (a) Voltage drops as function of the temperature T , at the source and drain electrodes in PDIF-CN2 micrometric OTFT. (b) Drain-source current in linear polarization and (c) corresponding contact resistances. Data have been acquired in Argon-saturated atmosphere.

A similar analysis has been performed for PDI8-CN2 based OTFTs. In this case, the organic semiconductor has been deposited on bare, i.e. not-functionalized, substrates in order to keep the interface structure as simple as possible and to facilitate the comparison with data retrieved from graphene-based samples discussed in the next section. From electrical characterization in vacuum conditions, field-effect mobility in saturation regime of the order of $\mu_{FET} \approx 2 - 4 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ have been extracted from transfer characteristics, indicating the effective quality of the obtained thin films. Surface potential profiles acquired in air and contact resistances as function of the applied voltages (V_{ds} and V_{gs}) are reported in Figure 4.6. Interestingly, in the PDI8-CN2 case, charge injection appears to be favored over the extraction at the drain electrode, as suggested by the presence of smaller voltage drops at the source with $+0.05\text{V} \leq \Delta V_{\text{source}} \leq +0.3\text{V}$ for $+0.2 \leq V_{ds} \leq +5\text{V}$ (Figure 4.6a). The overall contact resistance therefore follows mainly the functional trend of R_D . Values ranging between $+0.2\text{V} \leq \Delta V_{\text{drain}} \leq +0.8\text{V}$ are observed, corresponding to minimum values of about $R_{\text{total}} \approx 40\text{ k}\Omega\text{ cm}$. Despite the presence of a factor x4 respect to the PDIF-CN2 devices, however, it should be pointed out that the calculated values of R_c are strictly dependent on the overall transport properties of the entire active channel. Considering $R_c = \Delta V / I_{ds}$, it is thus clear that PDI8-CN2 shows a more robust R_c contribution since it has lower I_{ds} , although voltage drops can be considered comparable to the PDIF-CN2 case (Figure 4.4).

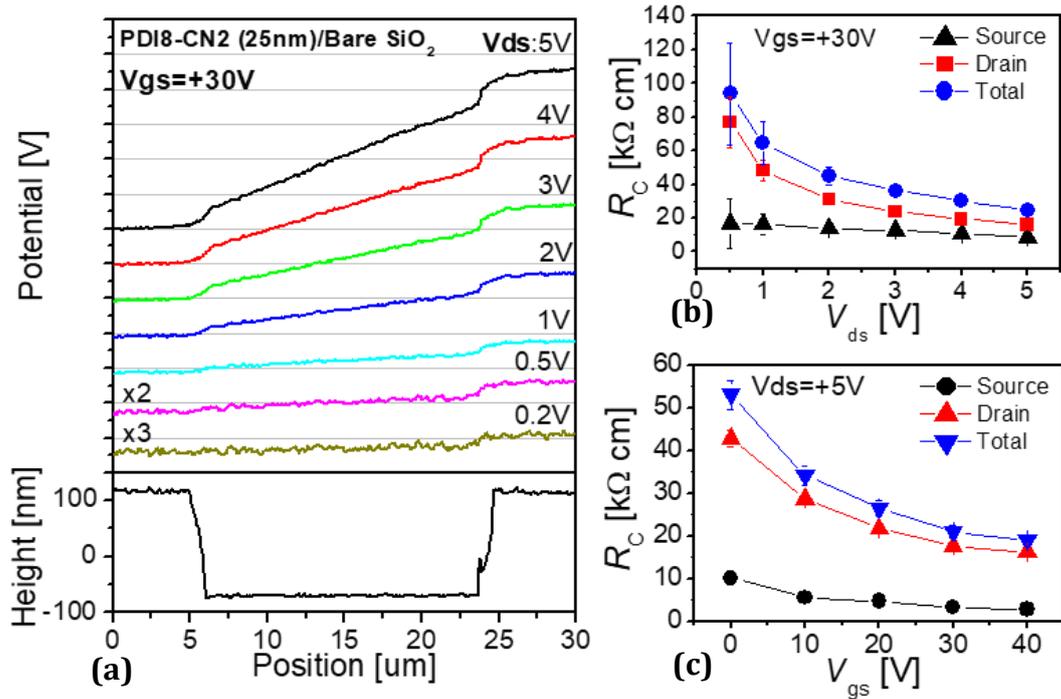


Figure 4.6 (a) Surface potential profiles of a micrometric PDI8-CN2 OTFT, acquired in air via SKPFM, for different applied drain-source voltages ($V_{gs}=+30V$). The lower panel shows the corresponding channel topography. Curves are shifted for clarity while the y-axis spacing is of 1V. (b) Contact resistances as function of V_{ds} extracted from voltage drops at the electrodes evaluated from (a). (c) Contact resistances as function of the gate potential

The influence of the organic thin film thickness (t) has been investigated considering three different samples with $t=12nm, 25nm, 40nm$. As it can be observed from Figure 4.7, surface voltage profiles show an increasing source contribution for increasing thickness, counterbalanced by progressively decreasing voltage drops in correspondence of the drain electrode. This qualitative picture reflects on the response of the voltage drops to the applied V_{ds} , as reported in Figure 4.7b and c. While maximum ΔV_{drain} values decrease from 0.8V to 0.2 V for $V_{ds} = 5V$, sharing a similar saturating trend for every t , the source electrode shows an exponential increase of ΔV_{drain} in correspondence of $t=40nm$ with values as high as $\approx 1.9V$ for $V_{ds}=+5V$.

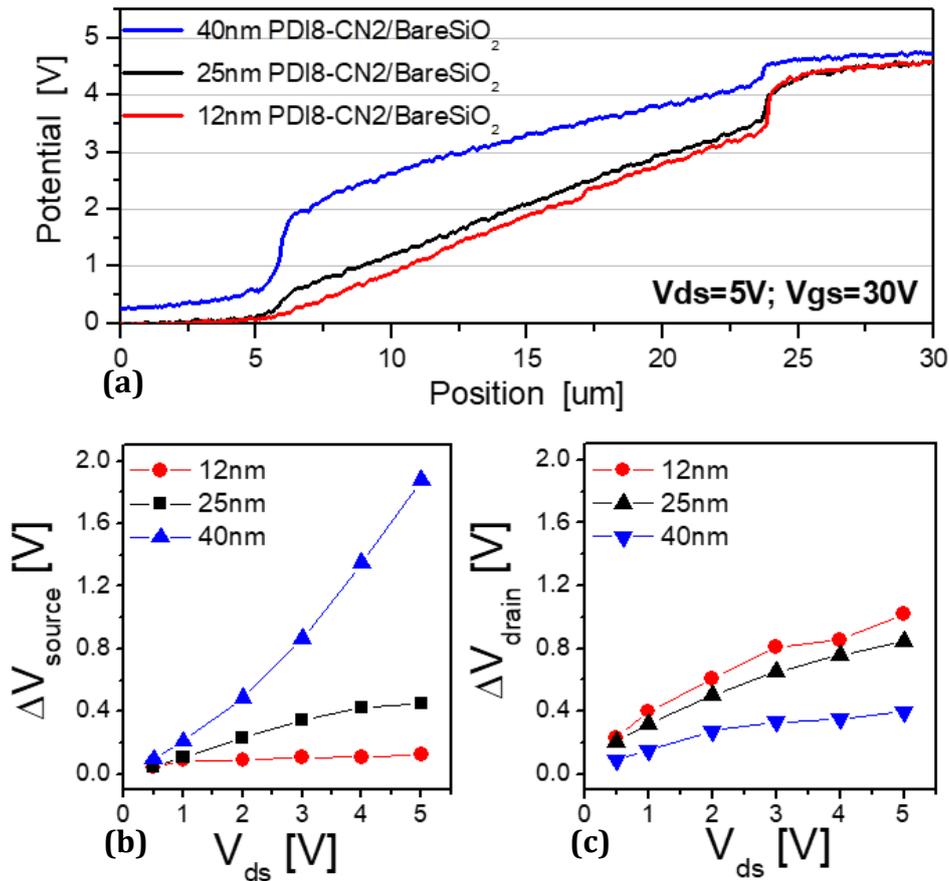


Figure 4.7(a) Surface voltage profiles of OTFTs with gold electrodes, based on PDI8-CN2 thin films deposited on bare SiO₂ substrates. Different organic thin film thicknesses have been considered. Voltage drops extracted at (b) the source and (c) the drain electrode as function of the applied V_{ds} .

The observed phenomenology can be addressed by considering the thin film morphology of the PDI8-CN2, especially in the vicinity of the gold electrodes. Referring to the NC-AFM analysis reported in Figure 4.8, for all the considered thicknesses, molecular terraces with a height of approximately 1.8nm are clearly observable, suggesting the polycrystalline order of the organic solid. It is possible to distinguish the different stages of thin film growth resulting in different grain dimensions (Figure 4.8d-f). The rms roughness (σ_{rms}) increases from 1.3nm for $t=12\text{nm}$ to $\sigma_{rms}=1.6\text{nm}$ for $t=25$ and $\sigma_{rms}=1.8\text{nm}$ in correspondence of $t=40\text{nm}$, due to progressive growth of the PDI8-CN2 crystallites and their tendency towards a more three-dimensional profile. These considerations still hold when referring to the gold/organic interfaces reported in Figure 4.8a-c where organic thin films are observed to be contiguous with the electrode edges. Despite this, few hypotheses can be made regarding the observed phenomenology for the voltage drops at the electrodes. First, the general increase of σ_{rms} reflects on the statistical distribution of grain boundaries in the proximity of the gold contact. Respect to the energetic considerations typically assessed for contact effects (see Section 1.3), a more pronounced effect of the morphological disorder therefore cannot be excluded. Secondly, in this particular architecture, the gold electrode is not characterized by an abruptly terminated edge: a sloping border protruding for more than 1 μm can be observed referring to Figure

4.8a-c, probably due to photomask shadowing effects. It is thus clear that a thicker organic film will cover the gold electrode edges at a greater extent. On the other hand, this covered sloping areas, despite directly connected to the active channel, especially for thicker films, are shielded from the applied gate bias resulting in poorer, or even null, charge accumulation. This is, of course, particularly detrimental for the charge carrier injection occurring at the source electrode.

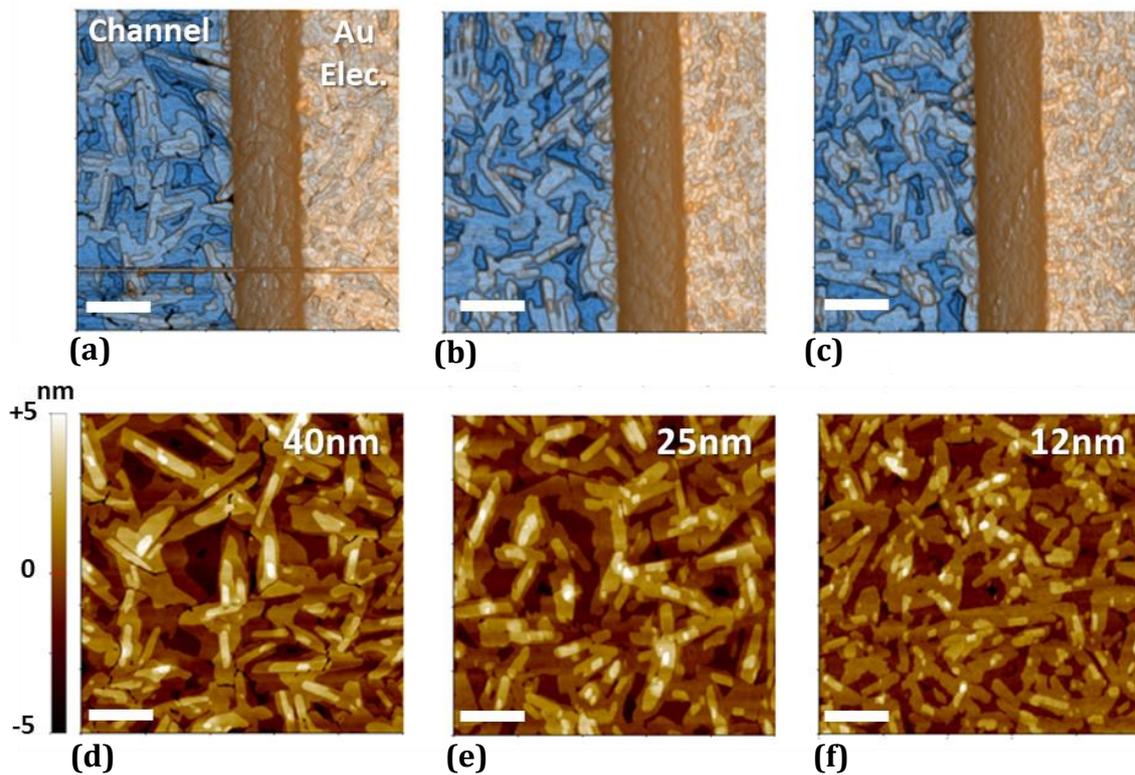


Figure 4.8 (a)-(c) Non-Contact AFM topographies, reported in enhanced color mode, of the organic/gold interfaces for different thin film thicknesses, respectively $t=40\text{nm}$, 25nm and 12nm . Gold electrodes thickness is of about 170nm . It is possible to observe the presence of a gold sloping border in between the organic active channel and the electrode (dark orange areas). (d)-(f) Corresponding typical morphologies acquired within the active channel of the organic transistors. For all the images, the white markers are $1\mu\text{m}$.

4.3 MICROMETRIC DEVICES WITH CVD-GRAPHENE ELECTRODES

For the analysis of the surface potential in the case of graphene-based micrometric devices described in Section 2.6, two different samples have been considered. In this case, PDI8-CN2 thin films have been deposited by means of OMBD with two different thicknesses: 27nm and 43nm. Deposition rate and substrate temperature are the same for both samples ($R=0.7\text{nm}/\text{min}$, $T_{\text{sub}}=94^\circ\text{C}$).

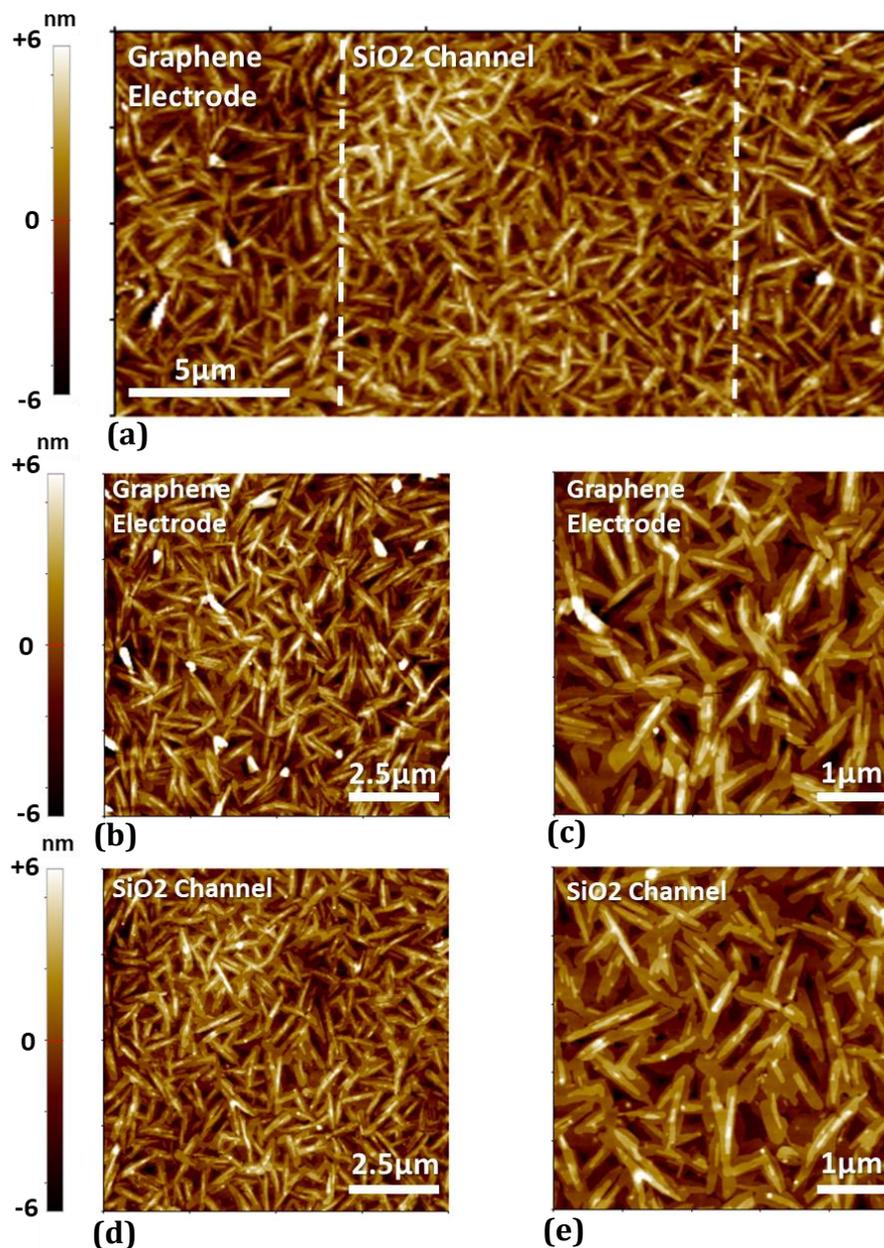


Figure 4.9 NC-AFM analysis of a 43nm thick PDI8-CN2 thin film deposited via OMBD on the graphene-based micrometric OFET layout ($L=10\ \mu\text{m}$, $W=3\text{mm}$ with an interdigitated electrode architecture and distributed gate electrode). The SiO₂ substrate (300nm) is not treated with HMDS in this case. (a) Overview of the OFET channel. The white dashed lines help to distinguish the edges of the graphene electrodes. (b) $10\times 10\ \mu\text{m}^2$ and (c) $5\times 5\ \mu\text{m}^2$ topographies showing the thin film morphology on the graphene electrode. (d) and (e) individuates the same analysis of the PDI8-CN2 morphology within the SiO₂ channel.

Differently from the previously discussed case of gold-based architectures, organic thin film morphology of the samples under analysis shows essentially no impact of the graphene electrodes on the PDI8-CN2 growth. Referring to Figure 4.9a, in fact, the contact edges are barely discernible, and the interfaces are hinted only by a greater presence of sparse impurities: presumably resist residues characterizing only the graphene surface (Figure 4.9b and c). Nevertheless, the overall morphology, both within the active channel (Figure 4.9d and e) and on the electrodes, is totally compatible with what observed in standard gold-based layouts of Section 4.2. Organic thin films are characterized by the presence of elongated crystallites with flat molecular terraces with a stepped morphology with heights of roughly 1.8nm, in accordance with the unit cell c-axis length of PDI8-CN2.

4.3.1 Transport properties of CVD-graphene electrodes

Transport properties of the graphene electrodes have been tested in GFET configuration. In this case, CVD-graphene (Graphenea, Inc.) is transferred on 300nm thick thermal SiO₂ acting as dielectric ($C_{ox} \approx 11.05 \text{ nF/cm}^2$). In analogy with devices of Section 3.1.4, transfer characteristics ($I_{ds}-V_{gs}$) of micrometric graphene strips ($W=2\mu\text{m}$, $L=4\mu\text{m}$) have been acquired in vacuum for pristine graphene, after two subsequent thermal annealing performed in vacuum at 375K for 1 hour and at 425K for 4 hours, respectively, and after the deposition of the PDI8-CN2 thin film. Results are plotted in Figure 4.10.

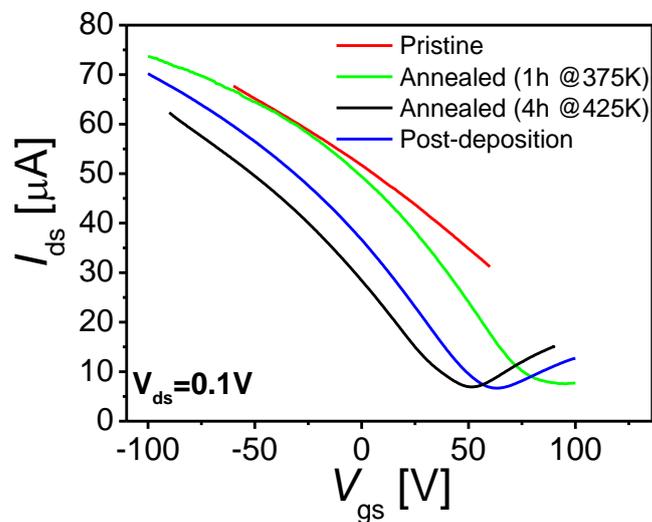


Figure 4.10 Transfer curves for a micrometric strip ($L=4\mu\text{m}$, $W=2\mu\text{m}$) of CVD-graphene in GFET configuration (Commercial CVD-Graphene by Graphenea, Inc. transferred on 300nm SiO₂ acting as distributed gate with $C_{ox} \approx 11.05 \text{ nF/cm}^2$). Curves have been acquired for pristine graphene, after a thermal annealing, in vacuum, at 375K for 1 hour, after 4 hours at 425K and after the deposition of 43nm thick PDI8-CN2 thin film.

Pristine samples appear to be heavily p-doped with neutrality points V_D deeply shifted towards positive gate voltages (outside of the considered voltage range). The subsequent thermal annealing procedures partially restore the conditions of graphene towards an intrinsic state: a shift of the neutrality points towards lower gate voltages with a final $V_D =$

50V is measured after keeping the sample in vacuum at 425K for 4 hours. Moreover, in accordance with results of Section 3.2.1, the interaction with the electron-withdrawing group of perylene diimides influence the final doping state of the graphene. After the organic deposition, neutrality points are typically observed to settle around $V_D \approx +57V$. Charge carrier mobilities, estimated by DTM and FTM methods (see Section 1.6.2) are reported in Figure 4.11. Maximum values, ranging from $\mu_{FET} \approx 7 \times 10^2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for holes to $\mu_{FET} \approx 2 \times 10^2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in the case of electrons, are inferred from the calculated DC transconductance of GFETs (Figure 4.11a). By including the effect of contact resistances through the fitting curve of equation (1.29), gate-independent hole ($\mu_p = 786 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and electron mobility ($\mu_n = 1162 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), as well as and residual charge density ($n_0 = 1.5 \times 10^{12} \text{ cm}^{-2}$), can be obtained from the total resistance curves of the devices ($R_{tot} = V_{ds}/I_{ds}$)(Figure 4.11 b).

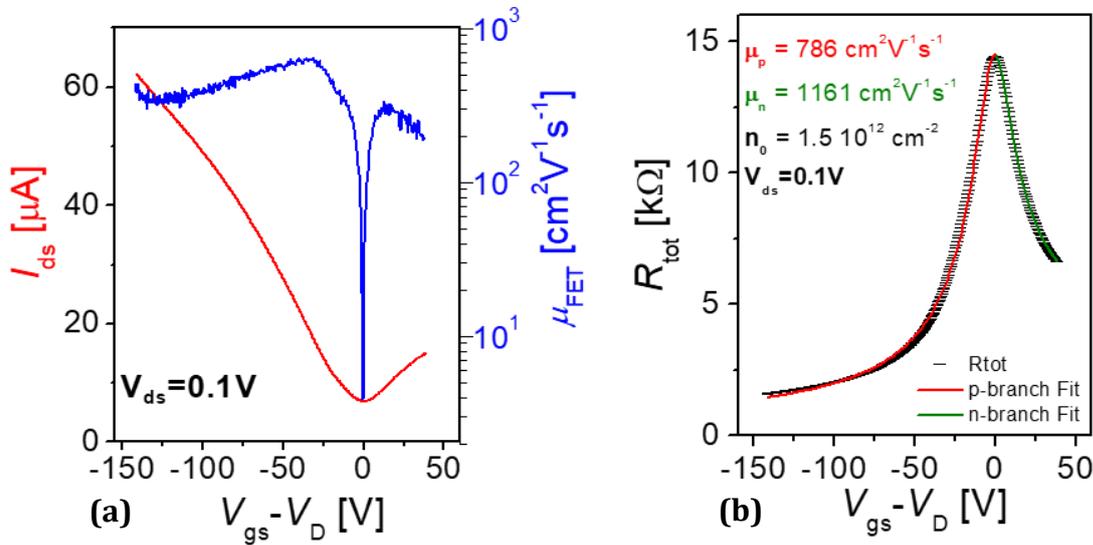


Figure 4.11 (a) Charge carrier mobility (blue solid line) for both hole and electrons extracted starting from transfer characteristics (red line) for a micrometric strip of CVD graphene in GFET configuration. (b) Total resistivity of the same device fitted via equation (1.29) from which gate-independent hole (μ_p) and electron mobility (μ_n), as well as and residual charge density (n_0) can be estimated. For both graph $V_D = +50V$.

4.3.2 Electrical characterization

After the PDI8-CN2 deposition, micrometric OFETs have been electrically characterized by acquiring both transfer and output curves. Current-voltage characteristics acquired in vacuum conditions are shown in Figure 4.12: in this case, reported data refer to a 27nm thick PDI8-CN2 film.

The absence of a proper functionalization of the SiO_2 substrate has a great influence on overall electrical characteristics of the transistors, especially in terms of threshold voltages. On-set values as low as $V_{th} = -50V$ are in fact typically observed. In addition to this, modest hysteresis phenomena are present as well, with dissimilar current values measured between forward and backward V_{gs} sweeping, mostly ascribable to charge trapping phenomena at the dielectric/organic interface.

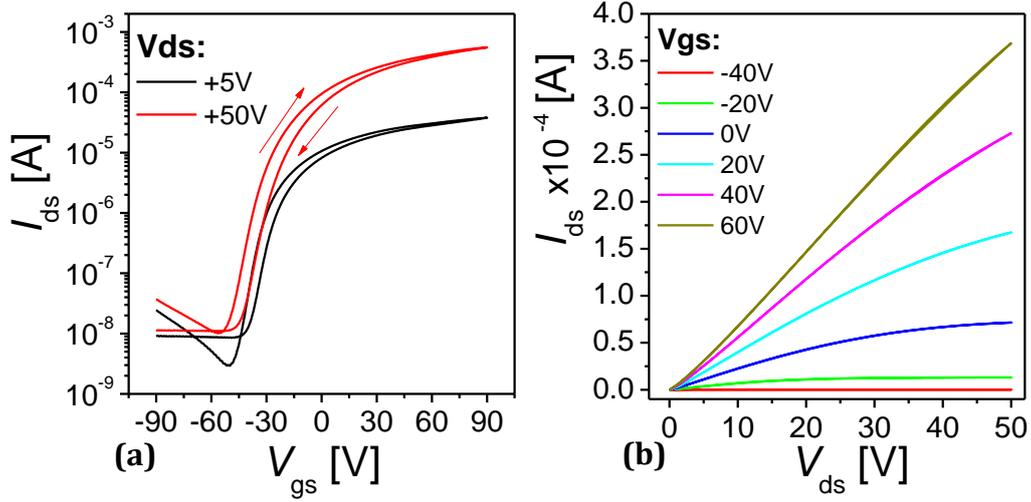


Figure 4.12 Transfer characteristics acquired in vacuum for a PDI8-CN2 based micrometric OFET with CVD-Graphene electrodes. In this case, two different V_{ds} values have been considered. (b) Corresponding output characteristics, acquired in vacuum, measured for $-40 \leq V_{gs} \leq +40V$ with $\Delta V_{gs} = 20V$.

Despite the aforementioned issues, electrical performances of graphene-based devices are interestingly comparable to those obtained for state-of-the-art PDI8-CN2 OFETs ($L=20\mu m$, $W=1.1cm$) with HMDS-functionalized substrates and standard gold electrodes. A comparative analysis can be made referring to Figure 4.13 where field effect mobilities in linear ($V_{ds}=+5V$) and saturation regime ($V_{ds}=+50V$) are considered. Similar μ_{FET} values are observed, with shared maxima at $\mu_{FET} = 1 \times 10^{-2} cm^2 V^{-1} s^{-1}$ and $3 \times 10^{-2} cm^2 V^{-1} s^{-1}$ in linear and saturation regime, respectively.

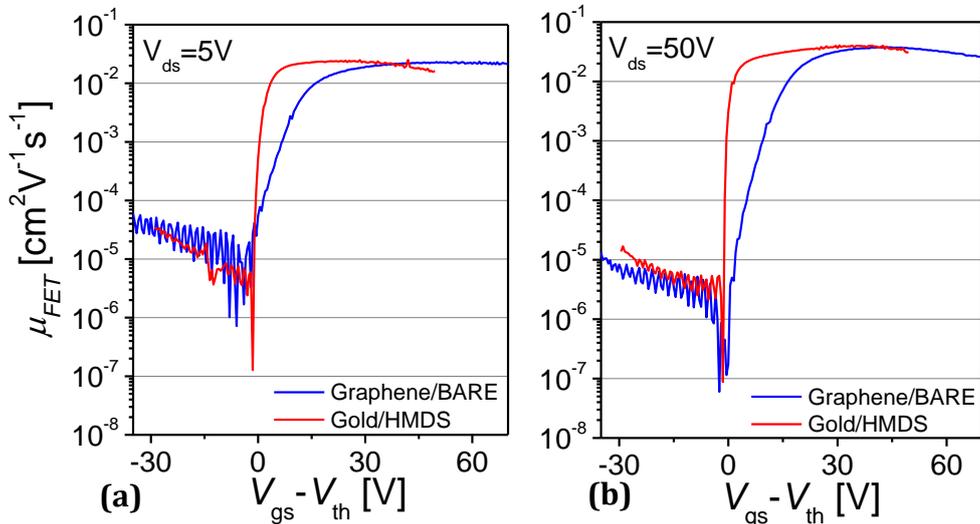


Figure 4.13 Comparative analysis of the field-effect-mobility, acquired in vacuum conditions, evaluated for micrometric PDI8-CN2 OFET with graphene electrodes and un-treated SiO_2 substrates ($L=10 \mu m$, $W=3mm$) and with gold electrodes and HMDS-functionalized dielectric interface ($L=20\mu m$, $W=1.1cm$). (a) and (b) plots individuate $\mu_{FET} V_s \cdot (V_{gs} - V_{th})$ curves calculated in linear ($V_{ds}=+5V$) and saturation regime ($V_{ds}=+50V$), respectively. For the graphene-based architecture, threshold voltages of $\approx -50V$ have been taken in account for the comparison.

Gate-dependent mobilities differ mostly in terms of on-set slopes in the vicinity of $V_{gs} - V_{th} = 0V$ for which the effect of the dielectric thicknesses, as well as of the different W/L ratios, are clearly observable.

Before introducing the results of the kelvin probe analysis on graphene electrodes, it should be reminded that the latter measurements are typically performed in air. A preliminary analysis, accounting for the influence of atmospheric contaminants, is thus clearly needed. At this regard, it is possible to refer to the comparison between output curves acquired in vacuum and under atmospheric exposure reported in Figure 4.14.

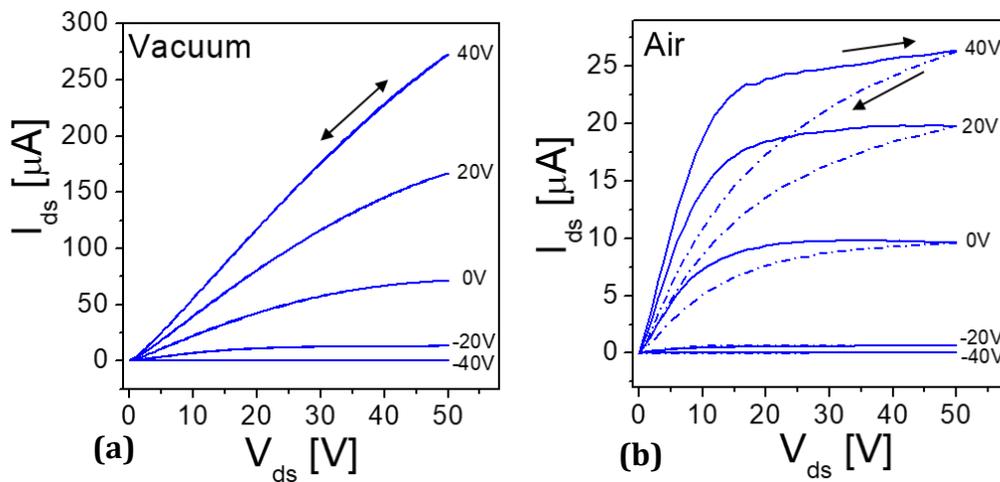


Figure 4.14 (a) Output current-voltage characteristics for graphene-based PDI8-CN2 micrometric OFET, acquired in vacuum ($P \approx 10^{-5}$ mbar), for $-40V \leq V_{gs} \leq +40V$. (b) Output curves acquired in air for the same gate-source voltage interval. Dot-dashed lines individuate the I_{ds} values acquired for V_{ds} sweeping backwards.

Functional trend of the currents appears to be heavily influenced by atmospheric contaminants, with current saturation achieved for much lower V_{ds} ($\approx +10V$) and large current hysteresis opening up for backwards sweeping voltages. Moreover, variations of one order of magnitude in terms of overall drain-source currents are typically obtained considering similar applied V_{gs} .

4.3.3 Surface Voltages Profiles and Contact Resistances via SKPFM

Concerning the SKPFM investigation of surface voltage profiles for graphene-based architectures, the qualitative picture suggested by Figure 4.15 appears quite different from gold-based architectures investigated in Section 4.2. Surface voltage profiles, in this case for the 40nm thick PDI8-CN2 thin film, indicate the presence of steep voltage drops localized mostly in correspondence of the grounded source electrode. No contact effects are observed in correspondence of the drain interface where the electrode influence is suggested only by the presence of a different slope of the surface voltages starting from approximately 15 μm .

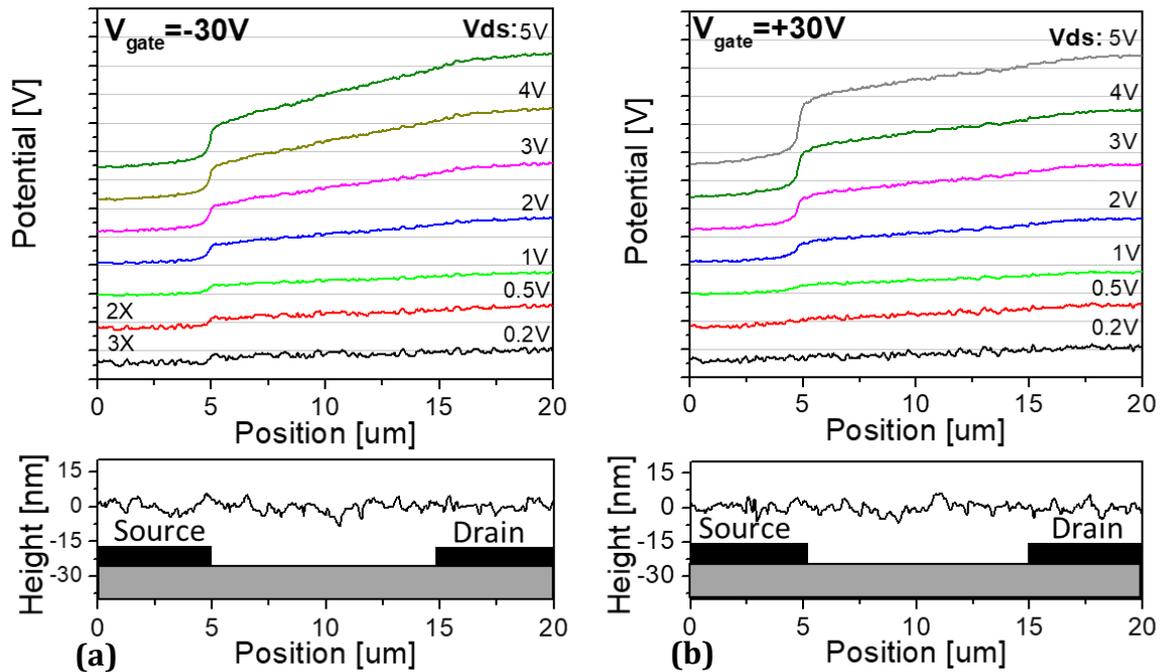


Figure 4.15 Surface voltage profiles, acquired via SKPFM, for the PDI8-CN2/Graphene-Electrodes micrometric OFET ($L=10\ \mu\text{m}$, $W=3\text{mm}$). Applied drain-source voltages range from 0.2V to 5V. Gate voltages are fixed to (a) $V_{\text{gs}}=-30\text{V}$ and (b) $V_{\text{gs}}=+30\text{V}$. Lower panels individualize the NC-AFM topography of the device channel. Curves are shifted for clarity and major ticks of the y-axis is of 1V.

The ongoing analysis will thus focus mainly on the contact effects observed on source electrodes. The response of voltage drops to transversal electric field (V_{ds}) can be observed in Figure 4.16, where results from graphene-based sample are compared with those obtained in the gold case, for different considered PDI8-CN2 thickness. For graphene electrodes, similar trends are observed in terms of ΔV_{source} as function of V_{ds} , by varying the film thickness: voltage drops appear to grow exponentially with the applied transversal field, similarly to the case of 40nm thick film and gold-electrodes.

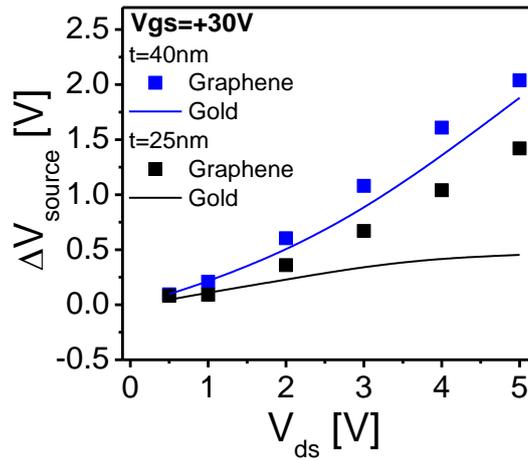


Figure 4.16 Comparison of measured source voltage drops, at a fixed V_{gs} , between graphene and gold electrodes with different organic thin film thickness (40nm and 25nm).

For the 40nm thick film, contact resistances are reported in Figure 4.17a. In this case a wider V_{ds} range has been considered. The functional trends appear to differ significantly from the case of gold electrodes, with values diverging for increasing V_{ds} and $V_{\text{gs}} > 0$. It should be pointed out that in this case, a wider bias range is considered, and the currents appear to saturate (Figure 4.17b). Focusing on the values in correspondence of $V_{\text{ds}} = 5\text{V}$ values of the order of $80\text{ k}\Omega < R < 180\text{ k}\Omega$ are obtained.

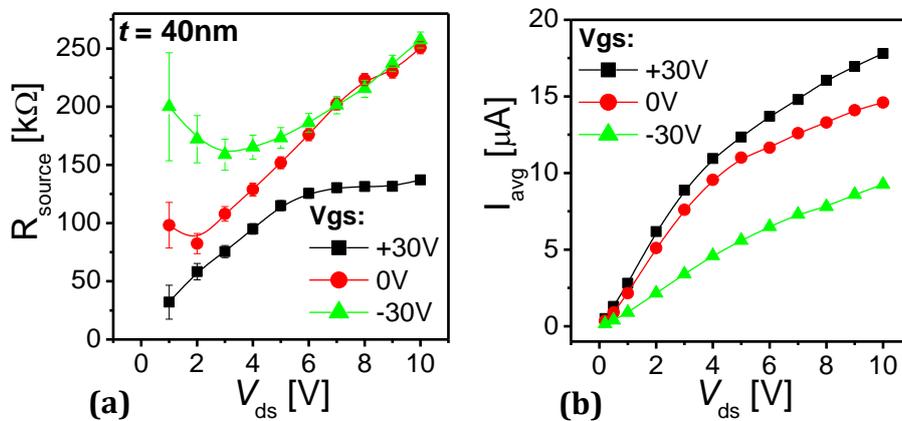


Figure 4.17 (a) Calculated contact resistance at the source electrodes for different applied gate biases. (b) Corresponding output curves obtained considering the average current values used for the determination of R_{source} .

Considering the response of the surface voltage distributions to V_{gs} , as reported in Figure 4.18a, it is possible to note that the effect on the source electrode appears to be much more robust with respect the gold case. A decrease of more than one order of magnitude is observed in terms of R_{source} , with values $650\text{ k}\Omega \leq R_{\text{source}} \leq 34\text{ k}\Omega$ for $-60\text{V} \leq V_{\text{gs}} \leq +40\text{V}$ (Figure 4.18c). A corresponding voltage drop increase from 0.35V to 0.9V is observed in the same gate-source range (Figure 4.18b). It should be noted that, in this case, on-set voltages of -60V are measured for the graphene-based OFET under analysis.

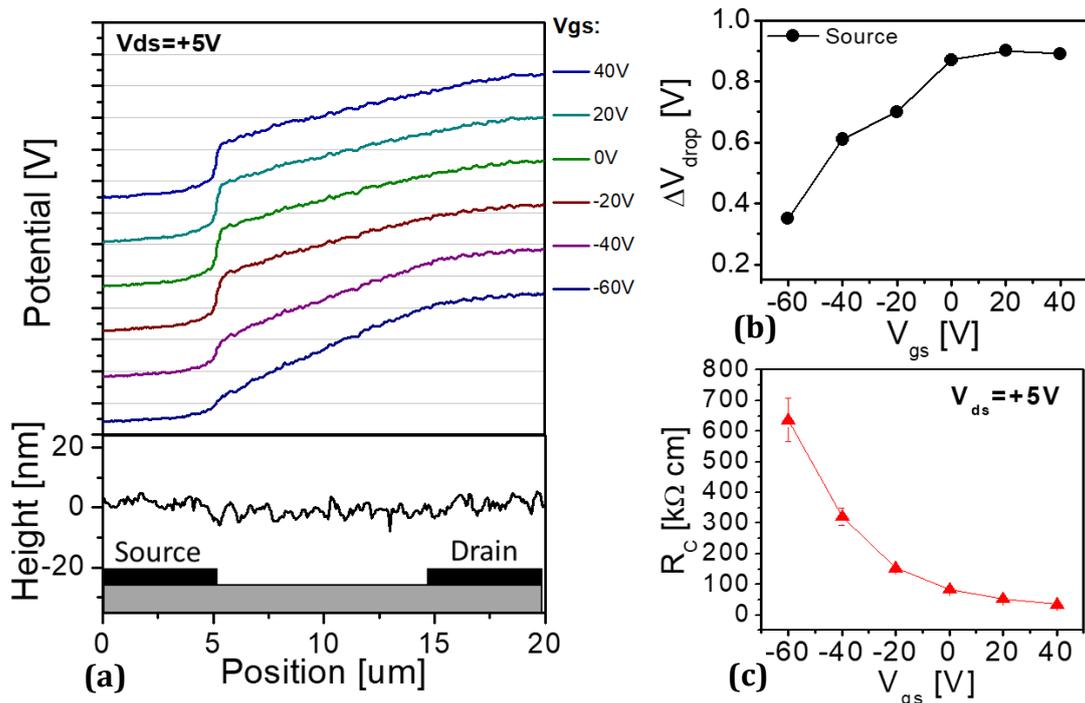


Figure 4.18 (a) Surface voltage profiles for the graphene-based PDI8-CN2 micrometric OFET, acquired for different V_{gs} values. Lower panel individuates the thin film morphology over the entire active channel. (b) Voltage drops in correspondence of the source electrode, as function of V_{gs} . (c) Calculated contact resistance at the source electrode, as function of V_{gs} , obtained from voltage drops of (b).

The effect of the temperature on the contact effects has been addressed with a procedure similar to Section 4.2 for PDIF-CN2 samples and gold electrodes. In this case, surface voltage profiles, over the 27nm PDI8-CN2 thin film, have been investigated for $300K \leq T \leq 360K$ for a fixed V_{gs} and V_{ds} (+30V and +5V, respectively). Results are reported in Figure 4.19. In contrast with results obtained in the case of gold electrodes (Figure 4.5), graphene-based devices appear to be much more affected by temperature with ΔV_{source} varying from values as high as $\Delta V_{source} = +2V$, at room temperature, to $\Delta V_{source} \approx +1.45V$ at $T = 360K$. For this sample, the effect on the drain electrode has been considered as well. More in detail, the voltage slopes (ΔV_{slope}) have been tracked as function of the temperature (Figure 4.19c): a sigmoidal growth is observed with ΔV_{slope} increase for growing T .

Lastly, contact resistances have been calculated starting from ΔV_{slope} and ΔV_{source} , in addition to the average current values evaluated as function of T (Figure 4.20). Differently from what reported in Fig for gold-based architectures, the prominent decrease of R_c here is not purely dictated by the exponential increase of the channel current (Figure 4.20a). Consequently, also considering the drain contribution, a steep reduction of $R_c(T)$ is observed with final values as low as $R_c \approx 40k\Omega$ for $T = 360K$ (Figure 4.20b).

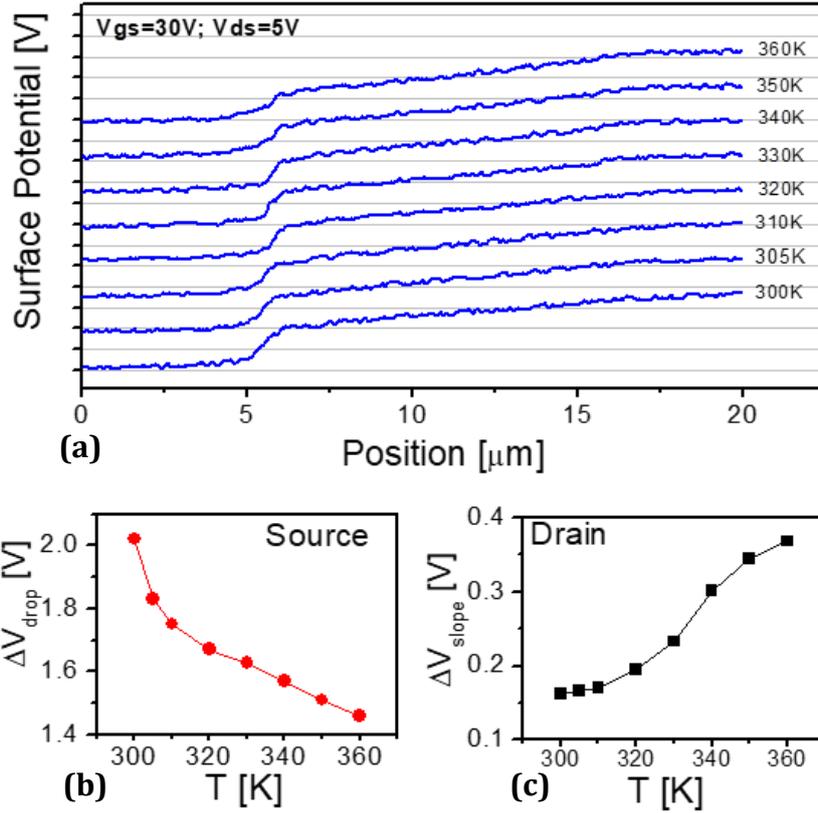


Figure 4.19 (a) Surface voltage profiles acquired via SKPFM for the micrometric OFET based on PDI8-CN2 thin film (27nm) and graphene electrodes. The curves have been acquired by varying the temperature with $300\text{K} \leq T \leq 360\text{K}$. (b) Voltage drop at the source electrodes extracted from profiles reported in (a) and (c) Voltage slope variations observed at the drain electrode as function of the temperature.

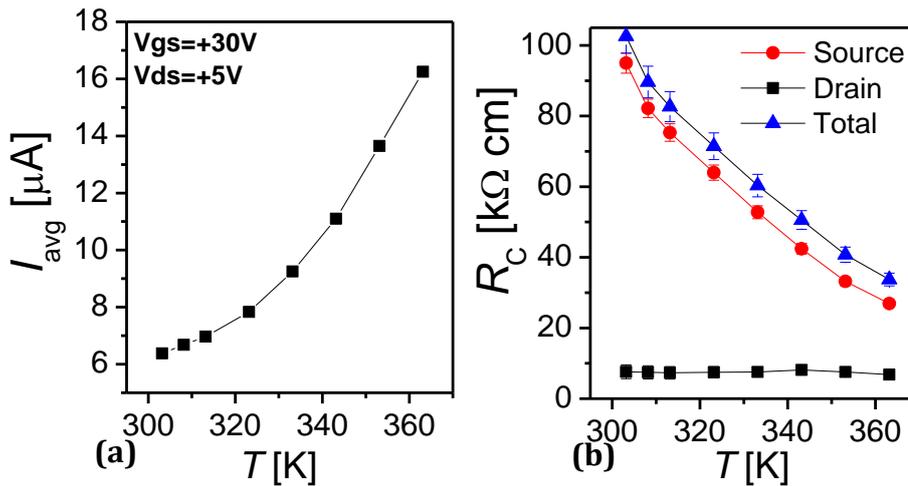


Figure 4.20 (a) Average current, acquired in air for fixed applied biases ($V_{\text{gs}}=+30\text{V}$; $V_{\text{ds}}=+5$) as a function of the temperature (T). (b) Contact resistances calculated as function of the temperature for the PDI8-CN2 thin film (27nm) micrometric OFET with graphene electrodes.

4.4 SURFACE SPECTROSCOPY VIA UPS/XPS

The Photoelectron Spectroscopy (PES) is a widely employed class of surface sensitive techniques that utilize photo-ionization and analysis of the kinetic energy distribution of the emitted photoelectrons to study the composition and electronic state of the surface region of a sample. The working principle is based on the photoelectron effect, where electrons are emitted from matter (metals and non-metallic solids, liquids or gases) as a consequence of their absorption of energy from electromagnetic radiation with a frequency greater than a critical threshold frequency. The emitted photoelectrons have kinetic energy E_{kin} determined by the Einstein relationship:

$$E_{kin} = h\nu - E_b - \phi_{sample} \quad (4.6),$$

where $h\nu$ is the energy of the incident radiation, E_b the binding energy of the emitted electrons and ϕ_{sample} is the work function of the sample. Depending on the excitation photon energies, PES is usually classified as ultraviolet and X-ray photoelectron spectroscopy, UPS and XPS, respectively.

This last section is devoted to the description of PES experiments aimed to the investigation of the Organic/Graphene interface. The analysis has been performed at the IMEM-CNR laboratories in Trento (Italy), in collaboration with Dr. Roberto Verucchi and Dr. Lucrezia Aversa.

As reported in the following discussion, UPS and XPS analysis have been performed on several PDI8-CN2 and PDIF-CN2 thin films deposited via OMBD on SiO₂(300nm)/CVD-graphene substrates (Graphenea, Inc.). The graphene/organic interface properties were evaluated by analyzing film deposited with two selected thicknesses (1nm and 3nm), for both molecules, in order to represent sub monolayer and single monolayer coverages. NC-AFM topographies of ultra-thin organic films are reported in Figure 4.21. The nucleation of organic molecules is clearly influenced by the presence of graphene wrinkles or defect around which the molecular condensation appears to take place. For PDIF-CN2 samples, from Figure 4.21a and b coverages of 43% and 90% have been determined for $t=1\text{nm}$ and $t=3\text{nm}$, respectively. In the case of PDI8-CN2 thin films, for $t=1\text{nm}$ and $t=3\text{nm}$, the corresponding coverages are 24% and 86%, respectively. Lastly, a 5x5 mm² substrate with a pristine CVD-graphene sheet has been used as reference sample. Similarly, for both molecules, 25 nm thick films deposited on a SiO₂ substrate (200nm) are used for the acquisition of reference spectra.

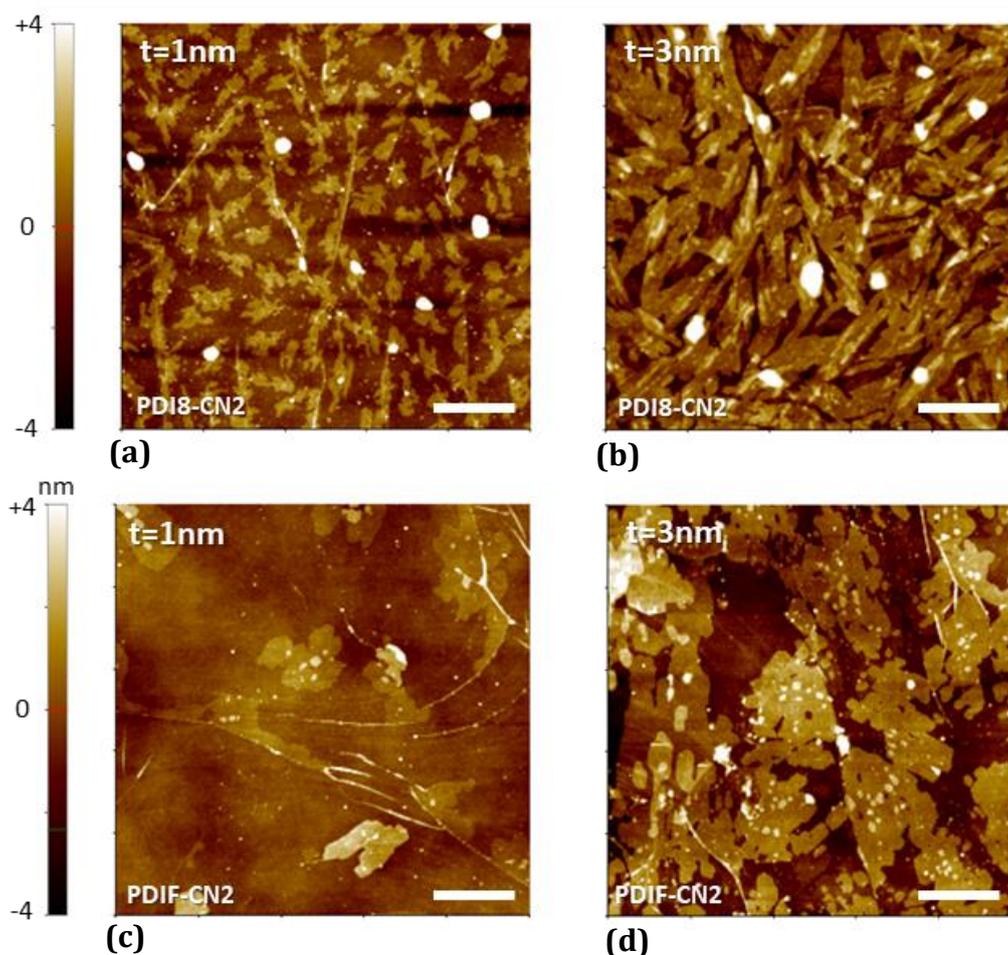


Figure 4.21 (a) and (b) NC-AFM topographies of PDI8-CN2 thin films deposited via OMBD on CVD-graphene sheets. Nominal thicknesses are $t=1\text{nm}$ and $t=3\text{nm}$, respectively. (c) and (d) individuate the same AFM analysis in the case of PDIF-CN2 thin films with equal nominal thicknesses. White markers are of $1\mu\text{m}$.

4.4.1 X-ray photoelectron spectroscopy

XPS is commonly used to investigate high binding energy of deep lying localized occupied states, that is core level region. The exact binding energy of the core levels gives valuable information on the chemical environment and bonding configuration of specific atom species. Hence, XPS is an information-rich method which provides qualitative and quantitative information on all the elements present on the surface (with the exception of H and He).

The process is schematically sketched in Figure 4.22. The electrons generated from a core level leave the surface with a kinetic energy that depends, in a first approximation, on the initial photon energy (100 eV and above), the binding energy and the work function of the solid.

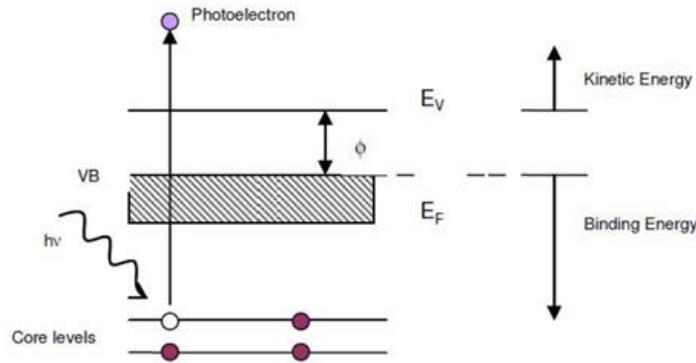


Figure 4.22 Schematic depiction of X-ray photoelectron emission process.

Elemental characterization is possible due to the intrinsic uniqueness of each atom electronic configuration, i.e. by evaluating the Binding Energy. Quantitative analysis can be performed measuring the peak area associated to an element, weighted by a sensitivity factor that takes into account the excitation efficiency of each element. For a homogeneous sample with an isotropic elastic diffusion of the photo-emitted electrons, the photocurrent intensity related to the *i*-species can be expressed as:

$$I(E_{kin}, i) = IN_i\sigma_i(k)\lambda(E_k)H \quad (4.7),$$

where I is the incident photon flux, N_i the atomic concentration of the *i*-species, $\sigma_i(k)$ the ionization cross section referred to the level *i* and to the incident photon momentum, $\lambda(E_k)$ is the escape depth length at the kinetic energy E_k and H individuates an instrumental factor. Since ab-initio calculation of some of the factors in equation (4.7) is quite difficult, the general procedure for this type of analysis is the use of calibrated quantities and the atomic sensitivity factors (ASF), which takes into account the excitation probability of the element *i*, for a certain impinging photon. In such a way the relative atomic concentration of the element *i* can be expressed as:

$$N_i = \frac{A_i}{ASF} \quad (4.8),$$

in which the peak intensity is its integrated area A_i . The ASF values are tabulated taking as reference the element *i* in a standard state.

The following XPS analysis of organic materials has been performed only for reference PDI8-CN2 and PDIF-CN2 thin films (25nm). As explained below, the complexity of the core level line shapes and their low photoemission signals in ultra-thin films on graphene require further detailed studies that, up to date, are still in progress.

4.4.2 XPS analysis of PDI8-CN2 and PDIF-CN2 reference films

XPS has been performed by means of a Mg K α X-ray source (photon at 1253.6eV) and a PSP electron energy analyzer. The total energy resolution is typically 0.86eV, and spectra were collected in low- and high-resolution modes, changing the Pass Energy (PE) of the analyzer (20eV for low resolution, 10eV for high resolution spectra). All the core level

binding energies (BE) were normalized to the Au 4f7/2 core level signal (at 84.0 eV), obtained from a sputtered gold surface. The core level analysis has been performed by Voigt line-shape deconvolution after the background subtraction by means of a Shirley function. The typical precision for each component's energy position is ± 0.05 eV. The uncertainty for the full width at half-maximum (FWHM) is less than $\pm 2.5\%$, while for the area evaluation it is about $\pm 2\%$. Both photon sources are mounted on the same UHV analysis chamber, and the collection geometry for photoemitted electrons is normal to the sample surface (normal incidence).

As reported in Figure 4.23, the survey spectra for both molecular species show the presence of carbon (C1s), oxygen (O1s), nitrogen (N1s) and fluorine (F1s), the latter only for PDIF-CN2. Other contributions come from Auger peaks or sample holder and are not considered in the following analysis. The equivalent spectrum for graphene is also shown, where signals from the SiO₂ (Si 2p and 2s core levels and O1s) substrate are clearly visible. The N1s peaks can be ascribed, in this case, to the spurious contribution of the sample holder.

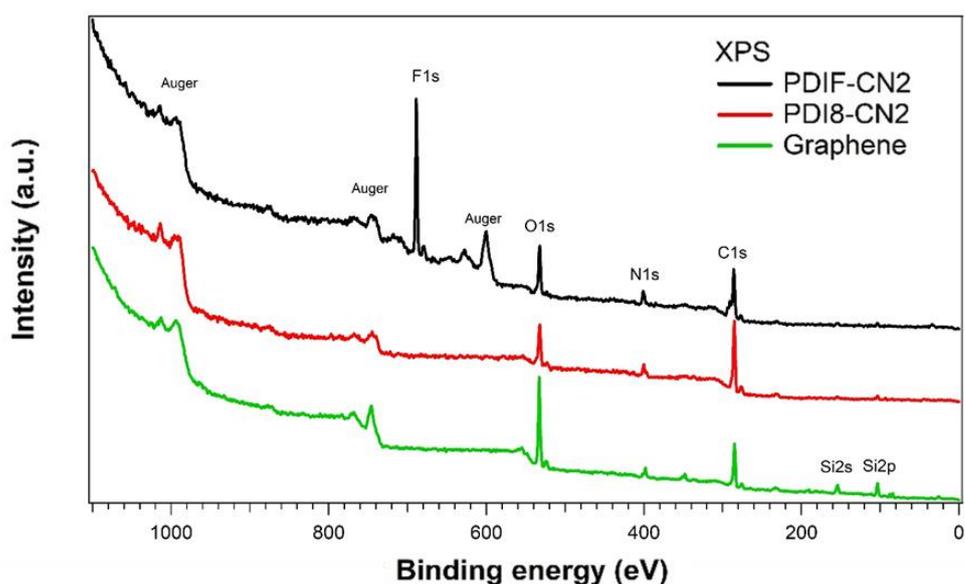


Figure 4.23 Survey XPS spectra for 25nm thick PDI8-CN2 and PDIF-CN2 films deposited via OMBD on HMDS-functionalized SiO₂ (200nm). The green solid line is the XPS spectrum of pristine CVD-Graphene transferred on 300nm thick SiO₂ (Graphenea, Inc.).

In the reference samples, the C1s contribution appears as a complex peak, with several components that reflects the presence of the different functional groups. In particular, for PDI8-CN2, it is possible to follow a model already reported in [201] by which the C1s can be reproduced by these peaks: C-C bonds and C-H of the aromatic core at 284.3 eV and 284.8 eV, C-H of the lateral chains at 285.7 eV, C close to C bonded to electron withdrawing groups at 286.2 eV, C in C \equiv N at 286.9 eV and C in N-C=O groups at 288.5 eV (Figure 4.24a). All peaks have similar width of about 1.1 eV. The model includes also presence of typical, broad satellite peak, due to electron energy loss and/or shake-up processes located at 290.2 eV.

Referring to Figure 4.24b, for PDIF-CN2, it is possible to identify the signals from C-F3 (293.6eV) and C-F2 (291.1 eV), N-C=O (288.7 eV), C≡N (286.8 eV) and one peak including all the C-C (285.8eV), indeed showing a larger width with respect to previous peaks (about 1.5 instead of 1.1 eV, due to the presence of more than one chemical species). Comparing similar chemical species, present in both molecules and reliably identifiable, as carbon atoms in C-N=O bonds, it is possible to observe a +0.2 eV shift towards higher BEs. This has been already observed in organic molecule with or without presence of fluorine atoms and attributed to their specific electron withdrawing properties [202,203].

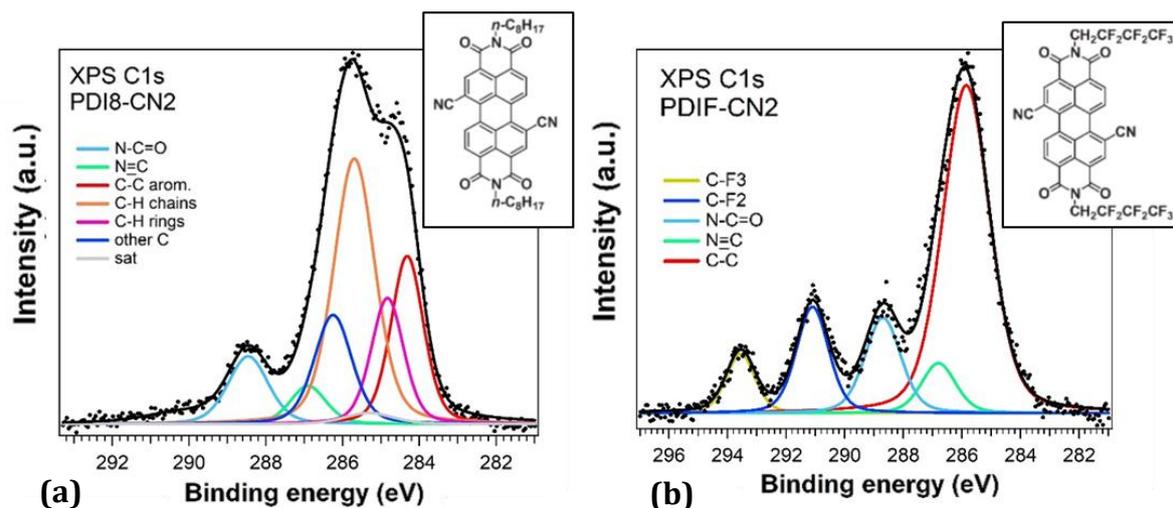


Figure 4.24 Detail of the C1s contribution for (a) 25nm thick PDI8-CN2 film and (b) 25nm thick PDIF-CN2 film deposited on HMDS-treated SiO₂ substrates (200nm). The insets show the molecular structures of the two moieties.

N1s core levels can be reproduced by two main peaks, well representing the two functional groups (labelled as N-C and N≡C in Figure 4.25a and b).

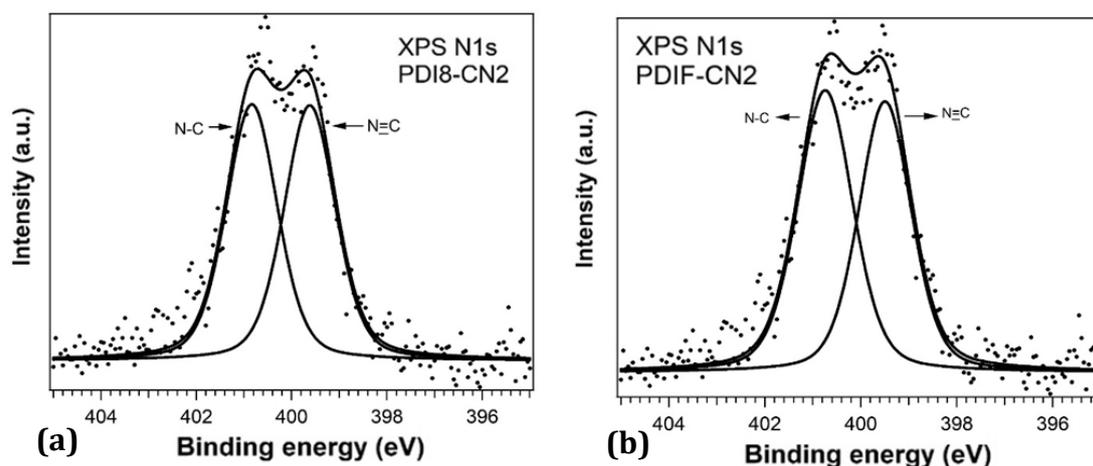


Figure 4.25 N1s core levels for (a) PDI8-CN2 and (b) PDIF-CN2 thin films.

Concerning analysis of O1s core level, an unusual broad peak is observed, by far larger than single components of carbon or nitrogen previously presented. Though never studied or commented in detail, this feature can be also found also in other papers [201].

O1s core level analysis in ex-situ experiments is always strongly influenced by presence of contaminations (water, COx) which can be hardly identified. Thus, any further deconvolution of these peaks could be not completely reliable. Despite this, considering the presence of a typical amounts of contaminants, the O1s peaks for both molecules are located at about 533 eV (Figure 4.26a and b), with a width of roughly 3 eV that can be used to calculate the surface stoichiometry. As final remark, in PDIF-CN2 samples, F1s is properly fitted introducing two contribution at 689.1 and 688.4 eV, for C-F2 and C-F3 groups respectively (Figure 4.26c).

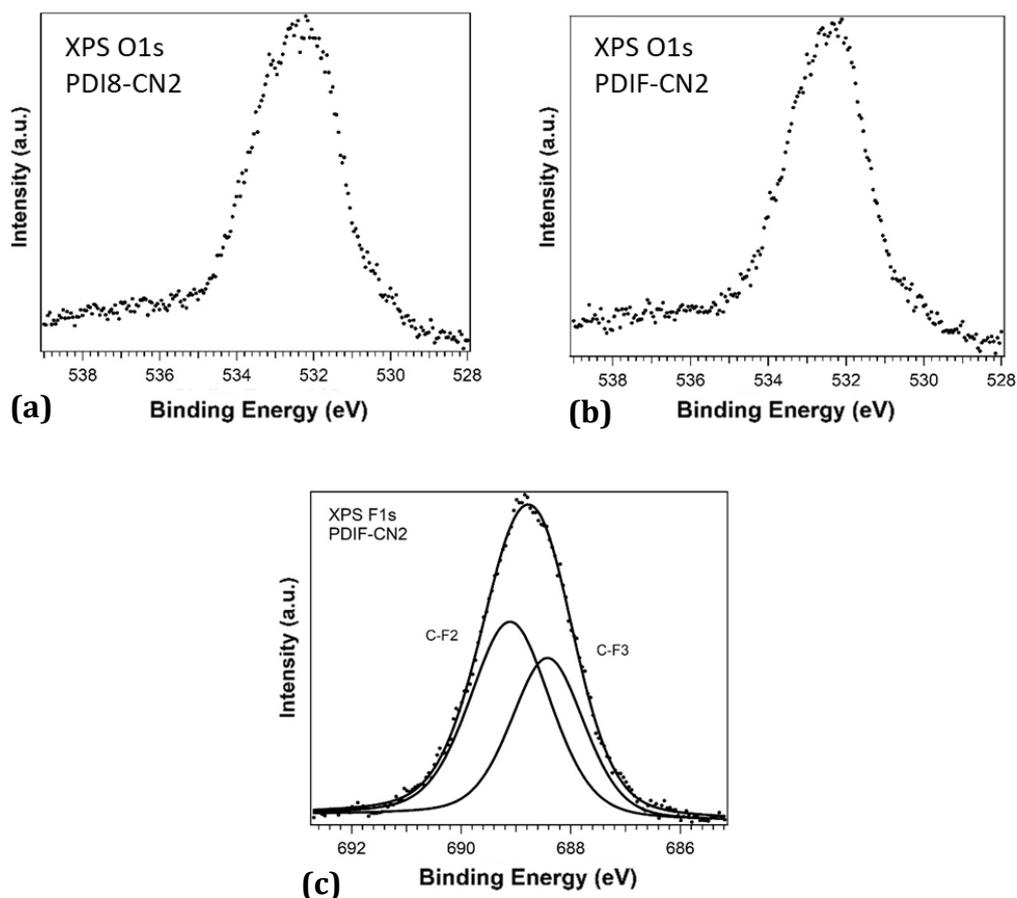


Figure 4.26 (a) and (b) O1s continuation to the XPS spectra of PDI8-CN2 and PDIF-CN2, respectively. (c) F1s peak individuating the fluorocarbon chains of PDIF-CN2.

From the total peaks area of C1s, F1s, N1s and O1s core levels, it is possible to estimate the atomic percentages at the surface. Results are in good agreement with theoretical values as summarized in Table 2, signifying that molecules are not damaged during the sublimation and/or deposition processes.

	C1s [%]	O1s [%]	N1s [%]	F1s [%]
PDIF-CN2	60.29	6.33	7.03	26.35
PDIF-CN2 theory	60.6	7.2	7.2	25
PDI8-CN2	81.66	9.43	8.91	-
PDI8-CN2 theory	84	8	8	-

Table 2 Percentages of different atomic species, estimated from the XPS analysis on the 25nm thick films of PDI8-CN2 and PDIF-CN2, respectively. Data are in good accordance with theoretical stoichiometry of the two molecular precursors.

4.4.3 UV photoelectron spectroscopy

In contrast with XPS analysis, UPS uses UV photons the energy of which ranges from few eV up to few hundreds of eV as excitation sources. The main difference from the XPS spectroscopy hence is that only the most external electronic levels of single atom, molecular bands (HOMO levels in the case of organic compounds, for example) of aggregates and high-laying energy bands in the case of solids (valence band for semiconductors), are involved in the process of photoelectron production. UPS have a probing depth of $\sim 15\text{\AA}$ and it is therefore used to extract important information about interaction processes involving the external electronic levels at the very interface.

The photoelectric effect generates free electrons with a kinetic energy which depends on the exciting photon energy $h\nu$, the work function of the sample (ϕ), the binding energy of the excited electron and the inelastic scattering events in the sample. Figure 4.27 represents a typical UPS spectrum, that can be divided in two regions:

- The left part is the low kinetic energy secondary-electron region, that represents the secondary electron cut-off (SECO). This cut-off, named photoemission onset, is associated to the vacuum level (E_{vac}), since electrons with less energy cannot come out from the solid. This onset gives the position of E_{vac} with respect to other photoemission features such as the highest occupied molecular orbital (HOMO).
- The right section of the spectra individuates the high kinetic energy valence band region, typically characterized by the presence of Fermi level (for metals) and VB offset, as well as HOMO for molecules.

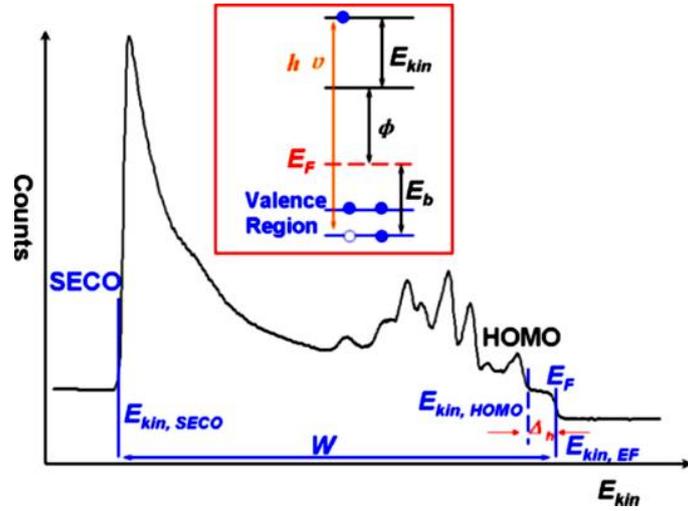


Figure 4.27 Example of a typical PES spectrum showing the various energy levels. The inset displays the schematic of photoelectron emission process in a PES experiment. From [204].

From the UPS spectrum is possible to calculate the sample work function according to the following equation:

$$\phi_{sample} = h\nu - W = h\nu - (E_{kin,EF} - E_{kin,SECO}) \quad (4.9),$$

where $E_{kin,EF}$ and $E_{kin,SECO}$ are the kinetic energy relative to Fermi level and the SECO respectively, and W is the spectrum width (i.e. the kinetic energy difference between E_F and the SECO). Being the $E_{kin,EF}$ always equal to the photon energy, the $E_{kin,SECO}$ value typically represents the work function of the sample.

In the case of a semiconductor, the Fermi level is located within the band gap, so that it is not possible to calculate the work function directly from the spectrum and the ionization potential (IP) must be considered. In the particular case of organic semiconductors, IP is calculated from the UPS spectrum as the difference energy between the HOMO and the vacuum level, or namely:

$$IP = h\nu - (E_{kin,HOMO} - E_{kin,SECO}) \quad (4.10)$$

4.4.4 UPS analysis of the organic/graphene interfaces

For the following data, UPS analysis has been performed with a He UV lamp (HeI, $h\nu=21.2$ eV) and the same PSP analyzer employed for the acquisition of XPS spectra. The valence band (VB) binding energy (BE) was referred to the Fermi level of an Au specimen in electric contact with the system. Samples are polarized at -7eV during the analysis. The substrate and organic WFs were evaluated from the position of the secondary electron cut-off (SECO), while the organic ionization potential (IP) can be evaluated (± 0.1 eV uncertainty) from the difference between the photon energy and the spectrum length (calculated taking into account the HOMO centroid position) via equation (4.10).

Figure 4.28 shows the UPS spectra acquired from the thick molecular films (25nm

deposited on 200nm SiO₂ substrates) and from a pristine graphene surface, showing both valence band/secondary cut-off regions (SECO) at higher resolution. The upper binding energy scale should be used as a reference, where 0eV is the position of the Fermi level.

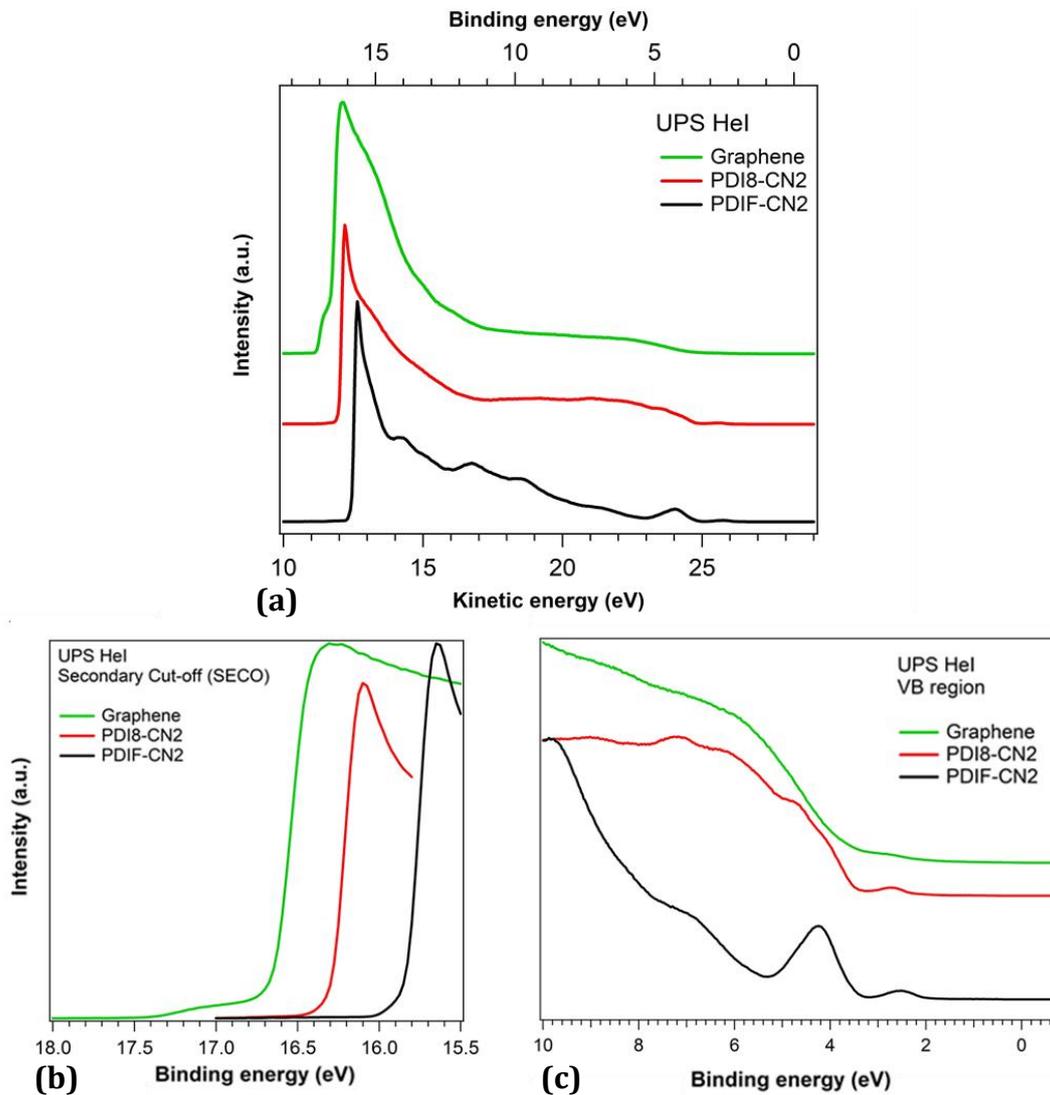


Figure 4.28 (a) High-range UPS spectra for the 25nm thick reference organic film deposited on HMDS-treated SiO₂ and for the pristine CVD-Graphene sheet transferred on 200nm SiO₂. (b) and (c) focus on the details of secondary cut-off (SECO) and valence bands (VB) of the spectra in (a).

Concerning the valence bands of the organic semiconductors (Figure 4.28b), they show the typical VB spectrum, in agreement with previously published results [205,206]. In the case of graphene, VB starts at 0eV and has the typical spectrum that is expected using this exciting photon energy, with a main broad band centered at about 6-7eV, and a small feature at 3eV. The measured spectra have been used to calculate several parameters, like work function and/or ionization potential (only for the organic films), via equation (4.9). Results are summarized in Table 3.

Sample	SECO (eV)	IP (eV)	WF (eV)
Graphene	16.75	-	4.45
PDI8-CN2	16.30	7.1	4.92
PDI8-CN2 ref.[206]	-	7.1	4.8
PDIF-CN2	15.84	7.33	5.38
PDIF-CN2 ref.[205]	-	7.5	5.6

Table 3 Values of secondary cut-off (SECO), ionization potentials (IP) and work functions (WF) of a pristine CVD-graphene sheet, of 25nm thick PDI8-CN2 and PDIF-CN2 thin films and their comparison with values retrieved from literature (ref.).

WF values for graphene are in good accordance with those expected for a single layer and in particular for intrinsic samples. For PDI8-CN2, WF and IP are observed to slightly diverge from reported values (+0.1eV, +0.5eV). Similar deviations are found for PDIF-CN2, with +0.2eV/+0.4eV for WF and IP, respectively. In both cases, it is plausible to ascribe the variations merely to the calculation method employed in the aforementioned works in which the top HOMO region has been considered rather than of the HOMO centroid. Moving to organic thin films at low coverages, deposited directly on the CVD-graphene surfaces, i.e. for 1nm and 3nm thick samples, UPS analysis reported in Figure 4.29 puts in evidence significant differences with respect to reference films.

For the 1nm PDI8-CN2 sample, in Figure 4.29a and c, the typical line shape of the molecular species is hardly detectable while a significant shift of about -1eV of the SECO position is observed (Figure 4.29b). Correspondingly, WF values are lower than those obtained for thick film and for pristine graphene. Moreover, PDI8-CN2 shows a double SECO threshold that typically suggests the presence of two different emitting surfaces, due to presence of different materials or an incomplete layer formation. The latter hypothesis is confirmed from AFM analysis of Figure 4.21, since only about half of the surface is covered by the PDI8-CN2. Nevertheless, the two WF values are lower also than graphene. The valence band line shape does not reproduce graphene or PDI8-CN2 molecular bands, however the behavior at Fermi level resembles the semi-metallic nature of graphene, without a real energy gap. This suggests the presence of a strong chemical interaction at the surface, or charge transfer, the nature of which has to be further investigated.

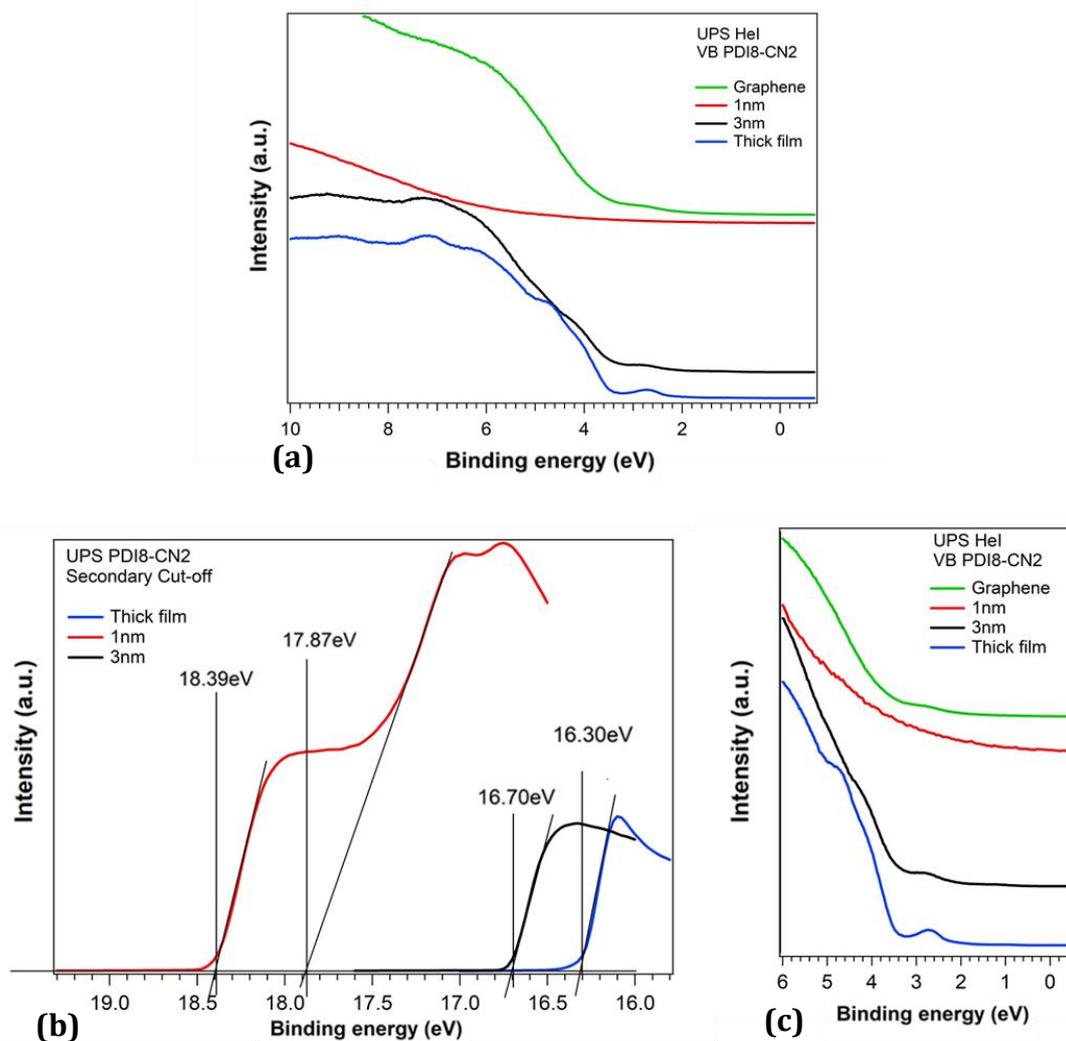


Figure 4.29 (a) UPS spectra of valence bands (VB) for the ultra-thin films of PDI8-CN2 (1nm and 3nm) deposited on CVD-Graphene and for the 25nm reference film deposited on HMDS-treated SiO₂. For comparison, the results for the pristine graphene sample are reported as well in the graph. (b) and (c) show, respectively, the detail of the secondary cut-off (SECO) and valence bands (VB) for binding energies ranging from 0eV and 6eV.

In the PDIF-CN2 case, the results for the 1nm film reported in Figure 4.30b presents a single SECO threshold, very close to that of graphene. For this sample, AFM data reveal a coverage of about 20%, so it is possible to consider that the UPS spectrum in this region is more representative of the graphene substrate rather than the molecular layer, indicating furthermore a weak interaction at the interface. The valence band shows typical features of the thick organic film, with HOMO and HOMO-1 clearly detectable, even if there is a possible superposition of the former with graphene band at about 3eV Figure 4.30a and c. A rigid shift towards higher binding energies, +0.6eV, is present if compared to a multilayer molecular film. However, the region at 7-10eV shows different features. When the nominal thickness is increased to 3nm, the VB line shape appears to coincide with the reference spectra of both molecules, with molecular bands shifted towards higher BE of 0.15 to 0.3eV for PDI8-CN2 and PDIF-CN2, respectively. The SECO regions

approach that of the reference samples with roughly 0.3eV lower values. Considering that the 1nm valence bands for both molecules show a line shape that is not clearly ascribable, for these samples, IP for only the 3nm films have been calculated. All the parameters are summarized in the following table:

Sample	SECO (eV)	IP (eV)	WF (eV)
Graphene (from Table 3)	16.75	-	4.45
PDI8-CN2(1nm)/Graphene	17.87-18.39	-	3.35-2.83
PDI8-CN2(3nm)/Graphene	16.7	7.37	4.52
PDIF-CN2(1nm)/Graphene	16.83	-	4.39
PDIF-CN2(3nm)/Graphene	16.16	7.91	5.06

Table 4 Secondary cut-off (SECO), ionization potential and work function values calculated for ultra-thin films of PDI8-CN2 and PDIF-CN2 deposited on CVD-Graphene. Data obtained for pristine graphene samples are shown for comparison.

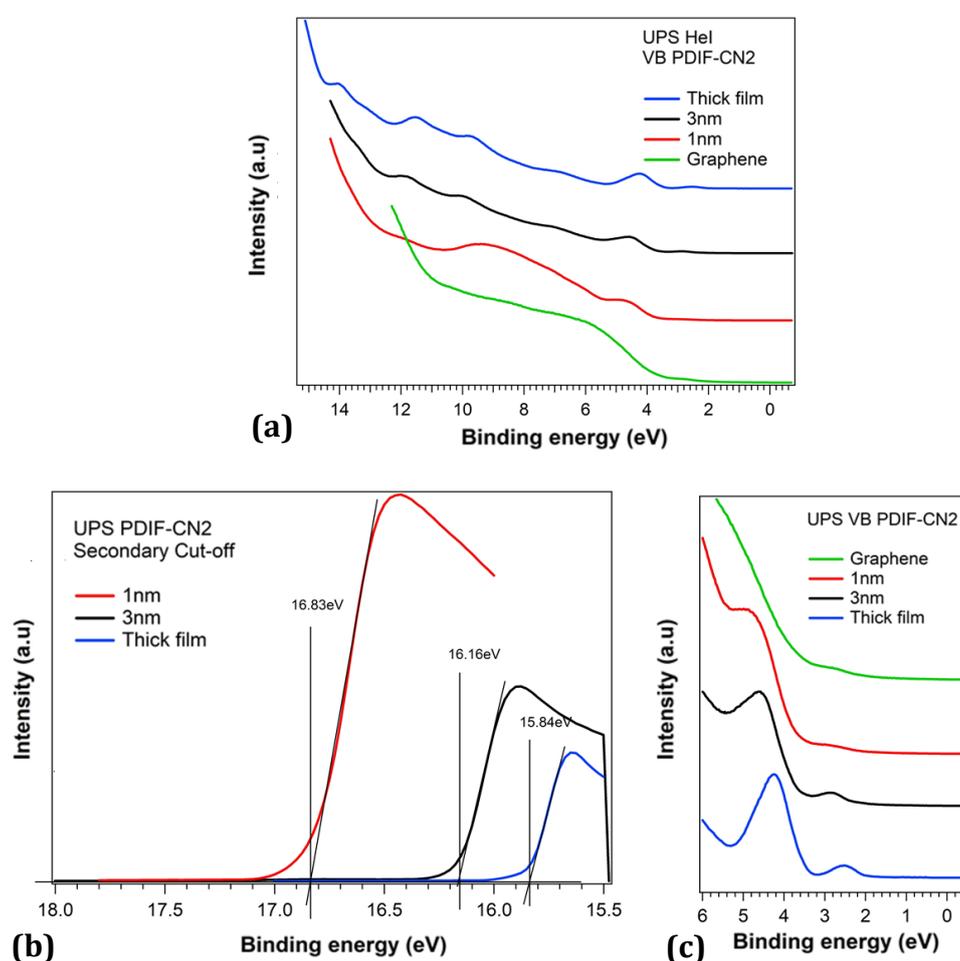


Figure 4.30 (a) UPS spectra of valence bands (VB) for the ultra-thin films of PDI8-CN2 (1nm and 3nm) deposited on CVD-Graphene and for the 25nm reference film deposited on HMDS-treated SiO₂. For comparison, the results for the pristine graphene sample are reported as well in the graph. (b) and (c) show, respectively, the detail of the secondary cut-off (SECO) and valence bands (VB) for binding energies ranging from 0eV and 6eV.

4.5 FINAL DISCUSSION

In this last chapter we demonstrated the capabilities of graphene electrodes in long channel OFETs based on PDI8-CN2 thin film evaporated by mean of OMBD. As a first interesting result, at the micrometric scale, graphene-based devices show electrical that can easily compete with state-of-the-art PDI8-CN2 devices with gold electrodes. Comparable field effect mobilities ($\mu_{FET} \approx 1 - 3 \times 10^{-2} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$) have been calculated through the electrical characterization of both architectures in vacuum.

We focused the attention on the contact resistances R_c , measured via SKPFM, affecting the OFETs by comparing the results obtained for gold-based and graphene-based architecture, especially addressing the role of the organic thin film thickness in the case PDI8-CN2.

As demonstrated by the analysis of the SKPFM profiles for state-of-the-art PDIF-CN2 devices with gold electrodes, the transistors considered cannot be assumed to be just injection-limited, since the values of R_{source} and R_{drain} are at least comparable and with the latter becoming even dominant at low V_{ds} . Voltage drops $\Delta V_{\text{drain}} \approx 0.8 \text{V}$ $\Delta V_{\text{source}} \approx 0.6 \text{V}$ at the source and drain electrodes, respectively, are typically observed in linear regime. Similar results have been obtained for PDI8-CN2 deposited on un-treated SiO_2 substrates, with film thicknesses below 40nm. The role of the morphology in the vicinity of the gold electrodes appears to have substantial influences for increased thicknesses for which R_{source} is observed to be enhanced.

Surface voltage distribution in graphene-based counterpart appears to be substantially different. In this case, drain resistances are absent while contact effects are observed to be concentrated at the electron injecting interface, i.e. the source electrode. Moreover, an enhanced response to both the gate voltage and temperature have been observed. The theoretical picture describing the contact effects appears to coincide with results found for graphene-based architectures rather than gold electrodes, since an inverse polarized p-n junction at the source and a forward polarized n-p junction at the drain electrode are expected. Experimental evidence can be thus partially explained referring to the morphological role of the electrodes on the overall electrical response of the interfaces. In graphene architectures, the atomically thin electrodes are observed to be barely noticed by the organic thin film growth and it cannot be excluded that also the area surrounding the very interface could in principle contribute in part to the charge injection and extraction mechanisms. This assumption is further strengthened if the partial permeability of graphene to longitudinal electric fields is taken in consideration. Conversely, gold electrodes can be assumed as a “true” physical barrier according to which morphological terms, comprising rms-roughness and grain boundary density, must be considered.

In the second part of the chapter we reported the results of the investigation of the CVD-graphene/organic interfaces via UPS and XPS analysis.

XPS investigation of reference films of both organic moieties essentially confirm the reported elemental analysis of previous works, ensuring that OMBD growth does not influence the actual stoichiometry of the interfaces. On the other hand, the

phenomenological picture given by UPS spectra highlights some peculiarities, especially in the case of pristine CVD-graphene samples or graphene/organic interfaces with monolayer or sub-monolayer coverages.

As a first remark, the magnitude of the electro-chemical interaction between organic molecules and graphene surface is further verified by the UPS analysis. In particular, an overall shift of the valence bands of 0.15eV and 0.3eV for PDIF-CN2 and PDI8-CN2 (3nm), respectively, verifies the interfacial transfer phenomena previously inferred from the electrical characterization of GFETs acquired after the organic thin film deposition. Regarding the properties of the pristine CVD-Graphene surface, work function calculation gives a value of $WF=4.55\text{eV}$, in total accordance with reported values referring to intrinsic exfoliated graphene. However, data appear to be quite discordant with both the estimated WF value via SKPFM ($\approx 5\text{eV}$) and with doping state inferred by electrical characterization of GFETs: the latter always suggesting the presence of highly p-doped CVD-graphene electrodes with neutrality point shifted towards positive gate voltages. It is possible to explain such variation in terms of the investigation technique, in this case the surfaces are probed via UV radiation rather than by field-effect induced at the dielectric/graphene interface, or in terms of the intrinsic properties of the pristine samples. More specifically, UPS measurements have been acquired for non-processed samples, i.e. pristine CVD-graphene sheets transferred on SiO_2 that have not underwent to any lithographic process. It is thus plausible that the fabrication procedure can affect irreversibly the doping conditions of graphene yet at the micrometric scale.

5 CONCLUSIONS

Despite great improvements, proper working conditions for OFETs with channel lengths below $1\mu\text{m}$ is still technologically challenging. On the other hand, the recent rise of graphene has prompted the relentless search for reliable technological applications of such a peculiar material.

In sight of this, in this work we demonstrated that those two topics can be beneficially combined in the development of n-type organic devices based on perylene diimides derivatives, with good transistor operation for channel length down to 140-200nm. We firstly tested CVD-graphene electrodes in nanometric channel transistors based on thermally evaporated thin films of PDIF-CN2. By a thorough comparison with short channel devices made with reference gold electrodes, we found that the output characteristics of the graphene-based devices respond linearly to the applied bias, in contrast with the supralinear trend of gold-based transistors. Moreover, current on/off ratios independent of the channel length and enhanced response for high longitudinal biases are demonstrated for L as low as 140 nm. These results are rationalized taking into account the morphological and electronic characteristics of graphene, showing that its use as electrodes helps to overcome the problem of Space Charge Limited Current and Drain induced Barrier Lowering, typically encountered in short channel devices. Despite the encouraging results, the firstly investigated architecture does not show a proper current saturation since the low gate capacitance given by the modestly thick SiO_2 layer (300nm resulting in $C_{\text{SiO}_2} \approx 11\text{nF}/\text{cm}^2$). In any case it can be considered as a valuable test-pattern for the investigation of fundamental aspects.

Further advances have been reached by the use of nano devices based on evaporated thin films of PDI8-CN2, with patterned local gate tracks and an ultra-thin film of Hafnium Dioxide as gate dielectric (8nm resulting in $C_{\text{HfO}_2} \approx 2.21\mu\text{F}/\text{cm}^2$). The largely improved gate modulation results in a proper output currents saturation for channel lengths down to 200nm, with supply biases of few volts. Through impedance spectroscopy, overlap capacitances and the overall AC response of CVD-graphene electrodes have been investigated as well. It appears that the contribution of the quantum capacitance of the graphene electrodes starts to be quite noticeable if compared to the contribution given by the bare oxide. We observed a capacity modulation with a distinct “V” shape resembling the characteristic of Graphene-FET transfer curves, reaching a minimum value in the vicinity of the Dirac point and an average modulation of about $1.4\text{ fF}/\mu\text{m}^2$. In this particular architecture, the cut-off frequency can be thus indirectly evaluated considering the DC transconductance and the measured overlap capacitance of the graphene electrodes. Values of the order of 10^5 Hz has been obtained for channel lengths of 200nm. Lastly, we focused on the organic/graphene interfaces investigate by Scanning Kelvin Probe Microscopy. In this case a micrometric graphene-based architecture ($L=10\mu\text{m}$) have been compared to state-of-the-art gold-based layouts. Electrical performances in vacuum condition are demonstrated to be interestingly comparable, with calculated field-effect mobilities in saturation regime of $\approx 4 \times 10^{-2} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ for both the architectures.

However, we observed differences in terms of surface voltage profiles, with contact resistances affecting solely the source electrode, in contrast with gold architectures where voltage drops are equally distributed at the injection (source) and extraction (drain) interfaces. Moreover, the overall phenomenology suggested an enhanced response of contact effects as function of the gate voltage and of the temperature. Results have been rationalized taking into account the morphological peculiarities of the graphene/organic interface given by the negligible thickness of the graphene and its permeability to the transversal electric field.

Further details on the interface energetics are provided by analyzing photoemission UPS/XPS spectra of bare graphene and organic/graphene interfaces with sub monolayer or 1-2 monolayer coverages of both PDI8-CN2 and PDIF-CN2. The UPS spectra revealed some discrepancies with the phenomenological picture discerned from SKPFM data and the electrical characterization of the graphene electrodes. Particularly, the work function of the bare graphene surface matches with the theoretical values obtained for undoped, i.e. intrinsic, graphene which appears to be in contrast with the p-type doping condition usually encountered in the graphene-based OFETs. Such differences are mainly ascribed to the investigation method which, in this case, is applied to unprocessed bare interfaces rather than to actual field-effect devices.

In conclusion, the use of CVD-graphene as electrode has been demonstrated as a valuable choice for the development of short channel OFETs. This contribution could hopefully clear the route to the future development of highly dense support circuitry in all-organic electronic devices, with possible applications in active matrix driven OLED panels or OLET arrays, requiring working frequencies of the order of $\approx MHz$, mechanical flexibility and low optical absorption.

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