UNIVERSITÀ DEGLI STUDI DI NAPOLI
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PH.D. THESIS

IN

INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

COMPACT HICUM MODELING OF DISTRIBUTED DYNAMIC LATERAL EFFECTS IN SIGE HBTS DURING LARGE-SIGNAL SWITCHING

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SCUOLA POLITECNICA E DELLE SCIENZE DI BASE
DIPARTIMENTO DI INGEGNERIA ELETTRICA E TECNOLOGIE DELL'INFORMAZIONE

Nomenclature

- ADS Advanced Design System
- BiCMOS Bipolar Complementary Metal Oxide Semiconductor
- BJT Bipolar Junction Transistor
- CMOS Complementary Metal Oxide Semiconductor
- ECC Emitter Current-Crowding
- HBT Heterojunction Bipolar Transistor
- HICUM HIgh CUrrent Model
- HICUM 1-T HICUM 1 Transistor
- HICUM 10-T HICUM 10 Transistors
- HICUM/L2 HICUM Level 2
- NQS Non-Quasi-Static
- QS Quasi-Static

Chapter 1

Introduction

1.1 Overview of bipolar transistors

Bipolar transistors (BJTs) have always had an important role in electronics field. But the eighties saw their importance falling down, because their higher speed became less important due to lower cost and higher integration of CMOS technologies. However BJTs still maintained an important foothold into some particular application areas, as communications, automation and measurement equipment, due to their better performances in the analog high-speed applications [1].

The nineties brought a new demand of high-speed devices. The BiCMOS technology was born: it allowed the integration of classical BJTs in silicon (Si BJTs) with CMOS technologies. But the silicon is not the best semiconductor to develop BJTs for high-speed applications. Indeed, the low carriers mobility in silicon for both electrons and holes limits the operating frequency of BJTs. So the development of devices with higher speed was obtained thanks to III-V semiconductors, e.g., GaAs and InP. Indeed, the BJTs made by III-V semiconductors have higher mobility density and higher saturation speed, which allows them to have a higher operating frequency. On the other hand, Si BJTs shows higher integration and lower cost. Moreover, there is no robust thermally grown oxide for GaAs and InP, the wafer are smaller and show higher defected density.

The coming of bipolar transistor in silicon-germanium heterojunction (SiGe HBTs) has allowed to keep the benefits of silicon, while increasing the performances at high frequencies applications. Indeed, the introduction of germanium into the silicon has many consequences. Due to smaller germanium bandgap with respect to silicon one, the lattice constant of germanium is larger than the silicon one. It makes the germanium useful in the silicon bandgap engineering. Moreover, SiGe HBTs can be implemented with Si CMOS and create with them a monolithic SiGe HBT BiCMOS technology.

1.2 Circuit models

The design and the optimization of circuits are based on simulation. The designer must have highly-accurate models of device in order to reduce the cost. However, these models should be simple in terms of computational effort.

The simplest way to imagine the carriers into a semiconductor is as a charged gas of free carriers. After the formulation of fundamental equations that describe the conservation and the motion of carriers, it is possible to follow the path of each carrier [2]. In order to simulate the path of each carrier, the Monte-Carlo method is the most used solution technique [3]. But this method has a huge computational cost.

The use of spherical harmonics expansion in order to resolve the conservation and the motion equations offers a significant improvement [4], but the computational cost is still high.

In most of the device simulations it is enough to consider the macroscopic quantities such as the average. In particular, the simplest way to describe the semiconductor physics involves only three equations: Poisson’s equation and the carrier continuity equations. Moreover, also the equations on material properties have been used. But even if this equation form is very simple, the computational cost is still

too expensive for design circuit [5]-[9]. So the need to develop a compact model arises.

The compact model must be sufficiently accurate in the simulation, but also sufficiently simple to be usable in practical circuits design. But the new technologies and the increasing of complex designs have made outdated the previous model formulation. Thus the compact models complexity increases.

1.3 HICUM Level2

The HIgh CUrrent Model, best known as HICUM, is a physics-based compact model for BJTs. In particular, HICUM Level 2 (L2) has the objective to build a large-signal equivalent circuit that works with technologies of continuously increasing current densities and frequencies. To achieve this, HICUM considers all the relevant phenomena occurring in modern devices.

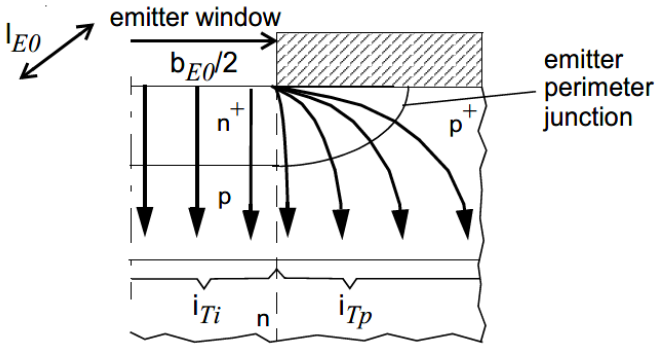

Fig. 1. *Schematic cross-section of the internal and perimetric region [2].*

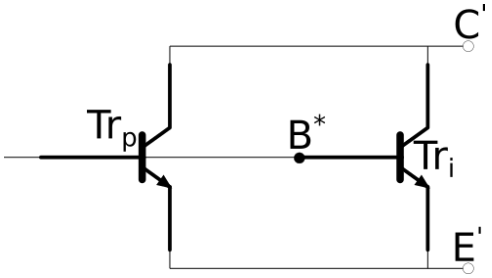

Fig. 2. *Schematic of the internal and perimetric region.*

In many processes the emitter doping profile diffuses laterally beyond the emitter window edge (**Fig. 1**), due to the high temperature processes. To consider this effect, HICUM is divided in an internal transistor Tr_i and in a perimetric transistor Tr_p (**Fig. 2**). The base current can be partitioned into an internal base current component I_{bi} and a perimetric base component I_{bp}. The first component flows into internal transistor Tr_i, while the second one flows into the perimetric transistor Tr_p. The two transistors carry the current components i_{Ti} and i_{Tp}, respectively.

The large-signal circuit of the internal transistor structure of HICUM/L2 is shown in **Fig. 3**, while the perimetric transistor structure is shown in **Fig. 4**.

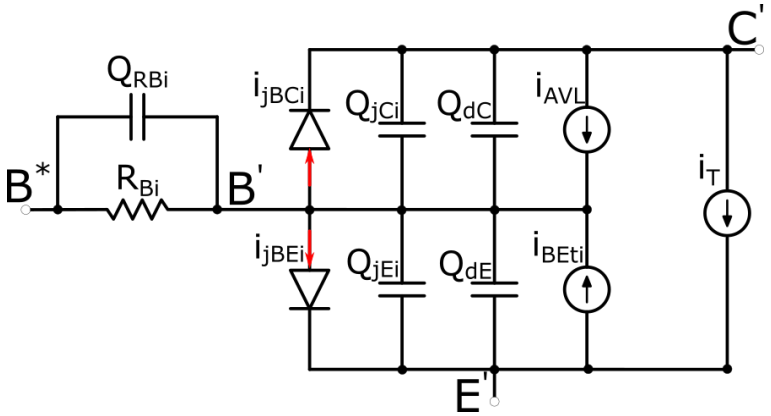

Fig. 3. *Large-signal equivalent circuit of the internal transistor structure of HICUM/L2.*

In **Fig. 3**:

- Q_{jEi} represents the internal base-emitter depletion charge and is function of internal base-emitter voltage $V_{B'E'}$ [10]-[12];
- Q_{jCi} represents the internal base-collector depletion charge and is function of internal base-collector voltage $V_{B'C'}$ [10]-[12];
- Q_{dE} represents the total minority charge "forward" component and is function of forward transfer current i_{Tf}, internal base-collector voltage $V_{B'C'}$ and internal collector-emitter voltage $V_{C'E'}$ [2];
- Q_{dC} represents the total minority charge "reverse" component and is function of reverse transfer current i_{Tr} [2];
- i_{jBEi} represents the sum between the quasi-static internal base-emitter space-charge region ($B'E'$ SCR) recombination current component I_{REi} and the quasi-static internal emitter back-injection current component I_{BEi}. Both these components are function of internal base-emitter voltage $V_{B'E'}$ [2];
- i_{jBCi} represents the current component flowing across the internal base-collector junction and is function of internal base-collector voltage $V_{B'C'}$ [2];
- i_T represents the quasi-static transfer current and it can be represented as sum of a "forward" component i_{Tf}, function of internal base-emitter voltage $V_{B'E'}$, and of a "reverse" component i_{Tr}, function of internal base-collector voltage $V_{B'C'}$. Both these components are function of all charges of the internal transistor as well [13]-[17];
- i_{AVL} represents the avalanche current component in the base-collector space-charge region ($B'C'$ SCR) and is function of the forward transfer current i_{Tf} and internal base-collector voltage $V_{B'C'}$ [18], [19];

- i_{BEti} represents the tunneling process at the internal base-emitter junction and is function of the base-emitter voltage $V_{B'E'}$ [20]-[24];
- R_{Bi} represents the internal base resistance and includes the effects of conductivity modulation and static emitter current crowding (ECC). It is function of all charges of the internal transistor and of the quasi-static internal emitter back-injection current component I_{BEi} [2];
- C_{rBi} represents a capacitance that takes into account about high frequency dynamic ECC at small-signal applications and is function of all charges of the internal transistor [2].

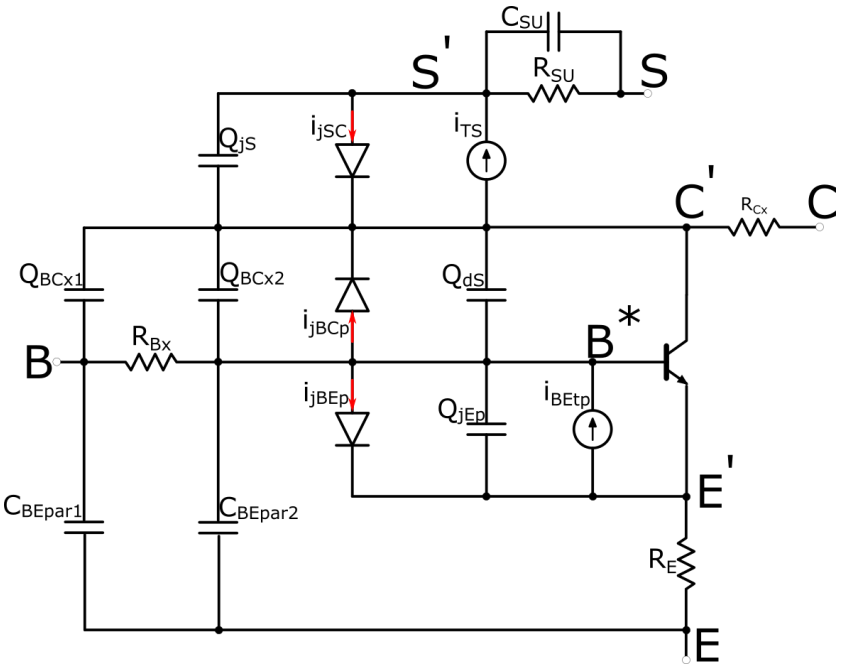

Fig. 4. *Large-signal equivalent circuit of the complete transistor structure of HICUM/L2. Tr_i represents the internal transistor structure, as shown in* ***Fig. 3****.*

Furthermore in **Fig. 4**:

- Q_{jEp} represents the perimetric base-emitter depletion charge and is function of the perimetric base-internal emitter voltage $V_{B*E'}$ [10]-[12];
- i_{jBEp} represents the sum between the quasi-static perimetric base-emitter space-charge region ($B*E'$ SCR) recombination current component I_{REp} and the quasi-static perimetric emitter back-injection current component I_{BEp}. Both these components are function of perimetric base-internal emitter voltage $V_{B*E'}$ [2];
- i_{jBCp} represents the current component flowing across the perimetric base-collector junction and is function of perimetric base-internal collector voltage $V_{B*C'}$ [2];
- i_{BEtp} represents the tunneling process at the perimetric base-emitter junction and is function of perimetric base-internal emitter voltage $V_{B*E'}$ [20]-[24];
- C_{BEpar} represents all the isolation capacitances between base and emitter regions and is split between external base node (C_{BEpar1}) and perimetric base node (C_{BEpar2}) [2];
- Q_{BCx} represents the sum of all the isolation capacitances between base and collector regions (C_{BCpar}) and the perimetric base-collector depletion charge (Q_{jCx}). This last component is function of the perimetric base-internal collector voltage $V_{B*C'}$. Moreover Q_{BCpar} is split between external base node (Q_{BCx1}) and perimetric base node (Q_{BCx2}) [2], [10]-[12];
- R_{Bx}, R_{Cx} and R_E are three lumped bias independent resistances;
- i_{TS} represents the quasi-static transfer current of the PNP transistor among perimetric base-internal collector-internal substrate ($B*$-C'-S') contacts. It can be represented as the sum of a "forward" component i_{TSf}, function of perimetric base-internal collector voltage $V_{B*C'}$, and of a "reverse" component i_{TSr}, function of internal substrate-collector voltage $V_{S'C'}$;

- i_{jSC} represents the current component flowing across the internal substrate-collector junction and is function of the internal substrate-collector voltage $V_{S'C'}$;
- Q_{dS} represents the total minority charge "forward" component in PNP transistor among perimetric base-internal collector-internal substrate (B^*-C'-S') contacts. It is function of forward transfer current of this transistor $i_{TSf,}$ internal base-collector voltage $V_{B'C'}$ and internal collector-emitter voltage $V_{C'E'}$;
- Q_{jS} represents the internal substrate-collector depletion charge and is bias independent;
- R_{su} and C_{su} represent the impedance between the internal substrate-collector depletion charge and the substrate contact. They are both bias independent.

1.4 Research topics

The compact models are based on hypothesis of quasi-static (QS) condition, i.e., that the carrier densities instantaneously follow the voltage applied across a junction. However, the carriers show a finite transit time at sufficiently high frequencies. So those which are farther from the junctions move with a delay with respect to applied voltage. These effects are called non-quasi-static (NQS) effects. They can be also divided into vertical non-quasi-static (NQS) effects and lateral non-quasi-static (NQS) effects. The focus of this thesis is to describe in the compact HICUM model the lateral NQS effects, also known as dynamic emitter current-crowding (ECC), in order to improve accuracy in large-signal applications.

The first step was to identify a good reference. Since performing measurements in time domain at very high frequencies is a nontrivial task, it was decided to refer to realistic 2D HBT simulations carried out by the software DEVICE [25].

The second step was to find a way to separate the vertical NQS effects from the lateral counterparts. Both these effects are indeed relevant and not separable in measurements or in DEVICE simulations. This issue was tackled by resorting to the following procedure. First, a distributed 10-transistor (10-T) HICUM model was implemented in the commercial Advanced Design System (ADS) circuit simulator. Then, it was shown that the results obtained with the distributed HICUM model with calibrated parameters favorably match with those determined by DEVICE. Finally, the distributed HICUM model was selected as a new reference, since, unlike measurements or DEVICE simulations, vertical NQS effects can be switched off and only lateral NQS effects can be analyzed.

The last step was to implement an improved version of the standard one-transistor (1-T) HICUM model equipped with a charge partitioning factor α (**Fig. 5**).

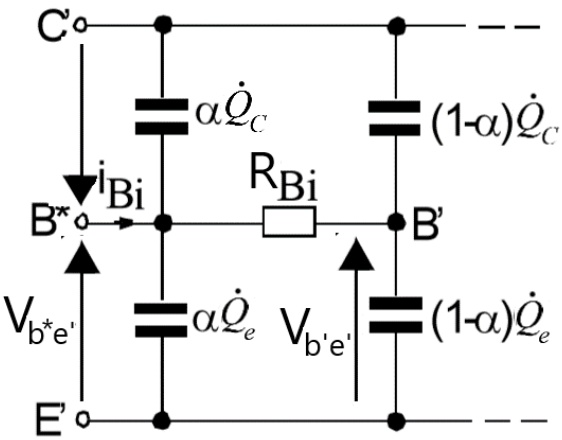

Fig. 5. *Implemented equivalent circuit with lateral charge partitioning across internal quasi-static base resistance R_{Bi}. C', E' and B' are the terminals of the internal transistor. B* represents the perimetric base node.*

This factor allows partitioning the internal HBT charge on both sides of internal base resistance. In this theses it is presented in Subsection 2.2.2 as a possible solution to describe the lateral NQS

effects for small-signal operation at high frequency. The idea presented in this thesis is to use this partitioning factor so to compensate the time shift due to the lateral NQS effects also for large-signal applications at high frequency. Additionally, an effort was done to describe this factor as function of input variables.

1.5 Thesis outline

The thesis is organized as follows:

- Chapter 2 reports a brief analysis that, starting from the physical BJT structure, leads to the distributed model (2.1). Then it is described how to arrive to a compact model representation in quasi-static (2.2), small-signal (2.2.2), and large-signal (2.2.3) operations. This chapter also introduces the idea of using the charge partitioning factor to accurately and efficiently describe the ECC effects for small-signal operations. Then, applying of charge partitioning factor at large-signal operations is proposed in this thesis;
- Chapter 3 reports the different approaches used in this thesis to model a SiGe HBT. First, the functioning principle of the DEVICE software (3.1) and the implemented transistor under test (3.2) are described. Then the implementation of the HICUM 1-T model version 3.0 (3.3.1) and the distributed HICUM 10-T model (3.4) are reported. Lastly, the HICUM 1-T model enriched with a charge partitioning factor and its implementation in Verilog-A are illustrated (3.3.2). Gummel plot, output plots, capacitances junctions plots and transition frequency plot are also shown for all these models to prove their reliability for static and small-signal operations;
- Chapter 4 reports the results obtained in large-signal applications. First of all, the data determined by the HICUM

1-T and 10-T models are compared to DEVICE simulations (4.1), which allows proving that the more accurate 10-T model can be definitely selected as a reference in lieu of the standard 1-T one. Then the improved 1-T model provided with charge partitioning factor is introduced, along with the procedure to estimate this relevant factor (4.2.1). Finally, the HICUM 1-T model with charge partitioning factor is compared to HICUM 10-T model (4.2.2 and 4.2.3);

- conclusions are reported in Chapter 5.

1.6 Publications

- R. Salvato, V. d'Alessandro, M. Tiebout "Extension of HICUM for large-signal applications of SiGe HBTs", 50th SIE meeting
- R. Salvato, M. Krattenmacher, V. d'Alessandro, C. Rubino, M. Schröter, "Lateral charge partitioning across the internal base resistance for modeling distributed dynamic lateral effects in SiGe HBTs during large-signal switching", 21st EuroSimE conference

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Chapter 2

Dynamic emitter current-crowding effects

In this Chapter the dynamic emitter current-crowding (ECC) is described. First of all how to arrive to a distributed model starting from a physical description of 2D transistor is described. Then the dynamic ECC effects are modeled for static and small-signal operations. Lastly, it is shown that it is not possible to achieve a generic solution of dynamic ECC for large-signal applications.

2.1 Physical description of internal transistor

Starting from a 2D transistor, **Fig. 6** shows how the base current i_{Bi} flows inside the transistor.

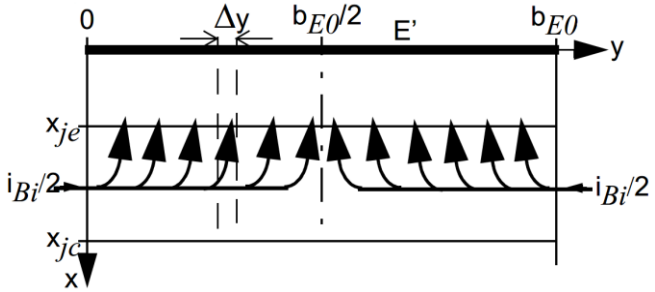


Fig. 6*. View of internal transistor with distributed current flowing inside [1].*

As shown in this picture, half current goes in from the left side (for $y=0$) and the other half current goes in from the right side (for $y=b_{E0}$). In each interval Δy a portion of base current is injected into the emitter, while the other part flows in the lateral section. For this reason, the behavior of BJT for $y \in \left[0, {}^{b_{E0}}/_{2}\right]$ is equal to that for $y \in \left[b_{E0}, {}^{b_{E0}}/_{2}\right]$. Therefore, the BJT is completely symmetric and all base current is injected into the emitter at $y=b_{E0}/2$.

The equivalent model of this distributed effect is shown in **Fig. 7**. In this picture each transistor represents a Δy portion depicted in **Fig. 6**.

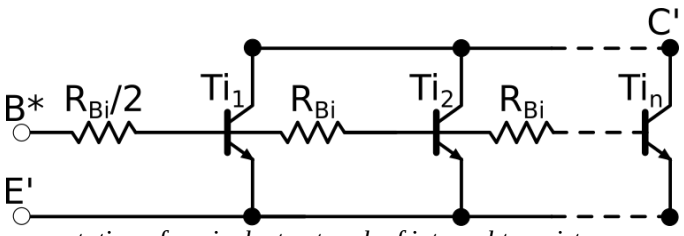


Fig. 7. *Representation of equivalent network of internal transistor.*

The purpose is to represent the described distributed effects with the minimum number of lumped elements. For all the aforementioned considerations concerning the HBT symmetry, in the next paragraph only half transistor is considered.

2.2 Current crowding effects

2.2.1 Static operation

Fig. 8 represents an equivalent network of internal transistor, where the base-collector junction is no shown, because the ECC effects are visible during high forward operation, where the dominant behavior is due to the base-emitter network.

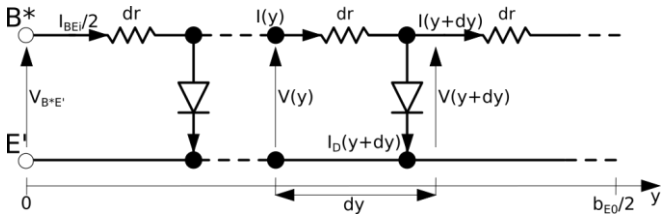


Fig. 8. *Representation of equivalent network of internal transistor without base-collector components.*

Every resistor dr of infinitesimal width dy is equal to:

$$dr = r_{SBi}\frac{dy}{l_{E0}} \tag{1}$$

The current I_D of the diode in the same infinitesimal width dy, instead, is:

$$I_D(y) = l_{E0}\, J_{SBi}\, e^{\frac{V(y)}{V_T}} dy \tag{2}$$

where J_{SBi} is the saturation current density, while $V(y)$ is the base-emitter voltage at y point.

The Kirchhoff equations of this network are:

$$I(y+dy) - I(y) = -I_D(y+dy) \tag{3}$$

$$V(y+dy) - V(y) = -dr\, I(y) \tag{4}$$

Replacing equation (2) in (3) and (1) in (4), it is obtained:

$$\frac{dI}{dy} = -l_{E0}\, J_{SBi}\, e^{\frac{V(y)}{V_T}} \tag{5}$$

$$\frac{dV}{dy} = -\frac{r_{SBi}}{l_{E0}} I \tag{6}$$

Differentiating the equation (5) and then replacing (2) and (6), is obtained:

$$\begin{gathered} \frac{d^2I}{dy^2} = -\frac{l_{E0}\, J_{SBi}}{V_T}\, e^{\frac{V(y)}{V_T}} \frac{dV}{dy} = \\ = \frac{I}{V_T}\frac{r_{SBi}}{l_{E0}}\frac{I_D}{dy} = \frac{I}{V_T}\frac{r_{SBi}}{l_{E0}}\frac{dI}{dy} \\ \downarrow \\ \frac{d^2I}{dy^2} - \frac{1}{2V_T}\frac{r_{SBi}}{l_{E0}}\frac{dI^2}{dy} = 0 \end{gathered} \tag{7}$$

The general solution of (7) is:

$$I(y) = K_2 tan\left(-\frac{K_1 + Cy}{K_2}\right) \text{ with } K_2 = \sqrt{-C\frac{2V_T\, l_{E0}}{r_{SBi}}} \tag{8}$$

where:

$$I\left(y=\frac{b_{E0}}{2}\right)=0\rightarrow K_1=-C\frac{b_{E0}}{2} \tag{9}$$

$$I(y=0)=\frac{I_{BEi}}{2}\rightarrow\frac{I_{BEi}}{2}=K_2 tan\left(K_2\frac{1}{2V_T}\frac{r_{SBi}}{l_{E0}}\frac{b_{E0}}{2}\right) \tag{10}$$

Replacing the constants C, K_1 and K_2 values into (8), the current distribution with respect to location y is obtained:

$$I(y)=4V_T\frac{l_{E0}}{r_{SBi}b_{E0}}Z\ tan\left[Z\left(1-\frac{2y}{b_{E0}}\right)\right] \tag{11}$$

where Z is defined as:

$$Z=K_2\frac{1}{4V_T}\frac{r_{SBi}b_{E0}}{l_{E0}} \tag{12}$$

Replacing (11) into (6) the voltage distribution is obtained:

$$V(y)=V(0)-2V_T\ ln\left(\frac{cos\left[Z\left(1-\frac{2y}{b_{E0}}\right)\right]}{\cos(Z)}\right) \tag{13}$$

The next step is to obtain a lumped network (**Fig. 9**) that produces the same characteristic of the distributed network (**Fig. 8**).

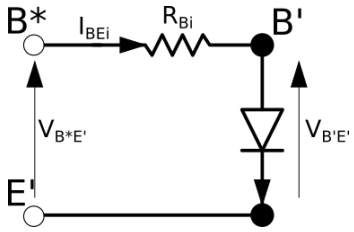


Fig. 9. *Representation of equivalent lumped network of internal transistor without base-collector components.*

The internal base-emitter voltage is:

$$V_{B'E'} = V_{B^*E'} - R_{Bi} I_{BEi} \text{ with } V_{B^*E'} = V(0) \tag{14}$$

while the internal base current in this circuit is:

$$I_{BEi} = I_{SBi} e^{\frac{V_{B'E'}}{V_T}} = I_{SBi} e^{\left(\frac{V_{B^*E'} - R_{Bi} I_{BEi}}{V_T}\right)} \tag{15}$$

The internal base current I_{BEi} is also equal to integration of injection current contributions I_D shown in (2) on the total emitter width:

$$\frac{I_{BEi}}{2} = \int_0^{\frac{b_{E0}}{2}} I_D(y)dy = \int_0^{\frac{b_{E0}}{2}} l_{E0}\, J_{SBi}\, e^{\frac{V(y)}{V_T}} dy = \tag{16}$$
$$= \frac{I_{SBi}}{2} e^{\left(\frac{V_{B^*E'}}{V_T}\right)} \frac{\sin(Z)\cos(Z)}{Z}$$

Comparing (16) with (15), the internal resistance value is obtained:

$$R_{Bi} = \frac{V_T}{I_{BEi}} ln\left(\frac{Z}{\sin(Z)\cos(Z)}\right) \tag{17}$$

These results were already obtained in [1].

2.2.2 Small-signal operation

Fig. 10 represents an equivalent network of internal transistor for small-signal operation. In this figure the base-collector junction is not shown, because the ECC effects are visible during high forward operation, where the dominant behavior is due to the base-emitter network. Moreover, the base-emitter elements were replaced by their associated admittances.

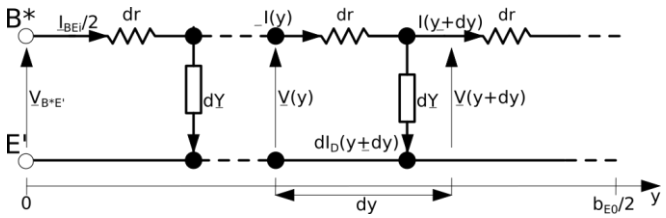


***Fig. 10**. Representation of equivalent network of internal transistor without base-collector components for small-signal operation.*

The admittance value dY is:

$$d\underline{Y} = dG + j\omega\, dC = l_{E0}(G^* + j\omega\, C^*)\, dy = l_{E0}\underline{Y}^* dy \tag{18}$$

$$\text{with } \begin{aligned} dG &= l_{E0} G^* dy \\ dC &= l_{E0} C^* dy \\ \underline{Y}^* &= G^* + j\omega C^* \end{aligned} \tag{19}$$

G^* and C^* represent the area specific values at the given bias point, respectively. The Kirchhoff equations for this network are:

$$\begin{aligned} \underline{I}(y+dy) - \underline{I}(y) &= -d\underline{I}_D(y+dy) \\ &= -l_{E0}\underline{Y}^*\, \underline{V}(y+dy)dy \end{aligned} \tag{20}$$

$$\underline{V}(y+dy) - \underline{V}(y) = -dr\, \underline{I}(y) \tag{21}$$

Differentiating (20) and replacing (1) into (21) and then (21) into (20), it is obtained:

$$\frac{d^2\underline{I}}{dy^2} - \underline{Y}^* r_{SBi}\underline{I} = 0 \tag{22}$$

The general solution of (22) is:

$$\underline{I}(y) = \underline{A}\cosh(\underline{k}\, y) + \underline{B}\sinh(\underline{k}\, y) \quad \text{with } \underline{k} = \sqrt{\underline{Y}^* r_{SBi}} \tag{23}$$

It must be emphasized that this solution is valid only assuming that G^*. C^* and dr do not depend on y. This is true when DC current crowding can be neglected.

$$\underline{I}(y=0) = \frac{\underline{I}_{BEi}}{2} \rightarrow \underline{A} = \frac{\underline{I}_{BEi}}{2} \tag{24}$$

$$\underline{I}\left(y = \frac{b_{E0}}{2}\right) = 0 \rightarrow \underline{B} = -\frac{\underline{I}_{BEi}}{2\ tanh\left(\underline{k}\frac{b_{E0}}{2}\right)} \tag{25}$$

Replacing the constants $\underline{A}$ and $\underline{B}$ values into equation (22), the current distribution with respect to y is obtained:

$$\underline{I}(y) = \frac{\underline{I}_{BEi}}{2}\frac{sinh\left(\underline{k}\left(\frac{b_{E0}}{2} - y\right)\right)}{sinh\left(\underline{k}\frac{b_{E0}}{2}\right)} \tag{26}$$

while replacing (26) into (21) allows obtaining the voltage distribution with respect to *y*:

$$\underline{V}(y) = \frac{\underline{I}_{BEi}}{2l_{E0}\underline{Y}^*}\underline{k}\frac{cosh\left(\underline{k}\left(\frac{b_{E0}}{2}-y\right)\right)}{sinh\left(\underline{k}\frac{b_{E0}}{2}\right)} \tag{27}$$

Next step is to obtain a lumped network (**Fig. 11**) that produces the same characteristic of the distributed network (**Fig. 10**).

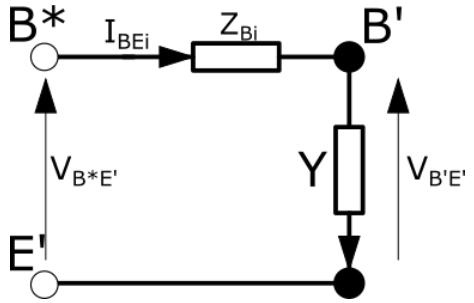


Fig. 11. *Representation of equivalent lumped network of internal transistor without base-collector components.*

The perimetric base-emitter voltage is:

$$\underline{V}_{B^*E'} = \underline{V}(y=0) = \frac{\underline{I}_{BEi}}{\underline{Y}}\ \underline{k}\frac{b_{E0}}{2}\ coth\left(\underline{k}\frac{b_{E0}}{2}\right) \tag{28}$$

while the lumped junction admittance is:

$$\underline{Y} = \underline{Y}^* b_{E0} l_{E0} = G + j\omega C \tag{29}$$

The closed-form solution for internal input impedance is:

$$\underline{Z}_{B^*E'} = \frac{\underline{V}_{B^*E'}}{\underline{I}_{BEi}} = \frac{1}{\underline{Y}} \, \underline{k} \frac{b_{E0}}{2} \, coth\left(\underline{k} \frac{b_{E0}}{2}\right) \tag{30}$$

which was first derived in [2].

At the end, the lumped internal base impedance is:

$$\underline{Z}_{Bi} = \frac{\underline{V}_{B^*E'} - \underline{V}_{B'E'}}{\underline{I}_{BEi}} = \frac{1}{\underline{Y}} \left[\underline{k} \frac{b_{E0}}{2} \, coth\left(\underline{k} \frac{b_{E0}}{2}\right) - 1\right] \tag{31}$$

Another lumped representation is with internal charge partitioning factor (**Fig. 12**).

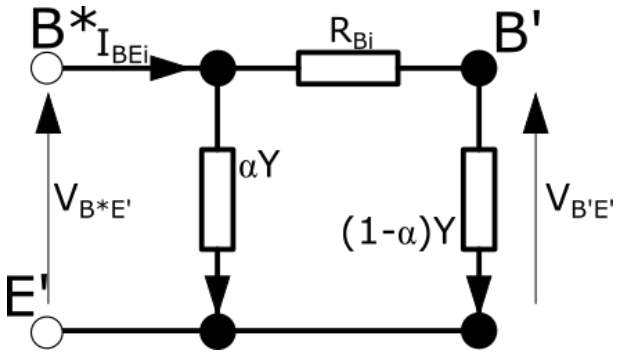


Fig. 12. *Representation of equivalent lumped network of internal transistor without base-collector components and with charge partitioning factor α.*

From this circuit, the internal input impedance is:

$$\underline{Y}_{B^*E'} = \frac{\underline{I}_{BEi}}{\underline{V}_{B^*E'}} = \alpha \underline{Y} + \frac{(1-\alpha)\underline{Y}}{1 + (1-\alpha) R_{Bi} \underline{Y}} \tag{32}$$

Solving this equation, the charge partitioning factor α is:

$$\alpha = \frac{1}{2}\left(1 + \frac{\underline{Y}_{B^*E'}}{\underline{Y}}\right) \pm \sqrt{\left(1 - \frac{\underline{Y}_{B^*E'}}{\underline{Y}}\right)\left[\frac{1}{4}\left(1 - \frac{\underline{Y}_{B^*E'}}{\underline{Y}}\right) + \frac{1}{R_{Bi}\underline{Y}}\right]} \qquad (33)$$

with $\alpha \in [0,1]$

Replacing (30) into (33) the charge partitioning factor α is obtained.

2.2.3 Large-signal operation

Due to its complexity, large-signal switching operation is very hard topic, which has required a long and intense research effort. The **Fig. 13** represents an equivalent network of internal transistor for large-signal operation. In this figure, the base-collector junction is neglected.

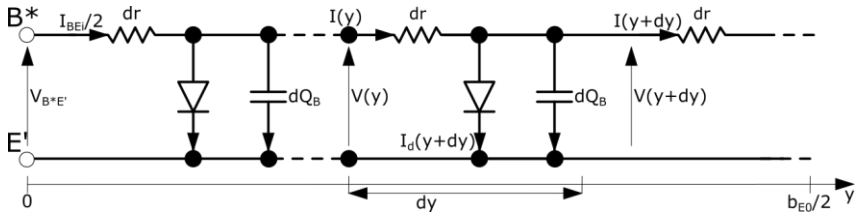


***Fig. 13**. Representation of equivalent network of internal transistor without base-collector components for large-signal operation.*

Every resistor dr of infinitesimal width dy is equal to:

$$dr = r_{SBi}(y)\frac{dy}{l_{E0}} \qquad (34)$$

The current of the i_D diode in the same infinitesimal width dy, instead, is:

$$I_d(y) = l_{E0}\, J_{SBi}\, e^{\frac{V(y)}{V_T}}\, dy \tag{35}$$

where J_{SBi} is the saturation current density, while $V(y)$ is the base-emitter voltage at y.

The two differential equations that govern the lateral voltage drop and current of this network are:

$$\frac{dV}{dy} = \frac{r_{SBi}(y)}{l_{E0}}\, I \tag{36}$$

$$\frac{dI}{dy} = l_{E0} \left(J_{SBi}\, e^{\frac{V(y)}{V_T}} + \frac{\partial Q_B(y)}{\partial t} \right) \tag{37}$$

Combining the equations (36) and (37) is obtained:

$$\frac{d^2V}{dy^2} = r_{SBi}(y) \left(J_{SBi}\, e^{\frac{V(y)}{V_T}} + \frac{\partial Q_B(y)}{\partial t} \right) + \frac{I}{l_{E0}}\, \frac{dr_{SBi}}{dy} \tag{38}$$

Assuming quasi-static conditions in vertical direction for the charging process, results:

$$\frac{\partial Q_B}{\partial t} = \frac{\partial Q_B}{\partial v} \frac{\partial V}{\partial t} = C_B(V) \frac{\partial V}{\partial t} \tag{39}$$

Replacing (36) and (39) into (38), the differential equation becomes:

$$\frac{d^2V}{dy^2} - \left(\frac{1}{r_{SBi}}\, \frac{dr_{SBi}}{dy} \right) \frac{dV}{dy} - r_{SBi}\, J_{SBi}\, e^{\frac{V(y)}{V_T}} = r_{SBi} C_B \frac{\partial V}{\partial t} \tag{40}$$

Unlike static and small-signal operations, a solution of this differential equation needs also the knowledge of the time dependent input signal. Therefore, a generic solution for this differential equation does not exist. Moreover, in a lot of applications the input signal amplitude is larger than the thermal voltage V_T. In this situation it is not possible to consider the base sheet resistance r_{sbi} and the total internal base Q_B bias independence. Thus in the fast switching applications, the bias dependence results also in a spatial dependence. Therefore, lumped representations of internal base region are not accurate for large-signal and fast switching.

References

[1] M. Schröter and A. Chakravorty, "Compact Hierarchical Bipolar Transistor Modeling with HICUM", World Scientific, 2010.

[2] R. L. Pritchard, "Two-Dimensional Current Flow in Junction Transistors at High Frequencies", Proc. IRE, vol. 46, pp. 1152-1160, 1958

Chapter 3

Description of used models

In this Chapter the executed simulations in static (DC) and in the small-signal high frequency analysis are described. In particular:

- in Subsection 3.1 the DEVICE software is described, along with its usefulness for the scope of the thesis;
- in Subsection 3.3 the classical HICUM/L2 version 3.0, the used procedure and the comparison between its results and those obtained by DEVICE are reported. In particular, the modification made in Verilog-A code to allow the use the charge partitioning factor is explained;
- in Subsection 3.4 the distributed HICUM/L2 version 3.0 composed by 10 internal transistors, its implementation and the comparison between its results and those determined by DEVICE are reported.

3.1 DEVICE simulation as reference

As previously mentioned, it was chosen to use 2D DEVICE simulations as reference instead of performing experiments, since measuring the large-signal switching behavior in bipolar transistors is a cumbersome task.

DEVICE is a program for numerical mixed-mode device and circuit simulation of semiconductor devices, including SiGe heterostructure transistors. The *Poisson's equation*, the *continuity equations for electrons and holes*, the *combined Poisson-continuity-transport equation for a single carrier type in frequency domain* and the *Schrödinger equation* can be solved by DEVICE. All the equations can be solved in different spatial dimensions (1D, 2D or 3D). Many different physical effects are taken into account. The device structure can be composed of an arbitrary number of regions with different physical properties.

DEVICE offers different operation modes, like:

- static or "quasi static" analysis, used for DC or small-signal analysis;
- transient analysis, with arbitrary signal functions at each contact;
- small-signal high-frequency analysis, which allows computing the elements of Y-, Z-, H- or S-parameter matrix.

3.2 HBT in DEVICE

The HBT under test has an emitter width amounting to 400 nm; as clarified above, DEVICE simulations are 2D, that is, the emitter length is assumed to be infinitesimal (**Fig. 14**).

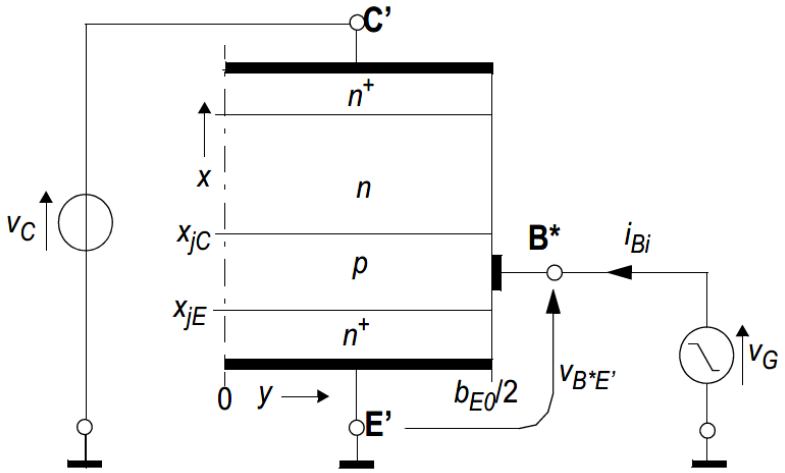
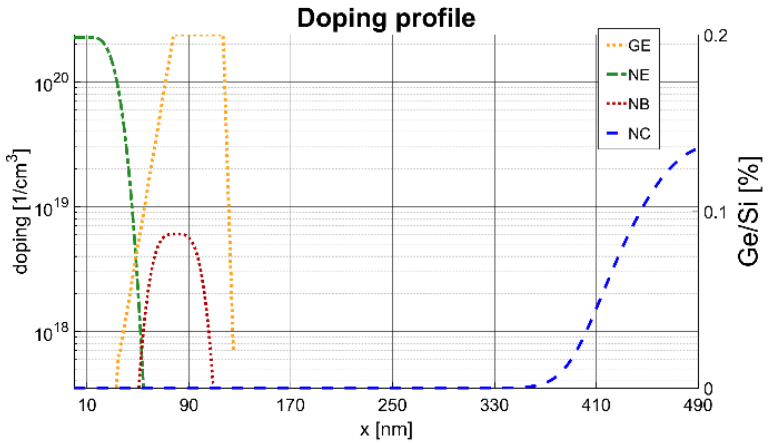
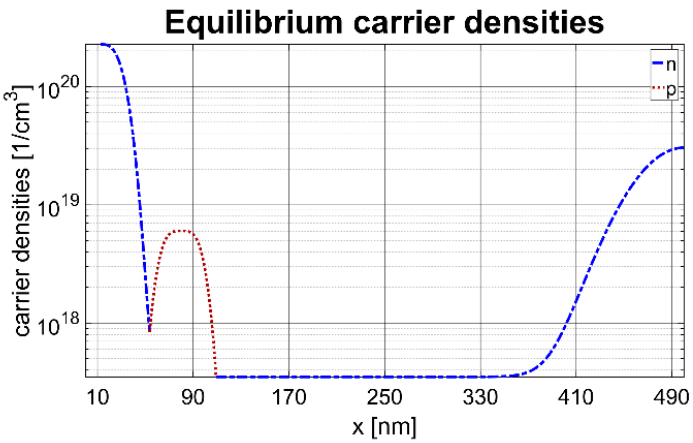


Fig. 14. *Reference structure simulated by DEVICE. For symmetry reasons, only half of the internal base region with the emitter window width b_{E0} needs to be considered. C', E' and B* are the internal collector node, the internal emitter node and the perimetric base node, respectively.*

The doping profile of the HBT is shown in **Fig. 15**.



(a)



(b)

Fig. 15. *Doping profile along the HBT (a), where the green dashed-dotted line is the emitter donor profile, the red dotted line is the base acceptor profile, the dashed blue line is the collector donor profile and the yellow dashed-dotted line is the percentage of germanium impurity profile, and equilibrium carrier densities (b).*

The considered equations for simulation are *Poisson's equation* and *continuity equations for electrons and holes*, while the other equations were deactivated.

In Appendix A the code used in DEVICE can be found.

3.3 HICUM 1-transistor implementation

3.3.1 Classical model

The HICUM 1-transistor (1-T) model implementation was performed using the Verilog-A file released from the University of Technology of Dresden and the University of California at San Diego. The used version was v3.0 of HICUM Level 2 (HICUM/L2). This Verilog-A file was compiled with Advanced Design System (ADS) of Keysight. After performing the simulation by DEVICE the parameters set for HICUM were extracted. The HBT HICUM parameters had been provided from University of Technology of Dresden. But a better extraction of some of them was necessary. The extraction procedure and the parameter values are reported in Appendix B. The accuracy of HICUM with calibrated parameters is witnessed by the comparison with DEVICE data in **Fig. 16** to **Fig. 19**.

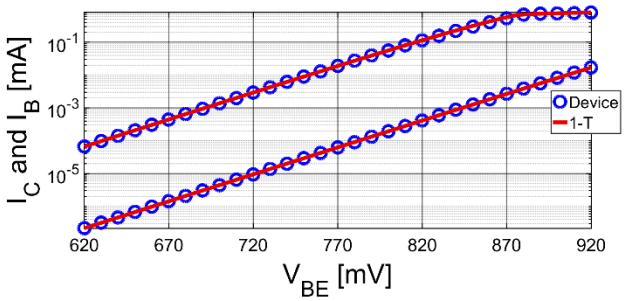
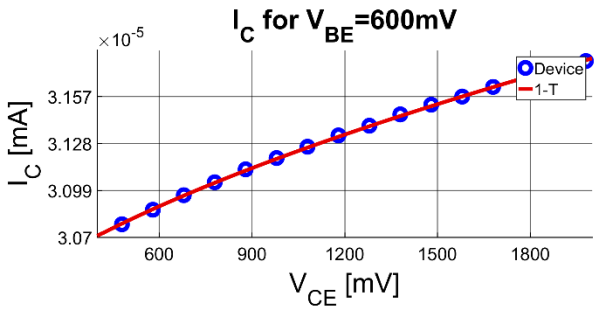
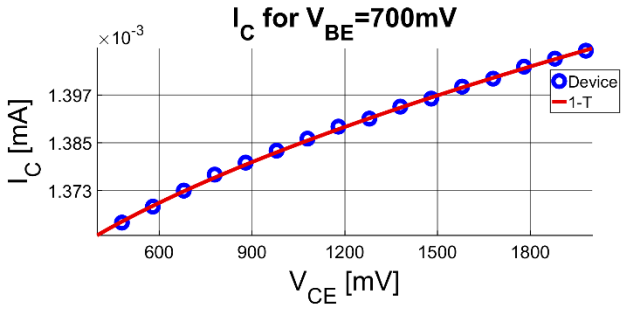


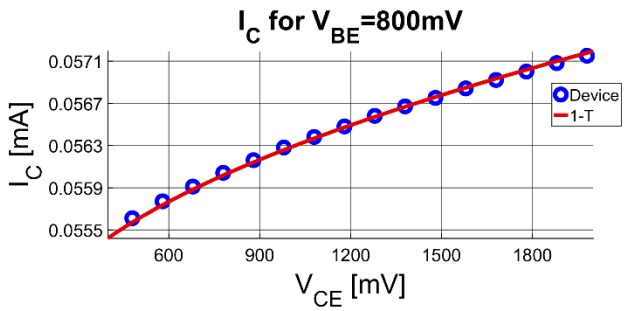
Fig. 16. *Gummel plot. The blue circles represent the DEVICE simulation, while the red solid line represents the HICUM 1-T model simulation.*



(a)

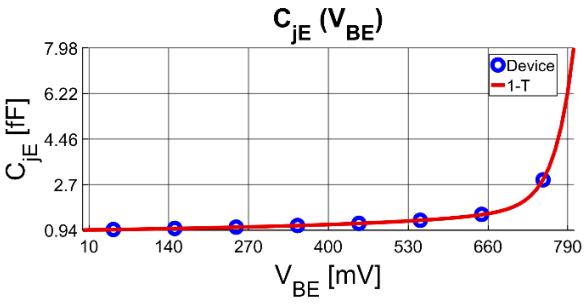


(b)

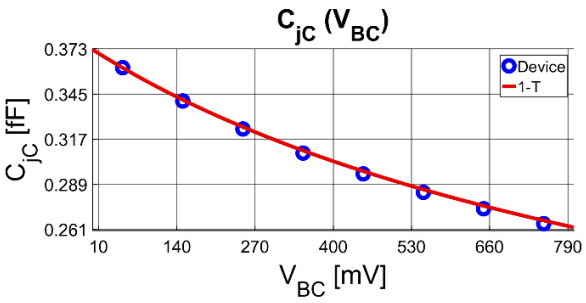


(c)

Fig. 17. *Collector current I_C as function of collector-emitter voltage V_{CE} for base-emitter voltage V_{BE}=600mV (a), V_{BE}=700mV (b) and V_{BE}=800mV (c). The blue circles represent the DEVICE simulation, while the red solid line represents the HICUM 1-T model simulation.*



(a)



(b)

Fig. 18. *Base-emitter junction capacitance C_{jE} as function of base-emitter voltage V_{BE} (a) and base-collector junction capacitance C_{jC} as function of base-emitter voltage V_{BC} (b). The blue circles represent the DEVICE simulation, while the red solid line represents the HICUM 1-T model simulation.*

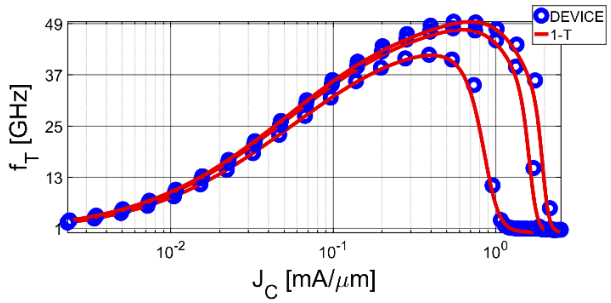


Fig. 19. *Transition frequency f_T as function of collector current I_C for different values of base-collector voltage V_{BC} (V_{BC}=500mV, V_{BC}=0V and V_{BC}=-500mV). The blue circles represent the DEVICE simulation, while the red solid line represents the HICUM 1-T model simulation.*

3.3.2 Model with charge partitioning factor

The HICUM/L2 1-T model with charge partitioning across the base resistance is a method conceived to efficiently describe the lateral dynamic ECC effects occurring in fast large-signal switching applications without resorting to a distributed approach. It must be remarked that the existing method conceived for DC ECC and for its quasi-static expression is based on the use of an internal base resistance r_{Bi}. However, this method is ineffective for large-signal switching applications because leads to inaccurate results. This inaccuracy will be shown in the next Chapter.

The charge partitioning across the internal quasi-static (i.e., DC) base resistance was implemented through the introduction of a new parameter α denoted as *charge partitioning factor* (**Fig. 5**).

Fig. 20 shows the implementation of factor α in Verilog-A.

```
I(br_bpei)      <+ type*ibep;
I(br_bpei)      <+ type*irep;
I(br_bpei)      <+ ddt(type*Qjep);
I(br_bpei)      <+ ddt(type*((Qdeix+Qjei)*alqb)); // added
I(br_biei)      <+ type*ibei;
I(br_biei)      <+ type*irei;
I(br_biei)      <+ type*ibh_rec;
I(br_biei)      <+ ddt(type*((Qdeix+Qjei)*(1-alqb))); // added only *(1-alqb)
I(br_bpsi)      <+ type*HSI_Tsu;
I(br_bpci)      <+ type*ijbcx;
I(br_bpci)      <+ ddt(type*(qjcx0_t_ii+Qdsu));
I(br_bpci)      <+ ddt(type*((Qdci+Qjci)*(alqb))); // added
I(br_be)        <+ ddt(cbepar1*V(br_be));
I(br_bpe)       <+ ddt(cbepar2*V(br_bpe));
I(br_bici)      <+ type*(ibci-iavl);
I(br_bici)      <+ ddt(type*((Qdci+Qjci)*(1-alqb)));// added only *(1-alqb)
I(br_sici)      <+ type*ijsc;
I(br_sici)      <+ ddt(type*Qjs);
I(br_sc)        <+ ddt(type*Qscp);
I(br_ciei)      <+ type*Itxf;
I(br_eici)      <+ type*itr;
```

Fig. 20. *Modified code for lateral charge partitioning factor α implementation in Verilog-A. In the code α is called al_{qb} and highlighted in yellow.*

3.4 HICUM 10-transistors implementation

The HICUM 10-transistor (10-T) model implementation was performed starting from the HICUM 1-T model with calibrated parameters. The internal emitter, base e collector nodes (E', B' and C', respectively) and the perimetric base node (B*) were defined as "output nodes" in Verilog-A file (**Fig. 21**) and the resulting Verilog-A file was compiled again. In the Verilog-A file the internal nodes are ei, bi and ci for internal emitter, base and collector node, respectively, while the perimetric base node is bp. Then the BJTs were connected as shown in **Fig. 22**.

```
module hicumL2va_ci_bp_bi_ei (c,ci,b,bp,bi,e,ei,s);

//Node definitions

inout           c,ci,b,bp,bi,e,ei,s;
electrical      c,b,e,s,ci,ei,bp,bi,si;
electrical      xf1,xf2;
electrical      xf;

electrical      tnode;

electrical      n1,n2;
```

Fig. 21. *Modified part of code of Verilog-A to define the internal emitter, base and collector nodes and the perimetric node as output nodes.*

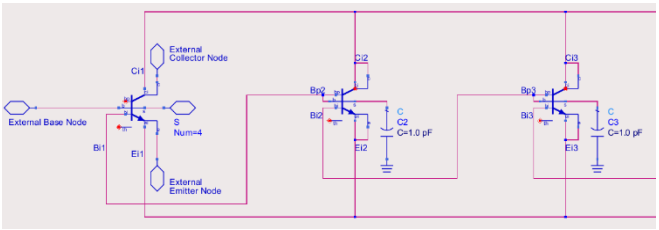


Fig. 22. *Schematic of 10-T model. Ci-m, Bi-m, Ei-m and Bp-m represent respectively the internal collector node, the internal base node, the internal emitter node and the perimetric base node of mth-transistor.*

In **Fig. 22** the schematic of the 10-T model is shown. Each transistor was numerated from 1 to 10 and the nodes were labeled as well (so the nodes Ei-m is the internal emitter node of mth-transistor). The BJTs

from 2 to 10 (only BJTs from the 1st to 3th are shown in **Fig. 22**) represent the internal BJTs of 10-T model from the 2nd to the 10th. In these BJTs, the perimetric parameters (as I_{bep}, I_{rep}, etc.) were set to zero, so just internal devices work. Moreover, all the internal and external emitter nodes of BJTs from 2 to 10 and the internal emitter node of the first BJT are shorted to each other. The same was performed for collector nodes. The internal and external emitter/collector nodes of each transistor from 2 to 10 are shorted each other because so the perimetric structure is bypassed. Moreover, all internal emitter/collector nodes of transistors from 2 to 10 are also shorted each other, as shown in **Fig. 7**. Regarding the base nodes, instead, each internal base node of mth BJT was shorted to perimetric base node of (m+1)th BJT. Therefore, an internal resistance appears in the base connections (in **Fig. 13** is the *dr* resistance).

Unlike the others transistors, the perimetric parameters of first transistor were set equal to extracted ones. So the first transistor works also as perimetric transistor and its external nodes are the accessible nodes of the 10-T model.

The parameters set for HICUM 10-T model were extracted starting from those of the standard α-less 1-T model. The used procedure to perform all is reported in Appendix B. The HICUM 10-T was tested using these parameters set and compared to DEVICE simulations. The results are reported in **Fig. 23** to **Fig. 26**.

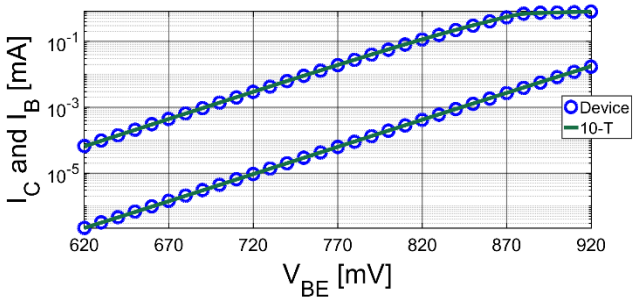
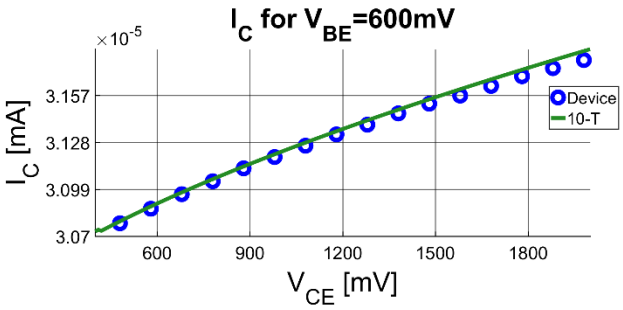
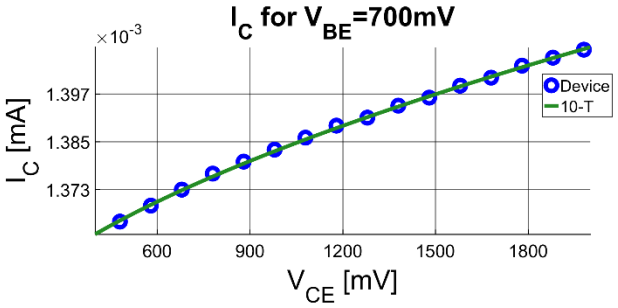


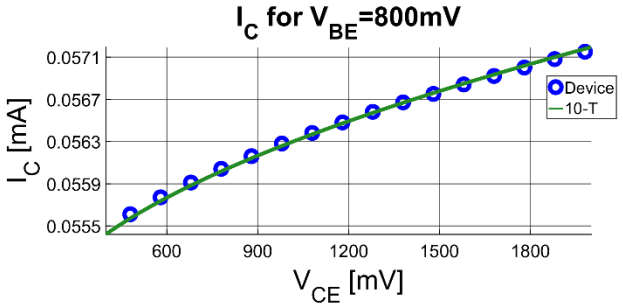
Fig. 23. *Gummel plot. The blue circles represent the DEVICE simulation, while the green dotted line represents the HICUM 10-T model simulation.*



(a)

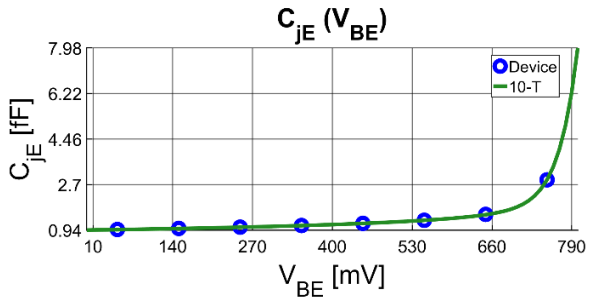


(b)

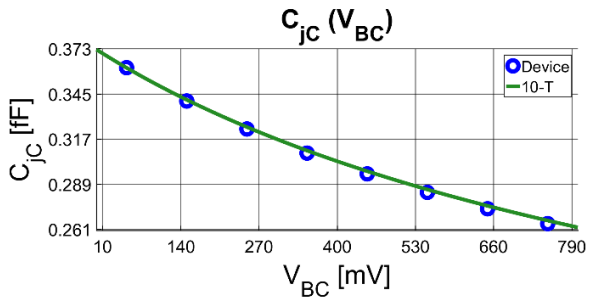


(c)

Fig. 24. *Collector current I_C as function of collector-emitter voltage V_{CE} for base-emitter voltage V_{BE}=600mV (a), V_{BE}=700mV (b) and V_{BE}=800mV (c). The blue circles represent the DEVICE simulation, while the green dotted line represents the HICUM 10-T model simulation.*



(a)



(b)

Fig. 25. *Base-emitter junction capacitance C_{jE} as function of base-emitter voltage V_{BE} (a) and base-collector junction capacitance C_{jC} as function of base-emitter voltage V_{BC} (b). The blue circles represent the DEVICE simulation, while the green dotted line represents the HICUM 10-T model simulation.*

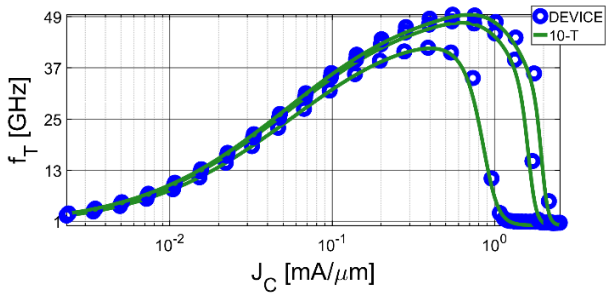


Fig. 26. *Transition frequency f_T as function of collector current I_C for different values of base-collector voltage V_{BC} (V_{BC}=500mV, V_{BC}=0V and V_{BC}=-500mV). The blue circles represent the DEVICE simulation, while the green dotted line represents the HICUM 10-T model simulation.*

Chapter 4

Model validations for large-signal switching applications

In this Chapter the tested models for large-signal high frequency applications are described. In particular:

- in Section 4.1 the simulations obtained using the 10-T model for large-signal high-frequency applications are compared to DEVICE simulations and HICUM/L2 1-T model. The focus of this comparison is to prove the 10-T model is a good reference for the aforementioned applications. This choice is due to the possibility in 10-T model to switch off the vertical NQS effects, which is not allowed in DEVICE. Switching off the vertical NQS effects allows studying the individual impact of the dynamic ECC;
- in Section 4.2 the HICUM/L2 model with charge partitioning factor is shown as new approach for large-signal high-frequency applications. This improved 1-T model is compared to the 10-T model by switching off the vertical NQS effects.

In all simulations, the applied signal is:

$$v_{sig} = V_{max}\left(1 - e^{(t/\tau)^2}\right) \text{ with } \tau = \frac{\sqrt{2}}{2\pi f} e^{1/2} \tag{41}$$

where V_{max} is the maximum voltage swing and its value changes from 5mV to 200mV. The choice of V_{max} values was made to analyze the models for both small-signal and large-signal applications. The input signal is added up to the DC base-emitter bias V_{BE}.

The simulations are performed using different bias points. In particular, the chosen base-emitter bias V_{BE} values are:

- $V_{BE} = 670mV$ to examine large-signal turn-on processes in a wide current-range. This because, looking at the Gummel plot (**Fig. 16** and **Fig. 23**), this bias is the begin of linear region of the HBT. At this voltage the transistor can still be considered off. The widest input current-swing is applicable in turn-on processes because this is the lowest point of linear region;
- $V_{BE} = 770mV$ to examine large-signal turn-on and turn-off processes at the medium-current regime.
- $V_{BE} = 870mV$ to examine large-signal turn-off processes in a wide current-range. This because, looking at the Gummel plot (**Fig. 16** and **Fig. 23**), this voltage is the end of linear region of the HBT. The widest input current-swing is applicable in turn-off processes because this is the highest point of linear region;

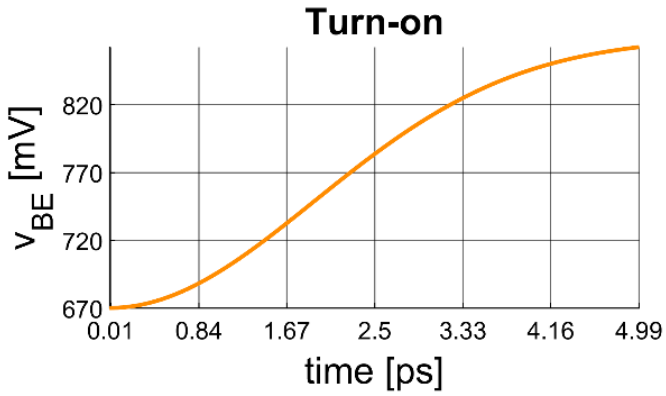
Instead, the collector-emitter bias V_{CE} values are $1V$ and $2V$, chosen to show the circuit operation at different bias.

At the end, $f=f_{T,max}$ is chosen. This choice is due to stress the circuit by very fast signals.

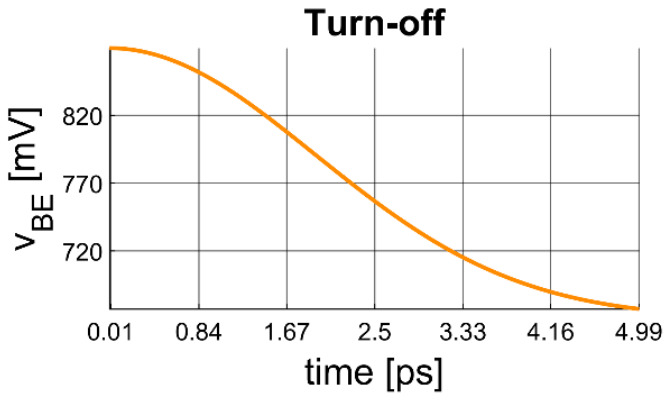
4.1 HICUM/L2 10-T model for large-signal switching applications

In this Section the simulations performed with the 10-T model is compared to those obtained by DEVICE and by the standard 1-T model. This comparison is performed to show that the 10-T model is a good reference for large-signal applications at very high frequencies, because this model fits very well with DEVICE ones. It is important to underline that, in this thesis, *turn-on process* and *turn-off process* do not have the classical meaning. Here turn-on process is defined more easily to be when a signal *is added* to applied bias in input, while *turn-off process* when a signal *is subtracted* to applied bias. In **Fig. 27** the differences from these two processes are explained. In **Fig. 27** *(a)* the transitory of turn-on process is shown; in this case a signal with maximum amplitude $V_{max}=200mV$ *is added* to the bias $V_{BE}=670mV$ and the base-emitter voltage V_{be} changes from $670mV$ to $870mV$ in about $5ps$. Indeed, in **Fig. 27** *(b)* the transitory of turn-off process is shown; in this case a signal with maximum amplitude $V_{max}=200mV$ *is subtracted* to the bias $V_{BE}=870mV$ and the base-emitter voltage V_{be} changes from $870mV$ to $670mV$ in the same time. In this voltage range the collector current I_c of the HBT goes from about 500nA at $V_{BE}=670mV$ to about 1mA at $V_{BE}=870mV$, i.e., it changes about 7 orders of magnitude.

For the sake of clarity, the turn-on and turn-off processes are separated in the following.



(a)



(b)

Fig. 27*. Turn-on (a) and turn-off (b) processes*

4.1.1 Turn-on process

In the turn-on process the maximum voltage swing V_{max}, defined in (41), is added to bias and the *total* base-emitter voltage V_{be}(t) is shown in **Fig. 27** *(a)*.

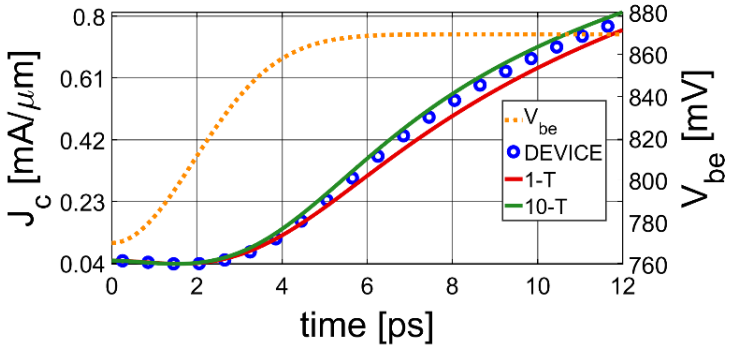
In the following plots collector and base current densities (J_c and J_b, respectively) are shown. In particular, blue circles represent DEVICE simulation, red solid lines the HICUM/L2 with 1-T model and green solid lines the 10-T model; their axis reference is the left y-axis. Instead, the orange dotted lines represent the applied base-emitter voltage V_{be} and its axis reference is the right y-axis.

Results and plots – medium-current regime

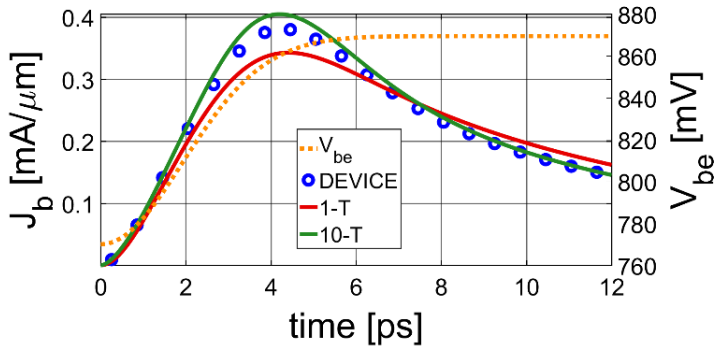
The following plots represent the simulations at medium-current regime, i.e., for $V_{BE}=770mV$. The two figures were chosen because:

- the first one (**Fig. 28**) is obtained for $V_{max}=100mV$ and $V_{CE}=1V$. This V_{max} value is the maximum voltage swing used for this bias. In this figure is possible to observe the good fitting of 10-T model and the inaccuracy of the 1-T model with respect to DEVICE simulation;
- the second one (**Fig. 29**) is obtained for $V_{max}=75mV$ and $V_{CE}=2V$. This figure was chosen to show the good fitting of 10-T model and the inaccuracy of 1-T model with respect to DEVICE simulation for this V_{CE} value as well.

In both these figures is possible to observe the good fitting of 10-T model and the deviation of 1-T model with respect to DEVICE simulations.

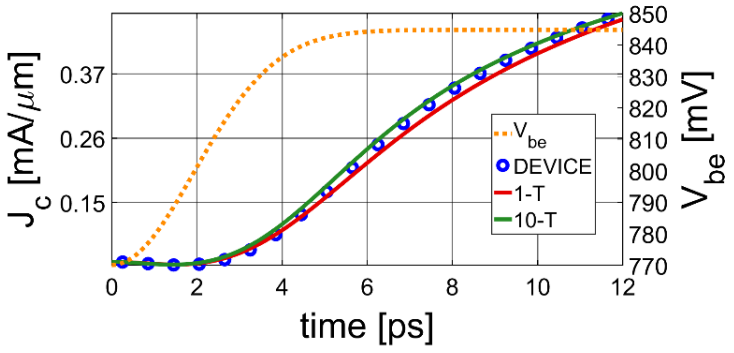


(a)

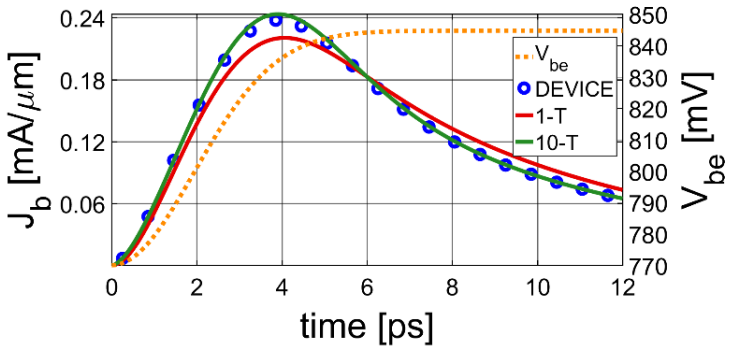


(b)

Fig. 28. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-on at V_{CE}=1.0V and V_{BE}=770mV. The applied signal has an amplitude V_{max}=100mV and a frequency of f=50GHz.*



(a)



(b)

Fig. 29. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-on at V_{CE}=2.0V and V_{BE}=770mV. The applied signal has an amplitude V_{max}=75mV and a frequency of f=50GHz.*

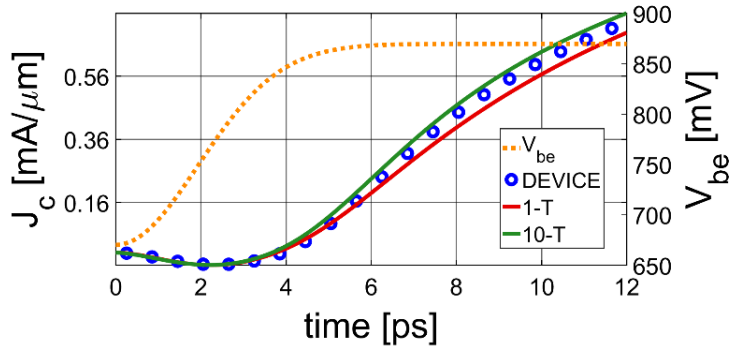
Results and plots - large-signal turn-on processes in a wide current-range

The following plots represent the simulations at large-signal turn-on processes in a wide current-range, i.e., for $V_{BE}=670mV$. This bias point is the begin of linear region of HBT under test.

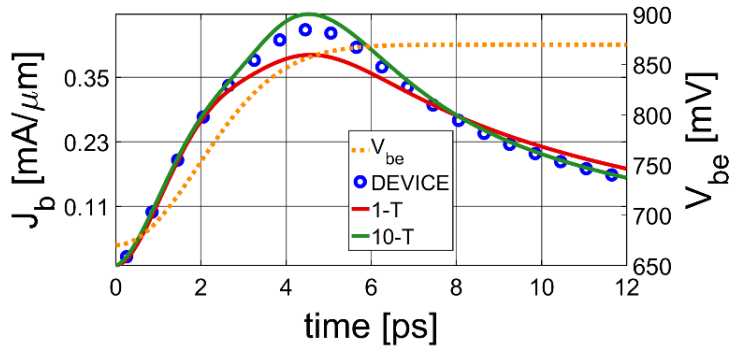
The two figures were chosen because:

- the first-one (**Fig. 30**) is obtained for $V_{max}=200mV$ and $V_{CE}=1V$. This V_{max} value is the maximum voltage swing used for this bias. In this figure is possible to observe the good fitting of the 10-T model and the inaccuracy of 1-T model with respect to DEVICE simulation;
- the second-one (**Fig. 31**) is obtained for $V_{max}=175mV$ and $V_{CE}=2V$. This figure was chosen to show the good fitting of 10-T model and the inaccuracy of 1-T model with respect to DEVICE simulation for this V_{CE} value as well.

In both these figures is possible to observe the good fitting of 10-T model and the deviation of 1-T model with respect to DEVICE simulations.

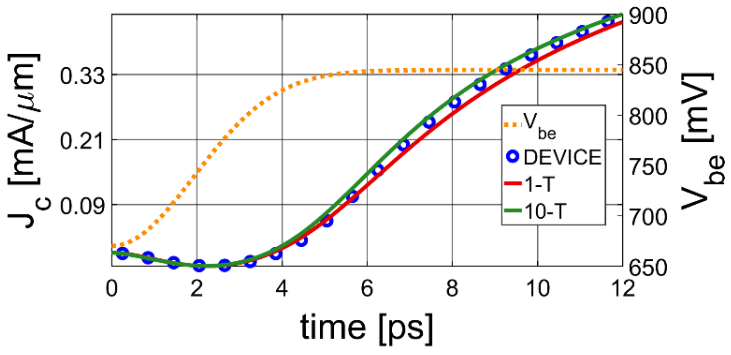


(a)

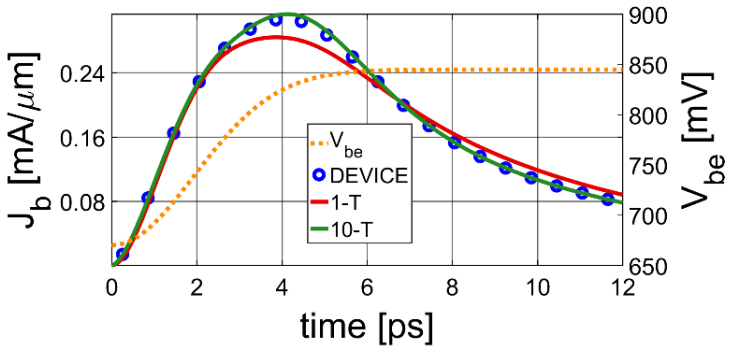


(b)

Fig. 30. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-on at V_{CE}=1.0V and V_{BE}=670mV. The applied signal has an amplitude V_{max}=200mV and a frequency of f=50GHz.*



(a)



(b)

Fig. 31. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-on at V_{CE}=2.0V and V_{BE}=670mV. The applied signal has an amplitude V_{max}=175mV and a frequency of f=50GHz.*

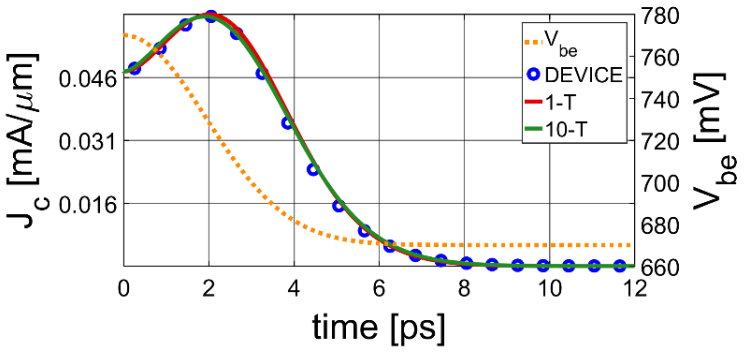
4.1.2 Turn-off process

In the turn-off process the maximum voltage swing V_{max}, defined in (41), is subtracted to bias and the base-emitter voltage V_{be}(t) is shown in **Fig. 27** *(b)*.

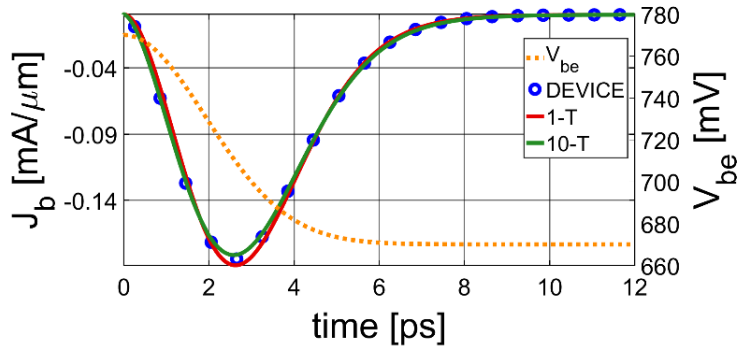
In the following plots collector and base current densities (J_c and J_b, respectively) are shown. In particular, blue circles represent DEVICE simulation, red solid lines the HICUM/L2 1-T model and green solid lines the 10-T model; their axis reference is the left y-axis. Instead, the orange dotted lines represent the applied base-emitter voltage V_{be} and its axis reference is the right y-axis.

Results and plots – medium-current regime

The following plot represents a simulation at medium-current regime, i.e., for $V_{BE}=770mV$. In this Section only one figure (**Fig. 32**) is shown because, even if it is obtained for $V_{max}=100m$, which represents the maximum voltage swing for this bias, it is possible to observe the good fitting of both 10-T and 1-T models with respect to DEVICE simulation. So the other simulations would not have given any more information. This figure shows that at medium-current regime the turn-off process is good even if modeled with the standard HICUM/L2 1-T model. This fitting is because, taking in consideration the second term of in (40), it is negligible in this case. Moreover, the base sheet resistance r_{sbi} and the total internal base Q_B can be consider bias independence. When it happens, (40) becomes (7). So, in this situation the HICUM 1-T model gives good results.



(a)



(b)

Fig. 32. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-off at V_{CE}=1.0V and V_{BE}=770mV. The applied signal has an amplitude V_{max}=100mV and a frequency of f=50GHz.*

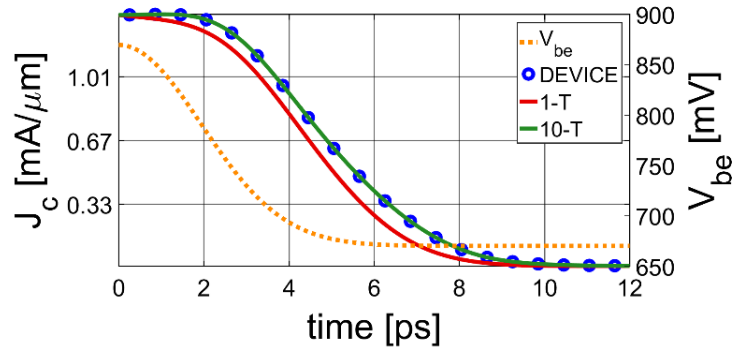
Results and plots - large-signal turn-off processes in a wide current-range

The following plots represent the simulations at large-signal turn-off processes in a wide current range, i.e., for $V_{BE}=670mV$. The two figures were chosen because:

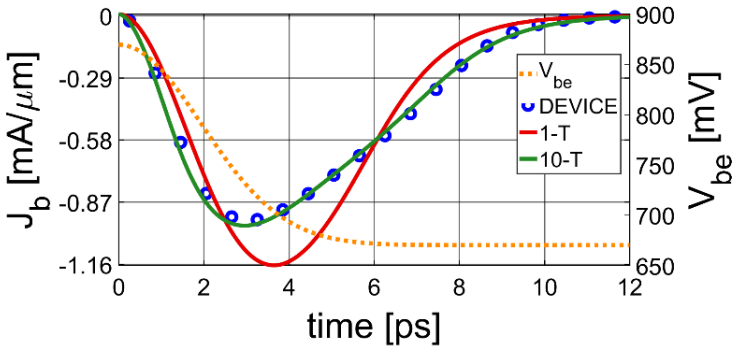
- the first one (**Fig. 33**) is obtained for $V_{max}=200mV$ and $V_{CE}=1V$. This V_{max} value is the maximum voltage swing used for this bias;
- the second one (**Fig. 34**) is obtained for $V_{max}=75mV$ and $V_{CE}=2V$. This figure was chosen because the V_{max} value is the minimum voltage swing used for this bias.

In both these figures is possible to observe the good fitting of 10-T model and the deviation of 1-T model with respect to DEVICE simulations. So the simulations obtained by HICUM/L2 1-T model in large signal turn-off processes in a wide current range do not fit well and a new model needs to be developed.

Unlike shown in previous case, in this case the HICUM/L2 1-T model does not give good result. This because, in this case, the second term of in (40) is not negligible anymore.

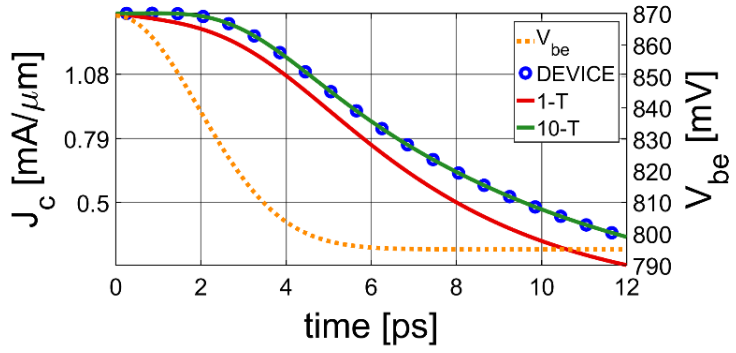


(a)

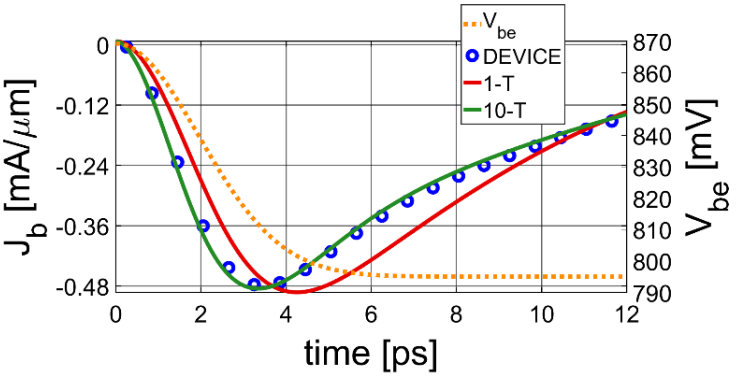


(b)

Fig. 33. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-off at V_{CE}=1.0V and V_{BE}=870mV. The applied signal has an amplitude V_{max}=200mV and a frequency of f=50GHz.*



(a)



(b)

Fig. 34. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-off at V_{CE}=2.0V and V_{BE}=870mV. The applied signal has an amplitude V_{max}=75mV and a frequency of f=50GHz.*

4.1.3 Observations

As can be inferred from **Fig. 28** to **Fig. 34**, the 10-T model offers a very good fitting with respect to DEVICE simulations for large-signal switching applications. This does not happen for 1-T model, where the figures show a mismatch for these applications. This mismatch is due to the inherent structure of the 1-T. This was shown in Subsections 2.2.1 and 2.2.2, where the passage from distributed model to HICUM/L2 1-T model was described. Indeed, in those Subsections the static and small-signal hypothesis were made to arrive to a distributed description of ECC effects.

Now, instead, the large-signal applications have been analyzed. So the hypothesis under which the model was developed are no longer valid. However, it has been shown also that HICUM/L2 10-T model provides good results. This could be expected. Indeed, in Section 2.1 how to go from physical BJT description to a distributed model was described.

By virtue of this agreement with DEVICE simulations, the 10-T model was taken as reference hereinafter to develop the improved 1-T model equipped with charge partitioning factor. This choice is due to the possibility to switch-off the vertical NQS effects in the 10-T model, which – as mentioned before – was not possible in DEVICE. The switching-off of vertical NQS effects allows focusing only on dynamic ECC effects.

4.2 HICUM/L2 1-T model with charge partitioning factor for large-signal switching applications

4.2.1 Estimation procedure for lateral charge partitioning factor

In this subsection the procedure to estimate the time shift Δt, time constant τ_{rB} and the lateral charge partitioning factor α are described. All obtained values for all executed simulations are reported in 0.

Change of reference model

The first step for the estimation of lateral charge partitioning factor α was to separate the vertical NQS effects from dynamic ECC (or also known as lateral NQS effects). Indeed, this separation is not possible in DEVICE, where all these effects are present. But it is accomplished by using a HICUM/L2 10-T model. Indeed, as shown in Subsection 4.1, the 10-T model has a good fitting with DEVICE for modeling large-signal switching applications at high frequencies and, moreover, unlike DEVICE, in 10-T model is possible switch-off the vertical NQS effects and consider only the lateral NQS effects.

Lateral charge partitioning factor description

For the internal transistor considered here and without vertical NQS effects, in an 1-T model with DC internal base resistance the time constant τ_{rB} determining $i_C(t)$ and $i_B(t)$ is given by:

$$\tau_{rB} = r_{Bi}(C_c + C_e) \tag{42}$$

where C_c+C_e is the total capacitance connected to the internal base node B' (as shown in **Fig. 5**). The approach therefore consists in changing the time constant τ_{rB} by the time shift Δt between the 1-T compact model and the 10-T model. This leads to the new internal time constant:

$$\tau'_{rB} = \tau_{rB} - \Delta t = \tau_{rB}\left(1 - \frac{\Delta t}{\tau_{rB}}\right) = \tau_{rB}(1-\alpha)$$
$$\text{with } \alpha = \frac{\Delta t}{\tau_{rB}} \in [0,1] \tag{43}$$

Because the time shift Δt and the internal time constant τ_{rB} are function of the collector current $i_C(t)$, they are evaluated at 50% of the maximum current swing. This ensures also the correct delay time in the large-signal circuit applications such as the jitter in eye diagrams.

Time shift evaluation procedure

The following procedure was performed to estimate the time shift Δt at 50% of maximum current swing:

- the collector current values at initial time t=0 and final time $t \to +\infty$ of transient analysis was taken into consideration. In particular, it was defined:

$$i_{C,i} = i_C(t=0)$$
$$i_{C,f} = i_C(t \to +\infty) \tag{44}$$

- the collector current at 50% of maximum current swing was defined as:

$$i_{C,50\%} = \frac{i_{C,f} + i_{C,i}}{2} \tag{45}$$

- $t_{50\%,1TM}$ and $t_{50\%,10TM}$ were defined as being the time instants where the collector current obtained by 1-T model (i.e., $i_{C,1TM}$) and that obtained by 10-T model (i.e., $i_{C,10TM}$) respectively, were equal to collector current at 50% of maximum current swing, i.e.:

$$\begin{aligned} i_{C,1TM}(t = t_{50\%,1TM}) &= i_{C,50\%} \\ i_{C,10TM}(t = t_{50\%,10TM}) &= i_{C,50\%} \end{aligned} \tag{46}$$

- the time shift Δt at 50% of maximum current swing is equal to:

$$\Delta t_{50\%} = t_{50\%,1TM} - t_{50\%,10TM} \tag{47}$$

Time constant evaluation procedure

The following procedure was performed to estimate the time constant τ_{rB}:

- the voltage v_{Bp} on perimetric base node B^* at instant time $t=t_{50\%,1TM}$ and the voltage v_{Bi} on internal base node B' at same instant time were measured;
- the current i_{Bi} through internal base resistance r_{Bi} at same instant time was measured;
- the internal base resistance r_{Bi} was obtained as:

$$r_{Bi} = \frac{v_{Bp} - v_{Bi}}{i_{Bi}} \tag{48}$$

- the admittance matrix Y was simulated;
- the total internal junction capacitance C_{ji} was obtained as:

$$C_{ji} = \frac{imag(Y_{11})}{2\pi f} \tag{49}$$

- the time constant τ_{rB} was obtained as:

$$\tau_{rB} = r_{Bi} C_{ji} \tag{50}$$

4.2.2 Turn-on process

As already described in Subsection 4.1.1, in turn-on process the maximum voltage swing V_{max}, defined in (41), is added to bias and the *total* base-emitter voltage V_{be}(t) is shown in **Fig. 27** *(a)*.

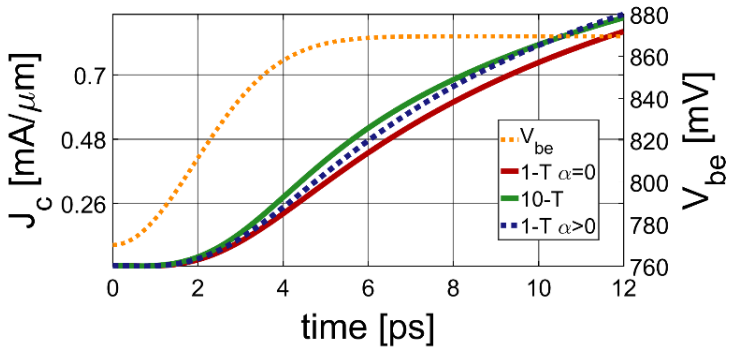
In the following plots collector and base current densities (J_c and J_b, respectively) are shown. In particular, red solid lines represent simulations obtained by the HICUM/L2 1-T model with partitioning charge factor $\alpha=0$, green solid lines represent those obtained by the 10-T model and the dark blue dotted lines those obtained by HICUM/L2 1-T model with partitioning charge factor $\alpha>0$. The reference of these plots are the left y-axis. Instead, the orange dotted lines represent the applied base-emitter voltage V_{be} and their reference is the right y-axis.

Results and plots – medium-current regime

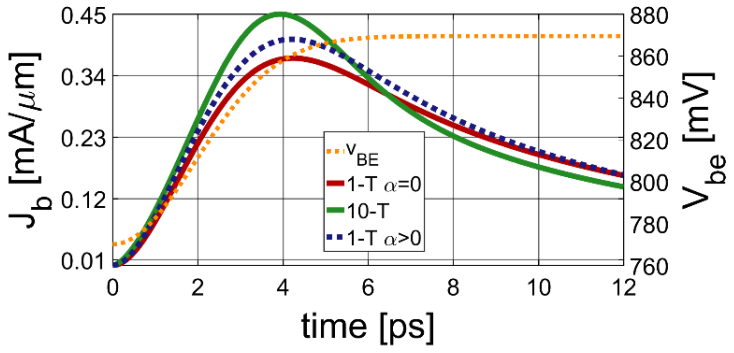
The following plots represent the simulations at medium-current regime, i.e., for $V_{BE}=770mV$. In particular:

- **Fig. 35** is obtained for $V_{max}=100mV$ and $V_{CE}=1V$. This V_{max} value is the maximum voltage swing used for this bias. The found charge partitioning factor is $\alpha=0.131$;
- **Fig. 36** is obtained for $V_{max}=75mV$ and $V_{CE}=2V$. The found charge partitioning factor is $\alpha=0.114$;

The bias and the V_{max} value chosen for these simulations are equal to those made in Subsection 4.1.1.

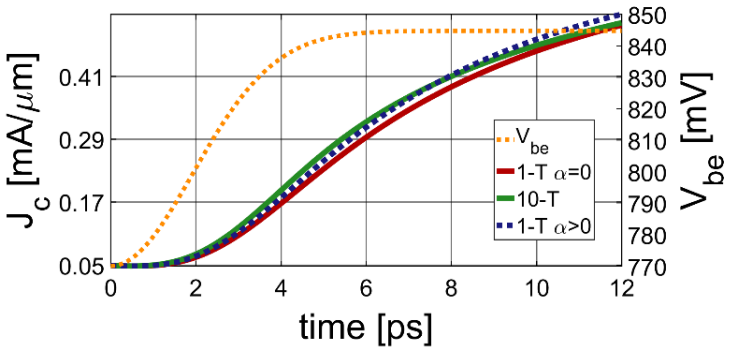


(a)

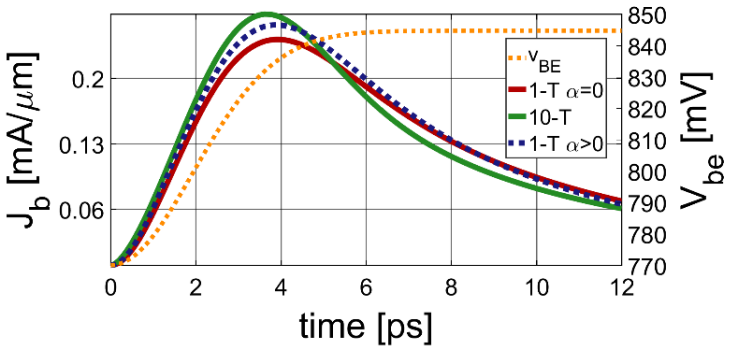


(b)

Fig. 35. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-on at V_{CE}=1.0V and V_{BE}=770mV without VNQS effects. The applied signal has an amplitude V_{max}=100mV and a frequency of f=50GHz. The charge partitioning factor is α=0.131.*



(a)



(b)

Fig. 36. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-on at V_{CE}=2.0V and V_{BE}=770mV without VNQS effects. The applied signal has an amplitude V_{max}=75mV and a frequency of f=50GHz. The charge partitioning factor is α=0.113.*

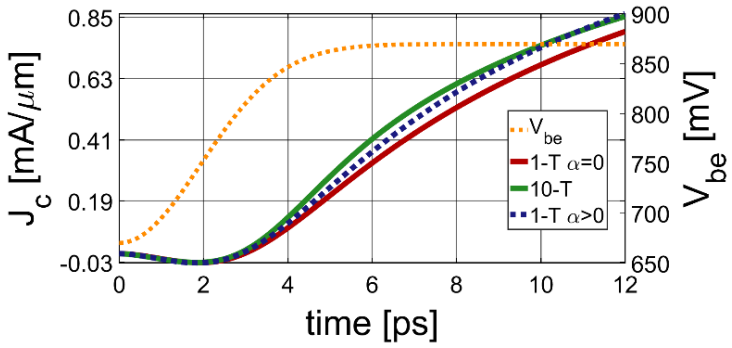
In **Fig. 35** and **Fig. 36** it is possible to observe an improvement of HICUM/L2 with partitioning factor with respect to HICUM/L2 without partitioning factor. It is important to underline that these simulations were obtained with a constant α value. Indeed, α was calculated for one specific point (i.e., at 50% of maximum current swing), and the perfect compensation happen in this point. Changing α, also the characteristic of 1-T model with charge partitioning factor changes. Another significant improvement can be obtained describing α as a function of some input variables. It is worth noting that, due to (50), the time constant τ_{rB} is already described as function of input variables. It follows that only the time shift Δt must be described as a function of input variables to have a good description of charge partitioning factor α.

Results and plots - large-signal turn-on processes in a wide current-range

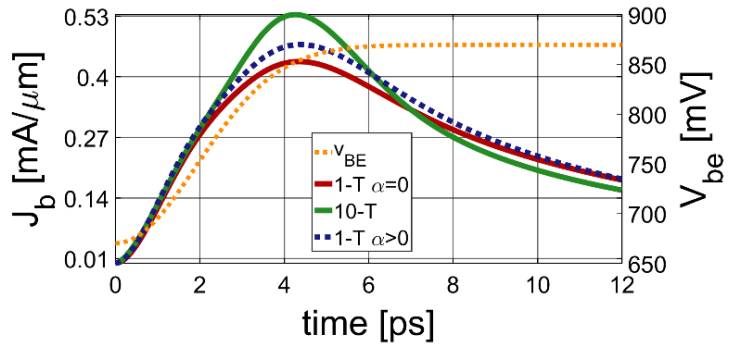
The following plots represent the simulations at large signal turn-on processes in a wide current range, i.e., for $V_{BE}=670mV$. In particular:

- **Fig. 37** is obtained for $V_{max}=200mV$ and $V_{CE}=1V$. This V_{max} value is the maximum voltage swing used for this bias The found charge partitioning factor is $\alpha=0.137$;
- **Fig. 38** is obtained for $V_{max}=175mV$ and $V_{CE}=2V$. The found charge partitioning factor is $\alpha=0.114$.

The bias and the V_{max} value chosen for these simulations are equal to those made in Subsection 4.1.1.

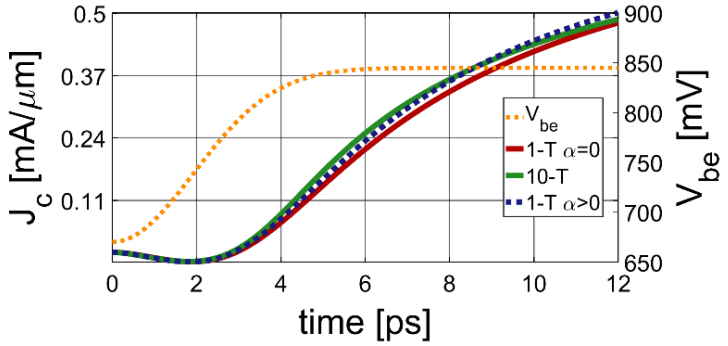


(a)

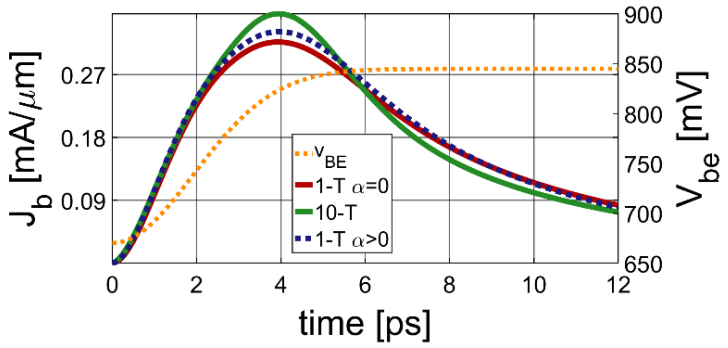


(b)

Fig. 37. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-on at V_{CE}=1.0V and V_{BE}=670mV without VNQS effects. The applied signal has an amplitude V_{max}=200mV and a frequency of f=50GHz. The charge partitioning factor is α=0.137.*



(a)



(b)

Fig. 38. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-on at V_{CE}=2.0V and V_{BE}=670mV without VNQS effects. The applied signal has an amplitude V_{max}=175mV and a frequency of f=50GHz. The charge partitioning factor is α=0.113.*

As shown for medium current regime, also in this case in **Fig. 37** and **Fig. 38** it is possible to observe an improvement of the 1-T model with partitioning factor with respect to that without partitioning factor. It is important to highlight that these simulations were obtained with a constant α value. Another significant improvement is probably obtainable describing α as function of some variables.

4.2.3 Turn-off process

As already described in Subsection 4.1.2, in the turn-off process the maximum voltage swing V_{max}, defined in (41), is subtracted to bias and the base-emitter voltage V_{be}(t) of transistor is shown in **Fig. 27** *(b)*.

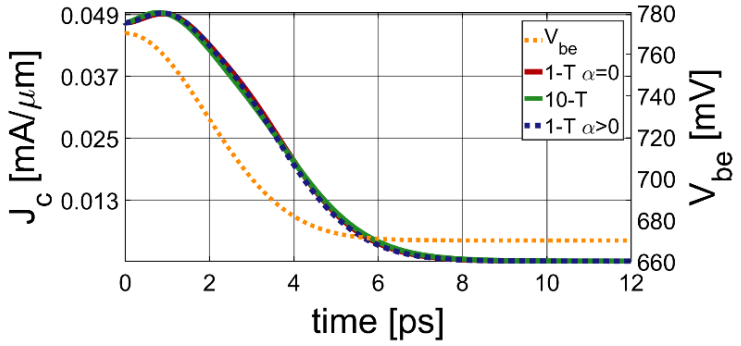
In the following plots collector and base current densities (respectively J_c and J_b) are shown. In particular, red solid lines represent simulations obtained by the HICUM/L2 1-T model with partitioning charge factor $\alpha=0$, green solid lines represent those obtained by the 10-T model and the dark blue dotted lines those obtained by HICUM/L2 1-T model with partitioning charge factor $\alpha>0$. The reference of these plots are the left y-axis. Instead, the orange dotted lines represent the applied base-emitter voltage V_{BE} and their reference is the right y-axis.

Results and plots – medium-current regime

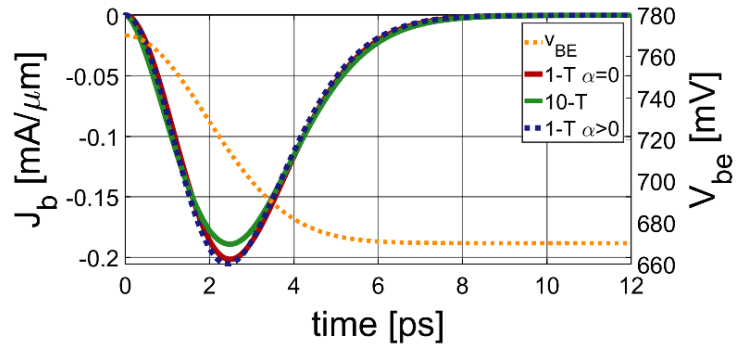
The following plot represents a simulation at medium current regime, i.e., for $V_{BE}=770mV$. As shown in **Fig. 32** of previous subsection, also here only one figure (**Fig. 39**) is represented. As observed in **Fig. 32**, both 10-T and 1-T models show a good fitting with respect to DEVICE simulation, even if this simulation is obtained for $V_{max}=100m$, that represents the maximum voltage swing for this bias. So the other simulations would not have given any more information. This figure shows that at medium current regime the turn-off process is already good modeled from HICUM/L2 1-T model. This fitting is because, taking in consideration the second term of in (40), it is negligible in this case. Moreover, the base sheet resistance r_{sbi} and the total internal base Q_B can be consider bias independence. When it happens, (40) becomes (7). So, in this situation the HICUM 1-T model gives good results.

As it can be expected in these cases, the simulations obtained by HICUM/L2 1-T with charge partitioning factor lead to the same

behavior as those obtained by HICUM/L2 without charge partition factor. The found charge partitioning factor is $\alpha=0.039$.



(a)



(b)

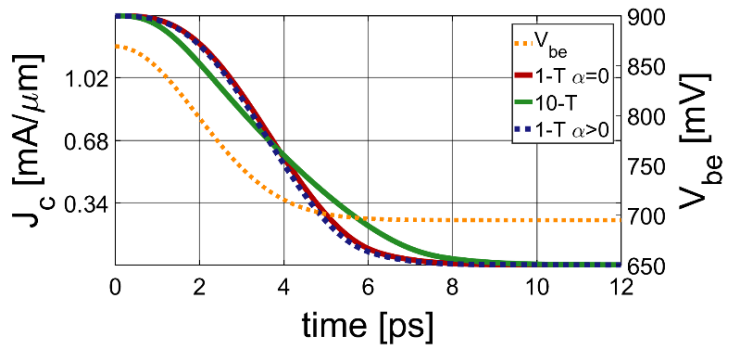
Fig. 39. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-off at V_{CE}=1.0V and V_{BE}=770mV without VNQS effects. The applied signal has an amplitude V_{max}=100mV and a frequency of f=50GHz. The charge partitioning factor is α=0.039.*

Results and plots - large-signal turn-on processes in a wide current-range

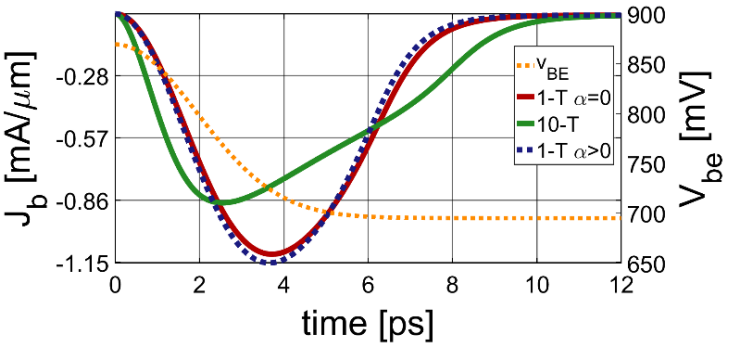
The following plots represent the simulations at large signal turn-off processes in a wide current-range, i.e., for $V_{BE}=670mV$. In particular:

- **Fig. 40** is obtained for $V_{max}=200mV$ and $V_{CE}=1V$. The found charge partitioning factor is $\alpha=0.009$;
- **Fig. 41** is obtained for $V_{max}=75mV$ and $V_{CE}=2V$. The found charge partitioning factor is $\alpha=0.010$.

The bias and the V_{max} value chosen for these simulations are the same of those made in Subsection 4.1.2.

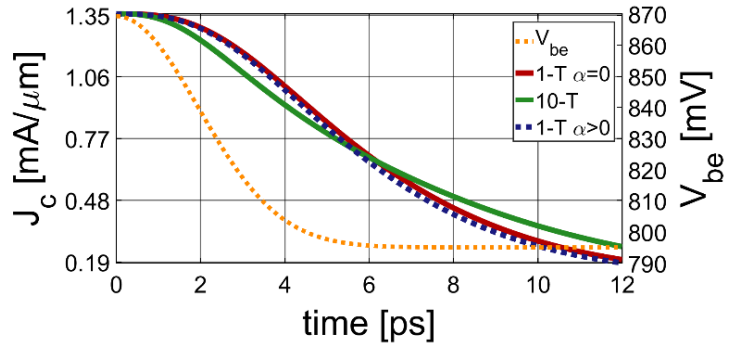


(a)

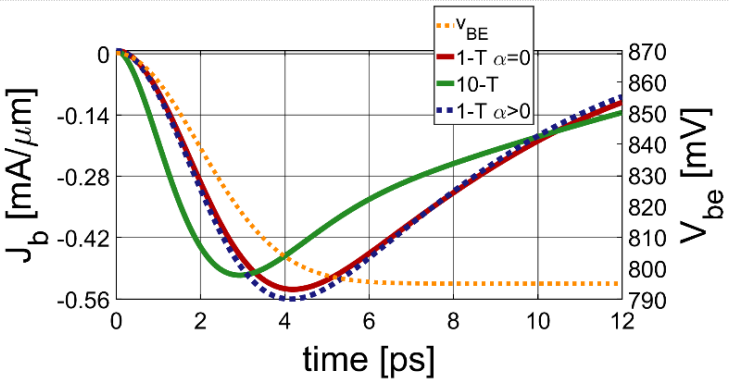


(b)

Fig. 40. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-off at V_{CE}=1.0V and V_{BE}=870mV without VNQS effects. The applied signal has an amplitude V_{max}=200mV and a frequency of f=50GHz. The charge partitioning factor is α=0.009.*



(a)



(b)

Fig. 41. *Time dependent collector current density J_c (a) and base current density J_b (b) during turn-off at V_{CE}=2.0V and V_{BE}=870mV without VNQS effects. The applied signal has an amplitude V_{max}=75mV and a frequency of f=50GHz. The charge partitioning factor is α=0.010.*

In large-signal turn-off processes in a wide current range the simulations by the 1-T model with charge partitioning factor do not have large improvement if it is compared with the counterpart without charge partitioning factor. The reason of this is due to the fact that the simulations by HICUM/L2 10-T and HICUM/L2 1-T without partitioning factor intersect each other almost at 50% of the maximum current swing. This implies that time shift Δt (evaluated in same point) is almost zero and with it also the charge partitioning factor α is almost zero (*0.009* and *0.010* for **Fig. 40** and **Fig. 41**, respectively). **Fig. 40** and **Fig. 41** were obtained with α almost zero and the 1-T model with charge partitioning factor has the same results of those without. Changing the value of the charge partitioning factor α would have changed the results of the improved 1-T model. So a description of charge partitioning factor α as function of input variables would allow obtaining better results.

Chapter 5

Conclusions

The coming of bipolar transistor in silicon-germanium heterojunction (SiGe HBTs) has allowed to keep the benefits of silicon, while increasing the performances at high frequencies applications. Therefore, there has been an increasing demand of HBTs.

In this thesis a problem that in last years has become very relevant was faced up, i.e., the modeling of the HBTs in SiGe for large-signal high-frequency applications.

Starting from the physical description of base-emitter junction in a BJT, it has come to a distributed description. For the assumptions made, the distributed model of the HBTs has to provide good results for static, small-signal and large-signal operations. To prove the validity of this, a distributed model was implemented in ADS. It was chosen to use 10 transistors to represent this distributed model. This number was chosen after some analyses. Indeed, improving the transistors number caused only an increase in computational burden and, therefore, the simulation time. But reducing the number causes a not so good transistor modeling.

After choosing the number of transistors, the distributed model (renamed 10-T model for the number of its internal transistors) was tested before in static, then in small-signal operations. The obtained results were compared with respect to the DEVICE simulations and the good overlap proves that this model is a valid description of the HBTs in static and small-signal operations.

Next step was to test the 10-T model in large-signal high speed operations. Also in this case the results obtained by this model show a good overlap with respect to DEVICE simulations. All of these

considerations have permitted to choose the HICUM 10-T model as new references, because:

- its simulations are faster than DEVICE ones;
- in it switching off the vertical NQS effects is possible, allowing to focus the analysis just on the dynamic ECC effects.

Even if the HICUM 10-T model is much faster than DEVICE, it is still too slow for practical large-signal high speed applications.

For this reason, the development of a new compact model becomes necessary. To perform this, the analysis was split into three different cases: static, small-signal and large-signal operations. Starting from distributed model, the mathematical approach of ECC effects for static and small-signal operation brought to a compact model description. This description uses a bias-depend internal base resistance r_{Bi} for static operation, while introduce an internal base capacitance C_{rBi} in parallel to r_{Bi} for small-signal operation. The internal base resistance r_{Bi} and the internal base capacitance C_{rBi} are already implemented in classical HICUM/L2 1-T model. But it is important to underline that in this same Subsection a new approach was proposed for small-signal application: partitioning the internal junction charge on internal base resistance r_{Bi}, using the partitioning factor (**Fig. 5** and **Fig. 12**). Also the mathematical analysis on charge partitioning factor was made in this same Subsection. After this description, the good fitting of simulations obtained by classical HICUM 1-T model was shown for static and small-signal operations. On the other hand, the simulations obtained by 1-T model shows deviations with respect the DEVICE ones for large-signal applications. This mismatch was displayed in different situation (turn on and turn off processes) and for different bias points. This mismatch is due to the inherent structure of the 1-T. Indeed, unlike of the other cases, a closed solution of differential equation (40) without knowing anything about input signal is not possible for large-signal operation.

In this thesis the use of the charge partitioning factor to compensate the time shift was proposed.

First of all, the charge partitioning factor was defined as the ratio between the time shift Δt from 1-T model and 10-T model simulations and the time constant. Because the charge partitioning factor results time-dependent, this factor was obtained in one instant time. This instant time was chosen being the instant time of 50% of maximum collector current swing. It is important to underline that the used simulations to obtain the time shift Δt were performed with vertical NQS effects turned off.

The turn-on process shows a better result than the classical HICUM/L2 1-T model and, the most important thing, a perfect overlap at 50% of maximum collector current swing. On the other hand, this does not happen for turn-off process. Indeed, looking **Fig. 40** and **Fig. 41**, in turn-off process the simulations obtained by classical HICUM/L2 1-T model overlap those obtained by 10-T model rightly at 50% of maximum collector current swing. The overlap in this point causes a time shift Δt equal almost to zero and, therefore, a charge partitioning factor equal almost to zero. On the other hand, varying the charge partitioning factor value, the HICUM/L2 1-T model with partitioning factor overlap on 10-T model in other points.

The future steps should be a description of charge partitioning factor as a function of input variables, so to allow its implementation in practical applications. If the description of charged partitioning factor proposed in (43) is considered valid, the time constant τ_{rB} is already descripted as a function of input variables by (50). So the problem is reduced to describe the time shift Δt as a function of input variables.

Another possibility is to develop a charge partitioning factor dependent from (33). But this equation was developed for small-signal operations and, therefore, its proper functioning for large-signal operations is not guaranteed as well.

Appendix A

Input data for DEVICE simulation

```
&SETTINGS  lang_vers='1.90'  num_dig=12  max_exp=300  tcpu_lim=1e6
tcpu_job=10000 /
TRAC 0

STRUcture
 &GEN_INFO spat_dim=2 stru_file=' ' /
 &REGION_DEF  reg_mat='SEMI'  mod_name='SILI'  low_xyz=0.0       0.0
upp_xyz=0.5   0.2 /
 &REGION_DEF  reg_mat='CONT'  mod_name='CON0'  low_xyz=0.0       0.0
upp_xyz=0.0   0.2  cont_name='E ' /   * Emitter contact

 &REGION_DEF  reg_mat='FOXI'  mod_name='FOXI'  low_xyz=0.0       0.0
upp_xyz=0.0785 0.0 /                * BE field oxid
 &REGION_DEF  reg_mat='SUPP'  mod_name='SUPO'  low_xyz=0.0785  0.0
upp_xyz=0.0815 0.0  cont_name='B ' /  * Base contact
 &REGION_DEF  reg_mat='FOXI'  mod_name='FOXI'  low_xyz=0.0815  0.0
upp_xyz=0.5   0.0 /               * BC field oxid

 &REGION_DEF  reg_mat='CONT'  mod_name='CON0'  low_xyz=0.5       0.0
upp_xyz=0.5   0.2  cont_name='C ' /   * Collector contact

 &REGION_DEF  reg_mat='SYMM'  mod_name='SYMM'  low_xyz=0.0       0.2
upp_xyz=0.5   0.2 /               * Symmetry line
.STR

DISC
 &MAN_GRID disc_dir='x' shift_loc=0 loc_pnts=
 0.15  100
 0.2   20
 0.5   40 /
```

```
 &MAN_GRID disc_dir='y' shift_loc=0 loc_pnts=
 0.2  20 /
.DIS

MODEls
 &CONTACT mod_name='CON0' v_con=0.0   zeta_vcon=0.5 /
 &SUPPLY  mod_name='SUPO' cont_dist=0.0 cont_curr=0.0 /
 &SEMICON mod_name='SILI'
  mobn_0=70       mobn_max=1400       mobn_dop=0.95E17       mobn_beta=0.7
mobn_alph=-2.5
  mobn_bett=0.35    mobn_betf=1.1092    mobn_hd=43.0    mobn_doph=2.43E20
mobn_beth=2.5
  mobn_rmin=3.1 user_mobn=1
  mobp_0=44      mobp_max=450          mobp_dop=2.4E17      mobp_beta=0.78
mobp_alph=-2.5
  mobp_bett=0.35     mobp_betf=1.213     mobp_hd=19.0     mobp_doph=5.1E20
mobp_beth=2.5
  mobp_rmin=2.3 user_mobp=1
  elaf_0=4.05      bgap_vg0=1.1242      bgap_vhd0=9e-3      bgap_alhd=1.48e-3
bgap_chd=0.5 bgap_dophd=1.0e17 bgap_gamhd=0.5
  vsn_0=1.07E7 vsn_al=0.0E-3 vsp_0=0.837E7 vsp_al=0.0E-3
  rmn_eff=1.043 rmp_eff=1.073 dens_stat=2.540933e19 /

 &MAT_COMP mat_type='GE' bulk_mat='SILI'
  bgap_a1=-1.01  bgap_a2=0.835  mefn_c=0.46 mefp_c=0.04
  elaf_a1=-0.15 elaf_a2=-0.02  epsr_a1=3.13344 epsr_a2=1.1665
  mobn_0a1=-20.0 mobn_0a2=-80.0   mobn_mxa1=-1879.0  mobn_mxa2=-400.0
  vsn_0a1=-3.5E7 vsn_0a2=6.8E7
  mobp_0a1=-20.0 mobp_0a2=300.0   mobp_mxa1=-780.0   mobp_mxa2=4200.0
  vsp_0a1=0.0  vsp_0a2=0.0
  mobn_latt=-1.0 mobn_zetal=0.8 mobp_latt=-1.0 mobp_zetal=0.8 /
.MOD

PROFile
 *        emitter: analytical profile
 &CONST_DOP d_con=-2.27e20 xyz_low=-0.1 -0.1 xyz_upp=0.0125 1.0 /
 &EXP_PROD d_max=-2.27e20 xyz_max=0.0125 0  a_xyz=0.0225 0
   beta_xyz=3 0  xyz_low=0.012501 -0.001 xyz_upp=1.0 1.0 /

 *        internal base profile (rSBi0= kOhm)
 &EXP_PROD d_max=6.0e+018 xyz_max=0.08 0  a_xyz=0.02168 0
   beta_xyz=3.5 0  xyz_low=-0.1 -0.1 xyz_upp=1.0 1.0 /
```

```
 *      collector: epi
 &CONST_DOP d_con=-3.0E17 xyz_low=-0.1 -0.1 xyz_upp=0.5 2.0 /
 &CONST_DOP d_con=-5.0E16 xyz_low=-0.1 -0.1 xyz_upp=0.5 2.0 /
 *       collector: buried layer
 &EXP_PROD d_max=-3e19 xyz_max=0.5 0.1  a_xyz=0.05 0.0
   beta_xyz=2.0 0  xyz_low=-0.1 -0.1 xyz_upp=0.5 1.0 /

 * material composition profiles
 &COMP_TRAP mat_type='GE' c_max=0.02 xyz_dlow=0.002 0 xyz_dupp=0.0 0
   xyz_low=0.033 -0.01 xyz_upp=0.125 1.0 xyz_rlow=0.5 0   xyz_rupp=0.5 0 /
 &COMP_TRAP      mat_type='GE'      c_max=0.18      xyz_dlow=0.042      0
xyz_dupp=0.008 0
   xyz_low=0.036 -0.01 xyz_upp=0.125 1.0 xyz_rlow=0.3 0   xyz_rupp=0.5 0 /
.PRO

ANALYZE

*    start of analysis block
* ======================================

SOLUtion
  &SEMICON iter_max=1000 rtol_pot=1.0E-5 atol_pot=1.0E-5 rsum_cur=0.0
rho_pn=-100 /
  &SOLVE equa_name='poisson' solu_sequ=1 solu_meth='LUFA'
        iter_solv=300 dpot_lim=0.03 damp_newt=1
        iter_max=500/ orde_meth=''
  &SOLVE equa_name='cont_hole' solu_sequ=1 iter_max=500 dpot_lim=0.05
        damp_newt=1.0
        solu_meth='LUFA'       orde_meth=0       iter_solv=300       relx_fac=1.0
rtol_var=0.01 /
  &SOLVE equa_name='cont_elec' solu_sequ=1 iter_max=500 dpot_lim=0.05
        damp_newt=1.0
        solu_meth='LUFA'       orde_meth=0       iter_solv=300       relx_fac=1.0
rtol_var=0.01 /
.SOL
```

Appendix B

HICUM parameters extraction and model cards

B.1 HICUM parameters extraction

The consider transistor in Device is an ideal 2D transistor. For this reason, the perimetric parameters can be neglected and only the internal parameters can be considered.

After this assumption, the procedure to obtain the parameters was the following:

- Y-matrix were obtained for different bias points and for low frequency (1% of f_T) from DEVICE simulation;
- the forward Gummel plot and the reverse Gummel plot were obtained from DEVICE simulation;
- the output plots were obtained for different bias points from DEVICE simulation.

From Y-matrix the internal junction capacitances C_{jEi} and C_{jCi} were estimated. In particular:

$$C_{jEi} = \frac{I(Y_{11} + Y_{12})}{\omega} \tag{51}$$

$$C_{jCi} = \frac{I(-Y_{12})}{\omega} \tag{52}$$

The internal base-emitter junction capacitance C_{jEi} was obtained as function of V_{BE} for $V_{BC}=0$, while and the internal base-collector junction capacitance C_{jCi} was obtained as function of V_{BC} for $V_{BE}=0$. Fig. **18** and Fig**. 25** show their plots.

The parameters *cjei0*, *vdei*, *ajei* and *zei* were obtained from C_{jEi} plot, while the parameters *cjci0*, *vdci*, *vptci* and *zci* were obtained from C_{jCi} plot.

Even from Y-matrix the transition frequency f_T was estimated. In particular:

$$f_T = \frac{f}{I\left({}^{Y_{11}}/_{Y_{21}}\right)} \tag{53}$$

The transition frequency f_T was obtained as function of transit current I_C, for different V_{BC} values. Fig. **19** and Fig**. 26** show its plot.

The parameters *t0*, *tbvl* and *dt0h* were obtained from this plot for low IC values, while the parameters rci0, *vlim*, *vpt* and *vces* from this plot for high IC values. Also the parameter *tef0*, *gtfe*, *ahc*, *fthc*, *thcs*, *acbar*, *icbar*, *vcbar* and *tbfvs* were obtained from this plot.

From forward and reverse Gummel plots and from output plots were estimated the parameters *c10*, *qp0*, *mcf*, *hf0*, *hfc*, *hfe*, *hjci*, *hjei*, *ibeis*, *ibcis*, *mbei* and *mbci*.

After a first estimation, these parameters were adjusted using the optimize tool of ADS.

The other parameters were neglected to focus our analysis only to describe the interested effects.

Finally, the parameters of 10-T model were obtained with an opportune scaling of 1-T model ones.

B.2 HICUM parameters set model cards

B.2.1. 1-T model card

Name	*Value*	*Name*	*Value*
abet	*4.00000000e+01*	*cfbe*	*-1*
acbar	*6.03554000e-01*	*cjci0*	*3.73262577e-16*
af	*2.00000000e+00*	*cjcx0*	*0.00000000e+00*
afre	*2.00000000e+00*	*cjei0*	*9.33617403-16*
ahc	*1.20828000e-13*	*cjep0*	*0.00000000e+00*
ahjei	*2.61070138e+00*	*cjs0*	*0.00000000e+00*
aick	*1.00000000e-03*	*cscp0*	*0.00000000e+00*
ajei	*7.13599367e+00*	*csu*	*0.00000000e+00*
ajep	*2.50000000e+00*	*cth*	*0.00000000e+00*
alb	*0.00000000e+00*	*delck*	*2.00000000e+00*
alces	*0.00000000e+00*	*dt*	*0.00000000e+00*
aldck	*0.00000000e+00*	*dt0h*	*-1.28537000e-14*
alfav	*0.00000000e+00*	*dvgbe*	*0.00000000e+00*
alit	*6.50000000e-01*	*f1vg*	*-1.02377000e-04*
alqav	*0.00000000e+00*	*f2vg*	*4.32150000e-04*
alqf	*4.00000000e-01*	*favl*	*0.00000000e+00*
alrth	*0.00000000e+00*	*fbcpar*	*0.00000000e+00*
alt0	*0.00000000e+00*	*fbepar*	*1.00000000e+00*
alvs	*0.00000000e+00*	*fcrbi*	*0*
c10	*1.45910000e-32*	*fdqr0*	*0.00000000e+00*
cbcpar	*0.00000000e+00*	*fgeo*	*0.00000000e+00*
cbepar	*0.00000000e+00*	*flcomp*	*2.40000000e+00*

Name	*Value*	*Name*	*Value*
flcono	*0.00000000e+00*	*itss*	*0.00000000e+00*
flnqs	*1.00000000e+00*	*kavl*	*0.00000000e+00*
flsh	*0.00000000e+00*	*kf*	*0.00000000e+00*
fqi	*1.00000000e+00*	*kfre*	*0.00000000e+00*
fthc	*8.95492000e-01*	*kt0*	*0.00000000e+00*
ftit	*-1*	*latb*	*0.00000000e+00*
gtfe	*2.75283000e+00*	*latl*	*0.00000000e+00*
hcavl	*0.00000000e+00*	*mbci*	*1.04258245e+00*
hf0	*1.50239000e+00*	*mbcx*	*1.00000000e+00*
hfc	*5.53950000e-01*	*mbei*	*1.03003000e+00*
hfe	*1.53900000e+00*	*mbep*	*1.00000000e+00*
hjci	*3.32846000e-01*	*mcf*	*1.00327000e+00*
hjei0	*9.41569000e-01*	*mrei*	*2.00000000e+00*
hjei	*9.41569000e-01*	*mrep*	*2.00000000e+00*
hvdavl	*0.00000000e+00*	*msc*	*1.00000000e+00*
ibcis	*2.75289440e-20*	*msf*	*1.00000000e+00*
ibcxs	*0.00000000e+00*	*qavl*	*0.00000000e+00*
ibeis	*1.94474000e-20*	*qp0*	*3.54696000e-15*
ibeps	*0.00000000e+00*	*rbi0*	*3.96775395e+02*
ibets	*0.00000000e+00*	*rbx*	*0.00000000e+00*
icbar	*2.24726000e-04*	*rci0*	*4.03473000e+02*
ich	*0.00000000e+00*	*rcx*	*0.00000000e+00*
ireis	*0.00000000e+00*	*re*	*0.00000000e+00*
ireps	*0.00000000e+00*	*rhjei*	*3.00000000e+00*
iscs	*0.00000000e+00*	*rsu*	*0.00000000e+00*

Name	*Value*	*Name*	*Value*
rth	*0.00000000e+00*	*vlim*	*4.13256000e-01*
t0	*2.42824000e-12*	*vpt*	*6.31026000e+00*
tbhrec	*0.00000000e+00*	*vptci*	*5.55861498e+00*
tbvl	*2.13139000e-13*	*vptcx*	*1.00000000e+02*
tef0	*7.33135000e-12*	*vpts*	*1.00000000e+02*
thcs	*4.35239000e-09*	*vptsp*	*1.00000000e+02*
tnom	*2.68500000e+01*	*zci*	*4.91959999e-01*
tr	*0.00000000e+00*	*zcx*	*4.00000000e-01*
tsf	*0.00000000e+00*	*zei*	*2.99257873e-01*
tunode	*1.00000000e+00*	*zep*	*5.00000000e-01*
type	*1*	*zetabet*	*3.50000000e+00*
vcbar	*8.199000000e-01*	*zetaci*	*0.00000000e+00*
vces	*9.57874000e-03*	*zetact*	*3.00000000e+00*
vdci	*7.36814089e-01*	*zetahjei*	*1.00000000e+00*
vdck	*0.00000000e+00*	*zetarbi*	*0.00000000e+00*
vdcx	*7.00000000e-01*	*zetarbx*	*0.00000000e+00*
vdei	*8.29416465e-01*	*zetarcx*	*0.00000000e+00*
vdep	*9.00000000e-01*	*zetare*	*0.00000000e+00*
vds	*6.00000000e-01*	*zetacx*	*1.00000000e+00*
vdsp	*6.00000000e-01*	*zetarth*	*0.00000000e+00*
vgb	*1.17000000e+00*	*zetavgbe*	*1.00000000e+00*
vgc	*1.17000000e+00*	*zs*	*5.00000000e-01*
vge	*1.17000000e+00*	*zsp*	*5.00000000e-01*
vgs	*1.17000000e+00*		

B.2.2. 10-T model

Name	*Value*	*Name*	*Value*
abet	*4.00000000e+01*	*cjci0*	*3.73262577e-17*
acbar	*6.03554000e-01*	*cjcx0*	*0.00000000e+00*
af	*2.00000000e+00*	*cjei0*	*9.33617403-17*
afre	*2.00000000e+00*	*cjep0*	*0.00000000e+00*
ahc	*1.20828000e-13*	*cjs0*	*0.00000000e+00*
ahjei	*2.61070138e+00*	*cscp0*	*0.00000000e+00*
aick	*1.00000000e-03*	*csu*	*0.00000000e+00*
ajei	*7.13599367e+00*	*cth*	*0.00000000e+00*
ajep	*2.50000000e+00*	*delck*	*2.00000000e+00*
alb	*0.00000000e+00*	*dt*	*0.00000000e+00*
alces	*0.00000000e+00*	*dt0h*	*-1.28537000e-14*
aldck	*0.00000000e+00*	*dvgbe*	*0.00000000e+00*
alfav	*0.00000000e+00*	*f1vg*	*-1.02377000e-04*
alit	*6.50000000e-01*	*f2vg*	*4.32150000e-04*
alqav	*0.00000000e+00*	*favl*	*0.00000000e+00*
alqf	*4.00000000e-01*	*fbcpar*	*0.00000000e+00*
alrth	*0.00000000e+00*	*fbepar*	*1.00000000e+00*
alt0	*0.00000000e+00*	*fcrbi*	*0*
alvs	*0.00000000e+00*	*fdqr0*	*0.00000000e+00*
c10	*1.45910000e-34*	*fgeo*	*0.00000000e+00*
cbcpar	*0.00000000e+00*	*flcomp*	*2.40000000e+00*
cbepar	*0.00000000e+00*	*flcono*	*0.00000000e+00*
cfbe	*-1*	*flnqs*	*1.00000000e+00*

Name	*Value*	*Name*	*Value*
flsh	*0.00000000e+00*	*kf*	*0.00000000e+00*
fqi	*1.00000000e+00*	*kfre*	*0.00000000e+00*
fthc	*8.95492000e-01*	*kt0*	*0.00000000e+00*
ftit	*-1*	*latb*	*0.00000000e+00*
gtfe	*2.75283000e+00*	*latl*	*0.00000000e+00*
hcavl	*0.00000000e+00*	*mbci*	*1.04258245e+00*
hf0	*1.50239000e+00*	*mbcx*	*1.00000000e+00*
hfc	*5.53950000e-01*	*mbei*	*1.03003000e+00*
hfe	*1.53900000e+00*	*mbep*	*1.00000000e+00*
hjci	*3.32846000e-01*	*mcf*	*1.00327000e+00*
hjei0	*9.41569000e-01*	*mrei*	*2.00000000e+00*
hjei	*9.41569000e-01*	*mrep*	*2.00000000e+00*
hvdavl	*0.00000000e+00*	*msc*	*1.00000000e+00*
ibcis	*2.75289440e-21*	*msf*	*1.00000000e+00*
ibcxs	*0.00000000e+00*	*qavl*	*0.00000000e+00*
ibeis	*1.94474000e-21*	*qp0*	*3.54696000e-16*
ibeps	*0.00000000e+00*	*rbi0*	*1.02764827e+02*
ibets	*0.00000000e+00*	*rbx*	*0.00000000e+00*
icbar	*2.24726000e-05*	*rci0*	*4.03473000e+03*
ich	*0.00000000e+00*	*rcx*	*0.00000000e+00*
ireis	*0.00000000e+00*	*re*	*0.00000000e+00*
ireps	*0.00000000e+00*	*rhjei*	*3.00000000e+00*
iscs	*0.00000000e+00*	*rsu*	*0.00000000e+00*
itss	*0.00000000e+00*	*rth*	*0.00000000e+00*
kavl	*0.00000000e+00*	*t0*	*2.42824000e-12*

Name	*Value*	*Name*	*Value*
tbhrec	*0.00000000e+00*	*vpt*	*6.31026000e+00*
tbvl	*2.13139000e-13*	*vptci*	*5.55861498e+00*
tef0	*7.33135000e-12*	*vptcx*	*1.00000000e+02*
thcs	*4.35239000e-09*	*vpts*	*1.00000000e+02*
tnom	*2.68500000e+01*	*vptsp*	*1.00000000e+02*
tr	*0.00000000e+00*	*zci*	*4.91959999e-01*
tsf	*0.00000000e+00*	*zcx*	*4.00000000e-01*
tunode	*1.00000000e+00*	*zei*	*2.99257873e-01*
type	*1*	*zep*	*5.00000000e-01*
vcbar	*8.199000000e-01*	*zetabet*	*3.50000000e+00*
vces	*9.57874000e-03*	*zetaci*	*0.00000000e+00*
vdci	*7.36814089e-01*	*zetacx*	*1.00000000e+00*
vdck	*0.00000000e+00*	*zetact*	*3.00000000e+00*
vdcx	*7.00000000e-01*	*zetahjei*	*1.00000000e+00*
vdei	*8.29416465e-01*	*zetarbi*	*0.00000000e+00*
vdep	*9.00000000e-01*	*zetarbx*	*0.00000000e+00*
vds	*6.00000000e-01*	*zetarcx*	*0.00000000e+00*
vdsp	*6.00000000e-01*	*zetare*	*0.00000000e+00*
vgb	*1.17000000e+00*	*zetarth*	*0.00000000e+00*
vgc	*1.17000000e+00*	*zetavgbe*	*1.00000000e+00*
vge	*1.17000000e+00*	*zs*	*5.00000000e-01*
vgs	*1.17000000e+00*	*zsp*	*5.00000000e-01*
vlim	*4.13256000e-01*		

Appendix C

Data for time shift Δt, time constant τ_{rB} and lateral partitioning factor α

C.1 Turn on process

V_{CE}	V_{BE}	V_{max}	*Freq*	$\Delta t_{50\%}$	$\tau_{rB,50\%}$	α
1V	*670mV*	*200mV*	*50GHz*	*1.09ps*	*7.96ps*	*0.137*
1V	*670mV*	*175mV*	*50GHz*	*510fs*	*4.71ps*	*0.108*
1V	*670mV*	*150mV*	*50GHz*	*210fs*	*2.77ps*	*0.076*
1V	*670mV*	*125mV*	*50GHz*	*80.0fs*	*1.74ps*	*0.046*
1V	*670mV*	*100mV*	*50GHz*	*20.0fs*	*1.23ps*	*0.016*
1V	*670mV*	*75mV*	*50GHz*	*0.00s*	*961fs*	*0.000*
1V	*670mV*	*50mV*	*50GHz*	*0.00s*	*814fs*	*0.000*
1V	*670mV*	*25mV*	*50GHz*	*0.00s*	*731fs*	*0.000*
1V	*670mV*	*10mV*	*50GHz*	*0.00s*	*699fs*	*0.000*
1V	*670mV*	*5mV*	*50GHz*	*0.00s*	*690fs*	*0.000*
2V	*670mV*	*200mV*	*50GHz*	*1.14ps*	*8.03ps*	*0.142*
2V	*670mV*	*175mV*	*50GHz*	*540fs*	*4.74ps*	*0.114*

2V	*670mV*	*150mV*	*50GHz*	*230fs*	*2.77ps*	*0.083*
2V	*670mV*	*125mV*	*50GHz*	*90.0fs*	*1.73ps*	*0.052*
2V	*670mV*	*100mV*	*50GHz*	*30.0fs*	*1.21ps*	*0.023*
2V	*670mV*	*75mV*	*50GHz*	*0.00s*	*951fs*	*0.000*
2V	*670mV*	*50mV*	*50GHz*	*0.00s*	*812fs*	*0.000*
2V	*670mV*	*25mV*	*50GHz*	*0.00s*	*731fs*	*0.000*
2V	*670mV*	*10mV*	*50GHz*	*0.00s*	*700fs*	*0.000*
2V	*670mV*	*5mV*	*50GHz*	*0.00s*	*691fs*	*0.000*
1V	*770mV*	*100mV*	*50GHz*	*1.07ps*	*8.17ps*	*0.131*
1V	*770mV*	*75mV*	*50GHz*	*520fs*	*4.94ps*	*0.105*
1V	*770mV*	*50mV*	*50GHz*	*230fs*	*3.02ps*	*0.076*
1V	*770mV*	*25mV*	*50GHz*	*100fs*	*2.00ps*	*0.050*
1V	*770mV*	*10mV*	*50GHz*	*70.0fs*	*1.64ps*	*0.042*
1V	*770mV*	*5mV*	*50GHz*	*60.0fs*	*1.55ps*	*0.039*
2V	*770mV*	*100mV*	*50Hz*	*1.13ps*	*8.25ps*	*0.137*
2V	*770mV*	*75mV*	*50GHz*	*560fs*	*4.97ps*	*0.113*
2V	*770mV*	*50mV*	*50GHz*	*250fs*	*3.04ps*	*0.082*
2V	*770mV*	*25mV*	*50GHz*	*110fs*	*2.00ps*	*0.055*
2V	*770mV*	*10mV*	*50GHz*	*80.01fs*	*1.65ps*	*0.048*
2V	*770mV*	*5mV*	*50GHz*	*70.01fs*	*1.56ps*	*0.045*

Table 1. *Values of time shift Δt, time constant τ_{rB} and lateral partitioning factor α for different bias and input signals in turn-on process at 50% of maximum current swing*

C.2 Turn off process

V_{CE}	V_{BE}	V_{max}	*Freq*	$\Delta t_{50\%}$	$\tau_{rB,50\%}$	α
1V	*670mV*	*200mV*	*50GHz*	*70.0fs*	*7.79ps*	*0.009*
1V	*670mV*	*175mV*	*50GHz*	*90.0fs*	*7.84ps*	*0.011*
1V	*670mV*	*150mV*	*50GHz*	*110fs*	*7.85ps*	*0.014*
1V	*670mV*	*125mV*	*50GHz*	*120fs*	*7.93ps*	*0.015*
1V	*670mV*	*100mV*	*50GHz*	*160fs*	*8.06ps*	*0.020*
1V	*670mV*	*75mV*	*50GHz*	*200fs*	*8.42ps*	*0.024*
1V	*670mV*	*50mV*	*50GHz*	*290fs*	*9.21ps*	*0.031*
1V	*670mV*	*25mV*	*50GHz*	*520fs*	*11.0ps*	*0.047*
1V	*670mV*	*10mV*	*50GHz*	*820fs*	*13.1ps*	*0.063*
1V	*670mV*	*5mV*	*50GHz*	*960fs*	*14.0ps*	*0.068*
2V	*670mV*	*200mV*	*50GHz*	*80.0fs*	*7.90ps*	*0.010*
2V	*670mV*	*175mV*	*50GHz*	*80.0fs*	*7.94ps*	*0.010*
2V	*670mV*	*150mV*	*50GHz*	*100fs*	*7.96ps*	*0.013*
2V	*670mV*	*125mV*	*50GHz*	*120fs*	*8.02ps*	*0.015*
2V	*670mV*	*100mV*	*50GHz*	*150fs*	*8.18ps*	*0.018*
2V	*670mV*	*75mV*	*50GHz*	*190fs*	*8.53ps*	*0.022*
2V	*670mV*	*50mV*	*50GHz*	*300fs*	*9.32ps*	*0.032*
2V	*670mV*	*25mV*	*50GHz*	*530fs*	*11.1ps*	*0.048*
2V	*670mV*	*10mV*	*50GHz*	*810fs*	*13.2ps*	*0.061*

2V	*670mV*	*5mV*	*50GHz*	*930fs*	*14.2ps*	*0.065*
1V	*770mV*	*100mV*	*50GHz*	*30.0fs*	*761fs*	*0.039*
1V	*770mV*	*75mV*	*50GHz*	*40.0fs*	*860fs*	*0.046*
1V	*770mV*	*50mV*	*50GHz*	*40.0fs*	*997fs*	*0.040*
1V	*770mV*	*25mV*	*50GHz*	*40.0fs*	*1.18ps*	*0.034*
1V	*770mV*	*10mV*	*50GHz*	*50.0fs*	*1.34ps*	*0.037*
1V	*770mV*	*5mV*	*50GHz*	*50.0fs*	*1.40ps*	*0.036*
2V	*770mV*	*100mV*	*50Hz*	*50.0fs*	*834fs*	*0.060*
2V	*770mV*	*75mV*	*50GHz*	*40.0fs*	*935fs*	*0.043*
2V	*770mV*	*50mV*	*50GHz*	*40.0fs*	*1.05ps*	*0.038*
2V	*770mV*	*25mV*	*50GHz*	*40.0fs*	*1.21ps*	*0.033*
2V	*770mV*	*10mV*	*50GHz*	*50.0fs*	*1.36ps*	*0.037*
2V	*770mV*	*5mV*	*50GHz*	*60.0fs*	*1.42ps*	*0.042*

Table 2. *Values of time shift Δt, time constant τ_{rB} and lateral partitioning factor α for different bias and input signals in turn-off process at 50% of maximum current swing*