UNIVERSITÀ DEGLI STUDI DI NAPOLI FEDERICO II

PH.D. THESIS
IN
INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

# NUMERICAL SIMULATIONS AND ANALYTICAL MODELING OF THE THERMAL AND ELECTROTHERMAL BEHAVIOR OF ELECTRONIC COMPONENTS AND PACKAGES

ANTONIO PIO CATALANO

TUTOR: PROF. VINCENZO D'ALESSANDRO

XXXII CICLO

SCUOLA POLITECNICA E DELLE SCIENZE DI BASE
DIPARTIMENTO DI INGEGNERIA ELETTRICA E TECNOLOGIE DELL'INFORMAZIONE

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# List of abbreviations

| | |
|---|---|
| **1-D** | One-dimensional |
| **2-D** | Two-dimensional |
| **3-D** | Three-dimensional |
| **AlN** | Aluminum nitride |
| **BC** | Boundary condition |
| **CB** | Common-base |
| **CE** | Common-emitter |
| **CS** | Cooling surface |
| **Cu** | Copper |
| **DBC** | Direct bonded copper |
| **DCTM** | Dynamic compact thermal model |
| **DOE** | Design of experiments |
| **DoF** | Degree of Freedom |
| **DSC** | Double-sided cooled |
| **DUT** | Device under test |
| **EFV** | Elementary fin volume |
| **ET** | Electrothermal |
| **FC** | Flip-chip |
| **FEM** | Finite-element method |
| **GaAs** | Gallium arsenide |
| **GaN** | Gallium nitride |
| **GDS** | Graphic data system |

| | |
|---|---|
| **GSG** | Ground-signal-ground |
| **HBT** | Heterojunction bipolar transistor |
| **HEMT** | High-electron mobility transistor |
| **HI** | High-injection |
| **HS** | High-side |
| **HSK** | Heat-sink |
| **II** | Impact-ionization |
| **KIV** | Key input variable |
| **$L_E$** | Emitter length |
| **LS** | Low-side |
| **M1** | Metal 1 (also denoted as FIC) |
| **M2** | Metal 2 (also denoted as TM) |
| **MH** | Mutual-heating |
| **MPMM** | Multi-point moment matching |
| **NDR** | Negative differential resistance |
| **NTC** | Negative temperature coefficient |
| **PA** | Power amplifier |
| **PCB** | Printed circuit board |
| **$P_D$** | Dissipated power |
| **PM** | Power module |
| **RF** | Radiofrequency |
| **$R_{TH}$** | Thermal resistance |
| **$R_{THj-a}$** | Junction-to-ambient thermal resistance |
| **SH** | Self-heating |
| **$Si_3N_4$** | Silicon nitride |
| **SiC** | Silicon carbide |
| **SMD** | Surface mount device |
| **SOA** | Safe operating area |

| | |
|---|---|
| **SSC** | Single-sided cooled |
| **$T_0$=300K** | Reference temperature |
| **TIM** | Thermal interface material |
| **TFB** | thermal feedback block |
| **TM** | Top metal |
| **TP** | Thermal plate |
| **TRP** | Trend reversal point |
| **TVs** | Thermal vias |
| **WB** | Wire-bonding |
| **$W_E$** | Emitter width |
| **$Z_{TH}$** | Thermal impedance |

# Introduction

## 1.1 Motivations

Thermal issues are becoming increasingly relevant in any field of electronics. The restless scaling process [All02], the use of new materials (often suffering from poor thermal conductivity) to improve the electrical performances [Yod96], [Kon98], and the increase in switching frequencies [Bal89] represent just a few targets of companies and research centers involved in the area of electronic devices, circuits, and systems. Unfortunately, any progress obtained in these directions unavoidably leads to a new challenge in the management of Joule heating effects, which is currently a critical bottleneck to the performance and reliability of emerging technologies [Gar02]; such effects are here summarized in order of increasing impact: ironically, (i) the electrical performances turn out to be reduced [Ame93]; (ii) long-term reliability strongly decreases resulting in premature aging effects [Yan11]; in some severe and unlucky cases, (iii) irreversible failures of the system can be observed [Cia02].

In the modern scenario, the care given to the thermal management is constantly growing; a thermal-oriented design represents the only way to effectively and efficiently face the previously mentioned issues [Rem00]. Since the experimental thermal design was (and still is) considered expensive in terms of both money and time, thermal simulations are currently gaining attention as they offer several advantages; first, simulations make it possible to achieve a reliable prediction of the actual behavior of the electronic systems of interest; it is also possible to investigate the main mechanisms underlying the thermal problem in such systems [Tha15], which opens the way to smart solutions suited to mitigate its detrimental impact; last but not least, thermal simulations allows building compact thermal models to

perform electrothermal (ET) simulations [Amm99], which are devoted to evaluate the actual behavior of the devices and circuits under analysis.

## 1.2 Research topics

The study of state-of-the-art devices for radiofrequency (RF) applications and power circuits based on modern wide-band-gap (WBG) transistors is included in this thesis. Both categories are strongly affected by thermal effects, which represent topics of interest for the R&D community. In the following, an overview of the main research topics is given.

### 1.2.1 Devices for RF applications

Gallium Arsenide (GaAs) heterojunction bipolar transistors (HBTs) are the preferred technology for handset power amplifiers (PAs) in various wireless communication systems thanks to appealing features like high power density, cut-off frequency, efficiency, and linearity [Fre11]. However, GaAs HBTs are plagued by harmful thermal and ET effects induced by poor GaAs thermal conductivity (one third of that of silicon), mesa isolation (inhibiting the lateral heat flow), and high operating currents. ET effects are deleterious from multiple perspectives, since they shrink the DC safe operating area (SOA) at medium/high currents and degrade the RF performances. Pervasive examples are the *collapse of current gain* affecting multi-emitter GaAs HBTs, which can be SOA-limiting or even destructive [Bay93], [Sei93], [Liu93a], [Lio94], [Liu94], [Dho98a], as well as the discrepancy between dynamic and static error vector magnitude [Yoo07], thermal memory effects [Oza14], and reliability/ruggedness issues [Zam13a] in GaAs HBT PAs.

Since the late eighties a plethora of papers have been published, which deal with the thermal or ET behavior of single- and multi-emitter transistors as well as of circuits in GaAs technology. This thesis investigates several aspects and facets rarely or marginally covered in the literature, which are summarized in the following.

- **Role of semiconductor and metal layers**: Many studies focused on the metallization due to the important role played by

the upward heat flow in this technology [Gui94] (the low thermal conductivity of the GaAs substrate mitigates the downward flow to the backside). Most of them have proposed and/or investigated solutions based on thermal shunts ([Lio93], [Lio95], [Jen96], [Boz97], [Dho98b], [Yea99], [Wal03], [Kur03], [Cis11]). Other works dealing with multi-emitter transistors have promoted emitter or base ballasting [Liu96], [Dho98b], [Met13] and nonuniform finger spacing or length for assigned die and emitter areas [Lee01], [Met13]. Unfortunately, almost all the thermal analyses presented in the above papers are (sometimes unacceptably) inaccurate: the real – and complex – device structures are always represented with simplified (or even oversimplified) domains to allow (i) the development of analytical models for the temperature distribution or (ii) an easy construction/meshing of the 3-D geometry for numerical simulations; still now, in spite of the continuous improvement in PC performances, task (ii) is far from trivial if performed manually, especially when all technological details must be taken into account. Besides the metallization, the often overlooked role played by the emitter stack (previously investigated only in [Anh98]) deserves to be analyzed in state-of-the-art InGaP/GaAs because of the low thermal conductivities of the ternary InGaAs and InGaP emitter layers (even lower than GaAs), which make thermal shunt solutions less effective. A comprehensive and accurate study of the impact of semiconductor and metal layer in HBTs manufactured in this technology is still lacking in literature.

- **Comparison between packaging technology**: Some papers have also investigated the beneficial effect of a more thermally conductive and/or shorter path from the heat dissipation region and the sink, which can be obtained with flip-chip (FC) packaging [Sat93], [Aid93], [Bay96], [Jen96], [Anh98] or alternative solutions based on thermal vias [Hil95], [Cis11]. Since designs are moving to FC, the thermal impact of the emitter is expected to be amplified because of the heat propagation through it to the sink. In addition, no studies have been published that report an exhaustive thermal comparison between the conventional wire-bonding (WB) technology – still

largely adopted due to its flexibility, existing infrastructure, and low cost – and the FC assembly, which benefits from a smaller package size and aims to boost the performance.

- **Effects of dynamic thermal coupling in PA circuits**: Recently, the impact of thermal coupling on the PA behavior has attracted growing interest. In [Yam17], an experimental study performed on GaAs HBT PAs demonstrated that a tight thermal coupling between the transistor power stages and their bias circuits may cause a turn-on delay of the quiescent collector current, thus delaying the output power turn-on. An interesting analysis based on dynamic ET simulations is proposed in [Oza14], where light is shed on the influence of mutual-heating between the RF and bias transistors of a bipolar PA designed for WLAN. It is found that, if the devices are closer, the increased coupling (i) causes lower RF gain and undesired soft compression characteristics, but, on the other hand, (ii) minimizes thermal memory effects. No studies have been published that provide an exhaustive overview of the thermal coupling as a function of the circuit topology (i.e., the distance between devices) and the fabrication process.
- **Steady-state electrothermal behavior**: Designing robust circuits with GaAs devices requires special care because of the harmful ET effects previously mentioned. Thermal-aware design methodologies relying on suitable ET simulation tools are highly desired to alleviate performance and reliability degradation. Unfortunately, the choice of the simulation approach is challenging. Full 3-D ET simulations based on the finite-element method (FEM), e.g., with Atlas from Silvaco or Sentaurus from Synopsys, are computationally onerous or even unviable when dealing with complex structures like practical transistor arrays. In this thesis, this issue is tackled by resorting to an approach based on compact ET models; an in-depth overview of the main effects affecting the studied GaAs-based technology is then given.

### 1.2.2 Power devices and circuits

WBG devices represent the challenge of the modern technologies to increase the performances of circuits for power

applications. Silicon carbide (SiC) MOSFETs and gallium nitride (GaN) high-electron mobility transistors (HEMTs) are the most common devices based on WBG materials. The SiC-based devices are usually adopted in power modules (PM), while the circuits containing HEMTs are commonly realized on printed circuit board (PCB). The high values of power ($P_D$) dissipated by the devices lead to the need of conceiving and developing cooling solutions in both technologies. In this scenario, the thesis is aimed to the study of the following research topics:

- **Single-sided and double-sided cooled technologies for power modules**: Advanced thermal design of PMs is becoming increasingly important for the development of power systems with enhanced performance and reliability. Thermal issues are even more relevant in PMs based on WBG semiconductor devices which feature much higher heat-generation rates than their silicon counterparts. Designers efforts typically aim at effectively extracting heat from the active regions. Recently, double-sided cooled (DSC) PMs have gained interest over single-sided cooled (SSC) ones. DSC PMs include two direct bonded copper (DBC) substrates assembled in a sandwich-like configuration, with the power devices and their interconnections embedded in between them [Sal15]. Although not yet widespread at commercial level, the DSC technology offers many advantages: as demonstrated at voltage levels up to 1.2 kV [Las16], the replacement of WB with solid interconnect posts (also denoted as bumps) can help reduce the operating temperature and parasitic inductance, thereby (i) increasing the electrical performance, (ii) alleviating the ET stress, and (iii) improving long-term reliability. When moving to higher voltage classes (e.g., 3.3 kV), the distances and separation between parts have to be kept larger in order to ensure dielectric integrity. This can easily result in thermal performance degradation if the design is not thoroughly optimized. A fair comparison between SSC and DSC structures in terms of thermal performances deserves to be investigated; in particular, the role of the boundary conditions (BCs) applied on the cooling surfaces (CSs) of such modules has received limited attention in the literature.

- **Parameter fluctuations of multichip SiC power modules:** SiC MOSFETs are inexorably replacing the traditional Si counterparts in several fields. However, long-term reliability is a major factor that still needs improvement for such devices. This is particularly true for conversion systems exploiting parallel SiC transistors, usually adopted either as discrete components or within the same PM to overcome the poor current capability of commercially available single-die devices, which is limited to few hundred amps [Fab15]. In this case, technological fluctuations in device parameters and assembly-related ET and electromagnetic mismatches among chips can indeed result in unbalanced steady-state and dynamic performances [Wan14], [Ric18a], [Ric18b], [Ric18c]. Therefore, the implementation of configurations based on parallel SiC MOSFETs can be critical and needs to be optimized; at the same time, a thorough investigation of the ET behavior of such modules is required.
- **GaN-based printed circuit boards**: GaN technology represents an opportunity in power electronics to achieve very high switching frequency, thus enabling higher volumetric and gravimetric power density, strategic to the competitive development of many application domains (e.g., hybrid and electric transport). To that aim, high-frequency compatible surface mount device (SMD)-type packaging has recently established itself as the preferential option for GaN HEMTs. Since GaN-based circuits are still mainly realized using discrete components on PCB [Tra19], their thermal management can be critical because the difficulties in containing the number of interfaces between the devices (packaged in SMD case) and the cooling environment (i.e., ambient). The choice of cooling solutions for the circuits on PCB is usually supported by numerical simulations or experimental characterizations, both requiring time and technical skills [Ber09], [Ant18]; to alleviate the work of the thermal designers, simple analytical models to predict the impact of cooling solutions like thermal vias (TVs) and heat-sinks (HSKs) on the overall thermal behavior will be presented in this thesis.

## 1.3 Thesis outline

The thesis is organized as follows.

**Chapter 2** presents the technological details of devices, circuits, and systems, and gives insight into the main thermal issues jeopardizing them.

The methodologies exploited in this thesis are illustrated in **Chapter 3.** This Chapter focuses on (i) an *in-house* routine developed to support a commercial FEM software for performing extremely-accurate thermal simulations and (ii) a model-order reduction approach that automatically generates thermal feedback blocks (TFBs) suited to describe the power-temperature feedback for ET simulations. A detailed description of the procedure to evaluate the thermal resistance ($R_{TH}$) and the thermal impedance ($Z_{TH}$) – quantifying the steady-state and dynamic thermal behavior of the analyzed structure, respectively – is provided. The main findings of this work have been achieved by means of the *in-house* routine previously mentioned, which demonstrated to be generally suitable for thermal problems in *any* field of electronics, including photovoltaic panels/plants.

The subsequent chapters are aimed to show the purely-thermal achievements obtained for RF devices and the power systems. **Chapter 4** dwells on (i) the design of experiment (DOE) procedure to analyze the impact of the technological parameters of interest on the thermal behavior of GaAs HBTs; (ii) the impact of semiconductor and metal layers affecting the devices in different topologies and packaging styles; and (iii) the dynamic thermal coupling in RF circuits for WLAN PAs. **Chapter 5** presents results of devices for power applications; first, the thermal comparison of SSC and DSC technologies to realize PMs is shown; thermal models suitable to support the PCB thermal design are introduced and their accuracy is then examined.

**Chapter 6** describes the ET simulations of RF devices and SiC-based PMs. The Section focused on RF devices is organized as follows; first, the temperature-sensitive electrical modeling of HBTs is presented; then, the macromodeling technique to perform ET analyses in SPICE-like simulators is shown; finally, the simulation results concerning device test structures and HBT arrays are illustrated. The ET simulations performed on PMs are then presented; these are aimed

to quantify the effect of technology fluctuations on the ET behavior using the TFB built thanks to the MOR-based approach.

Conclusions are then drawn.

## 1.4 Publications list

- **A. P. Catalano**, A. Magnani, V. d'Alessandro, L. Codecasa, P. J. Zampardi, B. Moser, and N. Rinaldi, "Influence of layout and technology parameters on the thermal behavior of InGaP/GaAs HBTs," *Proc. IEEE 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 233–236, Jun. 2017.
- **A. P. Catalano** *et al.*, "Effect of heat sources modeling in DC circuit-level electrothermal simulation of power MOSFETs," *Proc. National Conference of Società Italiana di Elettronica (SIE)*, Jun. 2017.
- **A. P. Catalano**, A. Magnani, V. d'Alessandro, L. Codecasa, N. Rinaldi, B. Moser, and P. J. Zampardi, "Numerical analysis of the thermal behavior sensitivity to technology parameters and operating conditions in InGaP/GaAs HBTs," *Proc. IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct. 2017.
- **A. P. Catalano**, M. Riccio, L. Codecasa, A. Magnani, G. Romano, V. d'Alessandro, L. Maresca, N. Rinaldi, G. Breglio, and A. Irace, "Model-order reduction procedure for fast dynamic electrothermal simulation of power converters," *Lecture Notes in Electrical Engineering,* vol. 512, pp. 81–87, 2019.
- V. d'Alessandro, **A. P. Catalano**, A. Magnani, L. Codecasa, N. Rinaldi, B. Moser, and P. J. Zampardi, "Simulation comparison of InGaP/GaAs HBT thermal performance in wire-bonding and flip-chip technologies," *Microelectronics Reliability*, vol. 78, pp. 233–242, Nov. 2017.

- V. d'Alessandro, **A. P. Catalano**, L. Codecasa, B. Moser, and P. J. Zampardi, "Combined SPICE-FEM analysis of electrothermal effects in InGaP/GaAs HBT devices and arrays for handset applications," *Proc. IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2018.
- **A. P. Catalano** *et al.*, "Electrothermal analysis of GaAs-based HBT arrays for RF power amplifiers," *Proc. National Conference of Società Italiana di Elettronica (SIE)*, Jun. 2017.
- V. d'Alessandro, **A. P. Catalano**, L. Codecasa, B. Moser, and P. J. Zampardi, "Modeling thermal coupling in bipolar power amplifiers toward dynamic electrothermal simulations," *Proc. IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*, Aug. 2018.
- A. Borghese, **A. P. Catalano**, M. Riccio, L. Codecasa, A. Fayyaz, V. d'Alessandro, A. Castellazzi, L. Maresca, G. Breglio, and A. Irace, "An efficient simulation methodology to quantify the impact of parameter fluctuations on the electrothermal behavior of multichip SiC power modules," *Materials Science Forum*, vol. 963, pp. 855–858, 2019.
- V. d'Alessandro, **A. P. Catalano**, L. Codecasa, P. J. Zampardi, and B. Moser, "Accurate and efficient analysis of the upward heat flow in InGaP/GaAs HBTs through an automated FEM-based tool and Design of Experiments," *International Journal of Numerical Modeling – Electronic Networks, Devices and Fields*, vol. 32, no. 2, Mar./Apr. 2019.
- R. Trani, **A. P. Catalano**, A. Castellazzi, and V. d'Alessandro, "Thermal management solutions for a lightweight 3L GaN inverter," *Proc. ICPE - ECCE Asia*, 2019.

- **A. P. Catalano**, P. Guerriero, V. d'Alessandro, L. Codecasa, and S. Daliento, "An approach to the cell-level diagnosis of malfunctioning events in PV panels from aerial thermal maps," presented at *ELECTRIMACS*, 2019, and to be published in *Lecture Notes on Electrical Engineering*.
- **A. P. Catalano**, V. d'Alessandro, P. Guerriero, and S. Daliento, "Diagnosis of power losses in PV plants by means of UAV thermography," *Proc. IEEE International Conference on Clean Electrical Power*, pp. 306–310, Jul. 2019.
- L. Codecasa, **A. P. Catalano**, and V. d'Alessandro, "A-priori error bound for moment matching approximants of thermal models," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2019.
- **A. P. Catalano**, C. Scognamillo, A. Castellazzi, and V. d'Alessandro, "Optimum thermal design of high-voltage double-sided cooled multi-chip SiC power modules," *Proc. IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2019.
- **A. P. Catalano**, R. Trani, A. Castellazzi, and V. d'Alessandro, "Analytical modeling of through-PCB thermal vias and heat-sinks for integrated power electronics," *Proc. IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2019.
- P. Guerriero, **A. P. Catalano**, I. Matacena, L. Codecasa, V. d'Alessandro, and S. Daliento, "Experimental assessment of malfunction events in photovoltaic modules from IR thermal maps" *Proc. IEEE International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2019.
- **A. P. Catalano**, O. Olanrewaju, V. d'Alessandro, and A. Castellazzi, "Evaluation of vertical mechanical displacement in SiC-based power modules," *Proc. International Symposium on Advanced Power Packaging (ISAPP)*, Oct. 2019.

- C. Scognamillo, **A. P. Catalano**, R. Trani, V. d'Alessandro, and A. Castellazzi, "Influence of bumps height on electric field in double sided cooling power modules," *Proc. International Symposium on Advanced Power Packaging (ISAPP)*, Oct. 2019.
- R. Trani, **A. P. Catalano**, C. Scognamillo, V. d'Alessandro, and A. Castellazzi, "Optimum thermal management design for compact PCB-based high frequency GaN assemblies" *Proc. International Symposium on Advanced Power Packaging (ISAPP)*, Oct. 2019.
- **A. P. Catalano**, O. Olanrewaju, C. Scognamillo, V. d'Alessandro, and A. Castellazzi, "Stress-induced vertical deformations in state-of-the-art power modules: an improved electro-thermo-mechanical approach," *Proc. IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, Apr. 2020 (to be presented).
- **A. P. Catalano**, R. Trani, C. Scognamillo, V. d'Alessandro, and A. Castellazzi, "Optimization of thermal vias design in PCB-based power circuits," *Proc. IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, Apr. 2020 (to be presented).
- C. Scognamillo, **A. P. Catalano**, R. Trani, V. d'Alessandro, and A. Castellazzi, "3-D FEM investigation on electrical ruggedness of double-sided cooling power modules," *Proc. IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, Apr. 2020 (to be presented).

# Chapter 2

# Technologies under Test

The aim of this Chapter is to summarize the technology features of the device, circuits, and systems examined in the thesis. The description is conducted by underlining the critical points from the thermal and ET points of view.

Section 2.1 describes GaAs-based HBTs starting with the structure of the single-emitter device. The features of more complex configurations like multi-emitter devices, packaging technologies, HBT arrays, as well as WLAN circuits for PAs are then shown in detail.

In Section 2.2, the power systems are analyzed; in particular, technology details about (i) PMs realized with SiC MOSFETs and (ii) circuits on PCB in GaN technology are given.

## 2.1 GaAs-based HBTs

The RF devices under test (DUTs) are mesa-isolated NPN HBTs, manufactured by Qorvo for testing purposes on a GaAs substrate with an HBT-only process [Cat17a], [Cat17b]. Fig. 2.1 depicts two angled top views, which show that the RF DUTs are designed with a ground-signal-ground (GSG) pad configuration for experimental characterization through a probing station equipped with RF probes. For the single-emitter devices, a sketch of the cross section and a magnification of the intrinsic region are represented in Fig. 2.2. Two Au metallization layers, hereinafter denoted as M1 (metal 1) and M2 (metal 2), are available for the interconnections. Some thermal shunt effect is offered by a path composed by M1, M2, M1, and a thin insulating silicon nitride ($Si_3N_4$) layer, which allows the upward heat flow emerging from the emitter to be injected back into the GaAs substrate; PBO is adopted as a final passivation layer.

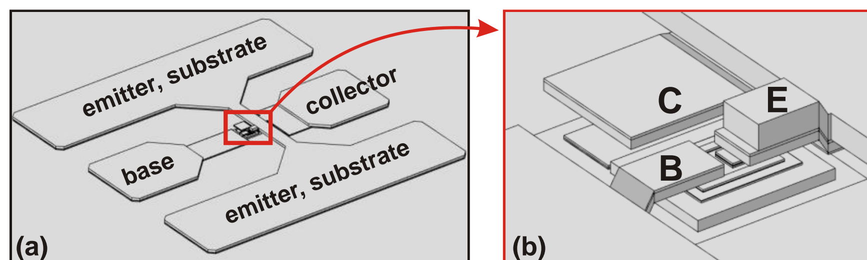



**Fig. 2.1** (a) Top view showing the GSG terminal configuration and (b) zoom of the intrinsic DUT highlighting the metals over emitter, base, and collector regions.

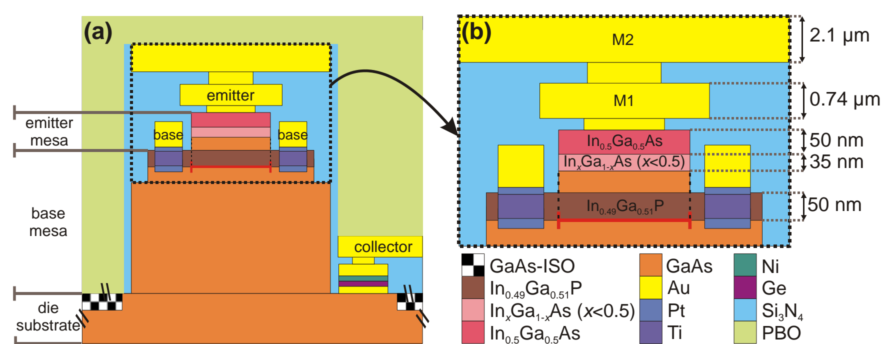



**Fig. 2.2** (a) Typical cross section of the single-emitter RF DUT; (b) magnification showing the semiconductor and metallization layers of interest, along with the reference values.

The emitter stack is composed by (from the top):

- an emitter cap with a highly-doped $In_{0.5}Ga_{0.5}As$ layer used to minimize the contact resistance with the Au metallization, and a grading $In_xGa_{1-x}As$ layer (with the Indium mole fraction $x$ decreasing from 0.5 to 0) to achieve a good lattice match with the underlying GaAs layer;
- the aforementioned GaAs layer as a set-back for easier processing;
- a deep $In_{0.49}Ga_{0.51}P$ layer in the base mesa at the metallurgical base-emitter junction (identified with a red line in Fig. 2.2); the InGaP alloy is widely used in modern devices in lieu of e.g., $Al_{0.25}Ga_{0.75}As$ to improve performance and reliability [Liu92], [Liu93b], [Tak94], [Low98], [Hsi00].

The base and collector are GaAs. Fig. 2.2a also shows the damaged GaAs-ISO region (used to ensure electrical insulation from

neighboring devices in complex circuits containing more than one transistor).

To apply the DOE strategy introduced in Section 4.1, a reference value (also indicated in Fig. 2.2b) and a practical (technologically-reasonable) variation range were chosen for each parameter, as summarized in Table 2.1. It is worth noting that the reference, the minimum, and the maximum values are indicated with 0, -1, and +1, respectively, consistently with the DOE nomenclature (see Section 4.1).

**TABLE 2.1** RANGES AND REFERENCE VALUES OF EMITTER AND METAL PARAMETERS USED FOR THE DOE ANALYSES (SECTION 4.1)

| | layer thickness | | | | |
|---|---|---|---|---|---|
| | $t_{In0.5Ga0.5As}$ | $t_{InxGa1\text{-}xAs}$ | $t_{In0.49Ga0.51P}$ | $t_{M1}$ | $t_{M2}$ |
| **reference (0)** | 50 nm | 35 nm | 50 nm | 0.74 µm | 2.1 µm |
| **minimum (-1)** | 30 nm | 25 nm | 30 nm | 0.74 µm | 2.1 µm |
| **maximum (+1)** | 70 nm | 60 nm | 50 nm | 1 µm | 3.5 µm |

## 2.1.1 Multi-emitter devices and packaging style

Multi-emitter devices are usually fabricated to increase the current capability. For the transistor analyzed in this thesis, a base mesa is shared by 4 emitter fingers, each with 2×20.5 µm$^2$ area (the total emitter area is then equal to 164 µm$^2$). The resulting domain defines an individual transistor, hereinafter also denoted as *unit cell*, which is schematically represented in Fig. 2.3a.

In the traditional WB technology (Fig. 2.3b), the HBTs enjoy two M1 and M2 layers, with M2 located over the emitter (top metal or TM style). The 380×300 µm$^2$ thinned (100-µm-thick) GaAs die is placed on an 830×830 µm$^2$ 270-µm-thick laminate, which comprises eight 600×600 µm$^2$ 12-µm-thick Cu plates connected by 3×3 circular Cu vias with 125 µm diameter, 200 µm pitch, and 25 µm vertical thickness, all embedded in a dielectric.

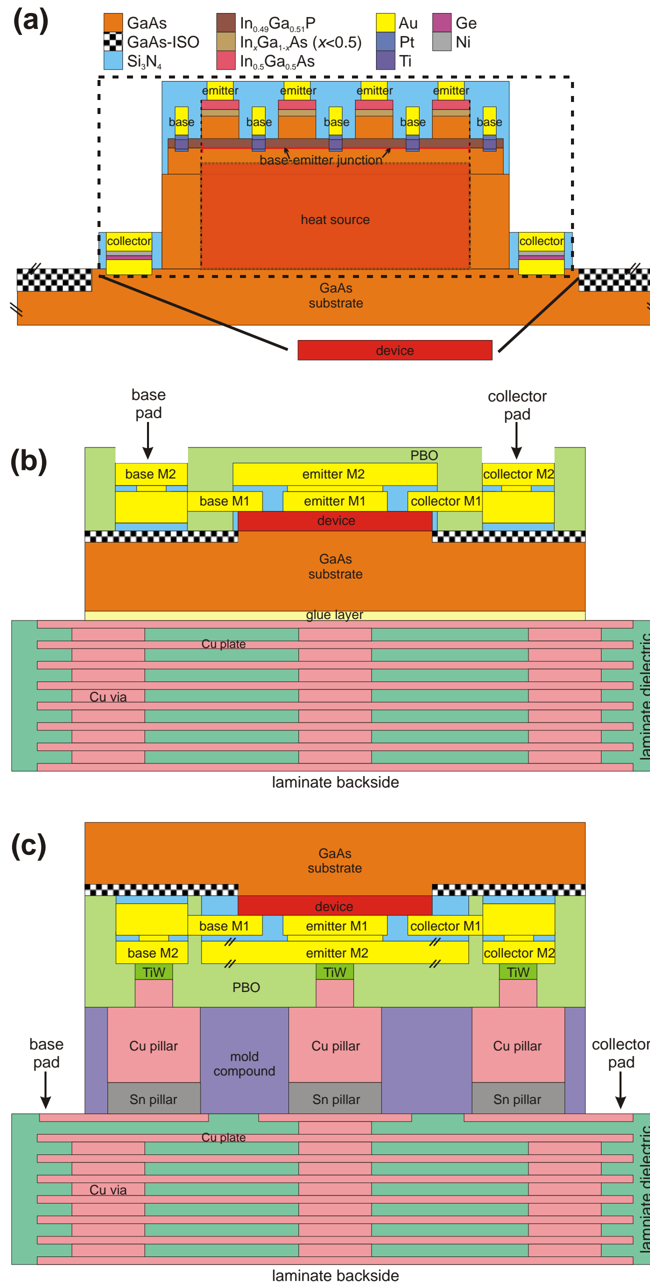



**Fig. 2.3** Schematic cross sections (not to scale) of (a) the intrinsic transistor region of the four-emitter RF DUT, and of the whole structures (including packaging) in (b) WB and (c) FC technologies. The intrinsic region in (a) is also referred to as 'device' in (b) and (c) for the sake of clarity.

The device test pads sit on the underlying substrate through a thin $Si_3N_4$ layer providing some thermal shunt effect [Mag14]. Wire bonds are not present since the DUTs are designed for experimental characterization through a probing station.

Recently, high-performance technologies are moving to FC assembly, since this is assumed to offer a variety of benefits compared to the traditional WB solution, including superior thermal and electrical performance, as well as lower package height, at the price of higher cost (unless the pillar rules are kept similar to SMD); nowadays complex modules for several applications are fabricated using FC packaging. The FC DUT is represented in Fig. 2.3c; the 250-µm-thick die is flipped (i.e., the metallization faces the package), and M2 emitter, base, and collector are connected through three pillars (also referred to as bumps) to the laminate, where the pads are accessible for probing, thus allowing experimental characterization. The 80 µm-diameter pillars are composed by a 40-µm-thick Cu portion and a 10-µm-thick Sn solder, and are buried in a mold compound used as underfill material. A typical FC laminate design is adopted, which – differently from the WB counterpart – uses only a central row of three Cu vias (instead of a 3×3 arrangement), the 'inner' one being vertically located below the heat source; a lower number of TVs is indeed found in FC designs in order to save space for signal routing. This allows carrying out a fair comparison between WB and FC technologies shown in Section 4.3.

### 2.1.2 Multi-mesa and arrays

Domains with more than one *unit cell* (defined in Subsection 2.1.1) are described in the following. The analysis shown in Section 6.1 first focuses on test devices provided with 65×65 $\mu m^2$ pads (in a GSG configuration) for experimental characterization. The devices have been designed with a single *unit cell*, as well as with 2 and 3 paralleled cells, respectively (Fig. 2.4, top). Subsequently, the investigation is conducted on transistor arrays for output stages of PAs comprising 24 and 28 *unit cells*, respectively (Fig. 2.4, bottom).

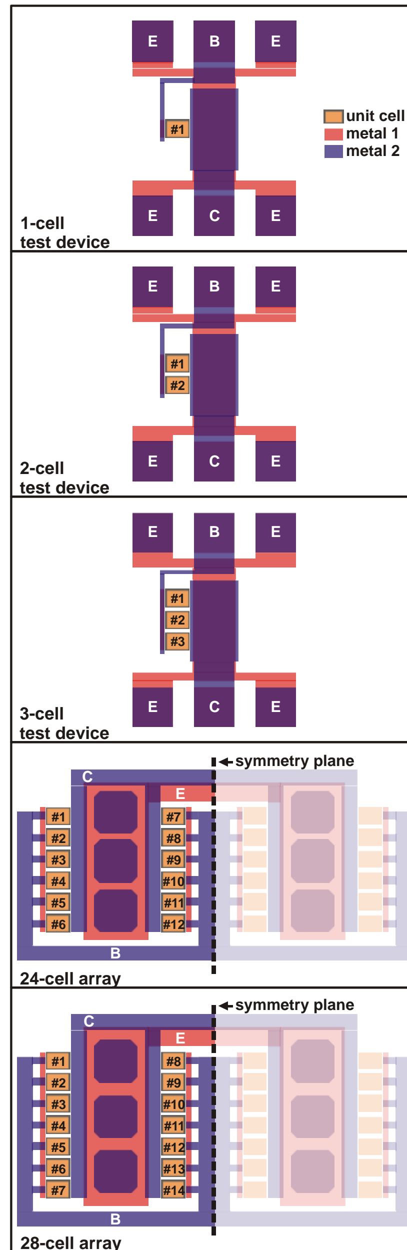



**Fig. 2.4** Schematic layouts representations of all the structures analyzed in Section 6.1. From the top: 1-, 2-, 3-cell test devices; 24- and 28-cell arrays; only half of the arrays (comprising 12 and 14 *unit cells*, respectively) was thermally and electro-thermally simulated.

More specifically, the 24-(28-) cell array is arranged in 4 columns composed by 6 (7) cells each. The arrays are again assumed to lie on a 620-µm thick (unthinned) GaAs substrate, which is common for yield probing, i.e., for *known good die* identification.

The 3-D structure and mesh of the test device with 2 *unit cells* is shown in Fig. 2.5; a magnification on the active region – highlighting the metal layers covering the devices – is shown in Fig. 2.5b. Fig. 2.6 depicts mesh and structures of the 28-cells array counterpart.

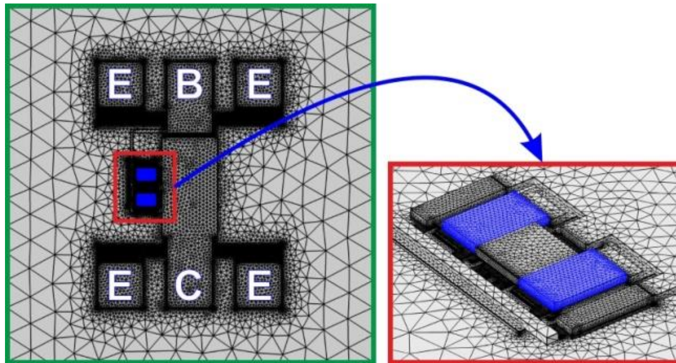



**Fig. 2.5** Mesh for the test device composed by 2 paralleled 4-finger *unit cells*. The elements (tetrahedra) and degrees of freedom (DoFs) are $2.4\times10^6$ and $3.3\times10^6$, respectively. A horizontally-large substrate (not fully represented in the figure) was considered to safely neglect the effect of the lateral adiabatic sides on the temperature field over the base-emitter junction.

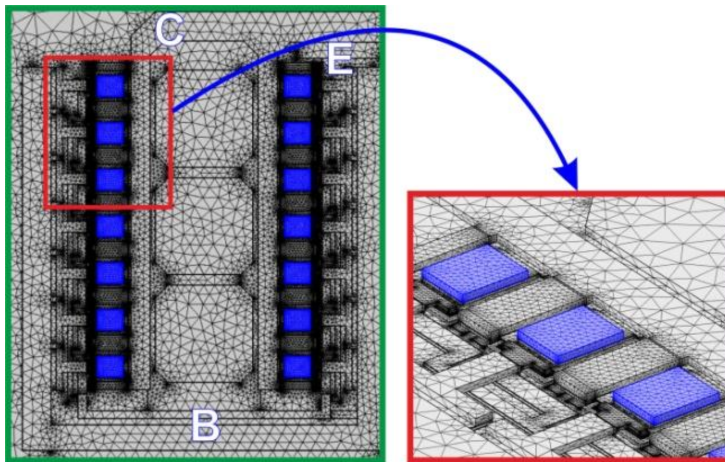



**Fig. 2.6** Mesh for half of the 28-cell array with 7 *unit cells* per column. The elements and DoFs are $3.9\times10^6$ and $5.2\times10^6$, respectively.

### 2.1.3 WLAN power amplifiers structures

The HBT-only process previously shown is considered. The RF power HBT (denoted as #1) has four $2 \times 20.5$ µm$^2$ emitter fingers (the total emitter area is $A_E$=164 µm$^2$), while the bias device (referred to as #2) has only one emitter finger with area $2 \times 10.5$=21 µm$^2$. The thinned GaAs substrate is 75-µm thick. The (grounded) emitter terminals of the HBTs are connected by the 2$^{nd}$-level Au TM, which is expected to be important in terms of thermal coupling, as shown in [Dai05] for steady-state conditions; away from the active regions, the TM runs over a dielectric layer (either $Si_3N_4$ or BCB). The top view of the PA structure and mesh are shown in Fig. 2.7a, while Fig. 2.7b depicts a magnification of the active area highlighting (i) the two devices and (ii) the interconnection among them realized by means of M2.

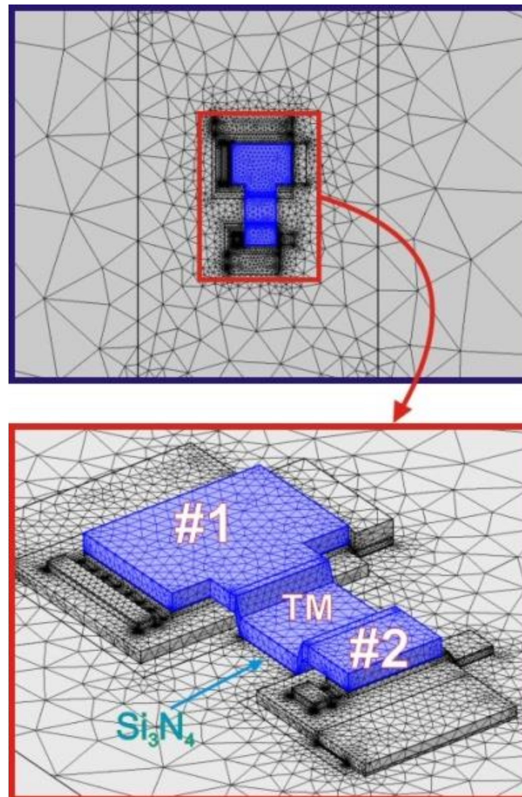



**Fig. 2.7** Mesh of the reference PA illustrating the RF (#1) and bias (#2) transistors. The elements (tetrahedra) and DoFs are about $5 \times 10^5$ and $7 \times 10^5$, respectively.

## 2.2 Power Systems

This Section offers a detailed overview of the power systems under test. The multi-chip SiC PMs fabricated in the SSC and DSC technologies are presented. The same is made for the GaN-based PCB with emphasis on the role played by TVs and HSK, both analyzed in Section 5.2.

### 2.2.1 SiC-based power modules

Here a description is provided of the main features of the SSC and DSC technologies, along with the differences between them. Fig. 2.8 depicts the schematic cross sections of both PMs technologies emphasizing the materials and the BCs. 3-D representations of the electrical connections in both domains are shown in Fig. 2.9.

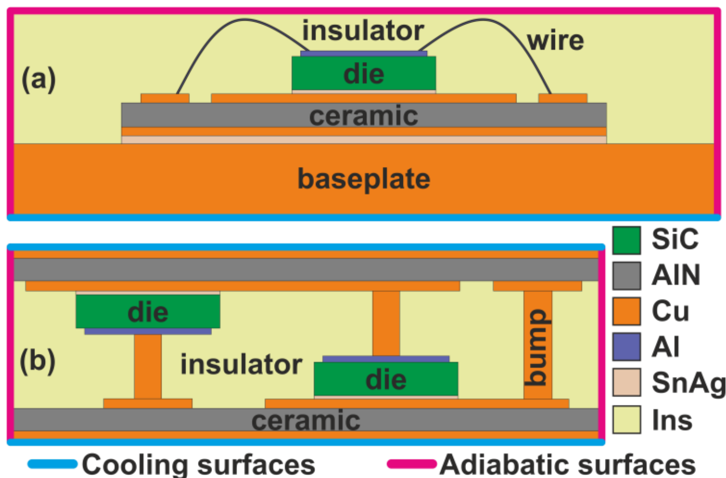



**Fig. 2.8** Schematic cross sections (not to scale) of (a) SSC and (b) DSC PMs illustrating details about materials, thermal BCs, and interconnections (wires and bumps, respectively).

In SSC PMs, the devices lie on the same layer and the interconnections are granted by aluminum wire bonds (Fig. 2.9a) with a diameter of 0.3 mm [Hus18]. Instead, in DSC PMs, the devices are arranged on two different layers and the electrical connections are ensured by copper (Cu) bumps; for the case analyzed in Section 5.1, vertical interconnections are realized by 1 mm-thick and 3.3 mm-wide

bumps shaped as rounded edge cuboids (Fig. 2.9b). The DBC substrate of SSC PMs sits on a thick Cu baseplate, which – besides acting mainly as a mechanical support – carries out the function of thermal interface towards a HSK (or other cooling systems) mounted underneath. The DSC has two DBCs with insulating gel in between them and is prone to be enclosed in a forced liquid cooler, with direct substrate impingement [Sol14a].

Placed between the heat generation regions and the CSs, ceramic layers composing the DBCs play a crucial role in terms of thermal behavior for the SSC and DSC technologies. Both DBCs based on aluminum nitride (AlN) and $Si_3N_4$ are commercially available. In modern large-volume fabrication process of PMs, AlN is typically the material of choice due to its good thermal conductivity and lower cost [Sol14b]. In this thesis, AlN-based DBCs are considered as the standard substrates for both SSC and DSC structures.

A 3-D representation of the modules is shown in Fig. 2.10.

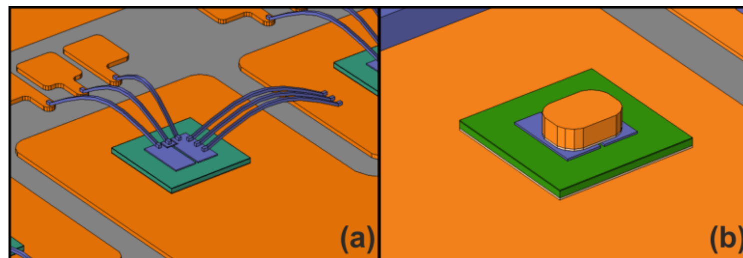



**Fig. 2.9** 3-D representation of the electrical interconnections in the PMs under analysis; (a) SSC wires and (b) DSC bumps.

The PMs studied in Section 6.2 – where ET simulation results with MOR-based TFB are shown – is realized in SSC technology with eight transistors in a half-bridge configuration with 4 devices for each electrical side; the analyses conducted in Section 5.1 – aimed to the thermal comparison of SSC and DSC architectures – are also referred to PMs realized an half bridge, but, in this case, with four transistors (i.e., two for each high and low side).

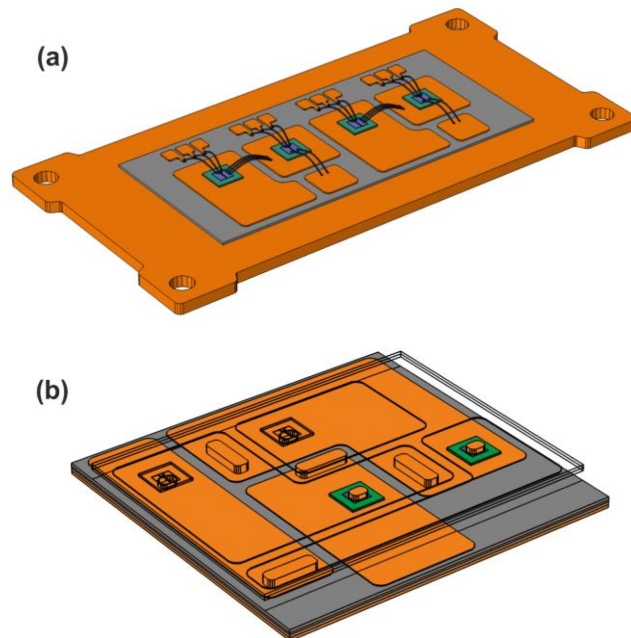



**Fig. 2.10** 3-D structures of (a) SSC and (b) DSC PMs; for illustrative purposes, the top DBC, the transistors, and interconnections are shown in transparency in (b).

### 2.2.2 GaN-based printed circuit board

The cross section of a typical PCB assembly is shown in Fig. 2.11. The electrical contacts of the device package are soldered on the board while the thermal contact is soldered on a PCB area where TVs are realized [Pin00]. On the other side of the board, the designers are used to place a HSK to assist heat removal. The heat flux is mainly vertical and goes from the device to the HSK external surfaces (i.e., the ones exposed to air). Consequently, the design of TVs and HSK plays a paramount role in mitigating the thermal behavior of the devices realized on PCB; an optimum design ensures the targeted circuit performance and reliability, and thus allows reaching most of the superior features of the device technology [Zen18]. The choice of TVs and HSK is usually supported by numerical simulations or experimental characterizations [Ber09], [Ant18].

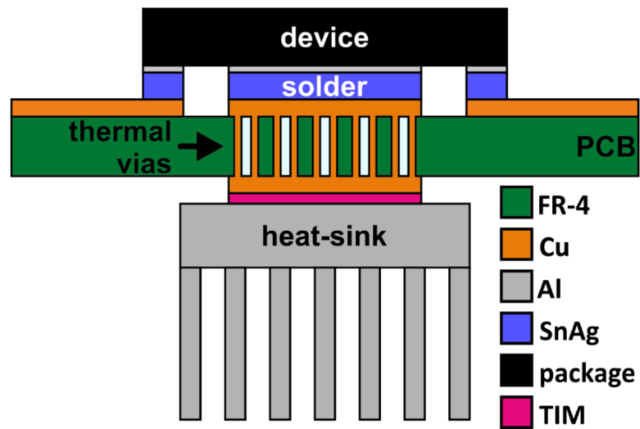



**Fig. 2.11** Schematic cross section (not to scale) of a GaN package sited on a FR-4 PCB pointing out the TVs and HSK positions.

# Chapter 3

# Methodologies

This Chapter describes the methodologies and the approaches exploited to (i) perform thermal simulations and (ii) obtain TFBs devised for ET simulations based on compact models. First, the *in-house* routine to automatically carry out steady-state and dynamic FEM thermal simulations is described; although this is exploitable for each kind of domain, the RF devices were selected as an example to provide an accurate explanation of the tool features. Details about the evaluation of $R_{TH}$s and are also given. An overview of MOR approaches is briefly presented considering – in this case – PMs as application example. The Chapter ends with the thermal properties of the materials composing the analyzed structures.

## 3.1 FEM thermal simulations tool

The flowchart of the proposed tool is schematically sketched in Fig. 3.1. The purely-thermal simulations were performed with the commercial FEM software package COMSOL Multiphysics [COM16].

The *core* of the tool is represented by an *in-house* MATLAB routine [Cod14], [Mag14], [Cat17a], [Cat17b], as will be clarified shortly. The layout of electronic devices, usually stored in graphic data system (GDS) files, comprises a defined number of layers, each corresponding to a mask of the technology process. The GDS layout of a DUT is shown in Fig. 3.2.

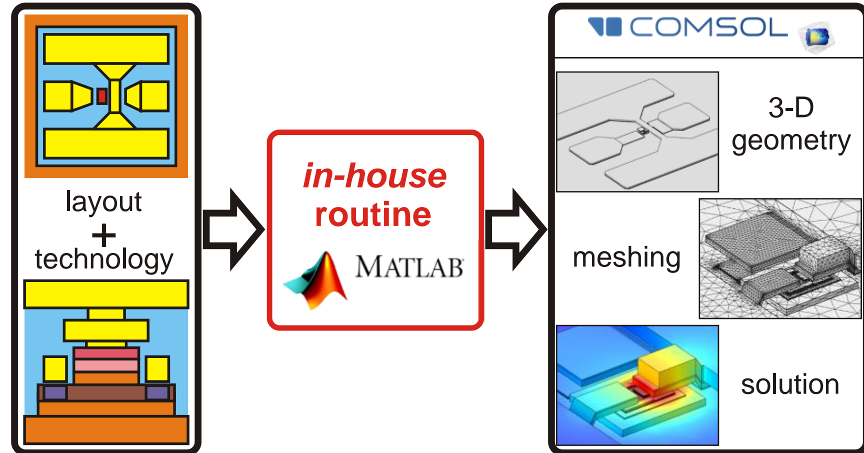



**Fig. 3.1** Flowchart of the proposed tool for automatic FEM simulation in COMSOL Multiphysics environment.

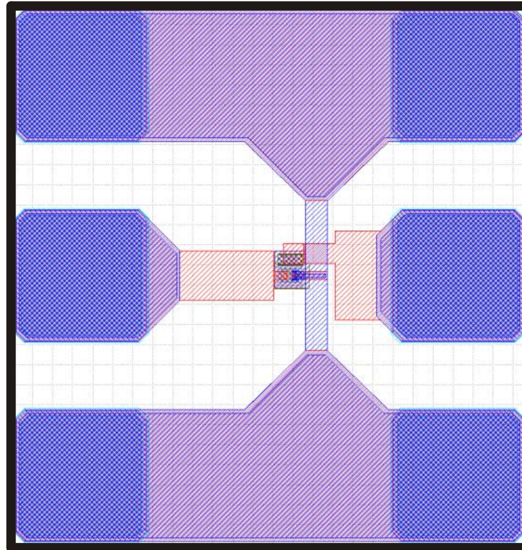


**Fig. 3.2** Example of a GDS layout of the RF DUT (Section 2.1).

The GDS file only contains 2-D information on the device along the horizontal (substrate) plane. Conveniently, starting from the full knowledge of the process, it is possible to define a correspondence between each layer of the layout and its technology features, namely, (i) the thickness, (ii) the quote, i.e., the distance from the top surface of the substrate (denoted as $z$-coordinate in the COMSOL environment),

and (iii) the material parameters; these data are fed to the *in-house* MATLAB routine with a simple code. It is worth noting that (i) and (ii) define the geometry along the third dimension (perpendicular to the substrate plane). The Griesmann's GDSII Toolbox [Link1] is exploited to import the whole layout from the GDS file into the routine. The 2-D layer geometry, described by the position of the vertices, is converted into a matrix; subsequently, this matrix is linked to the corresponding technology features. Then the detailed 3-D geometry of the DUT is *automatically* built in COMSOL Multiphysics by resorting to the MATLAB-COMSOL Livelink [COM16] with the following procedure. Using the collected information, for each layer the routine executes an extrusion process (the flowchart of which is depicted in Fig. 3.3) in 3 steps: (i) it defines a workplane at the layer quote and draws the 2-D horizontal geometry on it (Fig. 3.3b); (ii) it extrudes the layer up to the assigned thickness (Fig. 3.3c); (iii) it then associates the built volumes to a selection (i.e., a group) including all the volumes made of the same material.

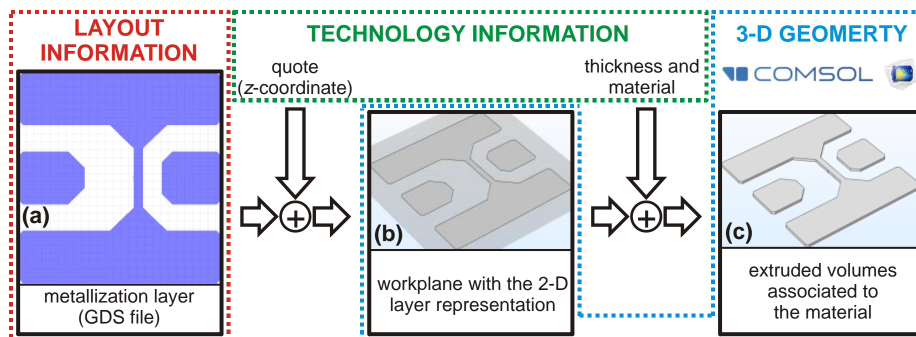



**Fig. 3.3** Flowchart of the extrusion process: (a) metallization layer from the GDS file; (b) workplane in the COMSOL environment with the 2-D representation of the layer; (c) corresponding extruded volumes.

The final outcome is an *exceptionally accurate* and thus realistic representation of the sophisticated 3-D device structure, which is almost impossible to achieve with a prone-to-error and time-intensive manual process (even done by an expert COMSOL user) due to the high number of layers included in the GDS file and their often complex shapes. The routine also handles the meshing process of the resulting 3-D structure in COMSOL. In order to obtain a good trade-off between accuracy and

simulation runtime, the regions where the highest temperature gradients are expected (i.e., those including or surrounding the active device, where the power is dissipated) are extra-densely meshed; moving to regions where the temperature field is not of interest, the mesh is made gradually coarser. The optimized mesh of an RF DUT is shown in Fig. 3.4. Preliminary analyses were performed to demonstrate the mesh convergence, i.e., further mesh refinements did not produce appreciable change in the solution.

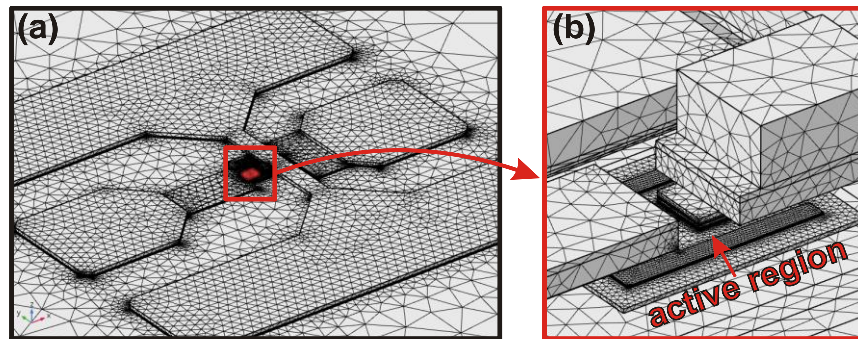



**Fig. 3.4** Mesh of the reference single-emitter RF DUT with $W_E \times L_E = 2 \times 3.5\ \mu m^2$: (a) full view; (b) detail of the extra-fine mesh around the active region.

The BCs, the heat source position, the sensing region, as well as the thermal conductivities are straightforwardly defined within the routine. Nonlinear thermal effects can in principle be activated to describe reliability testing conditions [Cat17], [dAl17].

### 3.1.1 Steady-state analyses

The steady-state thermal simulations are executed in COMSOL, where very low tolerance is set and the numerical solver PARDISO [Sch01] is enabled to exploit the multi-core facilities of modern CPUs. To provide an example of simulation time, 30 s and 150 s are needed for the single simulation of the smallest ($2 \times 3.5\ \mu m^2$) and the largest ($4 \times 20.5\ \mu m^2$) single-emitter RF DUTs, respectively, on a desktop PC equipped by a single Intel i7-5960X and 64 GB RAM. The resulting temperature maps in the whole 3-D structure can be explored with the COMSOL graphic interface in the post-processing stage (an example is shown in Fig. 3.5).

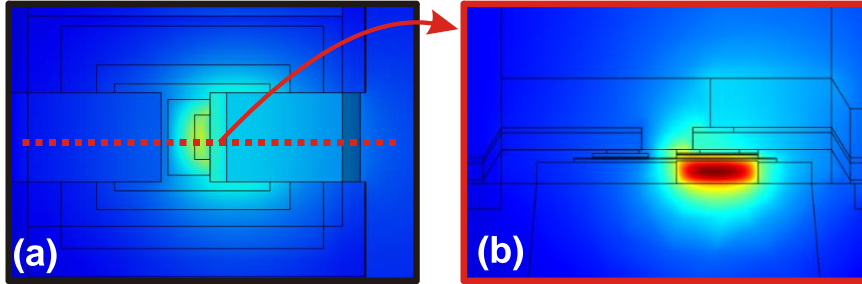



**Fig. 3.5** Temperature field in a RF DUT, as determined by COMSOL: (a) top view and (b) cross section view along the dashed red cut in (a).

The *in-house* routine *automatically* performs the following operational sequence: (i) as mentioned before, it builds the DUT geometry and generates the optimized mesh; (ii) after the COMSOL simulation, it stores the temperature field for further processing; (iii) it calculates some quantities of interest from selected data. This cycle is then repeated for the other DUTs without any user interaction, thus yielding a considerable time saving.

For the analysis conducted in this thesis, the most important quantity to compute is the $R_{TH}$ [K/W], which synthetically describes the steady-state thermal behavior of the devices. In case of multiple devices, the COMSOL results (i.e., the temperature fields) are elaborated to determine the matrix comprising the self-heating (SH) thermal resistances of each device and the mutual-heating (MH) thermal resistances among them. In particular, the $R_{TH}$ matrix evaluation is obtained by the following procedure: (i) a dissipated power $P_{Dj}$ is applied to the *j-th* device; (ii) the simulation results are computed to evaluate the average temperature $T_i$ over the sensing region of the *i-th* device; (iii) Eq. (3.1) is then exploited to evaluate the SH (i=j) and MH (i≠j) thermal resistances.

$$R_{THij} = \frac{T_i - T_0}{P_{Dj}} = \frac{\Delta T_i}{P_{Dj}} \tag{3.1}$$

where $T_0$=300 K is the *reference temperature*. The location of the sensing region depends upon the analyzed device: in RF bipolar transistors, it is associated to the metallurgical base-emitter junction

(see Fig. 2.3), while corresponding to the whole top surface of the device die in the PMs and PCBs.

It must be remarked that, despite the (unfortunate) nomenclature, the MH $R_{TH}$ is an indicator of the degree of thermal coupling between the devices.

### 3.1.2 Transient analyses

Transient thermal simulations can also be performed in COMSOL Multiphysics environment; these analyses are aimed to quantify the dynamic thermal behavior of transistors. The thermal impedance $Z_{TH}$ is a time function summarizing the dynamic response of a device; in case of multiple devices, it is expressed by means of a matrix formulation.

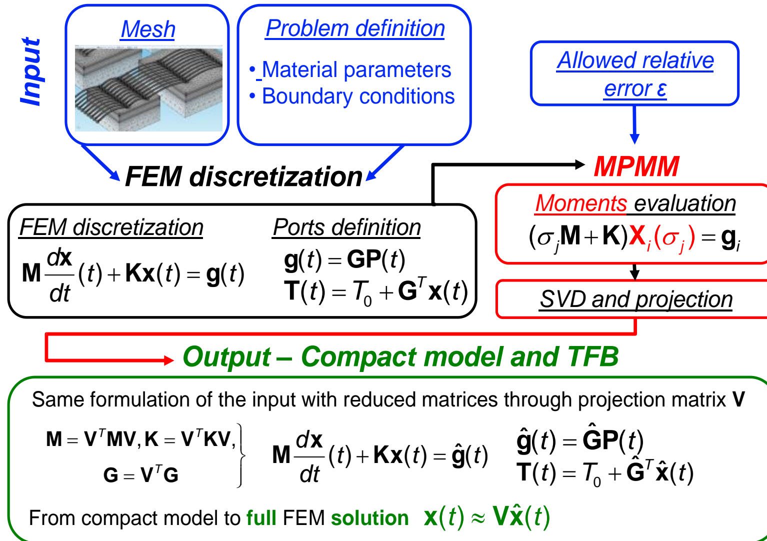
Transient simulations require simulation time and CPU resources higher than the steady-state counterpart; to provide an example, a FEM simulation performed on an RF DUT structure meshed by $5\times10^5$ ($7\times10^5$) tetrahedral elements (degrees of freedom, or DoFs) requires about 50 minutes using the same desktop PC previously mentioned.

Following the same procedure adopted for the $R_{TH}$ matrix, the thermal impedance one can be obtained by applying a step of dissipated power to the heat source of the *j-th* device (i.e., $P_{Dj}$) and by evaluating the *i-th* temperature average ($T_i$) – being a function of the time – in each sensing region; the $Z_{TH}$s are then calculated from [Die61]

$$Z_{THij}(t) = \frac{T_i(t) - T_0}{P_{Dj}} = \frac{\Delta T_i(t)}{P_{Dj}} \tag{3.2}$$

## 3.2 Model-order reduction approaches

To extract the TFBs used to perform steady-state and dynamic ET simulations, it is possible to exploit MOR techniques; the MOR-based approach is briefly described in this Section by means of the work-flow reported in Fig. 3.6.



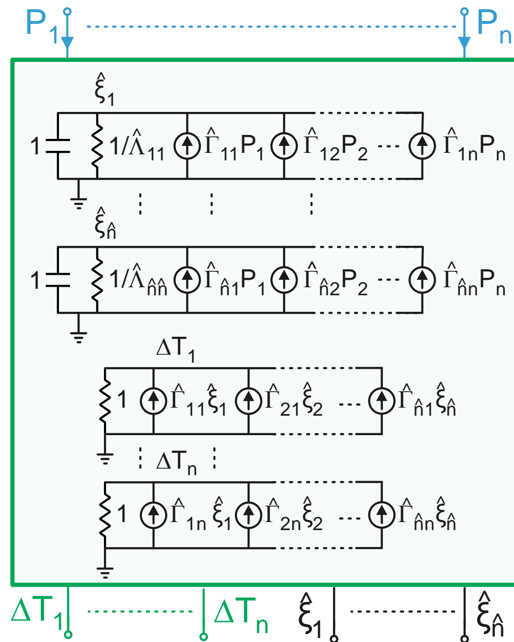



**Fig. 3.6** Proposed TFB extraction procedure (top) and topology (bottom).

The mesh obtained from commercial (e.g., COMSOL) or open-source tools (e.g., SALOME SMESH), as well as material properties and BCs, are provided as input to a routine developed by

Codecasa *et al.* [Cod03a], [Cod03b], [Cod14]. The fully automatic MOR relies on the Multi-Point Moment Matching (MPMM) technique [Cod03a], [Cod03b] and its subsequent improvements – also known in literature as FANTASTIC [Cod14], [Mag14] –, in which the model precision is user-defined by specifying a single error parameter. The TFB topology for $n$ heat sources requires a small number $\hat{n}$ of RC pairs, and is given as output in the form of SPICE netlist.

The MPMM algorithm involves the solution of a limited number of thermal problems in the frequency domain (denoted as *moments*) at automatically evaluated frequencies $\sigma_j$. The TFB is equipped with the following terminals: $P_1, \ldots P_n$ are the power inputs for the heat sources, the average temperature rises of which are given by $\Delta T_1, \ldots \Delta T_n$; $\hat{\xi}_1, \ldots, \hat{\xi}_{\hat{n}}$ are additional variables that allow reconstructing the temperature field over all the points of mesh, and at any time instant, in a *post-processing* step. This approach benefits from the following advantages: (i) it is extremely fast since it does not require costly transient thermal simulations in pre-processing, while preserving all the information of the detailed FEM model; (ii) it can be used for power devices and circuits, including modules and packages, with arbitrary geometries. As will be shown in Section 6.2, the MOR-approach has been exploited to analyze the ET behavior of multi-chip SiC-based PMs.

## 3.3 Materials thermal properties

### 3.3.1 RF devices

The thermal conductivities adopted for the materials, as well as their temperature dependence, described by

$$k(T) = k(T_0) \cdot \left( \frac{T}{T_0} \right)^{-m} \tag{3.3}$$

$$k(T) = k(T_0) - \alpha \cdot (T - T_0) \tag{3.4}$$

with the *reference temperature* $T_0$, are shown in Table 3.1; it can be inferred that (3.3) is for semiconductors and $Si_3N_4$, while (3.4) applies to some metals. More specifically, the conductivities of ternary alloys $A_{1-x}B_x$ were calculated from those of the basic materials A and B by resorting to the following relation [Pal04]:

$$k_{AB} = \frac{1}{\frac{1-x}{k_A} + \frac{x}{k_B} + \frac{(1-x)\cdot x}{C_k}} \tag{3.5}$$

$C_k$ [W/µmK] being denoted as *bowing factor*. Eq. (3.5) allows accounting for the (sometimes significant) conductivity reduction for $x$ values far from 0 and 1. As an example, for the $In_xGa_{1-x}P$ alloy the inputs are $k_{GaP}$ (=$k_A$) = $0.77\times10^{-4}$ W/µmK, $k_{InP}$ (=$k_B$) = $0.68\times10^{-4}$ W/µmK, $C_k$=$0.014\times10^{-4}$ W/µmK, and the mole fraction $x$; in this case, the normally-used lattice matched conditions ($x$=0.49) almost lead to the lowest thermal conductivity. For the ion-implanted (with boron) GaAs region, amorphized to ensure electrical isolation and thus identified as GaAs-ISO in Fig. 2.1, the thermal conductivity was assumed to degrade with respect to crystalline GaAs by a factor 1/100, which was chosen as a reasonable average between the values encountered in [Lie08], [Kim10].

The dynamic thermal properties of materials composing the RF devices are shown in Table 3.2. Temperature dependences of mass density and specific heat are not taken into account in this thesis; then their values at $T_0$ were considered. Since the transient simulations were not performed on the FC structures and old technologies, the dynamic thermal properties of Sn, mold compound, TiW, and $Al_{0.25}Ga_{0.75}As$ were not reported.

The mass density $\rho$ and specific heat $c$ of ternary alloys $A_{1-x}B_x$ were calculated as follows:

$$\begin{aligned} \rho_{AB} &= (1-x)\cdot\rho_A + x\cdot\rho_B \\ c_{AB} &= (1-x)\cdot c_A + x\cdot c_B \end{aligned} \tag{3.6}$$

**TABLE 3.1** THERMAL CONDUCTIVITY VALUES FOR SIMULATIONS OF RF DEVICES

| material | thermal conductivity $k(T_0)$ [W/µmK] | temperature dependence |
|---|---|---|
| GaAs | $0.46\times10^{-4}$ [Pal04] | (3.1), m=1.25 [Pal04], [Pou92], [Pas04] |
| $In_{0.5}Ga_{0.5}As$ | $0.048\times10^{-4}$ [Pal04] | (3.1), m=1.175 [Pal04] |
| $In_xGa_{1-x}As$ | $0.092\times10^{-4}$ [Pal04] average in the layer | (3.1), m=1.212 [Pal04] |
| $In_{0.49}Ga_{0.51}P$ | $0.052\times10^{-4}$ [Pal04] | (3.1), m=1.4 [Pal04] |
| $Al_{0.25}Ga_{0.75}As$ | $0.131\times10^{-4}$ [Pal04] | (3.1), m=1.28 [Pal04] (not used in this work) |
| ion-implanted GaAs | $0.0046\times10^{-4}$ | (3.1), m=1.25 |
| Ge | $0.6\times10^{-4}$ [Pal04] | (3.1), m=1.25 [Pal04] |
| Au | $3.18\times10^{-4}$ [Anh98], [Lie08] | (3.2), $\alpha=6.98\times10^{-8}$ W/µmK$^2$ [Lie08] |
| Pt | $0.71\times10^{-4}$ [Anh98], [Lie08] | independent |
| Ni | $0.91\times10^{-4}$ [Lie08] | (3.2), $\alpha=8.1\times10\text{-}8$ W/µmK$^2$ [Lie08] |
| Ti | $0.22\times10^{-4}$ [Anh98], [Lie08] | independent |
| Cu | $3.98\times10^{-4}$ [Lie08] | (3.2), $\alpha=5.83\times10^{-8}$ W/µmK$^2$ [Lie08] |
| Sn | $0.67\times10^{-4}$ [Lie08] | (3.2), $\alpha=4.03\times10^{-8}$ W/µmK$^2$ [Lie08] |
| $Si_3N_4$ | $0.185\times10^{-4}$ [Kri97], [Pal04] alternative value used for comparative analysis: $0.015\times10^{-4}$ [Anh98] | (3.2), m=-0.33 [Pal04] |
| glue (epoxy) | $1.2\times10^{-4}$ [Link2] | independent |
| mold compound | $0.007\times10^{-4}$ | independent |
| TiW | $1\times10^{-4}$ | not known (not used in this work) |
| laminate dielectric | $0.0065\times10^{-4}$ | independent |
| PBO | $0.0014\times10^{-4}$ | independent |
| BCB | $0.0024\times10^{-4}$ | independent |

**TABLE 3.2** MASS DENSITY AND SPECIFIC HEAT VALUES FOR SIMULATIONS OF RF DEVICES

| **material** | **Mass density** $\rho$ **[Kg/µm$^3$]** | **Specific heat c [J/KgK]** |
|---|---|---|
| GaAs | $5.32\times10^{-15}$ [Pal04] | 322 [Pal04] |
| $In_{0.5}Ga_{0.5}As$ | $5.493\times10^{-15}$ [Pal04] | 358 [Pal04] |
| $In_xGa_{1-x}As$ | $5.41\times10^{-15}$ [Pal04]<br>average in the layer | 340 [Pal04]<br>average in the layer |
| $In_{0.49}Ga_{0.51}P$ | $4.457\times10^{-15}$ [Pal04] | 466 [Pal04] |
| ion-implanted GaAs | $5.32\times10^{-15}$ | 322 |
| Ge | $5.327\times10^{-15}$ [Pal04] | 360 [Pal04] |
| Au | $19.32\times10^{-15}$ [Lie08] | 129 [Lie08] |
| Pt | $21.45\times10^{-15}$ [Lie08] | 133 [Lie08] |
| Ni | $8.906\times10^{-15}$ [Lie08] | 445 [Lie08] |
| Ti | $4.54\times10^{-15}$ [Lie08] | 523 [Lie08] |
| Cu | $8.954\times10^{-15}$ [Lie08] | 384 [Lie08] |
| $Si_3N_4$ | $3.1\times10^{-15}$ [Pal04] | 787 [Pal04] |
| glue (epoxy) | $4.2\times10^{-15}$ [Link2] | 324 [Link2] |
| laminate dielectric | $3.4\times10^{-15}$ | 381 |
| PBO | $1.54\times10^{-15}$ | 1400 |
| BCB | $2.25\times10^{-15}$ | 1120 |

### 3.3.2 Power systems

The thermal properties of the material composing the PM and PCB structures are summarized in this Section. It is worth noting that the analyses carried out on SiC- and GaN-based technologies do not consider *nonlinear* effects.

Table 3.3 shows steady-state and dynamic thermal properties of the materials of the SiC-based PM.

Only steady-state thermal simulations were carried out on PCB domains; the $k$ values of the materials of interest are reported in Table 3.4.

**TABLE 3.3** THERMAL CONDUCTIVITY, SPECIFIC HEAT, AND MASS DENSITY OF THE MATERIALS USED IN FEM SIMULATIONS OF SIC-BASED PMS

| material | thermal conductivity k [W/mK] | Specific heat c [J/KgK] | Mass density ρ [Kg/m$^3$] |
|---|---|---|---|
| **SiC** | 370 [Gol01] | 690 [Cod16] | 3211 [Cod16] |
| **Al** | 200 [Lie08] | 900 [Lie08] | 2700 [Lie08] |
| **AlN** | 285 [Gol01] | 600 [Gol01] | 3255 [Gol01] |
| **Cu** | 398 [Lie08] | 385 [Lie08] | 8900 [Lie08] |
| **SnAg** | 57 [See00] | 220 [See00] | 7500 [See00] |
| **Insulator** | 0.29 | 1624 | 1024 |
| **$Si_3N_4$** | 18.5 [Pal04] | 787 [Pal04] | 3100 [Pal04] |

**TABLE 3.4** THERMAL CONDUCTIVITY OF MATERIAL COMPOSING THE GAN-BASED PCB USED IN FEM SIMULATIONS

| material | thermal conductivity k [W/mK] |
|---|---|
| **GaN** | 125 [Gol01] |
| **SiC** | 370 [Gol01] |
| **Cu** | 398 [Lie08] |
| **Al** | 200 [Lie08] |
| **FR-4 (PCB)** | 0.29 [Aza96] |
| **SnAg** | 57 [See00] |
| **Insulator foil (HSK)** | 0.95 |
| **Graphene** | 500 [Gho10] |
| **$Si_3N_4$** | 18.5 [Pal04] |
| **AlN** | 285 [Gol01] |

# Chapter 4

# Thermal analyses of RF bipolar devices

This Chapter summarizes the purely-thermal results obtained for the HBTs described in Section 2.1. The heat spreading and heat shunt mechanisms are analyzed to explain how the thermal behavior is influenced by (i) semiconductor and metal layers composing the devices, (ii) the packaging technology, and (iii) the interconnection between devices. The DOE approach was adopted to achieve a comprehension of the phenomena previously mentioned as well as to obtain a model of the $R_{TH}$s as a function of the parameters of interest; then Section 4.1 is aimed at explaining the DOE procedure and its advantages. The thermal performances of single-emitter devices are explored in Section 4.2, which considers 6 sizes of the emitter mesa; more specifically, (i) a comparison with alternative technologies for the emitter stack is made, and (ii) the influence of the layers of interest is examined. WB and FC packaging techniques in four-emitter HBTs are compared in Section 4.3, while the dynamic thermal coupling between devices composing a circuit for RF PAs is investigated in Section 4.4.

## 4.1 Design of experiments technique

DOE is an efficient approach adopted in every field of engineering (as well as science and finance) to establish approximate models for the prediction of a system response as a function of multiple key input variables (KIVs), also simply denoted as parameters, including their *combined* influence [All06], [Zam13b]. The results obtained by a defined – typically small – number of tests (also referred to as experiments) are analytically processed to evaluate the coefficients of the DOE model (or DOE expansion) describing the system response. The model accuracy is higher if the maximum variation of the response

with respect to a reference condition is small as the KIVs concurrently span their range; for a 20% variation, the DOE model usually ensures reliable predictions.

The main advantages of DOE are as follows: (i) a small number of tests, (ii) a relatively simple model implementation, and (iii) the capability to account for the mutual interaction between all the KIVs.

The system response is represented by the device $R_{TH}$, while the KIVs are the 5 thicknesses of semiconductor and metallization layers reported in Section 2.1 (Table 2.1). The DOE procedure allows obtaining a set of coefficients [K/W] for the $R_{TH}$ model given by

$$
\begin{aligned}
R_{TH} = {} & R_{TH,ref} + R_{THa}\cdot a + R_{THb}\cdot b + R_{THc}\cdot c + R_{THd}\cdot d + R_{THe}\cdot e + \\
& + R_{THab}\cdot(a\cdot b) + R_{THac}\cdot(a\cdot c) + R_{THad}\cdot(a\cdot d) + \\
& + R_{THae}\cdot(a\cdot e) + R_{THbc}\cdot(b\cdot c) + \\
& + R_{THbd}\cdot(b\cdot d) + R_{THbe}\cdot(b\cdot e) + R_{THcd}\cdot(c\cdot d) + \\
& + R_{THce}\cdot(c\cdot e) + R_{THde}\cdot(d\cdot e) + \\
& + R_{THabc}\cdot(a\cdot b\cdot c) + R_{THabd}\cdot(a\cdot b\cdot d) + R_{THabe}\cdot(a\cdot b\cdot e) + \\
& + R_{THacd}\cdot(a\cdot c\cdot d) + R_{THace}\cdot(a\cdot c\cdot e) + R_{THade}\cdot(a\cdot d\cdot e) + \\
& + R_{THbcd}\cdot(b\cdot c\cdot d) + R_{THbce}\cdot(b\cdot c\cdot e) + \\
& + R_{THbde}\cdot(b\cdot d\cdot e) + R_{THcde}\cdot(c\cdot d\cdot e) + \\
& + R_{THabcd}\cdot(a\cdot b\cdot c\cdot d) + R_{THabce}\cdot(a\cdot b\cdot c\cdot e) + \\
& + R_{THabde}\cdot(a\cdot b\cdot d\cdot e) + R_{THacde}\cdot(a\cdot c\cdot d\cdot e) + \\
& + R_{THbcde}\cdot(b\cdot c\cdot d\cdot e) + R_{THabcde}\cdot(a\cdot b\cdot c\cdot d\cdot e) \\
& a = \frac{t_{In_{0.5}Ga_{0.5}As}}{t_{In_{0.5}Ga_{0.5}As,ref}} - 1,\ b = \frac{t_{In_xGa_{1-x}As}}{t_{In_xGa_{1-x}As,ref}} - 1, \\
& c = \frac{t_{In_{0.49}Ga_{0.51}P}}{t_{In_{0.49}Ga_{0.51}P,ref}} - 1,\ d = \frac{t_{M1}}{t_{M1,ref}} - 1,\ e = \frac{t_{M2}}{t_{M2,ref}} - 1
\end{aligned}
\tag{4.1}
$$

Expansion (4.1) describes $R_{TH}$ as a function of the thicknesses of interest ($t_{In_{0.5}Ga_{0.5}As}$, $t_{In_xGa_{1-x}As}$, $t_{In_{0.49}Ga_{0.51}P}$, $t_{M1}$, $t_{M2}$ contained in the variables *a*, *b*, …, *e*, respectively) using 32 coefficients organized and described as shown in Table 4.1.

For the sake of brevity, the DOE is here illustrated for the simpler case with 3 KIVs only, i.e., the layers of the emitter stack (Table 4.2); the generalization to the case of 5 KIVs (considered in this work) can be easily derived. According to the so-called *full factorial* approach, the 3-KIV DOE requires the FEM simulations (tests) of the 9 DUTs reported in Table 4.2a, namely, a DUT with all the KIVs set to their reference values (denoted with the index 0), and $2^3$=8 DUTs with all the combinations of the minima and maxima of the KIVs (identified with indices -1 and +1, respectively); this implies that the 3-D geometry and corresponding mesh must be generated for each DUT. Test results (i.e., the FEM $R_{TH}$s) are processed with simple formulas to determine the DOE coefficients; it is worth noting that this step is *not* based on fitting or calibration stages.

**TABLE 4.1** DESCRIPTION OF THE COEFFICIENTS OF THE DOE MODEL (4.1).

| number | parameter | | description |
|---|---|---|---|
| **1** | $R_{TH,ref}$ | **reference $R_{TH}$** | **$R_{TH}$ with KIVs reference values** |
| **5** | $R_{THa}$, $R_{THb}$, …, $R_{THe}$ | **self-slopes** | **effect of the single KIV** |
| **10** | $R_{THab}$, $R_{THac}$, …, $R_{THde}$ | **2nd-order mutual slopes** | **mutual interaction of 2 KIVs** |
| **10** | $R_{THabc}$, $R_{THabd}$, …, $R_{THcde}$ | **3nd-order mutual slopes** | **mutual interaction of 3 KIVs** |
| **5** | $R_{THabcd}$, $R_{THabce}$, …, $R_{THbcde}$ | **4nd-order mutual slopes** | **mutual interaction of 4 KIVs** |
| **1** | $R_{THabcde}$ | **5nd-order mutual slopes** | **mutual interaction of all the KIVs** |

Table 4.2b explains the procedure to evaluate the self-slope (1st-order coefficient) $R_{THa}$ related to the thickness of the $In_{0.5}Ga_{0.5}As$ layer, which is calculated as

$$R_{THa} = \left(\overline{R_{THa}(+1)} - \overline{R_{THa}(-1)}\right) \cdot t_{In_{0.5}Ga_{0.5}As,ref} \cdot \left(\max\left(t_{In_{0.5}Ga_{0.5}As}\right) - \min\left(t_{In_{0.5}Ga_{0.5}As}\right)\right)^{-1} \tag{4.2}$$

$\overline{R_{THa}(-1)}$ and $\overline{R_{THa}(+1)}$ being the averages of the test $R_{TH}$s corresponding to the 4 combinations of KIVs where $t_{In_{0.5}Ga_{0.5}As}$ is minimum (-1) and the 4 combinations where is maximum (+1), respectively. The difference of the averages is multiplied by the reference value $t_{In_{0.5}Ga_{0.5}As,ref}$ and normalized to the $t_{In_{0.5}Ga_{0.5}As}$ range.

**TABLE 4.2** EXAMPLE OF 3-KIV DOE: (A) LIST OF TESTS (FEM SIMULATIONS); (B) EVALUATION OF SELF-SLOPE $R_{THa}$ CORRESPONDING TO THE THICKNESS OF THE $In_{0.5}Ga_{0.5}As$ LAYER; (C) EVALUATION OF THE MUTUAL SLOPE $R_{THac}$ ASSOCIATED TO THE INTERACTION BETWEEN THE THICKNESSES OF THE $In_{0.5}Ga_{0.5}As$ AND $In_{0.49}Ga_{0.51}P$ LAYERS.

| List of tests (a) | $In_{0.5}Ga_{0.5}As$ | $In_xGa_{1-x}As$ | $In_{0.49}Ga_{0.51}P$ |
|---|---|---|---|
| | 0 (ref) | 0 (ref) | 0 (ref) |
| | -1 (min) | -1 (min) | -1 (min) |
| | -1 (min) | -1 (min) | +1 (max) |
| | -1 (min) | +1 (max) | -1 (min) |
| | -1 (min) | +1 (max) | +1 (max) |
| | +1 (max) | -1 (min) | -1 (min) |
| | +1 (max) | -1 (min) | +1 (max) |
| | +1 (max) | +1 (max) | -1 (min) |
| | +1 (max) | +1 (max) | +1 (max) |

| $In_{0.5}Ga_{0.5}As$ layer self-slope (b) | $In_{0.5}Ga_{0.5}As$ | $In_xGa_{1-x}As$ | $In_{0.49}Ga_{0.51}P$ |
|---|---|---|---|
| | -1 | -1 | -1 |
| | -1 | -1 | +1 |
| | -1 | +1 | -1 |
| | -1 | +1 | +1 |
| | +1 | -1 | -1 |
| | +1 | -1 | +1 |
| | +1 | +1 | -1 |
| | +1 | +1 | +1 |

| $In_{0.5}Ga_{0.5}As$ and $In_{0.49}Ga_{0.51}P$ layers mutual slope | $In_{0.5}Ga_{0.5}As$ | $In_xGa_{1-x}As$ | $In_{0.49}Ga_{0.51}P$ | product |
|---|---|---|---|---|
| | -1 | -1 | -1 | +1 |
| | -1 | -1 | +1 | -1 |
| | -1 | +1 | -1 | +1 |
| | -1 | +1 | +1 | -1 |
| | +1 | -1 | -1 | -1 |
| | +1 | -1 | +1 | +1 |
| | +1 | +1 | -1 | -1 |
| (c) | +1 | +1 | +1 | +1 |

The 2nd-order mutual slopes can be obtained by following a similar method. Let us refer to Table 4.2c, which evidences the indices related to the $In_{0.5}Ga_{0.5}As$ and $In_{0.49}Ga_{0.51}P$ thicknesses and includes the product between the two. The evaluation of the slope $R_{THac}$ corresponding to the above KIVs is calculated as

$$R_{THac} = \left[ \overline{R_{THac}(+1)} - \overline{R_{THac}(-1)} \right] \cdot \\ \cdot t_{In_{0.5}Ga_{0.5}As,ref} \cdot t_{In_{0.49}Ga_{0.51}P,ref} \cdot \\ \cdot \left[ \max\left(t_{In_{0.5}Ga_{0.5}As}\right) - \min\left(t_{In_{0.5}Ga_{0.5}As}\right) \right]^{-1} \cdot \\ \cdot \left[ \max\left(t_{In_{0.49}Ga_{0.51}P}\right) - \min\left(t_{In_{0.49}Ga_{0.51}P}\right) \right]^{-1} \tag{4.3}$$

$\overline{R_{THac}(-1)}$ and $\overline{R_{THac}(+1)}$ being the average values of the test $R_{TH}$s corresponding to the product indices -1 and +1, respectively; the difference $\overline{R_{THac}(+1)} - \overline{R_{THac}(-1)}$ is divided by the product between the ranges of $t_{In_{0.5}Ga_{0.5}As}$ and $t_{In_{0.49}Ga_{0.51}P}$, and multiplied by the product between the reference values. Higher-order coefficients can be evaluated following the same approach. A schematic description of the whole procedure is shown in Fig. 4.1.

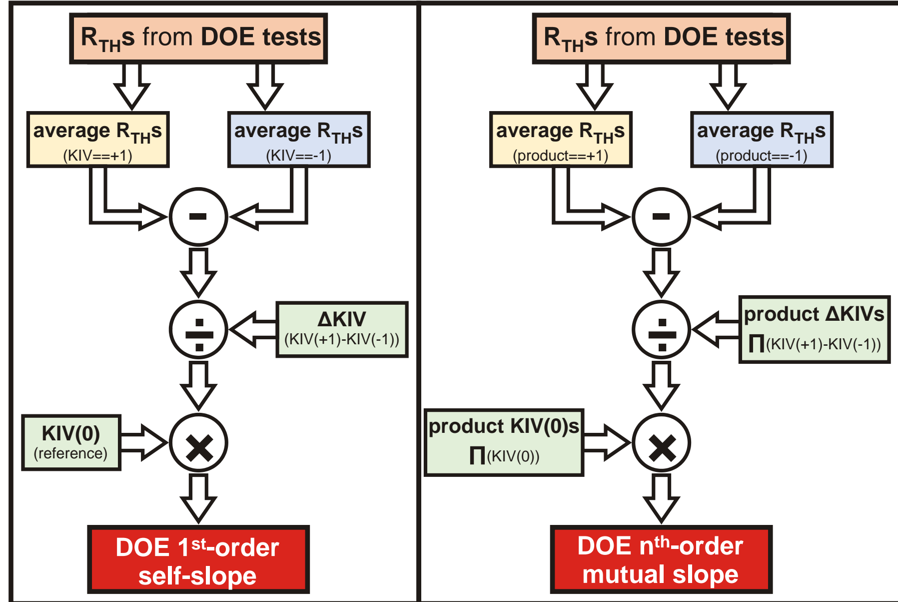



**Fig. 4.1** Representation of the FEM $R_{TH}$s processing to compute the DOE slopes.

## 4.2 Single-emitter devices

Table 4.3 shows all the coefficients of (4.1) obtained by applying the DOE approach on the $R_{TH}$ for the single-emitter structures shown in Section 2.1. In particular, 6 devices with different emitter sizes – namely, different emitter width ($W_E$) and length ($L_E$) – were analyzed; the $W_E$ is taken to be 2 µm and 4 µm, while 3.5, 10.5, and 20.5 µm are considered as $L_E$ values. The $R_{TH}$s of the reference RF DUTs were found to be slightly higher than those obtained in [Cat17a], e.g., 1989 K/W instead of 1878.3 K/W (+5.9%) for the 2×3.5 µm$^2$ DUT, and 722.3 K/W instead of 693.9 K/W (+4.1%) for the 4×20.5 µm$^2$ DUT; this discrepancy is attributed to the inclusion of the amorphized GaAs-ISO region (disregarded in [Cat17a]), which slows down the lateral heat propagation, and – to a lesser extent – to the improved mesh.

**TABLE 4.3** VALUES OF THE COEFFICIENTS OF THE DOE MODEL OF SINGLE-EMITTER DEVICES FOR 6 EMITTER SIZES

| | $W_E \times L_E$ [μm²] | | | | | |
|---|---|---|---|---|---|---|
| **coefficient [K/W]** | **2×3.5** | **2×10.5** | **2×20.5** | **4×3.5** | **4×10.5** | **4×20.5** |
| $R_{TH,ref}$ | **1989** | **1202.2** | **848.2** | **1530** | **988.6** | **722.3** |
| $R_{THa}$ | 102.67 | 41.92 | 20.03 | 80.77 | 33.35 | 15.89 |
| $R_{THb}$ | 36.74 | 15.18 | 7.36 | 28.92 | 12.13 | 5.99 |
| $R_{THc}$ | 137.29 | 52.21 | 25.51 | 93.99 | 36.58 | 17.96 |
| $R_{THd}$ | -75.46 | -39.66 | -23.65 | -65.71 | -36.06 | -22.29 |
| $R_{THe}$ | -142.76 | -109.88 | -59.76 | -130.55 | -100.57 | -57.25 |
| $R_{THab}$ | -7.07 | -2.87 | -1.55 | -4.41 | -1.64 | -0.89 |
| $R_{THac}$ | -15.28 | -5.99 | -3.18 | -9.65 | -3.57 | -1.87 |
| $R_{THad}$ | 2.72 | 0.54 | 0.27 | 2.62 | 0.73 | 0.25 |
| $R_{THae}$ | 5.26 | 2.92 | 1.06 | 4.66 | 2.46 | 0.96 |
| $R_{THbc}$ | -5.43 | -2.29 | -1.29 | -3.43 | -1.39 | -0.82 |
| $R_{THabd}$ | 1.13 | 0.14 | 0.01 | 0.87 | 0.18 | 0.05 |
| $R_{THbe}$ | 2.13 | 1.01 | 0.35 | 1.79 | 0.83 | 0.25 |
| $R_{THcd}$ | 2.89 | 0.64 | 0.26 | 2.39 | 0.51 | 0.26 |
| $R_{THce}$ | 5.51 | 2.53 | 0.88 | 4.41 | 2.13 | 0.71 |
| $R_{THde}$ | 10.12 | 6.51 | 2.47 | 8.74 | 5.73 | 2.38 |
| $R_{THabc}$ | 1.48 | 0.67 | 0.36 | 0.73 | 0.31 | 0.10 |
| $R_{THabd}$ | 0.06 | 0.15 | 0.05 | -0.15 | 0.07 | 0.03 |
| $R_{THabe}$ | -0.31 | -0.01 | -0.02 | -0.24 | -0.06 | 0.01 |
| $R_{THacd}$ | -0.22 | 0.08 | 0.01 | -0.42 | -0.10 | 0.02 |
| $R_{THace}$ | -0.44 | -0.13 | -0.09 | -0.45 | -0.08 | -0.07 |
| $R_{THade}$ | -0.29 | -0.01 | -0.07 | -0.23 | -0.19 | -0.04 |
| $R_{THbcd}$ | -0.27 | -0.11 | -0.18 | -0.08 | 0 | 0.12 |
| $R_{THbce}$ | -0.22 | -0.03 | 0.01 | -0.20 | 0 | 0.05 |
| $R_{THbde}$ | -0.01 | 0.05 | -0.02 | -0.15 | 0.03 | -0.01 |
| $R_{THcde}$ | -0.23 | -0.19 | 0.05 | -0.33 | -0.09 | 0.07 |
| $R_{THabcd}$ | 0.10 | 0.04 | -0.04 | -0.07 | -0.04 | -0.17 |
| $R_{THabce}$ | 0.16 | 0.04 | 0.01 | -0.04 | -0.01 | 0 |
| $R_{THabde}$ | -0.10 | -0.17 | -0.05 | -0.08 | -0.04 | 0 |
| $R_{THacde}$ | -0.37 | -0.44 | 0.18 | 0 | 0.15 | -0.16 |
| $R_{THbcde}$ | -0.02 | -0.01 | -0.02 | 0 | 0.11 | -0.08 |
| $R_{THabcde}$ | 0 | 0.31 | -0.10 | -0.23 | 0.03 | 0.02 |

### 4.2.1 Alternative technologies for the emitter stack

Another study was aimed at estimating the influence on $R_{TH}$ of technology solutions based on alternative emitter materials typical of previous GaAs technologies (see also [Anh98]) in single-emitter devices. Results are shown in Fig. 4.2; as can be seen, modern HBTs suffer from increased thermal issues with respect to the older ones, which is the price to pay for boosting the electrical performance and reliability. It was found that replacing the thermally-resistive ternary InGaAs emitter cap layers with GaAs (without altering the cap thickness) yields a -14.2% $R_{TH}$ decrease for the (smallest) $2 \times 3.5$ $\mu m^2$ DUT, which reduces of -4.5% for the (biggest) $4 \times 20.5$ $\mu m^2$ DUT. In a similar fashion, using a deep $Al_{0.25}Ga_{0.75}As$ emitter layer instead of $In_{0.49}Ga_{0.51}P$ (at the base-emitter junction in the base mesa) leads to an $R_{TH}$ decrease amounting to -4.6% and -1.5% for the aforementioned devices, respectively.

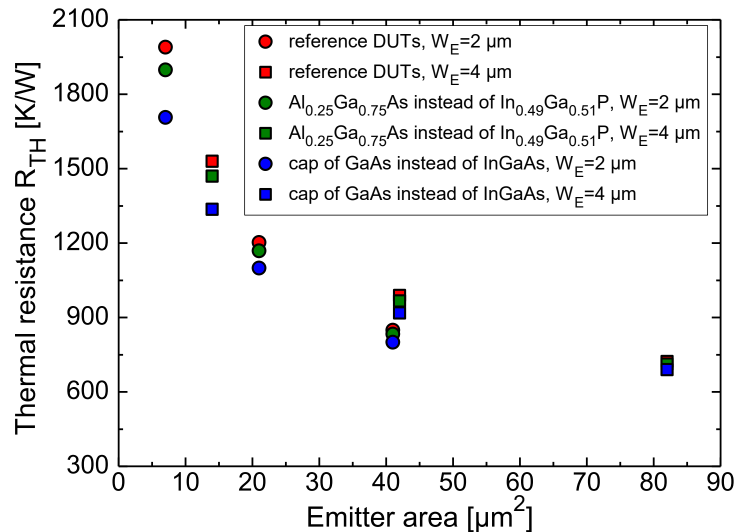



**Fig. 4.2** Impact of the emitter stack technology on $R_{TH}$ in single-emitter devices.

The analysis demonstrates that the role of the emitter layers on the thermal behavior becomes more relevant for downscaled devices, where the relative weight of the upward heat flow is higher due to the shrunk low-resistive path from the heat source to the substrate, while being marginal for large-emitter transistors, since in this case the

downward heat propagation to the sink is favored by the bigger mesa. It is noteworthy that all the above $R_{TH}$ reductions are higher than the ones reported in [Cat17a] (-7.9% and -1.2% for the GaAs cap, -3.5% and -0.7% for the deep $Al_{0.25}Ga_{0.75}As$ layer) since the presence of the damaged GaAs-ISO region moderately hampers the downward heat spreading, thereby enhancing the upward heat flow through the emitter stack.

### 4.2.2 Influence of technology parameters

The following considerations can be made on values/signs of coefficients in Table 4.3.

- The positive sign of the self-slopes of the emitter layers ($R_{THa}$, $R_{THb}$, and $R_{THc}$) evidences that a thicker (more thermally-resistive) emitter increasingly inhibits the upward heat flow, thus raising the $R_{TH}$.
- Conversely, thicker Au metallization layers cool down the DUTs, as witnessed by the negative sign of the corresponding self-slopes ($R_{THd}$ and $R_{THe}$), the major role being played by M2. This can be explained with the aid of the simplified cross section reported in Fig. 4.3, which schematically illustrates the shunt effect: the upward heat emerging from the base-collector SCR, after flowing through the thermally-resistive emitter stack, propagates in M1, then spreads in M2, and subsequently is injected into the GaAs substrate through M1 and the thin underlying $Si_3N_4$ layer; this represents an alternative path for the heat generated in the dissipation region to reach the HSK at the substrate backside. More specifically, the thermally-resistive emitter represents the *bottleneck* of this path, while the portion including M1, M2, M1, and the insulating $Si_3N_4$ layer favors the heat flow by virtue of (i) the high Au thermal conductivity, (ii) the huge metallization volume, and (iii) the large area of the M2-M1-$Si_3N_4$ 'landing' stacks. If M2 is thicker (Fig. 4.3b), the shunt effect is enhanced since the lateral heat spreading through M2 increases thanks to the larger Au section crossed by the heat (that is, M2 offers a lower equivalent thermal resistance). Summarizing, the shunt-induced cooling effect can be modulated by varying the

horizontal heat spreading through M2, in turn dependent on its thickness. The increase in M1 thickness has a lower benefit in terms of heat shunt, since the relatively low spreading enhancement is partially offset by the higher thickness of the M2-M1-$Si_3N_4$ 'landing' stacks.

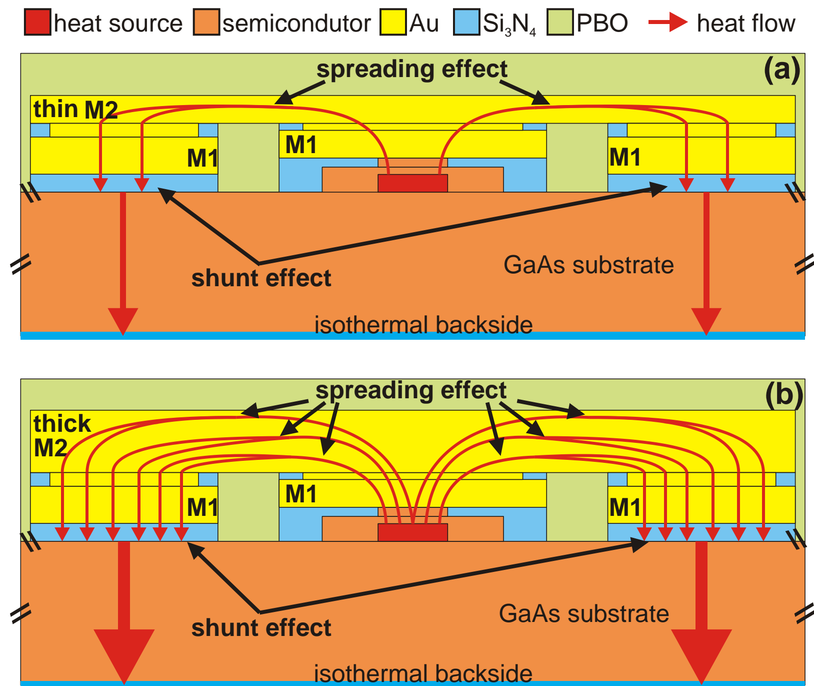
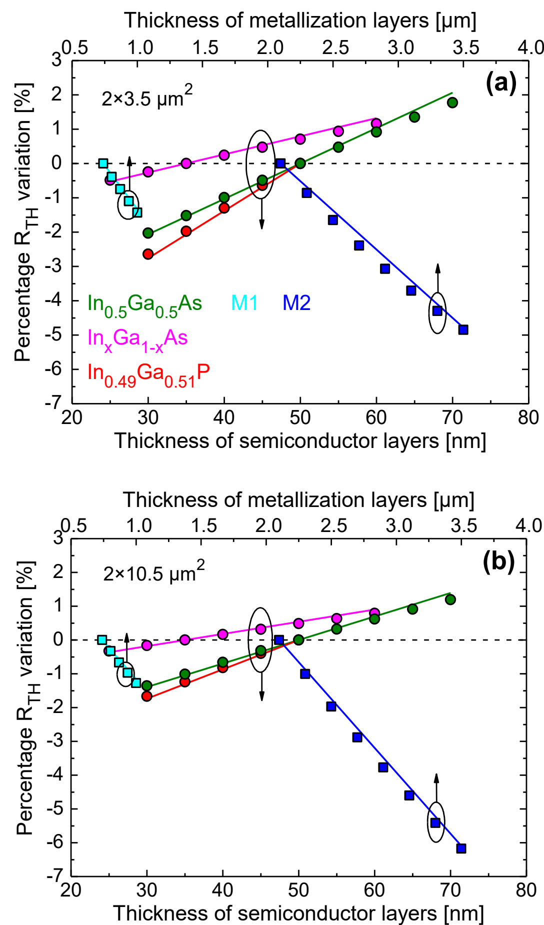


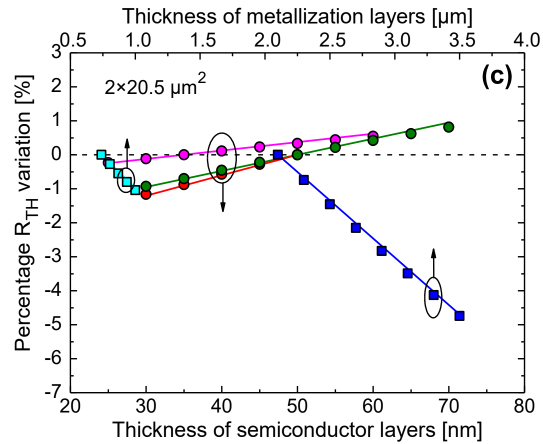

**Fig. 4.3** Schematic representation of heat spreading and heat shunt effects highlighting the impact of the increase of the thickness of the M2 layer: (a) thin and (b) thick M2 layer.

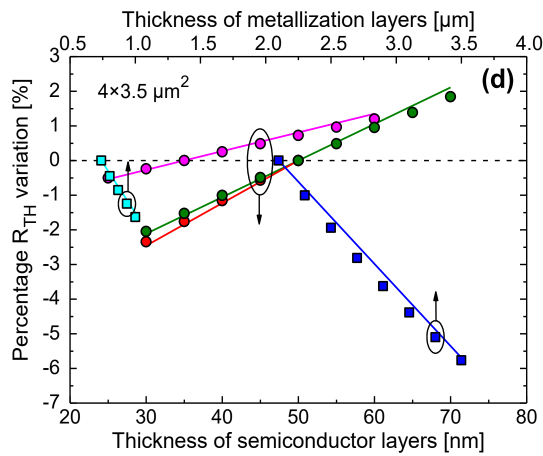
From the above findings it is inferred that, regardless of the combination of $W_E$ and $L_E$ the best (worst) thermal behavior of the DUTs, i.e., the lowest (highest) $R_{TH}$, is obtained by considering the thinnest (thickest) semiconductor layers and thickest (thinnest) metallization layers allowed in the assigned ranges. By making use of the DOE expansion (4.1) with coefficients taken from Table 4.3, it was calculated that in the best technology condition the DUTs would benefit from a $R_{TH}$ reduction (compared to the reference values $R_{TH,ref}$) spanning between -8.2% to -12.6%, whereas in the worst case they

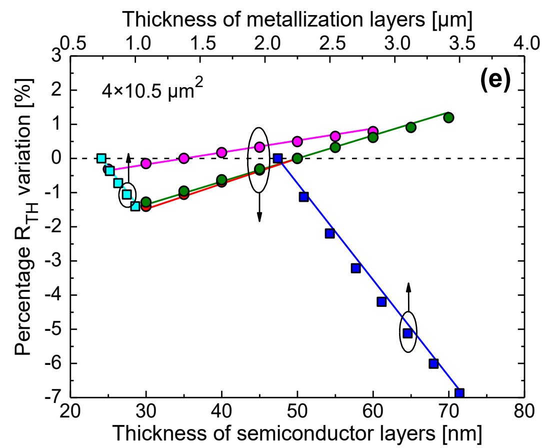
would suffer from a marginal $R_{TH}$ growth falling between 1.4% and 3.4%.

The accuracy of the DOE model (4.1) was verified by FEM simulations performed *a posteriori* (i.e., *after* the extraction of the coefficients listed in Table 4.3) for several combinations of the KIVs (~100 for each emitter × 6 emitters); the resulting $R_{TH}$s can be also referred to as *validation* data. The good alignment between (4.1) and the validation $R_{TH}$s for all DUTs is shown in Fig. 4.4, which reports the percentage $R_{TH}$ variation with respect to $R_{TH,ref}$ obtained by sweeping only one KIV at a time over the corresponding range and keeping the others at their reference values.




Thickness of metallization layers [μm]
0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
2×20.5 μm$^2$
(c)
Percentage $R_{TH}$ variation [%]
3 2 1 0 -1 -2 -3 -4 -5 -6 -7
20 30 40 50 60 70 80
Thickness of semiconductor layers [nm]


Thickness of metallization layers [μm]
0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
4×3.5 μm$^2$
(d)
Percentage $R_{TH}$ variation [%]
3 2 1 0 -1 -2 -3 -4 -5 -6 -7
20 30 40 50 60 70 80
Thickness of semiconductor layers [nm]


Thickness of metallization layers [μm]
0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
4×10.5 μm$^2$
(e)
Percentage $R_{TH}$ variation [%]
3 2 1 0 -1 -2 -3 -4 -5 -6 -7
20 30 40 50 60 70 80
Thickness of semiconductor layers [nm]

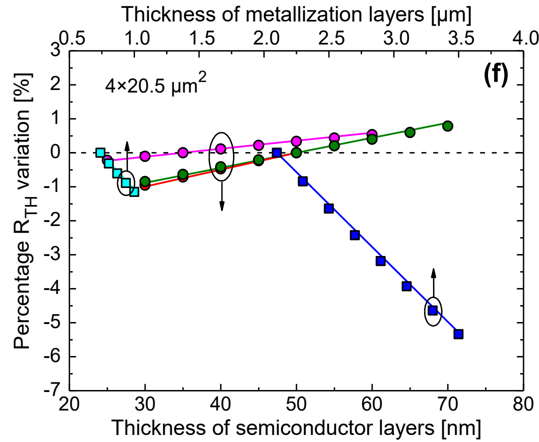



**Fig 4.4** Comparison between the DOE model (solid lines) and *a-posteriori* FEM validation data (symbols) in single-emitter RF DUT for $W_E \times L_E$ equal to (a) 2×3.5, (b) 2×10.5, (c) 2×20.5, (d) 4×3.5, (e) 4×10.5, and (f) 4×20.5 μm$^2$.

Fig. 4.4 allows quantifying (i) the $R_{TH}$ increase due to the lower upward flow induced by thicker semiconductor layers, and (ii) the $R_{TH}$ decrease favored by thicker metallization layers offering improved shunt effect, and thus enhanced heat removal. The following findings can be stated:

- Regardless of $W_E$ and $L_E$, $R_{TH}$ is more sensitive to the thickness of the deep $In_{0.49}Ga_{0.51}P$ layer than to the other layers belonging to the emitter stack, which can be ascribed to its closer proximity to the HS.
- For a given $L_E$, increasing $W_E$ from 2 to 4 μm does not significantly affect the upward heat flow: the impact of the layers of the emitter stack is slightly mitigated, while a marginal increase of the influence of M1 and M2 can be observed.
- For an assigned $W_E$, the KIVs of the emitter stack become more relevant for short (small-$L_E$) DUTs, which is due to the more important role played by the shunt-induced upward heat flow favored by the lower downward flow through the downscaled mesa. This can be also inferred from Fig. 4.5, which shows the 5 percentage self-slopes ($R_{THa}$, $R_{THb}$, $R_{THc}$, $R_{THd}$, $R_{THe}$) normalized to the $R_{THref}$s vs. emitter area (obtained by varying $L_E$ from 3.5 to 20.5 μm) for $W_E$=2 and 4 μm. The sensitivities to the thicknesses of M1 and M2 are expected to reduce for

higher $L_E$ due to the growing relevance of the downward flow. An unexpected behavior is only encountered for the M2 thickness at $L_E$=3.5 µm, where the absolute value of the percentage self-slope is lower than the $L_E$=10.5 µm one, regardless of $W_E$; this is attributed to the specific layout corresponding to $L_E$=3.5 µm, where the overlap between M2 and the underlying heat source is only partial (thus mitigating the impact of the M2 thickness), while being almost complete for longer DUTs.

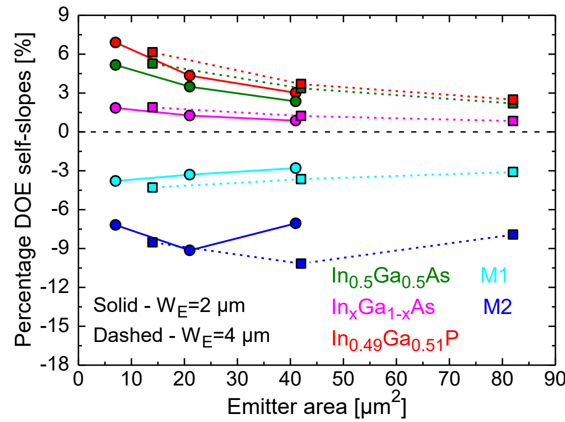



**Fig. 4.5** DOE self-slopes multiplied by 100 and divided by the $R_{TH,ref}$s against $W_E \times L_E$ for $W_E$=2 µm (solid lines) and 4 µm (dashed).

Further – and overwhelming – evidence of the accuracy of the DOE expansion is given in Fig. 4.6, which shows the comparison between (4.1) and *a posteriori* simulations for the DUT with $W_E \times L_E$=2×10.5 µm$^2$, performed by varying a KIV in the corresponding range, and keeping the others at the values leading to the best (worst) thermal behavior; this was obtained by considering the thinnest (thickest) semiconductor layers and the thickest (thinnest) metallization layers. Still a good matching is obtained, although the assigned KIVs are – at least in most cases – far from the reference values, which highlights the significance of this test.

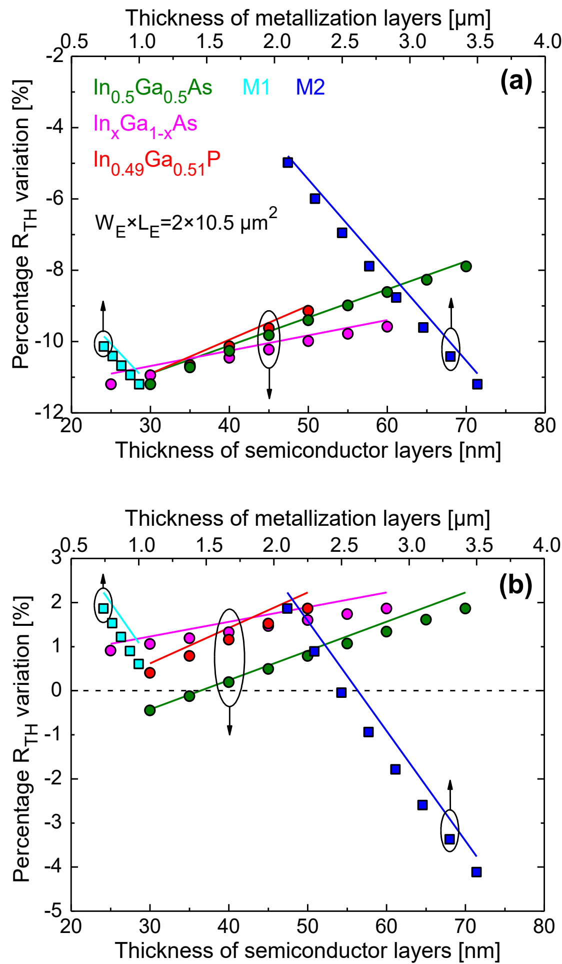



**Fig. 4.6** Comparison between the DOE model (solid lines) and *a-posteriori* FEM validation data (symbols) for the single-emitter RF DUT with $W_E \times L_E = 2 \times 10.5\ \mu m^2$; (a) best and (b) worst case for the fixed KIVs.

## 4.3 Influence of packaging techniques

Following the technology details provided in Subsection 2.1.1, the thermal behavior of WB and FC packaging styles was analyzed by means of FEM simulations. In both structures, the impact of emitter stack – hereinafter denoted as cap – and the dielectric choice were investigated. A further analysis was conducted to study the influence of

the geometrical features of the laminate on the $R_{TH}$s of both technologies. Finally, the DOE was applied to quantify the impact of semiconductors and metal layers on the thermal performances. Temperature dependence of the thermal conductivity was considered in the study about the WB technology pointing out the comparison with the actual device $R_{TH}$ and the one that can be (in principle) evaluated by means of measurement techniques based on infrared (IR) imaging.

### 4.3.1 Wire-bonding technology

The simulated $R_{TH}$ of the reference RF DUT $R_{TH,ref}$ with four emitters (Subsection 2.1.1) was found to be 436.6 K/W.

As previously shown with the single-emitter devices, a first study was aimed to estimate the influence on $R_{TH}$ of technology solutions based on alternative emitter materials. Table 4.4 shows that replacing the thermally-resistive ternary InGaAs emitter cap layers with GaAs (without altering the cap thickness) yields a -0.7% $R_{TH}$ reduction (but the emitter resistance may significantly grow up); similarly, adopting an $Al_{0.25}Ga_{0.75}As$ layer for the deep emitter (as in 'old' HBT technology) in lieu of $In_{0.49}Ga_{0.51}P$ provides a marginal cooling action (-0.5% $R_{TH}$ lowering). Simulations were also performed to 'emulate' the detrimental effect due to heavy process strain on the thermal conductivity of the InGaAs cap, which was set to the reference conductivity of $In_{0.5}Ga_{0.5}As$ divided by factors 2.5 and 5;[1] it was found that $R_{TH}$ increases by 0.7% and 1.2%, respectively. The same analyses were repeated by assigning a much lower thermal conductivity ($0.015\times10^{-4}$ W/µmK [Anh98]) to $Si_3N_4$, which surrounds the active device region (Fig. 2.3a). In this case, the $R_{TH}$ (474.3 K/W) grows by 8.6% compared to $R_{TH,ref}$ (436.6 K/W) due to the drastic shrinking of the path for the upward heat flow. A further study evidenced that with this poorly-conductive $Si_3N_4$ the layers of the emitter stack play a slightly more important role with respect to the reference case. Nevertheless, the value $0.185\times10^{-4}$ W/µmK is chosen as a reference since it is more commonly encountered in the literature.

[1] Such a choice stems from the fact that the mobility is known to undergo a strain-induced degradation by similar factors.

**TABLE 4.4** WB TECHNOLOGY: INFLUENCE OF EMITTER STACK ON $R_{TH}$

| | $R_{TH}$ [K/W] |
|---|---|
| **reference DUT** | 436.6 |
| **GaAs (instead of InGaAs) cap** | 433.7 (-0.7%) |
| **$Al_{0.25}Ga_{0.75}As$ instead of $In_{0.49}Ga_{0.51}P$** | 434.6 (-0.5%) |
| **k(cap)=0.0192×10$^{-4}$ W/μmK due to strain** | 439.8 (+0.7%) |
| **k(cap)=0.0096×10$^{-4}$ W/μmK due to strain** | 441.7 (+1.2%) |
| **thermal conductivity of $Si_3N_4$: 0.015×10$^{-4}$ W/μmK [Anh98] (reference: 0.185×10$^{-4}$ W/μmK)** | 474.3 (+8.6%) |

Another analysis was conceived to quantify the influence of the laminate design; the main results are reported in Table 4.5. It is shown that the laminate weakly contributes to the $R_{TH}$ of the whole structure thanks to the high thermal conductivity offered by the wide (the diameter being 125 μm) 3×3 Cu vias (i.e., it almost behaves as a thermal short-circuit): fully removing it and applying the thermal ground to the GaAs substrate bottom favors indeed only a -2.8% $R_{TH}$ reduction. Conversely, shrinking the vias to a diameter of 60 μm perceptibly hinders the downward heat propagation, and $R_{TH}$ increases by 5.2%. Further findings are: (i) little impact is induced by the thickness of the vias; (ii) $R_{TH}$ is almost insensitive to the thickness of the Cu plates due to a compensation between heat spreading and longer heat path to the sink; (iii) the role played by the (uncertain) thermal conductivity of the laminate dielectric can be safely disregarded since the heat flows mainly through the Cu vias. In a practical sense, this 'lack of sensitivity' is important for design support since these features often change from a laminate technology to another.

The individual and combined sensitivity to all parameters reported in Table 2.1 was then quantified from expansion (4.1), the coefficients of which, listed in Table 4.6, were determined from the few FEM $R_{TH}$s required by DOE. Fig. 4.7 illustrates the percentage $R_{TH}$ variation with respect to $R_{TH,ref}$; also in this case, only a parameter was varied in the assigned range while keeping the others equal to the reference values, or equal to values that minimize (maximize) $R_{TH}$, i.e., the minimum (maximum) thicknesses for the semiconductor layers and

maximum (minimum) for the metal ones. This allows gaining an in-depth insight into the influence of the parameters over the assigned ranges.

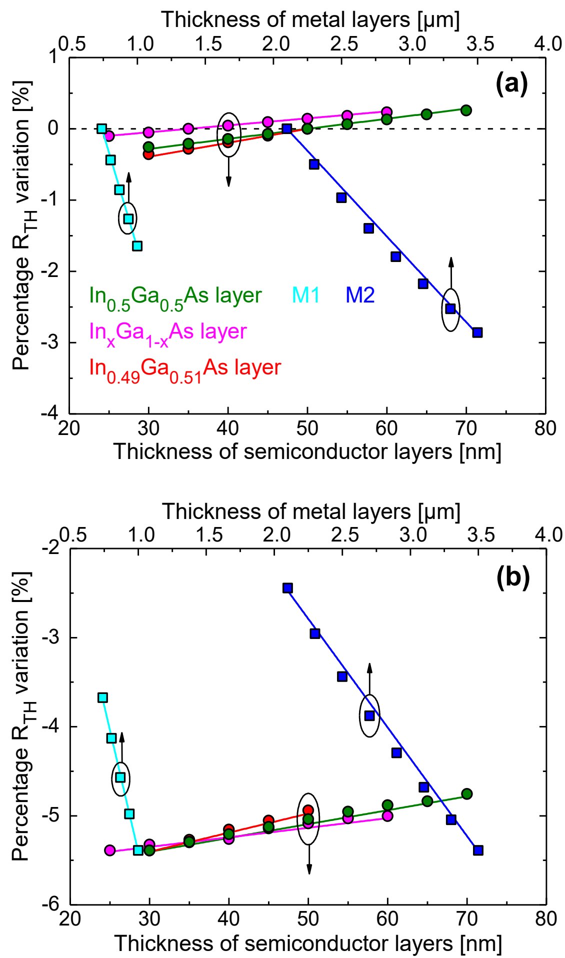
**TABLE 4.5** WB TECHNOLOGY: INFLUENCE OF LAMINATE DESIGN ON $R_{TH}$

| | **$R_{TH}$ [K/W]** |
|---|---|
| **reference DUT** | 436.6 |
| **DUT without laminate** | 424.3 (-2.8%) |
| **laminate vias thickness: 15 µm (reference: 25 µm)** | 434.7 (-0.4%) |
| **laminate vias thickness: 35 µm (reference: 25 µm)** | 438.5 (+0.4%) |
| **laminate vias diameter: 60 µm (reference: 125 µm)** | 459.2 (+5.2%) |
| **laminate metal layers thickness: 9 µm (reference: 12 µm)** | 436.7 (<0.1%) |
| **laminate metal layers thickness: 19 µm (reference: 12 µm)** | 436.7 (<0.1%) |
| **thermal conductivity of the laminate dielectric: $0.1\times10^{-4}$ W/µmK (reference: $0.0065\times10^{-4}$ W/µmK)** | 435.6 (-0.2%) |

**TABLE 4.6** WB TECHNOLOGY: COEFFICIENTS [K/W] OF THE DOE EXPANSION (4.1)

| **$R_{TH,ref}$** | **436.6** | **$R_{THbd}$** | 0.08 | **$R_{THbcd}$** | 0.03 |
|---|---|---|---|---|---|
| **$R_{THa}$** | 3.08 | **$R_{THbe}$** | 0.07 | **$R_{THbce}$** | 0.02 |
| **$R_{THb}$** | 1.49 | **$R_{THcd}$** | 0.31 | **$R_{THbde}$** | -0.02 |
| **$R_{THc}$** | 4.28 | **$R_{THce}$** | 0.14 | **$R_{THcde}$** | 0.1 |
| **$R_{THd}$** | -20.76 | **$R_{THde}$** | -0.34 | **$R_{THabcd}$** | -0.08 |
| **$R_{THe}$** | -18.9 | **$R_{THabc}$** | 0.02 | **$R_{THabce}$** | 0.02 |
| **$R_{THab}$** | -0.07 | **$R_{THabd}$** | -0.02 | **$R_{THabde}$** | 0.01 |
| **$R_{THac}$** | -0.3 | **$R_{THabe}$** | -0.02 | **$R_{THacde}$** | -0.04 |
| **$R_{THad}$** | 0.16 | **$R_{THacd}$** | -0.01 | **$R_{THbcde}$** | 0.01 |
| **$R_{THae}$** | 0.15 | **$R_{THace}$** | -0.02 | **$R_{THabcde}$** | 0.05 |
| **$R_{THbc}$** | -0.13 | **$R_{THade}$** | -0.03 | | |

Simulations were also carried out to examine the behavior of the four-emitters RF DUT under a large variety of operating conditions, which is particularly important for reliability studies (e.g., [Zam13a]). Nonlinear thermal effects were activated by enabling (3.3) and (3.4) in COMSOL with the coefficients reported in Table 3.1.



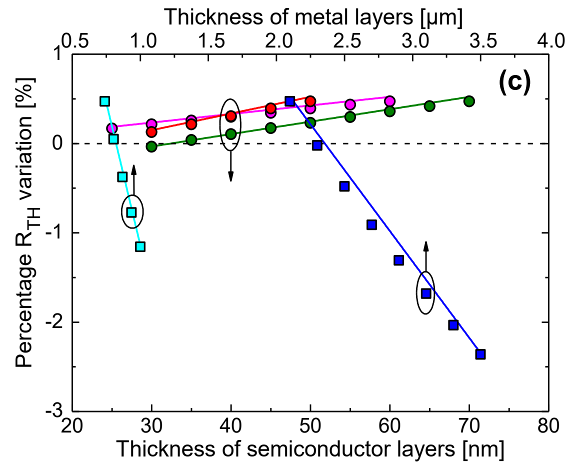



**Fig. 4.7** WB technology: percentage $R_{TH}$ variation with respect to $R_{TH,ref}$, as obtained by modifying only one parameter, and keeping the others equal to (a) the reference values, or equal to the values ensuring the (b) lowest and (c) highest $R_{TH}$. Expansion (4.1) (solid lines) with coefficients reported in Table 4.4 is compared to *validation* data (symbols).

Wide ranges were explored for the temperature of the laminate backside (which in practical cases might not be a good thermal ground) and $P_D$ (corresponding to $V_C$=5 V and $J_C$=1, 10, 20, 30, 40 kA/cm$^2$), both enhancing nonlinear thermal effects [Wal01]. Fig. 4.8 shows the average temperatures over the emitter M2 top and the base-emitter junction under the previously described conditions, while Fig. 4.9 illustrates the temperature distribution over a cross section taken along the emitter center for a backside temperature equal to $T_0$=300 K and power amounting to 164 mW.[2] This analysis is intended to provide clear guidelines concerning the limits (in terms of backside temperature and power) beyond which the device may experience thermally-induced reliability issues. As an example, the $P_D$ for $T_0$

[2] All simulations shown in this Chapter were performed by keeping unchanged the heat source geometry, which vertically coincides with the lightly-doped collector assumed to be fully depleted. However, it must be remarked that at high collector current density $J_C$ (high $V_{BE}$) the Kirk (base push-out) effect takes place, which 'pushes' the electric field (and thus the dissipation region) toward the interface with the $N^+$ subcollector. Additional simulations allowed determining that the thermal behavior is marginally mitigated by the Kirk effect in both packaging solutions since the thinner heat source is farther away from the base-emitter junction, whereas a slightly higher temperature is reached within the dissipation region due to the increased power density.

applied to the backside should not exceed 250 mW since the maximum operating temperature is usually assigned to 420 K.

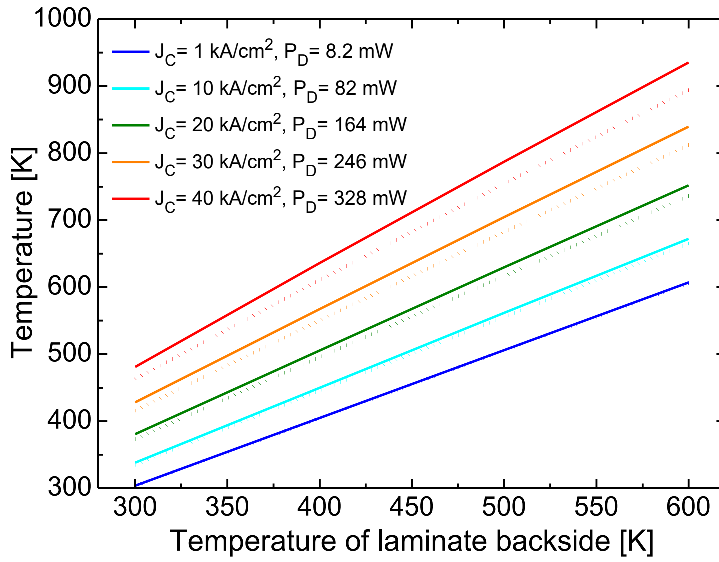



**Fig. 4.8** WB technology: average temperatures over the base-emitter junction (solid lines) and the top surface of emitter M2 'seen' by IR (dotted) as a function of temperature of laminate backside for various $P_D$s.

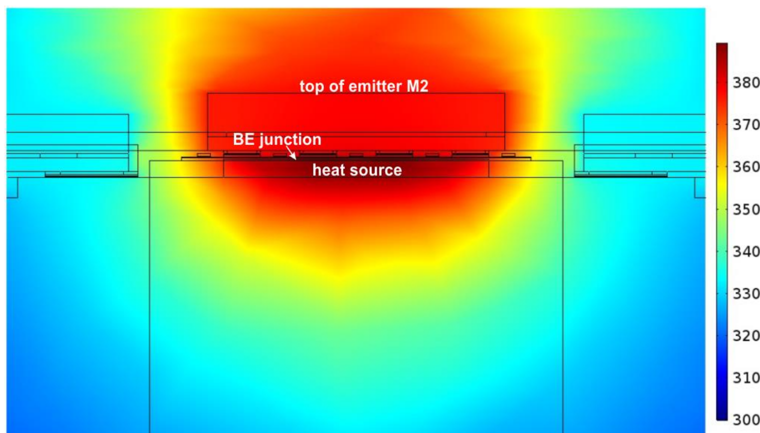



**Fig. 4.9** WB technology: temperature distribution over a cross section through the emitter center for a backside temperature equal to 300 K and power of 164 mW.

Additionally, it is found that the IR-based imaging, often exploited to get the temperature map over the M2 top, negligibly

underestimates the base-emitter junction temperature (which directly impacts the collector current), unless very high backside temperatures and/or powers are applied – which can be encountered during reliability testing.

### 4.3.2 Flip-chip technology

In the FC technology shown in Subsection 2.1.1, the simulated $R_{TH}$ of the reference RF DUT $R_{TH,ref}$ amounts to 245.8 K/W, which gives rise to -43.7% compared to the WB value (436.6 K/W);[3] the better thermal performance is achieved thanks to the more effective heat flow from the dissipating base-collector SCR to the package through M1, the large emitter M2, and the Cu/Sn pillars, while the poorly-conducting GaAs substrate is removed from the path.[4] Thus, it is found that the lower number of Cu vias compared to the WB package does not sizably affect the thermal behavior of the DUT.

On the other hand, the emitter architecture is expected to play a more relevant role since the emitter layers are part of the path for the heat to reach the thermal ground. This is confirmed by FEM results reported in Table 4.7; the adoption of a GaAs cap instead of the poor InGaAs conductor leads to a -4.2% $R_{TH}$ decrease (to be compared to a reduction of -0.7% in the WB packaging); a deep emitter composed by $Al_{0.25}Ga_{0.75}As$ gives rise to a -2.6% $R_{TH}$ reduction (in WB only favors -0.5%), and the effect of heavy strain on the cap is much more harmful than in WB ($R_{TH}$ grows up to 7.6% instead of 1.2%). In addition, it is found that the correct choice of the thermal conductivity of $Si_3N_4$ is very important when simulating FC assembly: selecting the low value reported in [Anh98] increases $R_{TH}$ by 21% (297.3 K/W) and greatly enhances the influence of the thermal conductivities of the emitter

[3] The opposite result (i.e., $R_{TH}$ of FC assembly higher than the WB counterpart) was obtained in [Lee07], where thermal simulations and infrared characterization were performed on a dual-band RF power amplified module with GaAs HBTs. However, this was due to the adoption of a bump smaller than the heat source in FC; the authors found out that by increasing the bump size the heat was more readily removed from the dissipating region, which turned into an $R_{TH}$ lower than the WB one.

[4] It is worth noting that, contrary to III-V HBTs, SiGe HBTs may not benefit thermally from a FC packaging for many reasons: (i) the silicon substrate enjoys high thermal conductivity; (ii) many companies use Al instead of Cu for the metallization; (iii) in some processes, the metal contacts are smaller than (and almost independent of) the emitter size (and thus smaller than the heat source).

layers (which in this case constitute the only available heat path to the ground); as an example, using a GaAs cap would imply a -9.2% reduction with respect to 297.3 K/W, and a heavy strain on the cap would entail a considerable $R_{TH}$ increase (up to 24.4%).

**TABLE 4.7** FC TECHNOLOGY: INFLUENCE OF EMITTER STACK ON $R_{TH}$

| | **$R_{TH}$ [K/W]** |
|---|---|
| **reference DUT** | 245.8 |
| **GaAs (instead of InGaAs) cap** | 235.6 (-4.2%) |
| **$Al_{0.25}Ga_{0.75}As$ instead of $In_{0.49}Ga_{0.51}P$** | 239.6 (-2.6%) |
| **k(cap)=0.0192×$10^{-4}$ W/μmK due to strain** | 257.4 (+4.9%) |
| **k(cap)=0.0096×$10^{-4}$ W/μmK due to strain** | 264.5 (+7.6%) |
| **thermal conductivity of $Si_3N_4$: 0.015×$10^{-4}$ W/μmK [Anh98] (reference: 0.185×$10^{-4}$ W/μmK)** | 297.3 (+21%) |

An analysis was conducted to understand the influence of the (uncertain [Aki92]) thermal conductivity of the plating TiW layer connecting M2 and pillar (also denoted as *under bump material*), which was assumed to lie between the Ti and W values. Results, reported in Table 4.8, demonstrate that the $R_{TH}$ sensitivity to this parameter is quite marginal: adopting the low Ti conductivity only leads to an 1.8% $R_{TH}$ increase. Moreover, it was found that varying the thickness of this layer over a wide range (20 to 200 nm) does not appreciably affect the thermal behavior of the DUT due to the relatively high thermal conductivity chosen as a reference (1×$10^4$ W/μmK).

The impact of the laminate architecture is expected to be more important than in the WB technology since the heat is more directed to the thermal ground in FC assembly (the upward flow being hampered by the low-conductivity GaAs substrate). The FEM data, listed in Table 4.9, show that the horizontal size of the three vias is very important: shrinking the diameter from 125 μm to 60 μm implies an $R_{TH}$ increase of 26% (it was only 5.2% in the WB packaging).

**TABLE 4.8** FC TECHNOLOGY: INFLUENCE OF CONNECTION ON $R_{TH}$

| | $R_{TH}$ [K/W] |
|---|---|
| **reference DUT** | 245.8 |
| **thermal conductivity of TiW: 0.22×10$^{-4}$ W/µmK (=$k_{Ti}$ [Aki92], [Lie08]) (reference: 1×10$^{-4}$ W/µmK)** | 250.2 (+1.8%) |
| **thermal conductivity of TiW: 1.78×10$^{-4}$ W/µmK (=$k_W$ [Lie08]) (reference: 1×10$^{-4}$ W/µmK)** | 245.1 (-0.3%) |
| **Cu instead of TiW** | 244.5 (-0.5%) |
| **thickness of TiW: 20 nm (reference: 50 nm)** | 244.7 (-0.5%) |
| **thickness of TiW: 100 nm (reference: 50 nm)** | 247.3 (+0.6%) |
| **thickness of TiW: 200 nm (reference: 50 nm)** | 250.1 (+1.8%) |

Thicker Cu plates slightly worsen the thermal behavior since the sink is moved farther away. It was also found that properly choosing the laminate dielectric is important in this technology due to the massive downward flow and, to a lesser extent, to the presence of only three vias: if the conductivity of this dielectric is 0.1×10$^{-4}$ W/µmK (instead of the reference 0.0065×10$^{-4}$ W/µmK) a -8.1% $R_{TH}$ reduction is reached (to be compared to the negligible -0.2% in the WB DUT).

**TABLE 4.9** FC TECHNOLOGY: INFLUENCE OF LAMINATE DESIGN ON $R_{TH}$

| | $R_{TH}$ [K/W] |
|---|---|
| **reference DUT** | 245.8 |
| **laminate vias thickness of 15 µm (reference: 25 µm)** | 236.5 (-3.8%) |
| **laminate vias thickness of 35 µm (reference: 25 µm)** | 254 (+3.3%) |
| **laminate vias diameter of 60 µm (reference: 125 µm)** | 309.7 (+26%) |
| **laminate metal layers thickness of 9 µm (reference: 12 µm)** | 245.4 (-0.2%) |
| **laminate metal layers thickness of 19 µm (reference: 12 µm)** | 247.4 (+0.7%) |
| **thermal conductivity of the laminate dielectric of 0.1×10$^{-4}$ W/µmK (reference: 0.0065×10$^{-4}$ W/µmK)** | 225.9 (-8.1%) |

Also for the FC DUTs, the DOE coefficients of expansion (4.1) were evaluated to examine the individual and interacting influence of the thicknesses of semiconductor and metal layers of interest; the values are reported in Table 4.10.

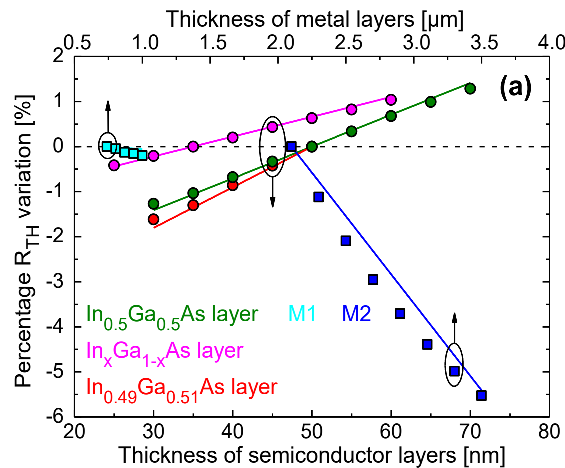
**TABLE 4.10** FC TECHNOLOGY: COEFFICIENTS [K/W] OF THE DOE EXPANSION (4.1)

| $R_{TH,ref}$ | **245.8** | $R_{THbd}$ | 0.01 | $R_{THbcd}$ | -0.02 |
|---|---|---|---|---|---|
| $R_{THa}$ | 8.68 | $R_{THbe}$ | 0.28 | $R_{THbce}$ | 0.02 |
| $R_{THb}$ | 3.79 | $R_{THcd}$ | -0.01 | $R_{THbde}$ | -0.04 |
| $R_{THc}$ | 11.08 | $R_{THce}$ | 0.63 | $R_{THcde}$ | 0.01 |
| $R_{THd}$ | -0.42 | $R_{THde}$ | 1.58 | $R_{THabcd}$ | 0.05 |
| $R_{THe}$ | -19.95 | $R_{THabc}$ | 0.03 | $R_{THabce}$ | -0.02 |
| $R_{THab}$ | -0.25 | $R_{THabd}$ | 0.04 | $R_{THabde}$ | -0.02 |
| $R_{THac}$ | -0.56 | $R_{THabe}$ | -0.03 | $R_{THacde}$ | 0 |
| $R_{THad}$ | -0.01 | $R_{THacd}$ | -0.06 | $R_{THbcde}$ | -0.13 |
| $R_{THae}$ | 0.53 | $R_{THace}$ | -0.05 | $R_{THabcde}$ | -0.11 |
| $R_{THbc}$ | -0.21 | $R_{THade}$ | -0.07 | | |

Fig. 4.10 witnesses that the $R_{TH}$ sensitivity to the thickness of semiconductor layers is more marked since they conduct the downward heat directed to the sink. Increasing the thickness of the $In_{0.5}Ga_{0.5}As$ layer from 50 nm (reference) to 70 nm leads to an $R_{TH}$ growth of 1.3% to be compared to 0.3% obtained for the WB case. It is worth noting that the thermal behavior is well mitigated by a thicker M2 (even more than in WB: increasing $t_{M2}$ from 2.1 µm to 3.5 µm leads to a -5.5% reduction in $R_{TH}$ instead of -2.9%), whereas the thickness of M1 has only a minor impact, as witnessed by coefficients $R_{THe}$=-19.95 K/W and $R_{THd}$=-0.42 K/W, respectively; in particular, the sensitivity to $t_{M1}$ is quite different from WB, for which $R_{THd}$=-20.76 K/W. In order to shed a light on this aspect, it must be recalled that in the FC technology M1 and M2 conduct the heat from the source to the sink; at a first glance, it could be believed that making them thicker would increase the thermal resistance due to the longer path to the sink (*heating effect*); on the other hand, the resulting bigger volume of such layers would also enhance the lateral spreading of the incoming heat (*cooling effect*). To identify

the dominating effect, it must be noted that the horizontal size of the emitter M1 is ~430 μm$^2$ (comparable to that of the heat source), while emitter M2 is made almost 100 times larger (~404×10$^2$ μm$^2$) to further favor the heat spreading. As a result, (i) if M1 is made thicker, the heating and cooling effects almost completely counteract each other: it is found that the marginally prevailing effect is determined by the combination of values for the other 4 DOE-examined parameters; (ii) if instead M2 is thicker, the cooling effect dominates since the heat emerging from the active device is free to laterally spread in a much bigger volume. This analysis is schematically shown in Fig. 4.11. As the best combination (thin emitter layers, thick M2) is chosen, a -9.4% $R_{TH}$ reduction is achieved (only -5.4% was evaluated for the WB assembly), whereas the worst combination (thick emitter layers, thin M2) leads to an $R_{TH}$ growth of about 2.5% (0.5% in WB). These results indicate that extra consideration should be given to the material design depending on the assembly technology to be used.

Overwhelming evidence of the accuracy of (4.1) is also given by Fig. 4.10, in which the DOE expansion is successfully compared to the ~100 FEM *validation* results computed *a posteriori*.[5]




[5] A slight DOE inaccuracy is observed for the $R_{TH}$ sensitivity to $t_{M1}$; this is ascribed to the fact that DOE might not properly work when the influence of a specific parameter depends on the combination of values of the other parameters.

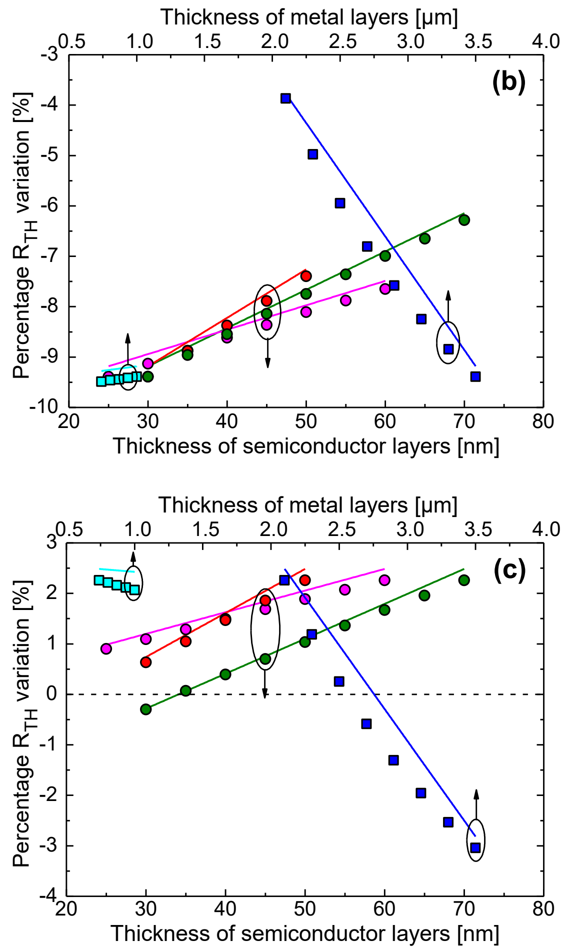



**Fig. 4.10** FC technology: percentage $R_{TH}$ variation with respect to $R_{TH,ref}$, as determined by modifying only one parameter, and keeping the others equal to (a) the reference values, or equal to the values corresponding to (b) thin emitter layers, thick metal layers, and (c) thick emitter layers, thin metal layers. Expansion (4.1) (solid lines) with coefficients reported in Table 4.8 is compared to *validation* data (symbols).

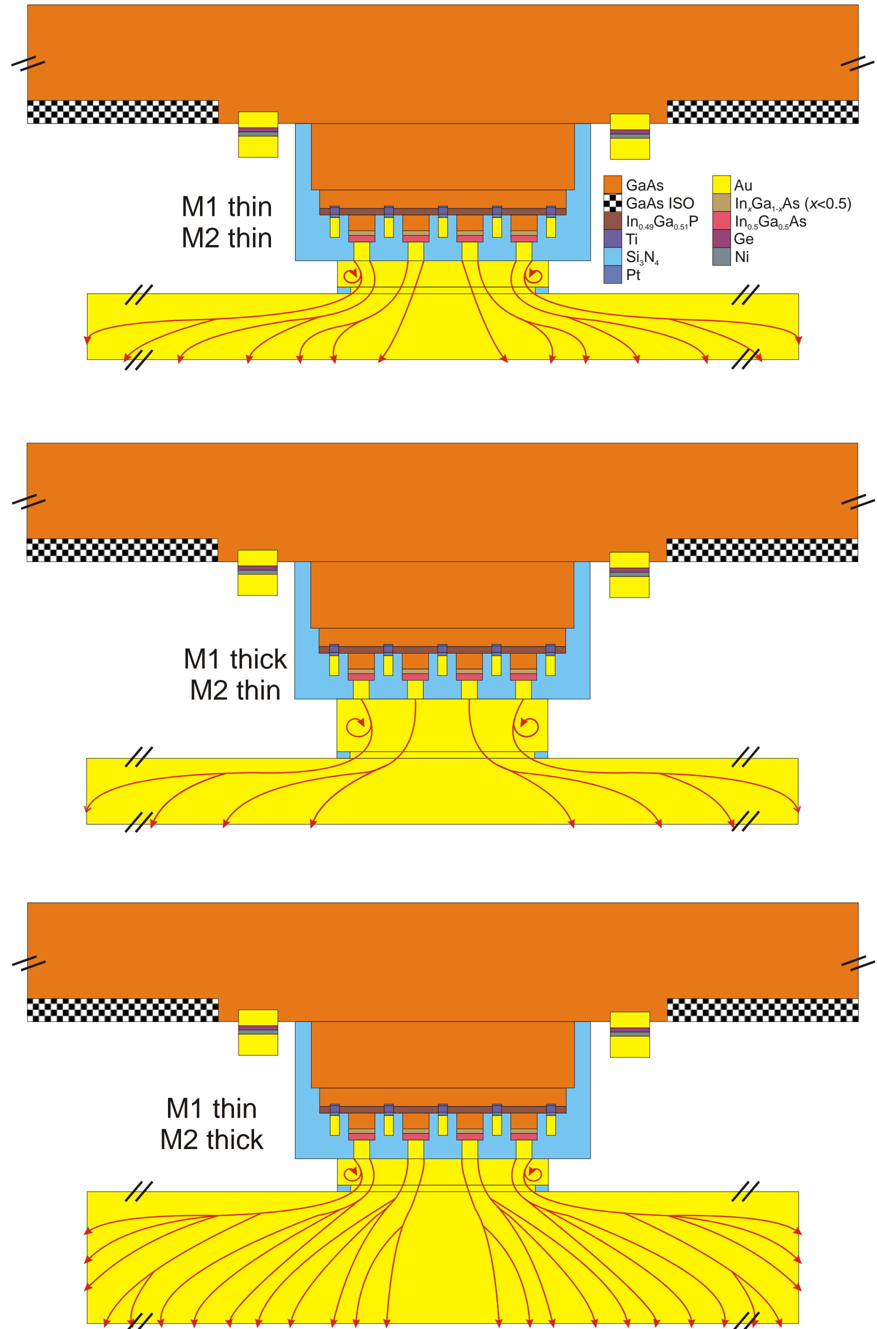



**Fig. 4.11** FC technology: DUT magnification (not to scale) illustrating the thermal impact of either a thicker M1 or a thicker M2 layer.

## 4.4 Dynamic thermal coupling

The FEM approach for dynamic thermal simulations (explained in Subsection 3.1.2) was exploited to analyze the thermal coupling between devices in circuits for RF PAs shown in Subsection 2.1.3. The following results involve (i) the thermal coupling between devices as a function of the distance and the interconnection styles and (ii) the extraction of Foster-like TFBs to perform dynamic ET simulations. The main heat transfer mechanisms are investigated to support the obtained results.

### 4.4.1 Analysis of the mutual-heating effects

Several analyses were performed to evaluate and explain the dynamic thermal coupling between transistors #1 and #2 (depicted in Fig. 2.7) for various technology and layout configurations. More specifically, the following emitter connection strategies were examined (see Fig. 4.12):

A. 2.1-µm-thick TM Au layer on a 0.15-µm-thick $Si_3N_4$ layer.
B. 3.5-µm-thick TM Au layer on a 0.15-µm-thick $Si_3N_4$ layer.
C. 2.1-µm-thick TM Au layer on a 1.1-µm-thick BCB layer.
D. 3.5-µm-thick TM Au layer on a 1.1-µm-thick BCB layer.

For each of the above cases, 4 values of the spacing between #1 and #2, defined as the length *d* of the GaAs-ISO region (see Fig. 2), were considered; in particular, *d* was set to 3, 10, 20, and 100 µm (the latter case being used to emulate marginal thermal interaction). The PA corresponding to case A with *d*=10 µm was chosen as a reference (see Fig. 2.7).

The transient thermal coupling was analyzed in terms of *steady-state value* of the thermal response (i.e., the mutual $R_{TH}$) and *thermal time constant* (i.e., the time needed for the thermal response to reach 1-1/e=63.2% of the steady-state value [Oza14]).

The mutual thermal impedances $Z_{TH21}$ simulated by varying *d* and connection style are reported in Fig. 4.13. The RF device dissipates power, and the temperature is sensed over the base-emitter junction of the bias device.

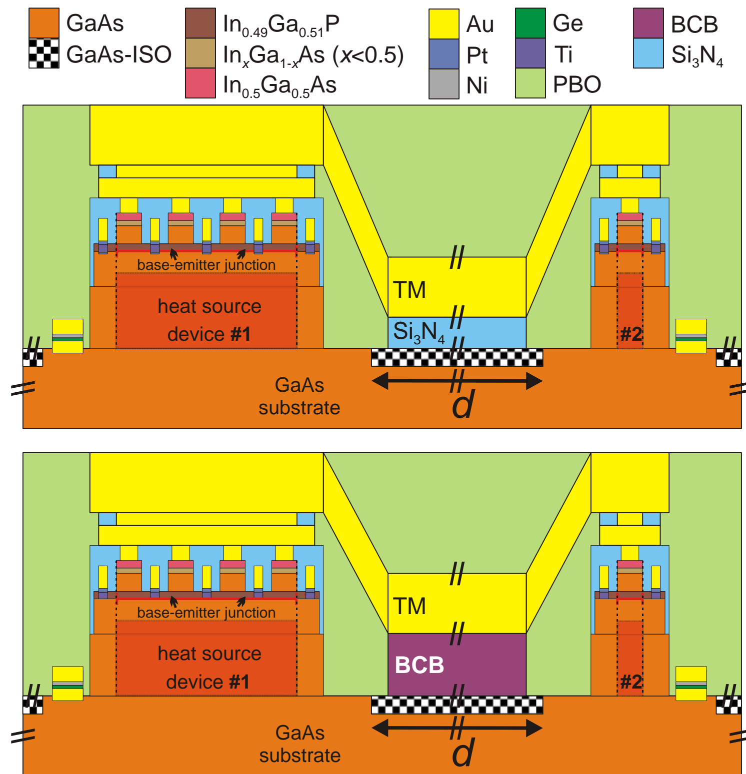



**Fig. 4.12** Schematic 2-D representation of the power RF (#1, left) and bias (#2, right) HBTs of the PA, illustrating the emitter connection strategies and the spacing *d* between devices.

The corresponding mutual thermal resistances $R_{TH21}$ and time constants $\tau_{TH21}$ are reported in Table 4.11. The following observations can be made.

- For a given spacing *d* (regardless of its value), the connection style D ensures the tightest coupling (i.e., the best thermal interaction) between transistors #1 and #2 in terms of both highest $R_{TH21}$ and shortest $\tau_{TH21}$. This can be attributed to (i) the larger section of TM crossed by the heat flow (compared to A and C); (ii) the greater thickness and lower thermal conductivity of BCB with respect to $Si_3N_4$ that 'forces' the heat to flow to #2 through the Au TM, instead of spreading into the substrate (compared to A and B); (iii) the shorter path for the heat generated by #1 to reach #2 (compared to A and B).

- The worst coupling is obtained in case A, where the TM section is the smallest, the thin $Si_3N_4$ dielectric allows a perceptible heat injection into the substrate (shunt effect), and the path is the longest.
- $R_{TH21}$ appreciably reduces from case D to A for a given *d* (more markedly in percentage for a longer *d*), whereas the time constant increases at a slower pace (it is weakly sensitive to the connection style for $d \leq 20$ µm). This is confirmed by a first-order 1-D analysis of the heat propagation, according to which $\tau_{TH}$ primarily depends on the distance between devices and on the TM parameters.
- Comparing cases B and C for a given distance *d*, it is found that B leads to a slightly tighter thermal interaction in terms of $R_{TH21}$, indicating that the thicker TM prevails over shorter path and shunt. These effects tend to balance for very high *d* where the heat shunt plays a major role (only a small portion of the heat reaches HBT #2).
- For all the connection approaches, the thermal coupling improves for decreased spacing. For instance, in case A, $R_{TH21}$ is shown to increase from 110.84 K/W for *d*=20 µm to 188.19 K/W (+70%) for *d*=3 µm. Meanwhile, $\tau_{TH21}$ reduces more slowly, i.e., from 33 to 20 µs (-39.4%).

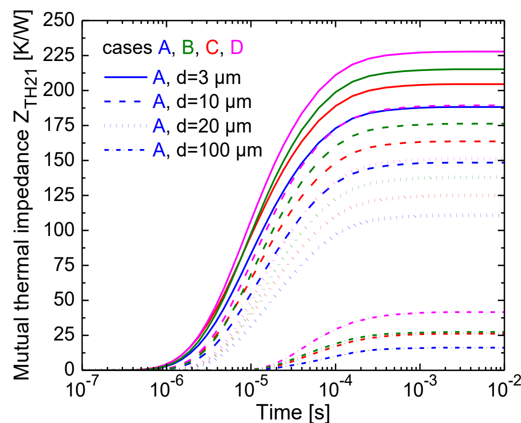



**Fig. 4.13** Mutual thermal impedance $Z_{TH21}$ vs. time as a function of emitter connection (shunting) style for spacing *d* equal to 3, 10, 20, and 100µm.

**TABLE 4.11** PARAMETERS OF THE MUTUAL THERMAL IMPEDANCE $Z_{TH21}$

| connection style | *d* [μm] | $R_{TH21}$ [K/W] | $\tau_{TH21}$ [μs] |
|---|---|---|---|
| A | 3 | 188.19 | 19.99 |
| B | | 215.20 | 18.93 |
| C | | 204.53 | 18.37 |
| D | | 227.84 | 17.98 |
| A | 10 | 148.48 | 25.07 |
| B | | 176.32 | 23.00 |
| C | | 163.69 | 23.14 |
| D | | 189.31 | 21.94 |
| A | 20 | 110.84 | 32.99 |
| B | | 138.00 | 28.98 |
| C | | 125.02 | 30.22 |
| D | | 151.32 | 27.50 |
| A | 100 | 16.21 | 104.22 |
| B | | 27.48 | 82.51 |
| C | | 26.17 | 93.00 |
| D | | 41.67 | 80.03 |

### 4.4.2 Equivalent thermal networks for ET simulations

Accurate and fast dynamic ET simulations of the PA – as well as of more complex circuits – can be enabled in ADS by resorting to the following procedure:

The 2×2 matrix of SH and mutual $Z_{TH}$s is determined by COMSOL in a *preprocessing stage* as discussed in Section 3.1; this computation needs to be performed *only once* for a given PA structure.

An equivalent thermal network composed by resistances, capacitances, and controlled sources is constructed to act as a TFB: the TFB is devised to receive the powers dissipated by the transistors, and calculate the junction temperatures to feed to the thermal nodes of the

device models. The TFB can be built by resorting to the simple Foster topology (Fig. 4.14), the RC pairs of which can be identified with standard techniques, such as that presented by Jakopović *et al.* [Jak90]. As shown in Section 3.2, a valuable alternative is to invoke the *in-house* tool FANTASTIC [Cod14] for the *fully automatic* construction of a *dynamic compact thermal model* (DCTM) and of the corresponding TFB from the COMSOL grid.

Then the internal 1-pole or 2-pole equivalent RC networks of the transistor models must be deactivated and simple additional components have to be added for the evaluation of the $P_{DS}$.

Lastly, the 'external' TFB has to be wired to the circuit branches carrying the powers and to the thermal nodes.

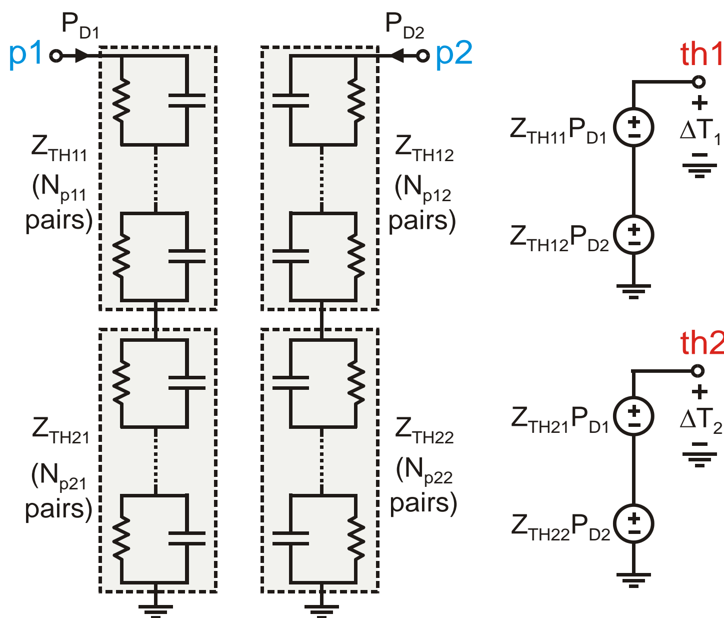



**Fig. 4.14** Equivalent RC network in a Foster topology for 2 heat sources.

Two approaches can be used to account for nonlinear thermal effects induced by very high temperatures: (1) a simple, yet approximate, method relies on the Kirchhoff's transformation [Car59] (see Eq. (6.7)), which can be implemented by a controlled source; (2) a more accurate solution involves the adoption of an advanced version of FANTASTIC suited to automatically generate a nonlinear DCTM and

the related equivalent network (comprising more components than the linear counterpart) [Cod16].

The standard approach from Jakopović and coworkers [Jak90] was used to identify the RC pairs of the Foster topology in Fig. 4.14 for the reference PA. The comparison between the COMSOL results and those obtained from the network is shown in Fig. 4.15. The choice of $N_{p11}$=9, $N_{p22}$=10 pairs for the SH impedances and $N_{p12}$=$N_{p21}$=6 for the mutual ones allowed obtaining results virtually coinciding with FEM data. It is worth noting that also other *in-house* heuristic identification approaches could in principle be used to slightly reduce the number of pairs without loss of accuracy.

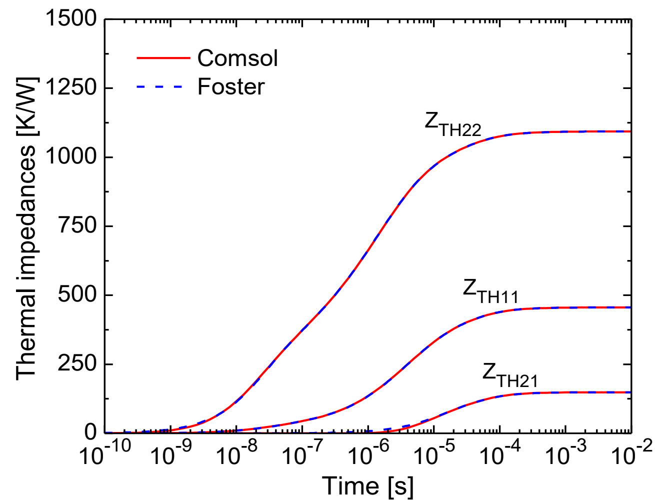



**Fig. 4.15** Thermal impedances $Z_{TH11}$, $Z_{TH21}$ ($\approx Z_{TH12}$), $Z_{TH22}$ of the reference PA: comparison between COMSOL results (red curves) and those computed by the Foster equivalent circuit in Fig. 4.14 with RC pairs optimized according to [Jak90] (dashed blue). The $Z_{TH21}$ Foster network suffers from little inaccuracy for short times (<5 μs) due to the gradual propagation of the heat coming from #1 through #2.

# Chapter 5

# Thermal analyses of power systems

In this Chapter, results of the purely-thermal analyses of PMs and PCB structures are shown. More specifically, Section 5.1 is aimed to compare the thermal behavior of SiC-based SSC and DSC PM technologies, the features of which were drawn in Subsection 2.2.1; the results focus on the heat spreading effects in both PMs, with particular emphasis on the role of the BCs applied on the CSs. The GaN-based PCB structures shown in Subsection 2.2.2 are then considered. First, analytical models to predict the $R_{TH}$s of TVs and HSK (both composing the PCB structure) are illustrated; then, a validation of the model accuracy is carried out by means of the tool shown in Section 3.1. Further simulations were performed to investigate the impact of (i) graphene layers in the solder process and (ii) materials for the HSK electrical insulation on the thermal behavior of devices on PCB.

## 5.1 Power modules technologies: SSC vs DSC

The thermal performances of SSC and DSC PMs are methodically compared in terms of SH and MH $R_{TH}$ of the individual transistors. The study is carried out by simulating extremely detailed structures in a broad range of convective BCs applied on the external CSs. An additional analysis is performed to compare AlN and $Si_3N_4$ as DBC ceramic materials in terms of thermal behavior. Following the simulation approach described in Section 3.1, the matrices containing SH and MH $R_{TH}$ (denoted as $R_{TH,SH}$ and $R_{TH,MH}$, respectively) were determined for the SSC and DSC PMs described in Subsection 2.2.1 by varying the BCs applied on the CSs. Since the ET effects affecting devices are more pronounced as their $R_{TH}$ grows, the maximum values of $R_{TH,SH}$ ($R_{THmax,SH}$) and $R_{TH,MH}$ ($R_{THmax,MH}$) were evaluated for each $h$ value. Results are shown in Fig. 5.1.

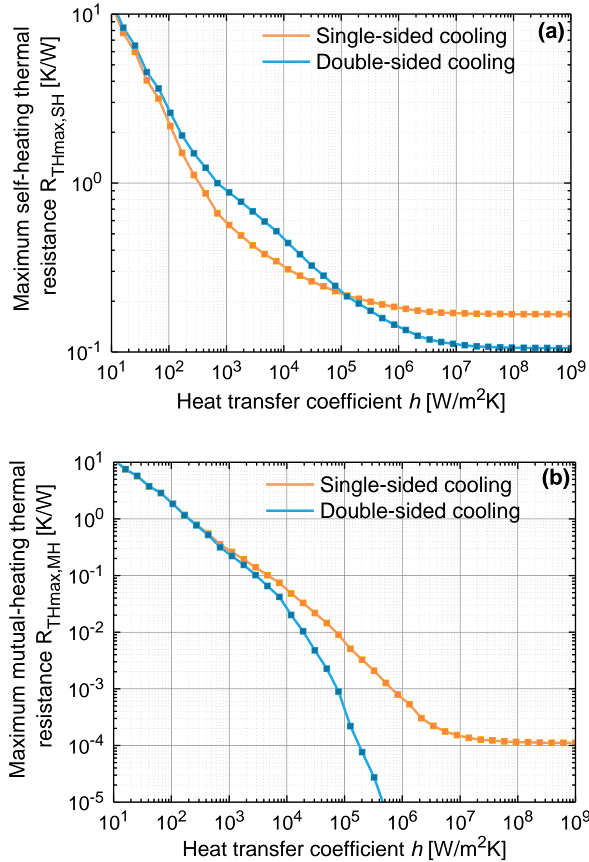



**Fig. 5.1** (a) $R_{THmax,SH}$ and (b) $R_{THmax,MH}$ vs. $h$ evaluated by FEM simulations; SSC data (orange lines) are compared with DSC results (blue).

Good BCs ($h>10^6$ W/m$^2$K) justify the choice of the DSC technology, since in this case a marked reduction in $R_{THmax,SH}$ (-23%) is obtained with respect to the SSC solution, and MH effects are negligible (Fig. 5.1b). On the other hand, Fig. 5.1a shows the occurrence of a trend reversal point (TRP) for $R_{THmax,SH}$ at $h\approx10^5$ W/m$^2$K, that is, the SSC technology has to be preferred for poorly-cooling BCs. This behavior can be explained as follows. While the SSC structure is composed by a thick and wide Cu baseplate that favors the heat spreading, the DSC PM enjoys two CSs closer to the heat sources (see Fig. 2.8). The balance between these two features is represented by the TRP, which separates the low convection region ($h<10^5$ W/m$^2$K), where the beneficial effect of the SSC baseplate prevails, from the high convection one

($h$>$10^5$ W/m$^2$K), where the couple of CSs of the DSC PM dominates. Figs. 5.2 and 5.3 support the comprehension of these phenomena by showing modules and directions of the heat flux vector (obtained by FEM simulations) in SSC and DSC PMs, respectively.

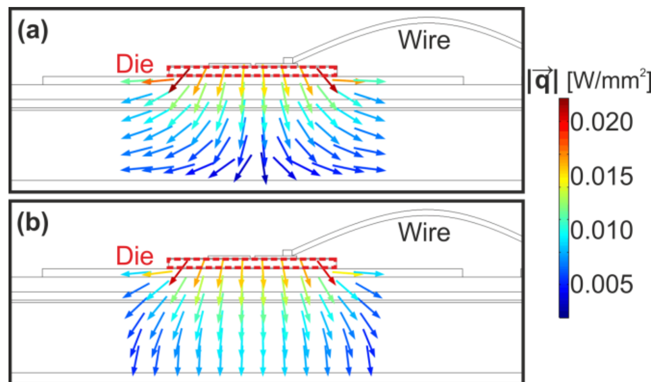



**Fig. 5.2** Heat flux maps showing the spreading effect in SSC structure for BCs corresponding to (a) h=$10^1$ W/m$^2$K and (b) h=$10^8$ W/m$^2$K. The die (containing the heat source region) is highlighted by a red box.

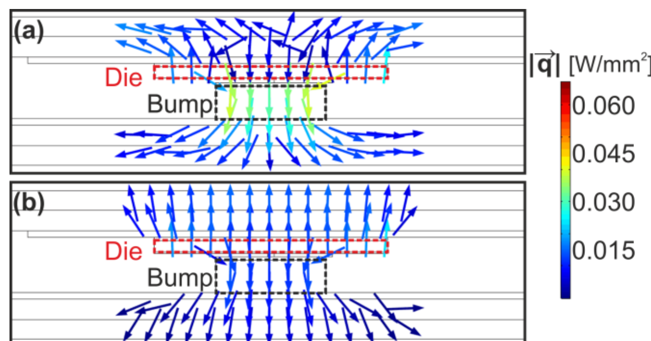



**Fig. 5.3** Heat flux maps obtained by simulations showing the spreading effect in DSC structure for BCs dictated by (a) h=$10^1$ W/m$^2$K and (b) h=$10^8$ W/m$^2$K. The die (containing the heat source region) is highlighted by a red box. A black box surrounds the vertical interconnection (bump) allowing the heat to flow through both CSs.

In both structures, low $h$ values encourage the heat spreading mechanism: in order to keep the outgoing heat flux unchanged, a larger area of the CSs needs to be exploited. The SSC baseplate allows obtaining $R_{TH,SH}$ values lower than the DSC counterpart by virtue of the enhanced heat spreading, which also gives rise to a more pronounced

MH between neighboring devices, i.e., to higher $R_{TH,MH}$ values. Instead, at high *h* values, a smaller portion of the CSs needs to be exploited to drain off the thermal power: the improved thermal exchange conditions lead to a significant heat spreading reduction; Figs. 5.2b and 5.3b show indeed that the heat flux in both SSC and DSC structures is much more vertical than that taking place at low *h* values (Figs. 5.2a and 5.3a). As a result, (i) a reduction in the $R_{TH,SH}$ and (ii) negligible MH effects are observed. It is worth noting that the $R_{TH,SH}$ saturates for both PM technologies as very high *h* values (i.e., almost-isothermal BCs) are reached. In this scenario, a further improvement of the cooling system might have a negative impact on the design cost, while resulting in no gain on the PMs performances.

A second analysis was aimed to quantify the effect of ceramic layers on the $R_{TH,SH}$ in both PM technologies. Table 5.1 shows the $R_{THmax,SH}$ in SSC and DSC architectures obtained with the target to compare $Si_3N_4$ and AlN as the DBC ceramic materials. The heat spreading mechanism in $Si_3N_4$-based DBCs leads to a TRP similar to that seen in AlN. The AlN advantages are almost negligible at low *h* values, whereas a significant $R_{THmax,SH}$ reduction (up to -70% in DSC) is observed for higher *h*.

**TABLE 5.1** $R_{THMAX,SH}$ FOR $Si_3N_4$- AND ALN-BASED DBCS IN SSC AND DSC PMS

| **$R_{THmax,SH}$ [K/W]** | **SSC** | | **DSC** | |
|---|---|---|---|---|
| ***h* [W/m²K]** | $10^2$ | $10^8$ | $10^2$ | $10^8$ |
| **$Si_3N_4$** | 1.75 | 0.418 | 2.38 | 0.354 |
| **AlN** | 1.49 (-14.9%) | 0.167 (-60.0%) | 1.90 (-20.2%) | 0.105 (-70.3%) |

The results can be physically explained as follows: the $R_{TH,SH}$ is obtained by a series of conductive and convective contributions, which represent the heat flux across the DBCs (and the baseplate in SSC PMs) and the thermal exchange through the CSs, respectively. As the BCs are bad (good), the convective (conductive) thermal resistance prevails over the other one, thus mitigating (enhancing) the advantages of the high-conductive DBCs in AlN technology. Moreover, the DSC $R_{TH,SH}$

is more sensitive to the conductive contribution (with respect to the SSC one) because of the two DBCs. As a consequence, using AlN – regardless of the BCs – implies a more significant $R_{TH,SH}$ reduction in DSC PMs.

The above analysis leads to the following observation: due to the high AlN production cost [Gho10], designers should realize AlN-based DBCs (for both SSC and DSC technologies) only when an efficient PM cooling system is ensured.

## 5.2 GaN-based PCB

This Section introduces the thermal modeling of TVs and HSK composing the PCB design. The models are aimed at a quick estimation of the $R_{TH}$s introduced by such structures; the geometrical features and the material properties are considered as input for the models predictions. To validate the accuracy of the proposed models, extremely detailed FEM simulations were performed following the procedure described in Section 3.1; the analyses aimed to validate the analytical models required simulations of the 3-D structures represented in Fig. 5.4a; Fig. 5.4b shows the high level of detail reached by means of the aforementioned routine.

The use of graphene layers in the solder process was also investigated; FEM simulation results are shown in Subsection 5.2.4, where the thermal advantages ensured by this alternative solder technique are reported.

HSK electrical insulating techniques usually introduce a further contribution on the overall $R_{TH}$; different technologies were studied and compared, the results of which are shown in Subsection 5.2.5.

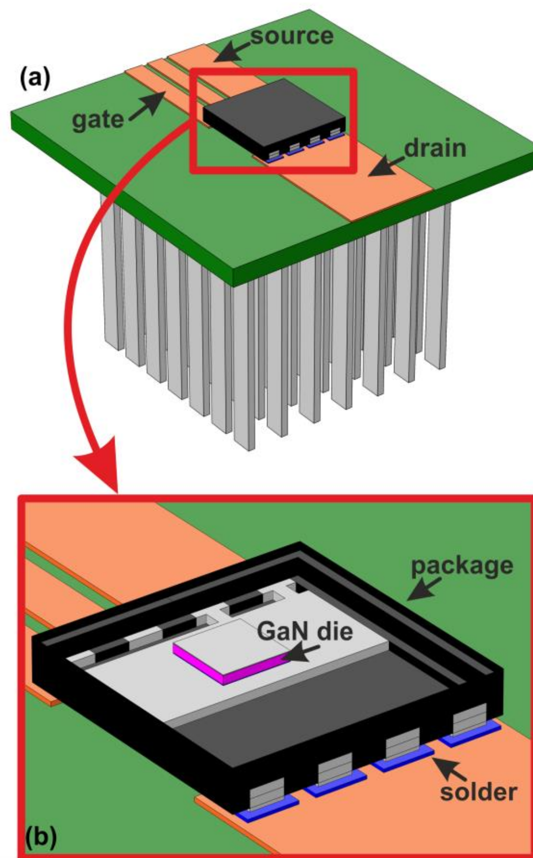



**Fig. 5.4** (a) 3-D representation of the domain in the COMSOL Multiphysics environment and (b) magnification on the package area containing the GaN die.

### 5.2.1 Modeling of thermal vias and heat-sinks

First, a brief description of the TVs technology and geometry is introduced for single-layer PCBs; the typical TVs structure is schematically represented in Fig. 5.5a. The technology process allows (i) creating holes in the FR-4 PCB, (ii) partially (or completely) filling them with Cu, (iii) covering the top and bottom surfaces with Cu thermal plates (TPs). The TV details are depicted in Fig. 5.5b. The process to realize TVs is characterized by (i) the radius *r* of the holes and (ii) the plating *p*, namely, the width of the Cu layer filling the

internal surface of the hole. The PCB designers choose the number of vias ($N_{TV}$) and their position on the TP.

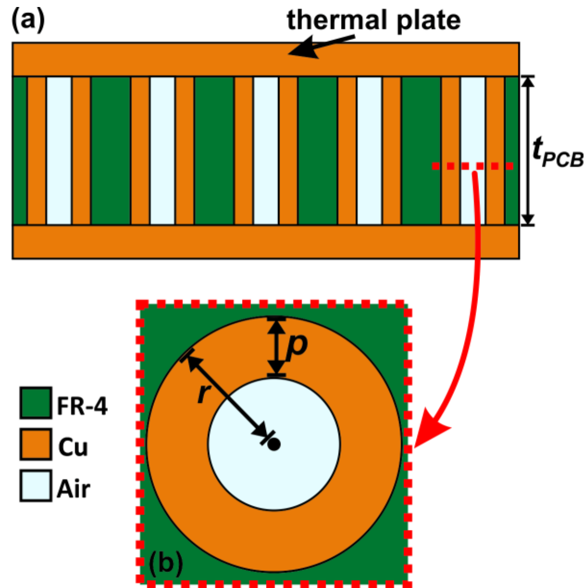



**Fig. 5.5** (a) Cross section of the TVs structure and (b) schematic representation of a TV highlighting its radius and plating.

Here an analytical scalable model is proposed for the thermal resistance ($R_{TH,TV}$) of the TVs, i.e., the resistance hindering the heat flow between the two TPs. The model accounts for the material and geometry parameters and allows obtaining a quick and simple estimation of the $R_{TH,TV}$. The model relies on the assumption of isothermal TPs, which can be justified by (i) the high Cu thermal conductivity and (ii) the high distance from the heat source located in the GaN die inside the device package. Since each TP was assumed as isothermal, the $R_{TH,TV}$ is composed by the parallel of three contributions: the conductive heat flow through the Cu, the FR-4, and the still air volume (Fig. 5.6); it follows that:

$$R_{TH,TV} = R_{THtot,Cu} \, // \, R_{THtot,FR-4} \, // \, R_{THtot,Air} \tag{5.1}$$

Based on geometrical arguments, the terms in (5.1) can be expressed as

$$R_{THtot,Cu} = \frac{t_{PCB}}{k_{Cu}} \cdot \frac{1}{N_{TV}\pi\left[r^2 - (r-p)^2\right]}$$
$$R_{THtot,FR-4} = \frac{t_{PCB}}{k_{FR-4}} \cdot \frac{1}{A_{TP} - \left(N_{TV}\pi r^2\right)} \qquad (5.2)$$
$$R_{THtot,Air} = \frac{t_{PCB}}{k_{Air}} \cdot \frac{1}{N_{TV}\pi (r-p)^2}$$

In (5.2), $k_{Cu}$, $k_{FR\text{-}4}$, and $k_{Air}$ indicate the thermal conductivities of the materials, $t_{PCB}$ is the board thickness, and $A_{TP}$ is the TP area. The main contribution in (5.2) is given by $R_{THtot,Cu}$, which is the smallest one because of the high $k_{Cu}$ value; $R_{THtot,FR-4}$ and $R_{THtot,Air}$ represent correction terms useful to improve the model accuracy in TVs designed with (i) small radii, (ii) small plating values, or (iii) small number of holes.

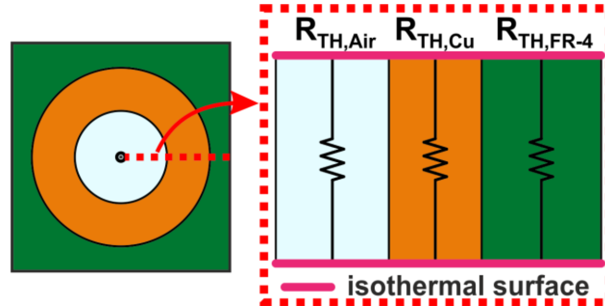



**Fig. 5.6** Schematic representation of thermal resistances composing the TVs model.

HSKs are usually realized with high thermal conductivity materials in order to drain off the heat by exploiting a larger thermal exchange surface. The analytical scalable model described below allows quantifying the $R_{TH}$ of the HSK ($R_{TH,HSK}$) when a fictitious heat source completely covers its top surface (Fig. 5.7a), which corresponds to the procedure commonly adopted to experimentally evaluate the $R_{TH,HSK}$ value provided in the datasheets. The model is suitable to describe HSKs with the following shape: a base – leaning on the surface

to be cooled – is in contact with several parallelepipedal fins favoring the convective heat flow.

The $R_{TH,HSK}$ is expressed through four $R_{TH}$s (Fig. 5.7a) describing the heat flux in the structure. Such resistances are obtained as a function of geometry, thermal conductivity of the materials, and convective BCs; the thermal power is assumed to be evenly dissipated over the heat source. The $R_{TH,HSK}$ expression is given by

$$R_{TH,HSK} = \left[R_{TH,Bcond} + (R_{TH,Uconv} \,//\, R_{THtot,F})\right] // \, R_{TH,Bconv} = \\ = \left[ R_{TH,Bcond} + (R_{TH,Uconv} \,//\, \frac{R_{TH,F}}{N_{Fin}}) \right] // \, R_{TH,Bconv} \quad (5.3)$$

where

$$\begin{aligned} R_{TH,Bcond} &= \frac{t_{Base}}{k_{HS} \cdot A_{Base}} \\ R_{TH,Bconv} &= \frac{1}{h \cdot A_{BaseExt}} \\ R_{TH,Uconv} &= \frac{1}{h \cdot A_{Unf}} = \frac{1}{h \cdot \left(A_{Base} - N_{Fin} \cdot A_{Fin}\right)} \end{aligned} \quad (5.4)$$

In (5.3), $R_{TH,Bcond}$ represents the conductive heat flow through the HSK base; it is placed in series with the parallel of $R_{THtot,F}$ and $R_{TH,Uconv}$, which model the thermal resistance of all the fins in parallel (i.e., the one of a single fin $R_{TH,F}$ divided by the number of fins $N_{Fin}$) and the convective heat flow of the unfinned surface of the base, respectively. The resulting thermal resistance is placed in parallel with $R_{TH,Bconv}$, which schematizes the heat flowing by the lateral surfaces of the base. The equations in (5.3) describe how $R_{TH,Bcond}$, $R_{TH,Bconv}$, and $R_{TH,Uconv}$ are evaluated by geometrical considerations on the heat flow mechanism; $h$ is the heat transfer coefficient applied on the HSK external surfaces, $k_{HSK}$ is the thermal conductivity of the HSK material, while $A_{Base}$ and $A_{BaseExt}$ represent the areas of the base section and of the base lateral external surfaces, respectively; $A_{Unf}$ corresponds to the

unfinned area, i.e., the area of the base bottom surface exposed to the ambient. To obtain the $R_{TH,F}$ value, a distributed approach is adopted: the fin is divided into several identical blocks denoted as elementary fin volumes (EFVs). For the sake of clarity, Fig. 5.7b shows the $R_{TH,F}$ model when the proposed approach is applied to a case of 3 EFVs; the total thermal resistance of the single fin is given by

$$\begin{aligned} R_{TH,F} &= R_{TH,EFV1} = (R_{TH,EFV2} + R_{TH,Fcond}) \,//\, R_{TH,Fconv} \\ R_{TH,EFV2} &= (R_{TH,EFV3} + R_{TH,Fcond}) \,//\, R_{TH,Fconv} \\ R_{TH,EFV3} &= (R_{TH,FconvTip} + R_{TH,Fcond}) \,//\, R_{TH,Fconv} \end{aligned} \tag{5.5}$$

where

$$\begin{aligned} R_{TH,Fcond} &= \frac{\frac{L_{Fin}}{3}}{k_{HS} \cdot A_{Fin}} \\ R_{TH,Fconv} &= \frac{1}{h \cdot \frac{A_{FinExt}}{3}} \\ R_{TH,FconvTip} &= \frac{1}{h \cdot A_{Fin}} \end{aligned} \tag{5.6}$$

Following (5.5), both convection and conduction associated to the fin are taken into account: $R_{TH,Fcond}$ represents the conductive thermal resistance through the elementary volume of the fin, $R_{TH,Fconv}$ is the convective thermal resistance due to the EFV external surfaces, while $R_{TH,FconvTip}$ takes into account the convective heat flux through the fin tip. In (5.6), $L_{Fin}$ is the fin length, while $A_{Fin}$ and $A_{FinExt}$ are areas of the fin section and the fin lateral external surfaces (excluding the tip), respectively.

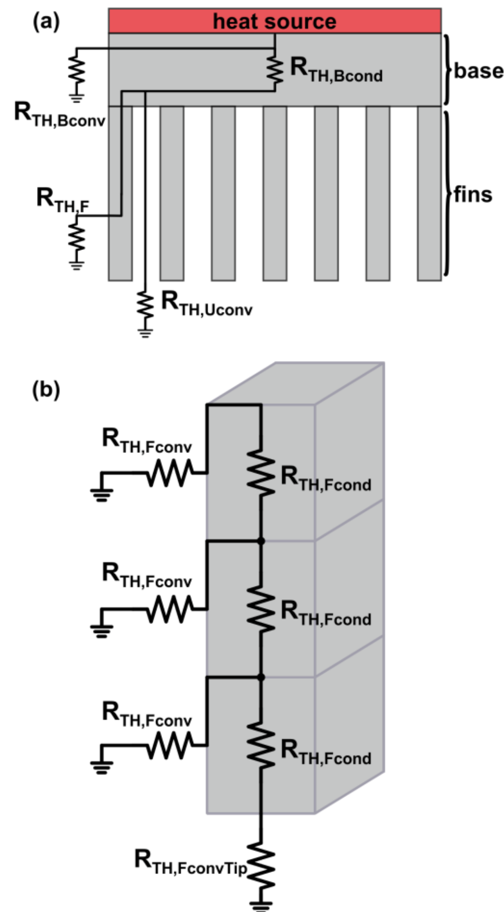



**Fig. 5.7** (a) Representation of thermal resistances of HSK model; (b) detail of the $R_{TH,F}$ features for a fin partitioned into 3 EFVs.

It is worth noting that $R_{TH,F}$ varies with the EFV number; for the HSKs analyzed in this thesis, the convergence value of $R_{TH,F}$ was reached by partitioning the fin into at least 50 EFVs. As schematically illustrated by (5.5), the $R_{TH,F}$ evaluation – regardless of the EFVs number – can be easily and quickly obtained with only a few lines of code.

## 5.2.2 Accuracy of thermal vias $R_{TH}$ model

A known value of $P_D$ is associated to the heat source, which corresponds to the GaN die located inside the package; convective BCs

were applied on the HSK external surfaces. The FEM simulations were run on a laptop PC equipped by a single i7-4720HQ CPU and an 8 GB RAM. For these structures, the average number of tetrahedra (DoFs) was $2.1\times10^5$ ($3.1\times10^5$) and the solution of each thermal problem was obtained in about 30 seconds.

The $R_{TH,TV}$ was evaluated by processing the temperature field as follows:

$$R_{TH,TV} = \frac{\overline{T_{TP,top}} - \overline{T_{TP,bot}}}{P_D} \tag{5.7}$$

where $\overline{T_{TP,top}}$ and $\overline{T_{TP,bot}}$ are the average values of the temperature field on the top and bottom TPs, respectively. The simulation results show a negligible temperature gradient on each TP, which confirms the accuracy of the assumption of isothermal TPs adopted in the model.

FEM thermal analyses were conducted on the topology shown in Fig. 5.4 with 6 reasonable PCB thermal designs: Fig. 5.8a (Fig. 5.8b) – realized by hiding all the structure volumes except those belonging the TVs – shows the design characterized by 40 (21) vias with $p$=0.1 mm and $r$=0.1 mm (0.3 mm) placed between two $3.2\times7$ mm$^2$-wide TPs.

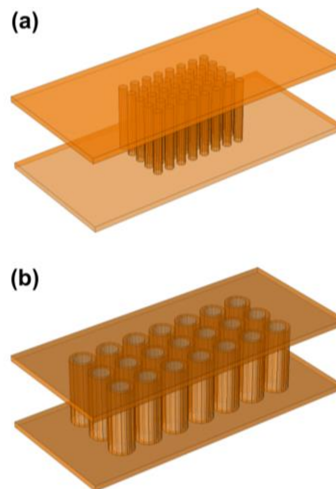



**Fig. 5.8** 3-D representation of TVs structures; (a) 40 0.1 mm-thick vias and (b) 21 0.3 mm-thick vias. The pictures were obtained by hiding the other volumes composing the whole structure.

The FEM simulations were performed for all designs. The results of the comparison between the TVs model and FEM simulations are shown in Fig. 5.9; the model predictions of $R_{TH,TV}$ vs. $N_{TV}$ are plotted for 3 vias radii (0.1, 0.2, and 0.3 mm) and compared with FEM data. Increasing the $N_{TV}$ value, the model allows quantifying the $R_{TH,TV}$ reduction, which is more pronounced with high radius values. A good agreement was observed: the mismatch in terms of $R_{TH,TV}$ was averaged on the 6 TVs designs and it turns out to be 7.5%, while the maximum (minimum) discrepancy of 15.8% (1.1%) was obtained in structures with 40 (21) vias and $r$=0.2 mm (0.3 mm).

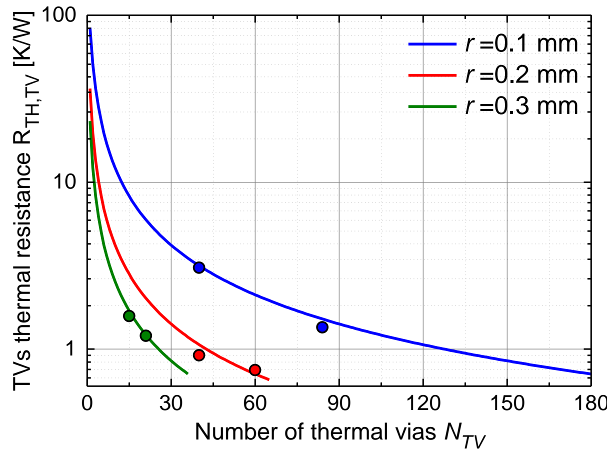



**Fig. 5.9** $R_{TH,TV}$ vs. $N_{TV}$ for different via sizes and p=0.1 mm; solid lines are referred to the model, whereas dots are obtained by 3-D FEM analyses.

### 5.2.3 Accuracy of heat-sink $R_{TH}$ model

Individual 3-D HSK structures were built to validate the model accuracy and the thermal problem was set up as follows: the $P_D$ was set on the HSK top surface while a convective BC was associated to all the external surfaces (except the top one, defined as adiabatic) composing the structure. The mean numbers of tetrahedra and the DoFs were about $2\times10^5$ and $3\times10^5$, respectively; the simulation runtime was approximately 20 seconds on the laptop PC previously mentioned. The $R_{TH,HSK}$ was calculated as

$$R_{TH,HSK} = \frac{\overline{T_{HSK,top}} - T_{amb}}{P_D} \tag{5.8}$$

where $\overline{T_{HSK,top}}$ is the average value of the temperature field on the top HSK surface, while $T_{amb}$ is the ambient temperature.

As far as the HSK model is concerned, two commercial HSKs geometries were analyzed to test its accuracy. Their shape and features (described in Fig. 5.10) are quite different in order to perform a high-spread investigation: the one described in Fig. 5.10a – corresponding to the HSK used in the TVs analyses – is commonly aimed to cool down single devices, while the HSK in Fig. 5.10b is usually designed as a cooling solution for the whole PCB.

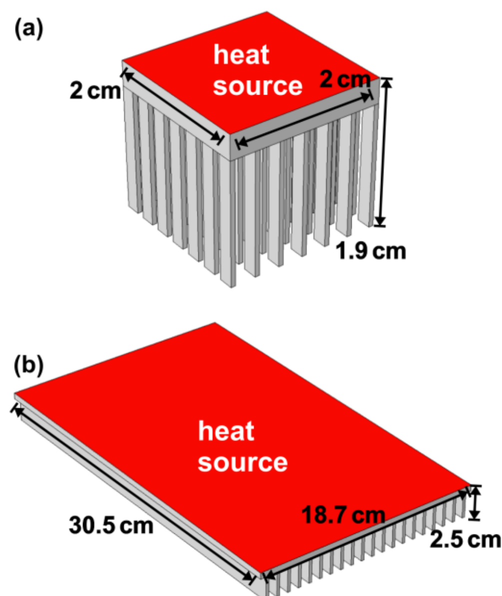



**Fig. 5.10** 3-D representation of (a) square base HSK with 49 fins and (b) rectangular base HSK with 20 fins; the physical HSK dimensions are shown in the picture, while the boundary heat source is highlighted in red.

Fig. 5.11a (Fig. 5.11b) shows the $R_{TH,HSK}$ vs. heat transfer coefficient $h$ for the HSK shown in Fig. 5.10a (5.10b). The model predictions were verified by means of a comparison with FEM data. Several simulations were run for both HSK structures and the $R_{TH,HSK}$s

were evaluated by applying (5.8). The analyses were carried out considering a wide range of heat transfer coefficients and a few values for the thermal conductivity of the material composing the HSKs. It was found that the model ensures a good match with numerical results: for medium and high $k_{HSK}$ values, the model predicts the $R_{TH,HSK}$s with an error <1%. To prove the accuracy and scalability of the model, simulations on a fictious HSK with very low thermal conductivity ($k_{HSK}$=100 W/mK) were carried out; a maximum disagreement of 2.2% was obtained for the HSK shown in Fig. 5.10a.

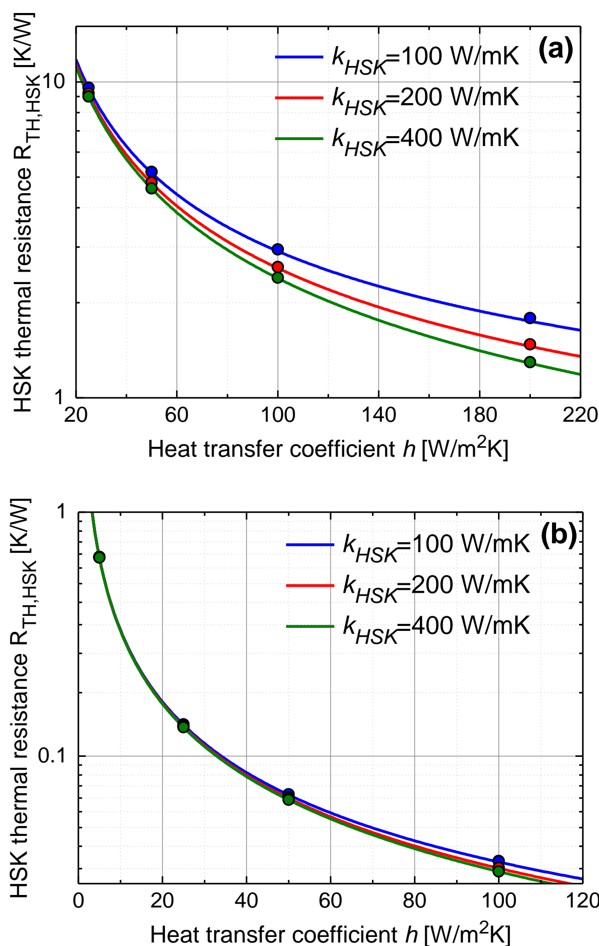



**Fig. 5.11** $R_{TH,HS}$ vs. $h$ in (a) square base and (b) rectangular base HSKs: solid lines are referred to the proposed HSK model, while dots are obtained by 3-D FEM simulations.

### 5.2.4 Graphene in the solder process

Novel materials, such as graphene foams – a picture of which is shown in Fig. 5.12 – could be exploited by introducing them in the solder process to enhance the heat disposal. Table 3.4 shows the thermal conductivity of the graphene layer used to realize the thermal contact between device and PCB TVs; the value was chosen as a reasonable average in a wide range [Wan87]. 3-D simulations were performed to quantify the improvement offered by this layer on the thermal resistance. In order to build a realistic structure including the graphene porosity, the thermal contact was composed by 50% of graphene and 50% of SnAg solder (as depicted in Fig. 5.13).

**Fig. 5.12** Example of new commercial graphene foams produced by Graphene Laboratories INC.

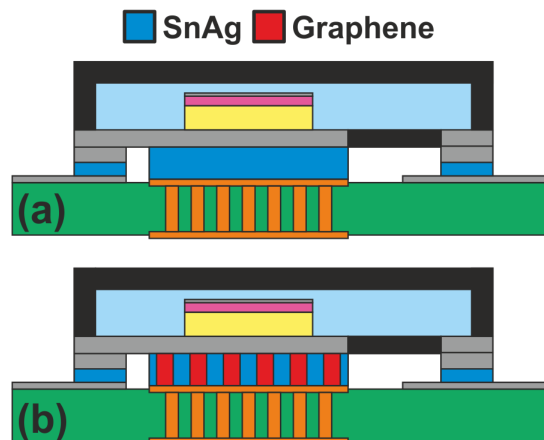



**Fig. 5.13** Details of contact between die and TVs; schematic cross section (a) without and (b) with graphene thermal contact.

Simulations were carried out for the PCB structure in the case of 21 Cu TVs with a radius of 0.3 mm placed in contact on a thermochuck; the junction-to-ambient thermal resistance ($R_{THj\text{-}a}$) was evaluated in structures with and without the graphene thermal contact. Table 5.2 shows the simulation results.

**TABLE 5.2** EFFECT OF GRAPHENE THERMAL CONTACT ON $R_{TH}$ JUNCTION TO AMBIENT FOR STRUCTURE WITH #21 TVS AND R=0.3 MM ON THERMOCHUCK

| | **$R_{THj\text{-}a}$ [K/W]** |
|---|---|
| **3-D simulation without graphene** | 5.08 |
| **3-D simulation with graphene** | 4.87 |

The effect of graphene thermal contact was also analyzed in structures with 21 TVs including the HSK effect. As result of interest, the $R_{TH}$s composing the whole $R_{THj\text{-}a}$ were evaluated exploiting the simulator facilities (Fig 5.14).

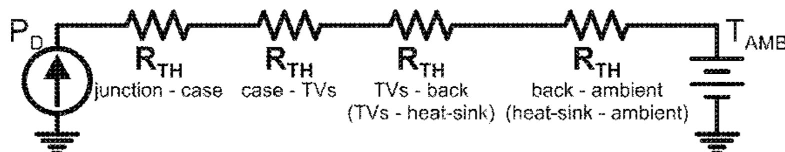



**Fig. 5.14** Details of the $R_{TH}$s composing the $R_{TH}$ junction to ambient.

The results are summarized in Table 5.3 in order to compare the domains with and without graphene layer.

Using graphene, an improvement of the $R_{THj\text{-}a}$ was observed, which can be ascribed to the reduction of the $R_{TH}$ case to back (case to HSK), obtained by the series of the case to TVs and TVs to back (TVs to HSK) ones. So, the presence of graphene thermal contact leads to (i) a reduction of the thermal stress of the solder connecting the case to the TVs and (ii) an improvement of the TVs behavior because of the heat spreading action favored by the high thermal conductivity of graphene.

**TABLE 5.3** EFFECT OF GRAPHENE THERMAL CONTACT ON $R_{TH}$ JUNCTION TO AMBIENT FOR STRUCTURE WITH #21 TVS AND R=0.3 MM

| **Structure on thermochuck** | | |
|---|---|---|
| **$R_{TH}$ [K/W]** | **Without graphene** | **With graphene** |
| **junction - case** | 0.60 | 0.59 |
| **case - TVs** | 0.33 | 0.18 |
| **TVs - back** | 1.21 | 1.14 |
| **back - ambient** | 2.94 | 2.96 |
| **junction - ambient** | 5.08 | 4.87 |
| **Structure on heat-sink** | | |
| **$R_{TH}$ [K/W]** | **Without graphene** | **With graphene** |
| **junction - case** | 0.60 | 0.59 |
| **case - TVs** | 0.33 | 0.18 |
| **TVs - HSK** | 1.23 | 1.17 |
| **HSK - ambient** | 12.19 | 12.20 |
| **junction - ambient** | 14.35 | 14.14 |

### 5.2.5 Impact of the heat-sink electrical insulator

In order to obtain an efficient cooling action, the HSKs are usually realized by thermally-conductive materials (e.g., aluminum and copper); as side effects, these materials are characterized by low values of resistivity that might drive to a biased HSK structure if an electrical insulator material is not placed in between the HSK and the PCB. Such layers are usually defined as thermal interface materials (TIMs), as shown in Fig. 2.11. This Section probes into their impact on the overall $R_{TH}$. The typical insulating foil (previously considered) allows a simple connection between the HSK and the PCB by virtue of its adhesive properties; unfortunately, it is characterized by a low value of thermal conductivity – as can be seen from Table 3.4 – leading to a high value of the HSK-to-ambient $R_{TH}$. Materials like $Si_3N_4$ and AlN enjoy higher values of thermal conductivity and, at the same time, a reasonable electrical insulation function; although their assembly process is more

complex than the one of insulating foils, the $R_{TH}$ reduction turns out to be considerable, thereby justifying their application. Results obtained by thermal simulations are shown in Table 5.4.

**TABLE 5.4** THERMAL RESISTANCES FOR DIFFERENT TIMS CONNECTING PCB AND HSK IN DOMAIN INCLUDING THE GRAPHENE THERMAL CONTACT

| $R_{THj-a}$ [K/W] | #21 TV r=0.3 mm | #60 TV r=0.2 mm |
|---|---|---|
| **insulating foil** | 14.14 | 13.31 |
| **$Si_3N_4$** | 7.94 | 7.34 |
| **AlN** | 7.56 | 6.99 |

Exploiting the $Si_3N_4$ as TIM, a $R_{TH}$ reduction of about -44% is observed for both the designs of TV. The higher thermal conductivity offered by AlN leads to the best improvement in thermal performance with a $R_{THj-a}$ reduction of about -47% with respect to the connection by insulating foil.

# Chapter 6

# Electrothermal simulations

In this Chapter, the ET behavior of RF HBTs and SiC-based PMs is investigated.

The analyses of RF transistors are performed to identify and quantify effects related to ET instabilities in test devices and practical arrays for handset PAs (see Subsection 2.1.2). Section 6.1 is organized as follows: first, an ET SPICE-compatible behavioral model of the individual HBT is described; the approach to perform ET simulations in SPICE-like environment is then shown; lastly, the simulation results are reported and explained.

The effect of technology fluctuations on SiC PMs is delineated in Section 6.2; here, the ET simulations are performed by making use of MOR-based TFBs to account for the power-temperature feedback.

## 6.1 Electrothermal effects in RF devices

### 6.1.1 HBT model

The collector current in forward active mode is given by [dAl16], [dAl18]

$$I_C = I_{CnoAV} + I_{AV} = M \cdot I_{CnoAV} = \\ = M \cdot \left(1 + \frac{V_{CB}}{V_{AF}}\right) \cdot \frac{1}{B_{HI}} \cdot A_E \cdot J_{S0} \cdot \exp\left(\frac{V_{BEj} + \phi \cdot \Delta T_j}{\eta \cdot V_{T0}}\right) \tag{6.1}$$

where $I_{CnoAV}$ is the current in the absence of impact-ionization (II) effects and $I_{AV}$ is the avalanche component.

In (6.1), $A_E$ [$\mu m^2$] is the emitter area; $J_{S0}$ [$A/\mu m^2$], $\eta$, and $V_{T0}$=0.02586 V are the reverse saturation current density, the ideality coefficient, and the thermal voltage, respectively, all at *reference*

*temperature* $T_0$; $V_{BEj}$ is the internal (junction) base-emitter voltage, that is, $V_{BEj}=V_{BE}-R_B \cdot I_B-R_E \cdot I_E$, where $V_{BE}$ is the externally-accessible base-emitter voltage, and $R_B$, $R_E$ [Ω] are the parasitic base and emitter resistances; $V_{AF}$ [V] is the forward Early voltage; the temperature rise $\Delta T_j=T_j-T_0$ [K] is defined in Subsection 3.1.1; $\phi$ [V/K] is the temperature coefficient of $V_{BEj}$. It is clear that (6.1) accounts for the temperature dependence of $I_C$ through a $V_{BEj}$ shift, while $J_{S0}$, $\eta$, $V_{T0}$ are kept at their $T_0$ values (e.g., [Zha96]). Parameter $\phi$ is assumed to depend on $I_E$ according to the following logarithmic law ([Liu94], [Nen04], [dAl10], [dAl11], [dAl14], [dAl16], [dAl18]):

$$\phi = \phi_0 - \eta \cdot \frac{k}{q} \cdot \ln\left(\frac{I_E}{A_E \cdot J_{S0}}\right) \tag{6.2}$$

where $\phi_0$ [V/K] is a fitting parameter, $k$ [eV/K] is the Boltzmann's constant, and $q$ [C] is the (absolute value of the) electron charge. M (≥1) is the $V_{CB}$-dependent avalanche multiplication factor, for which any model can in principle be adopted. For the GaAs HBTs under test, the classic Miller model [Mil57] was chosen

$$M = \frac{1}{1-\left(\dfrac{V_{CB}}{BV_{CBO}}\right)^{n_{II}}} \tag{6.3}$$

$BV_{CBO}$ [V] and $n_{II}$ being the open-emitter breakdown voltage and a fitting power factor, respectively. The term $B_{HI}$ (≥1) is introduced to describe high-injection (HI) effects, i.e., the Kirk-induced gain roll-off; $B_{HI}$ is modeled as [Nen06], [dAl16], [dAl18]

$$B_{HI} = 1+\left(\frac{\alpha_F \cdot I_E}{A_E \cdot J_{HI}}\right)^{n_{HI}} \tag{6.4}$$

where $\alpha_F$ is the common-base (CB) forward current gain, while $J_{HI}$ [A/μm$^2$] and $n_{HI}$ are fitting parameters. The common-emitter (CE) forward current gain $\beta_F$ is modeled as

$$\beta_F = \beta_{F0} \cdot \left(1 + \frac{V_{CB}}{V_{AF}}\right) \cdot \frac{1}{B_{HI}} \cdot \exp\left[\frac{\Delta E_G}{k} \cdot \left(\frac{1}{\Delta T_j + T_0} - \frac{1}{T_0}\right)\right] \qquad (6.5)$$

where $\beta_{F0}$ is the gain at $T_0$, at medium current levels (i.e., before the Kirk-induced fall-off), and in the absence of Early effect, while $\Delta E_G$ [eV] is the difference between the bandgaps of emitter and base yielding a negative temperature coefficient (NTC). The CB gain $\alpha_F$ in (6.4) is related to the CE counterpart by $\alpha_F=\beta_F/(1+\beta_F)$.

The base current is given by (e.g., [Rin06], [dAl18])

$$\begin{aligned} I_B &= I_{BnoAV} - I_{AV} = \frac{I_{CnoAV}}{\beta_F} - (M-1) \cdot I_{CnoAV} = \\ &= I_{CnoAV} \cdot \left(\frac{1}{\beta_F} + 1 - M\right) = I_{CnoAV} \cdot \left(\frac{1}{\alpha_F} - M\right) = \\ &= I_C \cdot \left(\frac{1}{\alpha_F M} - 1\right) \end{aligned} \qquad (6.6)$$

It is worth noting that replacing the simple M formulation (6.3) with a more complex one (e.g., [Rin06], [Sas10]), the model can be adopted for bipolar transistors fabricated in *any* technology if a proper parameter calibration procedure is performed (in Si BJTs, $\Delta E_G$ is *negative*, since the bandgap of the emitter is narrower than that of the base due to high doping levels).

The parameter extraction procedure is straightforward (details are reported in [dAl14], [dAl16]). The single-cell values used for the simulations described in Sections 6.1.3 and 6.1.4 are: $A_E$=164 µm$^2$; $J_{S0}=3.5\times10^{-26}$ A/µm$^2$; $\eta$=1.01; $V_{AF}$=1000 V (negligible Early effect); $\beta_{F0}$=135; $\phi_0$=5.4 mV/K; $\Delta E_G/k$=200 K$^{-1}$; $J_{HI}$=0.35 mA/µm$^2$; $n_{HI}$=1; $BV_{CBO}$=27 V; $n_{II}$=9 (as suggested in [Zam01]); $R_E$=1 Ω; $R_B$=3.5 Ω.

## 6.1.2 SPICE macromodeling technique

The simulation approach relies on the thermal equivalent of the Ohm's law and can be described as follows.

The $R_{TH}$ matrix computed during the pre-processing step is included in a TFB, where the $R_{TH}$s are represented by electrical ones. The TFB serves to evaluate the average temperature rises $\Delta T_j$ of the individual cells (output) from their (input) $P_D$s.

The bipolar transistor model is implemented with a SPICE-compatible subcircuit (which describes one *unit cell*) by resorting to the macromodeling technique. In addition to the standard base, collector, and emitter terminals, the subcircuits are equipped with an (input) node carrying the average temperature rise $\Delta T_j$, and an (output) power node. The main element is the standard SPICE BJT, while additional components (resistances and linear/nonlinear current/voltage sources) are included to describe specific physical mechanisms and modify the temperature-sensitive parameters (e.g., $V_{BEj}$ and $\beta_F$) during the simulation run. A sketch of the subcircuit is reported in Fig. 6.1.

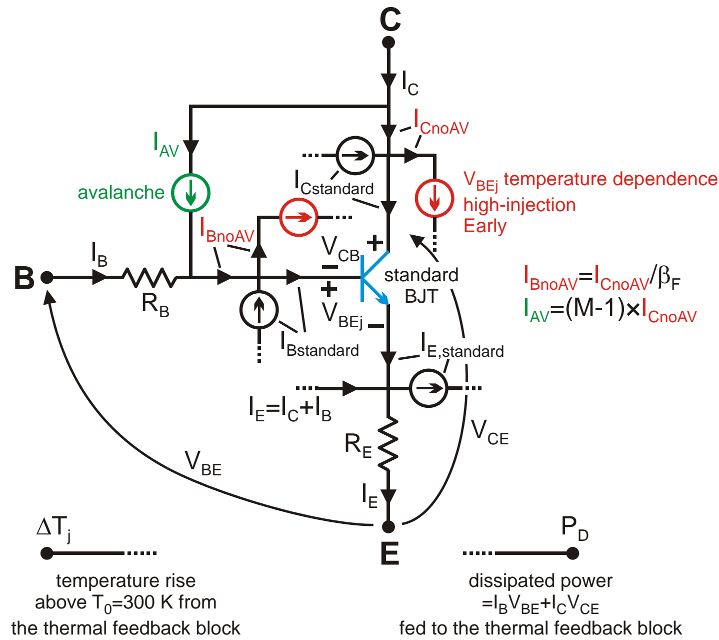



**Fig. 6.1** Simplified representation of the *unit cell* subcircuit.

The devices and arrays under analysis are constructed in the schematic of a SPICE-like circuit simulator by shorting the corresponding electrical terminals of the paralleled *unit cell* subcircuits,

and connecting their temperature and power nodes to the TFB. This leads to a purely electrical *macrocircuit* accounting for ET effects, where voltages and currents at specific nodes and branches are temperature rises and $P_D$s, respectively, and the electrical resistances in the TFB represent thermal ones (thermal-electrical equivalence). An illustration of the *macrocircuit* is shown in Fig. 6.2.

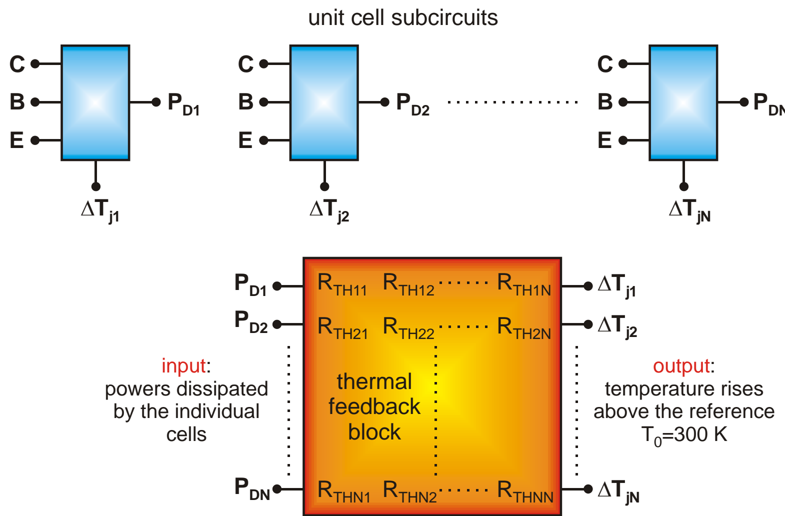



**Fig. 6.2** Sketch of the merely-electrical *macrocircuit* including ET effects through the thermal equivalent of the Ohm's law. The paralleled subcircuits describing the *unit cells* are connected to a TFB containing the $R_{TH}$s computed from the COMSOL outcome in the pre-processing stage.

Nonlinear thermal effects induced by the high cell temperatures are accounted for through the Kirchhoff's transformation [Car59]: the nonlinear temperature $\Delta T_j$ fed to the subcircuit is evaluated as (e.g., [Pou92])

$$\Delta T_j = T_0 \cdot \left[ m + (1-m) \cdot \left( \frac{\Delta T_{j\text{lin}}}{T_0} + 1 \right) \right]^{\frac{1}{1-m}} - T_0 \qquad (6.7)$$

where $\Delta T_{j\text{lin}}$ is the temperature rise determined under linear thermal conditions; the power factor m is set to 1.25, which is the value commonly adopted for GaAs [Pal04]. Eq. (6.7) is implemented with a nonlinear voltage-controlled voltage source.

The popular PSPICE program [PSP11] was used, although any other circuit simulator could in principle be chosen. The resulting *macrocircuit* is well-suited to describe the thermally-induced distortion in the DC characteristics of the test devices and arrays in spite of the constant (independent of $P_D$) and uniform (shared by all components) temperature set to $T_0$.

The following observations can be made: (i) thanks to the robust PSPICE algorithms, the *macrocircuit* is quickly solved: only a few seconds are required for the halved 28-cell array comprising 14 cells; (ii) it is easy to monitor key cell parameters, as well as voltages, currents, $P_D$s, and junction temperatures, thereby favoring a detailed understanding of the phenomena behind the DC ET behavior of the device/array.

It must be remarked that, contrary to advanced compact bipolar transistor models with temperature-dependent parameters and equipped with a thermal node (like HiCuM [Sch10], VBIC, and Mextram504 available in Keysight ADS), the proposed model/subcircuit is only suited to well describe the saturation and forward active modes under DC conditions. RF simulations including ET effects can be enabled by resorting to a similar strategy based on one of the aforementioned models in ADS; however, this requires additional effort to (i) perform transient thermal-only simulations in COMSOL; (ii) identify/synthesize an equivalent thermal network for the description of the SH and mutual $Z_{TH}$ to be included in the TFB (not available in the simulator); (iii) provide the advanced model with a power (output) node and deactivate the internal one- or two-pair thermal network; (iv) extract all the parameters of the model, which is a non-trivial task (quite cumbersome procedures are needed); (v) create the *macrocircuit* in ADS connecting the model instances among them and with the TFB. It should be noted that the adoption of the internal thermal networks of the models in lieu of the TFB would (i) lead to a significant inaccuracy in terms of SH (the typical single pair is not enough for the transient SH response [Mag14]), and (ii) exclude the mutual thermal interaction between *unit cells*, which however plays a relevant role, as discussed in Subsections 6.1.3 and 6.1.4. As an alternative, one could resort to an ET solver available in recent ADS releases that couples a layout-based numerical thermal tool to the circuit simulator (where the thermal

networks embedded in the transistor models are disabled); however, the iterative process leading to convergence is very resource-hungry.

On the other hand, if an user only wishes to explore the DC behavior – differently to the procedure in Subsection 4.4.2 describing the approach for dynamic ET simulations – to gain insight, the model proposed in this Section is a good candidate, since it is quite simple, accurate enough, and requires minimum effort in parameter extraction, which relies only on DC measurements.

### 6.1.3 ET behavior of test structures

Fig. 6.3 shows the $V_{BE}$-constant $I_C$–$V_{CE}$ characteristics of the single-cell HBT (the $R_{TH}$ of which was calculated to be about 440 K/W from the COMSOL temperature field). The curves of the unballasted device (Fig. 6.3a) are affected by a *flyback* mechanism followed by a negative-differential-resistance (NDR) branch [Pop70], [Lat81], [Rin05a], [Rin06], [LaS09], [dAl18], which can be simulated/measured by (i) incrementing $I_C$ or (ii) connecting a resistor $R_{Cext}$ to the collector terminal, sweeping $V_{Cext}$ on the available resistor node, and evaluating $V_{CE}$ as $V_{Cext}$-$R_{Cext}$·$I_C$. It is worth noting that increasing $V_{CE}$ beyond the value corresponding to the flyback would have instead led to a *thermal runaway* (shown for $V_{BE}$=1.25 V) with sudden device failure. Adding a base-ballast resistor (as suggested in [Liu96]) with $R_{Bext}$=400 Ω (Fig. 6.3b) (i) pushes the flyback rightward for low $V_{BE}$; (ii) prevents the flyback (and thus the runaway) at medium/high $V_{BE}$; however, (iii) it reduces the internal (junction) $V_{BEj}$ at medium/high current levels, decreasing and limiting the collector current.

Fig. 6.4 shows the behavior of the 2-cell test device under $I_{BTOT}$-constant conditions. For the unballasted case (Fig. 6.4a), a *bifurcation* phenomenon is observed: beyond a critical $V_{CE}$ (equal to 7.5 V for $I_{BTOT}$=0.5 mA, and decreasing for higher $I_{BTOT}$), one cell tends to conduct the whole current, while the other gradually runs dry [Liu93a], [Liu94], [Liu95], [Rin05b], [LaS06], [LaS10]. It is *not* possible to identify *a priori* which cell will take all the current, since it is determined by *random* (and unavoidable) technology and layout fluctuations. In PSPICE the cells are assumed electrically identical, and the current hogging in cell #2 is favored by a marginally higher SH $R_{TH}$ due to a slight layout asymmetry. As far as the total collector current

$I_{CTOT}$ is concerned, a smooth NDR behavior due to the $\beta_F$ NTC is observed in the $V_{CE}$ range where $I_{CTOT}$ is equally shared by the 2 cells.

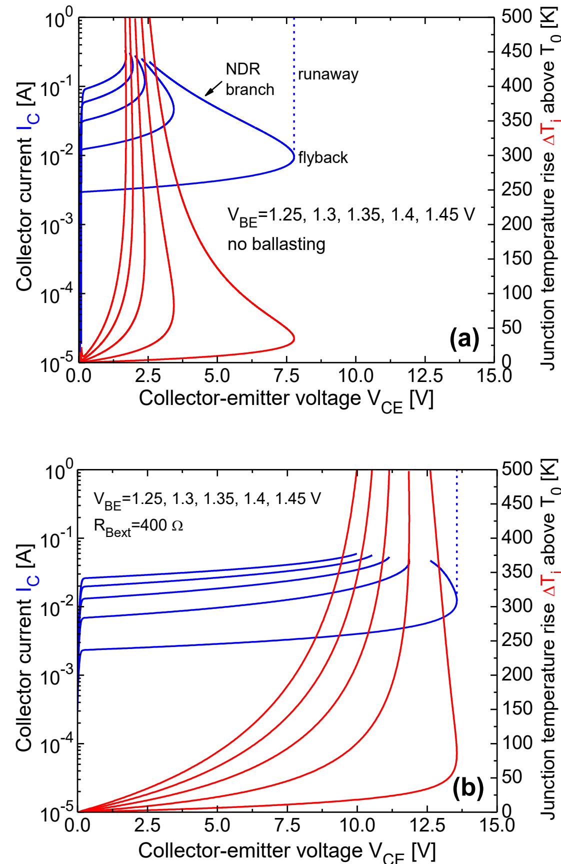



**Fig. 6.3** Test device with single *unit cell*: simulated collector current $I_C$ and corresponding temperature rise $\Delta T_j$ vs. $V_{CE}$ for various $V_{BE}$ values (a) without ballasting and (b) with $R_{Bext}$=400 Ω connected to the base.

The smooth NDR region is then replaced by a marked $I_{CTOT}$ reduction within the bifurcation region due to the 'faster' temperature growth with $V_{CE}$ in the hotter cell, which implies a significant $\beta_F$ decrease; such a behavior is also denoted as *collapse of collector current* [Liu93a] or *collapse of current gain* [Liu95], [Rin05b]. As $V_{CE}$ exceeds 14 V, the II current $I_{AV2}$ (=100 μA at $V_{CE}$=15 V) can no longer be neglected with respect to $I_{BTOT}$; as a result, the avalanche-less current $I_{BnoAV}$, almost equal to $I_{BTOT}$+$I_{AV2}$, perceptibly grows due to the $I_{AV2}$

increase, and in turn raises $I_{C2}$≈$I_{CnoAV}$ (≈$I_{CTOT}$). The inclusion of base ballasting with $R_{Bext}$=400 Ω per cell (Fig. 6.4b) removes the bifurcation phenomenon, thus restoring a uniform behavior along the whole $V_{CE}$ range [Liu96].

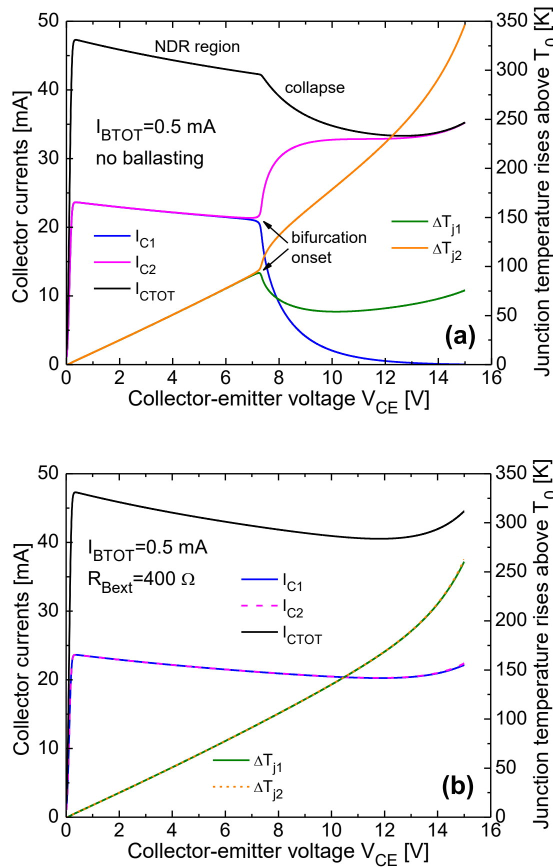



**Fig. 6.4** Test device with 2 *unit cells*: simulated collector currents and junction temperature rises against $V_{CE}$ for $I_{BTOT}$=0.5 mA (a) without ballasting and (b) ballasted with $R_{Bext}$=400 Ω.

Fig. 6.5 illustrates the behavior of the same 2-cell test device under $V_{BE}$-constant conditions. Let us examine the unballasted case (Fig. 6.5a). If $I_{CTOT}$ is swept, the current is equally divided between the *unit cells* until a flyback takes place, followed by an NDR branch still showing uniform operation; at low $V_{BE}$ (e.g., 1.22 V), a bifurcation will also occur for relatively low cell temperatures [Rin06], [LaS06]. A

similar behavior was observed for more paralleled BJTs in silicon-on-glass technology [LaS10]; in that case, an uneven current distribution was found to arise beyond the uniform NDR branch under $I_{CTOT}$-controlled conditions.

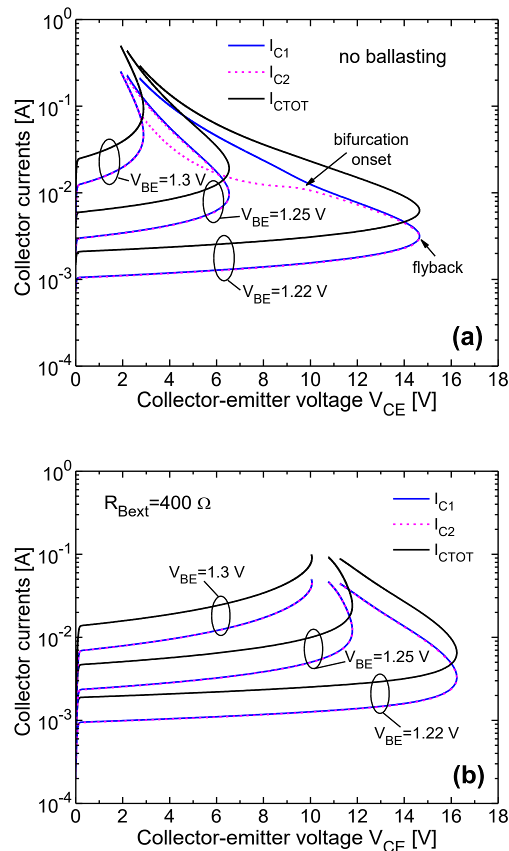



**Fig. 6.5** Test device with 2 *unit cells*: simulated collector currents vs. $V_{CE}$ for $V_{BE}$=1.22, 1.25, 1.3 V (a) without ballasting and (b) ballasted with $R_{Bext}$=400 Ω. The simulations were stopped as the junction temperature rises of both cells (or of the hottest cell in the bifurcation region) reached 500 K.

By increasing $V_{CE}$, the whole device (or at least one of the 2 cells) would have blown up beyond the value corresponding to the flyback; this means that our simulations do not confirm the experimental observation of a ‘safe’ collapse encountered in [Liu95], [Rin05b].The benefit of individually base-ballasting the cells is evident

in Fig. 6.5b: the flyback points are pushed toward higher $V_{CE}$ values and the low-$V_{BE}$ bifurcation vanishes; however, the current capability of the device is significantly reduced at high current levels.

It is also important to analyze the ET behavior of the 2-cell device under $I_{ETOT}$-controlled conditions, typical for differential pairs and comparators [Jar01]. Results obtained by increasing the total emitter current $I_{ETOT}$ for $V_{CB}$=8 V are shown in Fig. 6.6 without (6.6a) and with (6.6b) base ballasting, respectively.

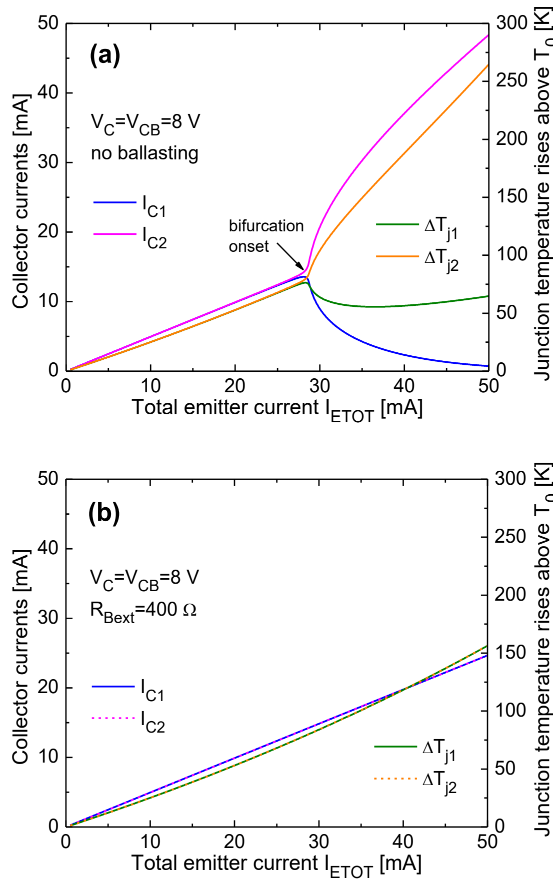



**Fig. 6.6** Test device with 2 *unit cells*: simulated collector currents vs. total collector current $I_{ETOT}$ for $V_{CB}$=8 V (a) unballasted and (b) ballasted with $R_{Bext}$=400 Ω. In (a), $\Delta T_{j1}$ increases beyond $I_{ETOT}$=37 mA due to the thermal coupling with cell #2.

Fig. 6.6a evidences that for a critical $I_{ETOT}$ value (28 mA for $V_{CB}$=8 V) a bifurcation phenomenon is triggered, and the whole $I_{CTOT}$

eventually flows in cell #2, rapidly increasing its temperature; a similar behavior would be obtained by assigning $I_{ETOT}$ and sweeping $V_{CB}$ [Rin06], [LaS06], [LaS09], [LaS10]. Applying the resistors $R_{Bext}$=400 Ω, thermal effects are weakened and the bifurcation disappears, limiting the temperature shared by the 2 cells to much lower values.

The ET behavior of the test device composed by 3 *unit cells* – assumed ideally identical in PSPICE – is now considered. The first simulation was performed under CE conditions by increasing $V_{CE}$ with a constant $I_{BTOT}$=0.7 mA; ballasting resistors $R_{Bext}$=400 Ω were applied to all cells. Fig. 6.7a depicts the collector currents, while Fig. 6.7b shows the temperature rises above $T_0$. It is found that cell #2 starts conducting more current due to the thermal coupling with both the adjacent (outer) cells #1 and #3. For higher $V_{CE}$ values, a counterintuitive behavior takes place: a bifurcation mechanism involving cells #1 and #3 occurs for $V_{CE}$>14 V; in particular, #3 eventually bears more current, whereas #1 turns off, as induced by the slightly higher SH $R_{TH}$ of #3 with respect to #1. By further increasing $V_{CE}$, cell #3 prevails over #2 since the SH $R_{TH}$ of #3 (396.2 K/W) is perceptibly higher than that of cell #2 (361.7 K/W), which enjoys a more effective upward heat flow through metal 2 (M2). The strongly uneven current distribution for $V_{CE}$>14 V turns into a collapse in the $I_{CTOT}$–$V_{CE}$ curve. For $V_{CE}$>16 V, cell #3 conducts the whole current and therefore $I_{B3}=I_{BnoAV3}-I_{AV3}\approx I_{BTOT}$=0.7 mA; the increase of $I_{AV3}$ with $V_{CE}$ due to the enhanced II leads to a growth in $I_{BnoAV3}$, which dominates over the NTC of $\beta_{F3}$, thus driving an $I_{C3}\approx I_{CTOT}$ increase. On the other hand, $\Delta T_{j3}$ exceeds 500 K for $V_{CE}$>15 V; consequently, cell #3 is likely to fail before restoring a positive $I_{CTOT}$ slope.

It is worth noting that increasing the emitter area of cell #1 by only 1 $\mu m^2$ the onset of the bifurcation takes place at the same $V_{CE}$ (14 V), but the behavior of #1 and #3 reverses: cell #1 prevails over #3, and eventually sinks also the current of #2. The $I_{CTOT}$–$V_{CE}$ curve coincides with the one obtained with ideally identical cells (shown in Fig. 6.7a). This means that it is impossible to foresee which of the outer cells will dominate, since it depends on unavoidable technological discrepancies. The practical implication is that the failure analysis should look at planes of symmetry, and not at the specific failed cell.

To understand whether the 3-cell test device enjoys a thermally-stabilizing effect dictated by the low SH $R_{TH}$ of the inner cell #2 (361.7 K/W), a test simulation was performed by considering all the SH $R_{TH}$s equal to 396 K/W (that is, the $R_{TH}$ of the central cell was assumed identical to those of the lateral cells). Fig. 6.8 demonstrates that the *classical* collapse with #2 conducting the whole current is obtained. Unfortunately, the collapse onset in the $I_{CTOT}$–$V_{CE}$ characteristic takes place at the same $V_{CE}$ of the real test device with lower $R_{TH}$ for #2; this means that the bifurcation mechanism occurring for the outer cells in the real case is as deleterious as the strong thermal coupling affecting #2 in the more ideal device with uniform $R_{TH}$s.

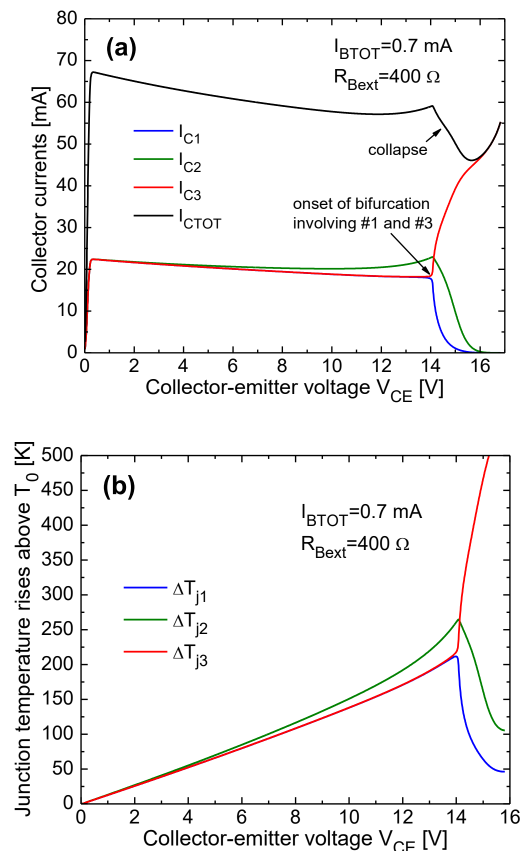



**Fig. 6.7** Test device with 3 *unit cells* ballasted with $R_{Bext}$=400 Ω: simulated (a) collector currents and (b) junction temperature rises above $T_0$ as a function of $V_{CE}$.

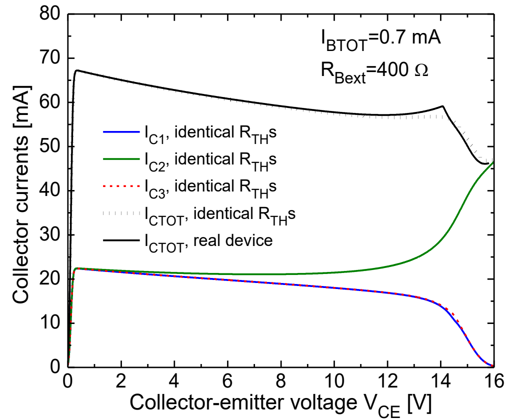



**Fig. 6.8** Test device with 3 *unit cells* ballasted with $R_{Bext}$=400 Ω and identical SH $R_{TH}$s: simulated collector currents vs. $V_{CE}$; also shown is the $I_{CTOT}$–$V_{CE}$ characteristics computed for the real structure.

Lastly, Fig. 6.9 shows the $I_{CTOT}$–$V_{CE}$ curves of the base-ballasted 3-cell device for various $I_{BTOT}$ values compared to the unballasted counterpart. Also for the latter case, it is found that the collapse originates from the bifurcation between the outer cells #1 and #3. However, this happens for much lower $V_{CE}$s, that is, the *collapse locus* significantly moves leftward, dramatically shrinking of the DC safe (i.e., uniform) operating area.

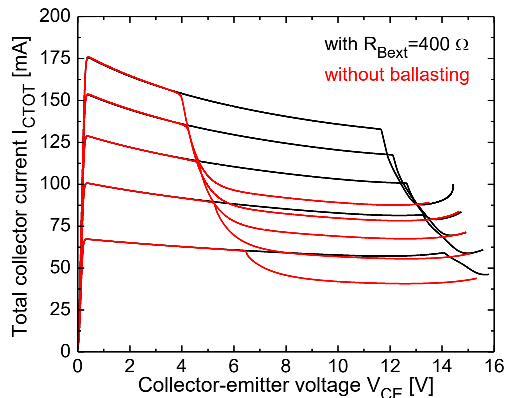



**Fig. 6.9** Simulated $I_{CTOT}$–$V_{CE}$ characteristics for the ballasted (black) and unballasted (red) 3-cell test device for $I_{BTOT}$=0.7, 1.2, 1.7, 2.2, 2.7 mA.

### 6.1.4 ET behavior of arrays for power amplifiers

As already mentioned in Subsection 2.1.2, only half of each array for PA output stages was actually simulated by exploiting the horizontal symmetry. This means (i) that only 12 (14) cells were taken into account for the 24-cell (28-cell) arrays; (ii) $I_{CTOT}$ and $I_{BTOT}$ are the total collector and base currents of the semi-arrays.

The analysis mainly focuses on $I_{BTOT}$-constant CE conditions, since GSM PAs are more or less biased with a constant $I_{BTOT}$.

Let us first consider the halved 24-cell array ballasted with the nominal $R_{Bext}$=400 Ω per *unit cell*. Fig. 6.10 reports the PSPICE results corresponding to $I_{BTOT}$=2 mA. As can be seen, a marked current/temperature nonuniformity takes place as $V_{CE}$ exceeds 7 V, leading to an $I_{CTOT}$ collapse (not shown in the figure). Below $V_{CE}$=10 V, symmetric cell pairs (namely, #9 and #10, #8 and #11, #7 and #12, and so on) still share the same current. As $V_{CE}$ reaches 10 V, all cells of the left column (#1 to #6) turn off, while a bifurcation mechanism occurs for all the symmetric cells of the right column (#7 to #12). Due to slight layout asymmetries, #9 prevails over #10, and then #8 and #7 dominate over #11 and #12, respectively; the uneven behavior is thus enhanced, and $I_{CTOT}$ decreases more steeply with $V_{CE}$. The inner cell #9 then sinks current from #8 and #7, even though it is likely to burn out before conducting the whole current of the semi-array ($\Delta T_{j9}$ exceeds 500 K at $V_{CE}$=10.1 V).

It must be remarked that introducing an intentional (very small) technological discrepancy between #9 and #10 to favor a slightly higher conduction of #10, this cell takes the whole current after the bifurcation onset; the $I_{CTOT}$–$V_{CE}$ curve, including the collapse region, remains instead unchanged.

The same behavior was found to occur for $I_{BTOT}$<2 mA; it must be remarked the temperature shared by #9 and #10 at the bifurcation onset reduces as $I_{BTOT}$ decreases.

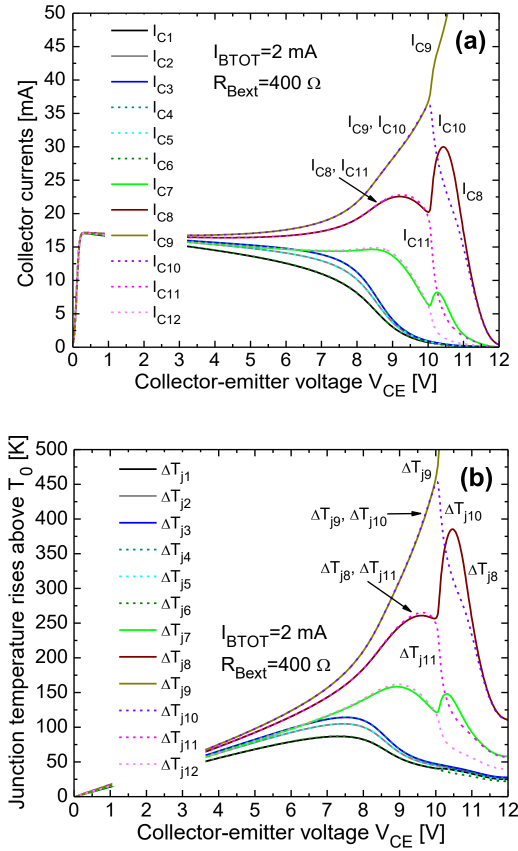



**Fig. 6.10** Simulated (a) collector current and (b) junction temperature rises above $T_0$ for the 12 cells of the halved 24-cell array ballasted with $R_{Bext}$=400 Ω per cell, and biased with $I_{BTOT}$=2 mA.

For $I_{BTOT}$≥2.5 mA, the right-column bifurcation takes place as the common junction temperature of cells #9 and #10 has already exceeded 500 K; in other words, the metallization over these cells is likely to melt before the bifurcation arises, and implies that the exacerbated $I_{CTOT}$ collapse can no longer be observed. This is related to the major role played by the mechanisms weakening the ET feedback, like ballasting and parasitic resistances, ϕ reduction with current, and HI effects. Fig. 6.11 shows the scenario for $I_{BTOT}$=3 mA.

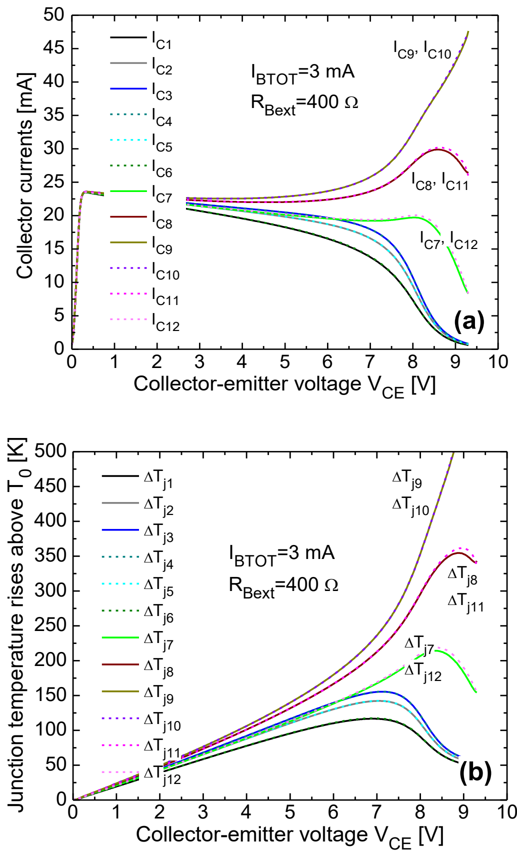



**Fig. 6.11** Simulated (a) collector current and (b) junction temperature rises above $T_0$ for the 12 cells of the halved 24-cell array ballasted with $R_{Bext}$=400 Ω per cell, and biased with $I_{BTOT}$=3 mA.

Fig. 6.12a illustrates the $I_{CTOT}$–$V_{CE}$ curves corresponding to various $I_{BTOT}$ values for the cases of nominal base ballasting ($R_{Bext}$=400 Ω per cell), emitter ballasting ($R_{Eext}$=4 Ω per cell, considered approximately equivalent to $R_{Bext}$=400 Ω by circuit designers), and full absence of ballasting. Fig. 6.12b shows the corresponding temperature rise above $T_0$ for the hottest cell #9. In the absence of ballasting, the $V_{CE}$ range enjoying uniform current and temperature distribution dramatically reduces; beyond a critical (and low) $V_{CE}$, the pair #9, #10 starts taking more current and then a bifurcation arises, eventually leading to the conduction of cell #9 only. The base ballasting with $R_{Bext}$=400 Ω is found to ensure a more

effective stabilizing effect than the emitter ballasting with $R_{Eext}$=4 Ω. It is noteworthy that for $I_{BTOT}$>2 mA, contrary to the base-ballasted solution, for the emitter-ballasted and unballasted cases the right-column bifurcation onset (and thus the onset of the sharper collapse shape) occurs for $\Delta T_{j9}=\Delta T_{j10}$ well below 500 K. An example is reported in Fig. 6.13, which shows the temperature rises for the unballasted case biased with $I_{BTOT}$=3 mA. It is inferred that in the bifurcation region, as #9 dominates, the cells symmetric with respect to #9 (i.e., #8 and #10, #7 and #11) tend to exhibit a similar behavior.

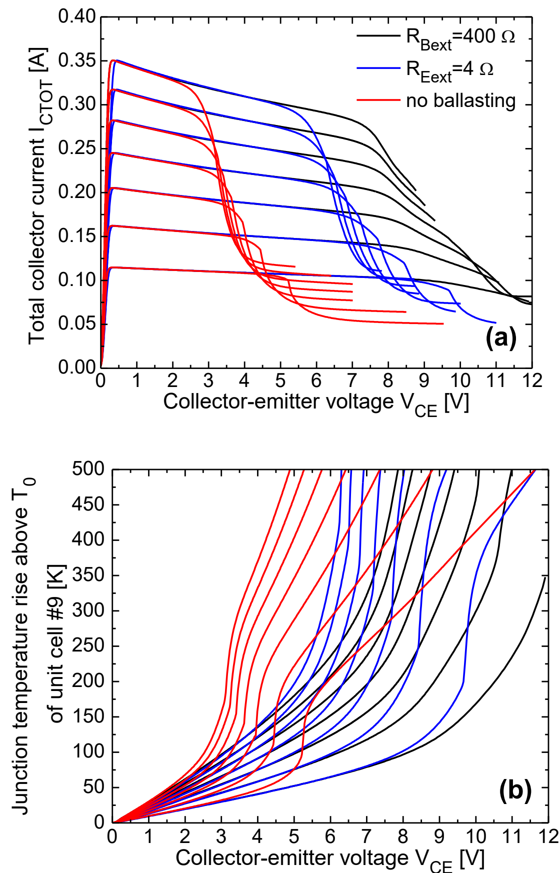



**Fig. 6.12** Simulated (a) total collector current and (b) junction temperature rises above $T_0$ of cell #9 vs. $V_{CE}$ for half of the 24-cell array biased with $I_{BTOT}$=1, 1.5, 2, 2.5, 3, 3.5, 4 mA. Comparison between the case with no ballasting (red), and those benefiting from $R_{Bext}$=400 Ω (black) and $R_{Eext}$=4 Ω (blue).

From the inspection of Figs. 6.12 and 6.13, the following findings emerge: (i) a smooth $\Delta T_{j9}$ increase corresponds to the uniform NDR region in the $I_{CTOT}$–$V_{CE}$ curve; (ii) the 'faster' $\Delta T_{j9}$ growth and the $I_{CTOT}$ collapse are associated with uneven current/temperature distribution, wherein the right-column cells (in particular, the inner ones) conduct almost all the current; (iii) the very sharp $\Delta T_{j9}$ rise and the more dramatic $I_{CTOT}$ collapse are induced by the right-column bifurcation, where cell #9 takes more and more current; (iv) the final linear increase in $\Delta T_{j9}$ and the $I_{CTOT}$ 'saturation' to a value much lower than the expected (isothermal at $T_0$) one are due to #9 carrying almost the entire current: in the absence of II (like in the unballasted case), $\Delta T_{j9}$ is almost equal to $R_{TH99}(T_{j9})\cdot\beta_F(T_{j9})\cdot I_{BTOT}\cdot V_{CE}$ where $V_{CE}$ increases linearly, and there is a compensation between the NTC of $\beta_F$ and the $R_{TH99}$ increase with temperature due to nonlinear thermal effects.

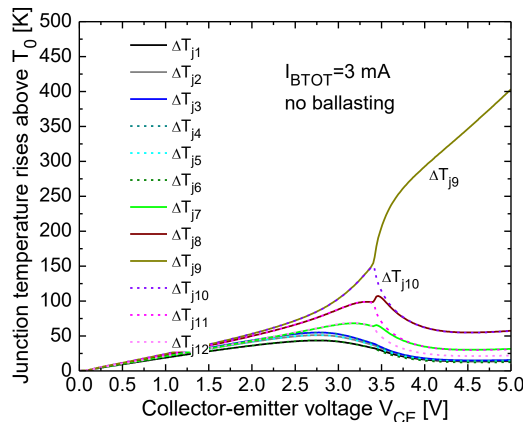



**Fig. 6.13** Simulated junction temperature rises above $T_0$ for half of the unballasted 24-cell array biased with $I_{BTOT}$=3 mA.

Fig. 6.14 depicts the PSPICE results obtained under CE conditions for $I_{BTOT}$=3.5 mA for the ET behavior of the halved 28-cell array with an odd number (=7) of cells per column, all ballasted with $R_{Bext}$=400 Ω.. It is found that beyond $V_{CE}$=7 V a severely-uneven current distribution occurs, leading to the collapse in the $I_{CTOT}$–$V_{CE}$ curve (not shown). The whole current is first conducted mostly by the inner cells, namely, #11 (the hottest one), and the #10, #12, and #9, #13 pairs, and then by #11 and the #10, #12 pair. The cells of the left column

(#1 to #7) tend to switch off. No bifurcation takes place for the symmetric right-column pairs as far as $\Delta T_{j11}$<500 K.

Simulations at lower $I_{BTOT}$ values led to the following observations: (i) again the collapse is induced by the marked current nonuniformity in current distribution arising at slightly higher $V_{CE}$s, and (ii) a bifurcation mechanism is triggered for the symmetric cells of the right column (#10 and #12, #9 and #13, #8 and #14) at $\Delta T_{j11}$ values well below 500 K.

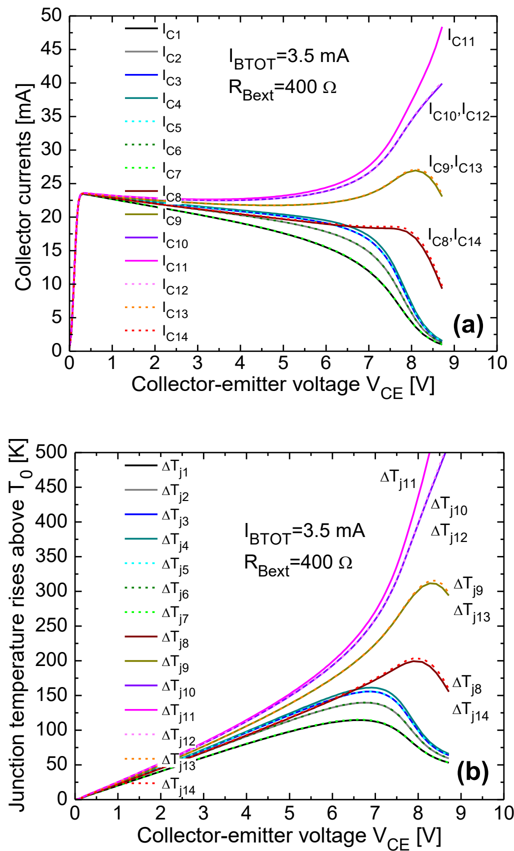



**Fig. 6.14** Simulated (a) collector currents and (b) junction temperature rises above $T_0$ for half of the ballasted 28-cell array biased with $I_{BTOT}$=3.5 mA.

Lastly, an interesting (and fair) comparison is performed between the halved portions of the ballasted 24- and 28-cell arrays by applying various $I_{BTOT}$ values ensuring the same total base current

density in both cases. Results are reported in Fig. 6.15; more specifically, Fig. 6.15a shows the $J_{CTOT}$–$V_{CE}$ characteristics ($J_{CTOT}$ being the total collector current density, defined as $I_{CTOT}/A_{ETOT}$), and Fig. 6.15b depicts the junction temperature rise of the hottest *unit cell* (#9 and #11 for the 24- and the 28-cell arrays, respectively).

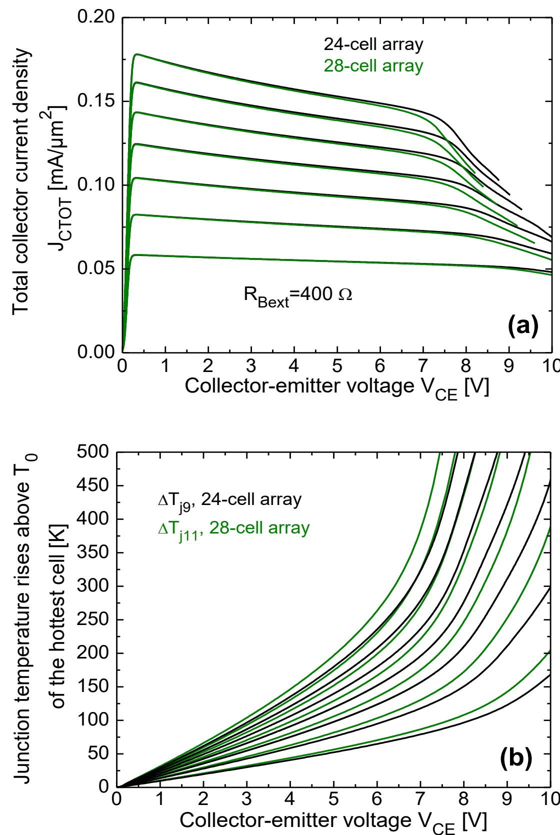



**Fig. 6.15** Simulated (a) total collector current density $J_{CTOT}$ and (b) junction temperature rises above $T_0$ of the hottest *unit cell* for half of the ballasted 24-cell (black) and 28-cell (green) arrays. The halved 24-cell array was biased with $I_{BTOT}$=1, 1.5, 2, 2.5, 3, 3.5, 4 mA, while the halved 28-cell one with $I_{BTOT}$=1.17, 1.75, 2.33, 2.91, 3.5, 4.08, 4.67 mA.

The analysis demonstrates that the 28-cell array featuring an odd number of cells per column is less thermally robust than the 24-cell counterpart with an even number of cells per column. This is attributed to the fact that *only the innermost cell* (#11) is subject to a strong

thermal coupling with the adjacent cells, while *two* cells (#9 and #10) concurrently bear this task in the 24-cell array. It is worth noting that, although this seems to be an expected result, there are still many designers using arrays with an odd number of cells per column.

## 6.2 Technology fluctuations of SiC-based PMs

Results for a multichip converter based on a SiC PMs are shown in this Section; the analyses are aimed to quantify the influence of parameter fluctuations on the dynamic ET behavior of these modules. A previously developed SiC SPICE MOSFET model [Ric18c] is used in conjunction with a TFB obtained by means of the MOR approach (introduced in Section 3.2). Exploiting the resulting microcircuit, it was possible to predict the temperature unbalances that arise among nominally identical, yet subject to unavoidable discrepancies, parallel devices operating in realistic circuit applications. As a case-study, a synchronous buck converter is simulated with properly-selected values of threshold voltage ($V_{TH}$) and current factor (K) of the SiC MOSFETs constituting the considered PM. The converter was based on a SiC PM where a high-side (HS) and a low-side (LS) MOSFET array, each comprising four parallel 1.2 kV-20 A-rated SiC devices, were arranged in a half bridge configuration. The 3-D COMSOL mesh used to obtain the TFB by means of MOR-based approach is shown in Fig. 6.16, where the PM topology, sizes, and features are illustrated. Insights on the manufacturing technology were given in Subsection 2.2.1.

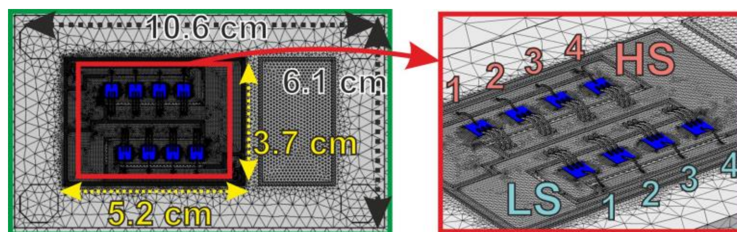



**Fig. 6.16** Top (left) and angled (right) views of the PM structure with HS and LS MOSFETs highlighted.

A schematic view of the microcircuit under analysis is then depicted in Fig. 6.17.

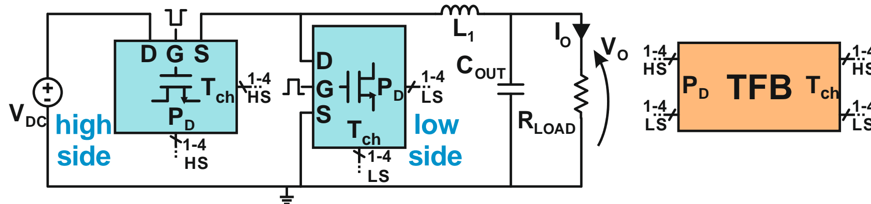



**Fig. 6.17** Circuit schematic of the buck converter under test. The arrays of parallel MOSFETs and TFB are highlighted in light blue and orange, respectively.

Within this simulation framework, the investigation focused on the impact of $V_{TH}$ and K mismatches on parallel connected MOSFETs. In order to evaluate the effects of parameters dispersion, a statistical description of their variability is necessary. Therefore, a realistic technological fabrication process was emulated, where the $V_{TH}$ and K fluctuations are well modeled by Gaussian distributions [Ric18c]. From these, two sets of $V_{TH}$ and K values, defining two different circuit test cases, were extracted for the devices belonging to the converter. In the first test condition (referred to as *balanced*), two unique $V_{TH}$ and K values, equal to the means of the distributions, are shared by all the MOSFETs of the arrays. For the second test condition (*unbalanced*), all the parameters were chosen to fall within a 2σ-wide interval. Fig. 6.18 shows that some of these values were arbitrarily selected at the interval edges in order to more clearly assess the influence of process tolerances on the operating conditions.

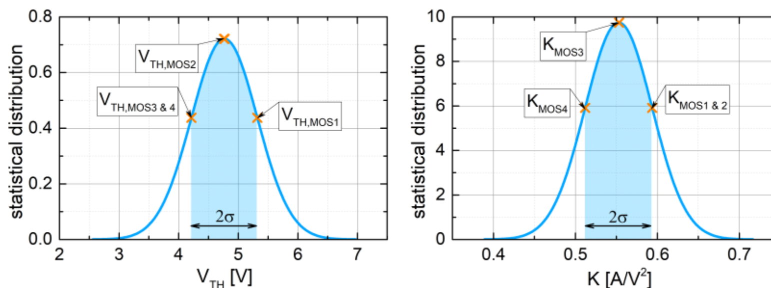



**Fig. 6.18** Unbalanced case: statistical distributions of $V_{TH}$ (left) and K (right); the selected values are marked.

Afterward, the DC-DC converter was simulated over 0.4 s of operation time ($80\times10^3$ switching events) with both the balanced and unbalanced PM configurations. In order to reach a complete

steady-state condition, the simulation interval was chosen sufficiently longer than the thermal and electrical time constants. Even though the simulation time step had an upper bound of only 10 ns, a total computation time of approximately 11 hours was required to simulate both cases simultaneously on a desktop PC equipped with a quad-core Intel i7-2600 CPU.

Fig. 6.19a and 6.19c show that the introduced parameter mismatch does not affect the circuit functionality since a difference of only 0.3% between the average output voltages ($V_{O,AVG}$) of the two test conditions was obtained. On the other hand, the thermal stress withstood by each device was found to be strongly dependent on the selected PM configuration. This is witnessed by Fig. 6.19b, which shows that in the balanced case the temperature mismatches within each array are only determined by the MOSFETs positions: the central devices MOS2 and MOS3 heat up more than the outer ones (MOS1 and MOS4) due to greater impact of mutual thermal effects. Fig. 6.19a illustrates the relatively uniform temperature distribution corresponding to the end of the considered time span. Conversely, for the unbalanced case, a temperature difference amounting to 67°C was observed between the HS transistors MOS3 and MOS1, as shown in Fig. 6.19d.

The highest thermal stress withstood by MOS3 is dictated by its lower $V_{TH}$ (which increases its current capability) and, therefore, by turn-off and turn-on transitions occurring ahead of and behind those of the other parallel MOSFETs, respectively. This makes MOS3 carry most of the transient current, in turn leading to higher switching losses. Interestingly, MOS4 is found to be less subject to thermal effects, although this device shares the same $V_{TH}$ value as MOS3; this can be attributed (i) to its smaller K (i.e., bigger $R_{ON}$), which determines a lower static current flow and thus a lower static $P_D$, and (ii) to a reduced thermal coupling with the other MOSFETs favored by its outer position (Fig. 6.20)

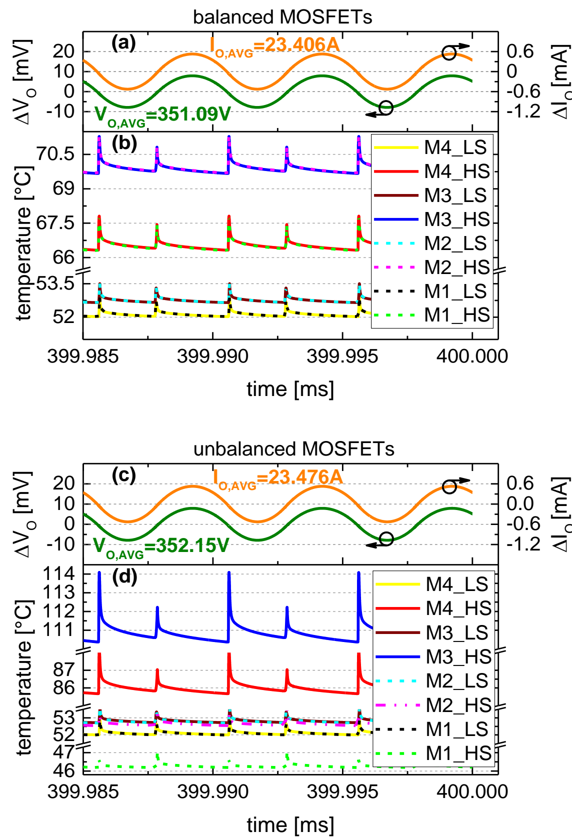



**Fig. 6.19** Output voltage and current of balanced (a) and unbalanced (c) PMs; HS and LS MOSFETs temperature waveforms for the balanced (b) and unbalanced (d) test cases.

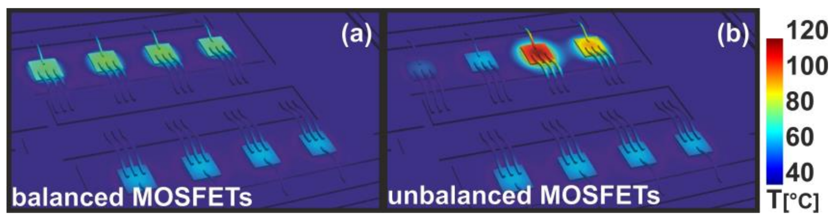



**Fig. 6.20** Temperature maps of balanced (a) and unbalanced (b) PM evaluated at 0.4s.

In both cases, LS devices undergo less severe thermal conditions since their power dissipation during switching transients is lower than that of their HS counterparts, which can be explained as follows: in this

circuit topology, when the LS transistors commutate, their drain-to-source voltage drop corresponds to the forward voltage of the internal body diodes as these start conducting during dead times. However, since in this application the conduction losses only account for a small portion of the total losses, the temperature differences among the LS MOSFETs are primarily imposed by their positions. Consequently, when moving from the balanced to the unbalanced configuration, the LS temperature distribution remains relatively unchanged.

# Conclusions

In this thesis, it has been shown how thermal analyses can support the study and design of electronic devices, circuit, and systems. An accurate investigation of RF devices and power systems has been carried out by mean of a tool that performs accurate 3-D FEM thermal simulations in the environment of COMSOL Multiphysics. Such a tool is based on a commercial 3-D FEM solver and an *in-house* routine for the automatic geometry construction and optimized mesh generation, as well as for the sequential solution of a given series of meshes, and data storing/processing. The high level of accuracy (almost impossible to achieve with a manual process) of these domains has made possible the analyses of thermal issues involving state-of-the-art technologies. At the same time, ET simulations based on compact models have been performed to study instability effects.

The main findings on GaAs-based HBTs for RF applications are summarized in the following.

- A comprehensive study of the role played by semiconductor and metal layers on the device thermal behavior has been carried out for single-emitter HBTs considering different emitter sizes; the analyses show that (i) thicker metallization layers – the major role being played by metal 2 – enforce the shunt effect, thus yielding a significant cooling action; (ii) nevertheless, for short devices, the influence of metal 2 is mitigated since it is not vertically aligned with the emitter stack; (iii) regardless of the emitter area and shape, the sensitivity of the thermal behavior to the deep $In_{0.49}Ga_{0.51}P$ layer is higher than to the other emitter layers; (iv) the thicknesses of the emitter layers are more important in small HBTs where the relevance of the upward heat flow is higher, while having little impact in big transistors that benefit from enhanced downward heat propagation.

- Both wire-bonding and flip-chip packaging solutions have been studied by performing accurate analyses involving all the key technology aspects, including the four-emitter device structure and the laminate technology. For the WB packaging, it has been found out that (i) the laminate design has little impact due to the high thermal conductivity of the Cu vias and plates, unless the vias are drastically shrunk; (ii) temperature maps taken by thermal scans over the M2 top closely resemble the temperature field over the base-emitter junction under non-harsh (i.e., nominal) operating conditions. By comparing the WB and FC technologies, it has been possible to evaluate an improved thermal behavior of FC packaging quantified as a -43.7% thermal resistance reduction. In addition, it has been shown that the role played by the emitter architecture and top metal is amplified in an FC structure. As a consequence, when dealing with FC systems special care should be taken in designing emitter, metallization, die-to-pillars connection, pillars, and laminate to minimize thermal issues.
- In practical HBT arrays for RF PAs, the influence of distance between devices (important because depending on design rules) and connection style has been investigated: (i) for an assigned spacing, the best dynamic thermal coupling is ensured by a thick metal layer running over a thick low-conductivity dielectric (which prevents heat shunt to substrate), whereas the thermal time constant is weakly affected by the connection strategy; (ii) the improved coupling driven by a lower spacing results in a significant increase in mutual resistance and a less marked reduction in thermal time constant. Afterward, a procedure has been outlined for performing dynamic ET analyses in the environment of circuit simulation programs.
- An approach combining a 3-D FEM thermal tool aided by an *in-house* routine and a SPICE circuit simulator has been exploited to provide an overview on the thermally-induced distortion in the I–V characteristics of the investigated structures, and to identify the limits of the safe behavior. Results of ET simulations demonstrated that (i) in the unballasted 3-cell test device, the collapse is triggered by a bifurcation involving the outer cells, which suffer from a SH thermal resistance higher

than that of the inner one; (ii) in arrays for output stages of PAs, base ballasting has been found to be more effective than emitter ballasting, which is typically suggested for breakdown-limited bipolar transistors; (iii) the arrays are more thermally robust if arranged in columns with an even number of unit cells, where *two* central cells concurrently bear the heat coming from the outer cells.

Power systems as SiC-based power modules and GaN-based PCB have been also analyzed by means of the presented simulation approach. The scientific achievements are here summarized:

- To support the PCB thermal design, analytical models – accounting for the dependence upon geometry, materials, and boundary conditions – have been proposed for the thermal resistances of (i) the thermal vias and (ii) the heat-sinks used to cool down power devices mounted on such structures. The comparison between TVs model and FEM simulations has been carried out on 6 PCB designs and shows an average $R_{TH,TV}$ mismatch of 7.5%; the HSK model has been validated by simulating the individual structures of 2 commercial HSKs used in power electronics, and a maximum error of 2.2% has been observed. The proposed models represent a solution for designers to quickly evaluate the thermal performances of the analyzed structures, as a valuable alternative to (i) complex analytical models, (ii) numerical thermal simulations, and (iii) experimental characterizations.
- In PCB structures, it has been possible to evaluate that the thermal behavior can be enhanced by the use of graphene foam, which appears effective in improving the thermal contact between the device case and the PCB, as compared with the case of a device soldered directly to the track. Moreover, the use of a ceramic layer as $Si_3N_4$ or AlN soldered between PCB and heat-sink can also play a key role in reducing the overall thermal resistance, in comparison with standard insulating foil.
- Single-sided and double-sided cooled PMs in SiC-technology have been compared in terms of steady-state thermal behavior to provide useful guidelines on (i) efficient cooling design and (ii) DBC materials choice taking into account the effect of the

boundary conditions applied on the cooling surfaces. It has been found that the DSC technology turns out to have better thermal performances than the SSC one if good convective BCs are ensured (i.e., forced liquid cooled), while a reversed behavior is observed as poorly-cooling BCs are applied. In addition, a study aimed to evaluate the impact of ceramic layers on the thermal performance has been carried out to quantify that the adoption of AlN in lieu of $Si_3N_4$ as ceramic material allows obtaining a maximum self-heating $R_{TH}$ reduction of -70% in DSC PMs with effectively-cooling BCs.

- A methodology to simulate thermally-induced unbalances arising in a power module made of mismatched SiC MOSFETs has been presented. The procedure has been successfully applied to the analysis of a synchronous step-down converter containing eight MOSFETs under balanced and unbalanced test conditions in terms of $V_{TH}$ and K. The significance of the proposed approach lies in the impossibility of identifying critical temperature discrepancies by a simple inspection of the converter output quantities. As a remarkable outcome, strongly dissimilar temperature distributions between the two scenarios have been obtained. While in the balanced case the maximum temperature gap among the individual MOSFETs was confined below 20°C, in the unbalanced one this gap was found to raise to 67°C, with the hottest device reaching 114°C. For a given application, the simulated temperatures obtained with this methodology can be fed to lifetime estimation equations to check whether or not a required target is reached. This, in turn, can provide guidelines on the maximum allowable process tolerances ensuring reliable devices parallelization.

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