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IN

INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

EFFECT OF PARAMETERS SPREAD ON THE PERFORMANCE OF SIC POWER MODULES: DERATING RULES AND ROBUSTNESS ISSUES

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List of Acronyms

1-D	One-Dimensional
2-D	Two-dimensional
3-D	Three-dimensional
AF	Acceleration Factor
BJT	Bipolar Junction Transistor
BV	Breakdown Voltage
CDF	Cumulative Distribution Function
DBC	Direct-Bonded Copper
DPT	Double Pulse Test
DR	Derating Rule
DUT	Device Under Test
ET	Electrothermal
FIB	Focused Ion Beam
FTO	Fail To Open
FTS	Fail To Short
HS	High Side
HVdc	High Voltage DC
ICU	Inverter Control Unit
II	Impact Ionization
ILD	Interlayer Dielectric
ILS	Inductive Load Switching
LIT	Lock In Thermography
LS	Low Side
MC	Monte Carlo
MOSFET	Metal Oxide Semicondutr Field Effect Transistor
MTTF	Mean Time To Failure
NTC	Negative Temperature Coefficient
pdf	probability distribution function

PM	Power Module
PTC	Positive Temperature Coefficient
PWM	Pulse Width Modulation
QEM	Quadratic Extrapolation Method
RMS	Root Mean Square
SC	Short Circuit
SEM	Scanning Electron Microscope
SOA	Safe Operating Area
SPICE	Simulation Program with Integrated Circuit Emphasis
TFB	Thermal Feedback Block
TN	Thermal Network
UIS	Unclamped Inductive Switch
VDMOS	Vertical Diffused MOS
WCA	Worst Case Analysis

Introduction and Outline

1.1 Motivations

Over the past 2 decades, the adoption of silicon carbide (SiC) metal oxide field effect transistors (MOSFETs) surged to the point that some companies have started to embedding them into their commercial products [Link1] [Link2]. This growing trend can be mainly attributed to the development and subsequent commercialization of devices with exceptional static and dynamic characteristics. Although they feature performances that are superior to those of their silicon (Si) counterparts, the highest current rating of state of the art commercial SiC MOSFETs is around 150 A [Link3] [Link4]. This limitation arises from the area of current SiC dies, the increase of which is constrained by the amount of defects of various types introduced by the manufacturing process [Alk16]. Specifically, given a processed wafer with a density of defects per unit area D [cm^{-2}], increasing the size of the single die would make more likely for a device to be defective [Mad21] [Kim20], thus negatively affecting the yield and, eventually, the cost. This is clarified through the idealized defects maps of Fig 1.1.

The value of the current rating limits the variety of applications where such devices can be adopted, thus intensifying the need for paralleling multiple chips to achieve higher current levels. E.g., in the three-phase traction inverter of the Tesla Model 3, 24 SiC MOSFET are used [Link1]. Therefore, each switching cell is presumably implemented through 4 MOSFETs in parallel. However, during the design of an array of parallel semiconductor devices, whether this is implemented at the module level (i.e., by connecting together various chips within the same package) or at circuit level (i.e., by wiring a number of discrete devices on the same circuit board), special care must be taken to mitigate the current imbalance among the parallel units. An

experimental example of uneven current distribution between two

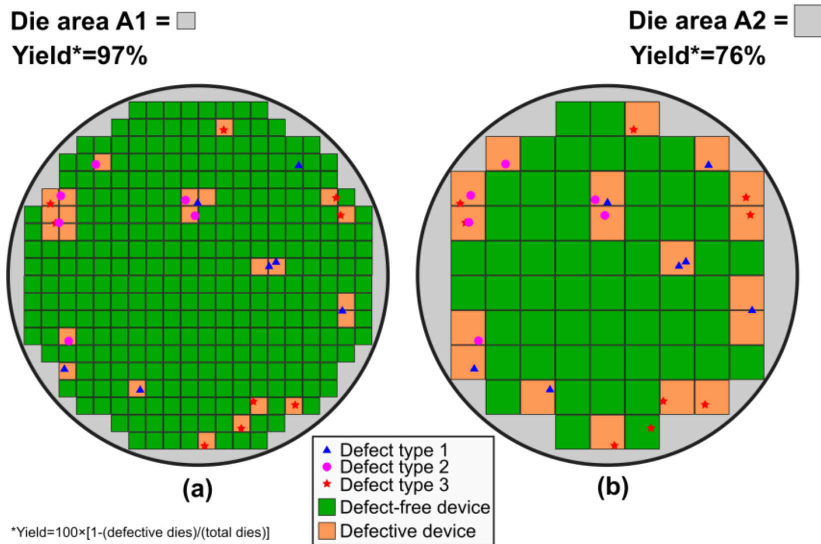


Fig. 1.1 Idealized defects maps of a semiconductor wafer with a density of defects D in the case of (a) dies of area A_1 and (b) dies of area $A_2>A_1$. Increasing the die size lowers the yield of the manufacturing process.

1.2 kV commercial MOSFETs is provided in Fig 1.2.

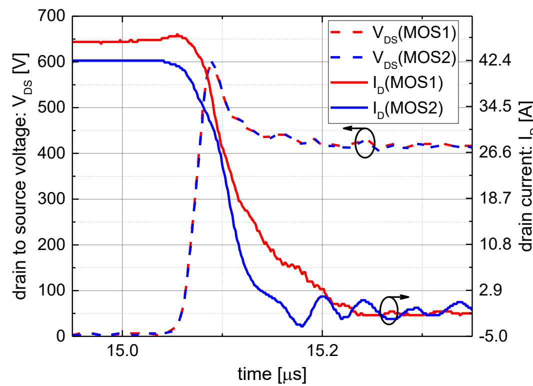


Fig. 1.2 Experimental turn-off switching waveforms (I_D, V_{DS}) of two parallel SiC MOSFETs on an inductive load: L_{LOAD}=50 μH; V_{DC}=400 V.

For SiC power modules, the uneven current sharing can be caused both by mismatches in inherent device parameters and by assembly-related aspects. Although these sources of uncertainty are present also when paralleling Si devices, their effect is made more

prominent for SiC by a less mature technological process (leading to bigger parameters fluctuations) and faster switching transients (exacerbating the effects associated to stray elements) [Zie18].

Most dominant device parameters affecting current sharing during parallel operation are threshold voltage V_{TH}, on-state resistance R_{on}, current factor K as well as large signal transconductance g_m. However, due to very high switching frequency reachable with SiC power MOSFETs, imbalance of circuit elements can also be responsible for severe current mismatch. Statistical fluctuation of gate driver resistances, source parasitic inductances, or non-symmetrical current path within power module can let the devices experience overcurrent and overvoltage stresses and critical electrothermal (ET) and electromagnetic (EM) behavior. Moreover, the performance gap might change over time since many parameters are affected by the temperature of the device and by its ongoing degradation.

This scenario can drastically impact on the devices reliability and reduce the expected application lifetime. The current trend is focused on a way to overcome these problems by determining derating rules (DRs) to be used in the application design where module with parallel SiC are used. DRs are becoming of a paramount importance to enable SiC technology in a wide range of high-current applications; unfortunately, at present time, there are no generally recognized DRs for SiC MOSFETs. To this purpose, a deep understanding of impact of device and circuit statistical parameters spread on the circuit electrical performances is required. In literature, an increasing number of scientific documents is being published on this topic.

First studies were related to parallel connection of unipolar SiC devices and different techniques to reduce current imbalance [Cui12], [Pef11], [Lim14], [Wan14], [Müt18]. Focus on the power module geometry and parasitic inductances was given in [Hai17] and [Li18], respectively. A detailed point of view on the effect of paralleling SiC MOSFET was reported in [Hor16], [Ish18], [Fab15], [Sad13], [Col15]. Active balancing techniques are discussed in [Xue13], [Xue14] while others rely on passive components [Mao17], [Hui18], [Du14], or layout optimization [Bęc17]. In terms of DRs, in [Ber18], [Ber18b] a criteria for the selection of maximum allowed statistical spread of R_{ON} and V_{TH} has been derived. Further analysis have been conducted to evaluate

robustness of multi-chip parallel solution under both unclamped [Cas18], [Fay18] and clamped [Hu16] inductive transient.

However, all the presented methodologies do not address the evaluation of DRs directly considering the statistical description of device and circuit parameters fluctuation. Therefore, to relate information about the statistical properties of a given manufacturer technology process with DRs needed for a rugged application design, a methodology that takes into account parameters variability [Don19], [Tsu20] is becoming the key approach to develop design guidelines for the safe operation of parallel SiC MOSFETs devices.

Simultaneously, virtual prototyping is also gaining increasing importance in assisting and verifying the design of power modules and converters [Eva16], [Baz20]. To investigate the ET behavior of electronic devices/circuits, various approaches have been proposed in literature. Commonly-adopted strategies rely on the coupling of a SPICE-like circuit simulator and a 3-D thermal-only numerical software package (e.g., COMSOL Multiphysics, ANSYS) in a relaxation procedure [van94], [Wun97], [Cat14]; however, this solution is onerous in terms of CPU time and memory storage, as well as prone to convergence problems. TCAD simulation tools (e.g., Sentaurus, ATLAS) allow simultaneously solving the semiconductor and heat flow equations within the same framework [Bre13], [Arv17]; the huge computational burden required, however, makes their adoption only suitable for device-level simulations. As an alternative to methods based on numerical tools, an inhouse approach based on a fully circuital representation of the whole device/circuit for self-consistent static and dynamic ET simulations with SPICE-like programs has been presented and successfully used for an IGBT-based boost converter [Cat17]; InGaP/GaAs HBT arrays for power amplifiers [dAl21] and, eventually, a SiC MOSFET PM [dAl20]. Considerable efficiency is gained with respect to [van94], [Wun97], [Cat14] since the thermal problem is modelled with an equivalent thermal network derived through an advanced model-order reduction algorithm.

The main research topics of this dissertation are the statistical derivation of easy-to-apply derating rules for the safe implementation of parallel arrays of SiC MOSFETs and the virtual prototyping of power modules and converters based on parallel SiC MOSFETs with unbalanced characteristics. The structure of this thesis, as well as other

research topics relevant to parallel connection of SiC MOSFETs are summarized in Section 1.2

1.2 Thesis Outline

The core of this manuscript is divided into the following chapters, each of which ends with a summary section to provide a quick reference to the corresponding main findings and results.

Chapter 2 presents a compact model SiC power MOSFETs for performing fully-coupled electrothermal simulations entirely within SPICE environment. The equations governing its behavior in different operation domains are detailed and implemented through a SPICE-compatible subcircuit.

In **Chapter 3,** the SiC MOSFET compact model is validated and its parameters are calibrated on target devices with breakdown voltage of 1.2 kV, 3.3 kV and 1.7 kV (the most common voltage classes for SiC MOSFETs currently on the market) to assess both the model accuracy and its scalability. The procedure for calibrating the parameters of the model is also illustrated.

Chapter 4 investigates a type of short-circuit failure that is interesting for the parallel connection of SiC MOSFETs. This failure mode results in a MOSFET with a partial short circuit between gate and source but that still retains the capability of blocking the current between drain and source. Therefore, the failure type is referred to as fail to open (FTO).

The impact of parameters spread on the electrothermal imbalances in parallel SiC MOSFETs is discussed in **Chapter 5.** Several relevant parameters, device- or assembly-related, are considered and, for each of them, the impact on the imbalance of static power dissipation, switching energy, and transient current sharing is studied. Exploiting Monte Carlo simulations, a procedure to derive a trade-off curve between the parameters spread and the temperature imbalance is also developed.

Chapter 6 shows a simulation approach to build virtual prototypes of SiC-based power modules that can be entirely run in a SPICE-like environment. Several case-studies are developed to evaluate the electrothermal imbalance in multichip SiC power modules under realistic operating conditions.

Conclusions are then drawn.

1.3 List of Publications

- M. Riccio, **A. Borghese**, G. Romano, V. d’Alessandro, A. Fayyaz, A. Castellazzi, L. Maresca, G. Breglio, and A. Irace, “Analysis of Device and Circuit Parameters Variability in SiC MOSFETs-Based Multichip Power Module,” 2018. [Online]. Available: https://www.scopus.com/inward/record.uri?eid=2-s2.0-85057005975&partnerID=40&md5=1602372b3901fa7b4b9e62ca133596eb

- **A. Borghese** *et al.*, "Effect of Parameters Variability on the Performance of SiC MOSFET Modules," *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, 2018, pp. 1-5, doi: 10.1109/ESARS-ITEC.2018.8607593.

- M. Riccio, G. Romano, **A. Borghese**, L. Maresca, G. Breglio A. Irace, and G. Longobardi, "Experimental analysis of electro-thermal interaction in normally-off pGaN HEMT devices," *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, 2018, pp. 1-6, doi: 10.1109/ESARS-ITEC.2018.8607347.

- **A Borghese** *et al.*, “An Experimentally Verified 3.3 kV SiC MOSFET Model Suitable for High-Current Modules Design,” in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2019, vol. 2019-May, pp. 215–218. doi: 10.1109/ISPSD.2019.8757576.

- **A. Borghese** *et al.*, "Statistical Analysis of the Electrothermal Imbalances of Mismatched Parallel SiC Power MOSFETs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1527-1538, Sept. 2019, doi: 10.1109/JESTPE.2019.2924735.

- M. Riccio, **A. Borghese**, L. Maresca, G. Breglio and A. Irace, "Fully-Coupled Electrothermal Simulation of Wide-Area Reverse Conducting IGBTs," *2019 25th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2019, pp. 1-4, doi: 10.1109/THERMINIC.2019.8923497.

- L. Maresca, **A. Borghese**, G. Romano, A. Fayyaz, M. Riccio, G. Breglio, A. Castellazzi, and A. Irace, "SiC MOSFETs," in *Modern Power Electronic Devices*, 2020, pp. 259–293. doi: 10.1049/PBPO152E_ch8.

- F. Richardeau F. Boige, A. Castellazzi, V. Chazal, A. Fayyaz, **A. Borghese**, A. Irace, and G. Guibaud, "SiC MOSFETs soft and hard failure modes: Functional analysis and structural characterization," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2020, vol. 2020-September, pp. 170–173. doi: 10.1109/ISPSD46842.2020.9170094.

- **A. Borghese**, M. Riccio, A. Castellazzi, L. Maresca, G. Breglio, and A. Irace, "Statistical Electrothermal Simulation for Lifetime Prediction of Parallel SiC MOSFETs and Modules," in *Proceedings - 2020 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems, IESES 2020*, 2020, pp. 383–386. doi: 10.1109/IESES45645.2020.9210690.

- A. Castellazzi, F. Richardeau, **A. Borghese**, F. Boige, A. Fayyaz, A. Irace, G. Guibaud, and V. Chazal, "Gate-damage accumulation and off-line recovery in SiC power MOSFETs with soft short-circuit failure mode," *Microelectronics Reliability*, vol. 114, 2020, doi: 10.1016/j.microrel.2020.113943.

- **A. Borghese**, M. Riccio, G. Longobardi, L. Maresca, G. Breglio, and A. Irace, "Gate leakage current sensing for in situ temperature monitoring of p-GaN gate HEMTs," *Microelectronics Reliability*, vol. 114, 2020, doi: 10.1016/j.microrel.2020.113762.

- F. Richardeau, **A. Borghese**, A. Castellazzi, A. Irace, V. Chazal, and G. Guibaud, "Effect of gate-source bias voltage and gate-drain

leakage current on the short-circuit performance of FTO-type SiC power MOSFETs," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2021, vol. 2021-May, pp. 255–258. doi: 10.23919/ISPSD50666.2021.9452253.

- C. Scognamillo, A. P. Catalano, **A. Borghese**, M. Riccio, V. d'Alessandro, G. Breglio, A. Irace, R. N. Tripathi, A. Castellazzi, and L. Codecasa, "Electrothermal Modeling, Simulation, and Electromagnetic Characterization of a 3.3 kV SiC MOSFET Power Module," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2021, vol. 2021-May, pp. 123–126. doi: 10.23919/ISPSD50666.2021.9452207.

- **A. Borghese**, M. Riccio, L. Maresca, G. Breglio, and A. Irace, "Gate Driver for p-GaN HEMTs with Real-Time Monitoring Capability of Channel Temperature," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2021, vol. 2021-May, pp. 63–66. doi: 10.23919/ISPSD50666.2021.9452317.

- **A. Borghese**, A. D. Costanzo, M. Riccio, L. Maresca, G. Breglio, and A. Irace, "Gate current in p-GaN gate HEMTs as a channel temperature sensitive parameter: A comparative study between schottky-and ohmic-gate GaN HEMTs," *Energies*, vol. 14, no. 23, 2021, doi: 10.3390/en14238055.

- C. Scognamillo, A. P. Catalano, M. Riccio, V. d'Alessandro, L. Codecasa, **A. Borghese**, R. N. Tripathi, A. Castellazzi, G. Breglio, and A. Irace, "Compact modeling of a 3.3 kV SiC MOSFET power module for detailed circuit-level electrothermal simulations including parasitics," *Energies*, vol. 14, no. 15, 2021, doi: 10.3390/en14154683.

- M. Riccio, **A. Borghese**, V. d'Alessandro, L. Maresca, and A. Irace, "Optimum module design II: impact of parameter design spread," in *SiC Power Module Design: Performance, Robustness and Reliability*, 2021, pp. 107–132.

- **A. Borghese**, A. Di Costanzo, M. Riccio, L. Maresca, G. Breglio, and A. Irace, “Gate Current in p-GaN Gate HEMTs as a Channel Temperature Sensitive Parameter: A Comparative Study between Schottky- and Ohmic-Gate GaN HEMTs,” *Energies*, vol. 14, no. 23, p. 8055, Dec. 2021, doi: 10.3390/en14238055.

Chapter 2

SPICE-Based Electrothermal Compact Model of SiC MOSFET

2.1 State of the Art

In the last years, several papers have focused on the modeling of SiC MOSFETs; a review of the models presented in literature is discussed in [Man15]. Many works start from models developed for Si MOSFETs and improve them with various parameters and empirical functions to reproduce the characteristics of the SiC counterparts [McN07]–[Mer14]. However, models based on an empirical formulation of the device behavior result in an onerous and prone-to-error calibration procedure. Recently, some models have been published with the aim of describing the specific mechanisms occurring in SiC MOSFETs. Effects caused by interface traps, their influence on the threshold voltage and the variation of the electron mobility are considered in [Lic15]. In [Lic15]–[Fu12], the nonlinear drain resistance is also modeled.

Various complicated physical models have been developed for device simulations [Pow07]–[Kra16], but in many cases they are too resource-hungry to be exploited for the analyses of complex circuits. A surface-potential-based model for circuit simulation is proposed in [Nak16]. An analytical temperature-dependent model implemented in PSPICE that covers static and dynamic behavior, leakage current, and breakdown voltage characteristics is proposed in [Joh16]. This model was shown to ensure a favorable matching of the R_{ON} at different temperatures, as well as of the low-current static avalanche I–V characteristic, but its accuracy in describing the pinch-off behavior and high-temperature out- of-safe-operating-area (SOA) conditions was not validated. In addition, like other physical models, it is based on many parameters that are unknown to the users, thus leading to a cumbersome

and painstakingly onerous calibration procedure. Although several models have been proposed in the last ten years, a validated SPICE model suitable for SiC power MOSFETs under extreme operating conditions, where very high temperatures are reached, is still missing in the literature.

In this Chapter, starting from a first attempt proposed in [dAl14], an accurate, yet simple enough, physics-based model is conceived and developed, which is associated to a straightforward parameter extraction methodology. The proposed model is oriented to ET simulation in real applications (e.g., power converters) with the possibility to enable physical phenomena occurring close to the device failure. The model extends the version in [dAl14] by including:

1) improved formulations for the nonlinear bias-dependent components of the drain resistance and for threshold voltage;
2) the thermally generated leakage current;
3) the parasitic npn transistor;
4) the nonlinear C_{DS} and C_{GD} capacitances;
5) the mobility degradation dictated by high electric fields.

The model presented in this Chapter is suited to cover a wider temperature range and is validated through comparison with static and dynamic experimental data, even during out-of-SOA operation (avalanche and short-circuit -SC- conditions). The model is implemented as a subcircuit fully compatible with most commercial SPICE-like software suites and can be solved by their powerful engines with low computational effort. An equivalent electrical network can be coupled to the circuit to account for the dynamic heat propagation. Consequently, it is easy to monitor the evolution of the MOSFET temperature, as well as of the temperature-sensitive parameters.

2.2 Model Equations

The proposed model is based on the partitioning of the device into an “intrinsic” conventional MOSFET, which describes the channel region, a bias-dependent resistance for the accumulation and JFET regions, and a constant resistance for the epitaxial lightly doped drift region (also referred to as epilayer in the following). All the physical quantities are temperature dependent; in the following, the temperature of the transistor (assumed uniform within the whole device) and the

reference temperature (300 K) will be referred to as T and T_0, respectively. The drain resistance is modeled with the series of two non-linear resistors according to the following expression:

$$R_D(V_{GS}, V_{\mathrm{drift}}, T) = R_{AJ}(V_{GS}, V_{\mathrm{drift}}, T) + R_{\mathrm{EPI}}(T) \tag{2.1}$$

where

$$R_{AJ}(V_{GS}, V_{\mathrm{drift}}, T) = \frac{V_{\mathrm{drift}}}{V_1 + V_{\mathrm{drift}}} \cdot \left[R_{AJ1}(T) + R_{AJ2}(T)\left(1 + \frac{V_{GS}}{V_2}\right)^{-\eta}\right]. \tag{2.2}$$

The bias-insensitive R_{EPI} describes the resistive contribution of the epilayer, while R_{AJ} accounts for the current path through the accumulation and JFET regions [Bal10]. $V_{drift} = V_{DS} - V_{ch}$ is the voltage drop across R_D, V_{ch} being the drop across the channel, while V_1, V_2, and η are fitting parameters. This formulation improves the one reported in [dAl14] in the high-current triode region and is derived on the basis of simple arguments. First, the resistance of the accumulation region reduces with gate voltage due to the increased concentration of attracted electrons; second, under high V_{drift} values, the high electric field occurring in the JFET region tends to saturate the electron velocity, thus degrading the mobility.

The temperature dependences are modeled by the following expressions:

$$R_{\mathrm{EPI}}(T) = R_{\mathrm{EPI0}}\left(\frac{T}{T_0}\right)^{r_0} \tag{2.3}$$

$$R_{AJ1}(T) = R_{AJ10}\left(\frac{T}{T_0}\right)^{r_1} \tag{2.4}$$

$$R_{AJ2}(T) = R_{AJ20}\left(\frac{T}{T_0}\right)^{r_2}. \tag{2.5}$$

R_{EPI0}, R_{AJ10}, R_{AJ20}, r_0, r_1, and r_2 being fitting parameters. These dependences are found to ensure a good alignment between model and

measurements up to about 500 K. To extend the model validity to higher temperatures with respect to [dAl14], a slight modification of the above formulations is required, which can be explained as follows. As discussed in [Reg00] and [Reg02], the following expression can be used to describe the temperature dependence of the "bulk" electron mobility even for T > 500 K:

$$\mu_L(T) = \mu_{L0}\left(\frac{T}{300}\right)^{-r+\frac{\alpha T}{300}}. \tag{2.6}$$

Therefore, the exponents in (2.3)–(2.5) become

$$r_i(T) = r_i - \alpha_i \frac{T}{300}. \tag{2.7}$$

The threshold voltage (V_{TH}) in SiC MOSFETs exhibits a strong temperature dependence for low-temperature values that can be attributed to the very high density of states located at the SiO_2/SiC interface [Mat08]. It has been reported that the interface states distribution within the bandgap increases exponentially towards the conduction band edge. As the temperature increases, less interface states are occupied [Zha13], thus leading to more electrons in the depletion region. This effect could allow for stable operation at high temperatures where the I_D increase caused by the V_{TH} shift can be compensated by the reduced carrier mobility. The V_{TH} reduction with temperature was described with the classical linear law in [dAl14], while in [Ung16] a piecewise linear function was proposed. However, the latter approach suffers from a discontinuity that can lead to convergence issues in a SPICE implementation. Therefore, the following exponential analytical expression was introduced:

$$V_{TH}(T) = [V_{TH}(T_0) - \beta_{TH}]e^{-\varphi_{TH}(T-T_0)} + \beta_{TH} \tag{2.8}$$

where the temperature coefficient φ_{TH} and the voltage β_{TH} are fitting parameters.

To model the temperature dependence of the electron channel mobility μ_n, many physical concurrent phenomena must be considered.

For low-temperature values, μ_n exhibits a weak positive temperature coefficient (PTC), whereas a negative temperature coefficient (NTC) takes place at high temperature. This can be directly attributed to the presence of interface traps [Per06], [Che12]. The temperature coefficient of μ_n in a SiC power MOSFET is indeed the result of an interplay between 1) the Coulomb scattering with the filled traps, leading to a PTC induced by the trap discharging with increasing temperature; and 2) the acoustic-phonon scattering yielding an NTC, where 1 and 2 prevail at low and high temperatures, respectively. In the proposed model, such a behavior is accurately described through the power relationship shown in (2.9), where the exponent m is temperature dependent

$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{-m(T)}. \tag{2.9}$$

Parameter m(T), usually considered positive and temperature independent for Si MOSFETs that are not subject to mechanism 1, is modeled with the following expression:

$$m(T) = -a_m + (a_m + b_m)\left[1 - c_m \exp\left(-d_m \frac{T}{T_0}\right)\right] \tag{2.10}$$

with a_m, b_m, c_m, and d_m being fitting parameters.

Impact-ionization (II) effects are activated by multiplying the II-unaffected drain current by the avalanche factor [Rin06]

$$M = 1 + a_{II} \tan\left\{f_I(I_D)\frac{\pi}{2}\left[\frac{V_{DS}}{BV_{DS}(T)}\right]^{b_{II}}\right\}. \tag{2.11}$$

The breakdown voltage BV_{DS} and the f_I term are given by

$$\begin{gathered} BV_{DS}(T) = BV_{DS0} \exp\left[c_{II}(T - T_0)\right] \\ f_I(I_D) = 1 - b_{AV} I_D \end{gathered} \tag{2.12}$$

where f_I is a nondimensional term needed to account for the current dependence of M; a_{II}, b_{II}, and c_{II} are fitting parameters.

The thermally generated leakage current I_{Therm} is modeled with the current contribution associated to the drain-body junction, which is reverse biased. I_{Therm} can be then expressed with the following equation [Fil13]:

$$I_{\text{Therm}} = \frac{qW_D n_i}{\tau_H} + qn_i^2 f(N_D, N_A). \quad (2.13)$$

In (2.13), it is possible to identify two terms: in the first (drift) term, W_D and τ_H are the depletion layer width and the carrier generation lifetime in the depletion region of the collector–base junction, respectively. In the second (diffusion) term, f describes an involved function defining the diffusion components of the electrons and holes based on acceptor N_A and donor N_D concentrations, on the carrier lifetime of holes τ_p and electrons τ_n, as well as on the diffusivity of holes D_p and electrons D_n. Moreover, for 4H-SiC, the intrinsic carrier concentration is given by [Bal05]

$$n_i(T) = 1.7 \times 10^{16} T^{\frac{3}{2}} e^{\left(2.08 \times \frac{10^4}{T}\right)}. \quad (2.14)$$

Using (2.12) and (2.13), the following simplified equation is adopted in the proposed model:

$$I_{\text{Therm}} = A_{\text{Therm}}\, n_i(T)^{\alpha_{\text{Therm}}} \quad (2.15)$$

where A_{Therm} and α_{Therm} are fitting parameters. The dynamic behavior of the MOSFET model is described with three parasitic capacitances, namely, C_{GS}, C_{GD}, and C_{DS}. As discussed in detail in [Che15], these capacitances have considerable impact on the transient characteristics during the switching process. However, it has been proved that the nonlinearity of C_{GS} plays a minor role, especially for positive gate voltage, so that it can be reasonably considered constant [Ren06]. Conversely, experiments show that there will be a significant deviation between simulation and actual device switching behavior if C_{DS} and C_{GD} are assumed constant. Differently from [dAl14], where the

embedded formulations were exploited, in the proposed model these nonlinear capacitances are expressed as

$$C_{DS}(V_{ds}) = \frac{C_{DS0}\left[\frac{\pi}{2} + \arctan\left(-\frac{V_{ds}}{V_{ds}^{*}}\right)\right]}{\pi/2} + C_{DSMIN} \tag{2.16}$$

$$C_{GD}\left(V_{gd}\right) = \left(C_{GD0} - C_{GDMIN}\right)\left[1 + \frac{2}{\pi}\arctan\left(\frac{V_{gd}}{V_{gd}^{*}}\right)\right] + C_{GDMIN}. \tag{2.17}$$

The voltage-dependent behavior of C_{DS} was modeled with the function reported in (2.16) for $V_{ds} > 0$ V, while it is kept constant for $V_{ds} < 0$ V [Gra89]. Similarly, for $V_{gd} < 0$ V the C_{GD} capacitance asymptotically decreases down to a minimum value C_{GDMIN} according to (2.17), while for $V_{gd} \geq 0$ V it is equal to C_{GD0} [Ric17]. Parameters V_{ds}^{*} and V_{gd}^{*} are used to fit experimental data for different switching voltages.

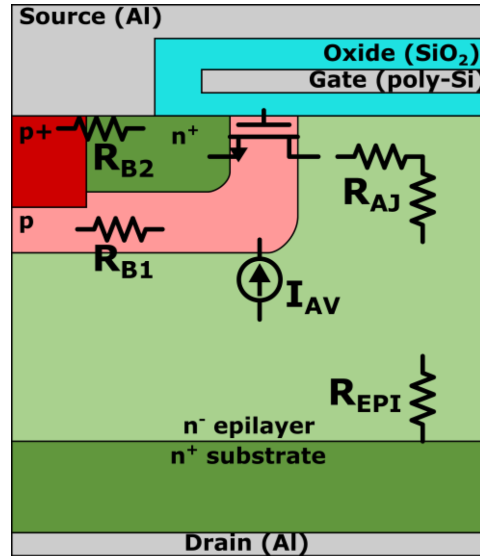


Fig. 2.1 Structure of the SiC power MOSFET and main equivalent circuit components.

2.3 Subcircuit

The schematic structure of a basic SiC VDMOS is shown in Fig. 2.1. In this picture, the most relevant equivalent circuit elements are illustrated for the different device regions. A sketch of the implemented subcircuit is represented in Fig. 2.2. In addition to the electrical terminals (drain, source, and gate), the subcircuit receives as an input the device temperature T, evaluated by the equivalent thermal network, and the reference temperature T_0. It is worth noticing that the proposed implementation can in principle be applied to any power MOSFETs regardless of technology, provided that the equations and/or parameter values included through the additional components are properly modified. A behavioral voltage-controlled voltage source, denoted as ΔV_{TH}, is connected in series with the intrinsic gate terminal to activate the temperature-induced V_{TH} reduction described by (2.18). The controlling voltage is the difference between the nodal voltages representing T and T_0, while the outcome is the V_{TH} variation given by

$$\Delta V_{TH} = (V_{TH0} - \beta_{TH}) e^{-\varphi_{TH}(T-T_0)} - \beta_{TH} + V_{TH0}. \qquad (2.18)$$

In this way, a proper voltage is added to the external gate voltage, leading to the desired temperature-dependent overdrive voltage given by

$$V_{G'S} - V_{TH0} = V_G + \Delta V_{TH} - V_S - V_{TH0} = V_{GS} - V_{TH}(T). \qquad (2.19)$$

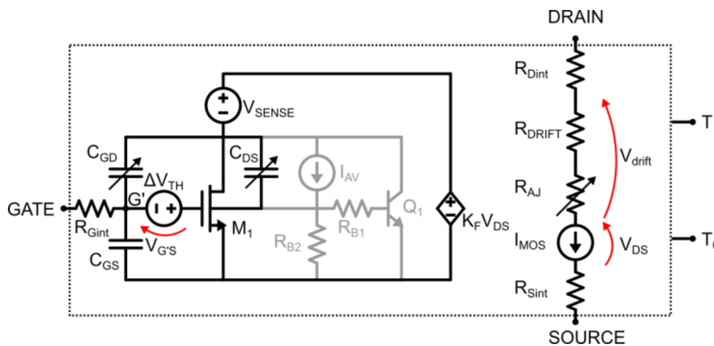


Fig. 2.2 Developed SPICE subcircuit, with electrical and thermal nodes. The elements in gray are needed to model the out-of-SOA operation.

The total MOSFET output current I_{MOS} is evaluated starting from the current of the zero-voltage source V_{SENSE} used as a current monitor. The term $I(V_{SENSE})$ includes the current of the MOSFET M_1, the currents through the capacitances, the thermally generated leakage current, the avalanche-induced current, and the current through Q_1. Then, the complete expression for I_{MOS}, valid for both linear and saturation regions, is given by

$$I_{\mathrm{MOS}} = \frac{I(V_{\mathrm{SENSE}}) \cdot f_\mu(T)}{\{1 + \theta_1[V_{GS} - V_{TH}(T)]\}(1 + \theta_2 \cdot V_{DS})}(1 + \lambda \cdot V_{DS}) \qquad (2.20)$$

where f_μ being a function accounting for the temperature dependence of the electron mobility in the channel

$$f_\mu(T) = \left(\frac{T}{T_0}\right)^{-m(T)}. \qquad (2.21)$$

Expression (2.20) of the MOSFET current includes the reduction in channel mobility due to the high transverse electric field dictated by high gate voltages through parameter θ_1. This results in a linear increase in the saturation current with $V_{GS} - V_{TH}$, instead of the classical quadratic function [Ric17]. The bias-independent λ parameter accounts for the channel modulation effect. In order to include the impact of the nonuniform channel doping density on the current, two different current factors have to be adopted for the linear and saturation regions, respectively. To implement this effect into SPICE, a parameter K_F is multiplied by V_{DS}, as reported in [Ric17]. The effect of the carriers velocity saturation at high V_{DS} (high parallel electric field) is modeled with parameter θ_2 [Tsi87]. Avalanche effects are included by adding a behavioral current source I_{AV} with the following expression:

$$I_{AV} = (M - 1)I_{D(M_1)} + M \cdot I_{\mathrm{Therm}} \qquad (2.22)$$

where $I_D(M_1)$ is the II-unaffected drain current, M is given by (2.11), and I_{Therm} accounts for the thermally generated leakage current.

A network is also added to account for the parasitic npn BJT formed by the body, source, and drift regions, which represent the base, emitter, and collector, respectively. The potential difference between base and emitter depends on two resistors: R_{B1} and R_{B2}. The presence of the parasitic BJT improves the model in [dAl14] and allows the modeling of a possible failure during out-of-SOA operation (as an example, during avalanche conditions, the BJT activation can be triggered if the I_{AV} current induces a sufficient voltage drop across the device internal base resistance).
Table 1 provides a summary of all the parameters on which the SiC MOSFET compact model is based.

2.4 Summary

In this Chapter, a temperature-dependent model for SiC power MOSFETs has been presented. The equations governing its behavior in different operation domains have been detailed. Specifically, the model describes the device operation in DC, transient and the out-of-SOA conditions, as well as the performance variation with the temperature. The influence of SiO_2/SiC interface traps on threshold voltage and channel mobility, the dependence on biasing of the drain resistance, impact ionization, and capacitance nonlinearity are some of the main physical phenomena that have been accounted for. The model has been implemented as SPICE-compatible subcircuit that includes a standard MOSFET, additional resistors, controlled capacitors, and controlled nonlinear sources to describe specific physical mechanisms and temperature dependences. This allows to perform fully-coupled electrothermal simulations entirely within SPICE environment, thus enabling the thermal aware design of circuits and power modules based on SiC MOSFETs.

TABLE 1 LIST OF PARAMETERS OF THE SIC MOSFET COMPACT MODEL

Symbol	Quantity	Type
K0	Current factor	Measurable
V_{TH0}	Zero-bias threshold voltage	Measurable
Θ_1	Transverse electric field factor	Fitting
Θ_2	Parallel electric field factor	Fitting
λ	Channel-length modulation factor	Measurable
K_F	Nonuniform channel doping factor	Measurable
R_{AJ10}	R_{AJ1} at reference temperature T_0	Fitting
R_{AJ20}	R_{AJ2} at reference temperature T_0	Fitting
R_{EPI0}	R_{EPI} at reference temperature T_0	Fitting
V_1	Drain resistance parameter	Fitting
V_2	Drain resistance parameter	Fitting
η	Drain resistance coefficient	Fitting
BV_{DS0}	V_{ds} breakdown voltage at low current	Measurable
b_{II}	Multiplication factor coefficient	Fitting
C_{GD0}	Zero-bias gate-to-drain capacitance	Measurable
C_{GDMIN}	Minimum gate-to-drain reverse-biased capacitance	Measurable
V_{gd}^*	Gate-to-drain capacitance parameter	Fitting
C_{DS0}	Zero-bias drain-to-source capacitance	Measurable
C_{DSMIN}	Minimum gate-to-drain reverse-biased capacitance	Measurable
V_{ds}^*	Drain-to-source capacitance parameter	Fitting
C_{GS}	Gate-to-source capacitance	Measurable
a_m	μ_n temperature parameter	Fitting
b_m	μ_n temperature parameter	Fitting
c_m	μ_n temperature parameter	Fitting
d_m	μ_n temperature parameter	Fitting
ϕ_{TH}	V_{TH} temperature coefficient	Fitting
β_{TH}	V_{TH} temperature parameter	Fitting
r_0	R_{EPI} temperature coefficient	Fitting
r_1	R_{AJ1} temperature coefficient	Fitting
r_2	R_{AJ2} temperature coefficient	Fitting
c_{II}	BV temperature coefficient	Fitting
b_{AV}	BV current coefficient	Fitting
A_{therm}	I_{therm} parameter	Fitting
α_{therm}	I_{therm} parameter	Fitting
α_i	μ_n temperature coefficient	Fitting

Chapter 3

Validation of SiC MOSFET Model

In this Chapter, the model static and dynamic ET performance are compared against the experimental curves of several SiC MOSFETs. Specifically, the parameters of the model were calibrated on target devices with breakdown voltage of 1.2 kV, 3.3 kV and 1.7 kV. These are the most common voltage classes for SiC MOSFETs currently on the market and therefore constitute a representative test bench. First, the procedure developed for calibrating the parameters of the model is illustrated. Successively, the model predictions are presented for both the 1.2-kV and the 3.3-kV devices. For the 1.2-kV MOSFET under test, the out-of-SOA behavior of the model was also verified. Eventually, a slightly modified and improved version of the model is presented with the results for the 1.7-kV devices.

3.1 Model Calibration Procedure

In this section, the procedure to calibrate the model parameters is described. The complete model with all the temperature dependences is based on 37 parameters, some of which have a physical meaning and can be directly extracted from measured data. However, depending on the application of the model and the required accuracy, a subset of parameters can be excluded (e.g., if the description of the parasitic npn BJT is not required, the related four parameters are unnecessary). The device under test (DUT) used in this section is a 1.2 kV–36 A (at $T = T_0$) 4H-SiC power MOSFET, part number C2M0080120D, manufactured by Wolfspeed [Link5]. The MOSFET current factor K and threshold voltage V_{TH} were directly extracted from the highest-slope portion (medium V_{GS}) of the isothermal I_D−V_{GS} transfer characteristics measured at various baseplate temperatures using the quadratic extrapolation method (QEM) [Bal87], [Aro07], [Swa16]. It is worth clarifying the meaning that V_{TH} and K have in this context. The

LEVEL-1 MOSFET (M1) placed in the subcircuit of Fig. 2.2 is governed by the Shichman-Hodges model [Shi68], therefore, the parameters K and V_{TH} are those featuring in the expression (3.1) of the drain current. K is sometimes referred to as MOSFET transconductance.

$$\begin{cases} I_D = \underbrace{\mu C_{ox}\frac{W}{L}}_{K}\left[(V_{GS}-V_{TH})V_{DS}-\frac{1}{2}V_{DS}^2\right], \begin{cases} V_{GS} > V_{TH} \\ V_{DS} < V_{GS}-V_{TH} \end{cases} \\ I_D = \frac{1}{2}\mu \underbrace{C_{ox}\frac{W}{L}}_{K}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}), \begin{cases} V_{GS} > V_{TH} \\ V_{DS} > V_{GS}-V_{TH} \end{cases} \end{cases} \tag{3.1}$$

The parameters in (2.8) needed to model the temperature dependence of the threshold voltage can be evaluated from the best-fit procedure of the extracted values. Moreover, since the temperature dependence of factor K is only attributed to the electron mobility, the extracted K values were used to calibrate the parameters of exponent (2.10) employed in (2.21).

In Fig. 3.1, the extracted current factor K normalized to the value at T_0 is shown as a function of temperature, along with the model with optimized parameters. Fig. 3.2 reports the threshold voltage against temperature. It can be inferred that the QEM technique leads to high values for $V_{TH}(T_0)$ (5.05 V) and φ_{TH} (4.12 mV/K) compared to similarly rated Si power power switches. Both findings were attributed to the high density of SiO_2/SiC interface traps [Wan08], [Che13]. The fast V_{TH} reduction with temperature - due to the emission of inversion electrons from the traps - entails a severe PTC for I_D, which in turn exacerbates the ET feedback [Ric13].

Moreover, the $V_{TH}(T_0)$ value obtained with the QEM is rather higher than that reported on the device datasheet (2.6 V), which is evaluated with the constant current method with $V_{GS} = V_{DS}$ at the reference $I_D = 5$ mA. However, in the proposed model, the main element is the standard LEVEL-1 component M_1 (see Fig. 2.2) and the correct value to be used for the threshold voltage parameter [V_{TH0} in (2.18) and (2.19)] is the one obtained by QEM. As evidence of the accuracy of the $V_{TH}(T)$ expression at very high temperatures, Fig. 3.2 also reports the favorable match with experimental data from [Ung16].

Parameter λ was extracted from an isothermal I_D-V_{DS} curve at low V_{GS} (e.g., 7–8 V) in the pinch-off region ($V_{DS} >> V_{GS} - V_{TH}$).

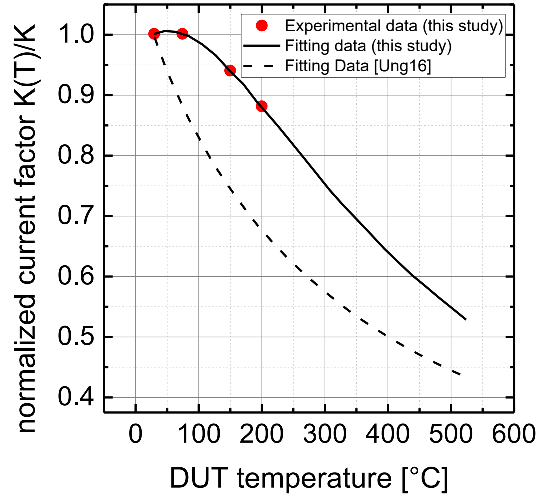


Fig. 3.1 Normalized MOSFET transconductance as a function of temperature. Circles are data extracted from isothermal I_D-V_{GS} curves, the dashed line corresponds to a typical Si power law, while the continuous line is the new model fitted on experimental data.

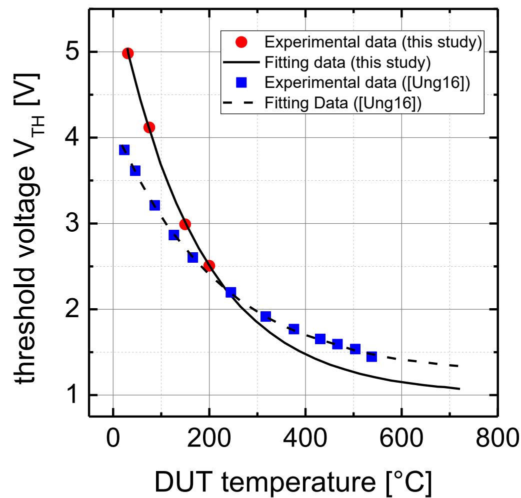


Fig. 3.2 Threshold voltage as a function of the temperature. Solid line and circles refer to the DUT analyzed in this study. Dashed line and squares refer to the data extracted from [Ung16].

The nonlinear drain resistances (R_{AJ}, R_{EPI}) in (2.1) and (2.2), together with parameters θ_1 and K_F, were determined comparing the model with: 1) isothermal I_D-V_{DS} output characteristics for different V_{GS}; and 2) the transfer characteristic at fixed $V_{DS} = 20$ V. More specifically, an automatic multistep calibration routine was implemented using the MATLAB Optimization Toolbox [Man1]. A flowchart depicting the calibration routine is sketched in Fig. 3.3.

In the first step, the procedure evaluates six parameters minimizing the error between the simulated and measured I_D-V_{GS} curve at ambient temperature: R_{EPI0}, R_{J10}, R_{J20}, V_2, θ_1, and η. Afterwards, using the numerical and experimental output curves I_D-V_{DS} at the reference temperature T_0, parameters K_F and V_1 are determined with the best-fit procedure.

Finally, with the I_D-V_{DS} at higher temperature (in this case $T = 470$ K) the automatic procedure determines parameters r_0, r_1 and r_2.

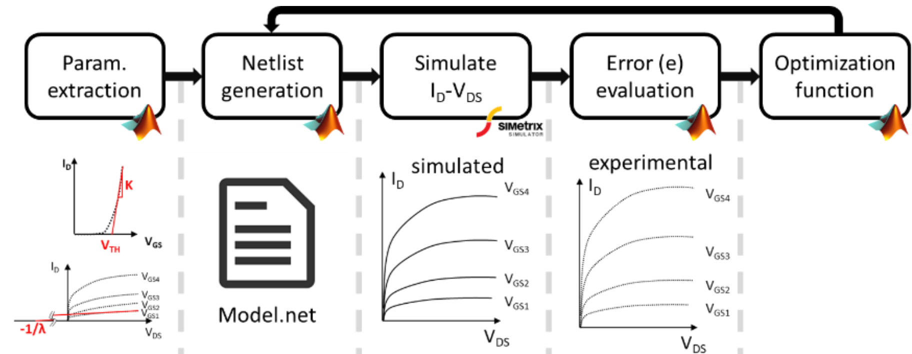


Fig. 3.3 Flowchart of the automatic routine for the optimization the parameters and the calibration of the static curves.

The parameters involved in the expression of the capacitances were tailored to match the experimental gate and drain voltage waveforms during an inductive load switching (ILS) turn-off and turn-on transient operated at different supply voltages. The starting guess values for the optimization procedure were extracted from the C–V curves reported on the DUT datasheet. The remaining parameters, used to model additional effects, were calibrated to favorably match experimental data during out-of-SOA operation. Parameter θ_2 is used to fit the drain peak current during SC operation (very high V_{DS}).

TABLE 2 CALIBRATED MODEL PARAMETERS

Symbol	Quantity	Value
K0	Current factor	1.01 A/V^2
V_{TH0}	Zero-bias threshold voltage	5.05 V
Θ_1	Transverse electric field factor	0.01 V^{-1}
Θ_2	Parallel electric field factor	0.014 V^{-1}
λ	Channel-length modulation factor	0.046 V^{-1}
K_F	Nonuniform channel doping factor	0.846
R_{AJ10}	R_{AJ1} at reference temperature T_0	0.18 Ω
R_{AJ20}	R_{AJ2} at reference temperature T_0	0.57 Ω
R_{EPI0}	R_{EPI} at reference temperature T_0	7.7 mΩ
V_1	Drain resistance parameter	10.75 V
V_2	Drain resistance parameter	0.074 V
η	Drain resistance coefficient	1.88
BV_{DS0}	V_{ds} breakdown voltage at low current	1642 V
b_{II}	Multiplication factor coefficient	4
C_{GD0}	Zero-bias gate-to-drain capacitance	0.6 nF
C_{GDMIN}	Minimum gate-to-drain reverse-biased capacitance	0.01 nF
V_{gd}^*	Gate-to-drain capacitance parameter	2.0 V
C_{DS0}	Zero-bias drain-to-source capacitance	2 nF
C_{DSMIN}	Minimum gate-to-drain reverse-biased capacitance	0.06 nF
V_{ds}^*	Drain-to-source capacitance parameter	10 V
C_{GS}	Gate-to-source capacitance	1.05 nF
a_m	μ_n temperature parameter	1.12
b_m	μ_n temperature parameter	0.86
c_m	μ_n temperature parameter	1.34
d_m	μ_n temperature parameter	0.96
ϕ_{TH}	V_{TH} temperature coefficient	5.34 mK^{-1}
β_{TH}	V_{TH} temperature parameter	0.85 V
r_0	R_{EPI} temperature coefficient	5.02
r_1	R_{AJ1} temperature coefficient	4.34
r_2	R_{AJ2} temperature coefficient	0.34
c_{II}	BV temperature coefficient	0.22 mK^{-1}
b_{AV}	BV current coefficient	−0.1 mA^{-1}
A_{therm}	I_{therm} parameter	18×10^{-9}
α_{therm}	I_{therm} parameter	0.65
α_i	μ_n temperature coefficient	0.1

In a similar fashion, the avalanche multiplication factor was tailored using the experimental waveforms obtained during an unclamped inductive switching (UIS) experiment. Furthermore, the parameters in (2.15) used to model the leakage current were calibrated using 2-D-TCAD simulations up to very high temperature (T = 2000 K). The temperature coefficients in (2.7) can be optimized to ensure the best agreement with the current drain waveform during the SC test, when the temperature increase exceeds 500 K. All the model parameters corresponding to the DUT are reported in Table 2.

3.2 Model Validation for 1.2 kV Devices

The proposed model was validated comparing SPICE simulation results with experiments; in this section, a broad set of results is reported, with a focus on harsh working conditions where a large amount of energy is dissipated by the device causing high ET stress. All simulations were performed within the environment of the tool SIMetrix [Man2]; nonetheless, the model can be used in any SPICE simulator as a standard sub-circuit.

3.2.1 Validation of the DC Behavior

Isothermal measurements of I-V characteristics of the DUT were performed by means of an in-house 250-A-rated curve tracer suited to supply down to 1-μs-wide current pulses, the device baseplate being set to assigned temperatures T through the thermochuck. In Fig. 3.4, the experimental I_D-V_{GS} curves at $T = T_0$ and T = 470 K are compared to simulation results. I_D-V_{GS} characteristics derived with the model version in [dAl14] are also reported. The calibrated SPICE model can predict with a high accuracy the device behavior for a wide range of V_{GS}, including the transition of the drain current from the standard quadratic region to a sublinear region. It is worth noticing that the improved description of the drain resistance with respect to [dAl14] allows extending the validity range of the model also in the high-current triode region. Figs. 3.5 and 3.6 depict the output curve family at $T = T_0$ and T = 470 K, respectively. In addition, in this case, it is evident how the model can describe with high accuracy the device behavior,

including the gradual transition from linear to saturation region, typical of SiC power MOSFETs.

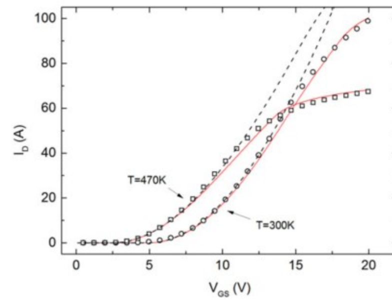


Fig. 3.4 Transfer characteristics under isothermal conditions, at T = T_0 = 300 K and T = 470 K. Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT analyzed in this Section; dashed lines correspond to the curves obtained with the previous model version presented in [dAl14].

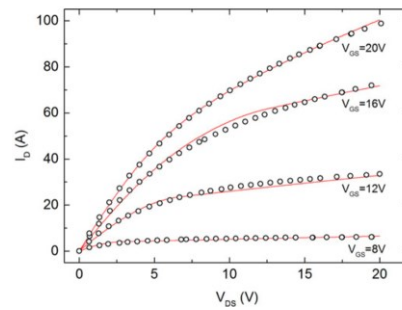


Fig. 3.5 MOSFET output characteristics at T = T_0. Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT.

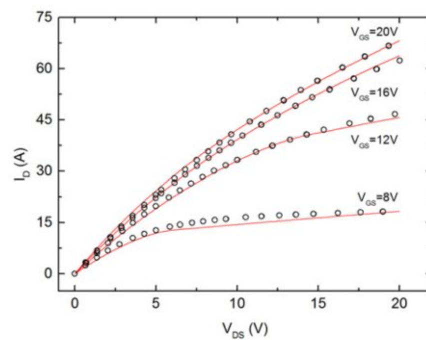


Fig. 3.6 MOSFET output characteristics at T = 470 K. Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT.

3.2.2 Validation of the Transient Behavior

To investigate the device switching behavior, a half-bridge converter board has been used as test circuit (see Fig. 3.7) configured to operate as a standard ILS test [Ros09]. The DUT was placed as low-side switch of the half bridge, while the high side was replaced by an inductive load of 1.9 mH with a 1.2 kV SiC Schottky diode connected in parallel (freewheeling diode). An Agilent waveform generator (33220A) provided the logic signal to the DUT driver (IXYS IXDD609SI). The driving circuit (optically isolated) was designed to supply adjustable ON-state and OFF-state voltages, set to + 20 V and – 6 V for this experiment. A current transformer was used to measure the drain current. The turn-on and turn-off dynamics of the SiC MOSFET were obtained with double-pulse tests. In the simulated circuit, the parasitic inductances of the device packages and the connections between the circuit components, as well as the parasitic capacitance of the inductive load, are taken into account. The gate drive is represented with a pulsed voltage source and a gate resistor. For the Schottky diode, a model provided by Wolfspeed was used [Link5]. Fig. 3.8 shows the waveforms of gate-source voltage, drain–source voltage, and drain current, which were obtained by measurements and by simulations of turn-on and turn-off of the SiC-MOSFET during a double-pulse test operated at a drain current of 26 A and T_0.

The main test parameters are as follows: supply voltage of 500 V, drain stray inductance equal to 200 nH, bipolar gate driver – 6 V/+ 20 V [Ric14], rise-time and fall-time of the driving gate signal of 100 ns, first pulse duration of 99 μs (conduction time before turn-off transient), second pulse after 20 μs (off-state before turn-on transient). Good agreement between simulation and measurements is achieved: the model fittingly predicts the drain voltage overshoot (~580 V), and the drain current and voltage slopes.

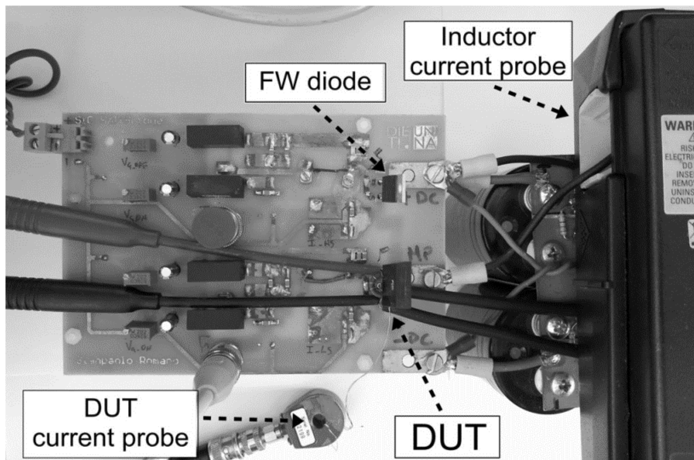
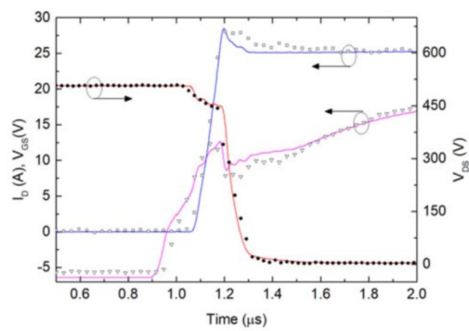
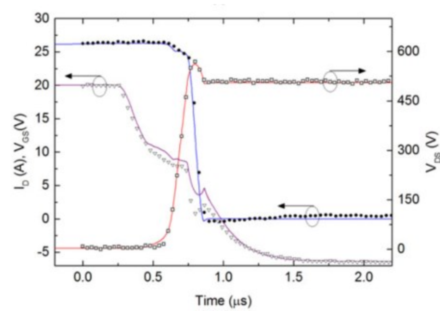


Fig. 3.7 Circuit used to evaluate the DUT switching waveforms.



(a)



(b)

Fig. 3.8 Inductive switching waveforms (I_D, V_{DS}, V_{GS}): (a) turn on and (b) turn off. Solid lines are SPICE numerical results; symbols refer to the experiment.

3.2.3 Validation on Parallel Devices

As anticipated in the introduction, connecting transistors in parallel might result in uneven current sharing, i.e., the non-uniform current partition in the considered parallel configuration. In other words, the transistors might not equally split the load current due to inevitable differences in their performance caused by fabrication fluctuations and asymmetric circuit design. Such an unbalanced current distribution can either happen when there is a continuous current flow (referred to as uneven static current sharing) or during a commutation phase (referred to as uneven transient current sharing). In principle, both events have a decisive impact on the power consumption, as this can also be divided into static and dynamic power loss.

Some measurements were performed on two parallel 1.2 kV SiC MOSFETs under double pulse test (DPT) with a load inductor of 50 µH and for different values of supply voltage - V_{DC} - (300 V and 400 V). The resulting experimental waveforms highlight that during both the turn-off (Figs. 3.9a, 3.9c) and turn-on phases (Figs. 3.9b, 3.9d) the devices conduct significantly different currents.

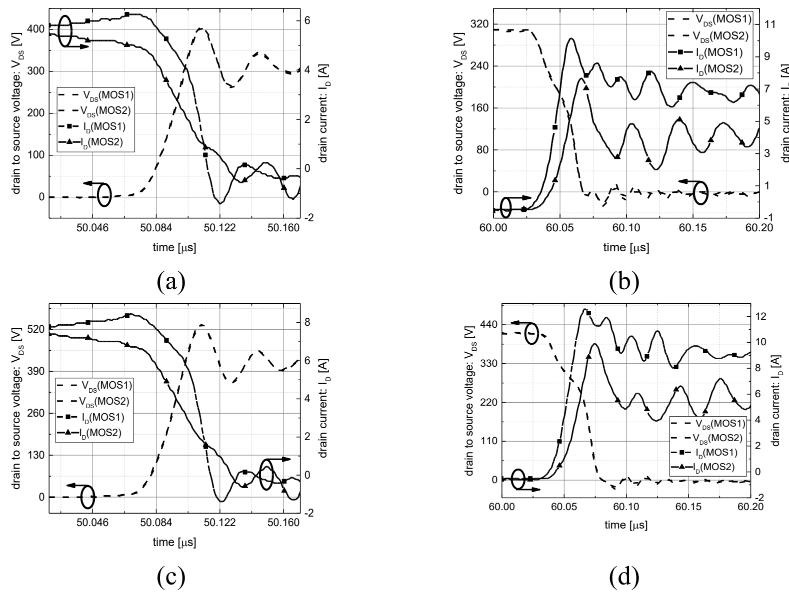


Fig. 3.9 Experimental switching waveforms (I_D, V_{DS}) of two parallel SiC MOSFETs under DPT at 25°C with L_{LOAD}=50 µH; (a) turn-off and (b) turn-on at $V_{DC} \approx 300$ V and $I_{LOAD} \approx 11$ A; (c) turn-off and (d) turn-on at $V_{DC} \approx 400$ V and $I_{LOAD} \approx 14$ A.

Since one of the objectives of this dissertation is to assist the design of parallel configuration of SiC MOSFETs through compact electrothermal simulations, it is of paramount importance to verify that the model presented in Chapter 2 can accurately predict the dissipation imbalance. Therefore, the current and voltage waveforms of an experimental turn-off of two parallel SiC MOSFETs (same DUTs presented in Section 3.1) were used to assess the validity of the model for reproducing the current imbalance.

TABLE 3 COMPARISON BETWEEN THE EXPERIMENTAL AND SIMULATED DISSIPATED SWITCHING ENERGY.

	MOSFET$_1$	**MOSFET$_2$**
Simulation	153.1 μJ	131.8 μJ
Experiment	141.5 μJ	115.05 μJ

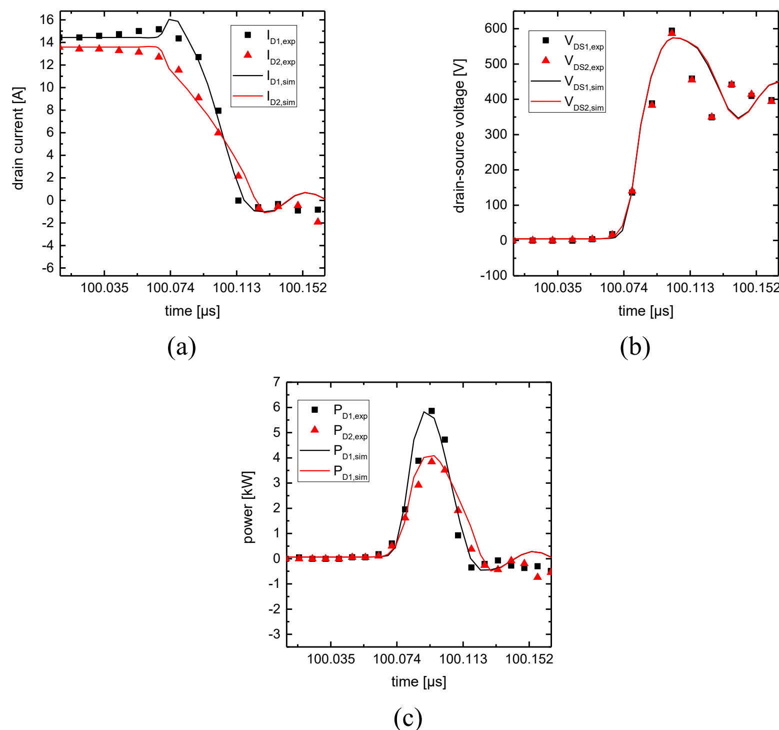


Fig. 3.10 Comparison between the experimental (symbols) and simulated (lines) waveforms of an inductive turn-off of two parallel MOSFETs; (a) drain current, (b) drain-source voltage and (c) dissipated power.

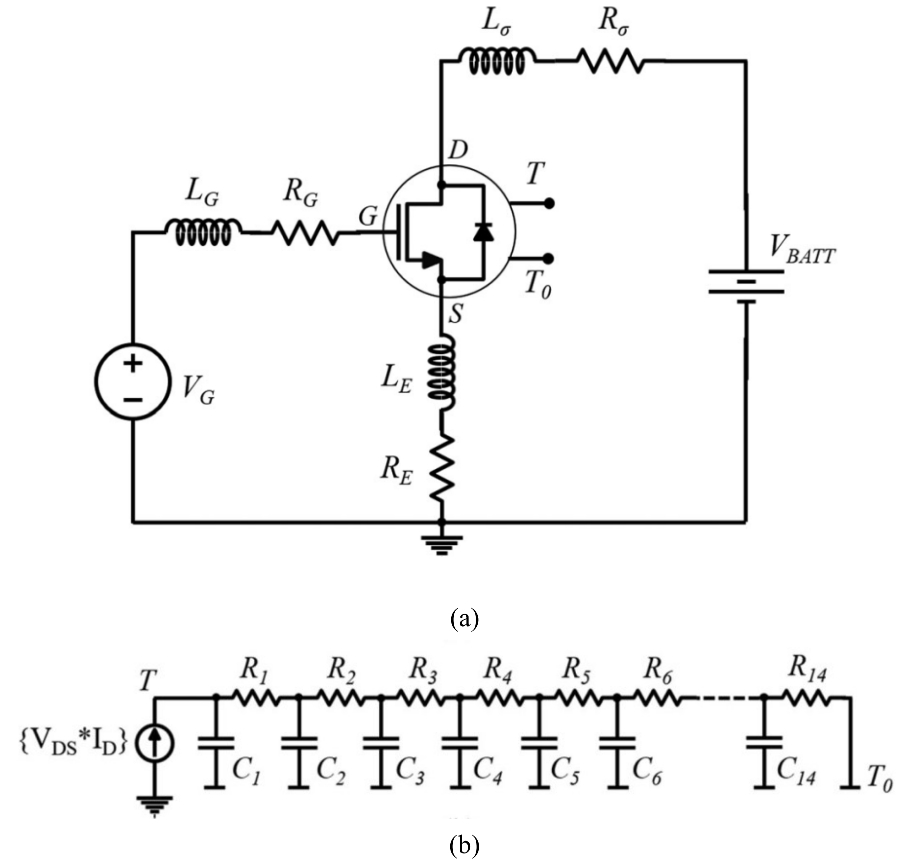
Specifically, the test was performed at 25°C with a supply voltage of 400 V and a load inductor of 1 mH. The pulse duration was chosen to have a nominal current per device of 14 A at the edge of turn-off (100 μs). Due to the uneven static current sharing, however, the actual magnitudes of the static currents conducted by MOSFET1 and MOSFET2 are 14.58 A and 13.28 A, respectively - Fig. 3.10a -. The current imbalance worsens during the switching transient and reaches the maximum value of 3.79 A around 100.1 μs. As the waveforms of Fig. 3.10c highlight, such an imbalance determines a difference in the dissipated power. A quantification of the accuracy in predicting the difference in transient power dissipation can be assessed by comparing the switching energies, obtained by integrating the waveforms of Fig. 3.10c. In particular, the values summarized in Table 3 were obtained by integrating the power from 100.06 μs to 100.12 μs, approximately.

3.2.4 Validation Out of SOA

The proposed model is suited to describe the device behavior even under harsh working conditions, when the high dissipated power within the device causes a critical and potentially harmful temperature increase. In this Section, the model validation during out-of-SOA conditions is presented for SC and UIS tests. In both cases, the operating limits are dictated by the temperature value. In the SC test, the transistor is turned on when a load SC already exists, i.e., the full dc-link voltage is applied to the DUT. The di/dt of the drain current is determined by the driver parameters (driver voltage, gate resistor) and the transfer characteristic of the device. The schematic of circuit used for ET simulations is depicted in Fig. 3.11a. A Cauer equivalent thermal network (see Fig. 3.11b) provided by the device manufacturer on the datasheet was used to evaluate the transient temperature evolution. The values of the RC elements forming the thermal network are reported in Table 4. The description of the circuit used to perform the SC tests is reported in [Mar14]. An HVdc power supply provides the test voltage, which is held by a 2.2-mF capacitors bank. A field-programmable gate array-based digital circuit provides a single pulse of the desired duration to the driving circuit. The test conditions are as follows: V_{GS} = 0/18 V, R_G = 15 Ω V_{BATT} = 758 V. Fig. 3.12 reports the comparison between

experimental waveforms of DUT drain current and drain-to-source voltage during two SC pulses with duration of 3 and 5 μs, respectively. The device temperature increase ΔT, evaluated by the thermal network during the simulation run, is reported against the conduction time. Besides favoring the physical interpretation of the SC behavior, widely addressed in literature [Cas14]–[Ion17], the model correctly describes the effect of an extremely high temperature increase on the device current, as confirmed by the good agreement between experiments and simulations. In Fig. 3.12b, the drain current evaluated with the temperature dependence of [dAl14] is also reported for comparison purposes; for temperature exceeding 450 K, it is evident how the new model predicts with higher accuracy the ET device behavior. In addition, as stated in [Wan16], the SC failure mechanisms of SiC MOSFETs can be driven by thermal runaway induced by temperature-generated current or high-temperature-related gate oxide damage. Fig. 3.12b shows the effect of the leakage when the device temperature approaches 1000 K, with the presence of a current tail in the drain current, correctly predicted by the ET simulation. This extremely high temperature value was first estimated by Huang in [Hua13], and confirmed by finite-element ET simulations in [Rom16]–[Ion17]. In these papers, it is also demonstrated by means of simulations and experiments that the state-of-art SiC power MOSFETs cannot sustain a standard 10 μs SC pulse (with $V_{BATT} = 2/3 \times V_{DSMAX}$), with a reduced ruggedness under SC conditions if compared with similarly rated silicon devices. The last validation for this DUT was performed with an UIS test [Fay17]. Under this working condition, the proper modeling of the avalanche multiplication factor M is of paramount importance. The schematic of the circuit adopted for the ET simulation is the same as in Fig. 3.11, where an inductance L_{load} is used instead of parasitic inductance L_{σ}. In the test circuit described in [Ros10], a 3.3-kV IGBT was used as parallel switch to charge the load inductor, kept in ON-state for a time long enough to reach the desired I_{max}. Moreover, the test circuit is also equipped with a series switch used to disconnect the power supply to prevent the DUT destruction in case of failure. The test conditions are as follows: $V_{GS} = 0/18$ V, $R_G = 15\ \Omega$, $V_{BATT} = 400$ V, and $L_{load} = 4.6$ mH. In Fig. 3.13, the comparison between experimental and numerical waveforms during an UIS test at $I_{max} = 20$ A is shown. It is found that the device is plagued by a temperature reaching about

600 K above T_0 during the avalanche time; nevertheless, also in this case, the model correctly describes the measured current and voltage.

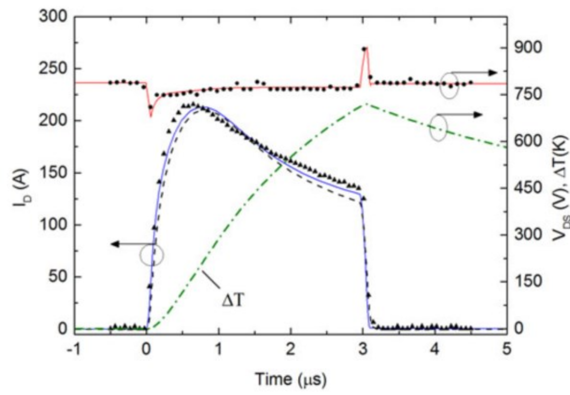


(b)

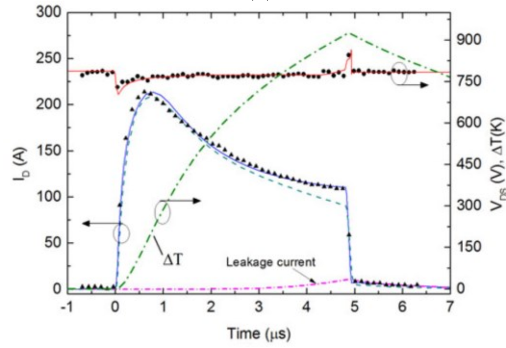
Fig. 3.11 Circuit used to evaluate the DUT switching waveforms.

TABLE 4 THERMAL NETWORK PARAMETERS

Node	1	2	3	4	5	6	7
R_i(mK/W)	13.3	13.3	37.8	36.9	83.6	58.4	43.2
C_i(J/K)	0.424 m	0.341 m	1.32 m	1.58 m	1.88 m	2.64 m	8.5 m
Node	8	9	10	11	12	13	14
R_i(mK/W)	51.2	51.9	47.5	46.6	58.7	40.8	10.4
C_i(J/K)	14.2 m	26 m	47.8 m	0.102	0.165	0.282	2.41



(a)



(b)

Fig. 3.12 SC electrical waveforms (I_D, V_{DS}) and temperature increase (ΔT) for both (a) 3 μs and (b) 5 μs pulse-length cases. Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT. The graph (b) also reports the leakage current.

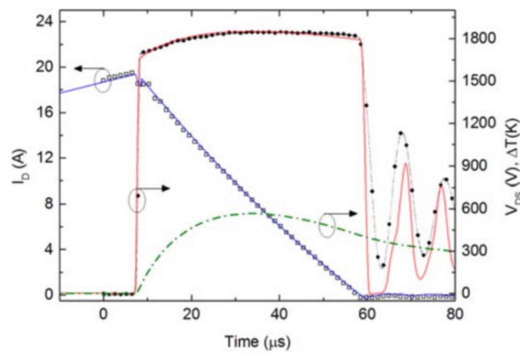


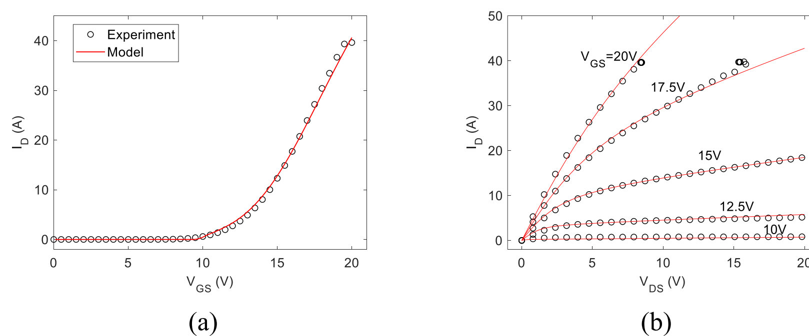
Fig. 3.13 UIS waveforms (I_D, V_{DS}) and temperature increase (ΔT). Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT.

3.3 Model Validation for 3.3 kV Devices

To verify the model scalability, its static and dynamic electrical behavior was also validated on 3.3 kV prototype MOSFETs.

3.3.1 Validation of the DC Behavior

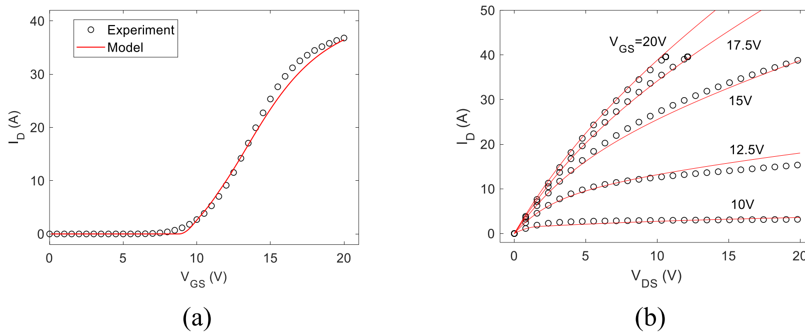
Experimental data of a 3.3 kV, 4H - SiC planar power MOSFET at different operating temperatures were used as the target curves of the tuning process of the parameters. As explained in Section 3.1, the first step for the DC calibration of the model consists in the estimation of the current factor (K_0 [A/V^2]) and threshold voltage (V_{TH0} [V]) at the reference temperature T_0. These were extracted through QEM from the steepest portion of the isothermal transfer characteristic at room temperature (300 K). In addition to these, the channel - length modulation parameter (λ [V^{-1}]) was measured from the output characteristics. To this purpose, the I_D-V_{DS} curve at the lowest V_{GS} bias (i.e., 10 V) was selected in order to guarantee the full operation in saturation mode of the device ($V_{DS} >> V_{GS} - V_{TH}$). Subsequently, the so obtained values were set in the LEVEL-1 MOSFET component and were used as the starting assumption of the iterative optimization procedure detailed in Section 3.1, which refined K_0, V_{TH0} and tuned the parameters of the drain resistance. At the end of this step, the simulated curves at 300 K reported in Fig. 3.14 were obtained. The overlap with the experimental DC characteristics highlights that excellent agreement was achieved at room temperature.



(a) (b)

Fig. 3.14 (a) I_D-V_{GS} and (b) I_D-V_{DS} curves at T = 300 K and V_{DS} = 10 V. SPICE model: solid line; symbols: experimental data.

Afterwards, the optimization procedure was iterated to evaluate the temperature coefficients of the static parameters. The comparison reported in Fig 3.15 shows that the model can accurately reproduce the DC characteristics also at 400 K, with only a slight deviation in the I_D-V_{GS} curve at high V_{GS}.



(a) (b)

Fig. 3.15 (a) I_D-V_{GS} and (b) I_D-V_{DS} curves at T = 400 K and V_{DS} = 10 V. SPICE model: solid line; symbols: experimental data.

3.3.2 Validation of the Transient Behavior

Successively, the parameters V^*_{ds}, V^*_{gd}, C_{DS0}, C_{DSMIN}, C_{GD0} and C_{GDMIN} of the MOSFET capacitances (C_{GS}, C_{GD} and C_{DS}) were calibrated to obtain a satisfactory reproduction of the transient characteristics. The experimental waveforms representing the objective of the calibration are the turn-on and turn-off transients obtained from a DPT on inductive load at 25 C. A schematic of the DPT setup is depicted in Fig. 3.16 and it features the following specifications: V_{TEST} = 1.8k V, R_G = 4.7 Ω and L_{load} = 12mH.

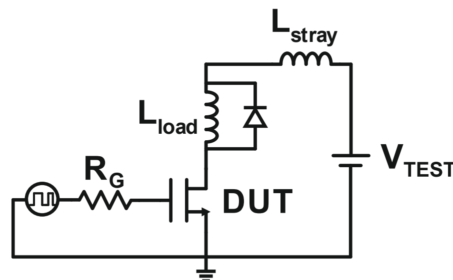


Fig. 3.16 Schematic of the simulated double pulse test setup. V_{TEST} = 1.8 kV; R_G = 4.7 Ω; L_{load} = 12 mH; L_{stray} = 500 nH.

The same circuit was simulated in SIMetrix but with the addition of the inductance L_{stray} = 500 nH to account for the parasitic elements introduced by the wires. The waveforms reported in Fig. 3.17 and Fig. 3.18 illustrate that, after the calibration step, both the turn-off and turn-on phases are properly reproduced by the model. A better quantification of the accuracy of the simulated waveforms can be assessed by analyzing the switching dissipated energies of Fig. 3.19, which verify that the model is not only able to predict the switching waveforms, but it can also provide a reliable estimation of the switching losses.

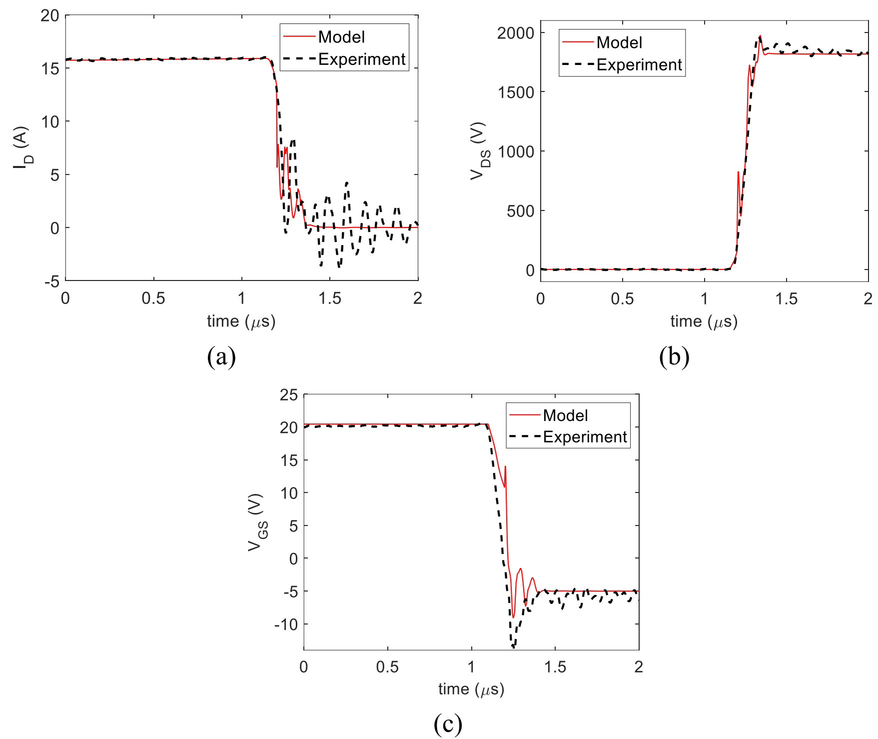


Fig. 3.17 Inductive turn-off waveforms: a) drain current; b) drain voltage; c) gate voltage. Solid lines: SPICE model; dashed lines: experimental data.

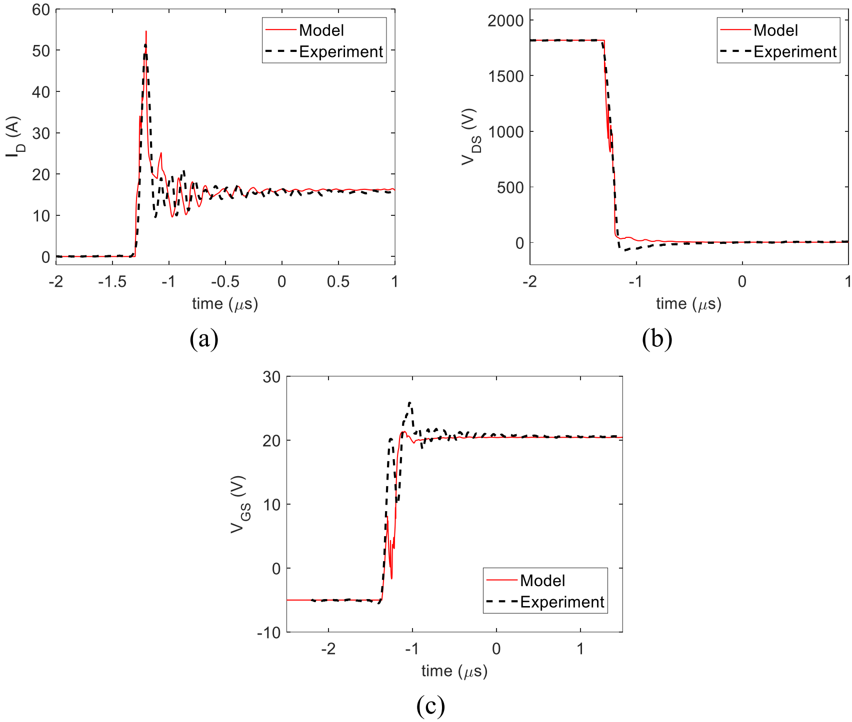


Fig. 3.18 Inductive turn-on waveforms: a) drain current; b) drain voltage; c) gate voltage. Solid lines: SPICE model; dashed lines: experimental data.

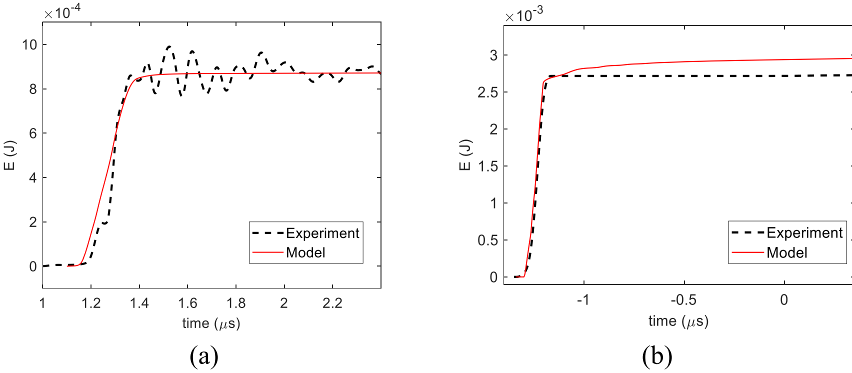


Fig. 3.19 Waveforms of dissipated energy during (a) turn-off and (b) turn-on. Solid line: SPICE model; dashed line: experimental data.

3.4 Model Validation for 1.7 kV Devices

To further explore the model scalability, the static and dynamic performance were also compared against experimental curves of 1.7 kV-60 A SiC MOSFETs. Since the devices are provided as bare dies, they were mounted onto a suitable test substrate to enable their electrical characterization (Fig. 3.20). The isothermal static current-voltage characteristics (I_D - V_{GS} and I_D - V_{DS}) of 17 DUTs were measured by an in-house developed pulsed curve tracer both at 25 °C and at 125 °C. Some parameters determining the on-state current and their spread were evaluated, and the resulting values are reported in Table 4. The MOSFETs exhibit some spread in their current-conduction behavior. Nevertheless, the spread of the transfer characteristics is confined within 15% (Fig. 3.21). Therefore, the DUT selected as reference for calibrating the model is the one exhibiting the median transfer characteristic. However, the impact of the technological fluctuations on the uneven current sharing can be easily included as reported in [Bor18] and described in Chapters 5 and 6.

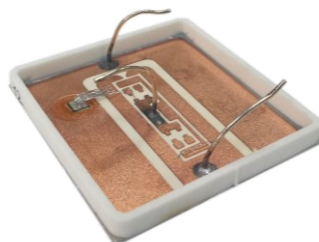


Fig. 3.20 Example of 1.7 kV SiC MOSFET under test mounted on the test substrate.

TABLE 4 MAIN PARAMETERS DETERMINING THE CURRENT CONDUCTION AND THEIR SPREAD MEASURED AT 25 °C.

Parameter	Threshold voltage: V_{TH} [V]	Transconductance: K [A/V^2]	Channel length modulation parameter: λ [V^{-1}]
Mean value ± spread	5.77 ± 0.17	0.84 ± 0.06	0.03 ± 0.004

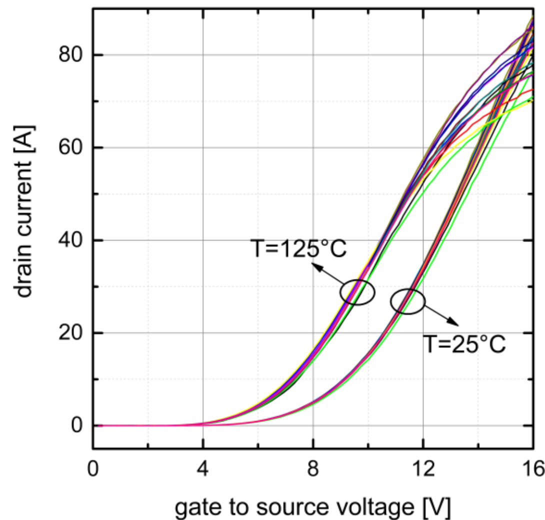


Fig. 3.21 Isothermal transfer characteristics of the 17 SiC MOSFETs under test.

The compact electrothermal model adopted in this case is a variant of the one presented in Chapter 2. compared to the latter, The modifications introduced can be summarized as follows:

- the modulation of charge in the channel region is modeled by a LEVEL-3 MOSFET SPICE primitive (referred to as M_{CH}) instead of a LEVEL-1 MOSFET;

following the approach suggested in [ONS21], a standard JFET (J_{RJ}) in series with M_{CH} was used to describe the modulation of the current path due to the expansion of the space charge region in the JFET area. Such a phenomenon was previously represented in Chapter 2 through a voltage dependent resistor R_{AJ}.

Replacing behavioral components with conventional SPICE primitives aids convergence, widens the model compatibility and reduces the number of fitting parameters. A schematic representation of its equivalent circuit is reported in Fig. 3.22, which highlights the main components used to model the static current flow. The model is fully electrothermal and includes the temperature dependence of the most relevant physical parameters in the same way done for the model in Chapter 2. Three capacitances determine the dynamic characteristics of the model. These are (i) the gate-to-source capacitance (C_{GS}) which is constant and equal to the capacitance of the LEVEL-3 MOSFET M_{CH},

(ii) the voltage dependent junction capacitance of the body diode (C_J), and (iii) the non-linear gate-to-drain capacitance (C_{GD}) modelled as per (2.17). Even though it was recently benchmarked in [Nel21] that modeling the MOSFET non-linear capacitances by arctangent function is not as accurate as other techniques suggested in the literature, it is also recognized that it provides a good trade-off between accuracy and simulation speed and it will be shown in Subsection 3.4.2 that the simulations produce adequate prediction of the switching power losses.

The results of the calibration are described in the following.

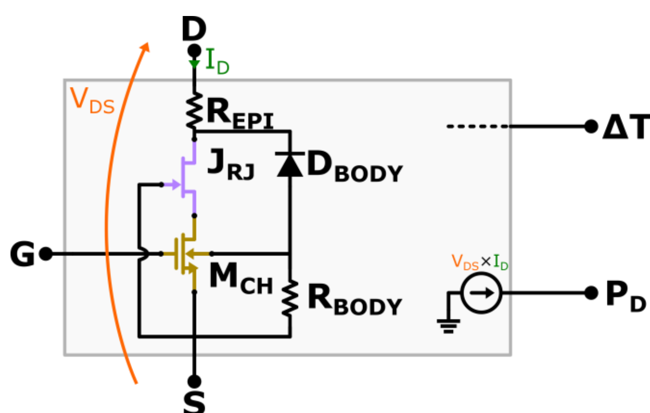


Fig. 3.22 Schematic representation of improved compact electrothermal model for SiC MOSFET. The capacitances are omitted for the sake of clarity.

3.4.1 Validation of the DC Behavior

The model parameters controlling the static electrical performances are calibrated through the automatic routine implemented MATLAB and SIMetrix outlined in Section 3.1. A subset of physical parameters, such as the threshold voltage (V_{TH} [V]), the current factor (K [A/V^2]), and the parameter accounting for the channel-modulation effect (λ [1/V]), are directly extracted from the experimental data and used as initial point of the optimization procedure.

From the comparison reported in Fig. 3.23a and b, it can be seen that excellent agreement was achieved between the experimental data and the fitted model at 25 °C. As shown by the data at 125 °C of

Fig. 3.23a and c, the variation of the DC performance with temperature is also correctly captured.

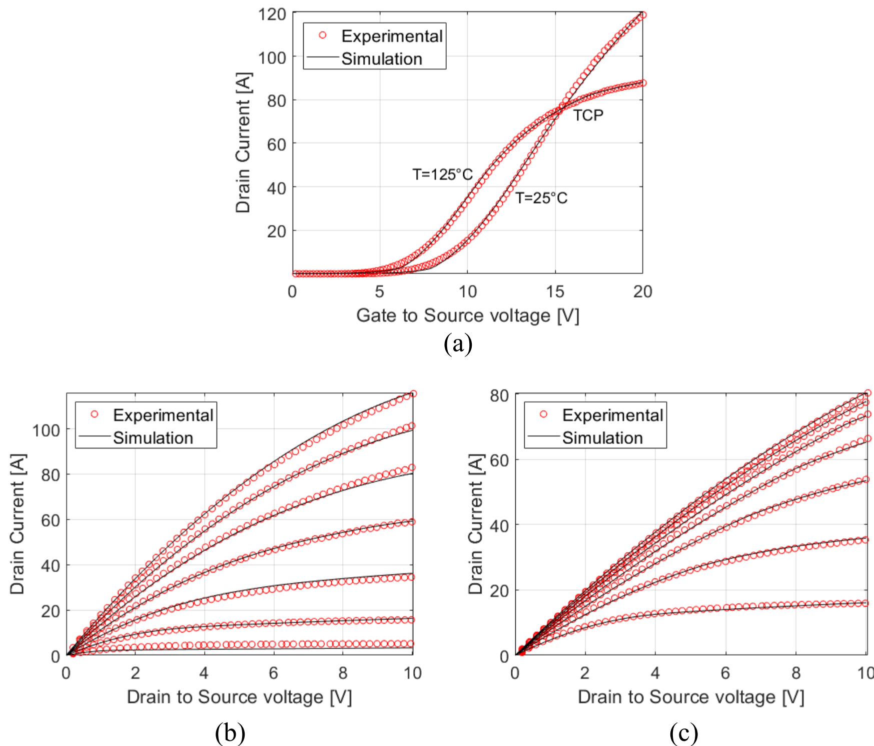


Fig. 3.23 Comparison between the experimental and simulated isothermal static curves for the (a) transfer characteristics, (b) output characteristics at 25 °C and (c) 125 °C.

3.4.2 Validation of the Transient Behavior

To characterize the dynamic behavior of the DUTs, a double pulse test (DPT) on an inductive load of 1 mH was conducted by placing in series two MOSFETs in a half-bridge configuration. The high-side switch acts as a freewheeling diode since the channel conduction was inhibited by connecting the gate and source terminals together. A schematic of the DPT setup is provided in Fig. 3.24.

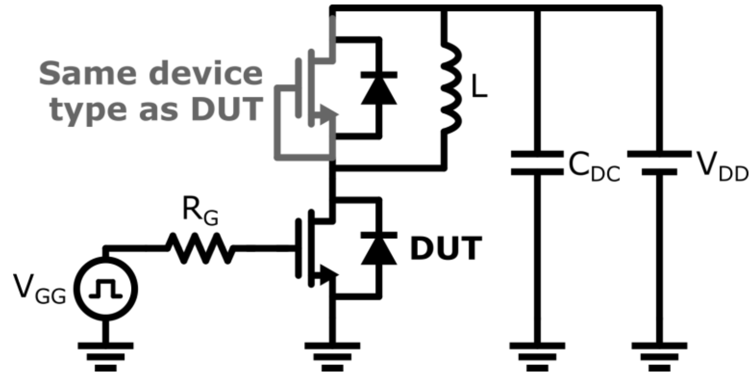


Fig. 3.24 Schematic of the double pulse test setup adopted for the characterization of the switching transients. V_{DD} = 800 V, C_{DC} = 550 µF, L = 1 mH, R_G = 11 Ω, V_{GG} = 19/-3.5 V.

The test was performed at 800 V - 28 A, with R_G = 11 Ω for both 25 °C and 125 °C, and careful evaluation of circuit parasitic components was carried out as it is known that they strongly affect the shape of the waveforms during switching transients. As witnessed by the waveforms of Fig. 3.25a and b, the model is able to precisely capture the very fast turn-on ($dV_{DS}/dt \approx 5.3$ kV/µs, $dI_D/dt \approx 275$ A/µs) and turn-off ($dV_{DS}/dt \approx 8.6$ kV/µs, $dI_D/dt \approx 225$ A/µs) switching transients, including the oscillations caused by the stray components. The accuracy of the of model is also substantiated by the comparison of Fig. 3.25c, where the experimental and simulated waveforms of the power dissipated by the DUT are superimposed. It is worth noticing that the model not only provides a correct estimation of the switching energy, i.e., of the integral of the power dissipated during the commutations, but also of the instantaneous value of the power itself. This is of paramount relevance when it is important to take into account the time evolution of the thermal phenomena since a well-modeled power dissipation translates into an accurate time-dependent heat source.

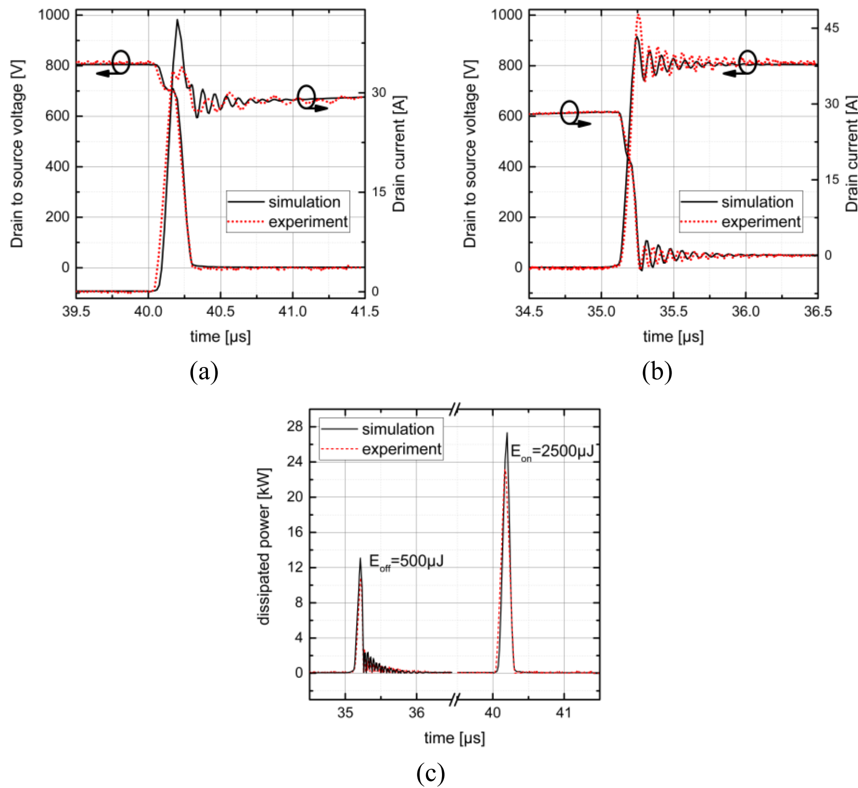


Fig. 3.25 Comparison between the experimental and simulated current and voltage waveforms obtained during (a) turn-on and (b) turn-off event on inductive load at 25°C, 800 V and 28 A. (c) Comparison between the experimental and simulated switching power dissipation.

3.4.3 Summary

In this Chapter, the validation of the compact model introduced in Chapter 2 has been presented. An automated calibration procedure based on MATLAB and SIMetrix for tuning the parameters determining the static behavior of the model has been explained. Successively, the accuracy of the model has been evaluated for power MOSFETs with different BVs, thus proving the model scalability to devices of various ratings.

First, the model performance was assessed for 1.2-kV commercial devices. In addition to the static and dynamic curves, the match with experimental data obtained during out-of-SOA conditions

has been also evaluated. Remarkably, the model capability of predicting the power dissipation imbalance of mismatched parallel MOSFETs has been assessed.

Subsequently, the model has been tuned to match the characteristics of 3.3-kV devices. Also in this case, a good agreement between simulation and the experimental data has been obtained.

As last test bench, the static and switching waveforms of 1.7-kV devices have been considered. In this case, a slightly modified version of the model has been utilized and very accurate estimation of the instantaneous power dissipation has been achieved.

Chapter 4

Soft Failure During Short Circuit

SiC power MOSFETs exhibit some key differences with Si MOSFETs and IGBTs. In particular, their features-set (e.g., smaller device volume, thinner gate oxide and absence of conductivity modulation) implies higher electro-thermal stress levels during short-circuit. On top of that, the present level of technology maturity is still associated with a greater spread in the value of some of the main device electro-thermal parameters, such as threshold voltage and on-state resistance. So, rather uneven degradation in parallel multi-chip structures is a likely occurrence. A type of short-circuit failure that is interesting for parallel connection is investigated in this Section.

The results and findings presented in this Chapter result from a research activity developed in conjunction with LAPLACE laboratory - University of Toulouse, France -, ITEC Lab - THALES, France - and SP^2 Laboratory (Kyoto University of Advanced Science, Japan).

4.1 SiC MOSFETs Soft and Hard Failure Modes

4.1.1 Introduction to Failure Modes of SiC MOSFETs During Short Circuit

A key robustness requirement in several application domains, particularly in the case of electric drive applications, is short-circuit (SC) withstand capability. A substantial body of literature has already been produced on the subject, pointing out potential criticalities in this respect, when transitioning from silicon (Si) transistors to SiC ones [Cas13]-[Rom15]. In particular, the studies in [Rom16] have pointed out the existence of a twofold SC failure mode, depending on the rate of temperature increase: a soft one, characterized by the device failing as a drain-to-source open circuit (Fail-To-Open behavior, FTO) and a

hard one, in which the transistor fails as a short-circuit between drain and source (Fail-To-Short behavior, FTS). The two different behaviors are exemplified in the results of Fig. 4.1a. The former features a collapse of the gate-source voltage to a value well below the threshold voltage (as a result of damage in the gate structure, the gate-source resistance after damage is lower than the external drive gate resistance, $R_{GS} << R_{G,EXT}$), which practically results in the device turning off. The latter features a shorting of the drain-source terminals, with drain current thermal runaway and collapse of the drain-source voltage. The specific failure mode is of great relevance for the application, with a clear preference for FTO-type transistors. These feature an intrinsic fault containment capability, which, in the case of parallel device or multi-chip modules-based designs, still enables to operate the system, even if at reduced power ratings, without additional complex or costly circuitry [Boi19]. Such an operational status is usually referred to as hopping-home mode and is a highly desirable feature of power conversion systems in some strategically relevant application domains, in particular transportation. For that reason, soft failing devices are of great interest and have already received dedicated attention in the recent past [Boi18].

Indeed, in contrast to FTO, the FTS mode typically implies a) the fast discharge of energy storage components (e.g., capacitors), with oftentimes explosion-like characteristics and a possible failure propagation typically for a module device where chips are close to each other; b) loss of functionality of the whole circuit in the case of parallel multichip architectures, either discrete or module based.

A preliminary screening on commercial 1.2 kV-rated MOSFETs delivered the results in Fig. 4.1b: a single manufacturer could be identified, whose device consistently performed as FTO for V_{DS} values up to 50% rated voltage, which is a representative application requirement [Boi18]. Because of its application interest, that device was considered further in detail. The DUT is a commercial discrete planar-gate 80 mΩ – 1200 V SiC MOSFET.

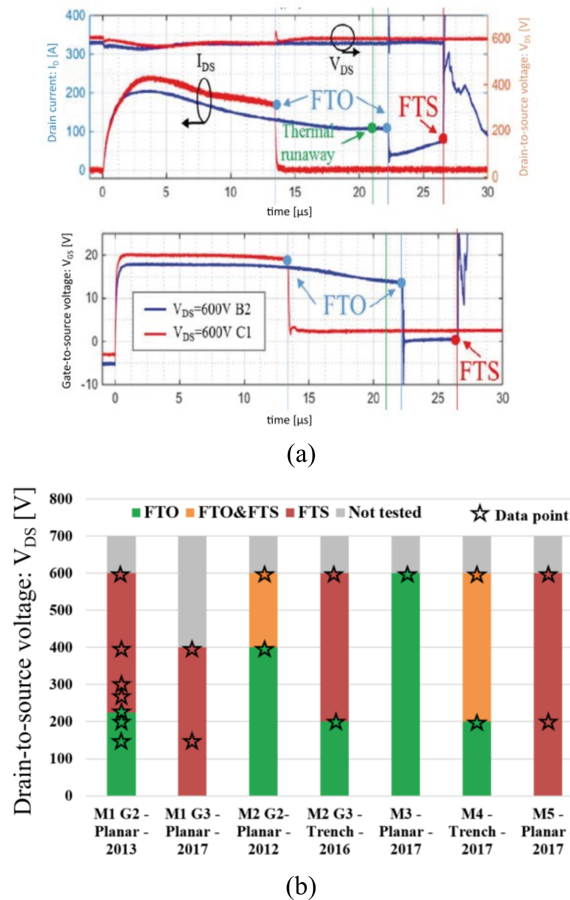


Fig. 4.1 (a) short-circuit current I_D and V_{DS}, (top) and V_{GS} (bottom); (b) summary of SC failure mode (FTO or FTS) for different commercial devices at different V_{DS}.

4.1.2 Gate Leakage Current as a Precursor of Failure

It has been previously found that the gate leakage current, $I_{G,LEAK}$, is an effective indicator of the onset of the failure during SC. Specifically, the insurgence of an increasing gate leakage current during SC designates that the dissipated energy is approaching the critical energy that the DUT can handle in short circuit [Che15b]. Moreover, for SC pulses shorter than a critical pulse width ($t_{PW,CRIT}$), nor damage accumulation neither device aging were observed, where $t_{PW,CRIT}$ is defined as the time instant when the steeper increase of $I_{G,LEAK}$ begins (Fig 4.2c) [Che15b].

As a first step, a series of non-destructive single-event short circuit tests was performed for assessing $t_{PW,CRIT}$. The latter was estimated by successive short circuit tests with a pulse width increasing by steps of 1 µs until a surge in $I_{G,LEAK}$ was observed. The waveforms of Fig. 4.2 show: (a) the SC drain current, I_D, (b) the gate-source voltage, V_{GS}, and (c) $I_{G,LEAK}$, for the device subjected to pulses of different duration. Here, V_{DS} = 600 V in all tests.

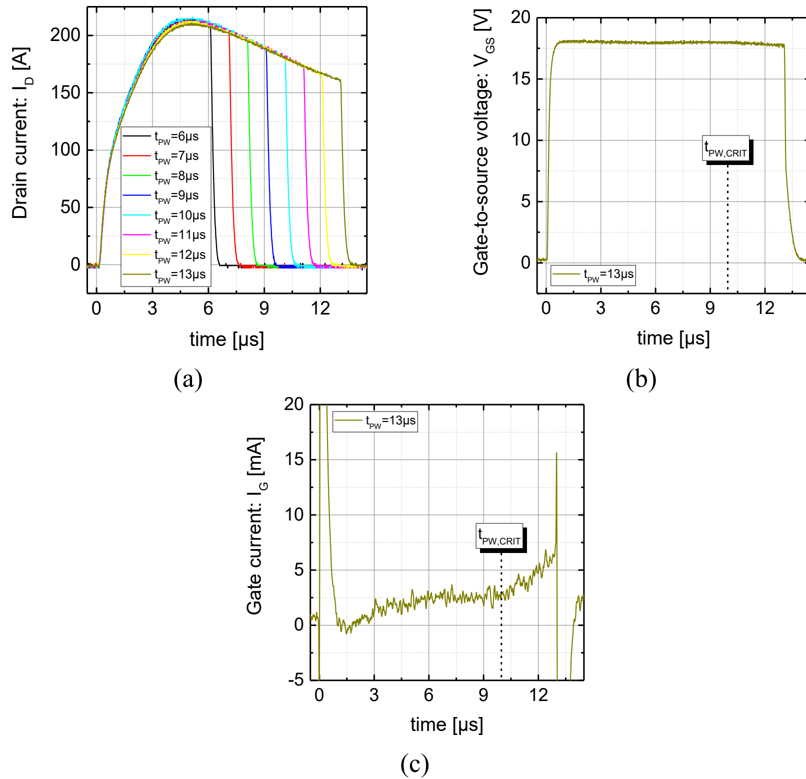


Fig. 4.2 Experimental results for SC tests at 25 C with vary pulse durations: (a) I_D, (b) V_{GS}, and (c) $I_{G,LEAK}$. A drop in V_{GS} and a steeper increase of $I_{G,LEAK}$ are noticeable from about 10 µs.

During the pulse, at about time =10 µs, $I_{G,LEAK}$ shows exponential increase onset. According to the results presented in [Che15b], $t_{PW,CRIT}$ was quantified as 10 µs for the device under test (DUT). In [Boi19b] The physical mechanism responsible for such a current increase was explained to be the thermionic emission (also

referred to as Schottky emission). While the Schottky emission can take place also in Si MOSFETs, the required temperature for its occurrence is higher than the temperature triggering thermal runaway during SC. Moreover, the energy barrier at the Si/SiO_2 interface is higher than that SiC/SiO_2 interface.

The pulse width was then reduced to 4 µs and repetitive stress was applied. If no $I_{G,LEAK}$ was observed after 2000 cycles, the short-circuit pulse width was increased by 1 µs. Fig. 4.3a shows degradation of the saturation characteristics after thousands of pulses; however, that was not found to be related to any degradation at gate level, as the results of Fig. 4.3b clearly show.

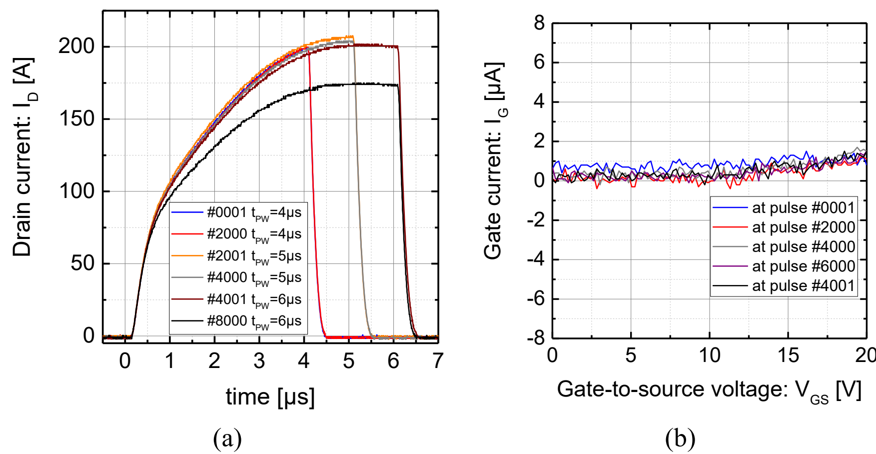


Fig. 4.3 Experimental results for repetitive SC test at 25°C with "short" pulse widths: (a) I_D and (b) $I_{G,LEAK}$. Although the device characteristics are clearly severely degraded, no relation can be detected with a modification of the gate structure characteristics under these stress conditions.

On the other hand, increasing the pulse width to 10 µs yields very different results (Fig. 4.4). The drain current is still degraded, Fig. 4.4a, but that is now clearly due to damage of the gate-structure, manifest in the form of substantial $I_{G,LEAK}$ value increase, on an accelerated basis between #3000 and #3200 cycles, Fig. 4.4b, and subsequent decrease, as a result of a low value series gate resistance in the transistor driving path, of the bias voltage applied across the gate-source terminals, Fig. 4.4c.

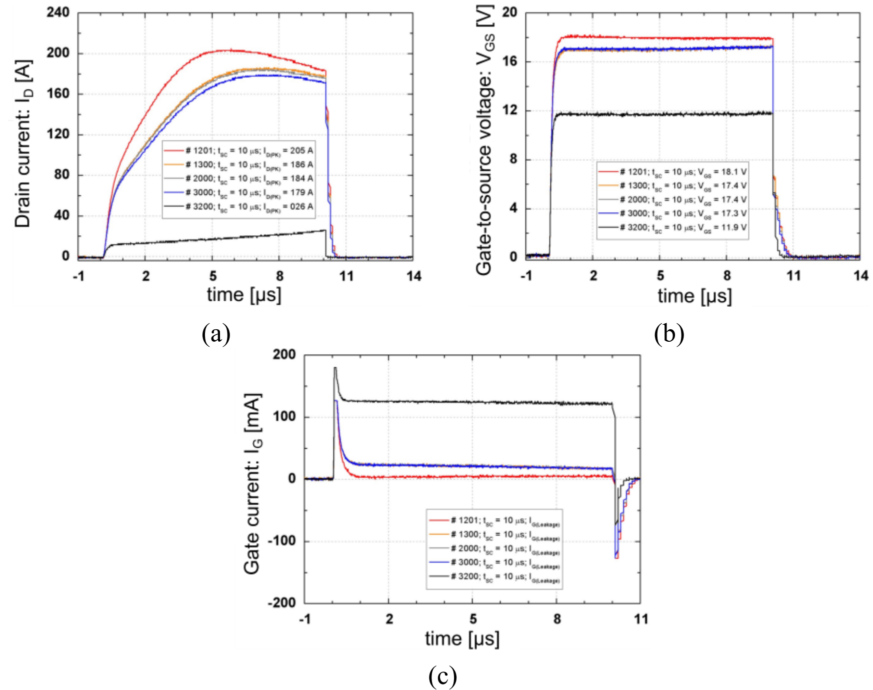


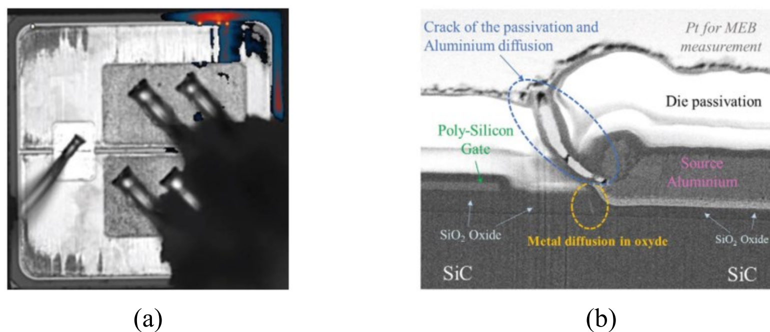
Fig. 4.4 Experimental results for repetitive SC test at 25°C with "long" pulse widths: (a) I_D, (b) V_{GS} and (c) $I_{G,LEAK}$. In this case, the change in device characteristics is strictly related to degradation of the gate, as manifest by the significant increase in gate current value.

4.1.3 Interpretation and Structural Analysis

The results are interpreted on the basis of two different failure mechanisms intervening, depending on the pulse width.

- For "short" pulses (<$t_{PW,CRIT}$) only reduced saturation current is manifest (Type-1 degradation), possibly caused by degradation of the chip metallization and subsequent V_{GS} de-biasing [Cas14b], [Sme11] or by an interface charging mechanism due to hot electrons.
- For "long" pulses, the aging of the gate structure is evident (Type-2 degradation). The latter is caused by cracks around the interlayer dielectric (ILD) triggered by the high difference in thermal expansion between the top Al and the SiO_2 and formation of metallic paths in the gate-source ILD, caused by the top Al melting at the edge of the chip during the short circuit, as presented in

Figs. 4.5a and 4.5b [Boi18]. The region of major degradation, and thus leading to eventual failure, was observed to change on the device surface, but it was always located near the border of the active area, where terminations of various type are present and where geometrical singularity appears between the peripheral gate distribution ring and the interdigital ramifications fingers, Figs. 4.6a and 4.6b.



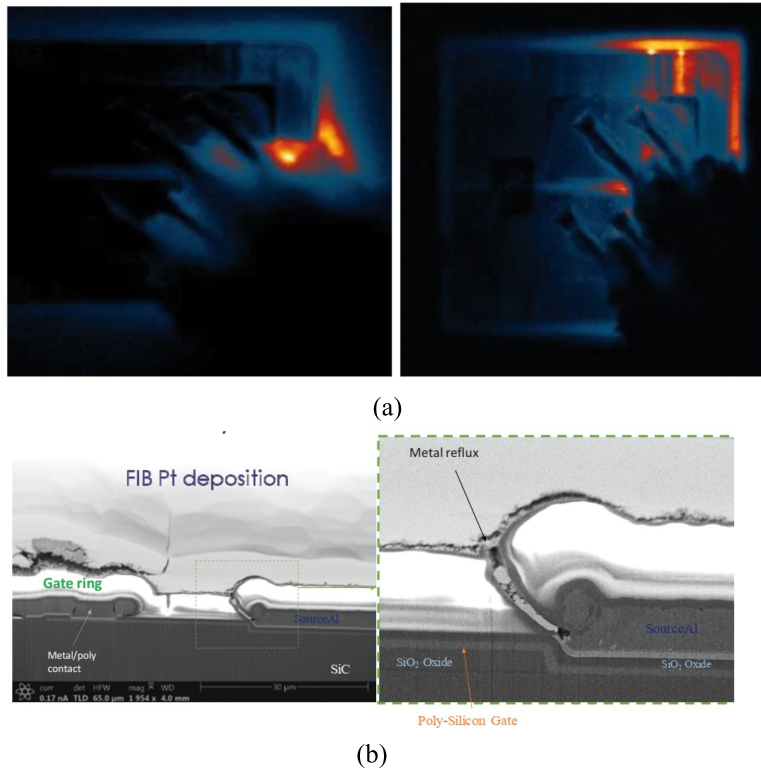
(a) (b)

Fig. 4.5 (a) Micrograph of MOSFET (bare-die top view) showing localized $I_{G,LEAK}$ increase; (b) scanning electron microscope (SEM) image of a device focused ion beam (FIB) microsection after destructive test.

4.2 Off-Line Recovery

Further repetitive short-circuit tests were performed on a new device of the same class of that considered in Section 4.1. Since the results reported in Section 4.1 highlighted that for $t_{PW} < 6$ µs no permanent gate damage could be detected, the pulse width was chosen to be equal to the critical pulse width ($t_{PW} = t_{PW,CRIT} = 10$ µs), so as to produce gradual damage accumulation but leaving a sufficient safety margin from the maximum single-pulse withstand capability of the DUT ($t_{SC,MAX} = 14$ µs). The results of this test campaign are illustrated in Fig. 4.7. Fig. 4.7a shows the drain current, I_D; Fig. 4.7b the gate-source bias voltage, V_{GS}, and Fig. 4.7c the corresponding gate current, I_G. As is evident from these results, the device characteristics are progressively degraded during the test: to a reduction of I_D (Fig. 4.7a), corresponds a decreased V_{GS} (Fig. 4.7b), as a result of increased gate leakage current (Fig. 4.7c). As detailed in Section 4.1.3, this is due

Type-2 degradation, i.e., the partial shorting of the gate and source terminals attributed to the creation of cracks and metal (aluminum, Al) diffusion into them.



(a)

(b)

Fig. 4.6 (a) Micrographs of MOSFET (bare-die top view) showing movement of localized $I_{G,LEAK}$ increase; (b) SEM image of device FIB microsection confirming the failure mechanism attributes to ILD, (the right hand-side image is a magnification of the area highlighted on the left hand-side one).

To further explain the occurrence of such a failure mechanism, finite-elements-based ET model was developed in [Boi19c, Ric19]. The model takes into account the temperature dependence of the conductivity and the mass heat of SiC and aluminum, as well as the solid-liquid phase transition of the Al top layer. Using structural computer aided design tools (specifically, COMSOL was used here), the model received as input $I_D(t)$ waveform of Fig. 4.7a, with a constant V_{DS} value of 600 V. Considering pulse number #1600, Fig. 4.8 shows the temperature rise of all the main layers of the chip during the short

circuit. It is clearly visible that the Al layer is above its melting point and that high thermal energy is injected into its liquid phase. Furthermore, according to [Liu20], at the Al melting temperature, the thick oxide is already cracked because the mechanical stress at the upper corner greatly exceeds its mechanical strength.

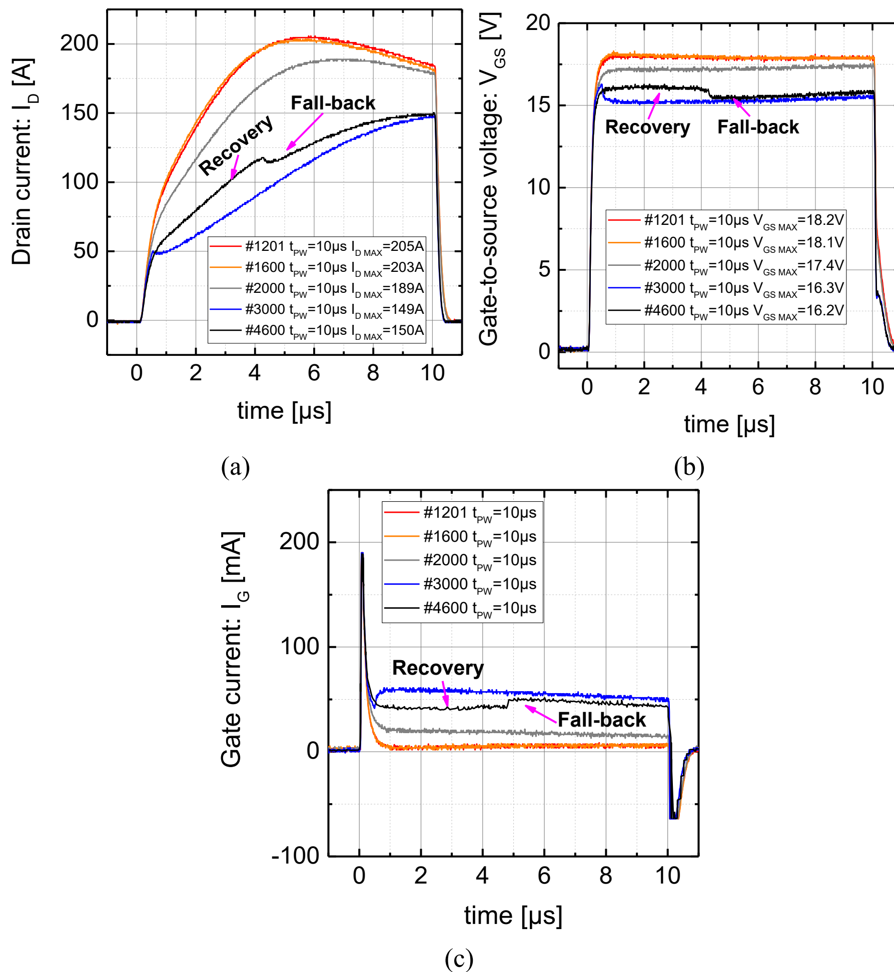


Fig. 4.7 DUT progressive degradation during repetitive SC at 25°C, manifest as a decrease of (a) I_D after #1600 pulses with t_{PW} = 10 μs at V_{DS} = 610 V – $V_{GATE\ DRIVE}$ = 18 V – $R_{GATE\ EXT}$ = 47 Ω – T_{CASE} = 25 °C; (b) corresponding V_{GS} waveforms; (c) corresponding I_G waveforms. In the results associated to pulse #4600, the device initially exhibits partial recovery, followed by degradation.

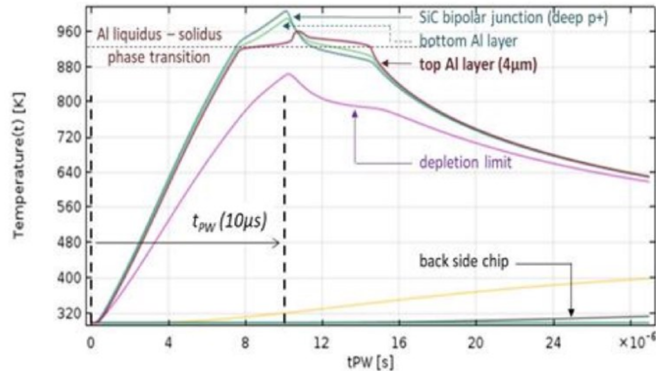


Fig. 4.8 1-D chip temperature simulation in short-circuit operation for pulse #1600: t_{PW} = 10 µs at V_{DS} = 610 V, $V_{GATE\ DRIVE}$ = 18 V – $R_{GATE\ EXT}$ = 47 Ω – T_{CASE} = 25 °C.

On the side of the gate ageing observation, a new consideration can be made in the results of Fig. 4.7: a partial recovery effect can be observed in going from pulse #3000 to pulse #4600. Here, the recovery is not stable, and half-way through the pulse the device characteristics fall back to the previous degraded state. Because of its potential relevance for the application, this observation triggered further detailed analysis of the effect, specifically of the possibility to force and control the recovery and stabilize the device characteristics, even if at a slightly degraded level. Based on the findings of [Fay19], a first attempt was made by statically sweep-biasing the degraded transistor (same device used previously for the tests of Fig. 4.7 in a V_{GS} range ≤ 12 V, with different limit values of gate pulsed current. Fig. 4.9 summarizes the results:

- Sweep 1 (black curve) corresponds to the first traced curve, in which the gate current was limited at 10 mA: here, as V_{GS} is increased beyond about 10.8 V, a sudden breakdown like characteristics is entered, with a steep increase of I_G.
- Sweep 2 (red curve) is a second sweep carried out straight after Step 1 to confirm the breakdown state.
- Sweep 3 (blue curve) is a sweep with increased limit value to 30 mA: here, as V_{GS} is increased beyond just 1 V a recovery effect is manifest, with I_G dropping suddenly again.

These results point out that the device gate characteristics can be partially recovered by producing moderate heat generation in the gate region. This is ascribed to a fusing effect taking place, which effectively disconnects degraded portions of the chip from the remaining cells. In this case, the device reaches a new stable, though slightly degraded state. However, if the pulse width t_{PW} is increased closer to the maximum duration $t_{SC,MAX}$ of the DUT, the level of damage accumulation is greater and for some devices analyzed, the I_G value after recovery was found to be too high for them to be still usable with typical gate-driver designs. In Fig. 4.9, at the end of the first series of low-voltage gate sweeping, the measured equivalent gate-source resistance was 2.4 kΩ, corresponding to a gate-drive supply of 135 mW at 18 V.

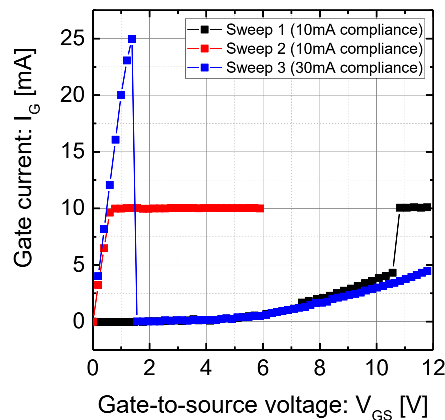


Fig. 4.9 Static characteristics (I_G vs V_{GS}) of device degraded by repetitive short circuit: first and third sweeping biasing-gate tests highlighting breakdown and recovery effects.

To try and get the entire gate recovery, a second series of transfer characteristics sweeping was carried out, the results of which are given in Fig. 4.10. Here, the gate bias voltage is increased up to the nominal voltage of 18 V at first and beyond such value subsequently. For reference, a Keysight™ B2902A SMU with 600 µs pulse duration was used for these tests; the effect of the pulse duration is discussed at the end of this Section. Fig. 4.10a shows that, for V_{GS} higher than 12 V and lower than 16 V, a chaotic transient behavior appears when the limit gate current is moved from 5 to 12 mA (step 1 to step 6): a first metallic injection effect appears in the form of a soft breakdown of the oxide,

following a fusing effect and a second metallic injection effect. In Fig. 4.10b, by gradually increasing the limit gate current up to 30 mA and increasing the bias voltage from 16 V to 30 V, the chaotic behavior disappears, giving way to a stable ohmic transfer characteristic. From an equivalent $R_{GATE} \cong 1.8$ kΩ at 12 V in step 1, $R_{GATE} \cong 1.3$ kΩ at 18 V in step 18, giving an acceptable gate-drive over-supply of 250 mW at 18 V to continue operation of the device in hopping-home mode. However, in Fig. 4.10c, in an attempt to further restore the gate oxide, the sweeping was repeated with a voltage bias higher than 18 V up to 30 V. A new stable ohmic state appears in this case with a lower $R_{GATE} \cong 465$ Ω at 15 V. Unfortunately, such value is too low, giving a gate-drive over-supply of 480 mW at 15 V.

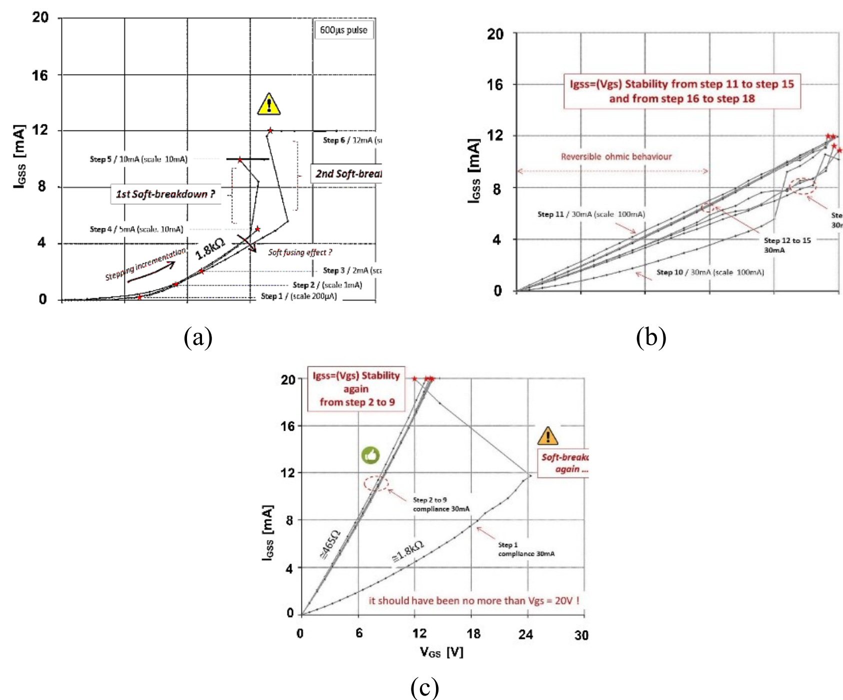


Fig. 4.10 $I_{GSS}(V_{GS})$ gate ohmic restoration analysis: (a) 5 mA to 12 mA, (b) 30 mA, (c) high gate-source bias and final metallic crack. All graphs share the bottom x-axis and scaling.

The preliminary qualitative conclusion can be drawn that the bias voltage and injected restoration energy values should be high

enough to eliminate the main ohmic paths for the device to be usable at nominal gate voltage, but they should not be too high, so as not to re-metallize again the cracked oxide Finally, in Fig. 4.10c, a final attempt was made to induce gate recovery by increasing the pulse duration from 600 μs to 600 ms. Even in this case of high energy injection, the ohmic state of the gate remains stable and, although the equivalent gate resistance is lower in this case, it remains nevertheless at a value which makes the device further use in a real circuit still possible, as demonstrated in the next section. The importance of this study for parallel connected SiC MOSFETs can be clarified through the following reasoning. Although a failed device behaves as an open circuit between drain and source, it still absorbs a continuous gate current. This might be a problem when parallel arrays of SiC MOSFETs are connected to a single gate driver since the absorbed gate current might be sufficiently big to lower the gate driving signal. This might result in *(i)* sub-optimal biasing of all the remaining MOSFETs and subsequent reduction of the system efficiency or *(ii)* biasing below the temperature compensation point (e.g., TCP in Fig. 3.25c) with possible trigger of thermal runaway of the remaining MOSFETs.

4.2.1 Structural Analysis and Operation of Partially Recovered Devices

The device was then characterized with the same SMU for reusing. Fig. 4.11 shows the transfer characteristics at $V_{DS} = 6$ V, comparing a new device and the recovered device from Fig. 4.10c. For illustration, at $V_{GS} = 12$ V, the comparison shows a decrease of only 20% in I_D for the recovered device, which proves the potential re-usability of the device. Afterwards, the plastic case of the device was opened by laser ablation followed by terminal chemical etching on the encapsulation resin. Fig. 4.12a shows the degraded die, with a very clear indication of severe damage to the top metal having accumulated in the proximity of the external gate-ring source-metal structural boundary. Lock-in-thermography analysis was also carried out, Fig. 4.12b, which confirmed the abnormal heating of the cracked gate fingers around the corner region, where mechanical stresses are likely to be highest during the short-circuit. After opening, the device was re-used within a circuit, at reduced drain-source bias, and it was still able

of conducting correct transient operation, as demonstrated by the results in Fig. 4.13, which refer to a single short-circuit pulse. It can be seen that the channel saturation current is reduced by 37% after the recovery gate-source process described above, as a result of the lowering of the $I_{DS}(V_{GS})$ curve presented in Fig. 4.11.

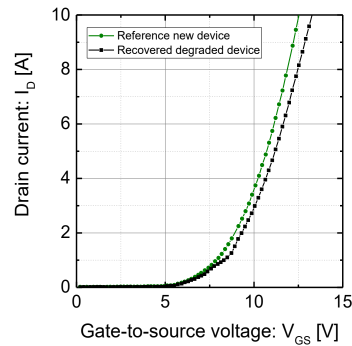
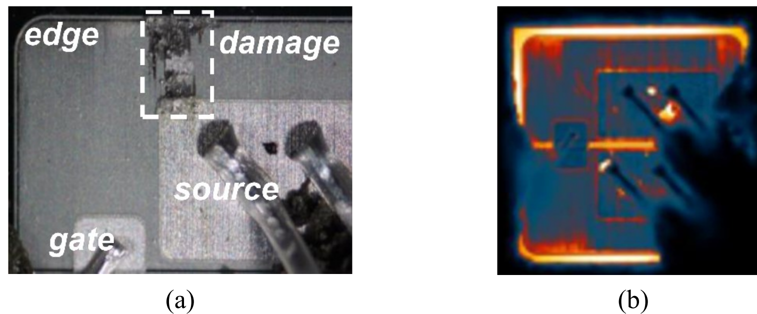


Fig. 4.11 Comparison of the transfer characteristic of the degraded device after recovery and of a new device of the same type. the curves were measured at V_{DS} = 6 V and T_{CASE} = 25 °C.



(a) (b)

Fig. 4.12 (a) Photograph of degraded device chip featuring damage accumulation at the boundary between gate-ring and source metal, (b) LIT analysis at V_{GS} = 10 V, I_{GSS} = 10 mA, I_{DS} = 1 A – 25 Hz.

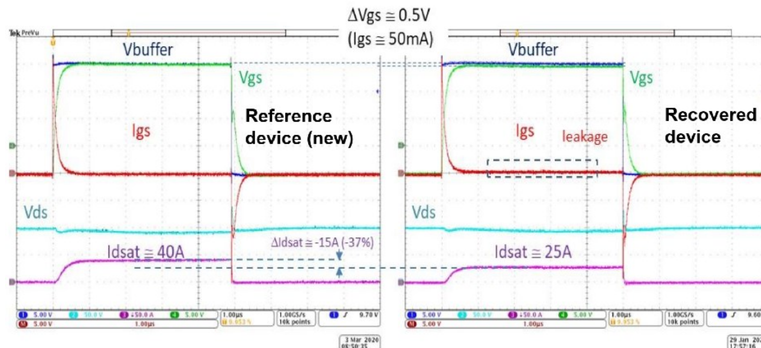


Fig. 4.13 Single-pulse short-circuit test (V_{DS} = 100 V; V_{GS} = 15 V, R_{GATE} = 10 Ω, T_{CASE} = 25 °C): comparison of new reference device (left) and degradation-recovered device (right).

4.3 Drain Leakage Path after SC-stress

As schematically illustrated in Fig. 4.14, a typical planar-gate SiC power MOSFET features at least 4 possible gate current leakage paths over the gate-oxide.

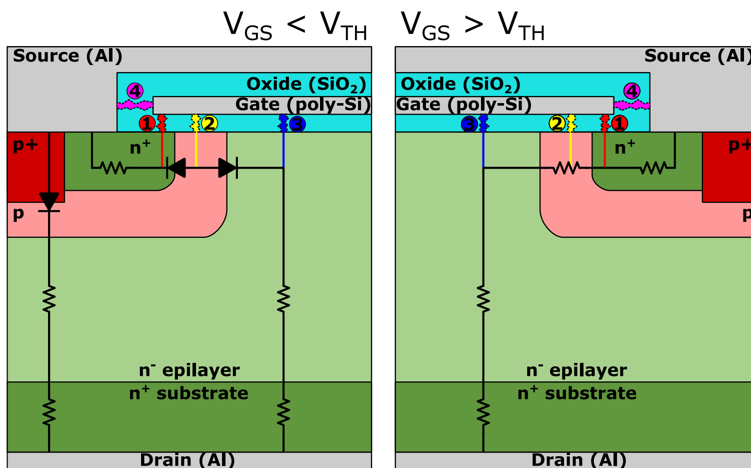


Fig. 4.14 Schematic depiction of SiC MOSFET cross-section with indication of three possible current-leakage paths between gate and source regions and one between gate and drain.

Path 1 is represented by the gate-oxide leak to the source N+ implants regions. Path 2 is a variant of Path 1, but terminated onto the transistor channel region, in the P-well, JFET-drift regions and possibly the body diode, too. Path 3 is a direct leakage path through the inter-cells gate-oxide and terminating directly onto the N- drift region. Finally, Path 4, the one which received most attention in specialist literature, is created between the gate-polysilicon and the top-side source metallic contact and through the SiO_2 interlayer-dielectric region (ILD). Paths 1, 2 and 4 close onto the source terminal, either directly the metal or the channel region. Path 3 directly onto the drain.

When the devices are degraded after repetitive short-circuit stress, the permanent gate-leakage current increases significantly and shows a pronounced dependence on the value of applied V_{GS}. Results presented here were obtained under relatively high values of the gate bias-voltage, ranging from 18 V to 23 V, on the same component, to amplify the electrical stress. The nominal gate-source voltage recommended by the manufacturer is 20 V and the maximum is 25 V in repetitive or static bias conditions. Over-biasing the gate during short-circuit with 600 V applied between drain and source leads to an excess current and power density applied to the chip ranging from 205 A for V_{GS}=18 V to 325 A for V_{GS}=23 V: an increase of 60% on the peak saturation current amplitude. However, as V_{GS} is increased from 18 V to 23 V, an additional new observation is made, which is well illustrated by the results of Fig. 4.15.

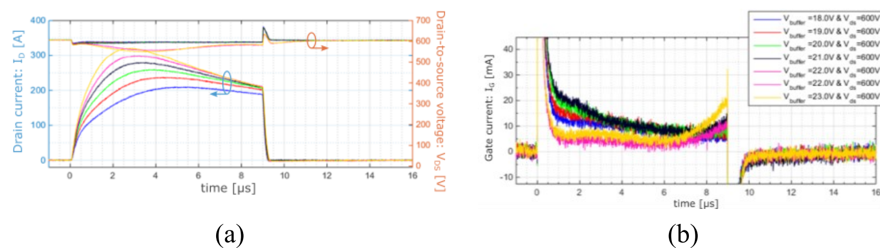
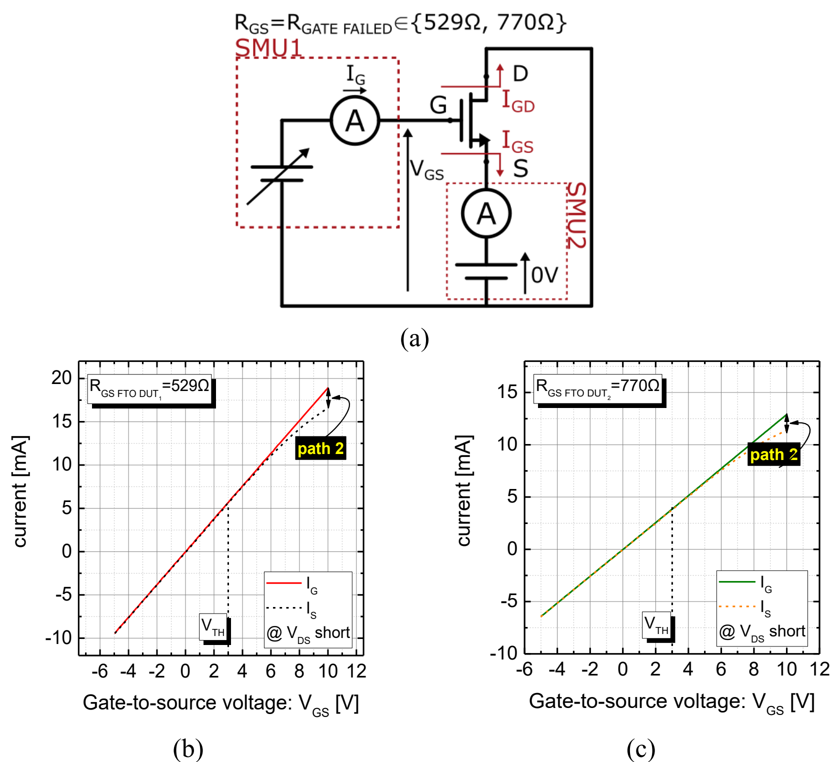


Fig. 4.15 (a) Short-circuit drain current (left) and drain-source voltage (right) and (b) corresponding gate leakage current for different values of gate-source bias voltage, between 18 and 23 V, at 25°C.

In Fig. 4.15a, a pronounced drop in V_{DS} can be observed with increasing V_{GS}; this, in turn, leads to a corresponding major drop of the

gate leakage current value in the initial portion of the SC pulse, as clearly visible in Fig. 4.15b. To further clarify this observation, offline measurements were carried out on degraded devices, that is, devices which had undergone a stress sequence as per Fig. 4.15.

The test setup and some representative test results are shown in Fig. 4.16: the DUTs, two SiC MOSFETs, had been previously stressed with different high V_{GS} values (21 and 23 V) and featured different degradation states, measured in terms of gate-source resistance of 529 Ω and 770 Ω, respectively.



(b) (c)

Fig. 4.16 (a) Schematic of experimental setup for static measurement of gate leakage and source currents for devices gate-degraded under short-circuit stress. (b) Current as a function of gate-to-source bias for the device stressed with SC pulses at V_{GS} = 21 V and (c) at V_{GS} = 23 V The solid line is the current measured at the gate terminal; the dashed line is the current measured at the source terminal. The two curves start to diverge at higher values of V_{GS}. The drain was shorted with the source in these tests.

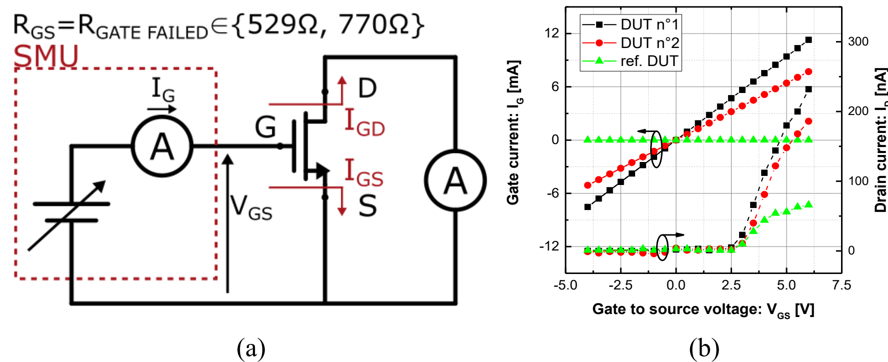
It should be noted that these gate resistances are 2 to 3 times lower than those measured in Section 4.1, which clearly shows the correlation between the power density applied to the chip and the impact on its accumulated gate damage, for the same stress-application time, which is between 9 μs and 10 μs. Obviously, as a result, the chip generally ages faster in repeated short-circuit cycles, a few cycles (<10) at V_{GS} = 23 V, are sufficient, whereas in Section 4.1, at V_{GS} =18 V, the chip could withstand almost 1000 cycles without significant damage. As per Fig. 4.16, a measurement of the leakage current as a function of V_{GS} for these devices (indicated as DUT_1 and DUT_2) reveals, the presence of a gate current component not terminated onto the source, as highlighted by the divergence of the gate and source current values as V_{GS} is increased. Such component, which becomes significant well beyond the nominal threshold voltage value V_{TH} = 3 V, is assumed to involve the channel region via Path 2, rather than Paths 1 and 4, which bypass the channel, and to be directly flowing into the drain region.

The fact that such leakage component no longer appears if $V_{GS} < V_{TH}$ indicates that Path 3 is not involved in this leakage mechanism.

The measurements in Fig. 4.16 were carried out with a two-channel source-meter unit (Keysight™ B2902A SMU). One measured the leakage I_G through the gate and the other measured the return leakage current I_S through the source. The difference of such currents is $I_G – I_S = – I_D$, that is, a leakage current component over the drain. However, as the total gate leakage current is of relatively high value, I_G = 23 V/530 Ω ≅ 43 mA, it is necessary to keep a high current range on both channels. This constraint greatly reduces the accuracy of the measurement on the current difference.

To circumvent this constraint and increase the measurement accuracy, the test setup illustrated in the schematic circuit of Fig. 4.17a was used: here, the second channel of the SMU is replaced by a precision ammeter (Keysight™ 34461A) in the drain-source loop, with a measuring range adapted this time only to the measurement of the leakage current trough the drain. Measurements were carried out again on DUT_1 and DUT_2 and this time also compared with a measurement onto a new device of the same type (ref. DUT), serving as benchmark reference. As shown in Fig. 4.17b, this new measurement confirms the first observation, that is, a significant current leakage of several hundred

nano-amperes as soon as V_{GS} approaches V_{TH}, confirming the existence of a leakage through the channel and the JFET-drift region via Path 2. Still, no leakage is measurable if the gate voltage is negative. In this case, if the device is left for a long time unbiased, the value of leakage current reduces significantly as compared to the value just after stress. This result thus tends to show that leakage by the ILD, as widely studied in the bibliography, is not the only path involved and that gate-oxide is also involved. In this mechanism, it should be noted that the body diode cannot conduct because it is short-circuited by the very low resistance of the drain measuring circuit, which consists of an ammeter without any threshold voltage, as it is not an SMU channel. An accurate failure analysis in the gate-oxide region is required to definitively confirm these results and analysis. That is quite complex due to the oxide being very thin and fine cracks very difficult to localize by classical methods such as lock-in thermography or Optical Beam Induced Resistance Change. The Al source metallization on top of the chip provides a shield which weakens the sensitivity of failure detection.



(a) (b)

Fig. 4.17 (a) Direct measurement of gate-drain current leakage with dedicated test setup applied on a gate-damaged device and (b) resulting curves.

Another consequence of the gate-damage failure-mode was also explored. In Fig. 4.18, when the drain is biased at high voltage, but with V_{GS} = 0 V or V_{GS} open, the leakage current is significantly higher than the value of the new reference device. At V_{DS} = 400 V, the leakage of a damaged device is 5 nA whereas it is less than 50 pA on a new device. This leakage was also partially highlighted in [Che20] with a comparable value, on a different reference DUT, but with the same

voltage rating and comparable active surface area, also subjected to a comparable energy stress level. However, its origin has yet to be found. Several hypotheses can be put forward: either *(i)* a small crack in the gate oxide of the JFET intercellular region: this defect path would parallel the defect in Path 2 discussed above; or *(ii)* a damage of the peripheral regions (i.e., field oxide and nitride at the top of the chip) of the device due to the thermomechanical stress applied in short-circuit operation. However, this measurement on a damaged component is not always stable within the same measurement or reproducible from one test to another. This problem is frequently encountered when electrical characteristics are measured on a component whose damaged state is not fully stabilized, particularly when it involves metallurgical and mechanical phenomena whose relaxation and diffusion constants may be long or evolving.

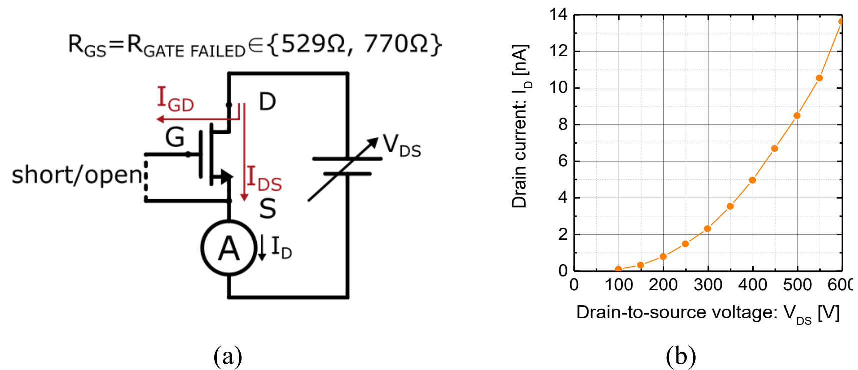


Fig. 4.18 (a) Direct measurement of drain-gate current leakage with $V_{GS} = 0$ V applied (shorted/opened gate-source gives the same results) and (b) resulting I_D - V_{DS} characteristic.

4.3.1 Optical Analysis of The Failure Mode

Finally, lock-in thermography tests on degraded devices indicated leakage not only on the running-gate finger: hot-spots on the active area are also detected, clearly visible in the results of Fig. 4.19a. It is interesting to note that, in this case, too, just as highlighted in [Che20], the devices feature partial recovery of the accumulated damage by ad-hoc off-line biasing, Fig. 4.19b. drain to source has also been observed at high drain-to-source bias (> 100 V). This might be

attributed either to a crack in the gate oxide or to a damage in the termination region of the device.

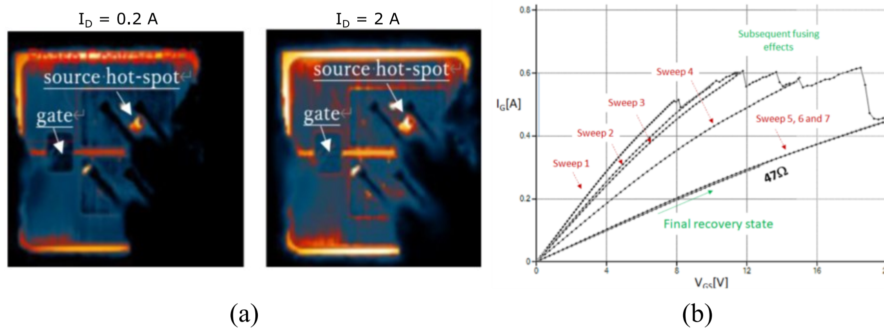


Fig. 4.19 (a) Lock-in thermography on degraded chip, under different drain current values for the same V_{GS} bias: next to leakage in the running gate-finger, a hot-spot on the source pad is also detected. (b) Progressive recovery effect by dedicated off-line tests (right), with the device reaching a final stable state (characterized however by excessive gate leakage current for realistic use in application).

4.4 Summary

A type of failure due to SC stress that is peculiar to SiC MOSFETs, and not observed in Si devices, has been studied in this Chapter. A commercial 1.2 kV – 80 mΩ SiC planar MOSFET that consistently showed this kind of failure has been identified. This failure mode results in a MOSFET with a partial short circuit between gate and source but that still retains the capability of blocking the current between drain and source. Therefore, the failure type is referred to as fail to open (FTO), and it is of interest for the parallel connection of multiple devices. The main advancements and findings can be summarized as follows.

- A transient gate leakage current of few mA is a salient precursor of failure during short circuit stress. the FTO occurs after repetitive short circuit tests with a pulse width comparable to the time at which the gate leakage current starts to rise, and a permanent gate leakage current of few mA is observed.
- Degradation and failure are the result of the creation of cracks in the top SiO_2 as a consequence of high thermo-mechanical stress and subsequent temperature-related extrusion of the top metallization.

- Thanks to the multicellular structure of power devices, it is possible to partially restore the functionality of the gate structure by proper electrical biasing. The device recovery has been implemented in an off-line setup by means of a simple pulsed mode source-meter-unit, by progressively increasing the gate current limit. This operation is only possible if the gate is not already damaged too severely. In addition, it was found that the voltage and injected recovery energy should be high enough to eliminate the main ohmic paths to be used at nominal gate voltage, but not so high as to cause excessive metal diffusion within the cracked oxide, which would yield a permanent short-circuit between the control terminals. The current level of controllability does not currently allow to exploit the recovery in real power conversion systems and further studies are necessary to assess its on-line feasibility.
- Measurements conducted on devices with different grades of degradation have shown the insurgence of a drain leakage current that does not flow through the source of the device. The occurrence of such a current only for values of gate bias above the threshold voltage suggests that the damaged area of the device also involves the gate oxide above the channel region. However, an accurate, yet nontrivial failure analysis is necessary to confirm this finding and exactly locate the damaged region. Furthermore, leakage current flowing from drain to source has also been observed at high drain-to-source bias (> 100 V). This might be attributed either to a crack in the gate oxide or to a damage in the termination region of the device.

Chapter 5

Guidelines for Parallel Connection of SiC MOSFETs

5.1 Impact of Parameters Spread on Parallel Devices During Conduction and Switching Operation

The objective of this section consists in identifying the key factors affecting the uneven current sharing and power dissipation occurring among parallel-connected SiC MOSFETs. The analysis focuses both on inherent device parameters and on assembly related power module parameters and their impact is quantified by both circuit simulations and analytical considerations.

The selection of the influencing parameters depends on what is the target of interest (e.g. avalanche robustness, long-term reliability, and efficiency). The requirement for improving the lifetime of multichip based SiC modules is that of minimizing the overstress endured by some devices due to asymmetrical electrothermal operating conditions. First, it is important to gain an understanding of what are the physical phenomena leading to such an asymmetrical behavior and what parameter variations are triggering such phenomena.

When using parallel transistor in hard switched applications, the current imbalance can occur both during the on-state (referred to as uneven static current sharing) and during the commutation phases (referred to as uneven transient current sharing). While both phenomena are detrimental because they produce unequal shares of power dissipation among the parallel units, the latter can also result in current overshoots during turn-on and turn-off that push the device out of the safe operating area (SOA). Straightforward precautions include current

derating and enhanced cooling effort. However, the former results in underexploited device performance while the latter might have a negative impact on the size and cost of the final system.

The differential quantities defined in Table 5 have been adopted as indicators of the electrothermal imbalances. The current spread indicators provide instantaneous information about the current distribution in the parallel configuration and they are important to check whether a device within the module is operating outside the boundaries of the SOA. Despite some devices have a certain degree of ruggedness against out-of-SOA operation, a repetitive violation of the current limits can promote some damage accumulation phenomena, such as the electromigration [Rah16]. Besides, the indicators associated to energy and power dissipation are more aggregate quantities, i.e., they depend on the current distribution in combination to the voltage across the device and provide information about the temperature distribution. For an arbitrary quantity x, the notation $\overline{x}$ represents the average value defined as in (5.1).

$$\overline{x} = \frac{\sum_N x_i}{N} \quad . \qquad (5.1)$$

TABLE 5 IMBALANCE INDICATORS OF RELEVANCE FOR SWITCHES OPERATED IN PARALLEL

Indicator type	Indicator	Formula	Description
Static	$\Delta P_{DC\%}$	$\frac{\lvert P_{DC1} - P_{DC2} \rvert}{\overline{P_{DC}}} \times 100$ (5.2)	Static power dissipation spread. The instantaneous power dissipation (P_{DC}) is evaluated as in (5.6).
Dynamic	$\Delta I_{ON\%}$	$\frac{\lvert I_{ON1} - I_{ON2} \rvert}{\overline{I_{ON}}} \times 100$ (5.3)	Current spread evaluated when the maximum current difference occurs during the turn-on transient.
	$\Delta I_{OFF\%}$	$\frac{\lvert I_{OFF1} - I_{OFF2} \rvert}{\overline{I_{OFF}}} \times 100$ (5.4)	Current spread evaluated when the maximum current difference occurs during the turn-off transient.
	$\Delta E_{SW\%}$	$\frac{\lvert E_{SW1} - E_{SW2} \rvert}{\overline{E_{SW}}} \times 100$ (5.5)	Switching energy spread. E_{SW} represents switching energy and it is calculated as in (5.7).

The static power dissipation is simply evaluated as in (5.6), while the switching energy is calculated according to (5.7). For the turn-on interval, the integration limits, $t_{ON,i}$ and $t_{ON,f}$, correspond to the instants in which $V_{gs}(t)$ increases to 10% of its final value ($t_{ON,i}$) and $V_{ds}(t)$ drops to 10% of its initial value ($t_{ON,f}$). Similarly, the instants $t_{OFF,i}$ and $t_{OFF,f}$ are identified by a 10% reduction of $V_{gs}(t)$ from its on-state value ($t_{OFF,i}$) and an increase of $V_{ds}(t)$ to 90% of its off-state value ($t_{OFF,f}$), respectively.

$$P_{DC} = V_{DS,on} \times I_{D,on} \tag{5.6}$$

$$E_{SW} = \underbrace{\int_{t_{ON,i}}^{t_{ON,f}} V_{ds}(t) \times I_d(t)dt}_{E_{on}} + \underbrace{\int_{t_{OFF,i}}^{t_{OFF,f}} V_{ds}(t) \times I_d(t)dt}_{E_{off}}. \tag{5.7}$$

For example, considering the circuit of Fig. 5.1, where 2 parallel MOSFETs share the current of a clamped inductive load, there are several parameters whose fluctuations may affect the spreads introduced in Table 5.

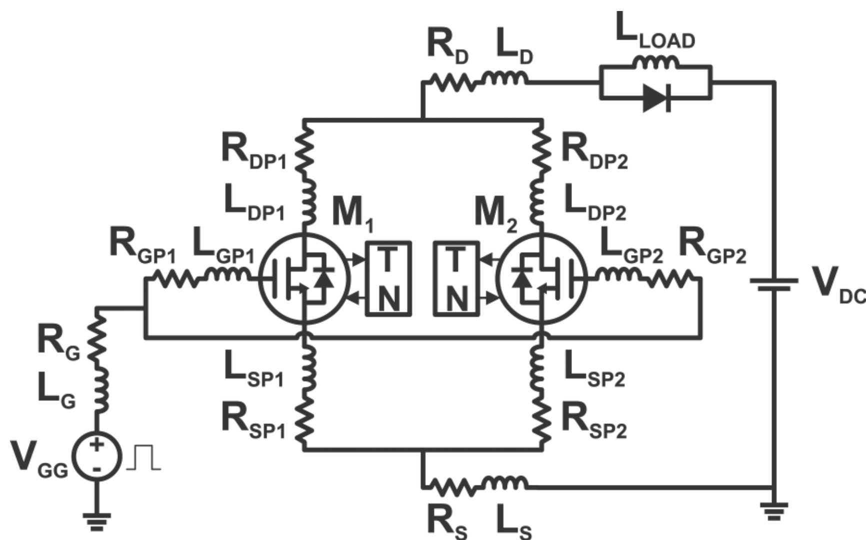


Fig. 5.1 Schematic representation of two parallel MOSFETs sharing current during clamped inductive load.

From the perspective of a module or circuit designer, the influencing parameters can be categorized into inherent device parameters (e.g., threshold voltage - V_{TH} - and on-state resistance - R_{ON} -) and assembly related parameters (e.g., parasitic inductances and resistances). The former may vary due to the random fluctuations associated to the semiconductor technological process, while the latter can change due to the asymmetries in the circuit design, tolerances of the components and of the manufacturing process. A detail must be discussed about the MOSFET on-resistance R_{ON}, since in most of the literature is considered as variable parameter for the statistical analysis. Although R_{ON} is a common and easily evaluable parameter to refer to, with this approach a problem arises because R_{ON} is itself dependent on V_{TH}. Therefore, the current factor, K, is used instead of R_{ON} to account for the uneven static current partition due to physical and geometrical statistical fluctuation. Indeed, it depends mainly on the MOSFET aspect ratio, channel electron mobility and properties of the gate oxide. Furthermore, K is a direct parameter of the SiC MOSFET compact model presented in Chapter 2 and used in this analysis. In the following, the subset of MOSFET parameters used for statistical analysis are K, V_{TH}, C_{GD} (i.e., gate–drain capacitance), C_{DS} (i.e., drain–source capacitance), and C_{GS} (i.e., gate–source capacitance). Detailed discussion about the importance of these parameters is reported in [Li18], [Fab15] and [Che15]. The parameters selected for this analysis are reported in Table 6. To assess the sensitivity of the spread indicators on the variation of each of those parameters, a double pulse test (DPT) on the circuit sketched in Fig. 5.1 was simulated several times by increasing the amount of mismatch for each parameter. Specifically, denoting as x a generic parameter reported in Table 6, x_1 in (5.8) and x_2 in (5.9) represent the values parameter associated to the left and right branches of the circuit, respectively. x_{BV} is the base value of the considered parameter and HD_r represents the relative half-distance between the parameters of the left and right branches defined according to (5.10). HD_r was swept from 0 to 0.5, thus covering a relative parameter spread (Δx_r) of 100%.

$$x_1 = x_{BV} \times (1 + HD_r) \tag{5.8}$$

$$x_2 = x_{BV} \times (1 - HD_r) \tag{5.9}$$

$$\Delta x_r = \frac{x_1 - x_2}{x_{BV}} \times 100 = 2 \times HD_r \times 100. \quad (5.10)$$

TABLE 6 DEVICE AND CIRCUIT PARAMETER LEADING TO UNBALANCED BEHAVIOR OF PARALLEL SWITCHES

	Description	Parameter	Base value
Device	Threshold voltage	V_{TH}	4.77 V
	Current factor	K	0.55 A/V^2
	Drain-source capacitance	C_{DS}	2 nF
	Gate-drain capacitance	C_{GD}	0.6 nF
	Gate-source capacitance	C_{GS}	2.1 nF
Circuit	Individual gate resistance	R_{GP}	1 Ω
	Individual source inductance	L_{SP}	3 nH

TABLE 7 CIRCUIT PARAMETERS AND TEST CONDITIONS

Description	Parameter	Value
Supply voltage	V_{DC}	1 kV
Pulsed gate voltage	$V_{GG}^-; V_{GG}^+$	-5V; +20 V
Load inductor	L_{LOAD}	140 µH
Load inductor current	I_{LOAD}	160 A
Individual drain inductance	L_{DP}	0.5 nH
Individual drain resistance	R_{DP}	5 mΩ
Common source inductance	L_S	1.5 nH
Common source resistance	R_S	10 mΩ
Common gate inductance	L_G	1 nH
Common gate resistance	R_G	4.7 Ω

The effect of each of these parameters is detailed in the dedicated sections reported in the following. The main test conditions, as well as the values of the remaining circuit components are listed in Table 7. It is important to highlight that the proposed analysis is meant to show the effect of different parameters spread, but also that the numerical results strongly depend on the test conditions, such as switching speed and values of the stray components.

5.1.1 Impact of Device Parameters

1) Threshold Voltage and Current Factor

Following the modeling approach adopted in Chapter 2, the drain current of the MOSFET described by (2.20) is here written in the simplified form of (5.11). This formulation describes both the linear and saturation region of the device and from it, the impact that both K and V_{TH} have on the drain current of a single MOSFET can be comprehended.

$$I_D = \frac{K_F K}{2} \cdot \frac{[(V_{GS} + V_{TH})V_{DS} - K_F \cdot V_{DS}^2/2]}{[1 + \theta_1(V_{GS} - V_{TH})](1 + \theta_2 V_{DS})}. \tag{5.11}$$

Since these parameters affect the behavior of the device in all the regions of operation, their fluctuations will have an impact on both the static and dynamic imbalance indicators introduced in the previous section.

The threshold voltage for a 1-D MOS structure can be approximated as in (5.12) [Bal10], where k is the Boltzmann constant, ε_s is the SiC dielectric constant, T is the absolute temperature expressed in [K], N_A is concentration of the acceptor dopant, n_i is the intrinsic concentration, C_{OX} is the gate oxide capacitance, q is the electron charge and Q_{OX} is the total charge in the oxide layer. From a technological point of view, several process fluctuations can influence the value of V_{TH}, e.g., the not-perfect control of the oxide thickness or of the acceptor concentration.

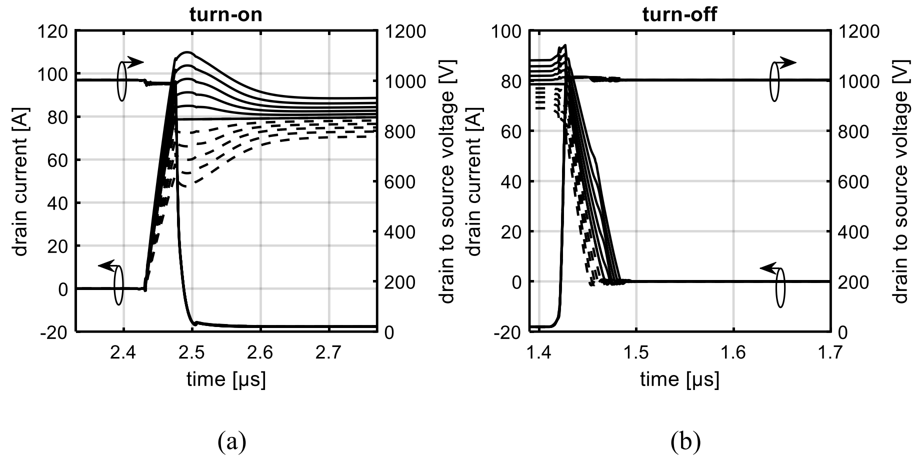
$$V_{TH} = \frac{\sqrt{4\varepsilon_s kT N_A \ln(N_A/n_i)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{OX}}{C_{OX}}. \tag{5.12}$$

The effect of V_{TH} on the current imbalance is visible in Fig. 5.2. If the external gate driving voltage is the same for all the devices (condition that will be assumed for all the scenarios tested in this Chapter), the MOSFET with the lower V_{TH} will experience a higher current flow due to a higher overdrive voltage (V_{GS} - V_{TH}), or, equivalently, due to a reduced on-state resistance, hence causing a higher P_{DC}. For the same MOSFET, an overstress will also occur during the switching transients. The phenomenon can be explained as follows. Considering the turn-on transition, if V_{GS} rises simultaneously for both switches, once it exceeds the lowest V_{TH}, the current in the corresponding MOSFET will start to increase, while the other switch will still be in the off state. Consequently, a current overshoot will develop in the first MOSFET until the second leaves the interdiction region. Similarly, the current burden during turn-off transition will also be more severe for the MOSFET with the lowest V_{TH} due to a delayed onset of the off state. Therefore, a transient current imbalance will establish during both the switching transients, which additionally leads to a difference in the switching energy dissipation.

Similar considerations can be drawn for K. Its dependence on physical and geometrical parameters is summarized by (5.13) [Bal10], where μ_n is the electron mobility in the channel and the W and L are the channel width and length, respectively.

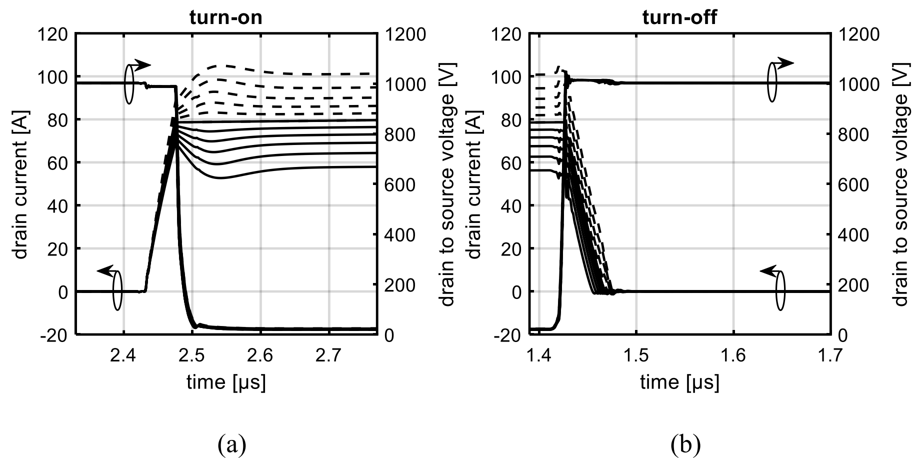
$$K = \mu_n C_{OX} \frac{W}{L}. \tag{5.13}$$

An increase in K determines a reduction of the on-state resistance, therefore, the device associated to the higher K will conduct a bigger share of the total load current. Such a difference is more pronounced during the conduction phase than the switching transients, however, a certain level of transient current spread is observed also during the commutations (Fig. 5.3).



(a) (b)

Fig. 5.2 Current imbalance during (a) inductive turn-on and (b) turn-off due to V_{TH} spread. Test conditions as per Table 7.



(a) (b)

Fig. 5.3 Current imbalance during (a) inductive turn-on and (b) turn off due to K spread. Test conditions as per Table 7.

The graphs of Fig. 5.4 report the considered imbalance indicators as a function of the relative spread for both K and V_{TH} and all of them exhibit a linear dependence on both $\Delta K_{\%}$and $\Delta V_{TH\%}$. Compared to $\Delta V_{TH,\%}$, the impact of $\Delta K_{\%}$ is more pronounced on $\Delta P_{DC\%}$ - Fig. 5.4a -, leading to a device dissipating 30% more power than the

other when $\Delta K_{\%} = 100\%$. The impact on $\Delta I_{ON\%}$ - Fig. 5.4b - is more pronounced for $\Delta V_{TH\%}$, while for $\Delta I_{OFF\%}$ the order is the opposite. However, $\Delta V_{TH\%}$, leads to a larger $\Delta E_{SW\%}$ due to a current overshoot at turn-on occurring when V_{DS} across the switch is still significant.

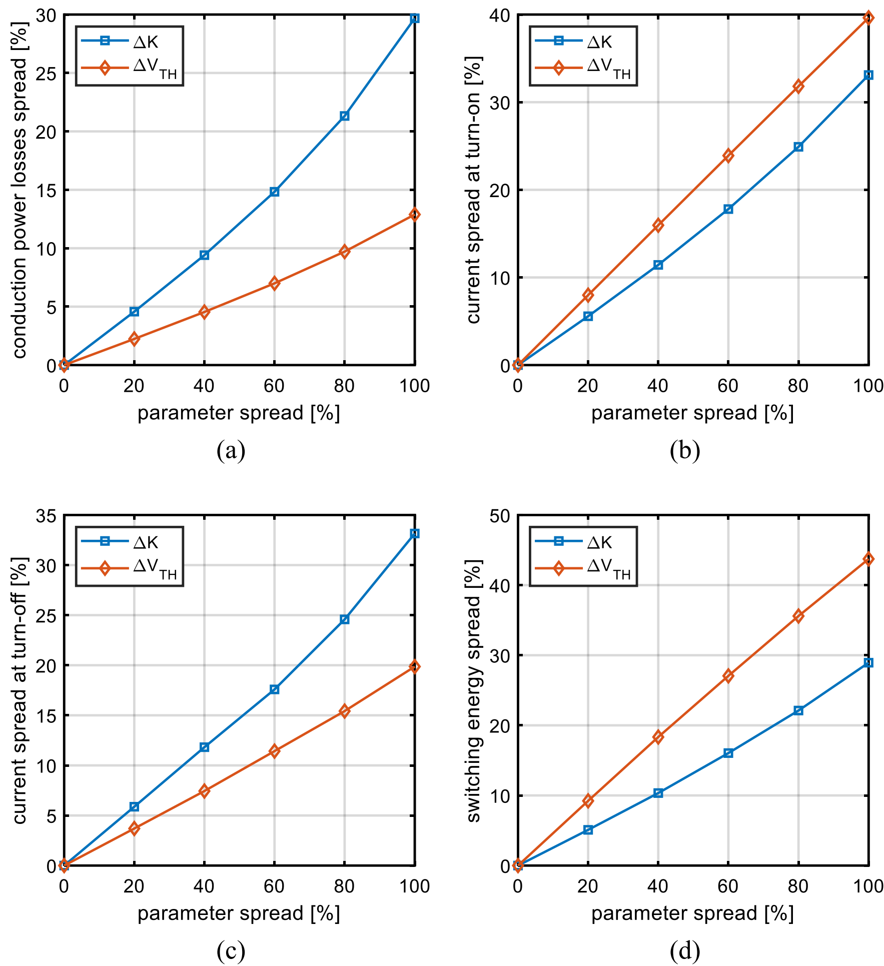


Fig. 5.4 Imbalance indicators as a function of the relative spread for both K and V_{TH}. (a) $\Delta P_{DC\%}$, (b) $\Delta I_{ON\%}$, (c) $\Delta I_{OFF\%}$ and (d) $\Delta E_{SW\%}$.

2) MOSFET Capacitances

The MOSFET parasitic capacitances influence the current and voltage changing rate during the switching transients. Therefore, they

will only affect the dynamic spread indicators and will not alter the static quantities. These capacitances are strongly nonlinear functions of the bias, with the only exception of C_{GS}, that was considered as constant according to Chapter 2. The latter is a commonly adopted approximation because, like C_{GD}, also C_{GS} is a capacitance corresponding to a MOS structure, but the voltage variation across it is much smaller than that across C_{GD} [Bal10].

In Chapter 2, the voltage dependence of C_{DS} and C_{GD} was modelled as prescribed in (2.16) and (2.17), where V_{ds}^{*} and V_{gd}^{*} are fitting parameters. Since C_{GS} is constant, its variation was achieved by simply sweeping its value. Instead, when referring to C_{GD} and C_{DS}, their variation was achieved by changing C_{GD0} and C_{DS0}. The values of the remaining parameters are $C_{DSMIN} = 0.06$ nF, $C_{GDMIN} = 0.011$ nF, $V^{*}_{DS} = 10$ V, and $V^{*}_{GD} = 2$ V, as per the calibration performed in Section 3.1.

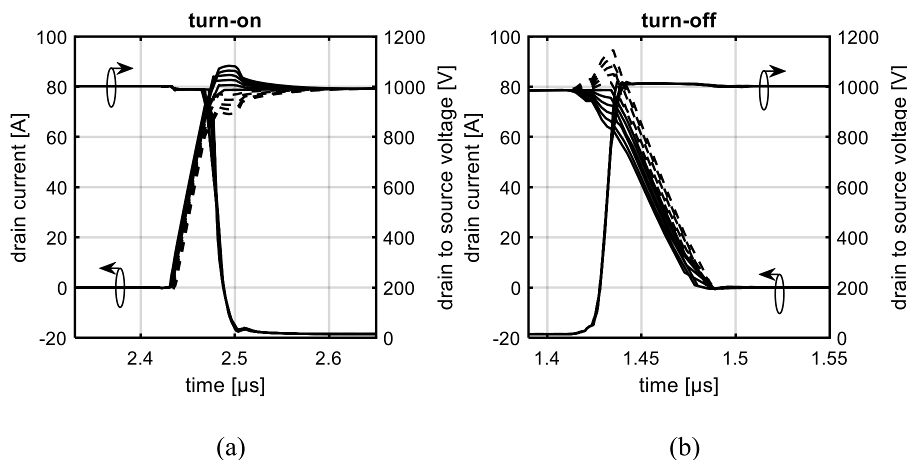
When the gate signal rises (falls), the capacitances C_{GD} and C_{GS} are charged (discharged) through the series of the gate driver resistor R_G (common to both devices) and the individual stray resistance R_{GP}, which represents both the package resistance and the gate internal resistance. The evolution over time of V_{GS} for the turn-on and turn-off transients can be described by (5.14) and (5.15), respectively. However, given the non-linearity of the capacitances, determining an exact formulation for the rise and fall time of V_{GS} is not trivial and a more detailed analysis can be retrieved from [Bal10], [Wan13].

$$V_{GS}(t) = V_{GG}^{+}\left\{1 - e^{-\frac{t}{(R_G+R_{GP})[C_{GS}+C_{GD}(V_{gd})]}}\right\} \tag{5.14}$$

$$V_{GS}(t) = V_{GG}^{-}\left\{e^{-\frac{t}{(R_G+R_{GP})[C_{GS}+C_{GD}(V_{gd})]}}\right\}. \tag{5.15}$$

Nonetheless, it is intuitive that a mismatch in C_{GS} or in C_{GD} will determine desynchronization of the two V_{GS} signals, leading to unequal turn-on and turn-off times and thus affecting the transient current distribution. An example of the current spread caused by C_{GS} mismatches is reported in Fig. 5.5. It is worth noticing that during the turn-on transient, the device with the smallest C_{GS} - solid line in

Fig. 5.5a - will endure a current overshoot due to an early commutation. Conversely, during the turn-off switching phase, the current overshoot occurs in the device with the biggest C_{GS}. This overstress alternation is also observed for C_{GD}. Consequently, the overstress periodically shifts from one device to the other and this tends to compensate the dissipation asymmetry if E_{SW} at turn-on and E_{SW} at turn-off are comparable.



(a) (b)

Fig. 5.5 Current imbalance during (a) inductive turn-on and (b) turn off due to C_{GS} spread. Test conditions as per Table 7.

The sensitivity of $\Delta I_{ON\%}$ (Fig. 5.6a) on the parameter spread is higher for ΔC_{GS} than for ΔC_{GD}, whereas $\Delta I_{OFF\%}$ (Fig. 5.6b) shows similar dependences on ΔC_{GS} and ΔC_{GD}. Nevertheless, the influence on $\Delta E_{SW\%}$ (Fig. 5.6c) is more noticeable for ΔC_{GD} than for ΔC_{GS}. In general, ΔC_{DS} was observed to have only a marginal effect on the distribution of both the transient current and of the switching energy.

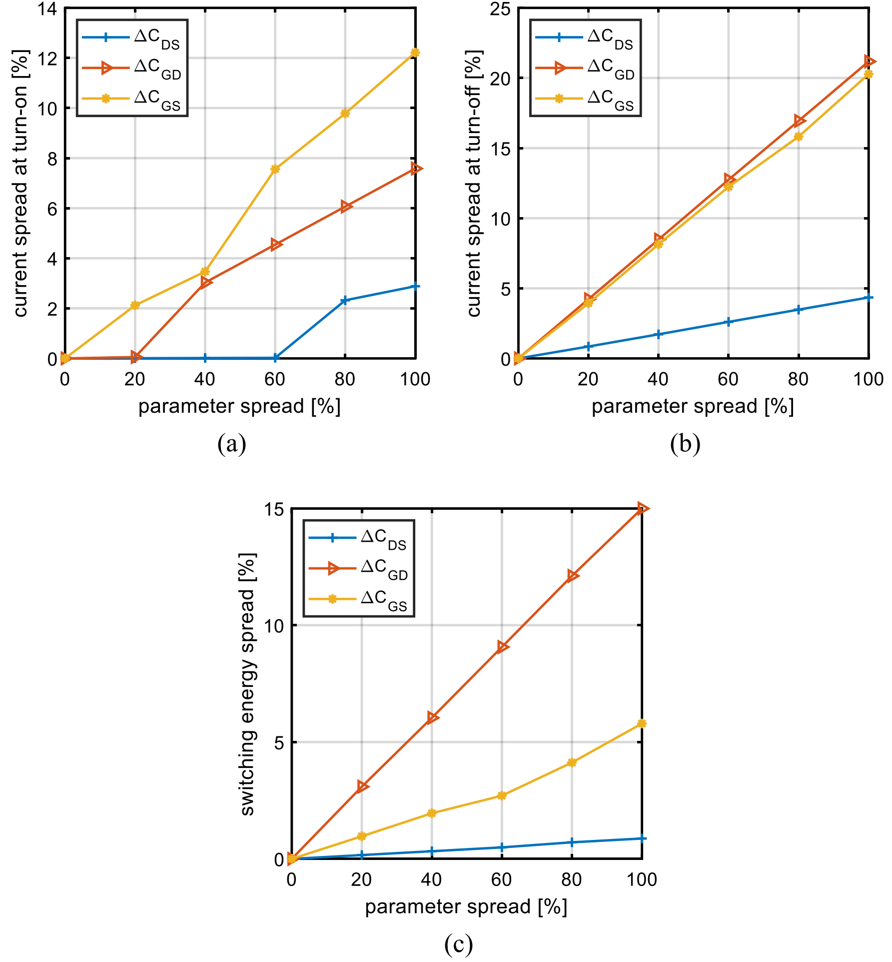


Fig. 5.6 Imbalance indicators as a function of the relative spread for C_{GS}, C_{GD}, C_{DS}. (a) $\Delta I_{ON\%}$, (b) $\Delta I_{OFF\%}$ and (c) $\Delta E_{SW\%}$.

5.1.2 Impact of Module Parasitic Parameters Spread

1) Gate Resistance and Source Inductance

The most influential non-device parameters are the individual gate resistance and source inductance.

The effect of L_{SP} is that of reducing the actual V_{GS} across the device during the drain current transients. Referring to the left branch of the circuit of Fig. 5.1, V_{GS} can be written as in (5.16). During the

turn-on phase, the transistor connected to the biggest L_{SP} will have a longer I_D rise time due to its reduced V_{GS}, thus leading to a current overshoot in the other device.

$$V_{GS1} = V_{GG}^{+} - i_G R_G - i_{GP1} R_{GP1} - L_{GP1} \frac{di_{GP1}}{dt} - L_{SP1} \frac{di_{SP1}}{dt} - i_S R_S - L_S \frac{di_S}{dt} \quad (5.16)$$

As shown in Fig. 5.7a, this current spread (ΔI_{ON}) caused by ΔL_{SP} can be significant. On the opposite, the transistor with the biggest L_{SP} will have a shorter I_D fall time during the turn-off phase. Considering the test conditions used for this analysis, ΔI_{OFF} is less sensitive to ΔL_{SP} (Fig. 5.7b).

The effect of fluctuations in R_{GP} is that of introducing different delays on the gate signal by influencing the charging and discharging rate of the MOSFET input capacitance ($C_{GS} + C_{GD}$). The MOSFET connected to the biggest R_{GP} will have slower turn-on and turn-off transitions, and therefore it will conduct more current at turn-off and less at turn-on. The impacts on ΔI_{ON} (Fig. 5.7a) and on ΔI_{OFF} (Fig. 5.7b) are comparable under the adopted test conditions.

In general, given the test conditions, the effect of ΔL_{SP} and ΔR_{GP} on the switching energy is not as significant as it was for the previous parameters.

2) Effect of Common Gate Resistance

As previously anticipated, the numerical results and the sensitivity of the various spread indicators are greatly affected by the operating conditions (e.g., load current, supply voltage and current slew-rate) and by the values of the surrounding stray components (e.g., common source and drain inductance).

This is confirmed by the data reported in Fig. 5.8, which prove that an increase in the gate driver resistor - R_G - tends to amplify the current imbalance by slowing down the switching transients. This effect is analyzed by means of simulations where three different values of gate resistance were used while introducing a gap in terms of V_{TH}.

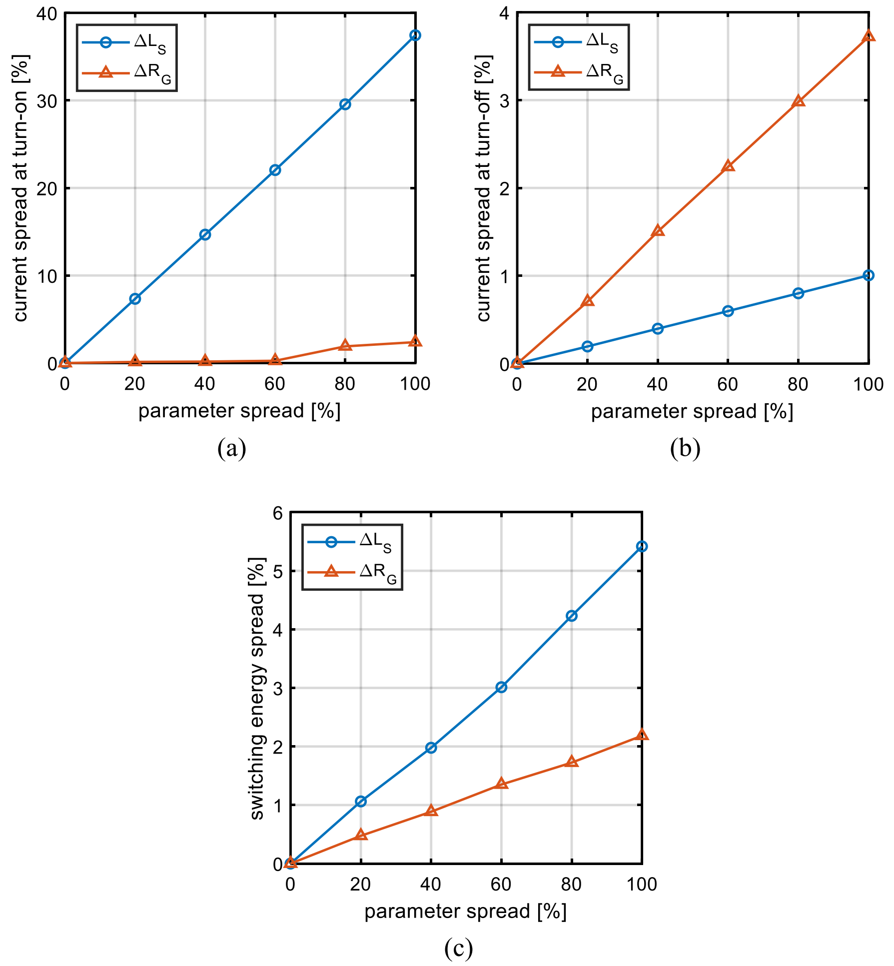


Fig. 5.7 Imbalance indicators as a function of the relative spread for L_S and R_G. (a) $\Delta I_{ON\%}$, (b) $\Delta I_{OFF\%}$ and (c) $\Delta E_{SW\%}$.

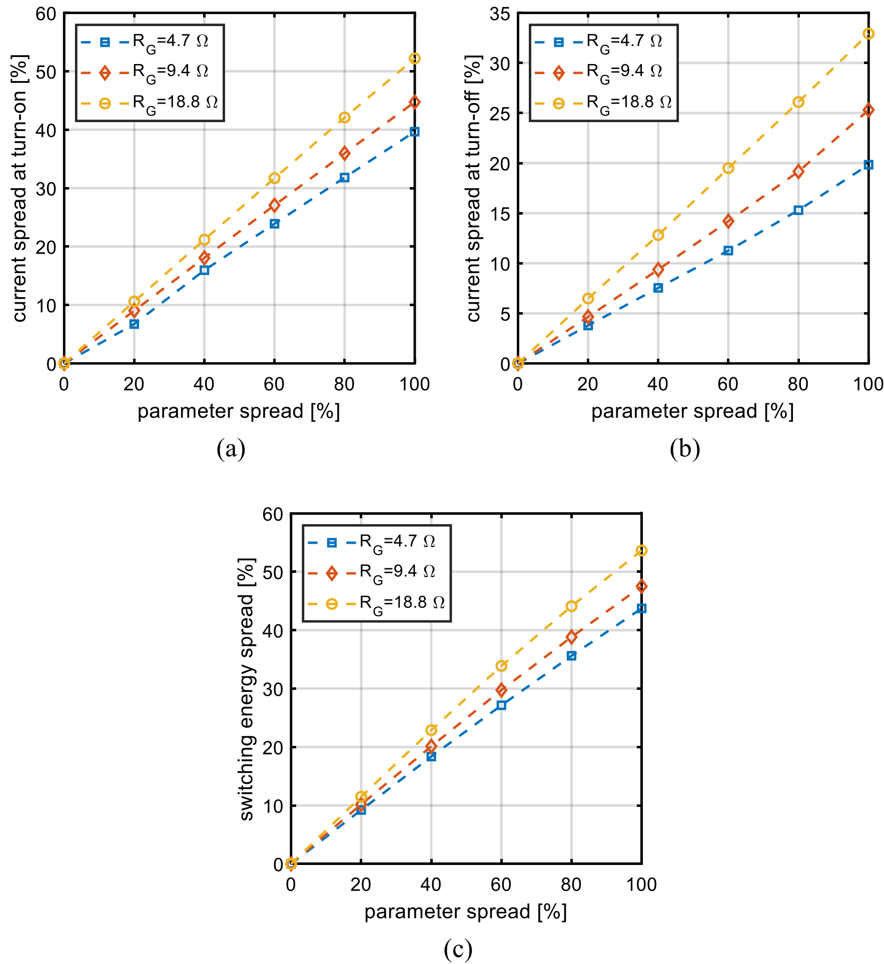


Fig. 5.8 Imbalance indicators as a function of the relative spread of VTH three different values of R_G. (a) $\Delta I_{ON\%}$, (b) $\Delta I_{OFF\%}$ and (c) $\Delta E_{SW\%}$.

5.2 Statistical Analysis of SiC MOSFETs Parameters Spread

Monte Carlo (MC) analysis is a statistical method that allows to evaluate the response of a deterministic system when one or more inputs or parameters are known with uncertainty and modelled as random

variables. MC techniques can be applied in many engineering and scientific fields, such as risk evaluation, random process simulations, yield analysis and reliability assessment. In practice, when referring to circuit analysis, it consists in the iterative repetition of a simulation with a randomly varying input. Therefore, the first necessary information for performing a MC simulation is the knowledge of the statistical dispersion of the quantities of interest and to describe it as a probability density function (pdf). This statistical description can either be built upon experimental data or come from models based on the physical phenomena underlying the manufacturing or technological process.

The pdf is fed to a random sampler that generates the random inputs for the circuit simulations. At the end of them, the outputs are usually interpreted and visualized by statistical tools. The chain of steps for the MC simulations conducted in this Chapter is outlined in Fig. 5.9.

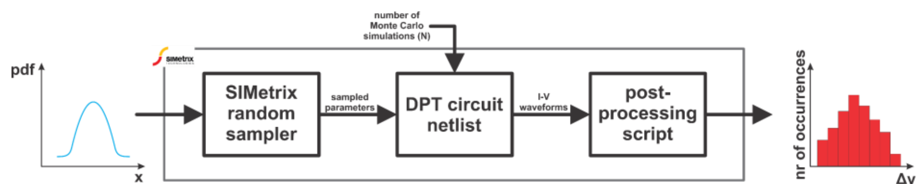
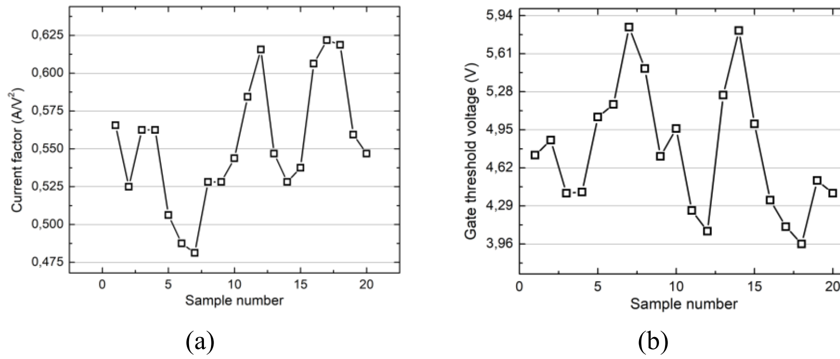


Fig. 5.9 Schematic representation of chain steps for a MC analysis.

Of the parameters reported in Table 6, an experimental characterization of K and V_{TH} was conducted on 20 MOSFETs belonging to the same production batch. The devices under test (DUTs) are second generation 1.2 kV-36 A SiC power MOSFETs by CREE (C2M0080120D) introduced in Section 3.1 and for which the model was calibrated. K and V_{TH} were evaluated by QEM as described in Section 3.1 and the resulting values are plotted in Fig. 5.10a and b, respectively. Afterwards, the values of K and V_{TH} were fitted to Gaussian distributions, whose characterizing parameters are summarized in Table 8. A comparison between the empirical and fitted CDFs (cumulative distribution functions) is provided in Fig. 5.11a and Fig. 5.11b for K and V_{TH}, respectively. For both quantities, a relative root-mean square error of 0.18 between the empirical and the fitted CDF was obtained. However, given the reduced number of tested samples, such pdf should not be intended as accurate description of

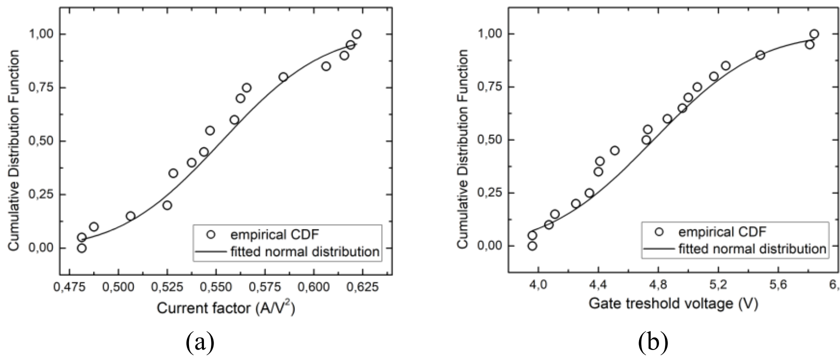
tolerances of the production process but rather as realistic spreads to illustrate the methodology detailed in the following sections.

Due to lack of experimental data, the pdfs describing the other parameters were also assumed to be Gaussian. The details about these distributions are provided in the corresponding sections.



(a) (b)

Fig. 5.10 Statistical fluctuation of (a) current factor K and (b) gate threshold voltage V_{TH} over 20 DUT samples (C2M0080120D) at room temperature.



(a) (b)

Fig. 5.11 Experimental (circle) and analytical (line) CDFs for (a) K and (b) V_{TH} of Fig. 5.10.

TABLE 8 PARAMETERS OF THE NORMAL DISTRIBUTION USED TO FIT THE DISPERSION OF K AND V_{TH}.

Mean value		Standard deviation		3σ-spread: (3σ/μ)×100
μ_K	0.55 A/V^2	σ_K	0.041 A/V^2	22%
$\mu_{V_{TH}}$	4.77 V	$\sigma_{V_{TH}}$	0.55 V	35%

5.2.1 Monte Carlo-Aided Module Design Approach

The analysis conducted in Section 5.1 investigated the effects of mismatches in inherent and external parameters on two parallel connected devices during inductive load switching. However, the non-uniformity worsen as the number of parallel devices increases and it is of primary importance to estimate the electrothermal imbalances when more than two devices are operated in parallel. Deriving an analytical formulation that relates the parameters spread to the imbalance indicators of interest is not a trivial task due the considerable number of parameters varying at the same time, the strong influence of the test conditions and the dependence on the number of connected switches. One way to estimate admissible tolerances for safely parallel multiple devices is to conduct a worst-case analysis (WCA). It consists in evaluating the circuit performance when the parameters values are at the tolerance limits (highest or lowest) that trigger the most unfavorable conditions. However, depending on the monitored quantity, the definition of the worst case might not be unique. Additionally, the WCA only provides an upper bound for the admissible tolerances [Sch16]. This might lead to derating rules or chip classification criteria that are too restrictive for SiC devices, which are still more expensive than Si counterparts. On the other hand, despite a higher complexity and the heavier time requirements, a MC-based analysis allows to better tailor the solution to the constraints.

In this section, a series of MC simulation is performed on the circuit of Fig. 5.12. This implements a clumped inductive switching test on a power module made of four parallel SiC MOSFETs. To account for the self-heating effect, each switch is connected to an instance of the equivalent thermal network - TN - presented in Fig. 3.13b (not reported in the schematic of Fig. 5.12 to improve readability). The test conditions and the values of the circuit components are specified in Table 9. Two MC campaigns were performed to analyze separately the impact of device and circuit parameters. The following two Subsections describe the outcomes of these two studies.

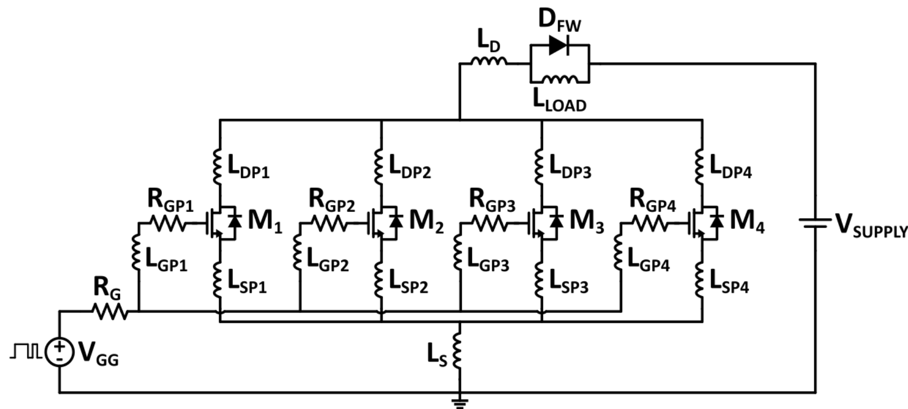


Fig. 5.12 Simplified circuit schematic used for ET simulations of the four paralleled SiC MOSFETs during double-pulse test.

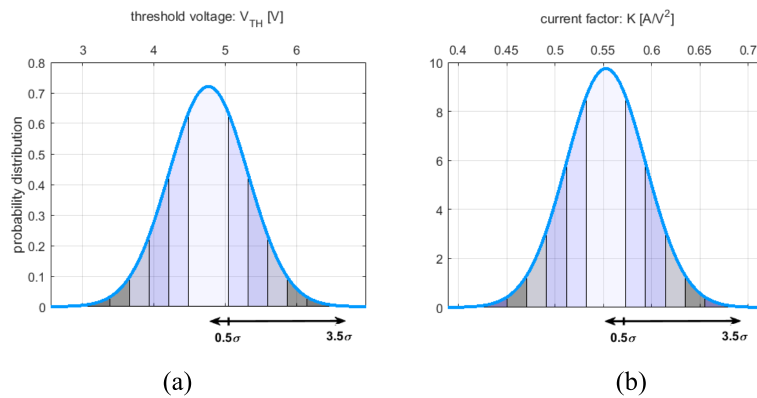
TABLE 9 DPT CONDITIONS AND CIRCUIT SPECIFICATIONS ADOPTED FOR THE MC ANALYSIS

Description	Parameter	Value
Supply voltage	V_{DC}	800 V
Pulsed gate voltage	$V_{GG}^{-}; V_{GG}^{+}$	-5V; +20 V
Load inductor	L_{LOAD}	1.9 mH
Load inductor current	I_{LOAD}	100 A
Common gate resistance	R_G	10 Ω
Test temperature	T	25°C

5.2.2 Analysis of Device Parameters

The device parameters were split into two subsets, one including K and V_{TH} and the other including the MOSFET capacitances. These two groups were studied by two separate batches of MC simulations. Starting from K and V_{TH}, their influence was investigated by considering their variations together during a set of 1200 statistically independent MC simulations and while all the other parameters were kept constant. The pdfs describing the variations of K and V_{TH} (Fig. 5.13) are those resulting from the fitting procedure of Subsection 5.2, i.e., normal distributions with (μ, σ)-pairs of (0.55, 0.041) A/V^2 and (4.77 V, 0.55) V for K and V_{TH}, respectively. Fig. 5.14 reports the turn-off waveforms of the individual MOSFETs current and

temperatures corresponding to a single simulation of the MC batch with highly mismatched parameters. The values of the latter are reported in Table 10, which witnesses that only transistor M1 has a lower V_{TH} that departs from that of the other devices. This causes a late turn-off of M1, thus forcing it to also carry the load current of the remaining devices that are already in interdiction. In this way, a significant current overshoot, and thus a temperature increase, occurs in M1.



(a) (b)

Fig. 5.13 statistical distributions of V_{TH} (left) and K (right); The shaded tolerance windows are used in the analysis of Section 5.2.4.

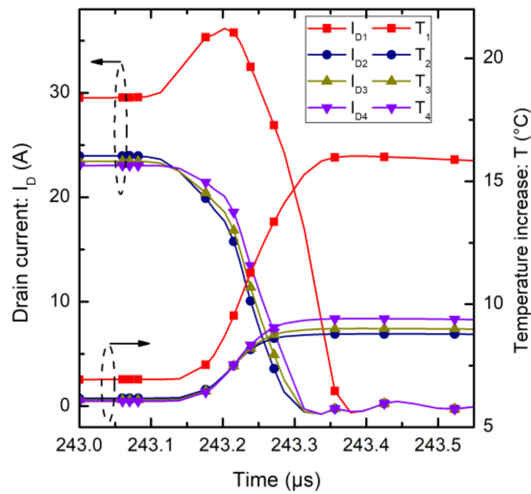


Fig. 5.14 Inductive turn-off drain current and junction temperature rise waveforms during harsh current unbalance condition.

TABLE 10 VALUES OF V_{TH} AND K CORRESPONDING TO WAVEFORMS REPORTED IN FIG. 5.14.

	M1	**M2**	**M3**	**M4**
V_{TH} [V]	3.91	5.6	5.4	5.12
K [A/V^2]	0.6	0.53	0.51	0.49

At the end of each simulation, the switching energy at turn-on (E_{on}) and at turn-off (E_{off}) were evaluated for each device as prescribed by (5.7). On average, all the MOSFETs dissipated the same amount of switching energy ($E_{on,avg}$ = 1.3 mJ and $E_{off,avg}$ = 1.79 mJ). However, this does not mean that the average energy unbalance is 0. To support this statement, it is possible to apply order statistics [Dav03] to calculate the statistical range of the switching energy (ΔE_{SWi}) as in (5.17)

$$\Delta E_{SWi} = \max\left(E_{SW1,i}, \dots, E_{SW4,i}\right) - \min\left(E_{SW1,i}, \dots, E_{SW4,i}\right) \quad (5.17)$$

where $E_{SW,i}$ represents the switching energy (either at turn-on or at turn-off) dissipated by one of the four MOSFETs at the *i-th* MC iteration.

Once all the MC simulations have been completed, it is possible to compute all the values of ΔE_{SWi} and to build an occurrence histogram to estimate the expected value of the energy spread (reported in Fig. 5.15a and 5.15b. Additionally, a histogram reporting the distribution of the maximum current peak was also calculated (Fig. 5.15c). The expected energy spreads are $E[\Delta E_{on}] = 0.72$ mJ (i.e., 55.4% of the average E_{on}) and $E\left[\Delta E_{off}\right] = 1.6$ mJ (i.e., 89.4% of the average E_{off}). The most likely drain overcurrent is $E\left[I_{D,MAX}\right] = 29$ A, which is 16% bigger than the nominal value (25 A) that would occur in case of balanced devices.

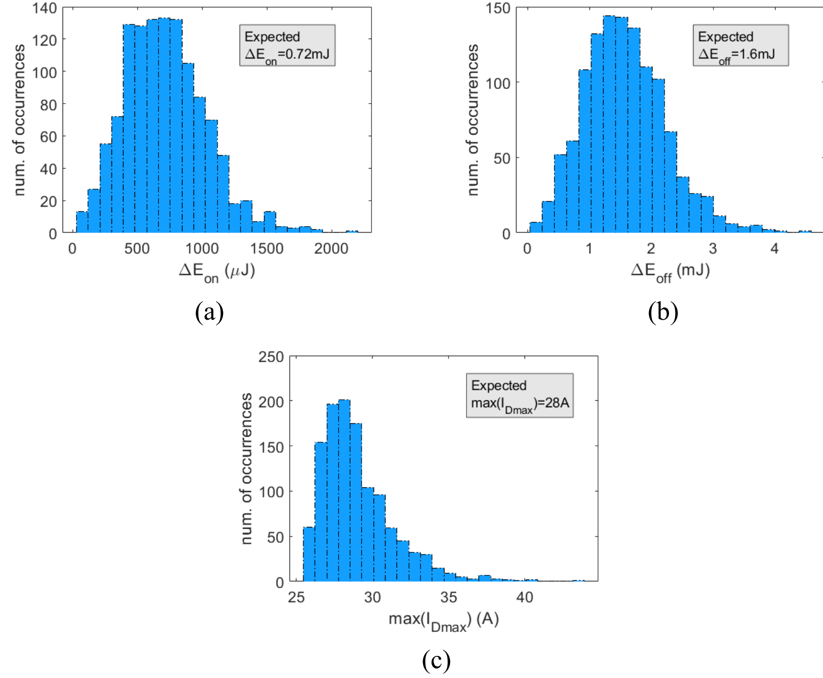


Fig. 5.15 Histograms resulting from 1200 ET MC simulations of DPT with Gaussian statistical variation of V_{TH} and K: maximum energy imbalance dissipated at (a) turn-on, at (b) turn-off and (c) maximum drain current at turn-off.

Afterwards, the MC campaign was repeated to assess the expected imbalances produced by the MOSFET capacitances, while no variation in K and V_{TH} was considered and under the same circuital conditions. The fluctuations of C_{GD}, C_{GS} and C_{DS} were modelled by normal distributions with a 3σ-spread of 50% around their mean value as summarized in Table 11.

TABLE 11 PARAMETERS OF THE NORMAL DISTRIBUTION ASSUMED FOR C_{DS}, C_{GD} AND C_{GS}.

Mean value		**Standard deviation**		**3σ-spread: (3σ/μ)×100**
$\mu_{C_{DS}}$	2 nF	$\sigma_{C_{DS}}$	0.33 nF	50%
$\mu_{C_{GD}}$	0.6nF	$\sigma_{C_{GD}}$	0.1 nF	50%
$\mu_{C_{GS}}$	1.05 nF	$\sigma_{C_{GS}}$	0.175 nF	50%

In this case, the average behavior of the circuit was reasonably close to the previous case, with $E[E_{on}] = 1.31$ mJ $E[E_{off}] = 1.76$ mJ and $E[I_{D,MAX}] = 29.8$ A (Fig 5.16c). However, the statistical ranges describing the energy spread were found to be less sensitive to the fluctuation of the capacitances, with $E[\Delta E_{on}] = 0.44$ mJ (Fig 5.16a) and $E[\Delta E_{off}] = 1.2$ mJ (Fig 5.16b).

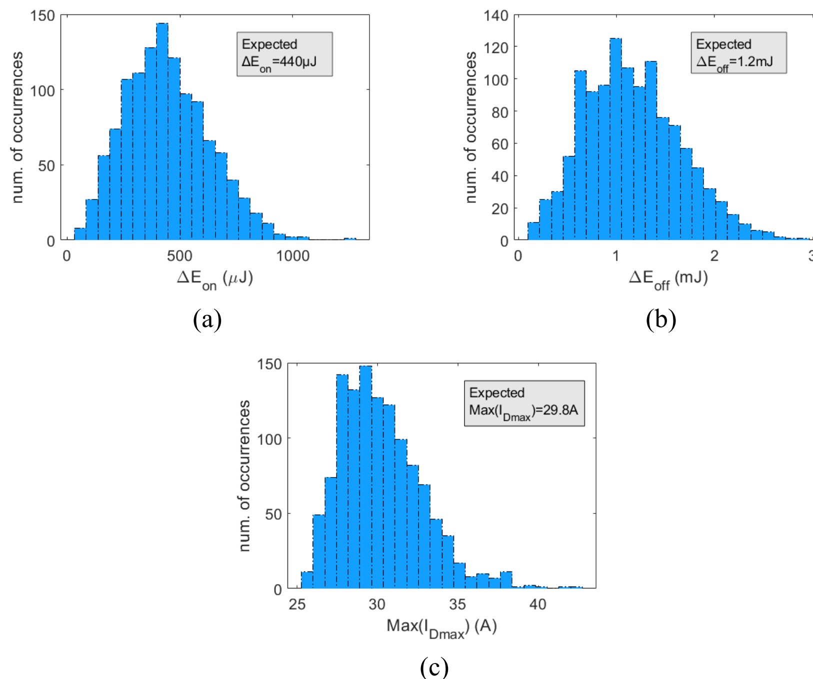


Fig. 5.16 Histograms resulted from 1200 ET MC simulations of DPT with Gaussian statistical variation of C_{GS}, C_{GD} and C_{DS}: maximum energy imbalance dissipated at (a) turn-on, at (b) turn-off and (c) maximum drain current at turn-off.

5.2.3 Analysis of Module Parasitic Parameters

Subsequently, the focus was shifted to the effect of the parasitic circuit components. These are the individual gate resistor (R_{GP}) and the individual source stray inductance (L_{SP}). For them as well, the statistical distribution chosen for conducting the study is the normal distribution

with characterizing parameters as per Table 12. Two separate sets of 1200 MC simulations were conducted for R_{GP} and L_{SP}.

TABLE 12 PARAMETERS OF THE NORMAL DISTRIBUTION ASSUMED FOR R_{GP} AND L_{SP}.

Mean value		Standard deviation		3σ-spread: (3σ/μ)×100
$\mu_{R_{GP}}$	4.6 Ω	$\sigma_{R_{GP}}$	0.74 Ω	48%
$\mu_{L_{SP}}$	7 nH	$\sigma_{L_{SP}}$	1.12 nH	48%

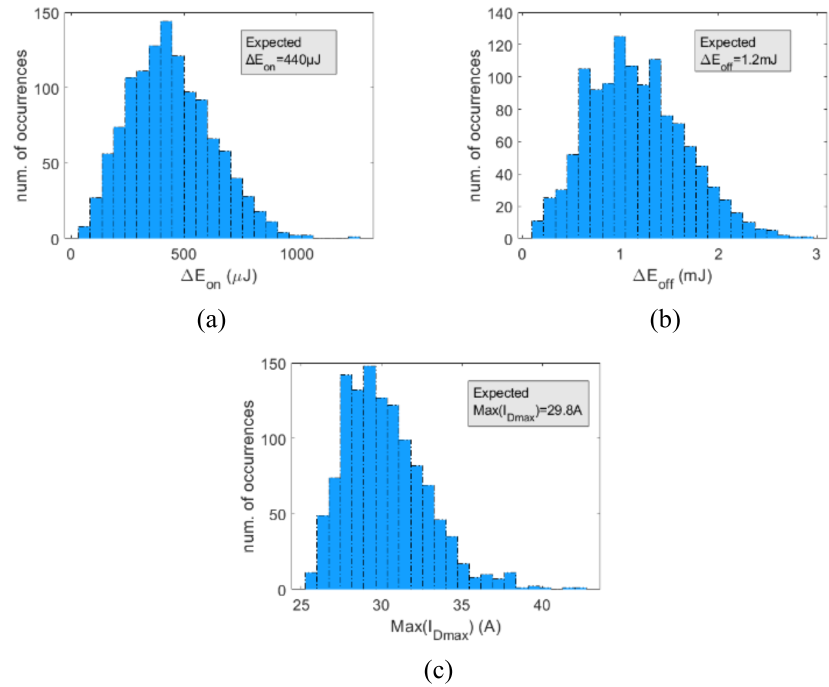


Fig. 5.17 Histograms resulted from 1200 ET MC simulations during a DPT with Gaussian statistical variation of R_{GP}: maximum energy imbalance dissipated at (a) turn-on, at (b) turn-off and (c) maximum drain current at turn-off.

The results concerning the MC simulations covering the variation of R_{GP} are reported in Fig. 5.17. The impact of R_{GP} was weaker than that of the previous parameters for all the monitored quantities. Specifically, $E[\Delta E_{on}] = 44$ m (Fig. 5.17a), $E[\Delta E_{off}] =$ 0.28 mJ (Fig. 5.17b) and $E[I_{D,MAX}] = 25.9$ A (Fig. 5.17c). However, it is worth recalling that the sensitivity to the parametric variation is

strongly influenced by the test conditions and that a high value of R_G magnifies the electrothermal imbalances by slowing down the commutations. Therefore, it is important to reduce both the spread and the mean value of the gate resistor to mitigate the current and energy imbalance.

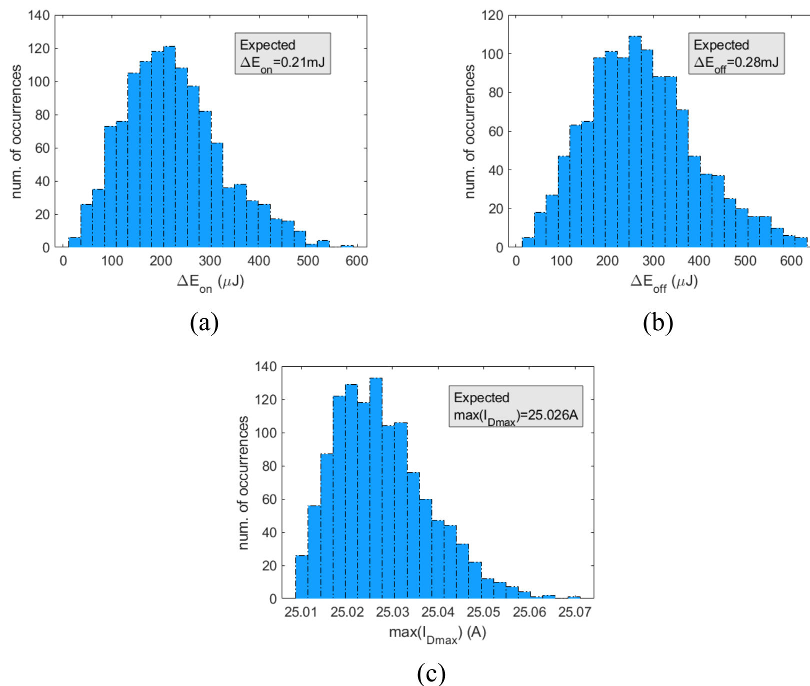


Fig. 5.18 Histograms resulted from 1200 ET MC simulations during a DPT with Gaussian statistical variation of L_{SP}: maximum energy imbalance dissipated at (a) turn-on, at (b) turn-off and (c) maximum drain current at turn-off.

As anticipated, L_{SP} influences the switching transient by introducing a negative feedback that reduces the actual gate to source voltage of a quantity $L_{SP}\times(di_D/dt)$. In principle, also the other stray inductances (L_{GP} and L_{DP}) influence the transient current sharing but, as previously reported in literature - [Lim14], [Li18] -, L_{SP} is the most critical of the three. The histograms resulting from the MC campaign for L_{SP} are depicted in Fig. 5.18 and report a statistical range of the energy at turn-off ($E[\Delta E_{off}] = 0.28$ mJ, Fig. 5.18b) and an overcurrent ($E[I_{D,MAX}] = 25.03$ A, Fig. 5.18c) that are comparable with those

produced by variations of R_{GP}, whereas the impact on ΔE_{on} given by L_{SP} ($E[\Delta E_{on}] = 0.21$ mJ, Fig. 5.18a) was more pronounced that that given by R_{GP}.

5.2.4 Guideline for Reliable Module Design

In order to extend the lifetime of electronic equipment as much as possible, it is of paramount importance to include the reliability considerations in the design phase.

When dealing with a power module (PM) made of several semiconductor chips, several failure types might determine an interruption of operation or destruction. These failure mechanisms can occur both at chip level (e.g., time dependent dielectric breakdown and body diode failure) and at package level (e.g., bond wires liftoff or fracture and cracks or voids in the solder layers) [Ni20]. In any case, while the temperature swing can trigger some of those failure mechanisms, the average temperature of operation generally acts as an accelerator for the progressive process of damage accumulation leading to the eventual failure. Given a failure mechanism characterized by an activation energy E_{aa} [eV], the mean time to failure of a semiconductor device can be expressed as (5.18), where T_j [K] is the absolute junction temperature, and k [eV/K] is the Boltzmann constant. The Arrhenius equation for reliability is commonly adopted to estimate the acceleration effect of the temperature [JED19], [Qiu17]. Specifically, the acceleration factor (AF) is defined as the ratio in (5.19), where $MTTF_1$ and $MTTF_2$ are the MTTF evaluated at T_{j1} and T_{j2}, respectively.

$$MTTF = A \cdot e^{-\frac{E_{aa}}{kT_j}} \tag{5.18}$$

$$AF = \frac{MTTF_1}{MTTF_2} = e^{-\frac{E_{aa}}{k}\left(\frac{1}{T_{j1}} - \frac{1}{T_{j2}}\right)}. \tag{5.19}$$

In the perspective of providing a tool to aid a design for reliability, a procedure to estimate the temperature imbalance arising in an array of parallel mismatched SiC MOSFETs is presented in this section. The procedure is based on repeated sets of MC simulations and it allows to select admissible parameters spreads that ensure that the

temperature dissymmetry is lower than a given threshold. The procedure is explained through the following application example.

A circuit for double pulse test, like the one of Fig. 5.12, is used to evaluate the statistical range of the switching energy for a PM subjected to some parametric variations.

In this example, seven batches of 1600 MC simulations were performed consecutively with V_{TH} and K set as the random parameters and varying according to the distributions described in Subsection 5.2.2. However, the pdfs set for each batch of MC simulations are first truncated over a certain tolerance window and then fed to the random sampler (Figs. 5.13 and 5.19). In this way, samples falling outside the tolerance window are rejected, thus allowing to evaluate appropriate screening boundaries. Specifically, let us consider a PM made of four parallel MOSFETs switched at a total load current of I_{LOAD} = 80 A. The width of tolerance interval for the distributions of K and V_{TH} was swept from 1σ to 7σ (Fig. 5.13 and 5.19) with a 1σ-step. The remaining test and circuit parameters are summarized in Table 13.

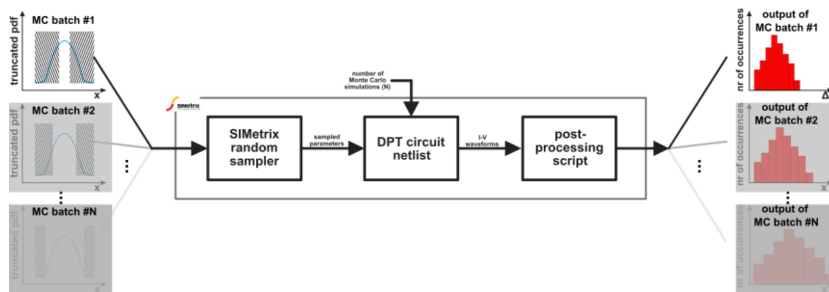


Fig. 5.19 Flowchart of the procedure based on successive batches of Monte Carlo simulations iterated by truncating the parameters distribution on an interval of increasing width.

An example of the resulting histograms of the turn-off energy is reported in Fig. 5.20. As already observed, the average turn-off energy is reasonably similar for all the MOSFETs of the array, and it is only marginally altered when the tolerance for K and V_{TH} is increased from 1σ (Fig 5.20a) to 4σ (Fig 5.20b). On the other hand, a clear impact on the dispersion of E_{off} is present, with the standard deviation growing from 65 μJ (Fig 5.20a) to 160 μJ (Fig 5.20b). Once a batch of MC

simulation is completed, the power dissipation is converted into a temperature imbalance via (5.20).

$$\Delta T = [\Delta E_{sw} \times f_{sw} + \Delta P_S \times D] \times R_{th}. \tag{5.20}$$

TABLE 13 DPT CONDITIONS AND CIRCUIT PARAMETERS.

Description	Parameter	Value
Supply voltage	V_{DC}	800 V
Pulsed gate voltage	$V_{GG}^{-}; V_{GG}^{+}$	-5V; +20 V
Load inductor	L_{LOAD}	142 µH
Load inductor current	I_{LOAD}	80 A
Common gate resistance	R_G	10 Ω
Individual gate resistance	R_{GP}	2.5 Ω
Individual source inductance	L_{SP}	9 nH
Common source inductance	L_S	12 nH
Test temperature	T	25°C

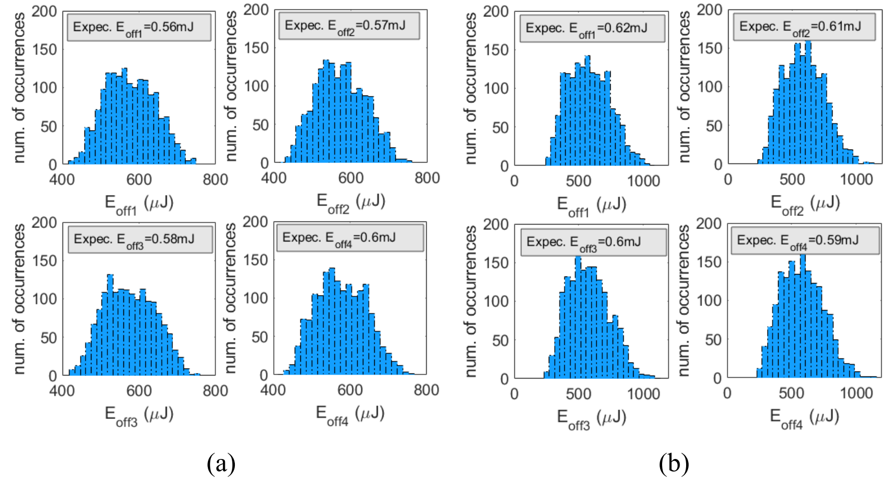


Fig. 5.20 Histograms of the turn-off dissipated energy resulted from 1600 MC ET simulations for the four MOSFETs at I_{LOAD} = 80 A; K and V_{TH} distributions truncated at (a) μ ± 0.5σ and (b) μ ± 2σ.

In it, ΔE_{sw} is the most likely switching energy imbalance, ΔP_S is the spread of static power dissipation, f_{sw} is the switching frequency, D is the duty cycle (assumed to be 0.5) and R_{th} is the thermal resistance

of the power module. Even if (5.20) is based on the approximation of the thermal problem to a 1-D equivalent, and more complex approaches could be used [Cod14], [Mag16] (see Chapter 6), such a simplification allows to develop an easy-to-use rule for screening the devices before parallelization.

The temperature imbalance was evaluated for different switching frequencies and assuming $R_{th} = 0.6\,K/W$. The resulting values are reported in Fig. 5.21 and show that ΔT tends to saturate once the width of the truncation window exceeds 4σ.

The curves of Fig. 5.21 can be used to guide the selection of the devices or to set an upper bound for the switching frequency. For example, if $\Delta T = 40$ °C is the temperature imbalance that ensures a certain desired lifetime, the data of Fig. 5.21 highlights that this is always possible if the PM is switched below 50 kHz. Conversely, if a switching frequency of 100 kHz or 200 kHz is required, then the parameters variability must be confined within 3.2 σ and 1.2 σ, respectively.

In this way, the allowable parameter spread can be identified, and thus, the devices can be properly selected prior to the implementation of the multichip structure.

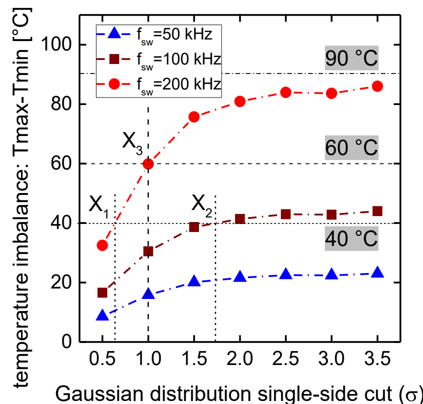


Fig. 5.21 Junction temperature increase imbalance as a function of the distribution cut for different switching frequencies.

5.2.5 Summary

In order to improve the design of PMs based on parallel SiC MOSFETs, the impact of parameters spread on the ET imbalances has been analyzed in this Chapter. Specifically, several relevant parameters, both related to the device or associated to the assembly, have been identified. For each parameter, the effect of its variability has been studied by simulating a DPT where two MOSFETs are connected in parallel and by analyzing the spread in terms of static power dissipation, switching energy, and transient current sharing (both at turn-on and at turn-off). Given the considered test conditions, the main outcomes can be summarized as follows:

- ΔV_{TH} noticeably affects both the static and the transient current sharing. The overstressed switch is the one with the lowest threshold voltage.
- ΔK also affects both the static and the transient imbalance indicators. However, its effect on the static power dissipation is more pronounced than that of ΔV_{TH}, while, for the dynamic power dissipation, ΔV_{TH} has a greater impact. The overstressed device is the one with the highest value of K.
- The MOSFET parasitic capacitances only affect the transient current sharing and have no impact on the static behavior. ΔC_{DS} has a marginal effect compared to that of ΔC_{GD} and ΔC_{GS}. The device experiencing the biggest current overshoot at turn-on (turn-off) is the one with the lowest (highest) C_{GS}. The same applies to C_{GD}.
- ΔR_{GP} only affects the dynamic behavior and the device with the highest R_{GP} will conduct more current at turn-off, but less during turn-on.
- ΔL_{SP} has an impact only on the dynamic imbalances and its effect was less significant than that of ΔR_{GP} in the considered test conditions.
- In general, increasing R_G tends to magnify the transient current sharing by slowing down the commutation.

Afterwards, the impact of the fluctuation of the various parameters has been evaluated by statistical means on a PM made of four parallel MOSFETs. A procedure to derive a trade-off curve between the parameters spread and the temperature imbalance has also

been developed. Such a methodology is based on batches of Monte Carlo simulations iterated by truncating the parameters distribution on an interval of increasing width. The resulting curves can be used to select the appropriate parameters variation limits or to define an upper bound to the switching frequency.

Chapter 6

Modeling and Design of Power Modules and Circuits

In Chapter 5, a methodology to derive a simple frequency derating rule or a selection criterion of the devices for building parallel arrays of SiC MOSFETs has been presented. However, some simplifications were made so that the analysis could be easily replicable and of broad use. The main simplifications are: (i) electrothermal steady state condition is not reached during the simulations of the DPT, (ii) no mutual heat exchange is considered because each MOSFET was connected to a separate TN. This Chapter consists of several case studies that overcome the aforementioned assumptions and show how more complex simulation approaches allow to build virtual prototypes of SiC-based power modules that can entirely be run in a SPICE-like environment.

6.1 Case-Study #1 Three-Phase Inverter Consisting of 36 Active Devices

In this Section, the model introduced in Chapter 2 is used to run the electrothermal simulation of a circuit application employing a vast arrangement of parallel devices. Such an application is meant to to validate suitability of the model in assisting the design of complex switching machines. Specifically, the selected case-study is a three-phase inverter whose schematic representation is provided in Fig. 6.1. It consists of three half-bridges (HB) connected in parallel to a DC voltage source of 1800 V, while the midpoints of the HBs are wired to a three-phase load in star configuration. The values of load inductance and resistance are 10 mH and 5 Ω, respectively. The whole inverter contains 36 active devices since the elementary switching cell of each leg is made of six parallel connected MOSFETs. In this application, the

modelled devices are the 3.3 kV MOSFETs described in Section 3.3 and each model instance was connected to an equivalent TN to enable the ET feedback. It must be specified that in this case-study, mutual heat exchange and nonlinear thermal effects are not considered, and they will be treated in Section 6.2. This choice is meant to isolate the performance of the model when simulating a complex converter from the additional simulation effort required to solve a complex TN. Albeit simple, a TN is however required to have a temperature evolution and to show that such a converter can be simulated until the ET transient terminates and steady state operation is reached.

The inverter was driven by an open-loop sine-triangle pulse-width modulation (PWM) controller depicted in Fig. 6.2. The carrier signal is a 100 kHz triangular waveform while the modulating one is a 100 Hz sine wave with a modulation index of 0.5. To avoid shoot-through conditions, a dead time of 900 ns was added between the switching edges of opposite transistors of the same leg. The gate voltage swings from -5 V to +20 V and two different resistors of 2.5 Ω and 6 Ω are connected to the gates of the high-side and low-side devices, respectively.

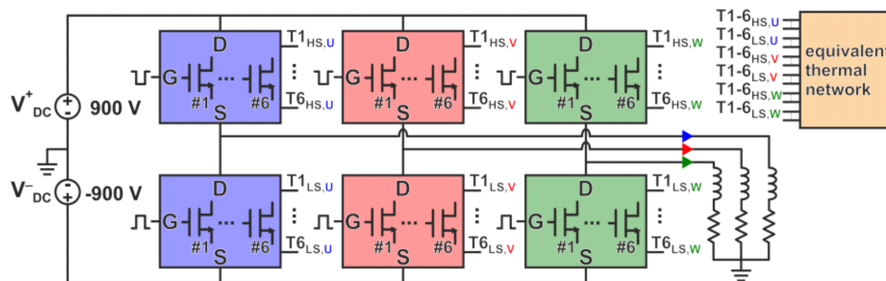


Fig. 6.1 Circuit schematic of the simulated three-phase inverter consisting of six parallel SiC MOSFETs per switching cell.

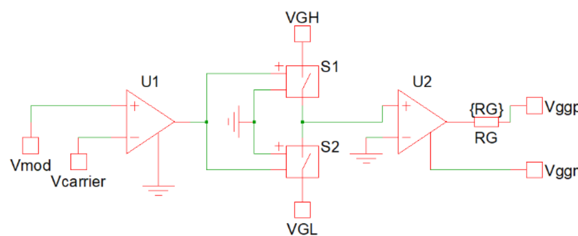


Fig. 6.2 Circuit schematic of the modelled PWM gate driver.

Despite the circuit complexity related to the high number of hard-switched power devices (36), an operation time of 40 ms (4×10^3 switching events) was simulated in less than 7 hours on a regular PC equipped with an Intel i7-2600 CPU. The waveforms of the output currents over the entire simulation interval are shown in Fig. 6.3a. Fig. 6.3b reports the individual temperatures of MOSFETs belonging to different sets of parallel devices. After a rise time of approximately 15 ms, the temperatures of both the high-side and low-side MOSFETs reach an average value of 55 °C and oscillate around it with a swing of ±5 °C.

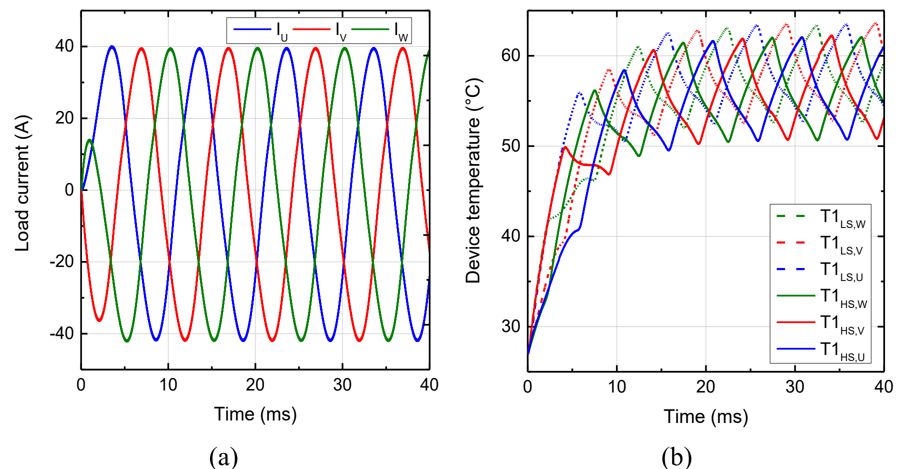


Fig. 6.3 Waveforms of (a) current in the load inductors and (b) individual temperatures of the MOSFETs from the six different subsets of parallel devices.

6.2 Modeling of a 3.3 kV Power Module

This Section describes the virtual prototyping of a PM based on 3.3 kV SiC MOSFETs and the simulation of a step-up converter and a single-phase inverter, both embedding the PM under investigation. Simulation times, convergence capability, and suitability to parametric analyses are discussed. The virtual prototyping methodology is based on an in-house approach relying on a fully circuital representation of the whole device/circuit for self-consistent static and dynamic ET simulations with SPICE-like programs. Considerable efficiency is

gained with respect to [Van94], [Wun97] and [Chv14] since the thermal problem is modeled with an equivalent thermal network derived through an advanced model-order reduction algorithm. Nonlinear thermal effects dictated by the high power densities were accounted for; moreover, improved accuracy was ensured by the inclusion of parasitics, which were experimentally estimated through an electromagnetic characterization of the assembly.

6.2.1 Power Module Under Investigation

The general-purpose approach presented in this Section is applied to a state-of-the-art PM characterized by two couples of SiC-based VDMOS transistors capable of withstanding up to 3.3 kV/50 A. Although the four devices can be used to realize a full H-bridge, here they are arranged in a half-bridge configuration with a doubled current rating. The assembly–compatible with standard PCB mounting processes [Cas14] is shown in Fig. 6.4, while its schematic cross-section is represented in Fig. 6.5. Each die is 7.2×7.2 mm^2-large and 0.4 mm-thick and contains one transistor; the two VDMOS couples lie on two separate 40×40 mm^2-large and 1.34 mm-thick direct-bonded copper (DBC) substrates, which consist in sandwich-like structures made of an aluminum nitride (AlN) sheet in between two copper (Cu) foils [Sco20]. While the bottom Cu foil is kept plain to ensure a good thermal contact with the 3 mm-thick baseplate underneath, the layout of the top one is composed by metal islands in order to realize the circuit topology. Electrical interconnections between Cu islands and devices are granted by aluminum (Al) wire bonds. An insulating gel is poured over the entire top surface in order (i) to increase the dielectric integrity and (ii) to avoid undesirable effects such as partial discharge and dielectric breakdown [Sco20b]. For the PM under analysis, a 5 mm-high silicon gel produced by Sylgard was considered [Sco20c]. Since the module PADs are covered by the insulating gel, Al vertical connectors are required to make them accessible.

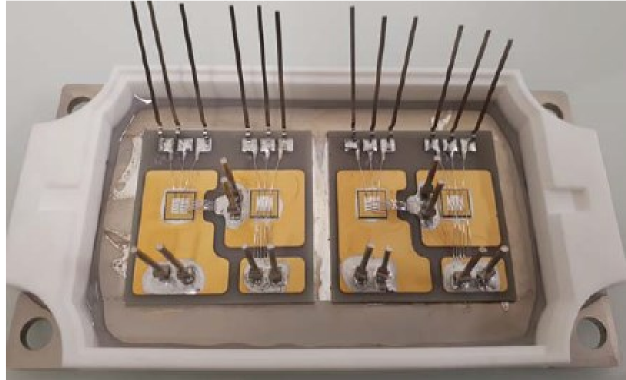


Fig. 6.4 Picture of the state-of-the-art PM under investigation: it embeds four 3.3 kV SiC VDMOS transistors placed on two separate DBC substrates, which in turn lie on a 120×60 mm^2 Cu baseplate.

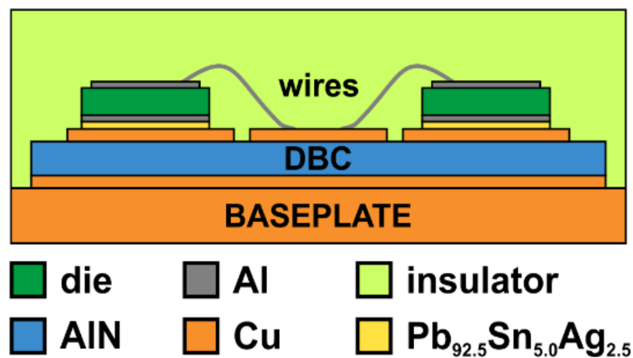


Fig. 6.5 Schematic cross-section (not to scale) of the PM under investigation. The materials are identified by different colors. Evidenced are: the Al wire bonds, the Cu baseplate, and the DBC substrate comprising Cu metallization and AlN layer.

6.2.2 Methodology

The simulation approach relies on the construction of a SPICE-compatible macrocircuit that models and fully couples the thermal and electrical behaviors of the PM under analysis. Such a macrocircuit also includes experimentally-extracted parasitics. The individual VDMOS transistors are described by the model of Chapter 2 and calibrated as per Section 3.3, the temperature-sensitive parameters of which are allowed to vary during the simulation run. The power-temperature feedback is accounted for with an equivalent thermal network extracted with low computational burden by means of a model-order reduction technique.

A preliminary study was devoted to the electromagnetic characterization of the PM parasitics. It consisted in the experimental evaluation of stray inductances, distributed resistances, and parasitic capacitances by varying frequency. To this aim, a Hioki IM3570 impedance analyzer [Link5] equipped with Hioki L2000 probes was exploited to measure the total loop parasitic inductance and resistance, as well as the common-mode capacitance. Results are shown in Table 14, which summarizes the values of the parasitics at the devices switching frequencies (f_{SW}) of interest for the case-studies investigated in Subsections 6.2.3 and 6.2.4.

TABLE 14 VALUES OF THE EXPERIMENTALLY-EXTRACTED PARASITICS AT THE FREQUENCIES OF INTEREST.

	f_{SW}=32 kHz	f_{SW}=64 kHz	f_{SW}=100 kHz
Total loop parasitic resistance	~5.4 mΩ	~5.2 mΩ	~4 mΩ
Total loop parasitic inductance	~130 nH	~30 nH	~120 nH
Common-mode capacitance	~121 pF	~118 pF	~118 pF

The power-temperature feedback is implemented by a thermal feedback block (TFB) comprising a linear equivalent network automatically extracted by FANTASTIC [Cod14], [Mag14]. Differently from approaches based on Foster-like thermal networks [Gór19], FANTASTIC relies on a model-order reduction technique and it does not require to perform thermal simulations in 3-D FEM software packages; it can be also adopted in multi-source thermal problems, typically making use of matrix-based approaches to account for the thermal coupling between devices [Sch15]. It must be remarked that nonlinear thermal effects play a relevant role in typical applications of SiC devices [Cod15]. While other techniques allow building thermal networks accounting for the temperature dependence of the thermal conductivity [Gór20], in this investigation a nonlinear correction applied through the Kirchhoff's transformation [Pou92] was required. By exploiting the thermal equivalent of the Ohm's law, the TFB can be employed in circuit simulators to enable the ET feedback. More

specifically, the power nodes of the transistor subcircuits represent the TFB input currents, while the thermal ones are connected to its output voltages. The resulting macrocircuit (which completely describes the coupled electrical-thermal problem) can be solved by any SPICE-like program (like PSPICE, LTSPICE, Eldo, ADS, SIMetrix) in relatively short times without occurrence of convergence issues; in this study, the SIMetrix framework was exploited.

The linear equivalent network extraction procedure is briefly explained in the following. First, a detailed 3-D geometry is created from PM structural data in the finite-element method (FEM) environment of COMSOL Multiphysics [COM18], as shown in Fig. 6.6; the building process is entirely automated by the in-house routine presented in [dAl19], which relies on the livelink between COMSOL and MATLAB. Then, the domain is discretized into a tetrahedral grid; a smart meshing approach was conceived in order to make the grid finer in the surroundings of the dies (Fig. 6.6). The mesh is in turn fed to FANTASTIC, which automatically builds a reduced-order model and extracts the corresponding equivalent network. Such a network associates the powers P_D dissipated by the heat sources of the four MOSFETs (inputs) to their temperature rises ΔT_{lin} averaged on the channel regions located on the top surface (outputs) under linear thermal conditions.

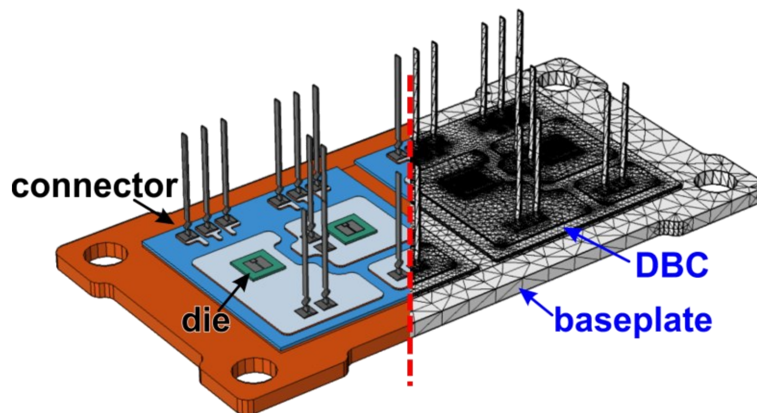


Fig. 6.6 3-D view of the PM geometry (left to the red dashed line) and tetrahedral mesh (right) automatically constructed in the COMSOL environment (the insulating gel is set as transparent for illustrative purposes). An exact replica of the real structure (Fig. 6.4) was obtained.

The thermal problem was set as follows. Four heat sources (one for each device) were considered to coincide with the active region of the transistors located on the top surface of the dies. Adiabatic boundary conditions were defined on all external surfaces except for the bottom baseplate one, on which a convective heat transfer coefficient $h = 3 \times 106$ W/m^{2}K was chosen to emulate the presence of a thermochuck (cold plate) [Cat20]; it must be remarked that any h value can in principle be adopted to model the effect of different cooling solutions.

Nonlinear thermal effects are accounted for by means of the Kirchhoff's transformation [Gór19]

$$\Delta T = T_0 \cdot \left[m_k + (1 - m_k) \cdot \frac{\Delta T_{lin} + T_0}{T_0} \right]^{\frac{1}{1-m_k}} - T_0 \qquad (6.1)$$

where ΔT represents the nonlinear-corrected temperature increment and m_k is a fitting parameter. The calibration of m_k was made through the following procedure. First, the self-heating thermal resistance (R_{TH}) of an individual VDMOS transistor under linear conditions was evaluated in COMSOL as $\Delta T_{lin}/P_D$. The temperature dependence of the thermal conductivities was then activated, and many COMSOL simulations were carried out with P_D logarithmically spanning the wide 1.8-1800 W range; hence, the nonlinear temperature rise averaged on the channel region was obtained as a function of P_D. As a final step, parameter m_k was calibrated through a least-squares algorithm to achieve the best agreement between the temperature rises ΔT obtained through (6.1) from $\Delta T_{lin}=R_{TH}\times P_D$ and those simulated by COMSOL under nonlinear conditions. Fig. 6.7 shows the results of the calibration.

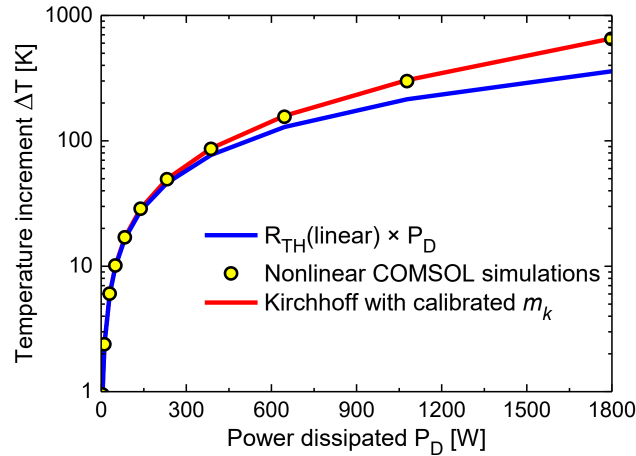


Fig. 6.7 Temperature increments vs. power P_D dissipated by the heat source. Comparison between nonlinear FEM simulations (yellow dots) and values obtained with the calibrated Kirchhoff's transformation (red curve). The graph also reports ΔT_{lin} given by the product of the linear thermal resistance value (R_{TH}) and P_D (blue curve).

6.2.3 Case-Study #2: DC-DC Step-up Converter

As a second case-study, the proposed simulation approach was applied to a 30 kW synchronous step-up DC-DC converter including the PM under analysis. Fig. 6.8 illustrates the schematic with emphasis on device subcircuits and parasitics. The connections are designed to realize the circuit configuration with two parallel devices at the high side (HS) and two parallel devices at the low side (LS); the gate signals V_G and $V_{G'}$ were generated to control the LS and HS devices, respectively. A switching frequency f_{SW}=100 kHz was considered. A sketch of the TFB is depicted in Fig. 6.9.

Table 15 summarizes the circuit parameters adopted in the ET simulations, chosen so as to respect the specifications on the output power. The parasitics were accounted for through the lumped elements R_σ, L_σ, and C_M, the values of which at f_{SW}=100 kHz were obtained by elaborating the experimentally-extracted total loop parasitic inductance and resistance, and common-mode capacitance shown in Table 14.

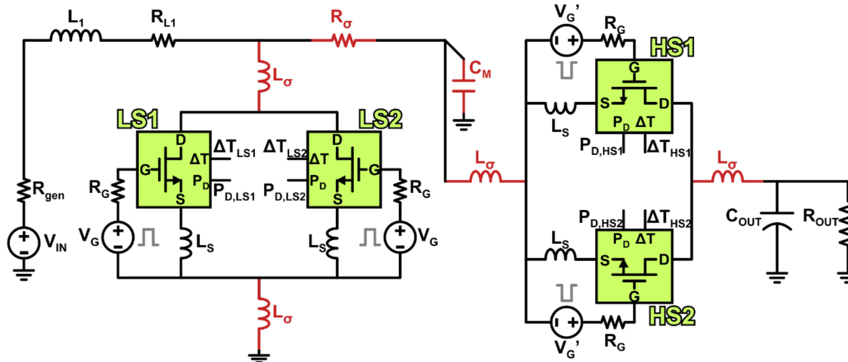


Fig. 6.8 Schematic of the half-bridge circuit driven in a synchronous step-up configuration. The light green boxes are the transistor subcircuits, while the parasitics are modeled with the passive components drawn in red.

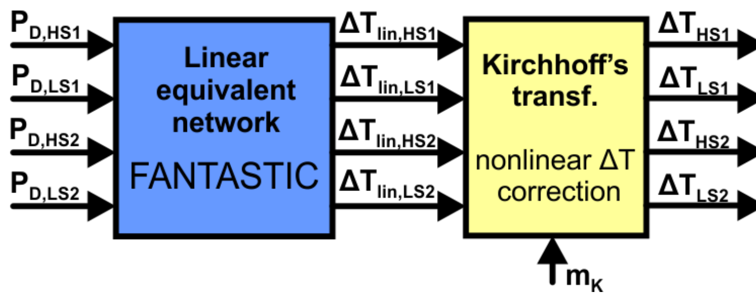


Fig. 6.9 Sketch of the TFB comprising (i) the linear equivalent network automatically built by FANTASTIC (light blue box) and (ii) the nonlinear correction performed by the preliminarily-tuned Kirchhoff's transformation (light yellow).

The efficiency of the step-up converter was computed to be η=94.35% by elaborating the ET simulation results. Fig. 6.10 shows the P_D values of the four devices at the limit cycle (i.e., during electrothermal steady state condition), while their operating temperatures averaged on the channel regions are reported in Fig. 6.11. The circuit configuration makes the LS devices dissipate much more power with respect to the HS ones, which results in a significant temperature difference between them (Fig. 6.11). The small temperature ripple (~1%) is due to the slow thermal dynamic behavior induced by the large thermal capacitance associated to the thick Cu baseplate.

TABLE 15 VALUES OF THE DC-DC CONVERTER CIRCUIT PARAMETERS SIMULATED IN SIMETRIX.

parameter	value
V_{IN}	800 V
R_{gen}	0.1 Ω
L_1	5 mH
R_{L1}	0.1 Ω
P_{OUT}	29 kW
R_G	4 Ω
C_{OUT}	10 μF
R_{OUT}	120 Ω
L_σ	30 nH
R_σ	4 mΩ
L_{WB}	1 nH
C_M	118 pF
f_{SW}	100 kHz
T_{ON}	5.5 μs

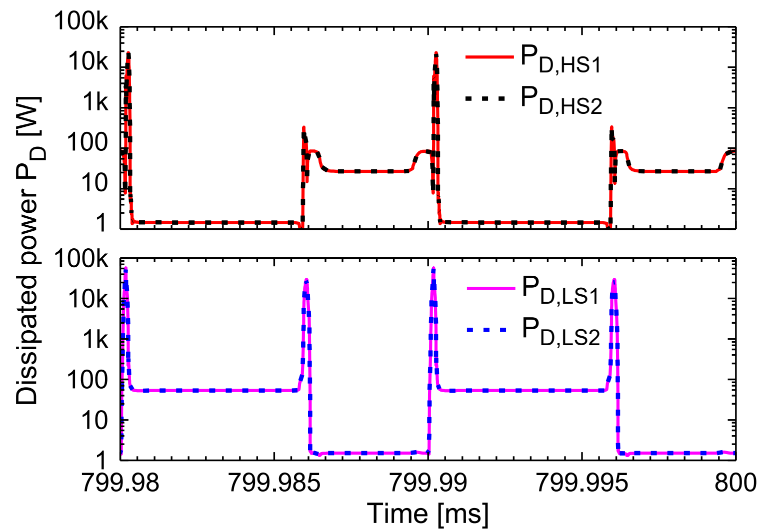


Fig. 6.10 SIMetrix simulation of the macrocircuit representing the DC-DC converter: power dissipated by the four VDMOS transistors vs. time in a two-period-long window at the limit cycle; the top (bottom) curves show the values referred to HS (LS) devices.

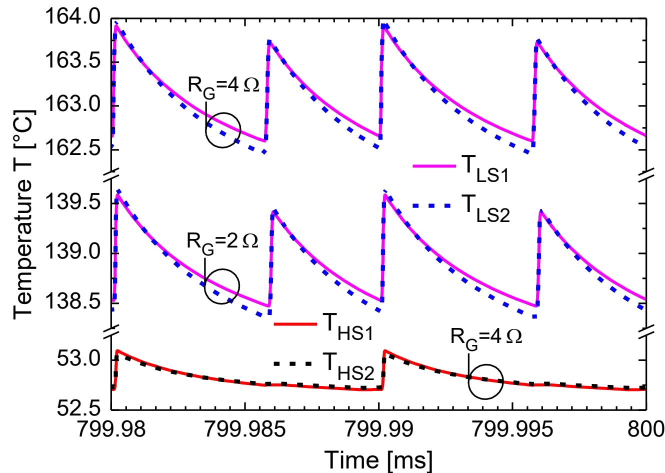


Fig. 6.11 SIMetrix simulation of the macrocircuit representing the DC-DC converter: temperature of the four VDMOS transistors (averaged on the active area) vs. time in a two-period-long window at the limit cycle. Also reported is the temperature evolution of the LS devices obtained by reducing the gate resistance R_G from 4 Ω (default value) down to 2 Ω.

After the dynamic ET simulation run, FANTASTIC, aided by a code to account for the Kirchhoff's transformation, enables the reconstruction of the whole spatial temperature field in the PM at chosen time instants with negligible computational cost (e.g., [dAl20]). This is a key option offered to designers, as the inspection of selected thermal maps represents a valuable support to estimate the PM reliability. Fig. 6.12 depicts the PM temperature field extracted at t=800 ms; an interesting finding is that the maximum temperature of the LS devices (~190°C) is ~30°C higher than the average one (Fig. 6.11).

As proof of the suitability of the proposed approach in parametric analyses, additional exemplificative simulations were performed to quantify the converter performances by modifying circuit parameters. To this aim, the gate resistance R_G and the switching frequency f_{SW} were varied in the ranges 2–6 Ω and 90–105 kHz, respectively. As a figure of merit of the circuit, η was evaluated and reported in Table 16, while Fig. 6.11 also shows the lower temperatures of the LS transistors obtained by reducing the gate resistance R_G from 4 Ω down to 2 Ω.

The main findings can be summarized as follows:

- higher R_G values increase η; however, designers should also consider the detrimental effects on di/dt.
- by reducing f_{SW}, the losses due to the reactive components and PM parasitics are mitigated, thus leading to higher η values.

The six simulations performed for this analysis allowed offering further evidence of the excellent convergence properties and the low CPU time requirements (~2 h for a time window of 800 ms).

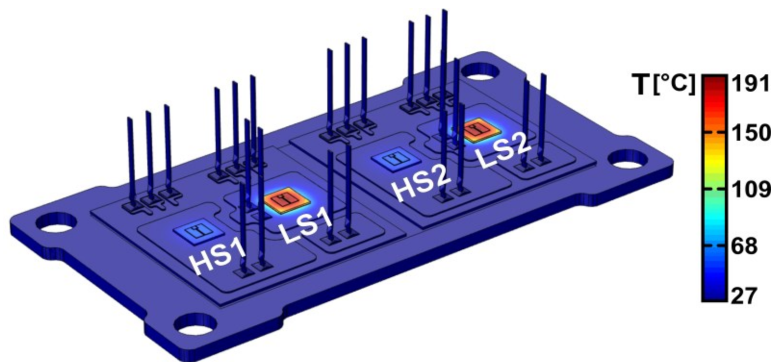


Fig. 6.11 Nonlinear-corrected spatial temperature distribution in the PM extracted by FANTASTIC in a post-processing stage, corresponding to the time instant t=800.0 ms of the DC-DC converter simulation. The insulating gel is set as transparent for illustrative purposes. The location of LS and HS devices is also highlighted.

TABLE 16 OUTCOME OF THE PARAMETRIC ANALYSIS CONDUCTED ON THE DC-DC CONVERTER: THE EFFICIENCY EVALUATED AT DIFFERENT R_G AND F_{SW} VALUES.

R_G	2 Ω	4 Ω	6 Ω
η	95.17%	94.35%	93.55%
f_{SW}	105 kHz	100 kHz	90 kHz
η	93.49%	94.35%	95.59%

6.2.4 Case-Study #3: Single-Phase Inverter

ET simulations of a single-phase inverter were also performed; the approach was applied to the macrocircuit schematically depicted in Fig. 6.12. The 50 Hz-400 V RMS inverter was designed to achieve a high efficiency value (~92%) providing a P_{LOAD}=4.5 kW RMS to R_{LOAD}; such electrical rates respect European AC standards and are

compatible with wind- and solar-energy conversion [Koj04], [Dog19]. The circuit required the use of an inverter control unit (ICU). As the load current is detected by means of a current sensing, the ICU generates ad-hoc voltage signals (V_{G_LS} and V_{G_HS}) to be fed to the gate drivers of the transistors. The control is based on a duty-cycle modulation technique. While the SIMetrix macrocircuit includes the same lumped parasitic components used for the DC-DC converter simulations, their values were varied according to f_{SW} (i.e., 64 kHz for the case-study). Concerning the power-temperature feedback, the same approach shown in Subsection 6.2.3 was adopted (Fig. 6.9). The parameters used in the inverter simulations are summarized in Table 17.

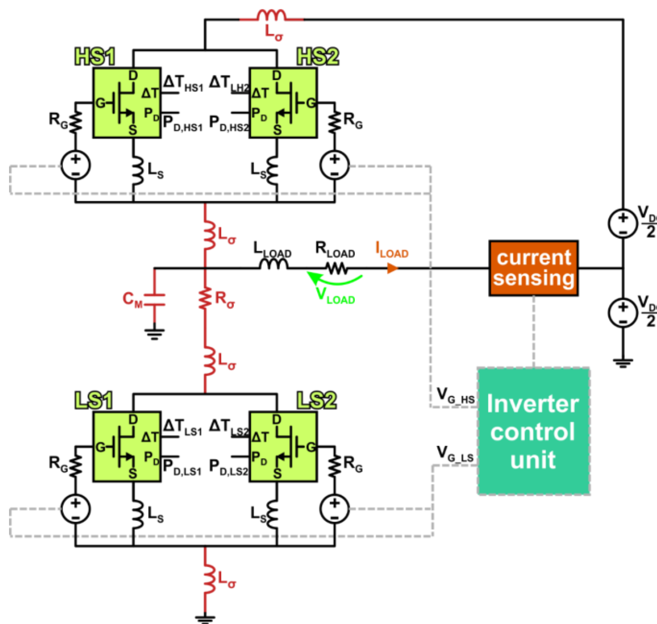


Fig. 6.12 Schematic of the half-bridge circuit driven in a single-phase inverter configuration. Evidenced are: the experimentally-extracted parasitics (red), the output current and voltage (orange and green arrow, respectively), the current sensing component (orange), the ICU (turquoise), and the logic signals (grey dashed lines) fed to the gate drivers of the four transistors.

An ET simulation of 1 s required ~1 h on a standard PC. The efficiency of the inverter was evaluated to be η=91.39%.

TABLE 17 VALUES OF THE INVERTER PARAMETERS ADOPTED IN SIMETRIX.

parameter	**value**
V_{DC}	1800 V
L_{LOAD}	5.8 mH
R_{LOAD}	40 Ω
$P_{OUT,RMS}$	4.5 kW
R_G	2 Ω
L_σ	7.5 nH
R_σ	5.2 mΩ
L_{WB}	1 nH
C_M	118 pF
f_{SW}	64 kHz

The current and voltage waveforms on the resistive load are shown in Fig. 6.13 over a 20 ms-wide time window at the limit cycle. The duty-cycle modulation technique leads the HS (LS) devices to dissipate more power in the first (second) half of the period. This is also confirmed by Figs 6.14 and 6.15, which depict the average temperature of the HS and LS devices, respectively. It must be underlined that (i) the high efficiency, (ii) the good boundary conditions applied to the bottom of the Cu baseplate, and (iii) the high R_{LOAD} value contribute to achieve low temperature increments (~30°C) with respect to T_0. As a main difference with the DC-DC converter, in which the LS devices turned out to be hotter than the HS ones, here the device temperatures are more evenly distributed. Again, the post-processing feature of FANTASTIC was exploited to extract the nonlinear-corrected temperature maps on the PM at the time instants t=987.0 ms (Fig. 6.16a) and t=996.5 ms (Fig. 6.16b).

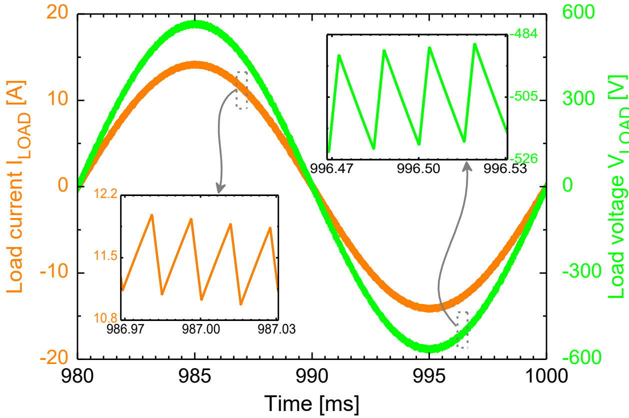


Fig. 6.13 Simulated I_{LOAD} (orange curve) and V_{LOAD} (green) vs. time in the last 20 ms window. Magnifications highlighting the ripple of I_{LOAD} and V_{LOAD} in four-period-long windows are also reported on the bottom-left and top-right corners, respectively.

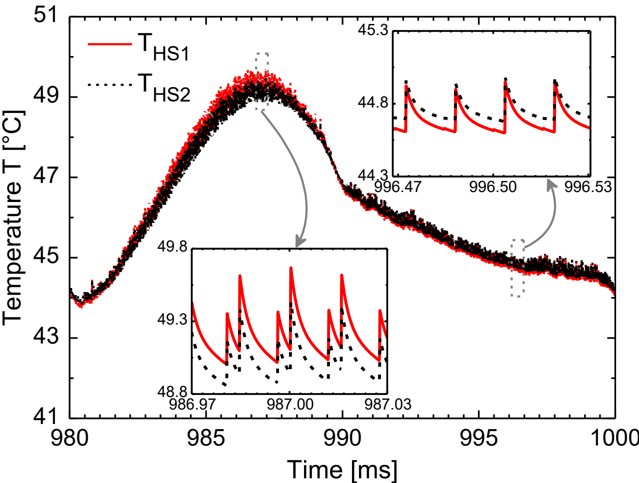


Fig. 6.14. Simulated temperature of the HS devices vs. time in the last 20 ms window. Magnifications highlighting the temperature ripple in four-period-long windows are also reported on the bottom-left and top-right corners.

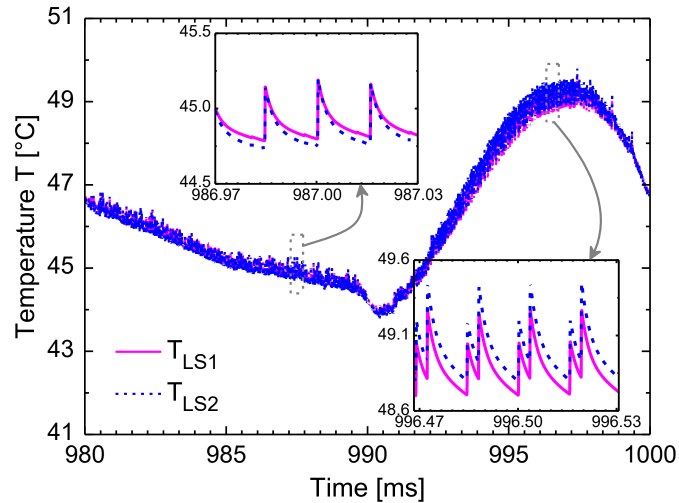


Fig. 6.15. Simulated temperature of the LS devices vs. time in the last 20 ms window. Magnifications highlighting the temperature ripple in four-period-long windows are also reported on the top-left and bottom-right corners.

As a last analysis, a parametric investigation (similar to the one carried out on the DC-DC converter) was conducted on the single-phase inverter. Table 18 shows the inverter efficiency η as a function of f_{SW} and R_G. The influence of such parameters was evaluated in a fast, yet trustworthy, simulation session that lasted ~4 h and proved the suitability of the approach even in parametric analyses of AC circuits.

TABLE 18 OUTCOME OF THE PARAMETRIC ANALYSIS CONDUCTED ON THE INVERTER: EFFICIENCY EVALUATED AT DIFFERENT R_G AND F_{SW} VALUES.

η	R_G=2 Ω	R_G=4.7 Ω
f_{SW}=32 kHz	95.32%	92.88%
f_{SW}=64 kHz	91.39%	87.32%

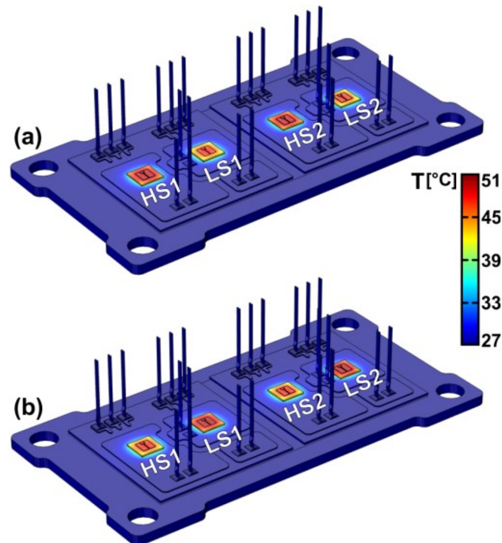


Fig. 6.16. Nonlinear corrected spatial temperature distributions extracted by FANTASTIC in a post-processing stage. The maps correspond to the time instants (a) t=987.0 ms and (b) 996.5 ms of the inverter simulation. The insulating gel is set as transparent for illustrative purposes. The location of LS and HS devices is also highlighted.

6.3 Case-Study #4: DC-DC Converter with Unbalanced MOSFETs

As last case-study, a circuit application relying on unbalanced parallel SiC MOSFETs is described in this section. In particular, this is meant to quantify the steady-state temperature gradient that can establish among mismatched devices operating in parallel under realistic circuit conditions. The circuit application is an 800 V-to-350 V DC/DC synchronous buck converter with an output current of ~23 A operated at 200 kHz (Fig. 6.17). This converter is based on a SiC PM where a high-side (HS) and a low-side (LS) MOSFET array are arranged in a half bridge configuration. Specifically, each of the HS and LS switching cells contain four parallel 1.2 kV-36 A-rated SiC devices described in Section 3.2 and placed on two opposite copper islands as shown in Fig 6.18. The ET feedback was enabled by connecting a TFB to the thermal nodes of the instances of the MOSFET model (Fig. 6.17). As described in Subsection 6.2.2, the TFB was extracted from the

meshed PM structure (Fig 6.18) through a model-order reduction technique [Cod14].

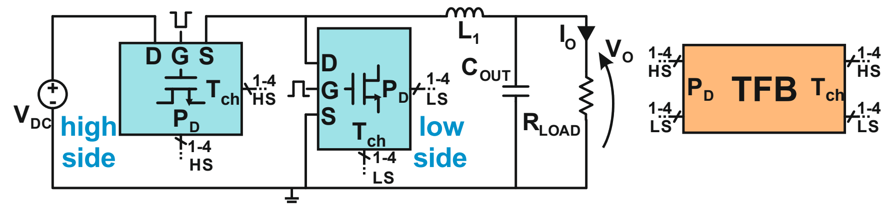


Fig. 6.17 Circuit schematic of the buck converter under test. The arrays of parallel MOSFETs and TFB are highlighted in light blue and orange, respectively.

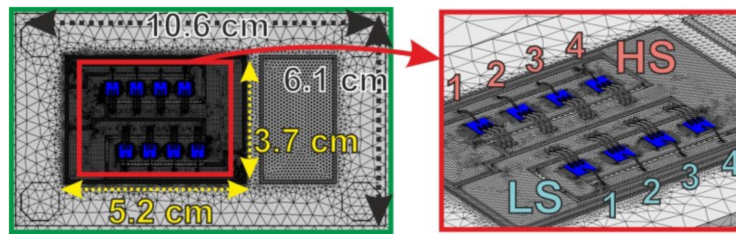
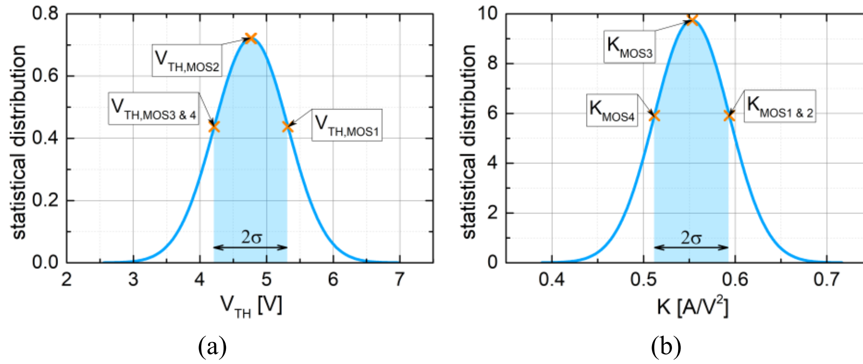


Fig. 6.18 Top (left) and angled (right) views of the PM structure with HS and LS MOSFETs highlighted.

Such a network couples the power dissipated by the devices to their temperature and allows accurately solving the 3-D heat-diffusion problem with much lower computation time than traditional numerical (e.g., finite-element) methods and includes both self- and mutual-heating effects. Moreover a 3-D temperature map can be reconstructed at each simulation time step.

Within this simulation framework, the investigation focused on the impact of V_{TH} and K mismatches on the parallel connected MOSFETs. Two sets of V_{TH} and K values, defining two different circuit test cases, were extracted from the pdfs obtained after the statistical characterization of Section 5.2, In the first test condition (referred to as balanced), two unique V_{TH} and K values, equal to the means of the distributions, are shared by all the MOSFETs of the arrays. For the second test condition (unbalanced), all the parameters were chosen to fall within a 2σ-wide interval. Fig. 6.19 reports the distribution of the parameters and highlights the individual values selected for K and V_{TH}. The values of K and V_{TH} are also summarized in Table 19 for ease of consultation.



(a) (b)

Fig. 6.19 Unbalanced case: statistical distributions of (a) V_{TH} and (b) K; the selected values are marked.

TABLE 19 VALUES OF V_{TH} AND K SET FOR THE ET SIMULATION OF THE DC/DC CONVERTER.

	M1	**M2**	**M3**	**M4**
V_{TH} [V]	5.33	4.77	4.21	4.21
K [A/V^2]	0.59	0.59	0.55	0.51

Although a mismatch in terms of MOSFET capacitances was found to be less influent than that of K and V_{TH} (Chapter 5), an imbalance of C_{GS}, C_{GD} and C_{DS} was also introduced. In particular, the selected values are reported in Table 20 and were obtained by sampling the distributions of the MOSFET capacitances obtained in Section 5.2.

TABLE 20 VALUES OF C_{DS}, C_{GD} AND C_{GS} SET FOR THE ET SIMULATION OF THE DC/DC CONVERTER.

	High Side				Low side			
	M1	**M2**	**M3**	**M4**	**M1**	**M2**	**M3**	**M4**
C_{DS0} [nF]	3.19	2.29	1.55	3.01	2.22	1.6	2.24	2.54
C_{GD0} [nF]	0.632	0.649	0.557	0.634	0.588	0.75	0.741	0.742
C_{GS} [nF]	2.35	2.08	2.35	2.03	2.28	2.46	2.36	1.99

Afterward, the converter was simulated over 0.4 s of operation time (80×10^3 switching events) with both balanced and unbalanced PM configurations. In order to reach a complete steady-state condition, the

simulation interval was chosen sufficiently longer than the thermal and electrical time constants. Even though the simulation time step had an upper bound of only 10 ns, a total computation time of approximately 11 hours was required to simulate both cases simultaneously on a desktop PC equipped with a quad-core Intel i7-2600 CPU.

Fig. 6.20a and 6.20c show that the introduced parameter mismatch does not affect the circuit functionality since a difference of only 0.3% between the average output voltages ($V_{O,AVG}$) of the two test conditions was obtained. On the other hand, the thermal stress withstood by each device was found to be strongly dependent on the selected PM configuration. This is witnessed by Fig. 6.20b, which shows that in the balanced case the temperature mismatches within each array are only determined by the MOSFETs positions: the central devices M2 and M3 heat up more than the outer ones (M1 and M4) due to greater impact of mutual thermal effects.

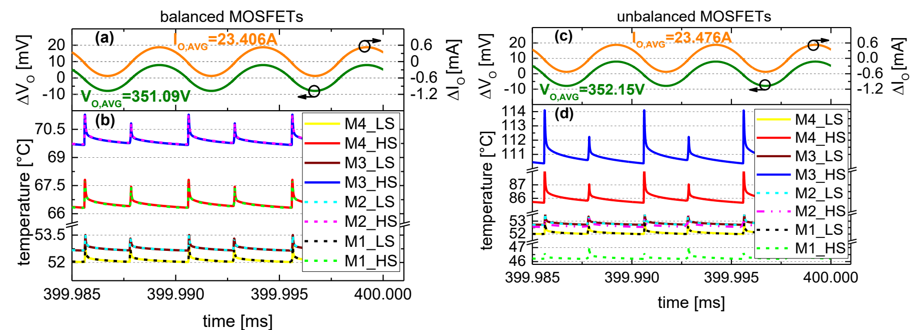


Fig. 6.20 Output voltage and current - (a) and (c) -, HS and LS temperature waveforms for the balanced (b) and unbalanced (d) test cases.

Fig. 6.21a illustrates the relatively uniform temperature distribution corresponding to the end of the considered time span. Conversely, for the unbalanced case, a temperature difference amounting to 67°C was observed between the HS transistors M3 and M1 - Fig. 6.20d.

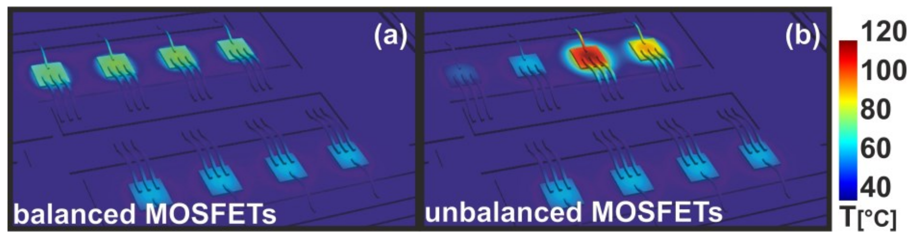


Fig. 6.21 Temperature maps at 0.4s.

The highest thermal stress withstood by M3 is dictated by its lower V_{TH} (which increases its current capability) and, therefore, by turn-off and turn-on transitions occurring ahead of and behind those of the other parallel MOSFETs, respectively. This makes M3 carry most of the transient current, in turn leading to higher switching losses. Interestingly, M4 is found to be less subject to thermal effects, although this device shares the same V_{TH} value as M3; this can be attributed (i) to its smaller K (i.e., bigger R_{ON}), which determines a lower static current flow and thus a lower static dissipated power, and (ii) to a reduced thermal coupling with the other MOSFETs favored by its outer position - Fig. 6.21b.

In both cases, LS devices undergo less severe thermal conditions since their power dissipation during switching transients is lower than that of their HS counterparts, which can be explained as follows: in this circuit topology, when the LS transistors commutate, their drain-to-source voltage drop corresponds to the forward voltage of the internal body diodes as these start conducting during dead times. However, since in this application the conduction losses only account for a small portion of the total losses, the temperature differences among the LS MOSFETs are primarily imposed by their positions. Consequently, when moving from the balanced to the unbalanced configuration, the LS temperature distribution remains relatively unchanged. However, it should be noticed that imbalances in terms of the body diodes were not considered in this study and that their dissipation can also be significant [Yan11].

6.4 Summary

The effects of mismatched devices on parallel connected MOSFETs have been examined in this Chapter through advanced ET simulation methodologies. The main achievements can be illustrated as follows.

In the first Section, the compatibility of the model with the simulation of complex switching converters has been proved through the simulation of a three-phase inverter containing 36 hard switched MOSFETs. Despite the circuit complexity, the simulation of 40 ms of operation time has been completed in less than 7 hours.

Successively, an efficient and versatile strategy for fast and accurate dynamic electrothermal simulations has been applied to a state-of-the-art multichip power module including four 3.3 kV SiC VDMOS transistors arranged in a half-bridge configuration. The strategy has been exploited to simulate a synchronous step-up DC-DC converter and a single-phase inverter embedding the aforementioned power module. In both cases, circuit parasitics have been included, the values of which were calibrated on the basis of the total loop parasitic resistance/inductance and common-mode parasitic capacitance experimentally extracted in a preliminary stage. 1 h and 2 h were required to perform the 800 ms-long DC-DC converter and 1 s-long AC inverter ET simulations, respectively. This allowed for effortlessly conducting an illustrative study on the impact of key parameters on the circuits performance (i.e., in terms of efficiency).

Eventually, the methodology introduced in Section 6.2 has been used to simulate thermally-induced unbalances arising in a power module made of mismatched SiC MOSFETs. The procedure has been successfully applied to the analysis of a synchronous step-down converter containing eight MOSFETs under balanced and unbalanced test conditions in terms of V_{TH} and K. The significance of the proposed approach lies in the impossibility of identifying critical temperature discrepancies by a simple inspection of the converter output quantities. As a remarkable outcome, strongly dissimilar temperature distributions between the two scenarios have been obtained. While in the balanced case the maximum temperature gap among the individual MOSFETs was confined below 20°C, in the unbalanced one this gap was found to raise to 67°C, with the hottest device reaching 114°C. For a given

application, the simulated temperatures obtained with this methodology can be fed to lifetime estimation equations to check whether or not a required target is reached.

Conclusions

In this thesis, the criticalities involved in the parallel connection of SiC MOSFETs have been analyzed. The first tool allowing this study is an in-house developed compact model for SiC MOSFETs capable of running fully-coupled electrothermal simulation if connected to an appropriate equivalent thermal network. The model is based on a simple mathematical formulation associated with a straightforward parameter extraction procedure; it can be implemented by a SPICE-compatible subcircuit including a standard MOSFET, additional resistors, controlled capacitors, and controlled nonlinear sources to account for specific physical mechanisms and temperature dependences. The influence of SiO_2/SiC interface traps on threshold voltage and channel mobility, the dependence on the bias of the drain resistance, the impact ionization, and the capacitance nonlinearity are accounted for.

The model accuracy has been verified over a selection of SiC MOSFETs covering the main voltage classes currently available on the market.

For 1.2 kV–36 A power MOSFETs, the model proved to be suited to represent broad ranges of voltage, current, and temperature, including out-of-SOA conditions. Excellent agreement has been obtained with the experimental transfer and output I–V characteristics, despite the smooth triode-saturation transition occurring in SiC transistors. Both the turn-on and turn-off current and voltage evolutions have been well predicted, including the drain voltage overshoot in the latter. Moreover, the calibrated model has been found to ensure good alignment with the measured waveforms under harsh out-of-SOA conditions dictated by SC and UIS tests, where the temperature can reach several hundreds of Kelvin degrees. In addition, the model was able to replicate the power dissipation imbalance that was experimentally obtained for mismatched devices during inductive load switching. Successively, the model has been calibrated to match the characteristics of 3.3 kV and 1.7 kV devices, and, in both cases all the subtleties of the static and dynamic electrical waveforms have been represented. The described validation, associated to ease of scalability,

supported the adoption of the model as a tool for thermal-aware design of SiC-MOSFETs-based power modules and circuits.

Afterwards, a peculiar failure type of SiC MOSFET subjected to short circuit stress has been experimentally investigated. A commercial 1.2 kV – 80 mΩ SiC planar MOSFET that consistently showed this kind of failure has been identified. This failure mode results in a MOSFET with a partial short circuit between gate and source but that still retains the capability of blocking the current between drain and source. Therefore, it is of interest for the parallel connection of multiple devices because the failure of a single transistor does not result in the failure of the others connected in parallel. The failure has been found to be caused by the creation of cracks in the top SiO_2 as a consequence of high thermo-mechanical stress and melting of the top metallization. Moreover, the failure interested only some cells of the whole device and a partial restore of the functionality of the gate structure has been found possible after injecting a small current through the gate terminal. However, it has been found that the voltage and injected recovery energy should be high enough to eliminate the main ohmic paths, but not so high as to cause excessive metal diffusion within the cracked oxide. Further studies are necessary to make the recovery a feature exploitable during on-line operation in real applications. Interestingly, a drain leakage current that does not flow through the source of the device has also been observed. The occurrence of such a current only for values of gate bias above the threshold voltage suggests that the damaged area of the device also involves the gate oxide above the channel region, which is generally regarded as the weakest oxide layer but had never been observed to be responsible for failure during short circuit.

In Chapter 5, the impact of relevant device and circuit parameters variability on parallel connected SiC MOSFETs has been evaluated by statistical means. This analysis laid the foundations for the development of a guideline for the identification of allowable parameters spread ensuring the safe operation of the parallel array. As a preliminary step, a subset of relevant device and circuit parameters has been identified. With reference to the device, these are the threshold voltage, the current factor, and the MOSFET capacitances; while, with reference to the circuit, the gate resistance and the source stray inductance have been selected. Successively, the fluctuations of both

threshold voltage and current factor have been quantified starting from the static characterization of a set of 20 1.2-kV, 36-A SiC power MOSFETs. The resulting experimental values have been found to be normally distributed. The remaining parameters have been assumed to be normally distributed with relative 3σ-spreads of 50% around their mean values. Based on the statistical description of K and V_{TH}, the general idea for a procedure to relate the parameters spread to the possible temperature imbalance has been illustrated. Such a procedure relies on the execution of multiple MC ET simulations and on the approximation of the thermal problem to a 1-D equivalent. An example of how its outcomes can be used as a first-order decision rule for the selection of appropriate performance variation limits of parallel SiC MOSFETs has been proposed.

Eventually, an efficient and versatile strategy for fast and accurate dynamic electrothermal simulations has been used for modelling virtual prototypes of multichip power modules. The resulting virtual prototypes have been simulated during their operation in complex switching converters and allowed to identify a critical temperature gradient resulting from mismatched characteristics of the devices. The significance of this finding lies in the fact that the temperature gradient could undermine the long-term reliability of the power module but does not significantly alter the output current and voltage waveforms. Therefore, it would be difficult to experimentally detect it without dedicated temperature monitoring of the individual chips.

Future Work

Compact modeling, virtual prototyping and ruggedness assessment are relevant research fields for the development of increasingly efficient and reliable SiC-based applications. Within these three fields, this dissertation dealt with the effect of parameters spread on the performance of SiC power modules. This section describes some possible future advancements.

The DC gate leakage current resulting from the soft failure type described in Chapter 4 might be exploited to build gate driver circuits for enhancing the reliability of power modules. When a device fails, the continuous absorption of a leakage current could lower the efficiency or threaten the reliability of the whole system. This might be prevented by a gate driver that monitors the DC gate current and disconnects the failed SiC MOSFET from the parallel assembly. In this way, the reliability and efficiency of the power module are restored, even if at a reduced power level.

The compact model presented in Chapter 2 has been validated across a broad range of cases. However, new and better SiC devices are constantly released on the market. In the last years, a clear interest for SiC trench MOSFETs has grown, with some promising samples already being commercially available. Validating the SiC MOSFET compact model for this category of devices surely represents a valid line of research. Moreover, another interesting step concerns the study of the fluctuation of the parameters determined by the technology shift from planar to trench. Furthermore, the study of parameters spread might be tackled by machine learning techniques rather than by classical statistical approach.

Eventually, an experimental verification of the temperature gradient developing during steady state operation due to unbalanced devices might possibly be pursued by infrared thermography.

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