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Analysis of heat propagation and electrothermal effects in electronic devices and circuits

by
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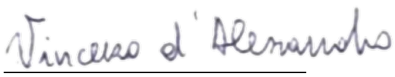

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Candidate's declaration

I hereby declare that this thesis submitted to obtain the academic degree of Philosophiæ Doctor (Ph.D.) in Information Technology and Electrical Engineering is my own unaided work, that I have not used other than the sources indicated, and that all direct and indirect sources are acknowledged as references.

Parts of this dissertation have been published in international journals and/or conference articles (see list of author's publications at the end of the thesis).

Napoli, March 9, 2023

Ciro Scognamillo

Abstract

Over the last 50 years, efforts of the academic research and industry in the field of electronics engineering have contributed to the development of devices and circuits based on semiconductors with unrivaled electrical features. However, the use of such technologies is still limited and hindered by thermally-induced issues. Self-heating phenomena - inevitably occurring even under standard working conditions - (i) negatively affect the electrical performance of devices, (ii) reduce their long-term reliability, and (iii) may lead to irreversible failures.

My research activity falls within this domain and addresses the study of heat propagation and electrothermal effects (i.e., the impact of power-temperature feedback on electrical characteristics). More specifically, I have been focusing on thermal/electrothermal modeling and simulation of devices and circuits; both tasks are of crucial importance in the design and testing stages, even more in the light of technological improvements that, paradoxically, may exacerbate the negative consequences of self-heating phenomena.

Among the topics I contributed to, it is worth mentioning how, through thermal analyses based on methodologies developed and updated during these three years, detailed studies were carried out on the behavior of single- and double-sided cooled power modules, SiC- and GaN-based devices, and power circuits included in printed circuit boards. The compact thermal networks extracted from such analyses were coupled with electrical models of transistors, thus generating highly-efficient electrothermal simulation tools.

In addition, an *in-situ* thermal impedance measurement technique is presented in this dissertation. The technique is unique in the field of power electronics, as it allows the identification of the dynamic thermal behavior of devices within the application environment in which they are deployed, without any need for laboratory measurements.

Keywords: electrothermal effects, electrothermal simulation, heat propagation, power electronics, thermal modeling.

Sintesi in lingua italiana

Negli ultimi anni gli sforzi della ricerca accademica e dell'industria nel settore dell'elettronica hanno contribuito allo sviluppo di dispositivi e circuiti basati su semiconduttore con caratteristiche elettriche eccezionali. L'impiego di tali tecnologie è tuttavia ancora oggi limitato e ostacolato da problematiche di natura termica. I fenomeni di surriscaldamento che inevitabilmente si verificano durante il funzionamento dei dispositivi tendono (i) a peggiorarne le prestazioni elettriche, (ii) a ridurne l'affidabilità a lungo termine e (iii) a provocarne la rottura nei casi più critici.

La mia attività di ricerca si colloca all'interno di questo contesto e affronta lo studio della propagazione del calore e degli effetti elettrotermici (i.e., l'impatto del feedback potenza-temperatura sulle caratteristiche elettriche) in dispositivi e circuiti elettronici. Alla luce delle migliorie tecnologiche che, paradossalmente, esacerbano le conseguenze negative dei fenomeni di surriscaldamento, la modellazione e simulazione elettrotermica accoppiata rivestono un'importanza cruciale sia nella fase di design che nella fase di testing.

Tra le tematiche a cui ho contribuito vale la pena sottolineare come, attraverso analisi termiche basate su metodologie sviluppate e aggiornate durante il triennio, siano stati effettuati studi dettagliati sul comportamento di moduli di potenza a singola e a doppia superficie di raffreddamento, dispositivi basati su tecnologia SiC e GaN, e circuiti di potenza implementati su PCB. Le reti termiche compatte estratte a valle di tali studi sono state accoppiate a modelli elettrici dei transistori, generando strumenti di simulazione elettrotermica altamente efficienti.

Infine, nella tesi viene presentata una tecnica di misurazione di impedenza termica *in-situ*. Si tratta di un *unicum* nel settore dell'elettronica di potenza, in quanto tale tecnica (i) permette l'identificazione del comportamento termico dinamico del dispositivo direttamente nell'ambiente applicativo in cui esso è impiegato e (ii) non richiede misurazioni dirette e/o indirette di temperatura.

Parole chiave: effetti elettrotermici, elettronica di potenza, modellazione termica, propagazione del calore, simulazione elettrotermica.

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This endeavor would have not been possible without the support of my family, for their unconditional help and understanding. I dedicate this thesis to my beloved Federica, who never ceases to amaze me with her willpower and resourcefulness - which undoubtedly I was inspired by.

List of Acronyms and Symbols

The following acronyms and symbols are used throughout the thesis.

$\boldsymbol{\alpha}$	Power law coefficient used to describe thermally-induced conductivity degradation
$\boldsymbol{\beta}$	Linear law coefficient used to describe thermally-induced conductivity degradation, [K^{-1}]
$\boldsymbol{\rho}$	Mass density, [Kg/m^3]
Al	Aluminum
AlN	Aluminum Nitride
BC	Boundary condition
$\boldsymbol{BV_{DS}}$	Breakdown drain-source voltage, [V]
$\boldsymbol{c_p}$	Heat capacity, [J/Kg·K]
CS	Cooling surface
Cu	Copper
CSF	Cumulative structure function

$\boldsymbol{C_\Sigma}$	Cumulative structure function
DBC	Direct bonded copper
DSC	Double-sided cooled
DSF	Differential structure function
DUT	Device under test
ET	Electrothermal
FEM	Finite-element method
$\boldsymbol{f_\tau}$	Thermal cut-off frequency, [Hz]
GaN	Gallium Nitride
GDS	Graphic data system
$\boldsymbol{h}$	Heat transfer coefficient
in-situ	Within the device application environment
IR	Infrared
$\boldsymbol{k}$	Thermal conductivity, [W/m·K]
MOR	Model order reduction
MPMM	Multi-point moment matching
PCB	Printed circuit board
PM	Power module
$\boldsymbol{R_\Sigma}$	Cumulative sum of thermal resistances
RF	Radiofrequency

$\boldsymbol{R_{TH}}$	Thermal resistance, [K/W]
$\boldsymbol{R_{TH,j-a}}$	Junction-to-ambient thermal resistance, [K/W]
SC	Short-circuit
SF	Structure function
SiC	Silicon Carbide
SSC	Single-sided cooled
$\boldsymbol{T_0}$	Reference temperature, [K]
$\boldsymbol{T_B}$	Ambient/backside/baseplate temperature, [K]
TFN	Thermal feedback network
$\boldsymbol{T_{ch}}$	Channel region temperature, [K]
$\boldsymbol{T_j}$	Base-emitter junction temperature, [K]
TEOL	Thermal equivalent of Ohm's law
TIM	Thermal interface material
TRP	Trend reversal point
TSEP	Temperature-sensitive electrical parameter
UIS	Unclamped inductive switching (test)
VDMOS	Vertical diffusion metal-oxide semiconductor
$\boldsymbol{z_{j-a}}$	Normalized junction-to-ambient power pulse thermal response
$\boldsymbol{Z_{TH}}$	Thermal impedance, [K/W]

$\boldsymbol{Z_{TH,j-a}}$	Junction-to-ambient thermal impedance, [K/W]
$\boldsymbol{Z_{TH,pulse}}$	Time-derivative of the thermal impedance, [K/sW=K/J]

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Chapter 1

Introduction

1.1 Motivations

Electronic circuits and systems have been amazingly evolving over the past 50 years [All02]: (i) they embed more, smaller, and faster transistors [Par05], [Ngu07], (ii) they are adopted in harsh environments [Joh04], under nontypical working and environmental conditions [Hag10], and at the edge of their safe operating area [Yan11], (iii) they are made of new materials – often worsening operative temperatures and hindering the heat propagation – to improve electrical performances [Yod96], [Kon98], [Rab12], and (iv) they deal with the rising energy demand providing more efficient, compact, and reliable power conversion mechanisms [Rod02], [Far10], [Kas13], [For17]. Despite the enormous variety of fields of application and the advancements in energy management and conversion, electronic devices have always been accompanied by the exact same issue: as they dissipate power, their rising temperature negatively affects their electrical performance (e.g., by shifting the bias point of a device used as an amplifier) and reliability, leading – in some cases – to irreversible failures. This is evidently a plague for the electronic engineering field [Bre99], [How01], [Spi02]. The main research topic of this dissertation is the investigation of the thermal and electrothermal (ET) dynamic behavior of electronic devices and circuits. Such an investigation is performed through thermal and ET analyses. While the former allows characterizing the heat propagation and temperature distribution, ET analyses serve the purposes of describ-

ing and modeling the coupled electrical and thermal behaviors of single devices and circuits. The study of ET effects has been historically relevant for power devices and whole systems (e.g., power modules, PMs, and printed circuit boards, PCBs), the safe operating area of which is typically limited by ET issues [Oet76], [Hag96], [Swa11], [Iwa17]. Thermal analyses can also be useful for the defect/fault detection in electronic devices. As the assembly heats up, each layer contributes to the overall temperature gradient by means of its own thermal properties. By investigating the temperature gradient, it is in principle possible to inspect such properties, as well as faults/defects that may have occurred in the system. Among all, a notable example is represented by infrared (IR) thermography [Ric17] and structure functions (SFs) [Szé88], [Ren02], [Ren05], where the thermal response of the system is elaborated to gather insights into the internal – and not accessible – assembly (e.g., to detect faults and defects). The influence of heating and cooling of a device on its electrical performance (e.g., I-V characteristics, switching transients) can be thus exploited to measure quantities in noninvasive manners. In this regard, the present dissertation will also delve into the development of a novel extraction technique for the thermal impedance (Z_{TH}) of power devices. Differently from traditional methods [Die61], [Chr96], [JED10], [Ave11], [Sch11], [Gon16], [Kim17], [Rac21], this technique (i) can be conveniently adopted without any need for temperature measurements or thermochuck/cold plates and (ii) enables the *in-situ* characterization of any power device, i.e., the measurements can be performed without removing devices from the application environment in which they are deployed.

1.2 Thermal *vs.* electrothermal analyses

Thermal analyses represent the foundation of ET analyses: they consist in the study of heat propagation in the structure of interest, given a value/profile of dissipated power (P_D) applied to the region where the heat is generated (heat source). As an outcome, the temperature distribution in the 2-D or 3-D case-study is obtained, either in the regions of interest or in the whole domain. From the temperature distribution, the following thermal metrics can be evaluated: the thermal resistance (R_{TH}), which gives information about the steady-state thermal behavior of the structure, and

the Z_{TH}, describing its dynamic thermal response. Among the different numerical tools available in the market, such analyses are typically conducted in finite-element method (FEM) software packages (e.g., COMSOL Multiphysics, ATLAS, Flotherm); here, the structure is first subdivided into a definite number of points (elements) and the thermal problem is numerically solved for each element. It is also worth mentioning that the heat transfer equation can be analytically solved, as long as the geometry of the structure is simple enough. Figure 1.1 schematically depicts the flowchart of a thermal analysis.

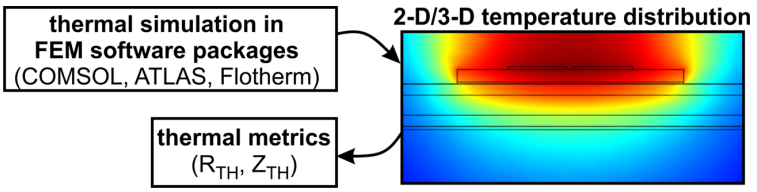

Figure 1.1. Schematic representation of a thermal analysis flow: thermal simulations are conducted in FEM environments; the temperature distribution over the domain under investigation is obtained; as an output, thermal metrics are finally calculated.

ET analyses make use of thermal-only studies and aim at describing the coupled electrical and thermal behavior of devices or circuits under standard or stress conditions. They revolve around the ET feedback: (i) a temperature distribution is obtained from thermal analyses conducted with a given value/profile of P_D; (ii) the temperature-sensitive electrical parameters (TSEP) of active devices are updated according to the new temperature values; (iii) a new P_D is calculated, which represents the input of point (i). The ET feedback is run until convergence, that is, the mismatch between the old and updated values of temperature and power drops below a tolerance value. Traditionally, approaches to ET simulations can be divided into:

- Physics-based (device-level), in which the simulator solves the full physical model for the electrical and thermal problems.
- Relaxation-based, in which the thermal and electrical problems are treated separately by two simulators – typically, a circuit simulation

program and a 3-D thermal-only numerical solver – and a supervisor is used to exchange data between them [DeF14a], [Chv14].

- FEM-enriched, that is, the finite-volume/-element software package is extended to account for the electrical behavior of the device with simplified models [Košl3], [Pfo13].

- Thermal Feedback Network (TFN)-based. In this case a standard circuit tool (e.g., PSPICE) is used to perform the coupled ET simulation, in which the thermal problem is modeled through an electrical circuit with the thermal equivalent of Ohm's law (TEOL).

Physics-based, relaxation-based, and FEM-enriched approaches all ensure trustworthy results; however, their computational burden makes them inconvenient and not prone to be included in thermal-aware design workflows. The ET simulations reported in this dissertation rely on the TFN-based approach, it being more efficient as it is defined as "fully-circuital": once a pre-processing thermal analysis is performed, the thermal metrics are used to describe the steady-state/dynamic thermal behavior of active devices, that is, a TFN is built. The TFN is a circuit composed by resistances and, if dynamic simulations are required, capacitances (R_{TH}s and thermal capacitances, C_{TH}s, respectively), which provides the temperature increment over ambient (ΔT) when fed with P_D value(s)/profile(s). Such a TFN is coupled with an electrical macromodel (i.e., a subcircuit) of the active device(s), forcing currents and voltages at the electrical nodes. The macromodel of an individual transistor is composed by (i) a standard device component as a main element, as well as (ii) resistances, and supplementary linear/nonlinear controlled sources to include specific physical mechanisms and to allow the variation of the TSEPs during the simulation run. The electrical subcircuits are connected to the TFN in order to account for the ET feedback: the ΔTs provided to each electrical device are determined at any time instant from the P_D generated by all the active components, i.e., the heat sources in the thermal model. As a result, the dynamic ET behavior of the electronic system is represented by a merely electrical network that can be solved by a commercial SPICE-like circuit simulator with little requirement in terms of CPU time and memory storage, as well as reduced possibility of convergence problems. Differently

from the other approaches, a TFN-based ET simulation only involves averaged quantities; the aforementioned ΔTs are the temperature increments averaged over a region of interest that mainly impacts the electrical behavior of the individual devices. The reconstruction of the entire temperature distribution is not allowed since this piece of information is lost. Figure 1.2 shows a schematic depiction of the ET feedback in a TFN-based approach.

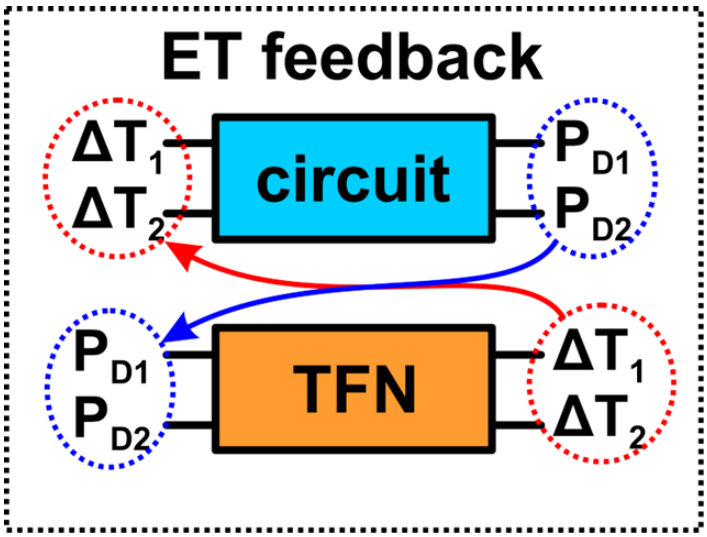

Figure 1.2. Schematic representation of a TFN-based ET simulation. The circuit is fed with the ΔT values obtained by the TFN, which elaborates them based on the P_D values of devices embedded in the circuit.

TFNs can be built through traditional approaches borrowed from the electrical engineering field (e.g., [Jak90]); however, model order reduction (MOR)-based approaches are getting the attention of research and industry. Extracting a TFN from a FEM detailed model requires an onerous pre-processing stage, during which dynamic simulations are carried out, whereas MOR approaches (i) reduce the detailed model into a lighter version and (ii) extract the TFN without any need for simulations. In addition, the TFN built by means of a MOR tool is typically more efficient and accurate with respect to the traditional one. Table 1.1 summarizes both thermal and ET analyses, with emphasis on the different approaches.

Table 1.1. Description of thermal and ET analyses, with emphasis on different approaches and input/output of each problem.

analysis	approaches	input	output
thermal	Either numerical (FEM tools) or analytical (the latter is unviable in complex structures).	P_D profile (e.g., evolution in the time domain) or fixed value, assigned to a region denoted as heat source.	Temperature distribution, from which thermal metrics (R_{TH}, Z_{TH}) can be evaluated.
ET	Numerical (FEM tools), where the electrical and thermal problems are concurrently solved, relaxation, TFN-based, MOR.	P_D (either a function of time or a constant value) and the temperature distribution over the structure under investigation are bound: the temperature distribution (generated by P_D) updates the electrical parameters of active devices, in turn changing the value of P_D. Fully-circuital approaches only involve average quantities (P_D, ΔT): such an average is performed over regions in the active devices impacting their electrical behavior	

1.3 Thesis outline

The remainder of this dissertation is organized as follows.

Chapter 2 introduces the thermal problem and defines the relevant thermal metrics (R_{TH}, Z_{TH}). Approaches for the thermal modeling of active devices, governing equations for self- and mutual-heating phenomena, both steady-state and dynamic, are provided. The Chapter includes the description of (i) the *in-house* routine developed for thermal analyses in the COMSOL Multiphysics FEM environment and (ii) modeling strategies for nonlinear thermal effects. FANTASTIC is also briefly illustrated, as a notable example of MOR-based approach for the extraction of TFNs.

In Chapter 3, FEM-based thermal analyses based on the methodology shown in Chapter 2 are described. The analyses are applied to SiC-based

PMs in order to carry out a fair comparison between two PM technologies in terms of their cooling capabilities. An *in-house* tool for the extraction of SFs – and, therefore, for the fault/defect detection – in PMs characterized by upward and downward heat fluxes is also presented.

Chapter 4 describes a novel experimental technique for the extraction of Z_{TH} in power electronics devices working in their standard operative conditions. More specifically, a thermal impedance measurement technique drawing inspiration from Rinaldi's approach [Rin01] is first presented and then unambiguously verified through the 'simulated experiments' methodology applied to (i) a SiC-based multichip PM and (ii) a GaN-based PCB-embedded power circuit.

Chapters 5 and 6 present TFN-based ET simulations. Chapter 5 focuses on the simulation of a single device (a SiC MOSFET), which is subdivided into a definite number of individual cells. This *multicellular* approach aims at optimizing the trade-off between computational efficiency and accuracy when multiple heat sources are accounted for. The strategy is articulated as follows: (i) the device is discretized into an assigned number of individual cells described with a simple, yet accurate model accounting for the relevant influence of SiO_2/SiC interface traps; (ii) the cell model is implemented with a SPICE-compatible subcircuit; (iii) thermal analyses are conducted on an exceptionally accurate 3-D FEM representation of the device; (iv) a dynamic TFN is obtained from the FEM representation by exploiting FANTASTIC and also taking into account nonlinear thermal effects; (v) a purely-electrical macrocircuit describing the whole ET behavior of the power device is constructed and simulated in very short times and with unlikely occurrence of convergence problems.

Chapter 6 shows the simulation of multi-chip power circuits embedded in PMs, namely, a synchronous step-up dc-dc converter and a single-phase inverter. Single devices of such circuits are not subdivided into individual cells, whereas mutual thermal and electrical interactions between multiple devices are considered. Good accuracy is ensured by considering electromagnetic effects due to parasitics, and low CPU times are needed with no convergence issues in spite of the high switching frequencies. The impact of some key parameters is effortlessly quantified, showing the efficiency and versatility of the approach.

In Chapter 7, conclusions are finally drawn.

Chapter 2

Characterization of the thermal behavior of electronic devices

2.1 The thermal problem

2.1.1 Modeling steady-state self-heating effects

The steady-state thermal behavior of an electronic device is effectively described by the R_{TH} [K/W], which represents an indicator of the inaptitude of the component to drain the heat off the power dissipation region and is given by

$$R_{TH} = \frac{T - T_B}{P_D} = \frac{\Delta T}{P_D} \tag{2.1}$$

where T is the temperature averaged over a region markedly impacting the electrical behavior of the device (e.g., the base-emitter junction of a bipolar transistor, T_j, or the channel region of a MOSFET, T_{ch}), and T_B is the backside (or baseplate, or ambient) temperature that can be assigned through a thermochuck/heater. P_D is evaluated as

$$P_D = I_B \cdot V_{BE} + I_C \cdot V_{CE} = I_E \cdot V_{BE} + I_C \cdot V_{CB} \tag{2.2}$$

in a bipolar transistor, and as

$$P_D = I_D \cdot V_{DS} \tag{2.3}$$

in a MOSFET. R_{TH} depends on (i) device and heat source geometry, (ii) thermal conductivities k [W/μm K] of the materials crossed by the heat emerging from the heat source, and (iii) boundary conditions. Additionally, it must be considered that the value of k in semiconductors and metals decrease with temperature, thus lowering the heat transfer efficiency, while those of insulating materials typically increase. The thermally-induced k degradation introduces a nonlinearity in the heat conduction equation, and the resulting effects are referred to as nonlinear thermal effects. It is well known that, in a practically relevant temperature range, the k of many semiconductors of interest reduces with a power law

$$k(T) = k(T_0) \cdot \left(\frac{T}{T_0}\right)^{-\alpha} \tag{2.4}$$

where the reference temperature T_0 is equal to 300 K and $\alpha > 0$, while for the metals the decrease is well described by the following linear model:

$$k(T) = k(T_0) - \beta \cdot (T - T_0) \tag{2.5}$$

where $\beta > 0$. Commonly accepted values for $k(T_0)$, α, and β corresponding to the most relevant semiconductors and metals are reported in Table 2.1. Modeling approaches taking into account nonlinear thermal effects are detailed in Section 2.3.

2.1.2 Modeling transient self-heating effects

As far as the dynamic thermal behavior of devices is concerned, the Z_{TH} [K/W], also referred to as normalized temperature rise response to a power step, is defined as (e.g., [Die61], [Chr96], [Rus10])

$$Z_{TH}(t) = \frac{T(t) - T_B}{P_D} = \frac{\Delta T(t)}{P_D} \tag{2.6}$$

where$T$and T_B have their customary meaning, and P_D is the amplitude of a power step applied at t=0. Hence, Z_{TH}(t) numerically coincides with

the temperature rise response [K] to a unitary power step. Eq. (2.6) can be rewritten as

$$\Delta T\left(t\right) = T\left(t\right) - T_B = Z_{TH}\left(t\right) \cdot P_D \tag{2.7}$$

The R_{TH} value can be obtained from the Z_{TH} by evaluating its static value

$$R_{TH} = \lim_{t \to \infty} Z_{TH}\left(t\right) \tag{2.8}$$

Figure 2.1 schematically shows typical waveforms for $P_D(t)$ and $Z_{TH}(t)$.

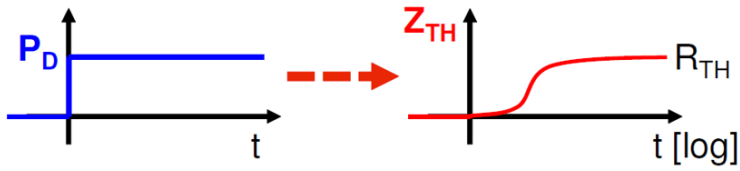

Figure 2.1. Schematic depiction of the $P_D(t)$ unitary step (left) and of the $Z_{TH}(t)$ (right), traditionally shown with the logarithmic x-axis as its time evolution spans multiple decades.

For a general dissipated power profile $P_D(t)$, Eq. (2.8) can be extended as follows [Ger00], [Ger02]:

$$\begin{aligned} \Delta T\left(t\right) &= \int_0^t \frac{dZ_{TH}}{d\tau}\left(t-\tau\right) \cdot P_D\left(\tau\right) d\tau = \frac{dZ_{TH}(t)}{dt} \otimes P_D\left(t\right) = \\ &= Z_{TH,pulse}\left(t\right) \otimes P_D\left(t\right) \end{aligned} \tag{2.9}$$

that is, $\Delta T(t)$ is expressed as a convolution product between $Z_{TH,pulse}(t) = dZ_{TH}/dt$ [K/sW=K/J] and the transient power profile P_D(t) [Cod05]. $Z_{TH,pulse}(t)$ can be defined as the temperature rise response to an ideal (infinite) power pulse (or impulse) applied at t=0 divided by the unitary energy of the pulse (not practically measurable in a direct way); by calculating $Z_{TH,pulse}(t)$ as dZ_{TH}/dt, it can be seen that it rapidly increases, then decreases, and reduces to 0. It is straightforward to verify that, if P_D is a constant power step applied at t=0, Eq. (2.9) reduces to Eq. (2.7). Let us now consider the case in which the TFN is represented by an equivalent (passive) Foster (chain) network composed by N series-connected RC

pairs [Jak90]. TFNs are based on the TEOL, where current, voltage, resistances, and capacitances actually correspond to power [W], temperature rise [K], thermal resistances [K/W] and capacitances [J/K], respectively. In general, if $Z(s)$ is the impedance of the system,

$$\Delta T\left(s\right) = Z\left(s\right) \cdot P_D\left(s\right) \tag{2.10}$$

Considering the specific case of the Foster network,

$$Z\left(s\right) = \sum_{i=1}^{N} \frac{R_{THi}}{1 + sR_{THi}C_{THi}} = \sum_{i=1}^{N} \frac{R_{THi}}{1 + s\tau_{THi}} = \sum_{i=1}^{N} \frac{R_{THi}/\tau_{THi}}{s + 1/\tau_{THi}} \tag{2.11}$$

In the time domain, Eq. (2.4) becomes

$$\Delta T\left(t\right) = Z\left(t\right) \otimes P_D\left(t\right) = \int_0^t Z\left(t - \tau\right) \cdot P_D\left(\tau\right)\, d\tau \tag{2.12}$$

where $Z(t)$ [K/sW] can be found by anti-transforming Eq. (2.11) and is given by

$$Z\left(t\right) = \sum_{i=1}^{N} \frac{R_{THi}}{\tau_{THi}} \cdot \exp\left(-\frac{t}{\tau_{THi}}\right) \tag{2.13}$$

Let us now observe that, if a power step with amplitude P_D is applied to the Foster network at t=0, the response $\Delta T(t)$ can be mathematically evaluated as

$$\Delta T\left(t\right) = \sum_{i=1}^{N} R_{THi} \cdot \left[1 - \exp\left(-\frac{t}{\tau_{THi}}\right)\right] \cdot P_D \tag{2.14}$$

where R_{TH} is given by the sum of the thermal resistances R_{THi} associated to the single RC pairs

$$R_{TH} = \sum_{i=1}^{N} R_{THi} \tag{2.15}$$

and, comparing Eq. (2.15) and Eq. (2.7), the thermal impedance $Z_{TH}(t)$

is given by

$$Z_{TH}(t) = \sum_{i=1}^{N} R_{THi} \cdot \left[1 - \exp\left(-\frac{t}{\tau_{THi}}\right)\right] \tag{2.16}$$

Moreover, by comparing Eq. (2.16) and Eq. (2.13), it can be easily understood that

$$Z(t) = \frac{dZ_{TH}(t)}{dt} \tag{2.17}$$

and therefore $Z(t)$ coincides with $Z_{TH,pulse}(t)$, as the derivative of the step response is the pulse response. Hence, Eq. (2.10) and Eq. (2.12) can be rewritten as [Cod05], [Mag13]

$$\Delta T(s) = Z_{TH,pulse}(s) \cdot P_D(s) \tag{2.18}$$

$$\Delta T(t) = Z_{TH,pulse}(t) \otimes P_D(t) \tag{2.19}$$

where $Z_{TH,pulse}(s)$ is the L-transformation of the derivative of the thermal impedance $Z_{TH}(t)$.

2.2 FEM thermal simulations tool

The flowchart of the *in-house* routine developed to automate steady-state and dynamic thermal analyses in the commercial FEM software package COMSOL Multiphysics [COM18] is sketched in Figure 2.2. The routine is described in the following, along with sample pictures taken from an analysis performed on a single-emitter RF device under test (DUT):

- As a first input, the routine is fed with 2-D information about the device (in the x-y plane), typically provided within a Graphic Data System (GDS) file. GDS files comprise a defined number of layers, each corresponding to a mask of the technology process. It is worth highlighting that GDS files are flexible, that is, they can also be used as a starting point for assemblies that are not built according to the photolithographic process (e.g., PMs or PCBs), as long as a correct subdivision of the structures into layers is performed.

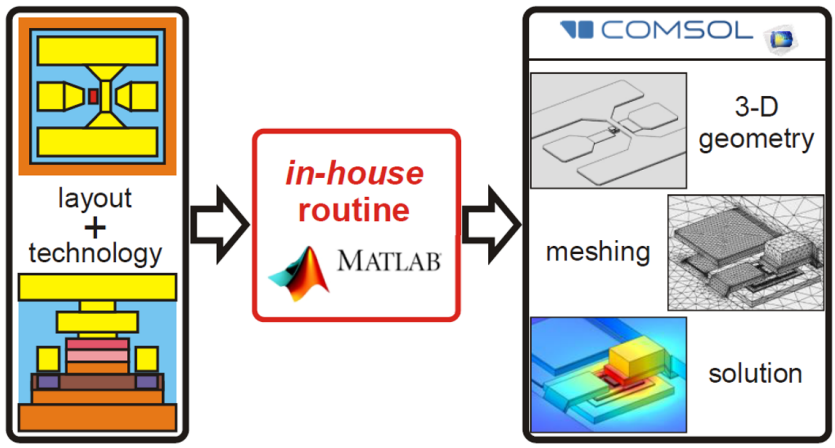

Figure 2.2. Flowchart of the *in-house* routine developed to automatically perform thermal analyses in the COMSOL environment; it relies on the livelink between MATLAB and COMSOL Multiphysics.

- The routine is also fed with technology features, namely, (i) the quote, i.e., the distance from the top surface of the substrate (denoted as z-coordinate in the COMSOL environment), (ii) the thickness, and (iii) the material parameters. All three pieces of information are required for each layer composing the structure, the first two defining the geometry along the third dimension (perpendicular to the substrate plane).
- The Griesmann's GDSII Toolbox [GDSII] is adopted to import the GDS file into MATLAB that is already linked to an active COMSOL Multiphysics session.
- Using the collected information, for each layer the routine executes the following extrusion process (Figure 2.3): (i) an x-y workplane is built where the plane geometry is drawn, (ii) the geometry is extruded by the given thickness, and (iii) the built volumes are associated to a selection including all the volumes made of the same material. The outcome is an exceptionally-accurate representation of the 3-D device/assembly structure.
- The domains are discretized into a tetrahedral grid using a smart

approach: the regions where the highest temperature gradients are expected (i.e., in the surrounding of the active device, where the power dissipation occurs) are extra-densely meshed, while the grid gradually coarsens moving to the edges of the domains. This ensures the best trade-off between simulation time/computational resources and accuracy. The optimized mesh of an RF DUT is shown in Figure 2.4. Preliminary analyses are commonly performed to demonstrate the mesh convergence, i.e., further mesh refinements do not appreciably modify the solution.

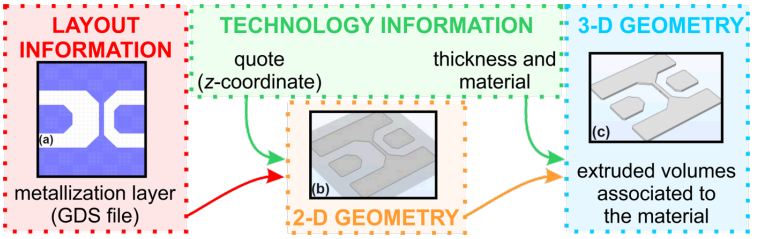

Figure 2.3. Flowchart of the extrusion process: (a) metallization layer from the GDS file; (b) workplane in the COMSOL environment with the 2-D representation of the layer; (c) corresponding extruded volumes.

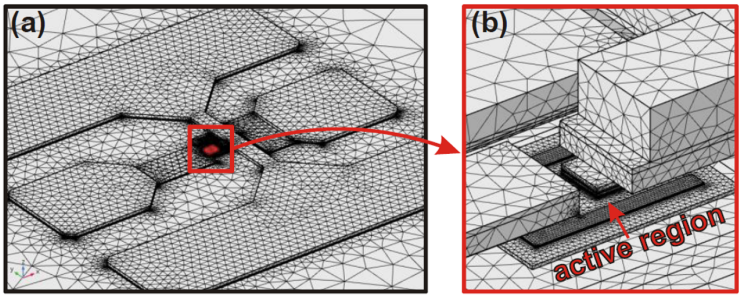

Figure 2.4. Mesh of a single-emitter RF DUT: (a) full view; (b) detail of the finer discretizing grid in the surrounding of the device region, where highest temperature gradients are expected.

- The thermal problem is properly defined to emulate the typical conditions encountered during on-wafer/laboratory experimental char-

acterizations: adiabatic (i.e., thermally reflecting), isothermal (i.e., fixed temperature), and convective (i.e., with an assigned heat transfer coefficient h) boundary conditions (BCs) can be applied. The heat source and cooling surfaces (CSs) are also defined.

- The solution of the thermal problem is carried out, either performing a steady-state or a dynamic simulation, and the post-processing is done in MATLAB.

2.2.1 Steady-state and dynamic thermal simulations

The steady-state thermal-only simulations are conducted using the above *in-house* routine: the numerical solver PARDISO [Sch01] is enabled to exploit the multi-core features of modern CPUs. Depending on (i) the size of the domain under investigation, that is, the number of elements (tetrahedra) into which the assembly is discretized, and (ii) the material properties, which are optionally dependent on the device temperature (Section 2.1.1), simulations can last from tens of seconds up to tens of minutes. The resulting temperature maps in the 3-D structure are visualized in the COMSOL Multiphysics graphical interface (Figure 2.5).

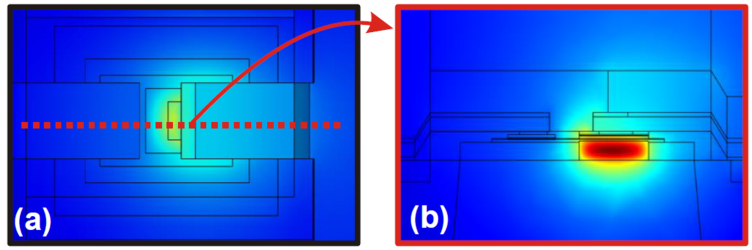

Figure 2.5. Solution of a thermal simulation run by COMSOL Multiphysics: temperature field in a single-emitter RF DUT. (a) top view and (b) cross-section view along the dashed red cut in (a).

The *in-house* routine and COMSOL solver also provide tool for the investigation of the time evolution of temperature; these analyses are aimed to quantify the self- and mutual-heating thermal impedances of devices. Simulation time and CPU resources are higher than the steady-state case, as simulations typically last more than 1 h on a normal PC.

2.2.2 Model-order reduction techniques

To extract the TFNs used to perform steady-state and dynamic ET simulations, a MOR-based approach can be exploited, as briefly described in this Section by means of the workflow reported in Figure 2.6. The mesh obtained from commercial (e.g., COMSOL) or open-source tools (e.g., SALOME SMESH), as well as material properties and BCs, are fed as an input to a routine developed by Codecasa [Cod03a], [Cod03b], [Cod14]. The fully automatic MOR relies on the Multi-Point Moment Matching (MPMM) technique [Cod03a], [Cod03b] and its subsequent improvements, also known in literature as FANTASTIC [Cod14], [Mag14], in which the model precision is user-defined by specifying a single error parameter. The TFN topology for n heat sources requires a small number of RC pairs and is given as output in the form of SPICE netlist. The MPMM algorithm involves the solution of a limited number of thermal problems in the frequency domain (denoted as moments) at automatically evaluated frequencies σ_j. The TFN is equipped with the following terminals: P_1, ... P_n are the power inputs for the heat sources, the average temperature rises of which are given by ΔT_1, ... ΔT_n; ξ_1,..., ξ_n are additional variables that allow reconstructing the temperature field over all the points of mesh, and at any time instant, in a post-processing step. This approach benefits from the following advantages: (i) it is extremely fast since it does not require computationally-demanding dynamic thermal simulations in the pre-processing, while preserving all the information of the detailed FEM model; (ii) it can be used for power devices and circuits, including modules and packages, with arbitrary geometries. As will be shown in Chapter 5, the MOR-approach has been exploited to analyze the ET behavior of multi-chip SiC-based PMs.

2.3 Modeling nonlinear thermal effects

As seen in Section 2.1.1, the thermal problem is inherently characterized by a nonlinearity in the heat transfer equation, as the device temperature increases (and k decreases) for two distinct physical mechanisms: (i) the raise in T_B (nonlinear thermal effect due to the backside temperature) and (ii) the increase in P_D (nonlinear self-heating effect).

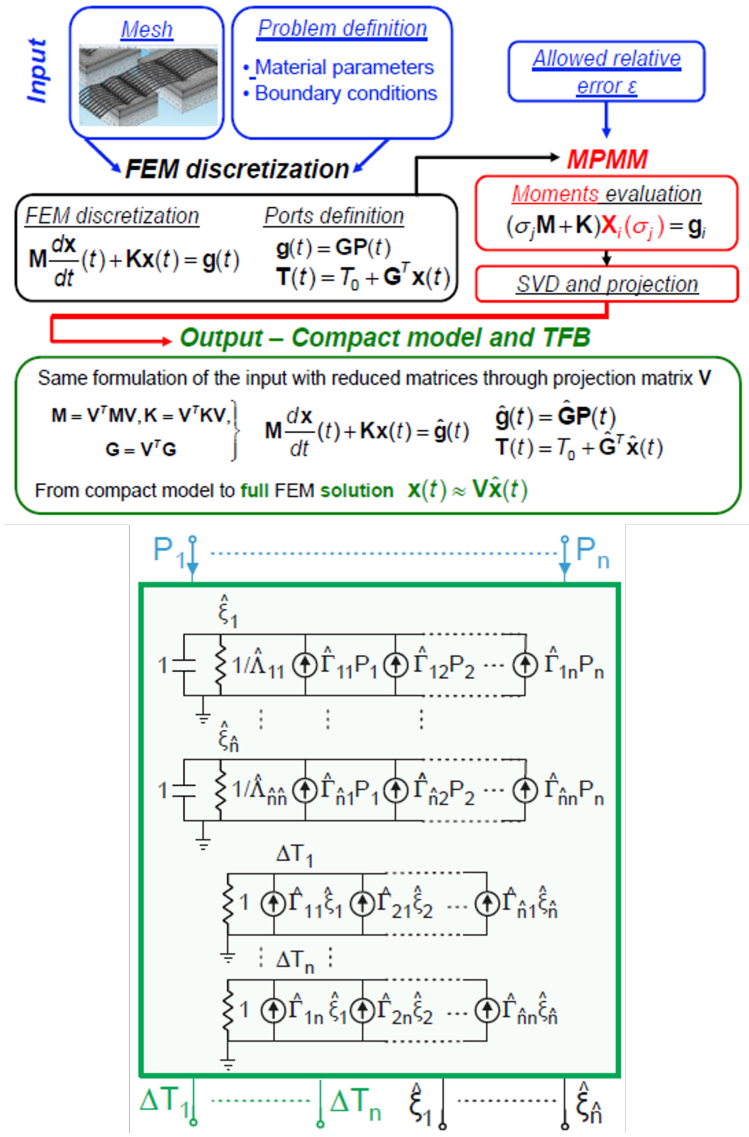

Figure 2.6. Schematic flow of the extraction procedure of a TFN based on FANTASTIC (top) and TFN topology implemented with SPICE primitives (bottom).

Consequently, R_{TH} is a monotonically-growing function of both T_B

and P_D, and should be more properly formulated as $R_{TH}(T_B, P_D)$, where the dependence on T_B and P_D does not come from the explicit presence of these quantities on the RHS of Eq. (2.1), but implicitly stems from the k reduction with increasing temperature [Wal02]. In the following, an illustrative overview and a straightforward modeling approach for the R_{TH} dependence on T_B and P_D are provided by considering an ideal device composed of a single homogeneous semiconductor obeying Eq. (2.4) (single-semiconductor assumption). For this simple case, R_{TH} is inversely proportional to k; consequently, the R_{TH} increase dictated solely by T_B (i.e., for very low P_D) can be described by the power law [Yea99], [Wal02], [Paa04].

$$R_{THB0} = R_{TH}\left(T_B, P_D \to 0\right) = R_{TH00} \cdot \left(\frac{T_B}{T_0}\right)^{\alpha} \tag{2.20}$$

where R_{TH00} is the R_{TH} of the device at T_B=T_0 and very low P_D (ideally for P_D→0 W, i.e., in the absence of the nonlinear self-heating effect) while R_{THB0} is the R_{TH} of the device at an arbitrary T_B value and very low P_D. The nonlinear self-heating effect due to P_D can be accounted for by invoking Kirchhoff's transformation [Car59], [Joy75], [Nec89], which leads to

$$R_{TH}\left(T_B, P_D\right) = \frac{T_B}{P_D} \cdot \left\{ \left[1 - (\alpha - 1) \cdot \frac{R_{THB0} \cdot P_D}{T_B} \right]^{\frac{-1}{\alpha - 1}} - 1 \right\} \tag{2.21}$$

It is worth highlighting that, in principle, Kirchhoff's transformation (i) requires a homogeneous domain and (ii) only works in the steady-state case. However, it was demonstrated that:

- by calibrating R_{TH00} and α in a not homogeneous domain, nonlinear self-heating effects can still be accounted for [dAl22].
- Kirchhoff's transformation is a good approximation even in the transient case, as shown in Chapters 5 and 6).

In the case of a homogeneous domain, α coincides with the nonlinear coefficient of the material, while in the other case the calibration of R_{TH00} and α can be performed according to a 2-D "brute force" approach suggested by Yeats [Yea99]. Reference data (e.g., extracted through thermal-only FEM simulations in the COMSOL environment, as detailed in Section 2.2)

are used to find the parameters values ensuring the best agreement with Eq. 2.21[1].

[1]Generally, after such 2-D optimization, the R_{TH00} value is very similar to the linear R_{TH} extracted by COMSOL in a linear thermal-only simulation, i.e., a simulation conducted by deactivating the thermally-induced k degradation.

Table 2.1. Values of thermal conductivity and nonlinear parameters for the most important semiconductors and metals in electron devices.

material	$k(T_0)$ [W/μm·K]	α	β [K^{-1}]
Si	1.422×10^{-4} [Sha63], 1.45×10^{-4} [May67], 1.48–1.54×10^{-4} [Pal04], 1.56×10^{-4} [Gla64]	1.25 [Lee93], 1.3 [Wyb88], [Bon95], 1.33 [Sha63], [Neg89], [May67], 1.4 [Wal02], [Gla64], 1.65 [Pal04] although 1.3 seems better (see Ref. [2] in [Pas04])	-
GaAs	0.44×10^{-4} [May67], 0.37–0.46×10^{-4} [Pal04], 0.55×10^{-4} [Bla82]	1.25 [Pal04], 1.27 [Wal02], [Bla82]	-
GaN	1.25–1.5×10^{-4} [Pal04]	0.43 [Pal04]	-
4H-SiC	3.7×10^{-4} [Pal04], [Ali65], 0.696×10^{-4} [Jar17]	1.29 [Jos00]	-
6H-SiC	3.2–4.9×10^{-4} [Pal04], 3.87×10^{-4} if normal to the c axis; 30% lower if parallel to the c axis [Bur79]	1.29 [Jos00], 1.49 if normal to the c axis [Bur79]	-
Al	2.39×10^{-4} [Lie08]	-	2.1×10^{-8} [Lie08]
Cu	3.97×10^{-4} [Lie08]	-	5.2×10^{-8} [Lie08]

2.4 Summary

In this Chapter, the theory behind thermal analyses is provided, along with (i) thermal metrics describing the steady-state and dynamic thermal behavior of electronic devices and circuits, (ii) thermal parameters of the most relevant semiconductors and metals for electronic devices, and (iii) insights into nonlinear thermal effects and steady-state/dynamic thermal modeling. The *in-house* tool for automatic FEM thermal analyses in the COMSOL Multiphysics environment is also presented.

Chapter 3

Thermal investigation of power electronics systems

In this Chapter, results of the thermal analyses on PMs are shown. More specifically, Section 3.1 compares the thermal behavior of SiC-based single-sided cooled (SSC) and double-sided cooled (DSC) PM technologies; results focus on the heat spreading effects in both PMs and special attention is given to the role of the BCs applied on the CSs. BCs were varied by modifying the h value spanning the range 10^1–10^9 W/m^2·K, that is, from free convection to forced liquid cooling. Section 3.2 applies the SF algorithm to Z_{TH}s of flawed DSC PMs, with the aim of identifying the defects/faults in seemingly flawless systems by means of simple thermal measurements.

3.1 Power modules technologies: SSC vs. DSC

3.1.1 Single-sided cooled power modules

SSC PMs represent the standard in the power electronics industry, as they are a common solution to implement a power circuit on a substrate in lieu of a PCB. As depicted in Figure 3.1, such a PM is characterized by two couples of a commercial SiC VDMOS transistor manufactured by CREE (BV_{DS}=1.2 kV, max I_D=36 A [CREE]) and it is compatible with standard PCB mounting processes [Cas14]. Although the four devices can

be used to realize a full H-bridge, here they are arranged in a half-bridge configuration with a doubled current rating.

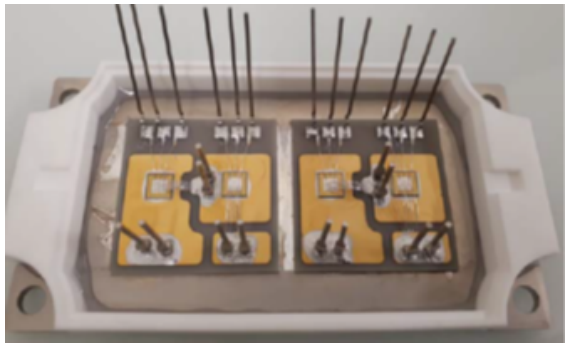

Figure 3.1. Picture of the SSC PM under investigation: it embeds four 3.3 kV SiC VDMOS transistors placed on two separate DBC substrates, which in turn lie on a 120×60 mm^2 Cu baseplate.

Figure 3.2 shows the schematic cross-section of the SSC PM.

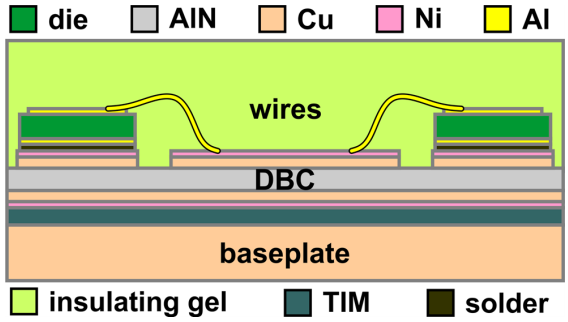

Figure 3.2. Schematic cross-section (not to scale) of the SSC PM, with materials identified by different colors. Evidenced are: the Al wire bonds, the Cu baseplate, and the DBC substrate comprising Cu metallization and AlN layer.

Each die is 7.2×7.2 mm^2-large and 0.4 mm-thick and contains one transistor; the two VDMOS couples lie on two separate 40×40 mm^2-large and 1.336 mm-thick direct-bonded copper (DBC) substrates, which consist in sandwich-like structures made of an aluminum nitride (AlN) sheet in

between two copper (Cu) foils [Sco20a], as shown in Figure 3.3. Among the materials adopted for the insulating sheet, ceramic ones offer a good trade-off between thermal conductivity, electrical ruggedness, and thermal expansion coefficient. While the bottom Cu foil is kept plain to ensure a good thermal contact with the 3 mm-thick baseplate underneath, the layout of the top one is composed by metal islands in order to draw the circuit topology. Electrical interconnections between Cu islands and devices are granted by aluminum (Al) wire bonds with a diameter of 0.3 mm [Hus18]. An insulating gel is poured over the entire top surface in order (i) to increase the dielectric integrity and (ii) to avoid undesirable effects such as partial discharge and dielectric breakdown [Sco20b]. For the PM under analysis, a 5 mm-high silicon gel produced by Sylgard was considered [Sco20c]. Since the module PADs are covered by the insulating gel, Al vertical connectors are required to make them accessible.

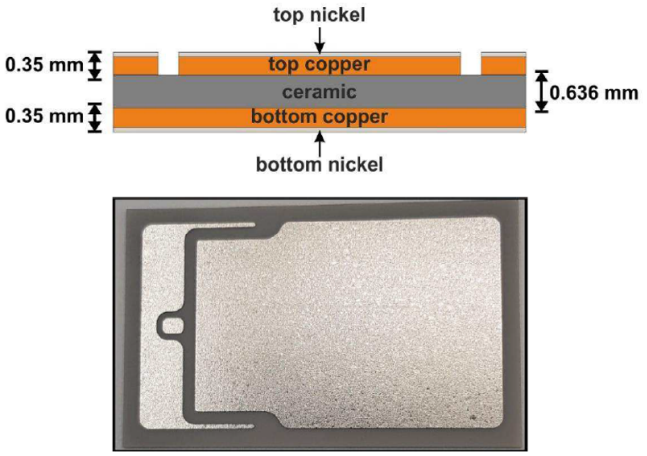

Figure 3.3. (top) Schematic cross section of DBC substrate highlighting material and thickness of each layer; (bottom) picture of a DBC substrate ready to be used in the PM fabrication process.

3.1.2 Double-sided cooled power modules

Differently from the SSC architecture, DSC PMs (Figure 3.4) are characterized by two interfacing substrates. Dies are soldered through thin

solder films, thus connecting the drain/collector contact of the power device to the substrate. Wirebonds adopted in SSC PMs are replaced by vertical Cu interconnections denoted as electrical bumps. Bumps can have several shapes: for instance, filled and hollow cylinder-shaped bumps can be used [Li14], as well as spherical ones, and they effectively mitigate the impact of parasitic inductances and resistances. Electrical bumps are soldered to connect the device pads and the interfacing substrate; usually, one is used to connect the relatively small gate pad, while a higher number of bumps (e.g., 2 or 3) are placed on each source/emitter pad. Wider bumps are located between the interfacing substrates: they are referred to as mechanical bumps, since they also offer mechanical support to the assembly. DBCs in AlN technology were considered. Similarly to the SSC variant, the PM under investigation embeds four dies, each of them containing the same device as the SSC PM. The dies lie on the internal Cu layers, which are designed in the form of islands to realize the circuit topology. DSC PMs are also prone to be enclosed in forced liquid coolers, with direct substrate impingement [Sol14]. A schematic cross-section of the DSC PM under investigation is shown in Figure 3.5.

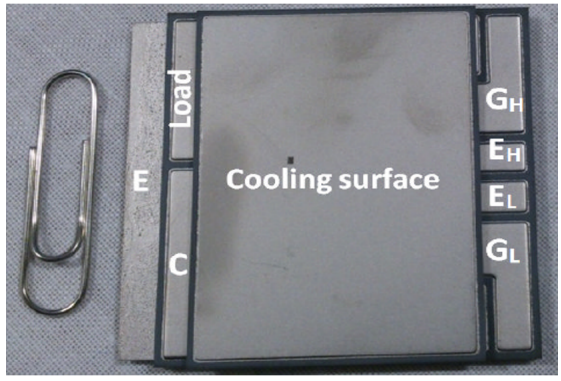

Figure 3.4. Picture of the DSC PM under investigation, the size of which is compared to a paperclip. External surfaces are either used for cooling purposes or electrical connections.

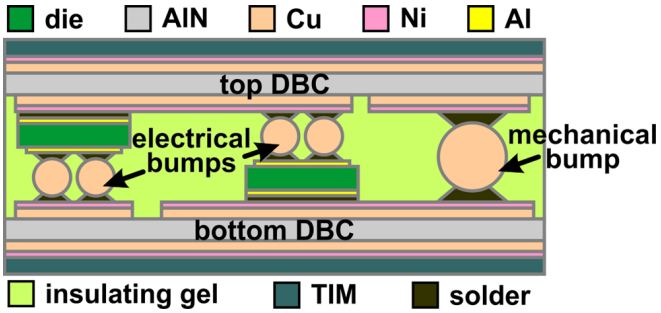

Figure 3.5. Schematic cross-section (not to scale) of the DSC PM, with materials identified by different colors. Evidenced are: the Cu electrical and mechanical bumps and the DBC substrates.

3.1.3 Thermal performance comparison

An exact replica of the two PMs was built in the COMSOL Multiphysics environment. Figure 3.6 shows both assemblies, while Figure 3.7 focuses on electrical interconnections (wirebonds for the SSC PM, cylinder-shaped bumps for the DSC counterpart). Materials parameters adopted in FEM simulations are reported in Table 3.1. The domains were meshed following the smart discretization strategy detailed in Section 2.2; results of this step are represented in Figure 3.8, showing details of the grid in the surroundings of electrical interconnections. The optimized meshing strategy is aimed to reduce the computational effort without sacrificing accuracy; in the SSC domain, the number of tetrahedra and degrees of freedom amount to 750k and 1000k, while the DSC is characterized by 450k tetrahedra and 650k degrees of freedom. As far as the thermal problem is concerned, both heat sources and sensing areas (where the temperature distributions are evaluated to obtain thermal metrics) were assumed to coincide with the top faces of the dies, which correspond to the channel region of the VDMOS transistors. With regards to the BCs, the cooling action was supposed to be accomplished solely by CSs; therefore, the heat flux through the remaining external surfaces was neglected. Such surfaces were then defined as adiabatic, while convective BCs with a heat transfer coefficient h were applied on the baseplate bottom surface (on the DBCs external surfaces) in the SSC (DSC) PM.

Table 3.1. Values of thermal conductivity, heat capacity, and mass density for the materials adopted in FEM simulations of SSC and DSC PMs.

material	$k(T_0)$ [W/m·K]	c_p [J/Kg·K]	ρ [Kg/m^3]
4H-SiC	370 [Table 2.1]	690 [Pal04]	3211 [Pal04]
AlN (ceramic)	150 [Cat19], [Pin02]	748 [Pal04]	3230 [Pal04]
Al	200 [Table 2.1]	905 [Lie08]	2707 [Lie08]
Cu	398 [Table 2.1]	384 [Lie08]	8954 [Lie08]
SnAg (solder)	57 [Cat19]	220 [Cat19]	7500 [Cat19]
insulator	0.29 [Cat19]	1624 [Cat19]	1024 [Cat19]
Si_3N_4	18.5 [Cat19]	787 [Cat19]	3100 [Cat19]

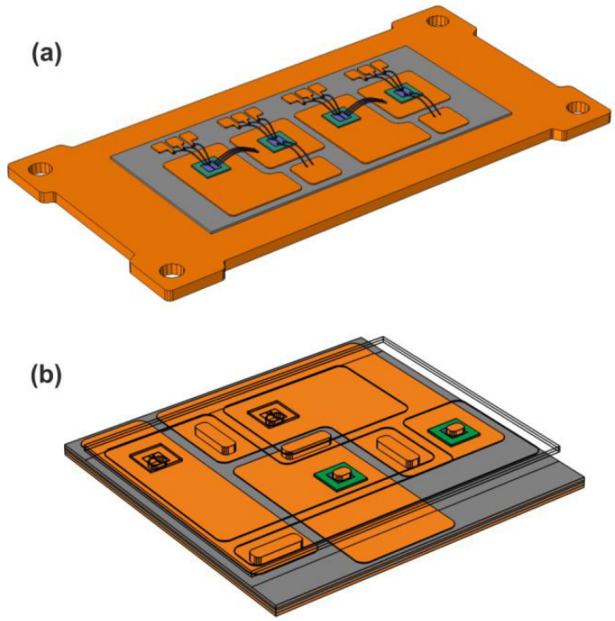

Figure 3.6. 3-D representations in COMSOL Multiphysics (draw mode) of (a) SSC and (b) DSC PMs; for illustrative purposes, the top DBC, the transistors, and interconnections are shown in transparency in (b).

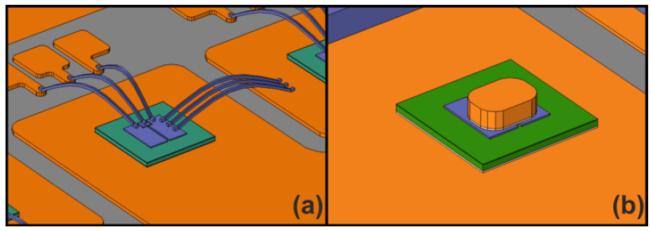

Figure 3.7. 3-D representation in COMSOL Multiphysics (draw mode) of the electrical interconnections in the PMs under analysis; (a) SSC wires and (b) DSC bumps.

A constant h value was adopted, which is assumed to include (i) the heating up of the cooling fluid and (ii) all the convection phenomena. Attention was paid to study the heat flux in such structures in the broad range h=3×10^{-1}–3×10^{8} W/m^2·K, where the minimum and maximum values replicate natural convection and the intimate contact between the CSs and an ideal thermochuck, respectively. Nevertheless, results shown are mostly related to a practical h range (identified within 3×10^{1}–3×10^{5} W/m^2·K) emulating cooling solutions in common applications [Sol15], [Cas17], [Li17].

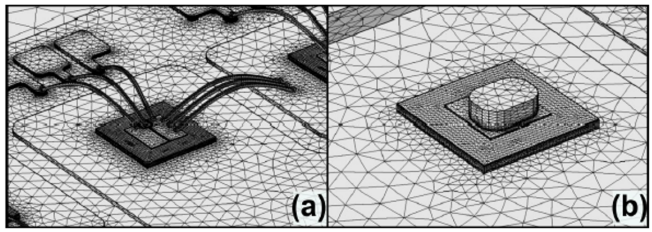

Figure 3.8. 3-D representation of dies and electrical interconnections in COMSOL Multiphysics (grid mode); (a) SSC wire bonds and (b) DSC bump.

The thermal performances of the PMs were methodically compared in terms of self- and mutual-heating R_{TH} of the individual transistors. The matrices containing self- and mutual-heating R_{TH} (denoted as $R_{TH,SH}$ and $R_{TH,MH}$, respectively) were determined for the SSC and DSC PMs by varying the BCs applied on the CSs. Since the ET effects affecting devices are more pronounced as their R_{TH} grows, the maximum values of $R_{TH,SH}$ ($R_{THmax,SH}$) and $R_{TH,MH}$ ($R_{THmax,MH}$) were evaluated for each

h value. Results are shown in Figure 3.9.

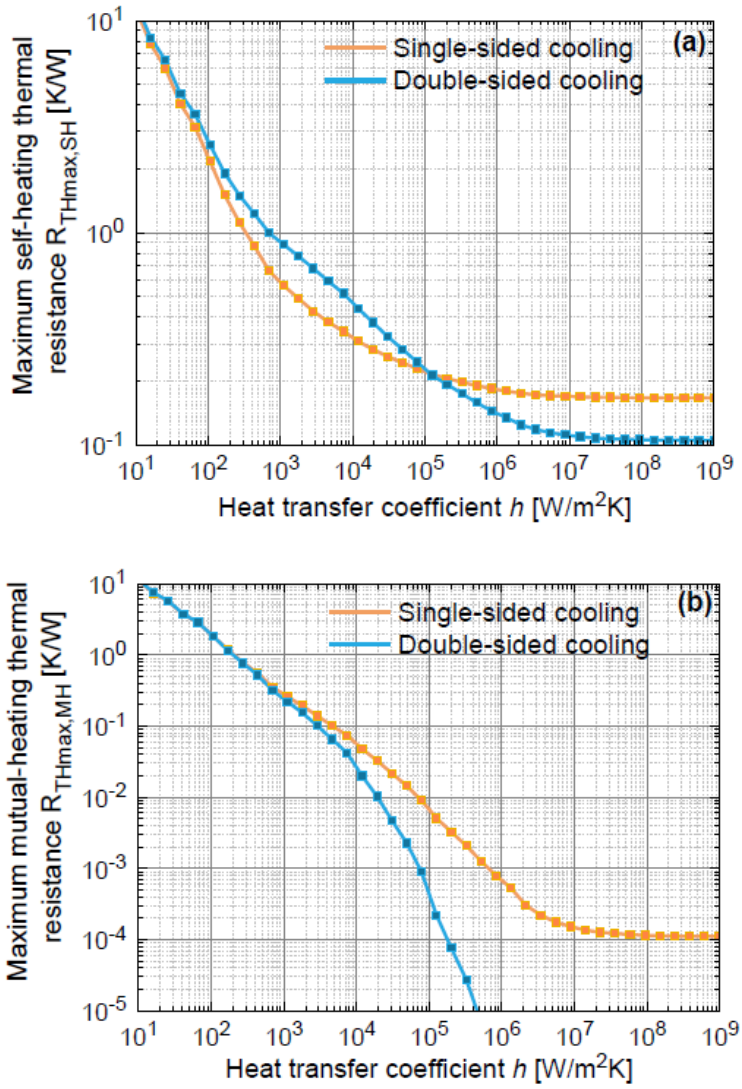

Figure 3.9. (a) $R_{THmax,SH}$ and (b) $R_{THmax,MH}$ *vs.* h evaluated by FEM simulations; SSC data (orange lines) are compared with DSC results (blue).

Good BCs (h>10^6 W/m^2·K) justify the choice of the more expensive

and harder-to-manufacture DSC technology, since in this case a marked reduction in $R_{THmax,SH}$ (down to -23%) is obtained with respect to the SSC solution, and mutual heating effects are negligible (Figure 3.9b). On the other hand, Figure 3.9a shows the occurrence of a trend reversal point (TRP) for $R_{THmax,SH}$ at $h \approx 10^5$ W/m^2·K, that is, the SSC technology has to be preferred for poorly-cooling BCs. This behavior can be explained as follows. While the SSC structure lies on a thick and wide Cu baseplate that favors the heat spreading, the DSC PM enjoys two CSs closer to the heat sources (see Figure 3.5). The balance between these two features is represented by the TRP, which separates the low convection region ($h < 10^5$ W/m^2·K), where the beneficial effect of the SSC baseplate prevails, from the high convection one ($h > 10^5$ W/m^2·K), where the couple of CSs of the DSC PM dominates. Figures 3.10 and 3.11 support the comprehension of these phenomena by showing modules and directions of the heat flux vector (obtained by FEM simulations) in SSC and DSC PMs, respectively. In both structures, low h values encourage the heat spreading mechanism: in order to keep the outgoing heat flux unchanged, a larger area of the CSs needs to be exploited. The SSC baseplate allows obtaining $R_{TH,SH}$ values lower than the DSC counterpart by virtue of the enhanced heat spreading, which also gives rise to a more pronounced mutual-heating between neighboring devices, i.e., to higher $R_{TH,MH}$ values. Instead, at high h values, a smaller portion of the CSs needs to be exploited to drain off the thermal power: the improved thermal exchange conditions lead to a significant heat spreading reduction; Figures 3.10b and 3.11b show indeed that the heat flux in both SSC and DSC structures is much more vertical than that taking place at low h values (Figures 3.10a and 3.11a). As a result, (i) a reduction in the $R_{TH,SH}$ and (ii) negligible mutual-heating effects are observed. It is worth noting that the $R_{TH,SH}$ saturates for both PM technologies as very high h values (i.e., almost-isothermal BCs) are reached. In this scenario, a further improvement of the cooling system might have a negative impact on the design cost, while resulting in no gain on the PMs performance. A second analysis was aimed at quantifying the effect of ceramic layers on the $R_{TH,SH}$ in both PM technologies.

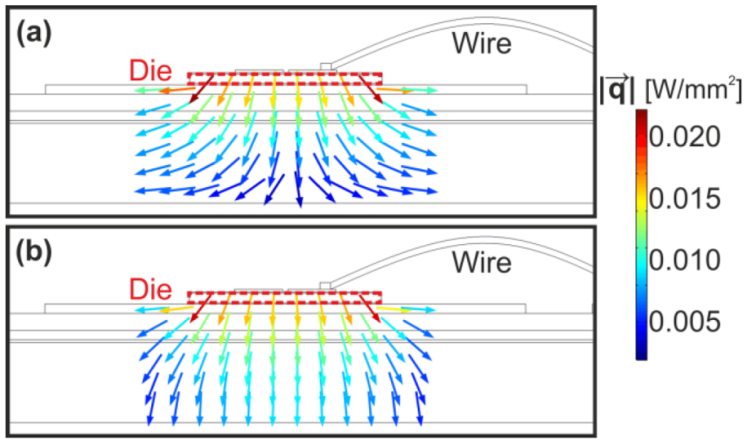

Figure 3.10. Heat flux maps showing the spreading effect in SSC structure for BCs corresponding to (a) h=10^1 W/m^2·K and (b) h=10^8 W/m^2·K. The die (containing the heat source region) is highlighted by a red box.

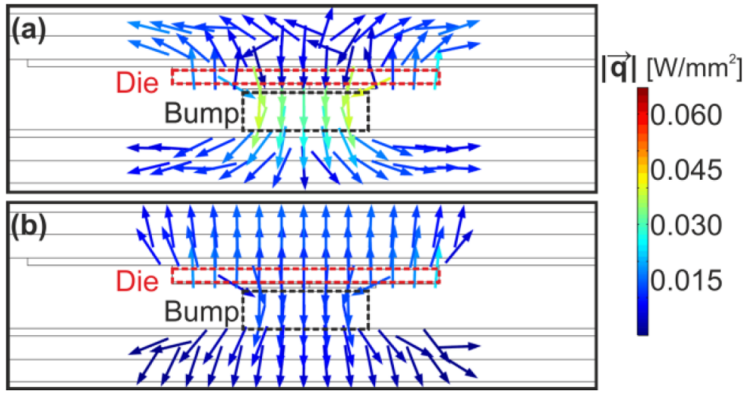

Figure 3.11. Heat flux maps obtained by simulations showing the spreading effect in DSC structure for BCs dictated by (a) h=10^1 W/m^2·K and (b) h=10^8 W/m^2·K. The die (containing the heat source region) is highlighted by a red box. A black box surrounds the vertical interconnection (cylindrical bump) allowing the heat to flow through both CSs.

Table 3.2 shows the $R_{THmax,SH}$ in SSC and DSC architectures obtained with the target to compare Si_3N_4 and AlN as DBC ceramic materials.

Table 3.2. $R_{THMAX,SH}$ for Si_3N_4- and AlN-based DBCs in SSC and DSC PMs.

	SSC $R_{THMAX,SH}$ [K/W]		DSC $R_{THMAX,SH}$ [K/W]	
h	10^2	10^8	10^2	10^8
Si_3N_4	1.75	0.418	2.38	0.354
AlN	1.49 (-14.9%)	0.167 (-60.0%)	1.90 (-20.2%)	0.105 (-70.3%)

The heat spreading mechanism in Si_3N_4-based DBCs leads to a TRP similar to that seen in AlN. The AlN advantages are almost negligible at low h values, whereas a significant $R_{THmax,SH}$ reduction (down to -70% in DSC) is observed for higher h. The results can be explained as follows: the $R_{TH,SH}$ is obtained by a series of conductive and convective contributions, which represent the heat flux across the DBCs (and the baseplate in SSC PMs) and the thermal exchange through the CSs, respectively. As the BCs are bad (good), the convective (conductive) contribution prevails over the other one, thus mitigating (enhancing) the advantages of the high-conductive DBCs in AlN technology. Moreover, the DSC $R_{TH,SH}$ is more sensitive to the conductive contribution (with respect to the SSC one) because of the two DBCs. As a consequence, using AlN – regardless of the BCs – implies a more significant $R_{TH,SH}$ reduction in DSC PMs. The above analysis leads to the following observation: due to the high AlN production cost [Gho10], designers should realize AlN-based DBCs (for both SSC and DSC technologies) only when an efficient PM cooling system is ensured. Figure 3.12 shows the maximum self-heating Z_{TH}s ($Z_{THmax,SH}$s) of SSC and DSC PMs obtained by means of a dynamic thermal analysis (as described in Section 2.2). The study of the numerical $Z_{THmax,SH}$s allowed quantifying the PMs behavior in the time domain; in particular, as BCs get better, the thermal responses in PMs are faster: at the lower bound of the practical h range, the steady-state values are reached at $t{\approx}10^4$ s and $t{\approx}2{\times}10^3$ s in SSC and DSC structures, respectively. Such a difference in the thermal inertia is due to heat spreading effects; the SSC thermal response turns out to be slower thanks to the big thermal capacitance associated to the baseplate. Conversely, no discrepancies in the thermal inertia were observed in the SSC and DSC behavior at $h{=}3{\times}10^5$ W/m^2·K (i.e., both reach their steady-state values in $2{\times}10^1$ s). Therefore, such remarks

confirm that in absence of extra-efficient cooling systems designers should prefer the SSC technology, in which the higher inertia may reduce the thermal stress in switching applications. The dynamic thermal behavior of both technologies was modeled with the 1- and 3-pair Foster networks; results are also reported in Figure 3.12.

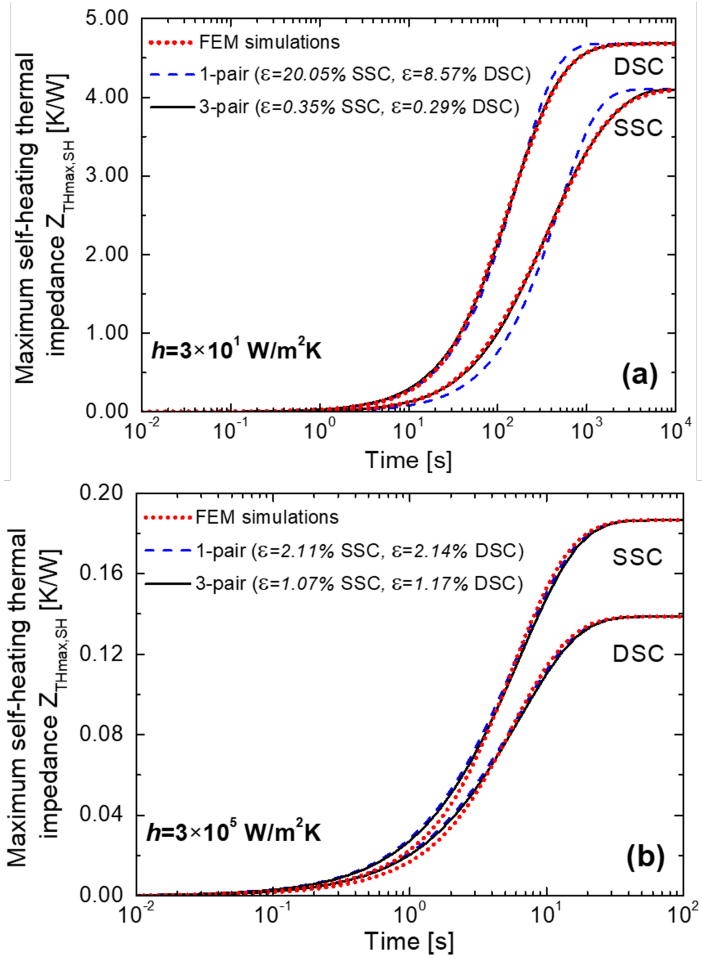

Figure 3.12. Comparison between the FEM $Z_{THmax,SH}$ (red dotted lines) and thermal models: 1-pair (blue dash) and 3-pair Foster network (black solid). The legends also contain the approximation errors ϵ.

According to

$$\varepsilon = \frac{\sqrt{\int \left(Z_{TH}(t) - Z_{TH,Foster}(t)\right)^2 dt}}{R_{TH}} \tag{3.1}$$

it was possible to quantify the mismatch between the numerical Z_{TH}s and the thermal models. The analysis allows inferring that – regardless of BCs and the PM technology – the modeling with 3 pairs properly fits the PM dynamic behavior (since ϵ values span within 0.29-1.17%). The simpler Foster network with 1 RC pair introduces a significant error when the PMs are not properly cooled (i.e., at h=3×10^1 W/m^2·K). On the other hand, at the upper bound of the practical h range, a 1-pair Foster network can be reasonably adopted, leading to ϵ values of ∼2%.

3.2 Defect detection in DSC PMs

As seen in Section 3.1, advancements in the power electronics market have led to more compact and reliable assemblies such as DSC PMs. Despite the replacement of the fragile wirebonds – representing one of the weaknesses of the SSC variant – with the more robust bumps, DSC PMs are still prone to faults and manufacturing defects, which require fast and accurate detection. In this Section, an approach based on SFs targeted to the fault/defect detection in DSC PMs is presented. As shown above, these assemblies are characterized by a bidirectional (upward and downward) 3-D heat flow due to the presence of two cooling surfaces, which makes the adoption of SFs more challenging.

3.2.1 SF extraction *in-house* tool

The SFs were introduced by Protonotarios and Wing in 1967 [Pro67] and thoroughly studied by Székely [Szé88]; they represent a non-invasive technique to reliably assess the conditions of a generic assembly only requiring the extraction of the Z_{TH} of devices. Although SFs were conceived to analyze domains characterized by a 1-D heat flow, Rencz [Ren05] and Codecasa [Cod07] demonstrated their applicability also for the investigation of assemblies in which the heat flow is markedly 3-D. Currently, SFs

are largely used in the power electronics industry for failure and reliability analyses (e.g., [Ali16], [Rac21]) to such an extent that proprietary software packages embed SF extraction tools within their suites. For the purposes of this work, an *in-house* tool implementing the SF extraction algorithm (schematically depicted in Figure 3.13) was developed, which draws inspiration from the JEDEC standard illustrated in [JED10].

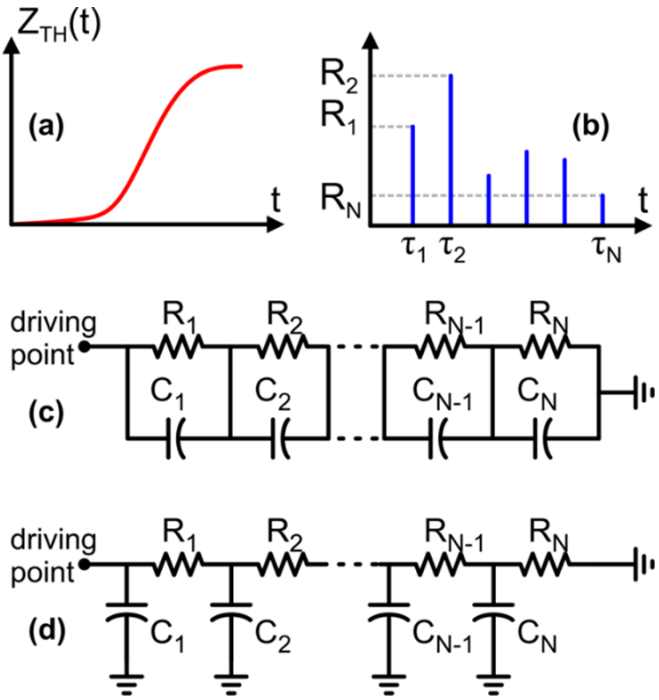

Figure 3.13. Schematic representation of the SF extraction algorithm. (a) Z_{TH} vs. time characteristics, representing the starting point of the SF extraction; (b) time constants spectrum, extracted by deconvolution; (c) Foster (chain) RC network; (d) Cauer (ladder) RC network.

The tool can be summarized as follows:

- The Z_{TH} vs. time waveform (Figure 3.13a) is fed as an input.
- The time constants spectrum is computed by exploiting a deconvolution-based approach; the spectrum associates a weight (i.e.,

an R_{TH} value) to each of the logarithmically-spaced time constants (Figure 3.13b).

- A lumped RC Foster network is reconstructed (Figure 3.13c). Such a network is composed by a high number of RC pairs (>100) to provide a high-resolution SF.

- The Foster network is then transformed into an equivalent ladder-shaped Cauer thermal network (Figure 3.13d) by a tridiagonalization approach making use of a partial re-orthogonalization ensuring robustness [Cod21].

- Finally, the cumulative and differential SFs are straightforwardly extracted from the Cauer network. More specifically, the cumulative SF (CSF) is given by the cumulative sum of C_{TH} values (C_Σ) vs. the cumulative sum of R_{TH} values (R_Σ). By further computing the CSF, the differential SF (DSF) is obtained as the derivative $\mathrm{d}C_\Sigma/\mathrm{d}R_\Sigma$ vs. R_Σ.

It is worth noting that the proposed approach can be applied to both simulated and measured Z_{TH}s.

3.2.2 Classification of defects/faults

The classification is based on the comparison between the SF of a non-defected assembly (used as a reference) and the SFs of assemblies with known defects. By assuming that each kind of defect leads to a specific shape of the corresponding SF, the classification consists in the observation of bifurcations between these SFs and the reference one. For a specific assembly, the classification can be done through the extraction of Z_{TH}s by means of either numerical simulations or experiments; the former – adopted here – are performed by emulating defects in the numerical environment, whereas the latter require the fabrication of assemblies with *ad-hoc* defects. Once the classification is done, the defect detection can be performed by comparing SFs of assemblies under test with the already classified ones. Six DSC PMs – inspired to the DSC PM described in Section 3.1.2 but embedding spherical bumps – were simulated in the COMSOL Multiphysics environment (Figure 3.14 shows details of the 3-D assembly and of the

tetrahedral grid). More specifically, a non-defected (reference, case #0) structure and others suffering from defects were investigated, as reported in Table 3.3. Cases #1, #2, #3 correspond to 1, 2, 3 detached bumps, respectively, case #4 to a defected thermal interface material (TIM), and case #5 to a delaminated solder.

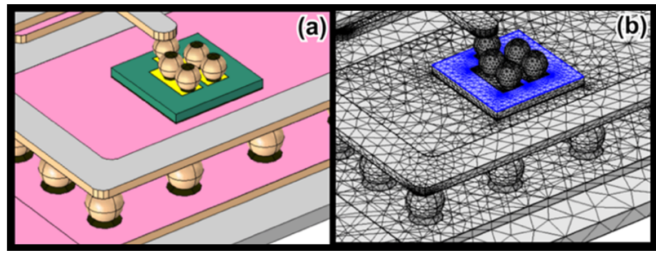

Figure 3.14. Detail of the DSC PM built in COMSOL Multiphysics (draw and grid mode); the top DBC was hidden for illustrative purposes. (a) geometry and materials details of the die region showing electrical and mechanical bumps and (b) corresponding tetrahedral grid. The heat source (coinciding with the sensing area) covers the whole top surface of the die and is highlighted in blue.

Figure 3.15 summarizes the emulated faults. The thermal simulation for the evaluation of each Z_{TH} required about 2 h. The Z_{TH}s were fed to the *in-house* tool illustrated in Chapter 2.2 to obtain the corresponding DSFs; the extraction process took 10 minutes. The DSFs of the defected PMs are compared to the reference one in Figures 3.16 and 3.17. The following observations can be made:

- Due to the bidirectional nature of the heat flow in DSC PMs, a one-to-one correspondence between DSF points and layers of the assembly cannot be defined. However, the proposed approach still allows identifying the defect through the observation of bifurcation mechanisms between the DSF of the defected PM and the reference one.
- By referring to cases #1, #2, and #3, an identification of these defects based on R_{TH}s is nontrivial since the detachment of bumps only slightly impacts the steady-state Z_{TH} value, i.e., the thermal resistance R_{TH} (the maximum increment being lower than 10% in case #3). However, as the number of detached bumps increases, a more

noticeable bifurcation is observed, which occurs in the surroundings of $R_{\Sigma} \approx 6 \times 10^{-2}$ K/W.

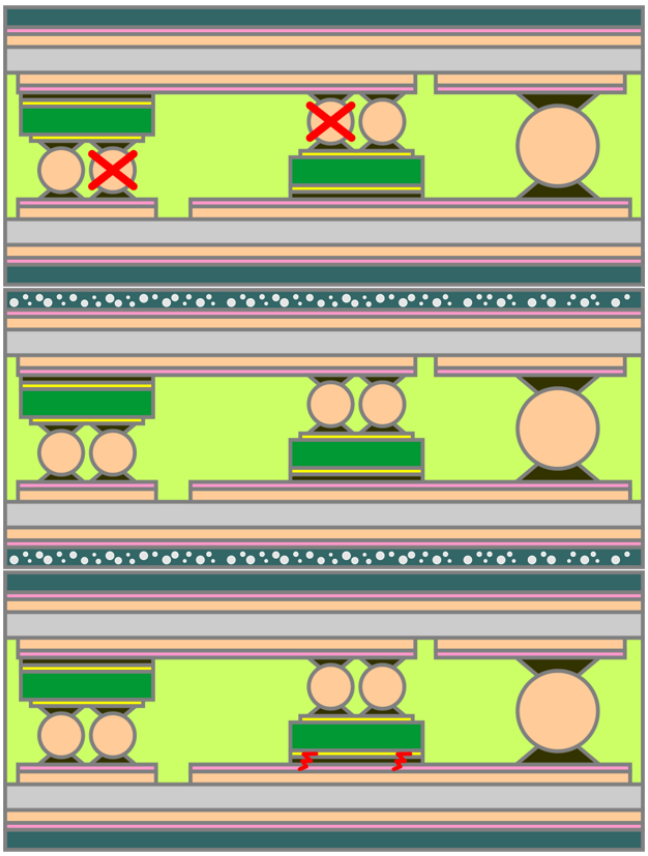

Figure 3.15. Schematic representation of emulated faults: (top) detached bumps, cases #1, #2, and #3; (middle) defected TIM; (bottom) detached solder below the die.

- Although they lead to the same increase in the overall R_{TH}, defects in cases #3, #4, and #5 affect the DSF in distinct regions of the DSF. The solder delamination occurs at R_{Σ} values lower than the one characterizing the bump detachment. On the other hand, the presence of voids/bubbles in the TIM moves the bifurcation point up

to R_{Σ}=5×10^{-1} K/W, as the heat flow reaches such a layer.

Table 3.3. Description of the defects emulated in the FEM environment. For each case, the corresponding R_{TH} value is also reported.

case	defect/fault	R_{TH}
reference (case #0)	Non-defected DSC PM (used as a reference).	0.83
n (out of 5) detached bumps (cases #1, #2, #3)	DSC PM in which the investigated device suffers from the detachment of 1, 2, and 3 out of 5 electrical bumps (cases #1, #2, and #3, respectively). In the FEM environment, n electrical bumps were removed from the geometry and replaced with insulating gel.	0.86 (#1) 0.89 (#2) 0.92 (#3)
defected TIM (case #4)	DSC PM with a defected TIM layer; the 20% of the layer was considered as composed by air, thus emulating the presence of bubbles. In the FEM environment, k, c_p, and ρ parameters of the TIM layer were obtained as the weighted average of the ones of TIM (80%) and air (20%).	0.91
delamination of die solder (case #5)	DSC PM with a defected solder layer. In the FEM environment, the SnAg k was reduced from 57 to 28 W/m·K.	0.91

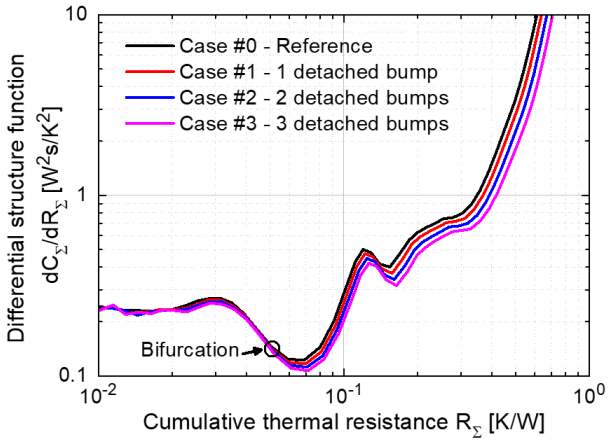

Figure 3.16. Effect of bumps detachment on DSF. The non-defected DSF in case #0 (solid black line) is compared to the ones in cases #1 (red), #2 (blue), and #3 (magenta) representing the detachment of 1, 2, and 3 bumps, respectively. Bifurcations in the DSFs (highlighted with a black circle) are observed at $R_\Sigma \approx 6\times10^{-2}$ K/W.

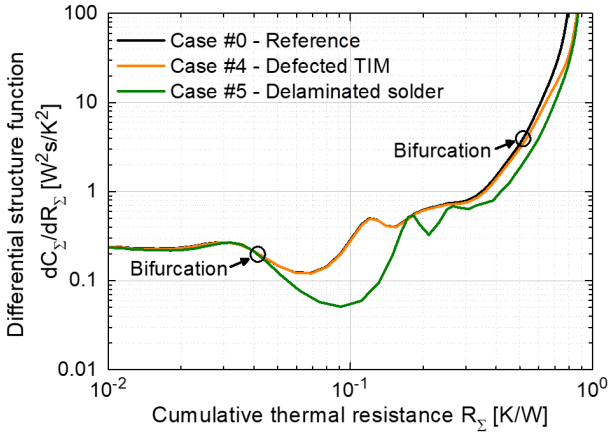

Figure 3.17. DSFs extracted through FEM simulations on case #0 (solid black line) compared with the ones of cases #4 (orange) and #5 (green) representing PMs affected by defected TIM and delamination of the die solder, respectively. Bifurcation points are also highlighted with black circles.

The above analysis allows inferring that each kind of defect introduces a discrepancy in the DSF with respect to the reference one. Once the relations between discrepancies and defects are classified by means of the proposed procedure, the approach can be exploited to identify the defects in a real potentially-faulted PM by comparing its experimental DSF with that of a non-defected PM.

3.3 Summary

In this Chapter, thermal analyses conducted on PMs are reported. First, their steady-state and dynamic thermal behavior was addressed by comparing two PM variants: SSC and DSC. As a main result, the state-of-the-art DSC PM turns out to be more convenient from a thermal point of view as long as very efficient BCs are ensured. Otherwise, the widespread and cheaper SSC solution is an overall better alternative to embed power circuits. Then, an *in-house* tool was proposed to obtain SFs by processing the Z_{TH}s; the Z_{TH}s were extracted through transient purely-thermal FEM simulations performed on the exact replica of a state-of-the-art PM. DSC PMs can be affected by solder delamination, detached interconnections, and voids/bubbles in the TIM. Such defects were emulated *ad-hoc* in the FEM software package by modifying geometry and material properties of the original domain. Results of reference (i.e., non-defected) and defected assemblies were finally compared to (i) prove the applicability of SFs in domains with a bidirectional heat flow and (ii) classify the effect of different kinds of defects on the SF.

Chapter 4

In-situ Z_{TH} measurement technique

The dynamic thermal metric introduced in Chapter 2, that is, the Z_{TH}, represents the focus of the present Chapter, where an overview of advantages and drawbacks of traditional techniques for its experimental extraction in power devices is provided. In addition, a novel technique is proposed, which addresses and potentially solves sticking points of the traditional counterparts. The theory behind the technique is inspired by Müller [Mül64] and Rinaldi [Rin01], who laid the theoretical foundations for the frequency-domain thermal characterization of RF transistors from low-frequency y-parameters. The technique is first presented along with the associated measurement setup, and then it is unambiguously validated through the 'simulated experiments' strategy applied to (i) a SiC-based multi-chip PM [Hus18] and (ii) a GaN-based PCB-integrated power circuit [EPC16]. The validation is performed by emulating the experimental procedure with TFN-based ET simulations accounting for a known $Z_{TH,j-a}$ used as a reference, and comparing the extracted $Z_{TH,j-a}$ with the reference counterpart.

4.1 Traditional Z_{TH} measurement techniques

The Z_{TH} of power semiconductor devices is typically measured in a laboratory by stimulating the DUT with square waves [Die61], [Chr96],

[JED10], [Rac21]. More specifically, the measurement is performed as follows:

- the assembly in which the device is embedded (e.g., the PM or the PCB-integrated power circuit) is put on a thermochuck/cold-plate to fix the temperature of the backside/baseplate – typically, T_B=300 K;
- the DUT is biased for a time long enough to reach the ET steady-state conditions: given a VDMOS transistor, V_{GS} and V_{DS} are applied to the device terminals;
- the P_D value is quantified by evaluating voltages/currents at the device terminals: given a VDMOS transistor, P_D=V_{DS}·I_D as described in Eq. (2.3);
- the DUT is turned off and its temperature is dynamically monitored during the so-called cooling phase.

To monitor the temperature, commonly-accepted methods can be either indirect (i.e., relying on a TSEP, the temperature dependence of which, or thermometer, must be preliminarily calibrated) or direct , such as temperature measurements through infrared (IR) cameras or thermocouples. Indirect methods require the calibration of a TSEP. Such a calibration is performed as follows: first, T_B is fixed with an external system. Then, the TSEP (e.g., the threshold voltage of a MOSFET) is monitored under known electrical conditions as a function of T_B. This way, a thermometer is obtained[1] . These methods represent an industry standard as they are easy to implement in a laboratory – given a correct calibration of the TSEP, this being a delicate procedure – and provide response times compatible with the fast thermal transient of modern devices (e.g., below 100 μs). However, they only allow the measurement of a global temperature value, averaged over the heat source of the device, thus hindering the detection of hotspots [dAl20] and leading to imprecise measurements when multi-chip power circuits are taken into consideration. In addition, the

[1]The sticking point of this calibration phase lies in finding the best trade-off between (1) ensuring that the device is working (that is, it is properly turned on) and (2) that it is only affected by negligible self-heating effects. This is necessary because the thermometer is basically a relationship between the TSEP and T_B+ΔT_j. In the case of non-negligible self-heating, ΔT_j increases and hampers the calibration procedure.

delicate calibration procedure is required before each measurement, since any modifications to boundary conditions and/or electrical connections directly influence the thermometer. Direct methods, on the other hand, rely on optical temperature indicators, such as the variation of IR radiation with temperature: local IR sensors, optical fibers, IR microscopes, and IR cameras [Spi02], [Car03], [Zar10]. These methods allow reconstructing a temperature map of the power device, enabling the localization of current hogging and hotspots. As will be observed in Chapter 5, the surface temperature of a power device is typically nonuniform, with tens of degrees of difference between the hottest and coldest points – i.e., the center and the side of the chip. However, as drawbacks, indirect methods (i) require either visual or mechanical access to the DUT and (ii) are not suitable for fast transient measurements. Table 4.1 summarizes advantages and disadvantages of the abovementioned traditional methods.

Table 4.1. Classification, description, and (dis)advantages of the presented methods for the measurement of Z_{TH} in power devices.

description	main advantages	main disadvantages
Indirect temperature assessment with a calibrated thermometer.	Industry standard, able to detect fast transient responses.	The thermometer must be calibrated before every measurement.
Direct temperature measurement by means of sensors or IR cameras.	Relatively easy procedure, no calibration needed.	Sensors must be placed near the die (or, the top surface of the die must be exposed for IR imaging).
	common disadvantages	
Need for a temperature-controlled environment (i.e., devices are tested in laboratory while placed on a thermochuck). *In-situ* ambient conditions are never taken into account.		

4.2 Extraction procedure

The *in-situ* technique allows characterizing the thermal behavior of power devices in the frequency domain. The role of describing the ther-

mal behavior in the frequency domain is played by the junction-to-ambient power pulse thermal response $Z_{j-a}(f)$, which is the F-transformation of the derivative of the thermal impedance $\mathrm{d}Z_{TH,j-a}(t)/\mathrm{dt}$ [Ger02]. Since this technique is applied with the purpose of obtaining the amplitude/magnitude of the thermal impedance/thermal response, only the magnitude of the quantities of interest will be accounted for. A simple fitting with a Foster thermal network allows converting any $Z(f)$ in the corresponding $Z_{TH}(t)$ and vice-versa. The extraction procedure is described for the specific case of a MOS transistor, yet, mutatis mutandis, it can be simply generalized to other power devices. The drain current I_D can be expressed as a function of the input voltages and devices temperature:

$$I_D = F_{I_D}\left(V_{DS},\ V_{GS},\ T_j\right) \tag{4.1}$$

which in the frequency domain becomes

$$I_D = F_{I_D}\left(V_{DS},\ V_{GS},\ Z_{j-a}\cdot P_D\right) \tag{4.2}$$

Let us consider an operating condition in which V_{GS}=V_{GSdc}, and V_{DS} is given by the superposition of a dc value and a small ac signal (V_{DS}=V_{DSdc}+V_{DSac}); in this case, the V_{DS} derivative of Eq. (4.2) is given by

$$\frac{dI_D}{dV_{DS}} = \left.\frac{\partial F_{I_D}}{\partial V_{DS}}\right|_{T_{jdc}} + \left.\frac{\partial F_{I_D}}{\partial T_j}\right|_{V_{DSdc}} \cdot \frac{dT_j}{dV_{DS}} \tag{4.3}$$

where T_{jdc} is the T_j unaffected by the small signal (i.e., only determined by the dc bias). Let us denote as g_o the magnitude of the frequency-dependent output conductance of the transistor and as $g_{o|T_{jdc}}$ its magnitude at T_j=T_{jdc}.

$$g_o\left(f\right) = \frac{dI_D}{dV_{DS}} \tag{4.4}$$

$$g_o|_{T_{j,dc}} = \left.\frac{\partial F_{I_D}}{\partial V_{DS}}\right|_{T_{jdc}} \tag{4.5}$$

By making use of Eq. (4.4) and Eq. (4.5) in Eq. (4.3), it follows:

$$\frac{dT_j}{dV_{DS}}(f) = \frac{g_o(f) - g_o|_{T_{jdc}}}{\left.\frac{\partial F_{I_D}}{\partial T_j}\right|_{V_{DSdc}}} \tag{4.6}$$

According to the perturbative approach shown in [Mül64]:

$$\begin{aligned} &\tfrac{dP_D}{dV_{DS}}(f) = I_{Ddc} + V_{DSdc} \cdot \tfrac{dI_D}{dV_{DS}}(f) = \\ &= I_{Ddc} + V_{DSdc} \cdot g_o(f) \end{aligned} \tag{4.7}$$

Since $T_j(f)$ and, thus, $\mathrm{d}T_j/\mathrm{d}V_{DS}$ are given by

$$T_j(f) = Z_{j-a}(f) \cdot P_D(f) \tag{4.8}$$

$$\frac{dT_j}{dV_{DS}}(f) = Z_{j-a}(f) \cdot [I_{Ddc} + V_{DSdc} \cdot g_o(f)] \tag{4.9}$$

the following holds true:

$$\begin{aligned} &Z_{j-a}(f) = \tfrac{dT_j}{dV_{DS}}(f) \cdot \tfrac{1}{[I_{Ddc}+V_{DSdc}\cdot g_o(f)]} = \\ &= \frac{g_o(f) - g_o|_{T_{jdc}}}{\left.\frac{\partial F_{I_D}}{\partial T_j}\right|_{V_{DSdc}} \cdot [I_{Ddc}+V_{DSdc}\cdot g_o(f)]} \end{aligned} \tag{4.10}$$

where Eq. (4.6) was exploited. In Eq. (4.10), $Z_{j-a}(f)$ is obtained as a function of:

- the output conductance of the device, $g_o(f)$, that can be measured for each frequency with simple electrical measurements (e.g., by applying sinusoidal waves to the device terminals and measuring $I_{Dac}(t)$ and $V_{DSac}(t)$);
- the output conductance at T_j=T_{jdc}, $g_{o|T_{jdc}}$, which is evaluated by fitting $g_o(f)$ at high frequency values;
- the bias point, i.e., I_{Ddc} and V_{DSdc} – which are well known since they are imposed by the user of the technique;
- the term $\partial F_{I_D}/\partial T_{j|V_{DSdc}}$ that represents an actual thermometer, similar to the one used to calibrate the TSEP in indirect methods. This

term requires demanding and prone-to-errors measurements, specific equipment to test the device at different T_B values, and hinders the extraction of the *in-situ* Z_{j-a}.

Since the last term should be in principle determined with a temperature-controlled environment, Eq. (4.10) is not directly applicable for *in-situ* extractions. To make the $Z_{j-a}(f)$ evaluation only relying on *in-situ* measurements of electrical signals, such a term is simplified as follows. First, Eq. (4.10) is normalized to $Z_{j-a}(0)$, which is the steady-state value of $Z_{j-a}(f)$ and represents the junction-to-ambient thermal resistance ($R_{TH,j-a}$). The normalized junction-to-ambient power pulse thermal response $z_{j-a}(f)$ is given by

$$z_{j-a}(f) = \frac{Z_{j-a}(f)}{Z_{j-a}(0)} = \frac{g_o(f) - g_o|_{T_{jdc}}}{g_o(0) - g_o|_{T_{jdc}}} \cdot \frac{I_{Ddc} + V_{DSdc} \cdot g_o(0)}{I_{Ddc} + V_{DSdc} \cdot g_o(f)} \tag{4.11}$$

where $g_o(0)$ is the measured value at f=0 Hz.

4.2.1 Measuring $g_{o|T_{jdc}}$ and $g_o(0)$

Electrical and thermal transients are characterized by very different time-/frequency-domain evolutions. The thermal transient is generally slower than the electrical one, with a difference of several order of magnitudes in their respective time constants. The same also applies to the frequency domain, as represented in Figure 4.1. It is possible to identify a thermal cut-off frequency (f_τ) above which the temperature of the device does not follow the sinusoidal $P_D(f)$ anymore. At $f<f_\tau$, the device behavior – and, thus, $g_o(f)$ – is influenced by both ac and dc heating; at $f>f_\tau$, on the other hand, the temperature of the device is only determined by the dc bias.

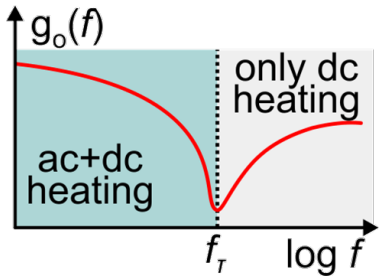

Figure 4.1. Schematic representation of the output conductance g_o as a function of the frequency f. The cyan (grey) box defines the frequency range below (above) the thermal cut-off frequency f_τ, where the device is affected by ac+dc (dc) heating.

As shown in [Sah10], the measurement of $g_{o|T_{jdc}}$ can be performed at $f>f_\tau$, where ΔT_{jac}=0 K, that is, T=T_{jdc}. Then, values at $f<f_\tau$ are extrapolated as depicted in Figure 4.2.

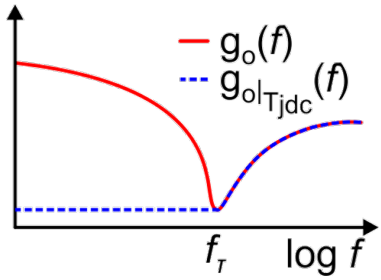

Figure 4.2. Schematic representation of g_o (solid red line) and $g_{o|T_{jdc}}$ (dashed blue line) as a function of the frequency f; g_o and $g_{o|T_{jdc}}$ coincide for $f>f_\tau$, while $g_{o|T_{jdc}}$ values at $f<f_\tau$ are obtained by extrapolation.

As far as $g_o(0)$ is concerned, it is evaluated as a derivative from dc measurements. More specifically, the device is biased with V_{DSdc} and V_{GSdc}, and I_{Ddc} is measured; then, Eq. (4.4) is applied in the surroundings of the bias point chosen for the investigation, thus obtaining $g_o(0)$.

4.3 De-normalization procedure

Once $z_{j-a}(f)$ is extracted, the corresponding $Z_{j-a}(f)$ can be evaluated through a de-normalization procedure, which makes use either of (i) the junction-to-case power pulse thermal response $Z_{j-c}(f)$ (i.e., the $Z(f)$ of the device not embedded in the assembly) taken from the device datasheet or (ii) the junction-to-board power pulse thermal response $Z_{j-b}(f)$ (i.e., the $Z(f)$ of the device embedded in the assembly and positioned on a thermochuck, fixing the temperature of the backside to 300 K). Figure 4.3 schematically depicts this procedure. First, a high-frequency matching range is identified, where the $Z_{j-c}(f)$ or $Z_{j-b}(f)$ (known) and $Z_{j-a}(f)$ (to be determined) coincide, as the heat is still confined in the device region. As shown in [Ren02] and [Des17], the heat emerging from the device does not instantly reach every region of the assembly; instead, at shortly after t=0 s (or, alternatively, at very high f values), the heat is still confined in the surroundings of the heat source. Depending on the thermal time constants of the layers composing the system, the heat starts flowing out of the die area and reaches the boundaries of the domain. The de-normalization procedure takes advantage of this piece of information: the thermal transients of the die and of the system in which the die is embedded coincide at very high frequencies – or, again, at very low times – since the heat has still not exited from the active region, that is, the surroundings of the heat source. Subsequently, $R_{TH,j-a}$=$Z_{j-a}(0)$ (or $R_{TH,j-b}$=$Z_{j-b}(0)$) is tuned to make $Z_{j-a}(f)$=$R_{TH,j-a}$·$z_{j-a}(f)$ coincide with $Z_{j-c}(f)$ in the matching range. Finally, $Z_{TH,j-a}(t)$ is obtained by fitting $Z_{j-a}(f)$ with a Foster network and computing its power step response.

It is worth highlighting that, although the presented technique offers the unique advantage of extracting the *in-situ* $Z_{TH,j-a}$, it requires:

- preliminary information about the thermal behavior of the device ($Z_{j-c}(f)$) or about the assembly when placed on a thermochuck ($Z_{j-b}(f)$);
- medium-to-long measurement sessions, depending on the features of the assembly under investigation.

The first requirement is needed in the de-normalization procedure; the second one is strongly related to the thermal behavior of the assembly.

For a generic PM with a thick Cu baseplate – introducing a high thermal capacitance that in turn delays the thermal response of devices embedded therein – frequencies as low as 10 mHz need to be investigated. Of course, the time constants are faster in lighter assemblies; the duration of the experiment may fall in the range of 10-30 mins. At the same time, in heavier assemblies (e.g., equipped with extra-large passive cooling systems), the whole experiment may last more than 2 h. Table 4.2 summarizes the presented *in-situ* technique, highlighting both its advantages and disadvantages.

4.4 Measurement setup

The measurement circuit sketched in Figure 4.4 is devoted to the extraction of g_o *vs.* frequency by operating in the time domain. The circuit requires:

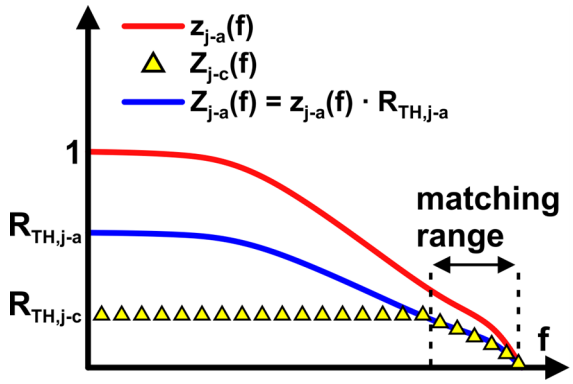

Figure 4.3. Schematic representation of the de-normalization process: the $R_{TH,j-a}$ value is tuned to overlap $Z_{j-a}(f)$ (solid blue line) and $Z_{j-c}(f)$ (yellow triangles) in the high-frequency matching range; $z_{j-a}(f)$ is also shown (solid red line). In this case, $R_{TH,j-a}$ was supposed to be lower than 1 K/W; however, the same procedure still holds true for $R_{TH,j-a}$>1 K/W.

- two voltage supplies (i.e., V_{GGdc} and V_{DDdc}) making the transistor work at the desired bias point, that is, V_{DSdc} and I_{Ddc};
- a voltage generator (V_{DDac}) applying a small-signal piecewise sinu-

soidal waveform;

- two voltage probes and a shunt resistor (R_{shunt}) allowing the sensing of $V_{DS}(t)$ and $I_D(t)$.

Table 4.2. Description and (dis)advantages of the *in-situ* technique for the measurement of Z_{TH} in power devices.

description	main advantages	main disadvantages
Indirect temperature assessment with purely-electrical measurements.	Able to measure the *in-situ* $Z_{TH,j-a}$. No need for a temperature-controlled environment nor for a calibration.	Need for information on the device $Z_{j-c}(f)$ or $Z_{j-b}(f)$, taken from datasheets or traditional measurements. Medium-to-long measurement sessions.

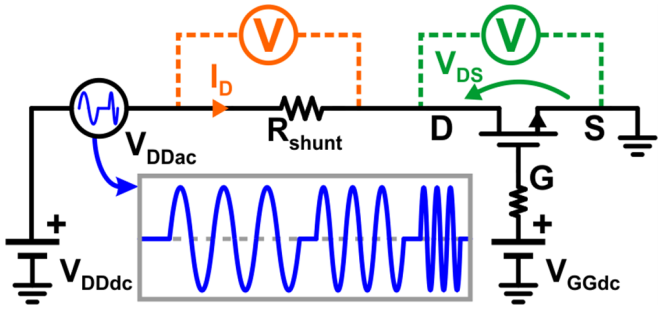

Figure 4.4. Circuit conceived to perform the measurements of the electrical signals $V_{DS}(t)$ and $I_D(t)$. The gray box shows the small-signal piecewise sinusoidal waveform (solid blue line).

For each frequency, the evaluation of g_o is performed according to the following equation:

$$g_o = \frac{RMS\left(I_D\left(t\right) - I_{Ddc}\right)}{RMS\left(V_{DS}\left(t\right) - V_{DSdc}\right)} = \frac{RMS\left(I_{Dac}\left(t\right)\right)}{RMS\left(V_{DSac}\left(t\right)\right)} \tag{4.12}$$

where RMS stands for root mean square. Between each frequency, a rest time was introduced to avoid interferences between sinusoidal transients at consecutive frequencies[2]. A rest time of 2 s was chosen, which was sufficient to let the temperature reach its steady-state value (i.e., ΔT_{jdc}) again, after the ET transient. Observing Figures 4.5 and 4.6, reporting the time evolution of $\Delta T_j(t)$ of a SiC power MOSFET (coinciding with the devices adopted in Chapter 3), it is possible to infer that:

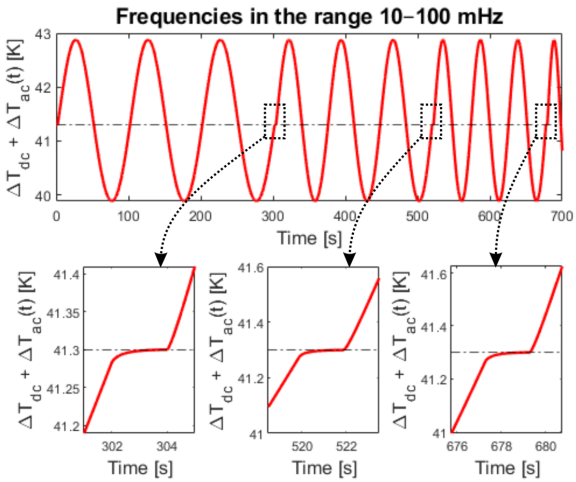

Figure 4.5. (top) Temperature increment ΔT_{jdc}+$\Delta T_{jac}(t)$ *vs.* time induced by V_{DSdc}+V_{DSac} in the 10–100 mHz range; (bottom) magnification of the 2-second rest time between consecutive frequencies.

[2]It is worth highlighting that measurements only start when the device has reached the ET steady-state conditions at ΔT_j=ΔT_{jdc} after the bias (V_{DSdc}, I_{Ddc}) has been applied; moreover, a small-signal piecewise sinusoidal voltage $V_{DSac}(t)$ is superimposed to V_{DSdc}. The rest time between two consecutive frequencies was introduced to prevent the ET transient induced by the f=f_1 sinusoid from interfering with the measurement of output conductance go at f_2, where f_2>f_1. As already highlighted in Section 4.2.1, the electrical transient is faster than the thermal one, with a difference of several order of magnitudes in the time constants. For this reason, the critical quantity to consider in order to prevent transients overlap is ΔT_j: the interference between the dynamic thermal responses of two consecutive frequencies has to be avoided.

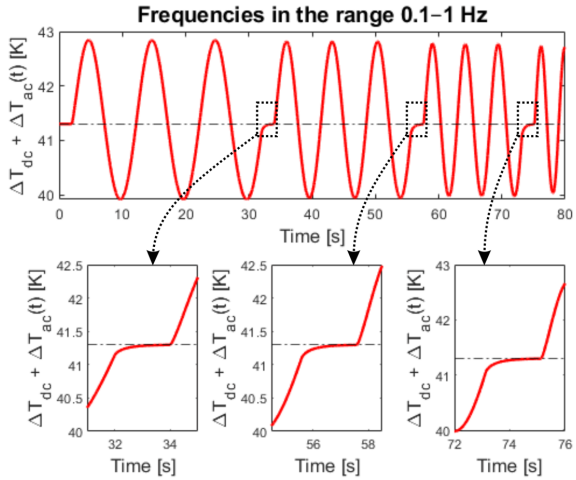

Figure 4.6. (top) Temperature increment ΔT_{jdc}+$\Delta T_{jac}(t)$ *vs.* time induced by V_{DSdc}+V_{DSac} in the 0.1–1 Hz range; (bottom) magnification of the 2-second rest time between consecutive frequencies.

- As the rest time is approaching, the device temperature is already close to its steady-state value ΔT_{jdc} (i.e., ΔT_{jac}≈0 K); this is due (i) to the inherent nature of the sinusoidal stimulus leading the device temperature to swing/oscillate around ΔT_{jdc}, and (ii) to the piece-wise sinusoidal signal ending after 3 full periods.

- Well before the end of the rest time, ΔT_{jac} reaches 0 K; hence, a rest time of 2 s represents a prudent choice.

- The rest time is compatible with the order of magnitude of the thermal time constant of the assembly under investigation (see [Cat20] for insights into thermal time constants). Actually, the thermal time constant of the assembly cannot be known a-priori since the Z_{TH} is the quantity to be measured; nonetheless, as a rule of the thumb, an approximate guess of the expected thermal time constant can be made considering the assembly and the cooling system, and the rest time can be chosen in the same order of magnitude. As an alternative way to quantify the thermal time constant, it is possible to perform its preliminary estimation by stimulating the DUT with an

electrical bias at t=0 s and waiting for an electrical signal (e.g., I_D, V_{DS}) to reach its steady-state value[3].

4.5 Case-study #1: multi-chip SiC-based PM

The 'simulated experiments' strategy ([Rus09], [Cat21]) was applied to one of the SiC-based VDMOS transistors embedded into the PM detailed in Chapter 3 and it was articulated as follows:

- First, the reference $Z_{TH,j-a}$ of the device was obtained through a dynamic thermal analysis on the exact replica of the PM (Figure 3.6). In the FEM simulations, h was set to $2{\times}10^3$ W/$m^2 \cdot K$ and it was applied to the bottom surface of the thick Cu baseplate, which emulates the contact with an efficient heat-sink [Cat20].
- The obtained reference $Z_{TH,j-a}$ was used to build a SPICE-compatible TFN with a Foster topology [Jak90]; the TFN was then coupled to the electrical model of the VDMOS transistor. The electrical model was calibrated on experimental data [Ric18] and is thoroughly described in [dAl20].
- Transient simulations were conducted in the OrCAD Capture software package [SPI11] on the ET model to emulate the experimental procedure presented in Section 4.2 to extract the $z_{j-a}(f)$.
- The de-normalization process and the time domain conversion were then carried out to obtain the thermal impedance $Z_{TH,j-a}(t)$.
- The reference and extracted $Z_{TH,j-a}$s were finally compared.

About the electrical circuit, the device was biased with V_{DDdc}=15 V, V_{GGdc}=10 V, and R_{shunt}=200 mΩ. For the given bias point, a preliminary investigation allowed observing that nonlinear thermal effects do not play a relevant role in defining the dynamic response of the assembly. The DUT is biased by the measurement circuit; the bias point leads to a temperature increment ΔT_{jdc}, which could in principle entail a reduction in

[3]More specifically, considering two consecutive times t_1 and t_2 and an arbitrarily small quantity ε, when $|I_D(t_2) - I_D(t_1)| < \varepsilon$ then t_2 can be considered as the time required to reach the ET steady-state with a reasonable degree of accuracy.

the thermal conductivities of materials – as detailed in Section 2.1.1. On the other hand, the superimposed small-signal sinusoidal waveforms lead to a negligible variation in the temperature slightly oscillating around ΔT_{jdc}. In short, nonlinear thermal effect can be considered as solely activated by the bias (dc) conditions. As shown in Figure 4.7, indeed, the steady-state thermal behavior is not significantly influenced by nonlinear thermal effects, and even less for the considered P_D bias value. At P_D=117 W, the mismatch between linear and nonlinear ΔT_{jdc}s turns out to be lower than 1.5%. However, more in general, if the bias point (representative of the operating conditions) and T_B lead to perceptible nonlinear thermal effects, then the device ET steady-state will inherently account for them. Consequently, the extracted thermal impedance $Z_{TH,j-a}(t)$ will be influenced by the thermally-induced k degradation as well.

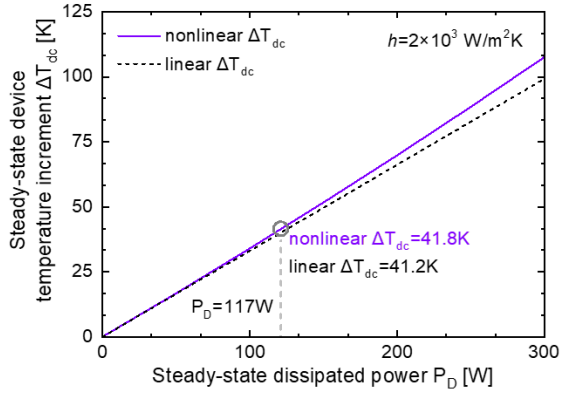

Figure 4.7. Steady-state analysis showing the temperature increment ΔT_{jdc} *vs.* dissipated power P_D in the PM under investigation obtained by linear (dashed curve) and nonlinear (solid) FEM simulations.

Concerning the piecewise waveform, 3-period sinusoids were adopted for each frequency. The logarithmically-spaced frequency range was 3 mHz–20 kHz with six points per decade. The V_{DDac} waveform was ∼1 hour long, while its amplitude was set at 0.5 V. The large thermal time constants introduced by the thick Cu baseplate led to a relatively long duration of the experiment, this being the main drawback of the *in-situ* characterization of the assembly under analysis. The I_D and V_{DS} *vs.*

time waveforms were computed according to Eq. (4.12), and $z_{j-a}(f)$ was extracted through Eq. (4.11). Results are shown in Figure 4.8, where the reference and extracted $z_{j-a}(f)$ are compared. An excellent agreement was achieved: considering the percentage mean-square error as a figure of merit, the mismatch between the two curves in the high-frequency matching range turned out to be 1.72%, while 0.34% was the discrepancy in the overall frequency range. The de-normalization process discussed in Section 4.3 was then applied. Given the geometrical information of the die, the device dynamic thermal response was numerically computed so as to obtain the $Z_{TH,j-c}(t)$.

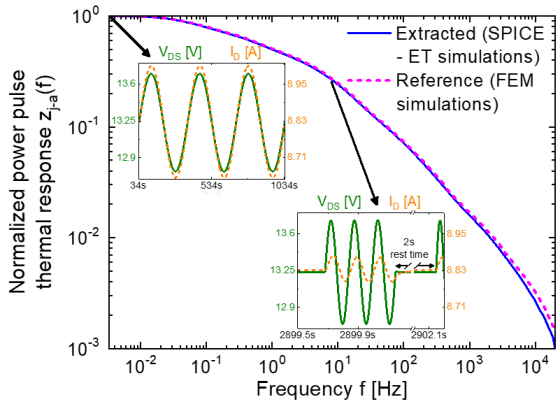

Figure 4.8. Comparison between extracted (solid blue line) and reference (dashed magenta) $z_{j-a}(f)$. Also reported are the V_{DS} (solid green line) and I_D (dashed orange) *vs.* time waveforms at f=3 mHz and f=6 Hz (top-left and bottom-right insets, respectively).

Results are shown in Figure 4.9; $R_{TH,j-a}$=0.35 K/W (to be compared with the reference $R_{TH,j-a}$=0.354 K/W) was found as the tuning value to overlap the curves in the 3–20 kHz matching range. Figure 4.9 witnesses the agreement between the extracted and reference thermal responses $Z_{j-a}(f)$ and impedances $Z_{TH,j-a}(t)$.

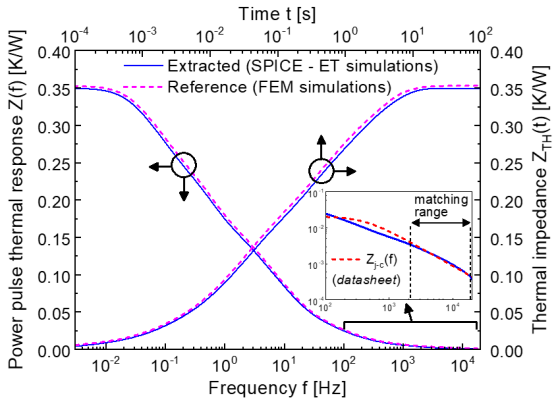

Figure 4.9. (bottom-left axes) comparison between extracted (solid blue line) and reference (dashed magenta) $Z_{j-a}(f)$. The inset (bottom-right corner) highlights the matching range and the overlap between $Z_{j-a}(f)$ and $Z_{j-c}(f)$ (yellow triangles). (top-right axes) comparison between extracted and reference $Z_{TH,j-a}(t)$.

4.6 Case-study #2: PCB-integrated GaN-based power circuit

The *in-situ* extraction technique was also validated against the $Z_{TH,j-a}$ of a GaN power HEMT manufactured by EPC [EPC] and inspired to the 2016C product (BV_{DS}=100 V, max I_D=18 A, R_{DSon}=16 mΩ) shown in Figure 4.10.

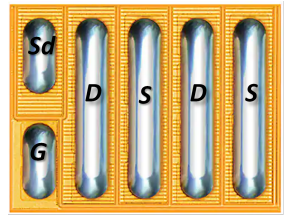

Figure 4.10. Picture of the GaN power HEMT chip used as case-study. Terminals are highlighted: gate (G), drive-source (Sd), drain (D), and source (S). The lateral dimensions are 2.1×1.6 mm^2.

First, the electrical model provided by EPC was enhanced in order to be included in the fully-circuital ET simulations; then, it was calibrated on experimental data extracted by the device datasheet [EPC16], as shown in Figures 4.11, 4.12, and 4.13. A Cauer network of a PCB-integrated assembly was extracted by means of thermal simulations in the COMSOL Multiphysics environment, according to the methodology shown in Chapter 2. Such TFN – characterizing the response of the assembly without the chip – was attached to the one provided by the company – describing the thermal behavior of the chip and provided by the manufacturing company. The *in-situ* extraction was finally emulated in the SPICE environment and the 'simulated experiments' strategy detailed in Section 4.5 was adopted. By considering the measurement circuit shown in Figure 4.4, the device was biased with V_{DDdc}=7 V, V_{GGdc}=1.8 V, and R_{shunt}=100 mΩ; $g_o(f)$ was measured according to Eq. (4.12). The logarithmically-spaced frequency range was 10 mHz–10 kHz with ten points per decade, and the ET simulation of 2.5 h lasted 30 mins on a normal PC. Results are shown in Figure 4.14, where the normalized reference and extracted Z_{j-a}s are compared.

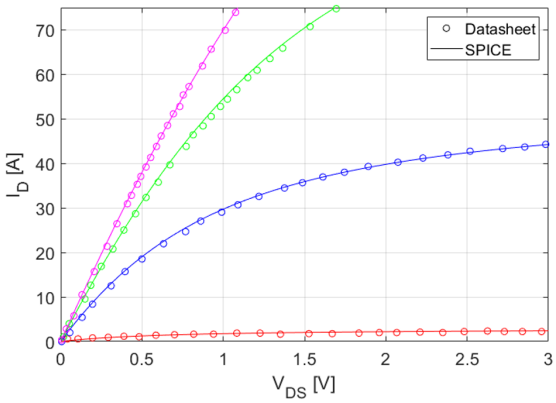

Figure 4.11. Validation of the electrical model provided by EPC and enhanced with ET capabilities: datasheet measurement points (circles) and SPICE results of I_D *vs.* V_{DS} characteristics at different V_{GS} values.

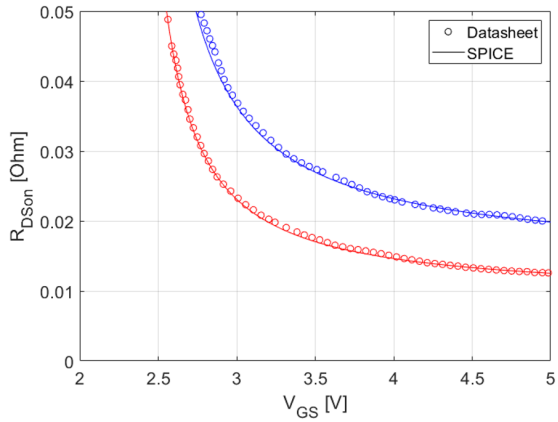

Figure 4.12. Validation of the electrical model provided by EPC and enhanced with ET capabilities: datasheet measurement points (circles) and SPICE results of R_{DSon} *vs.* V_{GS} at T=25°C (red curves) and 125°C (blue curves).

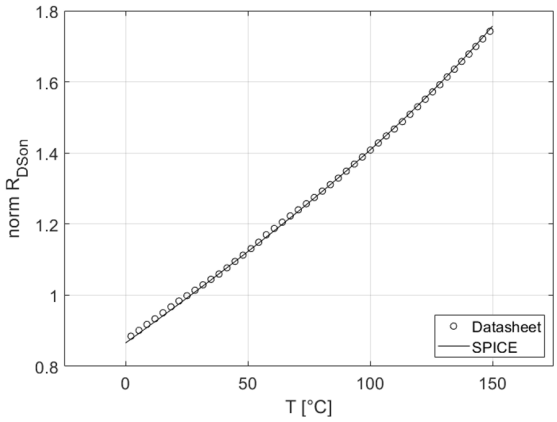

Figure 4.13. Validation of the electrical model provided by EPC and enhanced with ET capabilities: datasheet measurement points (circles) and SPICE results of the normalized R_{DSon} *vs.* T at V_{GS}=5 V and I_D=11 A.

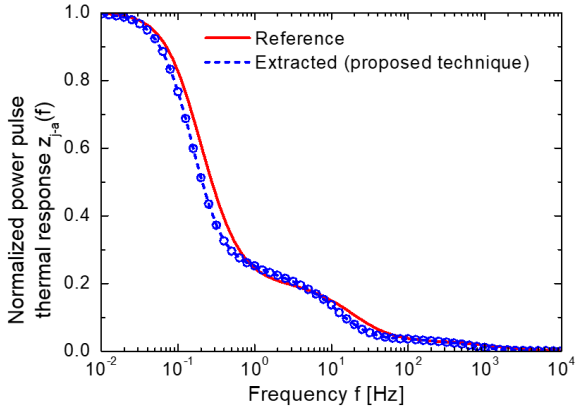

Figure 4.14. Comparison between reference (solid red line) and extracted (dashed blue) $z_{j-a}(f)$. For each point of the extracted curve, measurements according to Eq. (4.12) were performed by using the circuit depicted in Figure 4.4.

In this case, the de-normalization procedure was carried out by making use of the information provided by the company, that is, $Z_{TH,j-b}$. Figure 4.15 summarizes the procedure, also providing further insights into the scaling and showing the outcome of incorrect de-normalizations. Results after the de-normalization are shown in Figure 4.16, both in the time and frequency domains.

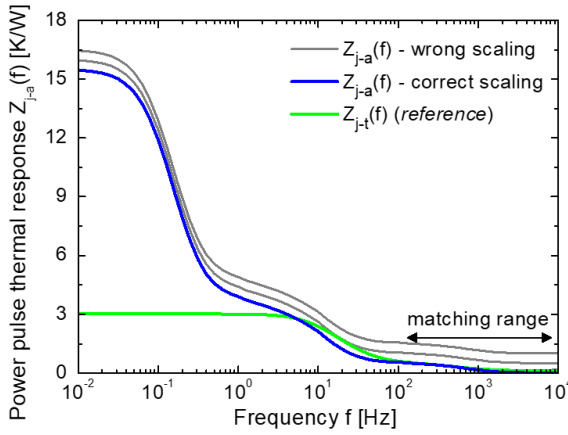

Figure 4.15. Schematic representation of the de-normalization process: a matching range is identified at high frequency values, and the $R_{TH,j-a}$ value is tuned to overlap $Z_{j-t}(f)$ (solid green line) and $Z_{j-a}(f)$ (blue) in such range. Wrongly scaled $Z_{j-a}(f)$ (grey) are also reported: if a wrong value of $R_{TH,j-a}$ is chosen, the mismatch in the high-frequency range leads to an overall error in the de-normalization.

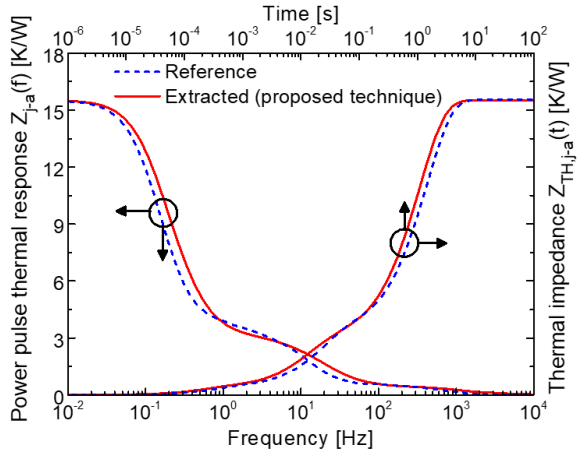

Figure 4.16. (bottom-left axes) comparison between extracted (solid red line) and reference (dashed blue) $Z_{j-a}(f)$. The transformation of the frequency domain $Z_{j-a}(f)$ into the time domain $Z_{TH}(t)$ was performed through a simple fitting, that is, a Foster thermal network was extracted.

4.7 Summary

This Chapter presents an innovative technique allowing the measurement of the overall junction-to-ambient Z_{TH}s of power devices mounted in a generic assembly and working under any environmental condition (*in-situ* extraction). The technique is applicable to any power semiconductor device without the need for temperature sensing; it only relies on the measurement of electrical signals and requires the knowledge of the junction-to-case Z_{TH} of individual devices (i.e., not embedded in the assembly). The Z_{TH} extraction process can take from tens of minutes to few hours, depending on how slow the dynamic thermal response of the assembly is. Since traditional methods do not allow *in-situ* measurements, their accuracy could be compared with the proposed technique one; therefore, an unambiguous and successful validation of the technique has been performed through the 'simulated experiments' strategy applied to two case-studies. First, the thermal behavior of a SiC-based VDMOS transistor embedded in a state-of-the-art multi-chip PM has been considered as a case-study; then, a PCB-integrated GaN-based power circuit was taken into account. ET simulations in a SPICE-like software package have been used to emulate the measurement setup and apply the proposed technique. Results have demonstrated an excellent assessment of the $Z_{TH}(t)$ in both cases. Therefore, this technique proposes itself as a valid solution for the *in-situ* thermal characterization of power devices, regardless of (i) their technology and (ii) the assembly they are embedded into.

Chapter 5

Multicellular ET simulation of a SiC power MOSFET

In this Chapter, an innovative approach for the TFN-based ET simulation of a single device is proposed. The DUT is subdivided into a number of individual cells, which represents a challenging task from the computational point of view. The aim of the approach is to optimize the trade-off between computational efficiency and accuracy when handling problems with a relatively large amount of heat sources. The approach relies on a fully-circuital representation of the whole device, wherein the TFN is obtained by invoking the MOR-based FANTASTIC tool [Cod14]. FANTASTIC is fed with a detailed 3-D representation of the DUT and provides TFNs without the need for dynamic thermal simulations in the pre-processing stage. Such TFNs improve those exploited in [dAl13], [dAl14] based on Foster networks extracted in a rather long pre-processing stage from transient FEM simulations of the DUT. As a case-study, a 4H-SiC power MOSFET was operated under dc, short-circuit (SC), and unclamped inductive switching (UIS) conditions.

5.1 ET simulation approach

The approach can be summarized as follows.

- The whole DUT is subdivided into an assigned number N of elementary cells, high enough to identify potentially-dangerous tempera-

ture gradients over the transistor active area, but not too high to prevent intolerably long CPU times or impossible memory storage. The schematic representation of an individual cell is provided in Figure 5.1, while Figure 5.2 shows the device subdivided into 79 cells.

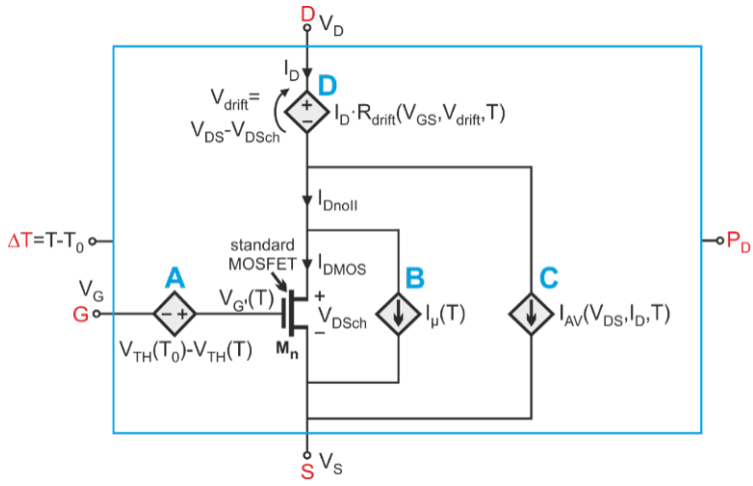

Figure 5.1. Sketch of the SPICE-compatible subcircuit for the transistor cell.

- Each cell is represented with a SPICE-compatible subcircuit implementing the above model through a macromodeling technique. It makes use of (i) a standard MOSFET at the reference temperature T_0=300 K as a "main" component to describe the channel region, and (ii) linear and nonlinear controlled sources to include all the model features that cannot be accounted for with the basic MOSFET, i.e., the temperature dependence of the threshold voltage V_{TH} and of the current factor K, the bias- and temperature-dependent drift resistance R_{drift}, as well as the bias- and temperature-dependent avalanching phenomenon. Besides the standard electrical terminals (gate, drain, source/body), the cell subcircuit is also equipped with an input node carrying the "voltage" ΔT (provided by the TFN introduced below), and with an output node offering the "current" P_D (to be fed to the TFN).

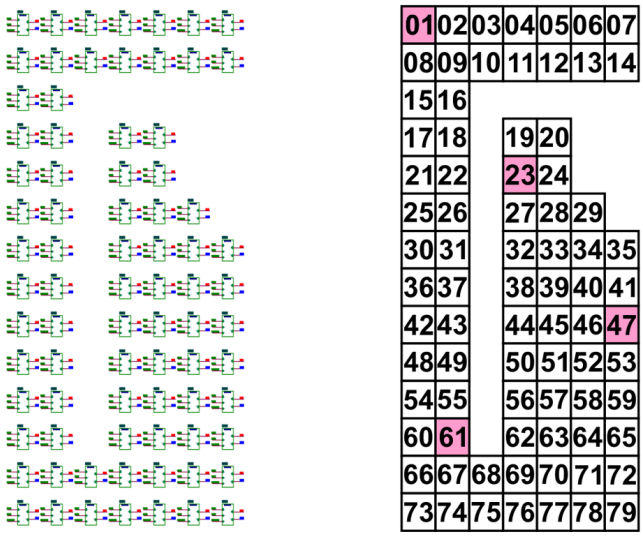

Figure 5.2. Discretization of the effective active area of half DUT: (left) PSPICE subcircuit with hierarchical blocks associated to the transistor cells; (right) cell numbering, with evidenced cells of interest for the ET analysis presented in this Chapter.

- The TFN is automatically constructed by invoking the FANTASTIC tool (based on a MOR approach, Section 2.2.2), which receives as an input the 3-D FEM representation of the DUT, with information about (i) the discretization into elementary cells (each of which corresponds to an individual heat source), (ii) material parameters, and (iii) BCs. All the mutual interactions among heat sources are accurately modeled.

- It must be remarked that the TFN describes the linear thermal problem; however, nonlinear thermal effects can be significant if the DUT is simulated under harsh conditions entailing high temperatures. In order to tackle this issue, a properly-tuned Kirchhoff's transformation [Joy75] was exploited, as described in Section 2.3.

- The cell subcircuits are then connected to the TFN in a commercial circuit simulation tool (like PSPICE, LTSPICE, Eldo, ADS, SIMetrix); as a result, the whole multicellular DUT is transformed

into a purely-electrical macrocircuit, which suitably accounts for ET effects. The solution of this macrocircuit under both steady-state and dynamic conditions is demanded to the robust engine of the circuit simulation tool, with very low computational effort and minimized occurrence of convergence issues compared to other numerical methods.

5.2 FEM representation of the DUT

The DUT was assumed to be soldered on an SSC PM, similar to the one described in Chapter 3. The device lies on a DBC substrate by means of a 50 μm-thick tin-platinum alloy layer ensuring both mechanical joint and electrical connection with the drain. Figures 5.3 and 5.4 show the top view and cross-section of the assembly, which enjoys the same symmetry of the DUT.

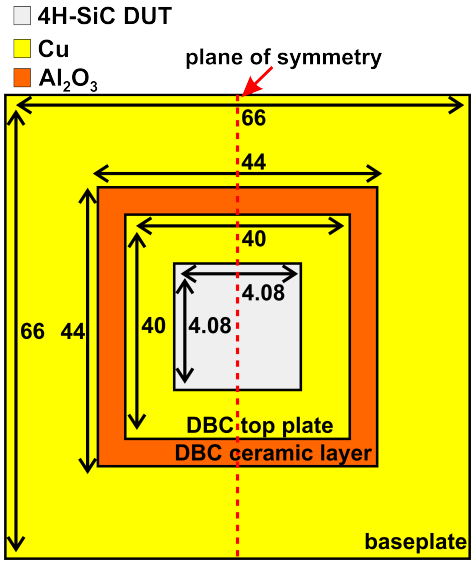

Figure 5.3. Sketch of the top-view (not to scale) of the domain to be ET simulated; all dimensions are expressed in mm.

The drain contact of the DUT is soldered on the top plate, while the bottom plate ensures a good thermal interface with the 3 mm-thick Cu

baseplate. The 3-D domain (Figure 5.5) was built in COMSOL Multiphysics as described in Section 2.2. The number of tetrahedra and degrees of freedom of the resulting grid are 3.8×10^5 and 5.2×10^5, respectively. Figure 5.6 plainly illustrates that the mesh is highly-fine over the die, while becoming gradually coarser by moving far away from the active region.

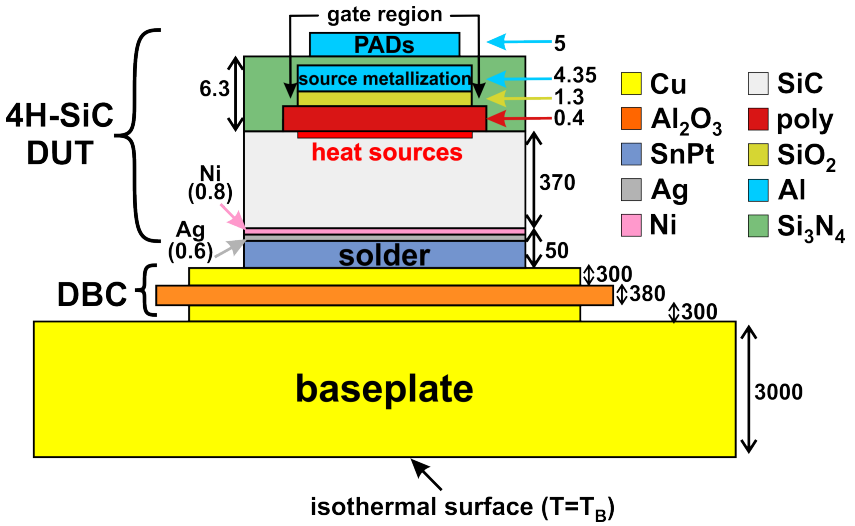

Figure 5.4. Sketch of the cross-section (not to scale) of the domain to be electrothermally simulated; all dimensions are expressed in μm.

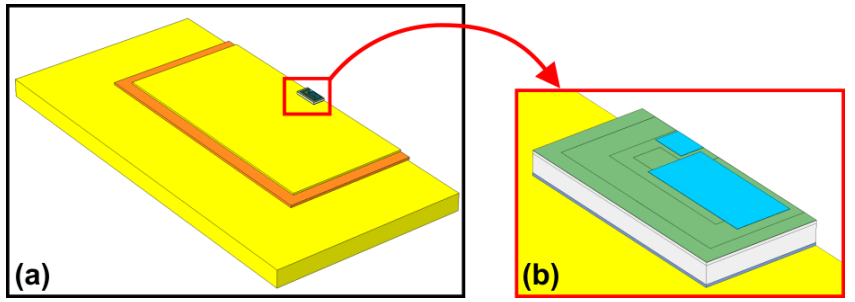

Figure 5.5. 3-D representation of the geometry of the domain under test in the COMSOL Multiphysics environment (*draw mode*); (a) whole structure and (b) magnification of the 4H-SiC VDMOS die.

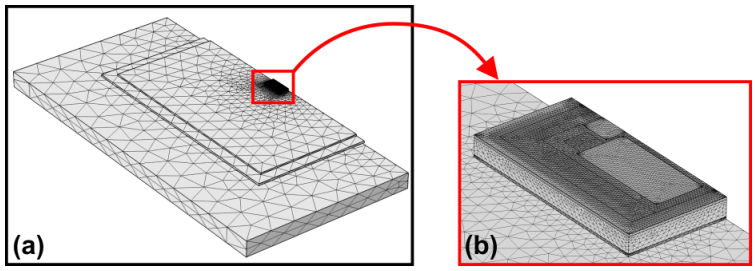

Figure 5.6. 3-D tetrahedral mesh of the domain under test in the COMSOL Multiphysics environment (*grid mode*); (a) whole structure and (b) magnification of the 4H-SiC die.

5.3 Construction of the DUT macrocircuit

The macrocircuit representing the ET behavior of the packaged DUT was constructed in the PSPICE environment as follows. The TFN, provided in the form of a netlist, was enriched with N nonlinear voltage-controlled voltage sources to account for Kirchhoff's transformation. Then the ΔT and P_D nodes of the subcircuits (the individual transistor cells) were connected to the Kirchhoff-equipped TFN. All the gate terminals of the subcircuits were shorted together, as well as the drain and source ones. It is possible to activate an electrical network to include the de-biasing over the source metallization. A simplified scheme of the adopted strategy is shown in Figure 5.7.

5.4 Steady-state and dynamic ET simulations

The macrocircuit was adopted to perform many PSPICE simulations of the DUT in both steady-state (dc) and dynamic conditions on a PC with an Intel Core i7-7700 (3.60 GHz) CPU and equipped with a 16 GB RAM. First, the I_D–V_{DS} output characteristics were determined with a V_{DS} step amounting to 0.1 V under isothermal (at T_0) and ET conditions. Isothermal conditions were obtained by deactivating the FANTASTIC-based TFN. The CPU time needed to simulate a single ET characteristic was nearly 100 s. Results are reported in Figure 5.8, which also shows the ΔT averaged over the effective active area (ΔT_{av}). It can be inferred that

the simulation runs were stopped as ΔT_{av} reached 500 K.

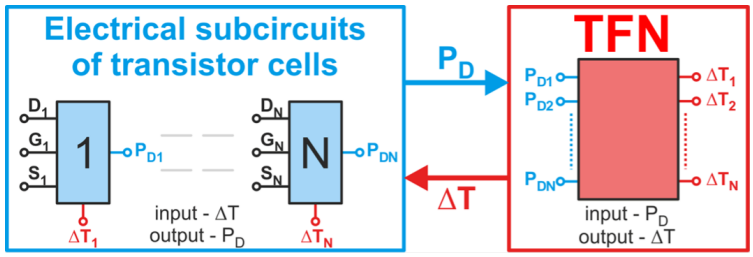

Figure 5.7. Schematic representation of the proposed strategy to perform a fully coupled ET analysis in a circuit simulation tool; the feedback loop between the electrical circuit (left) and the TFN (right) relying on the electrical equivalent circuit is highlighted (the voltage sources for Kirchhoff's transformation are omitted).

Afterward, SC tests were simulated. Such tests are typically used to quantify the device robustness under harsh and abnormal events, and involve large power dissipation (see e.g., [Cas12], [Hua13], [dAl14], [Ngu15], [Rom15], all focused on SiC MOSFETs). It must be remarked that the knowledge of the whole temperature distribution is important, since the value and position of the temperature peak are needed for reliability considerations. Various combinations of gate and supply voltages were applied. A gate resistance of 50 Ω was considered. The simulation of a single test required about 300 s with a fine time discretization. The total drain current I_D conducted by the DUT *vs.* time is shown in Figure 5.9a for all the analyzed cases, while Figure 5.9b illustrates the temperature rises ΔT_{av}. The first figure reveals that I_D first grows due to the positive temperature coefficient induced (i) by the reduction in threshold voltage and (ii) by the mobility increase (for the lowered Coulomb scattering), and then decreases since the negative temperature coefficient triggered by the acoustic-phonon scattering dominates [dAl14]. The temperature rises ΔT over cells #1, #23, #47, #61 (identified in the layout of Figure 5.2) are reported in Figure 5.9c for two cases, namely, V_{GS}=10 V/V_{DD}=200 V and V_{GS}=20 V/V_{DD}=200 V. From the inspection of the waveforms, it is found that an uneven temperature distribution takes place in the first case, where the milder bias conditions allowed the device to undergo the test for a longer period, within which the heat had enough time to signifi-

cantly spread; consequently, the mutual thermal interactions play a more relevant role, and favor a nonuniform temperature field.

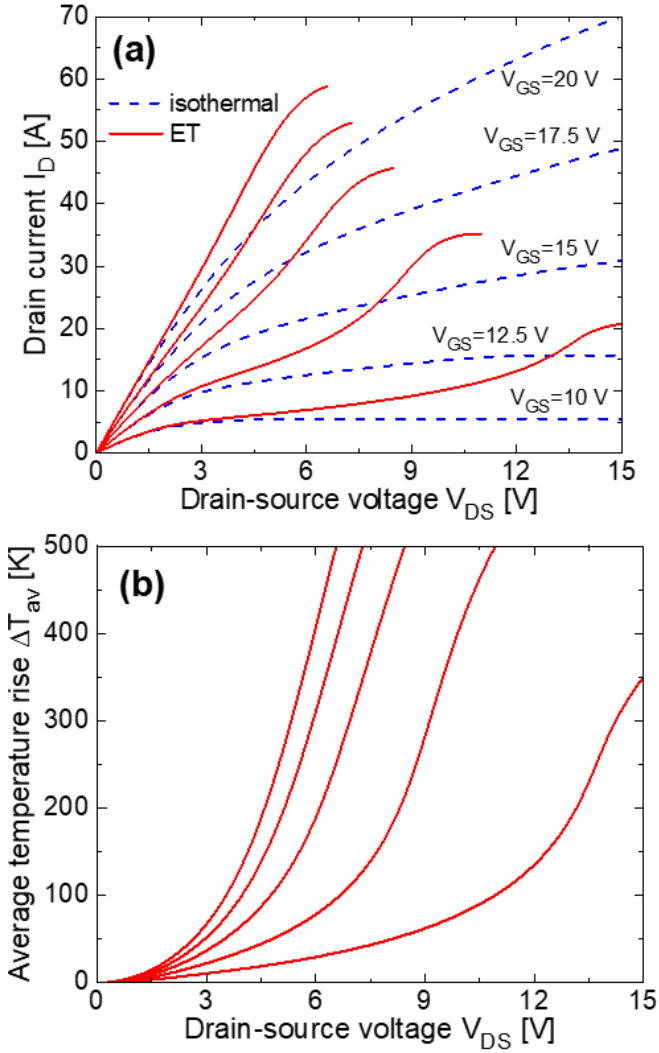

Figure 5.8. (a) I_D–V_{DS} output characteristics determined with the proposed approach under isothermal (dashed blue lines) and ET (solid red) conditions; (b) temperature rise ΔT_{av}=T_{av}-T_0 corresponding to the ET conditions, T_{av} being the temperature averaged over the whole effective active area.

The TFN generated with FANTASTIC, aided by a code accounting for Kirchhoff's transformation, enables the reconstruction of the whole temperature distribution in the packaged DUT at chosen time instants. This is a key option offered to designers, as the inspection of selected thermal maps represents a valuable support to estimate the PM reliability. More specifically, points A, B, C identified in Figure 5.9a and Figure 5.9b were selected, which approximately share the same ΔT_{av} value, i.e., 500 K. The computed temperature rise maps are shown in Figure 5.9d (top view) and Figure 5.9e (side view). As can be seen, despite the same ΔT_{av},

- point A, which falls at a time instant close to the beginning of the test, exhibits a uniform and superficial temperature field, since the heat is still confined in the top active region close to the generation area;

- the temperature distributions in B and C are increasingly uneven, which is again ascribable to the much longer stress times. In particular, C suffers from a severe temperature focusing over the innermost DUT area, and – as witnessed by the side view – the downward heat had enough time to reach and hit the DBC.

Lastly, the macrocircuit was used to simulate an UIS test. A gate voltage equal to 20 V was applied for 200 μs, and then was lowered to 0. The supply voltage was V_{DD}=150 V, while the inductance L was 2.3 mH. Again, the time elapsed by PSPICE for a single UIS test was about 300 s. Figure 5.10a shows the drain current I_D and the drain-source voltage V_{DS} *vs.* time in the span 190 μs to 230 μs, while Figure 5.10b illustrates the temperature rises of cells #1, #23, #47, #61. The temperature distribution was found to be almost uniform, as witnessed by the map taken at time instant t^*=210 μs where the dynamic average temperature peaks (Figure 5.10c).

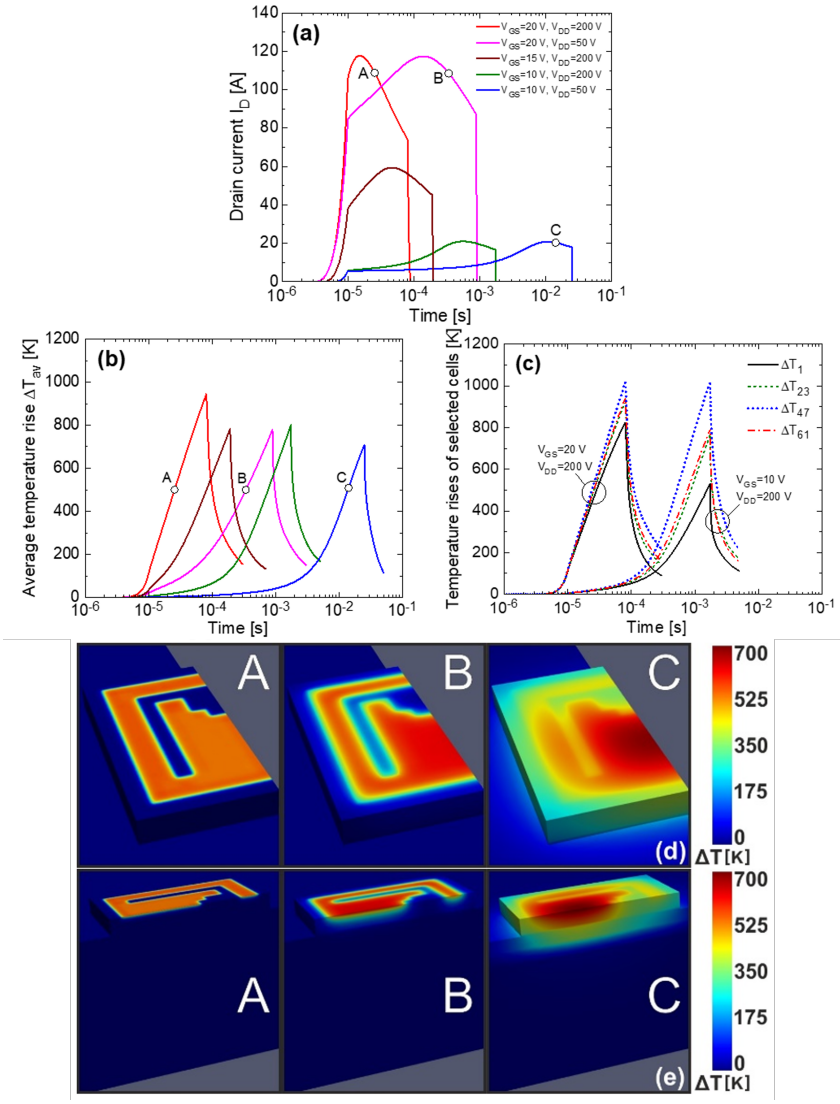

Figure 5.9. SC test: (a) drain current I_D *vs.* time for 5 cases; (b) corresponding temperature rises averaged over the effective active area; (c) temperature rises of the individual cells highlighted in Figure 5.2 for 2 cases; (d) top and (e) side views of 3-D temperature rise maps determined at points A, B, C shown in (a) and (b).

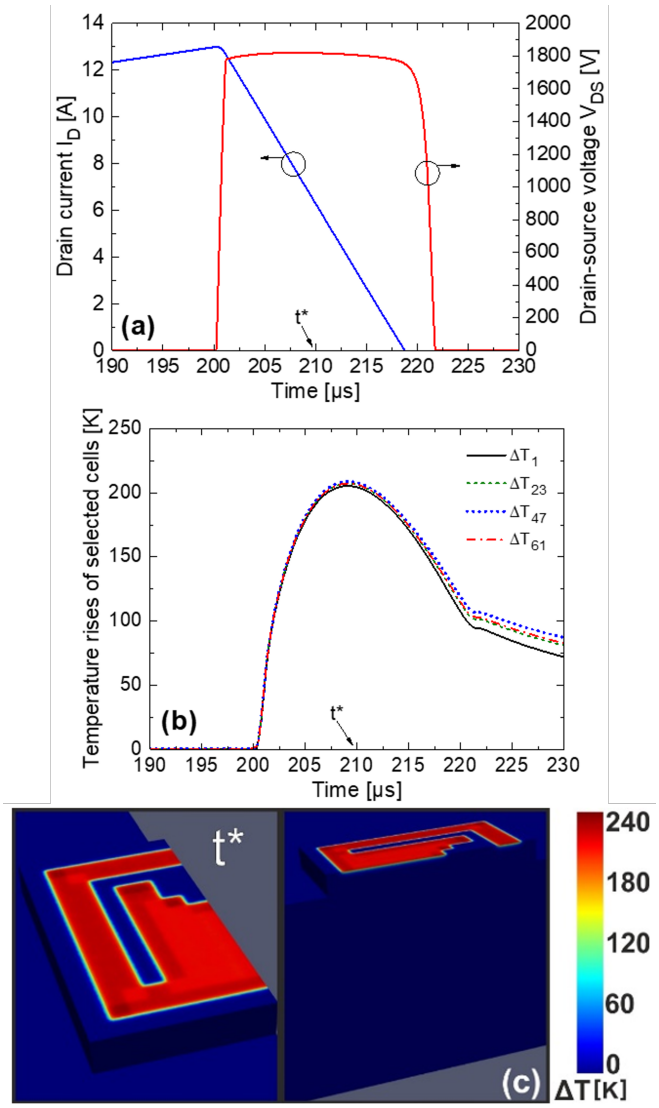

Figure 5.10. UIS test: (a) drain current I_D and drain-source voltage V_{DS} against time; (b) temperature rises of the individual cells identified in Figure 5.2; (c) top and side views of the temperature rise map calculated at time instant t^*=210 μs shown in (a) and (b).

5.5 Summary

This chapter presents an innovative approach for the ET simulation of a multicellular SiC MOSFET using a fully-circuital representation. The device is subdivided into a fixed number of individual cells, each described by (i) an electrical model based on a "real" MOSFET SPICE primitive and (ii) a TFN extracted by means of FANTASTIC, which is in turn fed with the 3-D representation of the DUT. Static and dynamic ET simulations were performed with no convergence issue and with a relevant advantage in terms of computational times if compared to traditional techniques. In addition, FANTASTIC allowed reconstructing the space-time temperature distribution of the whole DUT at any given time instant.

Chapter 6

Multi-chip ET simulation of power circuits

In this Chapter, an advanced TFN-based ET simulation strategy is applied to a multi-chip SiC-based PM. A synchronous step-up dc-dc converter and a single-phase inverter, both embedded into the SSC PM shown in Chapter 3, are simulated. Differently from Chapter 5, where a single device was simulated, the focus of this Chapter is on the simulation of power circuits embedding multiple power devices.

6.1 Parasitics characterization of the PM

A preliminary study was devoted to the electromagnetic characterization of the PM parasitics. It consisted in the experimental evaluation of stray inductances, distributed resistances, and parasitic capacitances by varying frequency. To this aim, a Hioki IM3570 impedance analyzer [Hioki] equipped with Hioki L2000 probes was exploited to measure the total loop parasitic inductance and resistance, as well as the common-mode capacitance. Results are shown in Table 6.1, which summarizes the values of the parasitics at the devices typical switching frequencies (f_{SW}). It is worth noting that, during the parasitics measurements, the devices were fully-on (V_{GS}=20 V) and the total loop parasitic resistance was evaluated by subtracting the devices on-state resistance (∼62 mΩ) from the measured value. The parasitic extraction did not take into account the coupling be-

tween inductance loops since the PM was designed so as to make such a mutual effect negligible [Hus18].

Table 6.1. Values of the experimentally extracted parasitics at the frequencies of interest.

f_{SW}	32 kHz	64 kHz	100 kHz
Total loop parasitic resistance	∼5.4 mΩ	∼5.2 mΩ	∼4 mΩ
Total loop parasitic inductance	∼130 nH	∼30 nH	∼120 nH
Common-mode capacitance	∼121 pF	∼118 pF	∼118 pF

6.2 Calibration of Kirchhoff's parameter

Nonlinear thermal effects are accounted for by means of Kirchhoff's transformation (Section 2.3). The calibration was performed as follows: first, the R_{TH00} of an individual VDMOS transistor was evaluated in COMSOL. The temperature dependence of k was then activated, and many COMSOL simulations were carried out with P_D logarithmically spanning the wide 1.8–1800 W range; hence, the nonlinear temperature rise averaged on the channel region was obtained as a function of P_D. As a final step, the α parameter was calibrated through a least-squares algorithm to achieve the best agreement between Eq. 2.21 and the results obtained through COMSOL under nonlinear conditions. Figure 6.1 shows the results of the fitting procedure, which demonstrate that the choice of the parameter α=0.9443 allows achieving an excellent agreement over a broad range of ΔT values (0–700 K).

6.3 Case-study #1: dc-dc step-up converter

As a first case-study, the proposed simulation approach was applied to a 30 kW synchronous step-up dc-dc converter including the PM under analysis.

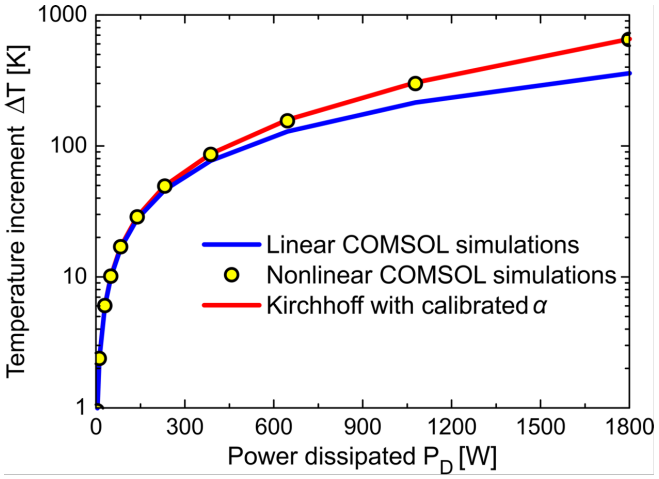

Figure 6.1. ΔT *vs.* P_D. Comparison between non-linear FEM simulations (yellow dots) and values obtained with calibrated Kirchhoff's transformation (red curve). The graph also reports ΔT_{lin} given by the product of R_{TH00} and P_D (blue curve).

Figure 6.2 illustrates the schematic with emphasis on device subcircuits and parasitics.

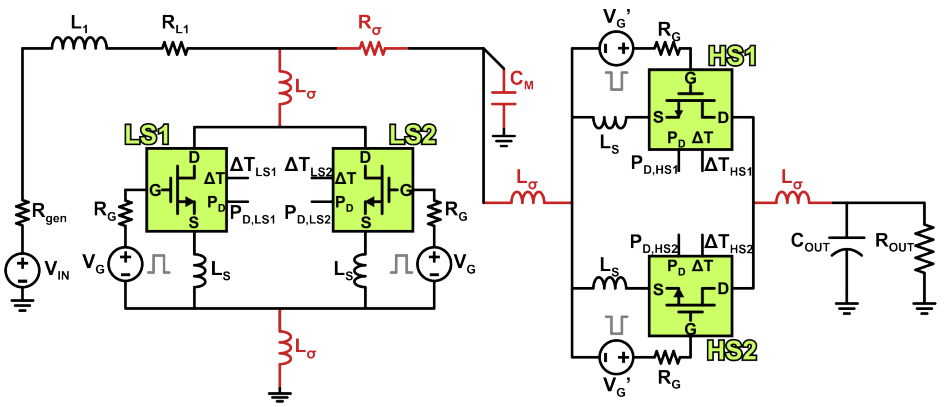

Figure 6.2. Schematic of the half-bridge circuit driven in a synchronous step-up configuration. The light green boxes are the transistor subcircuits depicted in Figure 5.1, while the parasitics are modeled with the passive components drawn in red.

The connections are designed to realize the circuit configuration with two parallel devices at the high side (HS) and two parallel devices at the low side (LS); the gate signals V_G and V_G' were generated to control the LS and HS devices, respectively. A switching frequency f_{SW}=100 kHz was considered. A sketch of the TFN is depicted in Figure 6.3. Table 6.2 summarizes the circuit parameters adopted in the ET simulations, chosen so as to respect the specifications on the output power. The parasitics were accounted for through the lumped elements R_σ, L_σ, and C_M, the values of which at f_{SW}=100 kHz were obtained by elaborating the experimentally extracted total loop parasitic inductance and resistance, and common-mode capacitance shown in Table 6.1. The efficiency of the step-up converter was computed to be η=94.35% by elaborating the ET simulation results. Figure 6.4 shows the P_D values of the four devices at the limit cycle, while their operating temperatures averaged on the channel regions are reported in Figure 6.5. The circuit configuration makes the LS devices dissipate much more power with respect to the HS ones, which results in a significant temperature difference between them (Figure 6.5). As already seen in Chapter 5, FANTASTIC was exploited to reconstruct the whole spatial temperature field in the PM at chosen time instants. Figure 6.6 depicts the PM temperature field extracted at t=800 ms; an interesting finding is that the maximum temperature of the LS devices (∼190°C) is 30°C higher than the average one (Figure 6.5).

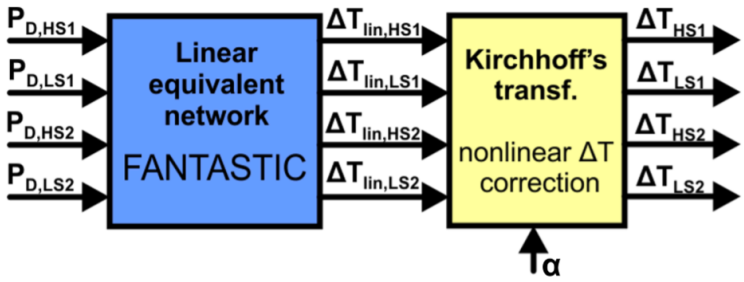

Figure 6.3. Sketch of the TFN comprising (i) the TFN automatically built by FANTASTIC (light blue box) and (ii) the nonlinear correction performed by preliminarily tuned Kirchhoff's transformation (light yellow).

Table 6.2. Values of the dc-dc converter parameters adopted in SPICE.

parameter	value
V_{IN}	800 V
R_{gen}	0.1 Ω
L_1	5 mH
R_{L1}	0.1 Ω
P_{OUT}	29 kW
R_G	4 Ω
C_{OUT}	10 μF
R_{OUT}	120 Ω
L_σ	30 nH
R_σ	4 mΩ
L_{WB}	1 nH
C_M	118 pF
f_{SW}	100 kHz
T_{ON}	5.5 μs

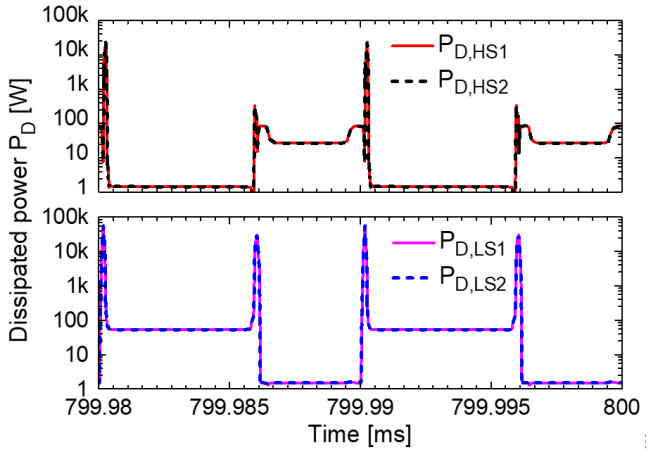

Figure 6.4. SPICE simulation of the macrocircuit representing the dc-dc converter: power dissipated by the four VDMOS transistors *vs.* time in a two-period-long window at the limit cycle; the top (bottom) curves show the values referred to HS (LS) devices.

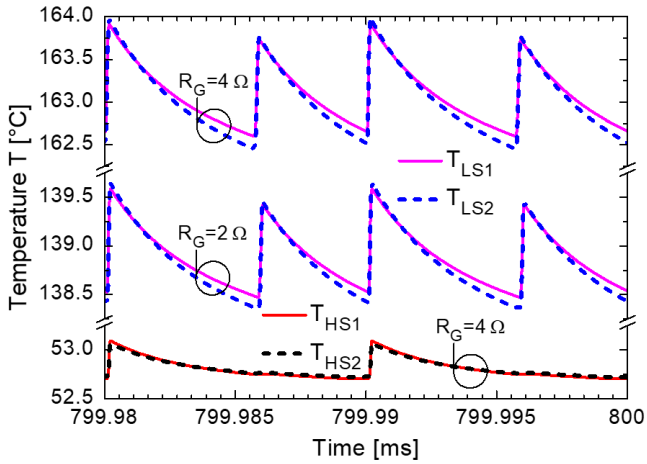

Figure 6.5. SPICE simulation of the macrocircuit representing the dc-dc converter: temperature of the four VDMOS transistors (averaged on the active area) *vs.* time in a two-period-long window at the limit cycle. Also reported is the temperature evolution of the LS devices obtained by reducing the gate resistance R_G from 4 Ω down to 2 Ω.

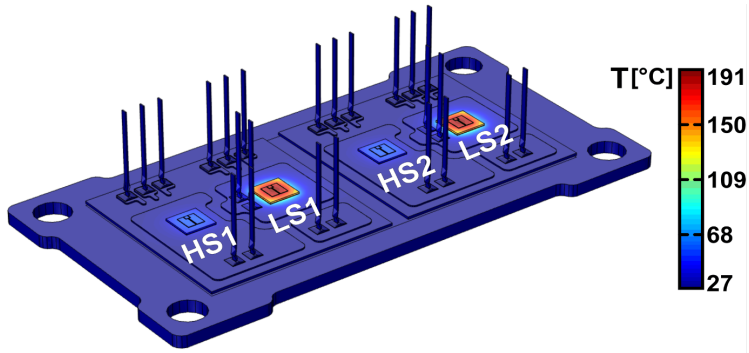

Figure 6.6. Nonlinear-corrected spatial temperature distribution in the PM extracted by FANTASTIC in a post-processing stage, corresponding to the time instant t=800.0 ms of the dc-dc converter simulation. The insulating gel is set as transparent for illustrative purposes. The location of LS and HS devices is also highlighted.

As proof of the suitability of the proposed approach in parametric

analyses, additional exemplificative simulations were performed to quantify the converter performances by modifying circuit parameters. To this aim, the gate resistance R_G and the switching frequency f_{SW} were varied in the ranges 2–6 Ω and 90–105 kHz, respectively. While the R_G range was chosen according to values typically adopted for SiC-based VDMOS, f_{SW} values were selected in a narrow range to ensure the circuit working in continuous current mode given the passive components values (i.e., L_1=5 mH and C_{OUT}=10 μF); in principle, any value of f_{SW} and R_G can be adopted. As a figure of merit of the circuit, η was evaluated and reported in Table 6.3, while Figure 6.5 also shows the lower temperatures of the LS transistors obtained by reducing the gate resistance R_G from 4 Ω (default value) down to 2 Ω. The main findings can be summarized as follows:

- lower R_G values increase η; however, designers should also consider the detrimental effects on di/dt.
- by reducing f_{SW}, the losses due to the reactive components and PM parasitics are mitigated, thus leading to higher η values.

The six simulations performed for this analysis allowed offering further evidence of the excellent convergence properties and the low CPU time requirements (∼2 h for a time window of 800 ms on a PC equipped by a single i7-4710HQ CPU and a 16 GB RAM).

Table 6.3. Outcome of the parametric analysis conducted on the dc-dc converter: the efficiency (η) evaluated at different R_G and f_{SW} values.

R_G	2 Ω	4 Ω	6 Ω
η	95.17%	94.35%	93.55%
f_{SW}	105 kHz	100 kHz	90 kHz
η	93.49%	94.35%	95.59%

6.4 Case-study #2: single-phase inverter

ET simulations of a single-phase inverter were also performed; the approach was applied to the macrocircuit schematically depicted in Figure 6.7.

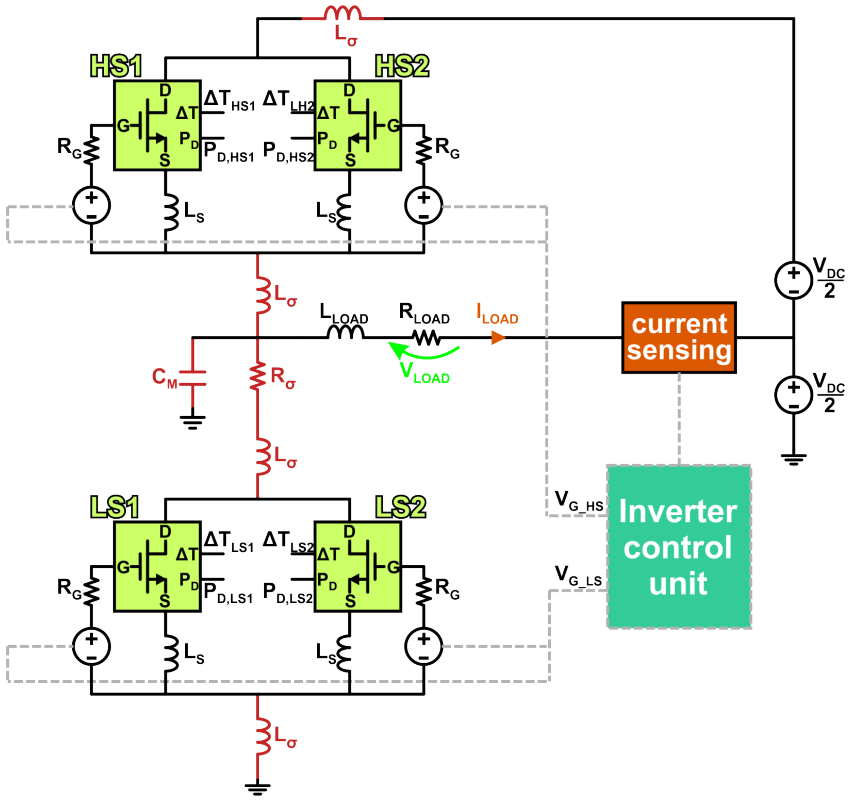

Figure 6.7. Schematic of the half-bridge circuit driven in a single-phase inverter configuration. Evidenced are the experimentally-extracted parasitics (red), the output current and voltage (orange and green arrow, respectively), the VDMOS subcircuits described in Figure 5.1 (light green boxes), the current sensing component (orange), the ICU (turquoise), and the logic signals (grey dashed lines) fed to the gate drivers of the four transistors.

The 50 Hz-400 V RMS inverter was designed to achieve a high efficiency value (∼92%) providing a P_{LOAD}=4.5 kW RMS to R_{LOAD}; such electrical rates respect European ac standards and are compatible with wind- and solar-energy conversion [Koj04], [Dog19]. Furthermore, the circuit can be easily modified into a double-pulse tester, which is widely adopted in parametric switching characterization of transistors [Mou18]. The circuit required the use of an inverter control unit (ICU). As the load current is

detected by means of a current sensing, the ICU generates ad-hoc voltage signals ($V_{G,LS}$ and $V_{G,HS}$) to be fed to the gate drivers of the transistors. The control is based on a duty-cycle modulation technique. While the SPICE macrocircuit includes the same lumped parasitic components used for the dc-dc converter simulations, their values were varied according to f_{SW} (i.e., 64 kHz for the case-study). The parameters used in the inverter simulations are summarized in Table 6.4.

Table 6.4. Values of the inverter parameters adopted in SPICE.

parameter	value
V_{DC}	1800 V
L_{LOAD}	5.8 mH
R_{LOAD}	40 Ω
$P_{OUT,RMS}$	4.5 kW
R_G	2 Ω
L_σ	7.5 nH
R_σ	5.2 mΩ
L_{WB}	1 nH
C_M	118 pF
f_{SW}	64 kHz

An ET simulation of 1 s required 1 h on a standard PC. The efficiency of the inverter was evaluated to be η=91.39%. The current and voltage waveforms on the resistive load are shown in Figure 6.8 over a 20 ms-wide time window at the limit cycle. The duty-cycle modulation technique leads the HS (LS) devices to dissipate more power in the first (second) half of the period. This is also confirmed by Figures 6.9 and 6.10, which depict the average temperature of the HS and LS devices, respectively. It must be underlined that (i) the high efficiency, (ii) the good BCs applied to the bottom of the Cu baseplate, and (iii) the high R_{LOAD} value contribute to achieve low ΔTs (∼30°C). As a main difference with the dc-dc converter, in which the LS devices turned out to be hotter than the HS ones, here the device temperatures are more evenly distributed.

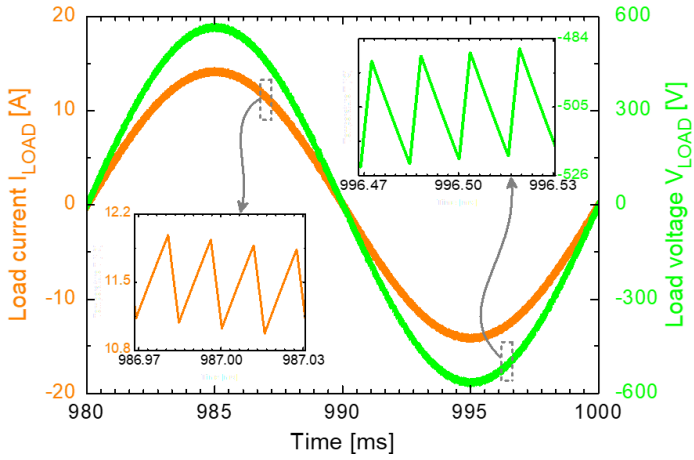

Figure 6.8. Simulated I_{LOAD} (orange curve) and V_{LOAD} (green) *vs.* time in the last 20 ms window. Magnifications highlighting the ripple of I_{LOAD} and V_{LOAD} in four-period-long windows are also reported on the bottom-left and top-right corners, respectively.

Again, the post-processing feature of FANTASTIC was exploited to extract the nonlinear-corrected temperature maps on the PM at the time instants t=987.0 ms (Figure 6.11a) and t=996.5 ms (Figure 6.11b). As a last analysis, a parametric investigation (similar to the one carried out on the dc-dc converter) was conducted on the single-phase inverter. Table 6.5 shows the inverter efficiency η as a function of f_{SW} and R_G. The influence of such parameters was evaluated in a fast, yet trustworthy, simulation session that lasted 4 h and proved the suitability of the approach even in parametric analyses of ac circuits.

Table 6.5. Outcome of the parametric analysis conducted on the inverter: efficiency (η) evaluated at different R_G and f_{SW} values.

f_{SW}	R_G=2 Ω	R_G=4 Ω
32 kHz	η=95.32%	η=92.88%
64 kHz	η=91.39%	η=87.32%

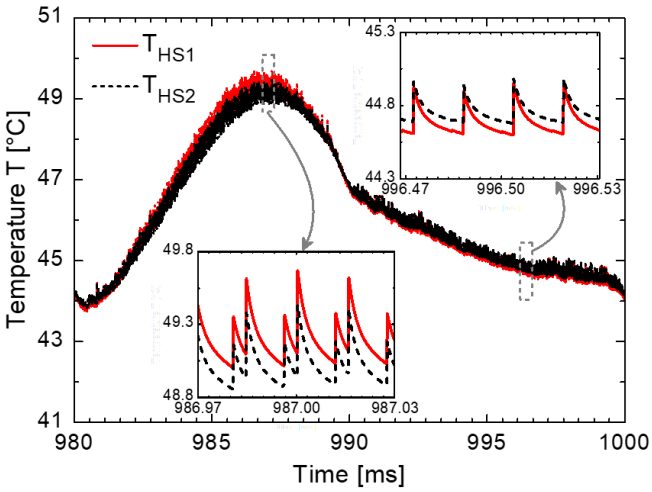

Figure 6.9. Simulated temperature of the HS devices *vs.* time in the last 20 ms window. Magnifications highlighting the temperature ripple in four-period-long windows are also reported on the bottom-left and top-right corners.

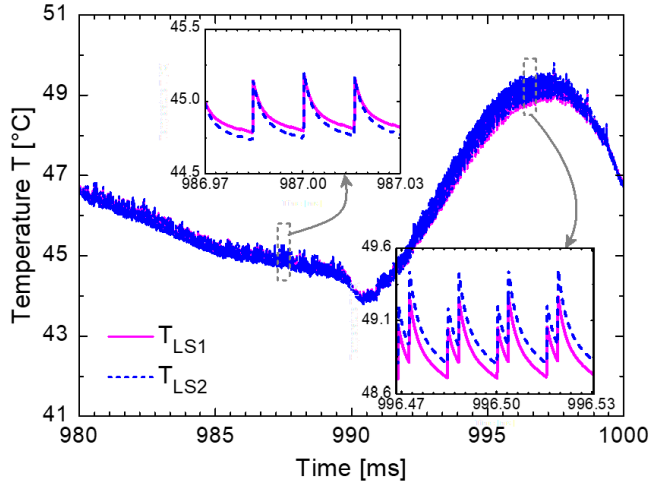

Figure 6.10. Simulated temperature of the LS devices *vs.* time in the last 20 ms window. Magnifications highlighting the temperature ripple in four-period-long windows are also reported on the top-left and bottom-right corners.

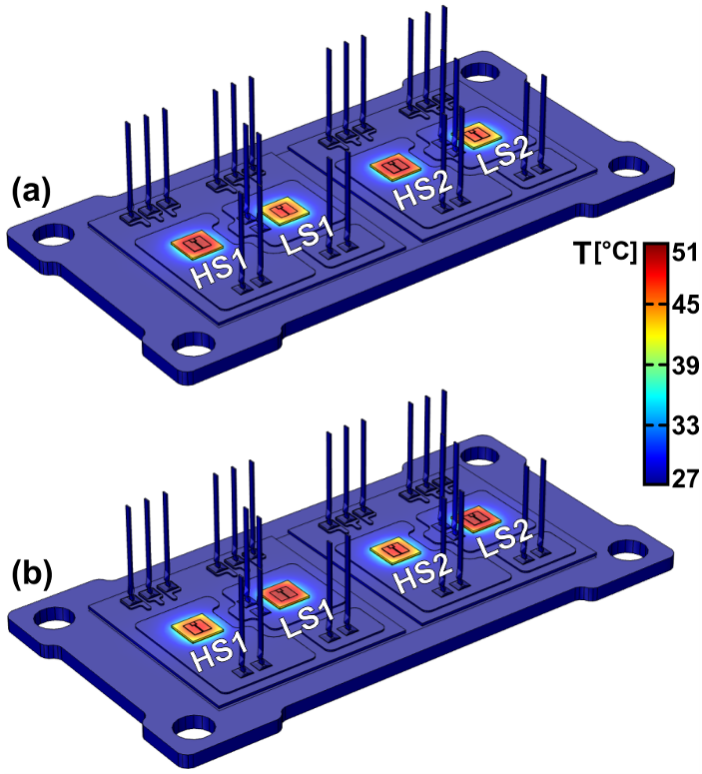

Figure 6.11. Nonlinear corrected spatial temperature distributions extracted by FANTASTIC in a post-processing stage. The maps correspond to the time instants (a) t=987.0 ms and (b) 996.5 ms of the inverter simulation. The insulating gel is set as transparent for illustrative purposes. The location of LS and HS devices is also highlighted.

6.5 Summary

An efficient and versatile strategy for fast and accurate dynamic TFN-based ET simulations was applied to a state-of-the-art multichip PM including four 3.3 kV SiC VDMOS transistors arranged in a half-bridge configuration. The individual devices are described with subcircuits implementing a behavioral model. The power-temperature feedback is included with an equivalent TFN automatically extracted by FANTASTIC with an

advanced MOR technique applied to a 3-D COMSOL mesh representing a very accurate replica of the real module; such a network is in turn equipped with a numerically calibrated Kirchhoff's transformation to account for nonlinear thermal effects. The strategy was exploited to simulate a synchronous step-up dc-dc converter and a single-phase inverter embedding the aforementioned PM. In both cases, circuit parasitics were included, the values of which were calibrated on the basis of the total loop parasitic resistance/inductance and common-mode parasitic capacitance experimentally extracted in a preliminary stage. Despite the complexity of the problem, the high switching frequency, the high temperatures reached, and the long-time range analyzed, the simulations were carried out in a relatively short time on a standard PC without convergence issues; more specifically, 1 h and 2 h were required to perform the 800 ms-long dc-dc converter and 1 s-long ac inverter ET simulations, respectively. This allowed for effortlessly conducting an illustrative study on the impact of key parameters on the circuit performance (i.e., in terms of efficiency). The analysis has shown that the proposed approach can be fruitfully used for the analysis and design of power conversion architectures in strategic domains of societal infrastructure, such as railway traction and renewable energy conversion.

Chapter 7

Conclusions

The underlying theme of this dissertation is the analysis of the dynamic thermal and electrothermal behavior of electronic devices and circuits. Modeling techniques for steady-state and dynamic self- and mutual-heating effects have been described, as well as an *in-house* tool for automatic 3-D finite-element method simulations in the COMSOL Multiphysics environment. The tool has been adopted in large simulation campaigns as it allows (i) building exceptionally-accurate 3-D representations of devices/systems, (ii) discretizing them into tetrahedral grids, (iii) setting up the thermal problem, and (iv) carrying out its solution.

Thermal-only analyses have been conducted on state-of-the-art single-sided and double-sided power modules, which have been compared by emulating different cooling systems. Results counterintuitively show that the adoption of the innovative, more expensive as well as less standardized double-sided technology is justified as long as very efficient boundary conditions are ensured; the physical reasons behind this effect (involving heat spreading mechanisms occurring in the assemblies) have been described.

Double-sided cooled power modules have also been subjected to a fault-detection analysis based on 'structure functions', that is, elaborations of the dynamic thermal responses of electronic systems. Structure functions allow detecting faults/defects in the layers crossed by the heat flow, and their usefulness has been demonstrated even in assemblies characterized by both upward and downward heat flows.

A novel thermal impedance measurement technique for power devices

has been developed: the technique is suitable for *in-situ* measurements, i.e., the power device can be fully characterized without removing it from its application environment. This is extremely useful in scenarios where the device is already deployed – e.g., in the fields of energy distribution, automotive, aircraft, and spacecraft – and eventual faults must be detected early and without interruption of service. In addition, the influence of the device operative conditions as well as the boundary conditions of its working environment is taken into consideration. The technique has been unambiguously validated through the 'simulated experiments' strategy, where the quantity to extract is compared to a known reference quantity. Simulated experiments confirmed the suitability and the accuracy of the technique in both SiC-based power modules and GaN-based PCB-integrated power circuits.

Extremely efficient and accurate electrothermal simulations have been performed adopting a fully-circuital approach: the device electrical behavior has been modeled through simple, yet accurate, physics-based models, while the thermal one has been (i) characterized with the *in-house* routine by means of thermal analyses, (ii) included in SPICE environment by means of thermal feedback networks – Foster and Cauer circuits, as well as networks provided by MOR tools such as FANTASTIC – based on SPICE primitives, and (iii) equipped with equations dealing with nonlinear thermal effects (Kirchhoff's transformation).

The above approach has been first applied to a multicellular SiC power MOSFET, the active area of which has been discretized into a high number of individual cells. Mutual electrical and thermal interactions between cells have been characterized under dc, short-circuit, and unclamped inductive switching conditions; in addition, the space-time temperature distribution of the whole device has been reconstructed at given time instants. The fully-circuital approach allowed performing electrothermal simulations with reasonable CPU times and with unlikely convergence issues, in spite of the high number of individual cells.

In addition to the ET simulation of single devices, multi-chip power circuits have also been investigated in a study involving a dc-dc step-up converter and a single-phase inverter included in single-sided power modules. Here, devices have been modeled with single cells, and mutual interactions between devices have been accounted for. The power module

parasitics have been experimentally characterized, and extremely-efficient simulations have been run with no convergence issues. Parametric investigations have been conducted, in order to emulate a designer acting on circuit parameters and proving the usefulness of the approach when included in thermal-aware designs workflows.

In the light of the results shown in this dissertation, it has been demonstrated that the developed tools and methodologies can be conveniently and successfully adopted to (i) aid testing and validation of electronic devices for the definition of their safe operating areas, (ii) support designers in thermal aware design workflows by enabling fully-circuital, extremely-accurate, fast, efficient, easy-to-converge, and entirely automated electrothermal simulations in SPICE environments, and (iii) assist fault/defect detection tasks by means of structure functions, based on valuable information such as thermal impedances extracted *in situ*.

It is finally worth mentioning that the above methodologies have been largely and successfully applied to investigate and model electrothermal effects in radiofrequency heterojunction bipolar transistors and in the field of renewable energies (photovoltaic modules and fields).

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