TESI DI DOTTORATO

UNIVERSITÀ DEGLI STUDI DI NAPOLI "FEDERICO II"

DIPARTIMENTO DI INGEGNERIA BIOMEDICA, ELETTRONICA E DELLE TELECOMUNICAZIONI

DOTTORATO DI RICERCA IN INGEGNERIA ELETTRONICA E DELLE TELECOMUNICAZIONI

ANALYTICAL MODELING AND NUMERICAL SIMULATIONS OF THE THERMAL BEHAVIOR OF BIPOLAR TRANSISTORS

ILARIA MARANO

Il Coordinatore del Dottorato
Ch.mo Prof. Giovanni POGGI

Il Tutore
Ch.mo Prof. Niccolò RINALDI

Anno Accademico 2007-2008

Acknowledgements

I wish to thank all people who helped me during these years giving me the possibility to complete my PhD. First of all, my tutor Prof. Niccolò Rinaldi, whose stimulating suggestions allowed me writing this thesis.

A special thank is for my *pseudo-tutore* Enzo: without his encouragement, patience and comprehension it would have been impossible for me to finish this work. He is a great friend and mentor. Thanks a lot!

I would like also to thank Luigi, Francesco, Marco, Valeria, Nicola, Davide, Lucio, Michele for the pleasant moments that we spent together and their kind words of encouragement.

I'm also very grateful to my parents and sister who always supported me and believed me even when I didn't.

Finally, the greatest thank is for my *husband*, Ciro, for his love and patience. Thanks for having been able to bear my numerous mood swings!

Index

Introduction

I.1. Thermal effects in semiconductor devices

Communication and information systems are subject to faster and faster changes. The increasing complexity of electronics systems, requiring higher and higher packing densities and faster circuit speeds, led to an increase in power dissipation and consequently to enhanced self-heating effects. In addition, in order to minimize cross-talk effects and improve high-frequency performances, isolation schemes based on buried oxide layers or deep trench are widely adopted in both bipolar and MOS technologies. These devices are extremely affected by self-heating effects, due to the low thermal conductivity of the buried oxide and the material filling the trench compared to that of silicon. Self-heating effects have become a crucial issue also in heterojunction bipolar transistors (HBTs) due to the high current levels these devices are devised to handle.

Unfortunately, it is well known that thermal effects can affect the reliability and performance of the system so that an exact prediction of the thermal behavior becomes of fundamental importance during device/circuit design. For this purpose an accurate investigation of thermal phenomena must be carried out in order to develop high-performance, low-cost and high-reliability electronic systems for high-frequency applications.

In principle, fully 3-D numerical simulations, which are predictive and allow accounting for all the details of an arbitrarily complex geometry, can be performed.

However, even if numerical simulation tools may reduce expensive technological efforts, the fine discretization requested to achieve satisfying simulation accuracy makes such methods too computationally demanding, thus becoming impracticable when

dealing with a large number of transistors. As an alternative, one can resort to high-efficiency analytical approaches, since they require a lower computational cost and can be easily included in electrothermal circuit simulation tools. Unfortunately, this is not a trivial task due to inherent structural complexity of the modern devices.

It is clear that both solutions present some disadvantages so that a proper choice about the option to be adopted in a given problem is very important and complex.

I.2. Thesis contents

This thesis deals with the analysis of the thermal behavior of bipolar transistors characterized by isolation schemes (i.e., *deep trench*, *shallow trench*, *buried oxide layer*) aimed at improving the high-frequency performance of the devices/circuits. The investigation focuses on three types of bipolar transistors: BJT isolated by deep trench and fabricated on SOI (silicon-on-insulator) substrates (i.e., characterized by a buried oxide layer), BJT isolated by deep trench and fabricated on conventional silicon bulk substrates, HBT SiGe characterized by deep and shallow trenches.

In Chapter 1, a brief introduction to the state-of-the-art isolation schemes is presented.

In Chapter 2, the thermal behavior of deep trench isolated structures on SOI substrates is thoroughly analyzed. Detailed 3-D numerical simulations have been performed to investigate the heat transfer capability of silicon-trenches and silicon-buried oxide interfaces and the impact of all technological and material parameters of interest. It has been shown that the heat transfer phenomena across the silicon island sidewalls can be well approximated by considering simplified convective boundary conditions with uniform heat transfer coefficients. Based on such a result, a novel analytical model has been developed for evaluating the temperature field in a trench SOI structure, which is based on the reduction of the domain under analysis to a silicon rectangular parallelepiped with convective boundary conditions at lateral and bottom faces. An extensive comparison with numerical results proves that the model, that is

entirely predictive, is extremely accurate in the overall parameter range (the accuracy has been demonstrated to lie within 5%) and can be adopted for a fast evaluation of the thermal resistance of a trench SOI device as well as of the temperature gradients within the silicon island surrounded by trenches and buried oxide in order to improve the thermal ruggedness during circuit design.

In Chapter 3, a complete and comprehensive analysis of the thermal behavior of trench-isolated bipolar transistors fabricated on conventional bulk-silicon substrates has been carried out. Fully 3-D numerical simulations are performed to analyze the impact of all technological parameters of interest. Based on numerical results, a novel strategy to analytically evaluate the temperature field is proposed, which allows accurately accounting for the heat propagation through the trench and the nonuniform temperature/heat flux distributions over the interface between the silicon trench box and the underlying substrate. The strategy is based on the reduction of the domain under analysis to a simplified structure subdivided into the silicon-only trench box with convective boundary conditions at lateral sidewalls and the silicon substrate. The resulting analytical model is (i) entirely predictive, namely, the thermal behavior of any trench-isolated bipolar transistor can be analyzed starting only from information concerning geometrical and material parameters; (ii) effective, since proper approaches have been chosen to describe the thermal process in both the trench well and the silicon substrate: a few seconds are indeed needed to evaluate a thermal resistance value; and (iii) highly accurate compared to all other predictive models available from the literature: an error <2% is obtained with respect to 3-D numerical simulations in a wide range of values for all technological parameters. As a consequence, the proposed model can be employed for an accurate, yet fast evaluation of the thermal resistance of a trench-isolated device as well as of the temperature gradients within the silicon box surrounded by the trench. Hence, it can be suggested as an effective means for optimizing the thermal design of bipolar transistors fabricated in deep-trench technology with both oxide lined and filled trenches.

Finally, in Chapter 4, the thermal behavior of SiGe heterojunction bipolar transistors (HBTs) is analyzed. Fully 3-D numerical simulations are performed to analyze the impact on the thermal behavior of all technological elements (e.g., shallow trench, metal slot

contacts, deep trench). The numerical results evidenced that the thermal behavior of the overall structure is similar to the one exhibited by a simplified structure in which the heat source is embedded in a bulk silicon substrate and laterally isolated by deep trench. Such a result allows extending to SiGe HBTs the model proposed for trench-isolated bipolar transistors. An accurate parametric analysis allows evaluating the influence on the thermal behavior of all technological parameters of interest (i.e., emitter length, deep and shallow trench depths, heat source thickness, distance between the active region and trench, trench geometry). The scaling effects on thermal resistance are also analyzed as well as the nonlinear effects introduced by the dependence of the silicon and tungsten thermal conductivity on temperature. An extensive comparison with numerical results proves that the model is rather accurate in the overall parameter range (a maximum error of 12% has been relieved).

Chapter 1

Isolation schemes in bipolar technology

A lot of improvements were introduced in bipolar technology since, around 1958, Jack Kilby of Texas Instruments and Robert Noyce of Fairchild Semiconductor independently co-invented the integrated circuit: the epitaxial collector regions above heavily doped buried layers were produced, LOCOS isolation was adopted in place of the junction isolation, narrow base regions were fabricated by means of the implantation of impurities and so on. In order to increase the cutoff frequencies, a reduction of device vertical dimensions was needed. Such aim was reached by realizing arsenic-doped emitters with shallow boron-doped bases. The current gain was further improved by fabricating emitter contacts in polysilicon. It was indeed observed that polysilicon contacts to monocrystalline emitter regions produced gains 4-5 times larger than the ones of comparable metal-contacted emitters. In 1980s, thanks to the plasma-etching processes, the concept of self-alignment was introduced, that allowed reducing significantly the device lateral dimensions and led to the fabrication of the device that represents the state-of-the-art of silicon high-frequency bipolar transistors [1].

Further advances were made by adopting novel isolation techniques, e.g., silicon-on-insulator schemes or shallow/deep trench isolation.

This Chapter briefly discusses the modern isolation techniques with their advantages and drawbacks.

1.1. Trench isolation

An integrated circuit is based on the concept that many components (passive and active) are fabricated together on the same semiconductor substrate. This target can be achieved only thanks to

device isolation.

In an ideal situation, in order to assure that the operation of one transistor does not affect the neighboring ones, each device would be surrounded by a perfect electrical insulator. Unfortunately, in reality this is not possible when dealing with semiconductors.

The earliest type of isolation was introduced by Noyce and it is known as *junction isolation* [2]. The junction isolation is based on the physical property of the silicon PN junction: current cannot flow in a reverse-biased junction. Therefore, the electrical isolation is assured providing the correct voltages to the materials keeping the PN isolation junctions in reverse bias. However, some non-ideal properties affect the PN junction behavior.

1. In a reverse-biased junction a current, even if low, always flows. This leakage current increases with temperature and results in a higher power dissipation by the devices that should be isolated, and therefore in a gain reduction.
2. There is an intrinsic capacitance associated with a PN junction depending on the reverse voltage applied across it. This capacitance can limit the circuit operating frequency and produce a higher harmonic distortion creating nonlinearities.
3. The junction isolation consumes a large amount of silicon area because of lateral diffusions. Furthermore, in high-voltage technologies the space required can become excessively large since the junction isolation size must increase with the applied voltage.
4. Finally, if the voltage applied across the reverse-biased junction generates an electric field exceeding the so-called *critical electric field*, the semiconductor will destroy and the current will begin to flow.

Fortunately, around 1980s, the advances in silicon etching technology (i.e., the capability to remove specific silicon areas) allowed realizing the first trenches separating *physically* the devices.

Nowadays many bipolar processes are based on trench isolation to improve packing density [3], reduce parasitic capacitances, minimizing cross-talk interference, and favor latch-up immunity [4]-[7] so as to improve high-frequency device performance.

Shallow trench isolation (STI), also referred to as BIT (Box Isolation Technique), prevents leakage current between adjacent

devices/circuits integrated on the same chip. STI is created during the semiconductor device fabrication process, before realizing active devices. The most important steps of the STI fabrication involve etching a pattern of trenches in silicon, depositing one (or more) dielectric materials to fill the trenches, and removing the excess dielectric using a technique such as chemical/mechanical planarization. STI results in higher packing densities, scaled design rules and lower parasitics that allow reaching higher yields for both CMOS and bipolar circuits. Although demanding on further process steps (i.e., etching and refilling), STI allows reducing the area needed for isolation between circuit elements and consequently the die size, cutting in this way the device cost [8]. However, the shallow trenches are not thick enough to penetrate the epitaxial and buried layers, and do not provide a complete electrical isolation [3]. As a consequence, also the deep trench isolation (DTI) is often adopted, since it provides a further parasitics and crosstalk reduction [6]. As stated before, shallow and deep trenches allow cutting the parasitic capacitances; in particular, they are employed to reduce the base–collector junction capacitance and the collector–substrate one, respectively [9], [10] (a capacitance reduction of 4 times can be obtained thanks to the deep trench employment [11]).

Fig. 1.1 shows the scanning electron microscope (SEM) view of a trench-isolated self-aligned NPN bipolar transistor.
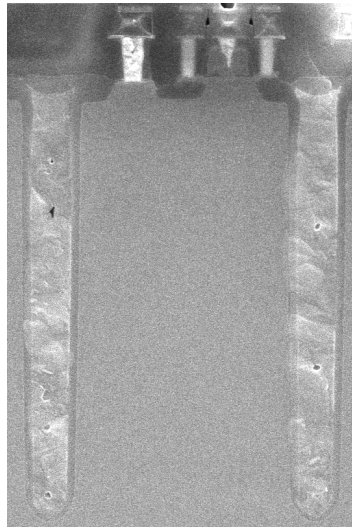

Fig. 1.1. SEM view of a self-aligned NPN transistor. Both shallow and deep trenches are integrated.

The adoption of isolation techniques based on deep trenches allows: a chip area reduction of the order 20-25% with respect to technologies employing standard junction isolation schemes [12]; a decrease by more than 6 orders of magnitude in the parasitic currents injected in the substrate [11]; a current holding increase of 10 times and a reduction in the current gain of the lateral parasitic transistors of about 6 times as compared to trench-free bulk transistors [13].

In conclusion, trench isolation, based on the use of non-conducting materials to isolate the transistors, allows overcoming almost all the non-idealities of junction isolation.

However trench isolation also exhibits some drawbacks.

The trenches are typically filled with an insulator (e.g., SiO_2) or polysilicon lined with SiO_2. Unfortunately, due to the poor thermal conductivity of the trench-filling materials, the heat flow coming from the active transistor area is mostly confined within the silicon-only region enclosed by the trench before spreading into the substrate, thereby leading to exacerbated thermal issues with respect to bulk-silicon transistors of comparable size.

Furthermore, even if the parasitic capacitances are reduced, transistors separated by a deep trench structure are still capacitively coupled to each other and this can affect the electric characteristics of adjacent transistors in dependence of voltage and frequency [8].

1.2. Silicon-on-insulator

To be fully isolated a transistor should be isolated on all sides.

As concerns the top isolation, in trench-isolated technology, a SiO_2 layer is used (as well as in junction-isolated technology). The bottom isolation, on the contrary, can lead to relevant improvements in the circuit performance.

In the silicon-on-insulator (SOI) technology, the top of the wafer (where the transistors/circuits are located) is electrically insulated by a SiO_2 layer from the silicon substrate. The buried oxide layer can be formed both by a thermal oxidation of the top silicon layer (e.g., [14]) and by an oxygen implantation on a screened oxide silicon wafer (e.g., [15]).

The employment of SOI substrates presents some advantages.

Firstly, a further electrical insulation is provided by the buried oxide [16] that results in a reduction of parasitic capacitances, crosstalk, substrate noise, and latch-up. For this technology, collector-substrate capacitances and collector resistance are lower, resulting in increased operating speeds [17]-[19] (a speed increase of 20-35% is obtained compared to bulk CMOS operating speeds [20]). Furthermore, a reduced power is required to achieve high performance (a 2 to 4 times lower power is needed to operate at the same speed as bulk CMOS [20]). The performance of passive components such as inductors and capacitors, are also improved [21]. In addition, the fabrication process is simplified since an N-type collector/substrate isolation region is no longer needed for the PNP transistor and different voltages may be used on different devices without adding processing steps required for triple wells [20].

Fig. 1.2 shows the SEM view of a transistor realized on SOI substrate.
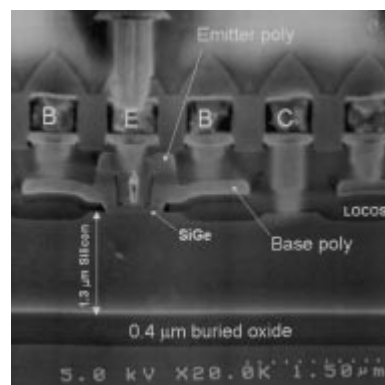
Fig. 1.2. SEM view of a SiGe HBT fabricated on SOI substrate.

Even if SOI complementary bipolar technology requires higher initial wafer costs, the reduction in the process complexity and the increase in circuit density fully justify its employment in most technologies.

However, the trend toward smaller and smaller device geometry and higher and higher operating current density leads to a greater sensitivity to thermal effects in bipolar transistors fabricated using the aforementioned technology. The buried oxide exhibits a very low thermal conductivity compared with the silicon one. Therefore the

thermal power produced by device junctions can be hardly removed resulting in enhanced self-heating effects that can have deleterious consequences on the reliability and performance of the transistors [22], [23].

1.3. Trench-isolated bipolar transistors on SOI substrates

Nowadays advanced technology solutions based on the concurrent adoption of deep trench isolation and buried oxide schemes are increasingly employed due to the need of electrically insulating the active devices from neighboring transistors and substrate. This solution allows overcoming the electrical drawbacks of junction isolation leading to negligible leakage current, reduced parasitic capacitances, and capacitance values independent of the applied voltage variations. In addition, an enhanced immunity to substrate noise and cross-talk are achieved [17], [19], [23].

These features result in faster operating frequencies (since distortion decreases and linearity improves) and lower manufacturing cost (since the isolation size and consequently the die size diminish).

In a trench SOI technology, the active area lies within a silicon island completely enclosed by dielectric layers that ensure the requested full electrical isolation. Fig. 1.3 shows a SEM view of a trench-isolated transistor realized on SOI substrate.
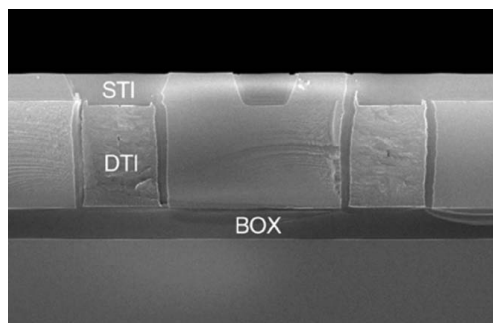
Fig. 1.3. SEM view of a trench-isolated transistor on SOI substrate.

Unfortunately, the poor thermal conductivities of trench materials and buried oxide make the heat removal from the active regions more difficult giving rise to excessively high junction temperatures, if compared to bulk transistors of comparable size embedded in silicon-only substrates, which results in performance and reliability degradation.

1.4. Thermal issues

As claimed before, due to the poor thermal conductivity of the trench-filling materials and buried silicon dioxide, the heat flow coming from the active transistor area, before spreading into the substrate, is mostly confined within the silicon-only region enclosed by the insulating layers. Therefore the adoption of isolation schemes based on deep trench and buried oxide layer makes the devices noticeably affected by self-heating effects with respect to bulk-silicon transistors of comparable size. This statement will be better clarified in the following.

In a bulk-silicon device the heat originated from the active region can flow radially (Fig. 1.4a). Fig. 1.4b shows the corresponding temperature field.
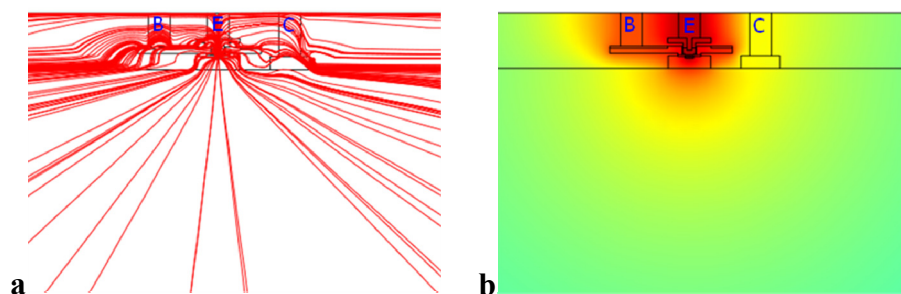
Fig. 1.4. Thermal behavior of a bulk bipolar transistor: (a) heat flux lines and (b) temperature field.

In a trench-isolated device the heat flows more hardly through the trench (Fig. 1.5a) so that the temperature reaches higher values in proximity of the heat source (Fig. 1.5b).
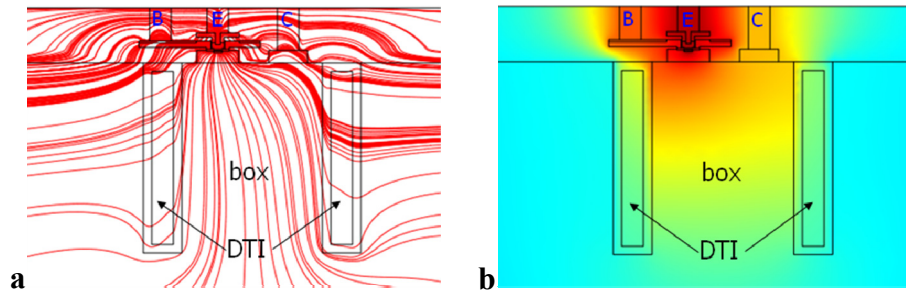
Fig. 1.5. Thermal behavior of a trench-isolated bipolar transistor: (a) heat flux lines and (b) temperature field.

Finally, in a bipolar transistor characterized by the simultaneous adoption of deep trench an buried oxide layer, no silicon paths are available for the heat removal from the active region, so that the heat flow is mostly confined within the silicon island (Fig. 1.6a). This performance exacerbates electrothermal issues with respect to other less drastic isolation schemes, i.e., based only on either trenches or a buried oxide layer, leading to higher temperature peaks (Fig. 1.6b).
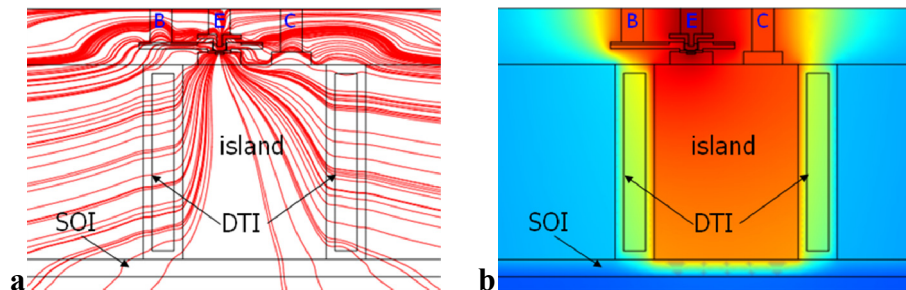
Fig. 1.6. Thermal behavior of a trench-isolated bipolar transistor fabricated on SOI substrate: (a) heat flux lines and (b) temperature field.

This is evidenced in Fig. 1.7., which illustrates the temperature rise above ambient normalized to dissipated power along a vertical line crossing the active area center for various structures, as evaluated through the commercial 3-D numerical simulator Comsol based on the finite element method [24].
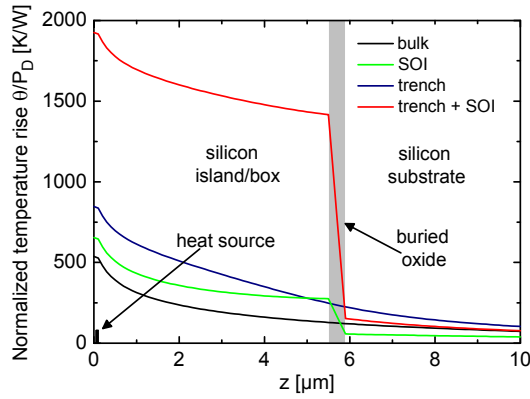
Fig. 1.7. Temperature rise above ambient normalized to dissipated power along the *z* axis as obtained by 3-D numerical simulations. An active region of $0.5 \times 20 \ \mu m^2$ is considered. The cut is taken through the heat source center. The cases of a bulk-silicon transistor (black line), a pure trench-isolated device (blue), a trench-free SOI structure (green), and a trench-isolated SOI one (red) are compared.

It is shown that the self-heating thermal resistance[1] of the trench-isolated SOI transistor, evaluated on the projection of the heat source center on the top surface, amounts to 1860 K/W, while values of (a) 550, (b) 650, and (c) 850 K/W were obtained by (a) removing both trenches and buried oxide (i.e., considering a conventional bulk-silicon device), (b) eliminating only the trenches (i.e., considering a trench-free SOI structure), and (c) removing only the buried oxide (i.e., considering a pure trench bipolar transistor), respectively.

References

[1] Reisch M. High-frequency bipolar transistors: Physics, Modeling, Applications. Springer; 2003.
[2] Thiel F, and Stibila M. The benefits of trench isolation in high-voltage, high-bandwidth semiconductors: Part I – The

---

[1] The self-heating thermal resistance R_{TH} represents an indicator of the device capability to dispose of heat and it is defined as the temperature rise above ambient normalized to dissipated power: $R_{TH} = \left(T_j - T_{AMB} \right) \big/ P_D$.

technology and the physics of trench isolation. [Online]. Available: http://www.analogzone.com/nett0614.pdf

[3]   Ashburn P. SiGe Heterojunction Bipolar Transistors. John Wiley and Sons; 2003.

[4]   Walkey DJ, Smy TJ, Reimer C, Schröter M, Tran H, Marchesan D. Modeling thermal resistance in trench-isolated bipolar technologies including trench heat flow. Solid-State Electron 2002;46(1):7-17.

[5]   Harame DL, Comfort JH, Cressler JD, Crabbè EF, Sun JYC, Meyerson BS, Tice T. Si/SiGe epitaxial-base transistors – Part II: Process integration and analog applications. IEEE Trans Electron Dev 1995;42(3):469-82.

[6]   Forsberg M, Björmander C, Johansson T, Ko T, Liu W, Vellaikal M, Cheshire A. Shallow and deep trench isolation for use in RF-Bipolar ICs. IEEE ESSDERC Proc 2000:212-5.

[7]   Ohue E, Oda K, Hayami R, Washio K. A 7.7-ps CML using selective-epitaxial SiGe HBTs. IEEE BCTM Proc 1998:97-100.

[8]   Lee SS, Allstot DJ. Electrothermal simulation of integrated circuits. IEEE J. Solid-State Circuits 1993;28(12):1283-93.

[9]   Washio K, Kondo M, Ohue E, Oda K, Hayami R, Tanabe M, et al. A 0.2-μm self-aligned SiGe HBT featuring 107-GHz f_{max} and 6.7-ps ECL. IEEE IEDM Proc 1999;557-60.

[10] Nii H, Yoshino C, Yoshitomi S, Inoh K, Furuya H, Nakajima H, et al. An 0.3-μm Si epitaxial base BiCMOS technology with 37-GHz f_{max} and 10-V BV_{CEO} for RF telecommunication. IEEE Trans Electron Dev 1999;46(4):712-21.

[11] Parthasarathy V, Zhu R, Khemka V, Roggenbauer T, Bose A, Hui P, et al. A 0.25μm CMOS based 70V smart power technology with deep trench for high-voltage isolation. IEEE IEDM Proc 2002;459-62.

[12] De Pestel F, Coppens P, De Vleeschouwer H, Colson P, Boonen S, Colpaert T, et al. Deep trench isolation for a 50 V 0.35 μm based smart power technology. IEEE ESSDERC Proc 2003:191-4.

[13] Gilbert PV, Crabtree PE, Sun SW. Latch-up performance of a sub-0.5 micron inter-well deep trench technology. IEEE IEDM Proc 1993;731-34.

[14]   Masui S, Kawamura K, Hamaguchi I, Yano T, Nakajima T, and Tachimori M. An analysis of buried-oxide growth in low-dose SIMOX wafers by high-temperature thermal oxidation. IEEE International SOI Conference Proc 1995;154-5.

[15]   Mulcahy C, Biswas S, Kelly I, Kirkwood D, and Collart E. The distribution of boron and arsenic in SOI wafers implementing SIMS. IEEE International Ion Implantation Technology Conference Proc 2002;1-4.

[16]   Leung YK, Kuehne SC, Huang VSK, Nguyen CT, Paul AK, Plummer JD, Wong SS. Spatial temperature profiles due to nonuniform self-heating in LDMOS's in thin SOI. IEEE Trans Electron Dev Let 1997;18(1):13-15.

[17]   Nigrin S, Wilson MC, Thomas S, Connor S, Osborne PH. A complementary bipolar technology on SOI featuring 50GHz NPN and 35GHz PNP devices for high performance RF applications. IEEE International SOI Conference Proc 2002;155-7.

[18]   Sun ISM, Ng WT, Kanekiyo K, Kobayashi T, Mochizuki H, Toita M, et al. Lateral high-speed bipolar transistors on SOI for RF SoC Applications. IEEE Trans Electron Dev 2005;52(7):1376-83.

[19]   Malm BG, Haralson E, Johansson T, Östling M. Self-heating effects in a BiCMOS on SOI technology for RFIC applications. IEEE Trans Electron Dev 2005;52(7):1423-8.

[20]   Simonton R. Special report: SOI wafer technology for CMOS ICs. [Online]. Available:
http://icknowledge.com/threhold_simonton/soitechnology.pdf

[21]   Mastrapasqua M, Palestri P, Pacelli A, Celler GK, Frei MR, Smith PR, et al. Minimizing thermal resistance and collector-to-substrate capacitance in SiGe BiCMOS on SOI. IEEE Trans Electron Dev 2002;23(3):145-7.

[22]   Kopp D. An efficient and accurate thermal model of Silicon-On-Insulator (SOI) integrated circuits. Thesis topic, Clarkson University. [Online]. Available:
http://www.clarkson.edu/honors/research/thesis.php

[23]   Ganci PR, Hajjar JJJ, Clark T, Humphries P, Lapham J, Buss D. Self-heating in high performance bipolar transistors fabricated on SOI substrates. IEEE IEDM Proc 1992;417-20.

[24]   Comsol Multiphysics 3.3. User's Guide. Comsol AB, 2007.

Chapter 2

Trench-isolated bipolar transistors on SOI substrates

Nowadays, the demand for increasingly smaller chip sizes and higher operation frequencies results in a growing number of processes making a concurrent use of deep trench isolation and silicon-on-insulator schemes. As stated before, this solution allows electrically insulating the active devices from both neighboring transistors and substrate, which leads to a number of attractive features, e.g., reduced parasitic capacitances, low leakage currents, and enhanced immunity to substrate noise and crosstalk [1]-[4].

Unfortunately, the poor thermal conductivities of trench materials and buried oxide, which surround the active area confining the heat flow coming from it, lead to enhanced self-heating effects with respect to bulk-silicon devices of comparable size. Hence, an accurate prediction of the thermal behavior of these structures is needed in order to optimize their design.

In principle, one can resort to fully 3-D numerical simulations, which allow accounting for all the geometry details. However, they are CPU/memory demanding, thus becoming unviable when the number of transistors becomes considerable. As an alternative, high-efficiency analytical approaches can be pursued, since they require a lower computational cost.

Unfortunately, developing analytical thermal models is not a trivial task due to inherent structural complexity of trench-isolated SOI bipolar transistors. Some analytical approaches have been conceived to evaluate the thermal resistances of *either* trench [5]-[9] *or* SOI structures [5], [10]. On the other hand, analyses that simultaneously account for deep trenches and SOI are rarely encountered in literature, although the trench and SOI combination is increasingly employed in ICs in order to achieve a full electrical

isolation of the active devices [11]-[13]. An estimate of the thermal resistance of a trench-isolated SOI structure can be obtained by considering the parallel of thermal resistances associated with the individual sidewalls and buried oxide layers [5]. However, this approach does not allow evaluating the whole temperature distribution in the silicon island surrounded by insulators. To our knowledge, only an attempt to solve this problem has been made in [14], where the authors develop a physics-based analytical model that describes the thermal process in trench SOI devices under transient conditions. However, the resulting mathematical formulation is based on severe assumptions (e.g., a 1-D heat flux through buried oxide and trenches) that adversely affect its accuracy, thus leading to a rather large discrepancy when compared to 3-D numerical results.

In this Chapter, a thorough investigation of the thermal behavior of trench-isolated devices fabricated on SOI substrates under steady-state conditions is presented. The Chapter is organized as follows.

First, detailed thermal-only 3-D numerical simulations are performed to analyze the influence of all geometrical and material parameters on the temperature distribution as well as the heat removal capability of the interfaces between silicon and insulating layers. It is demonstrated that the interfaces between the silicon island and the surrounding insulated materials exhibit a nonuniform proneness to transfer heat.

Subsequently, starting from the numerical results, a novel modeling strategy is developed, which involves the replacement of the actual domain with a simplified silicon-only one with proper boundary conditions that allow describing the thermal process. In particular, convective boundary conditions are adopted, which involve a proper choice of the heat transfer coefficients[2] [W/μm^{2}K] (also referred to as trench conduction parameters [15]). Therefore empirical expressions for the heat transfer coefficients are derived to account for their dependence upon all relevant parameters.

Afterward, based on the adopted strategy, an analytical model for the thermal resistance of trench SOI structures was developed. The resulting model is fully predictive, i.e., it allows evaluating the

---

[2] The heat transfer coefficient [W/μm^{2}K] is defined as the ratio between heat flux and temperature increase above ambient and describes the surface capability to transfer heat [see Eq. (2.2)].

thermal behavior of the structure only from information concerning the corresponding technological details (i.e., geometry and material properties).

Finally, the thermal behavior of a trench SOI structure as a function of all relevant geometry and material parameters is analyzed by means of the model and numerical data. An extensive comparison with 3-D numerical simulations has allowed proving that, despite its simplicity, the model is extremely accurate in a wide range of values for all relevant geometrical and material parameters playing a role. Besides, it requires extremely short simulation times without convergence problems. As a consequence, it can be conveniently used to predict technology-scaling trends as well as to detect temperature gradients within the silicon island.

2.1. Numerical analysis

The domain under analysis is shown in Fig. 2.1a and b, and is comprised of a silicon island surrounded by deep trenches and a buried oxide layer, embedded in a 300-µm thick silicon substrate, with bottom surface assumed to be in an intimate contact with an ideal heat sink at temperature $T_{AMB} = 300$ K.

An exact analytical description of the thermal process in a trench SOI structure is prohibitive due to its intrinsic geometrical complexity. For this reason, we have conceived an effective strategy to simplify the problem, which is similar to the approach exploited in [6] for trench-only devices, and can be summarized as follows: the actual domain (Fig. 2.1a and b) is replaced by a silicon-only domain identical to the silicon island with convective boundary conditions[3] at bottom and lateral faces, and adiabatic top surface (Fig. 2.1c and d).

---

[3] A convective boundary condition (also referred to as condition of 3rd kind or Robin condition) imposes a proportionality relationship between heat flux and temperature through the heat transfer coefficient [see Eq. (2.8)] at an assigned surface. It is noteworthy that, despite its nomenclature, the *convective* condition is used to describe a *heat conduction* phenomenon, namely, the heat transfer through the trench sidewalls and buried oxide.
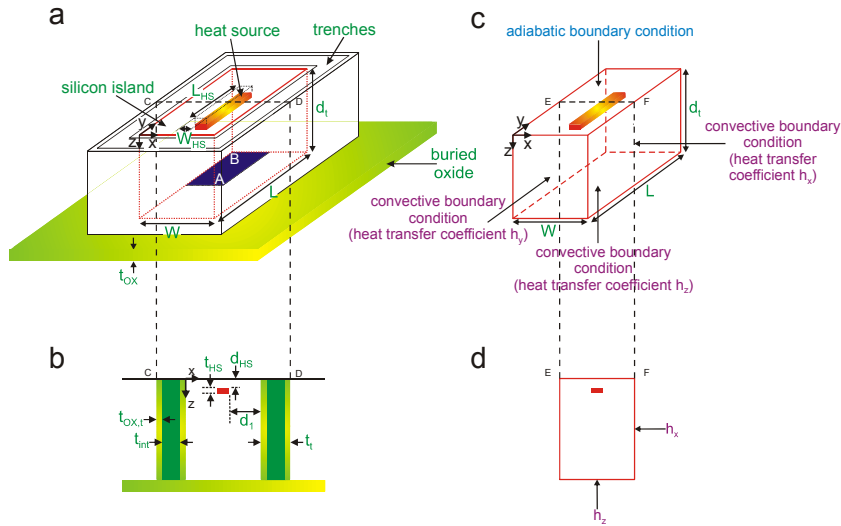
Fig. 2.1. (a) Analyzed trench SOI domain and (b) corresponding cross section; (c) simplified silicon-only domain with convective boundary conditions on lateral and bottom surfaces and (d) related cross section.

The proposed approach requires an adequate choice for the values of heat transfer coefficients associated with the convective conditions, which represent tuning parameters to describe the outward flux through the trench and buried oxide sidewalls in the actual structure. This task was accomplished by resorting to an extensive numerical analysis of the trench SOI structure. Such an investigation has been aimed at achieving a better understanding of the thermal behavior and its dependence upon all relevant geometrical and physical parameters, and deeply studying the heat removal capability of trenches and buried oxide. The analysis is carried out as follows.

A reference structure, with parameter values listed in Table 2.1, was defined. The numerical analyses were performed by varying an assigned parameter and keeping all other parameters constant and equal to the reference ones. All geometrical quantities have been varied, namely, the silicon island width/length, trench depth, buried oxide and trench thickness, and position and geometry of the heat source. The variations were chosen within ranges typical of bipolar technologies (see Table 2.1). The heat source region is represented as a rectangular parallelepiped with length and width equal to those of the emitter window, and vertically coinciding with the base-collector

space charge region. The heat generated by the source is assumed to be due to uniform power dissipation. The trenches have been initially assumed to be entirely filled with silicon dioxide, whose thermal conductivity was chosen to be 1.4×10^{-6} W/μmK (while 1.4×10^{-4} W/μmK was assumed for silicon).

Table 2.1
Geometrical parameters of the trench SOI structure.

parameter	description	reference domain [μm]	variation range [μm]
W	silicon island width	4	$2 \div 20$
L	silicon island length	22	$22 \div 40$
t_t	trench thickness	1	$0.5 \div 1.5$
d_t	trench depth	5.5	$1 \div 10$
t_{OX}	buried oxide thickness	0.4	$0.4 \div 1.2$
$t_{OX,t}$	trench oxide thickness	0.1	—
t_{poly}	thickness of the trench polysilicon layer	$t_t - 2t_{OX,t}$	—
W_{HS}	heat source width	0.5	$0.5 \div 3$
L_{HS}	heat source length	20	$9 \div 21$
t_{HS}	heat source thickness	0.05	—
d_{HS}	heat source depth	0.05	—
d_1	distance between trench and heat source	1.75	$0.25 \div 4.75$ (at W = 10 μm)

2.1.1. Heat transfer coefficient evaluation procedures

In order to study the heat transfer properties of the trench and buried oxide sidewalls, we analyze the corresponding heat transfer coefficient *h*. In fact, as stated before, the heat transfer coefficient describes the surface proneness to transfer heat out of the silicon-only domain (referred to as *silicon island*). For this purpose we followed two different *h* evaluation strategies:

1   *Punctual h*: in this case the heat transfer coefficient is evaluated as

$$h = \frac{f\left(x_P, y_P, z_P\right)}{T\left(x_P, y_P, z_P\right) - T_{AMB}}$$

(2.1)

where $f\left(x_P, y_P, z_P\right)$ and $T\left(x_P, y_P, z_P\right)$ are the heat flux and temperature in the projection of the MGC[4] of the heat source on the top surface, respectively, and T_{AMB} is the ambient temperature.

2 *Averaged h*: in this case the heat transfer coefficient is evaluated as

$$\bar{h} = \frac{\dfrac{1}{S}\int f\left(x, y, z\right) dS}{\dfrac{1}{S}\int T\left(x, y, z\right) dS - T_{AMB}} \tag{2.2}$$

being *S* the area of the surface at which *h* is associated.

2.1.2. Self-heating thermal resistance evaluation: adopted approaches and nomenclature

In our investigation, three approaches are adopted in order to (numerically) evaluate the self-heating thermal resistance R_{TH}:

1. *Punctual R_{TH}* approach: the temperature increase above ambient is evaluated on the projection of the MGC of the heat source on the top surface (see Fig. 2.2a).
2. *Surface-averaged R_{TH}* approach: the temperature increase above ambient is evaluated as an average over a rectangular domain corresponding to the projection of the overall heat source on the top surface (see Fig. 2.2b).
3. *Volume-averaged R_{TH}* approach: the temperature increase above ambient is evaluated as an average over the whole heat source volume (see Fig. 2.2c).

---

[4] MGC is the acronym for mass gravity center (of the heat source). It will be widely used in the following for simplicity.
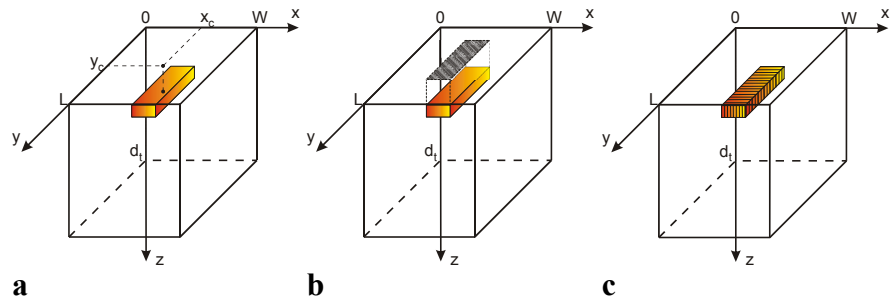
Fig. 2.2. The different approaches adopted for self-heating thermal resistance evaluation: punctual R_{TH} (a); surface-averaged R_{TH} (b); and volume-averaged R_{TH} (c).

Now, let us introduce the nomenclature adopted for the self-heating thermal resistance numerical evaluation:

1. *Actual R_{TH}* is the self-heating thermal resistance of the complete structure with trench and buried oxide layer (see Fig. 2.1a).
2. *Punctual-h R_{TH}* is the self-heating thermal resistance of the "fictitious" reduced silicon domain (see Fig. 2.1c). In this case the heat transfer coefficients are calculated from the values of temperature and heat flux evaluated on the projections of the mass gravity center of the heat source on the (lateral and bottom) faces by simulating the overall actual structure.
3. *Averaged-h R_{TH}* is the self-heating thermal resistance of the "fictitious" reduced silicon domain (see Fig. 2.1c). In this case the heat transfer coefficients are calculated from the averaged temperature and heat flux evaluated on the (lateral and bottom) faces by means of simulations of the overall actual structure.

For each case the self-heating thermal resistance will be evaluated by means of the 3 approaches addressed before.

2.1.3. Buried oxide thickness variation

Let us analyze the influence of the buried oxide thickness on the heat transfer capability of the silicon island sidewalls.

In the reference structure the buried oxide thickness amounts to 0.4 μm. In the analysis presented in this Paragraph such a thickness spans from 0.4 to 1.2 μm (see Table 2.1).

Firstly, the impact on the bottom silicon/buried oxide surface is analyzed.

As evidenced in Fig. 2.3, the proneness of the bottom surface to transfer heat away from the silicon island decreases with increasing buried oxide thickness (which is an intuitive result), both in the *punctual* and in the *averaged* case. Besides, an inspection of the figure reveals that the *punctual h* is lower than the *averaged* one. As will be evidenced in the following, this result holds for all the boundary surfaces in almost all the performed analyses.
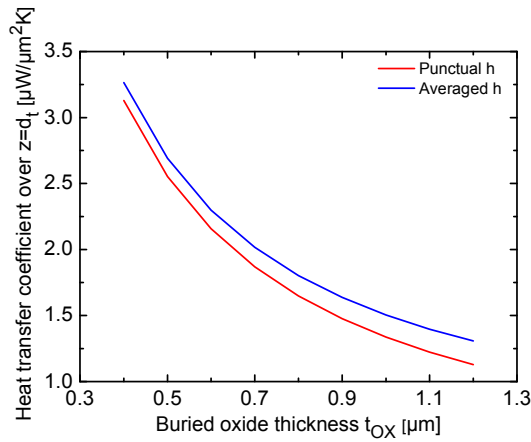
Fig. 2.3. Heat transfer coefficient over the bottom of the silicon island as a function of buried oxide thickness: both the *punctual* (red line) and *averaged* *h* (blue) are depicted.

Fig. 2.4a and b illustrate the temperature distribution over the bottom surface (i.e., the interface at $z = d_t$ between silicon and buried oxide) as obtained through a 3-D FEM simulation of the reference structure ($t_{OX} = 0.4$ μm) and of the structure corresponding to the case of the largest analyzed oxide thickness ($t_{OX} = 1.0$ μm), respectively. A dissipated power density of 20 mW/μm^3 is assumed. Note that due to the inherent symmetry of the structures, only one quarter of the domain has been simulated (see Fig. 2.1a). It is evident that the maximum temperature occurs at the projection of the MGC on the bottom surface (since this is the surface point closest to the heat

source). Furthermore, for $t_{OX} = 1.0$ µm the temperature values are obviously higher than those corresponding to the 0.4 µm case since the heat is more hardly removed from the silicon domain surrounded by oxide.

a   **b**

Fig. 2.4. Temperature distributions over one quarter of the bottom surface of the silicon island as evaluated by numerical simulations for: (a) $t_{OX} = 0.4$ µm, and (b) $t_{OX} = 1.0$ µm.

Fig. 2.5 shows the heat flux distribution over the bottom surface for the two previously analyzed cases.

a   **b**

Fig. 2.5. Heat flux distributions over one quarter of the bottom surface of the silicon island as evaluated by numerical simulations for: (a) $t_{OX} = 0.4$ µm, and (b) $t_{OX} = 1.0$ µm.

As can be seen in Fig. 2.5a, the flux distribution significantly increases in the close proximity of the lateral trenches, while being low (and approximately uniform) far from them. This behavior occurs also by increasing the buried oxide thickness, as evidenced by Fig. 2.5b. Furthermore, a peak is reached on the corner located between trench and buried oxide. This clearly illustrates that this point represents the favorite way for the heat flux to leave the silicon island

within which the active device region is located. It should be noted that the flux distribution over the edge $x = 0$ (which faces the longest heat source side) is higher than that over the edge $y = 0$.

As evidenced in Fig. 2.4 and Fig. 2.5, the buried oxide thickness enlargement results in a flux decrease and temperature increase.

Finally, Fig. 2.6 depicts the h distribution over the bottom surface.

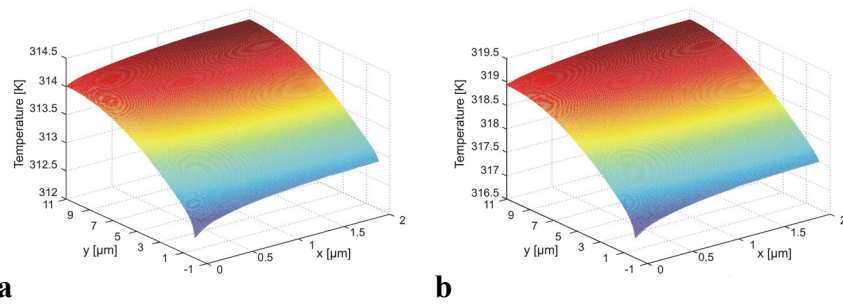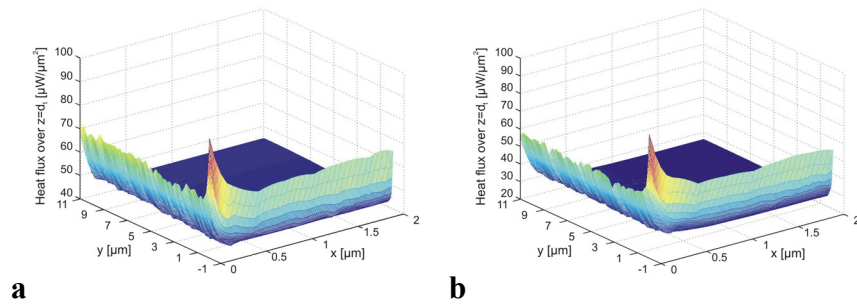**a**   **b**
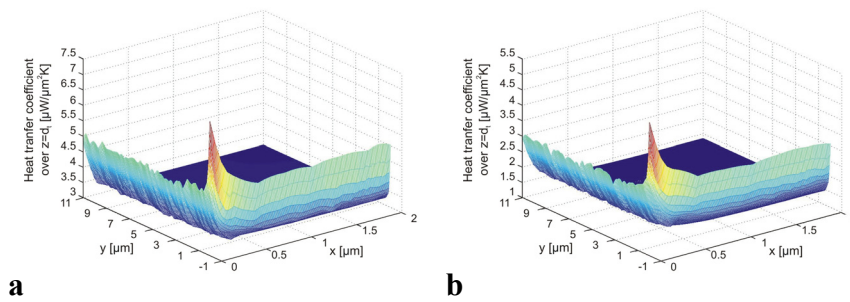
Fig. 2.6. Heat transfer coefficient distributions over one quarter of the bottom surface of the silicon island as evaluated by numerical simulations for: (a) $t_{OX} = 0.4$ μm, and (b) $t_{OX} = 1.0$ μm.

Some observations are in order.

1. A noticeably uneven h distribution arises: such a parameter exhibits a sharp growth along the edges between lateral trenches and buried oxide with a peak in the corner (point B in Fig. 2.1a), while a *plateau* region with a lower and uniform value occurs far away from the borders, due to the balance between the nonuniform heat flux and temperature distributions. It is therefore evidenced that:
    ➤ the heat removal is more effective in correspondence of the boundaries between walls;
    ➤ corners represent the preferential way for the heat to leave the silicon island.
2. This behavior allows clarifying why the *averaged h* value (which accounts for the h distribution nearby the surface borders) is higher than the *punctual h* (which is located well within the *plateau* region).
3. Both the *plateau* values and the border ones decrease with increasing the thickness of the buried oxide. As claimed before, this is a foreseeable behavior, since the bottom surface

more hardly allows the heat propagation toward the substrate for larger t_{OX} values.

Fig. 2.7 shows the *h* behavior over the bottom interface along a cut taken through the center of the bottom surface for two values of buried oxide thickness t_{OX}. As can be seen, the surface capability to transfer heat out of the silicon island reduces by increasing t_{OX}.
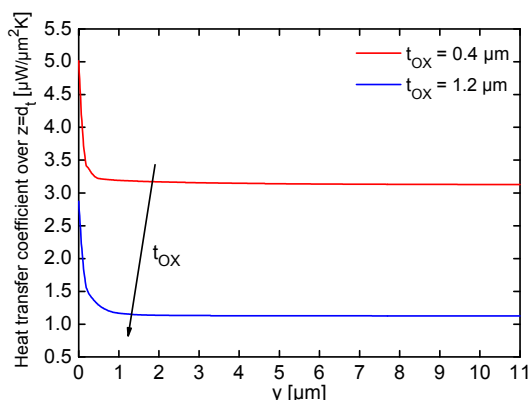
Fig. 2.7. Heat transfer coefficient distribution along length over the bottom surface of the silicon island for two values of buried oxide thickness; the sharp increase in the close proximity of $y = 0$ (i.e., the trench sidewall) is apparent. The cut is taken through the center of the surface.

In Fig. 2.8 the *averaged* and *punctual h* on the lateral faces $x = 0$ and $y = 0$ are reported (the behavior is identical on the opposite walls due to symmetry).
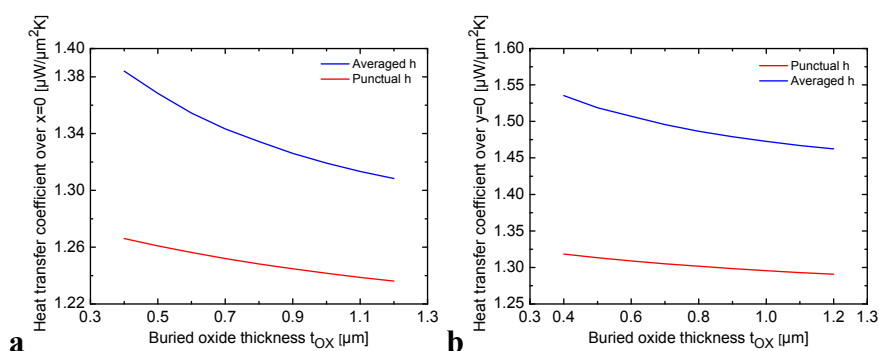
Fig. 2.8. Heat transfer coefficient as a function of buried oxide thickness over lateral sidewalls of the silicon island: (a) $x = 0$, and (b) $y = 0$. Both the *punctual* (red lines) and *averaged h* (blue) are depicted.

In both cases, the heat transfer coefficient slightly reduces with increasing the buried oxide thickness (as shown before, a noticeable variation instead occurs for coefficient h on the $z = d_t$ face). Besides, the *punctual h* is lower than the *averaged* one.

Fig. 2.9a and b illustrate the temperature field over the lateral surface $x = 0$ as obtained through a 3-D FEM simulation of the two structures under analysis (i.e., those with $t_{OX} = 0.4$ μm and $t_{OX} = 1.0$ μm, respectively). The maximum temperature occurs on the top surface at $y = y_c$. Conversely, the minimum value arises on the bottom surface at $y = 0$ (which is the farthest point from the heat source MGC). The temperature obviously attains higher values when the buried oxide is thicker ($t_{OX} = 1.0$ μm in Fig. 2.9b). As we will see, also the heat flux is higher, since the heat flows more easily through the lateral faces than through the bottom surface when the buried oxide thickness increases.

a   **b**
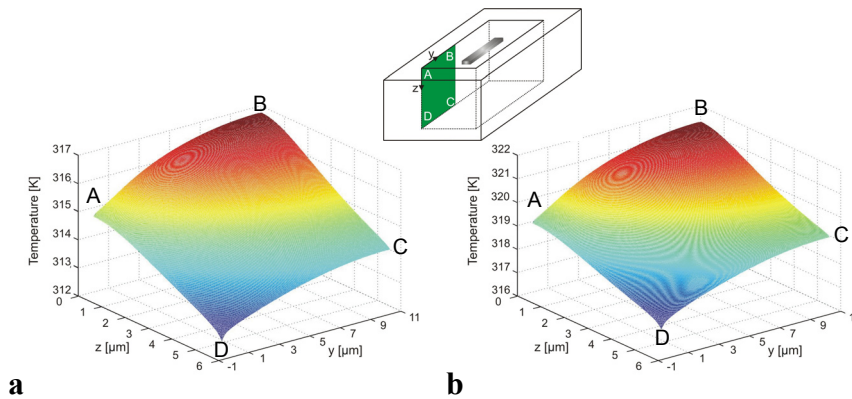
Fig. 2.9. Temperature distributions over half of the lateral surface $x = 0$ (see inset) as evaluated by numerical simulations for: (a) $t_{OX} = 0.4$ μm, and (b) $t_{OX} = 1.0$ μm.

Fig. 2.10 shows the heat flux distribution over the lateral surface $x = 0$ for the same values of buried oxide thickness.

As can be seen, the flux reaches the maximum value where the temperature is minimum, while being low and uniform far from the oxide walls. Similar results are obtained for the $y = 0$ surface.

a   b
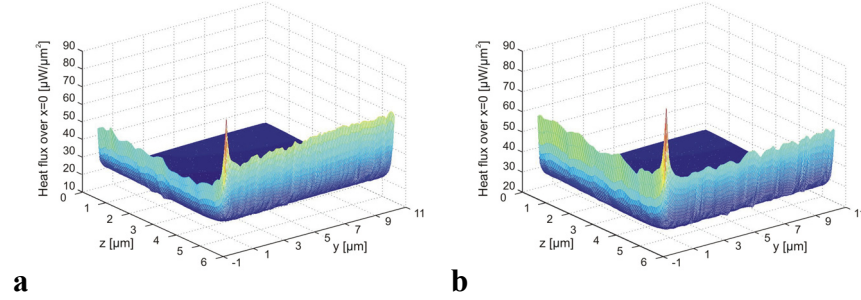
Fig. 2.10. Heat flux distributions over half of the lateral surface $x = 0$ as evaluated by numerical simulations for: (a) $t_{OX} = 0.4$ μm, and (b) $t_{OX} = 1.0$ μm.

Fig. 2.11 shows the heat transfer coefficient distribution over the $x = 0$ surface for buried oxide thicknesses equal to 0.4 μm (Fig. 2.11a) and 1.0 μm (Fig. 2.11b).

a   b
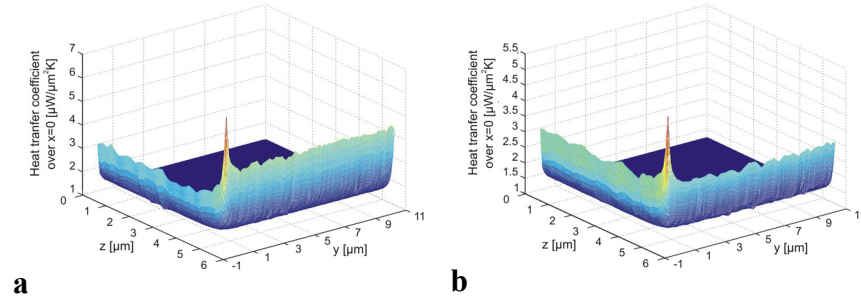
Fig. 2.11. Heat transfer coefficient distributions over half of the lateral surface $x = 0$ as evaluated by numerical simulations for: (a) $t_{OX} = 0.4$ μm, and (b) $t_{OX} = 1.0$ μm.

The following considerations can be drawn:

1. in the *plateau* region (located far from the borders), the heat transfer coefficient values remain almost unchanged, since the features of such a region do not vary in this analysis;
2. in a similar fashion, the heat transfer distribution along the trench-trench edge ($y = 0$) does not change;
3. the h values along the border between the surface and the buried oxide (i.e., $z = d_t$) decrease by increasing the buried oxide thickness: as a consequence, the *averaged h* on the

overall surface (also for the "border" values) lowers with increasing t_{OX}.

Fig. 2.12 details the behavior of the self-heating thermal resistance R_{TH} of the real (complete) domain as the buried oxide thickness t_{OX} increases. As can be seen, R_{TH} increases with t_{OX} since a large oxide thickness makes the heat removal from the heat source harder.
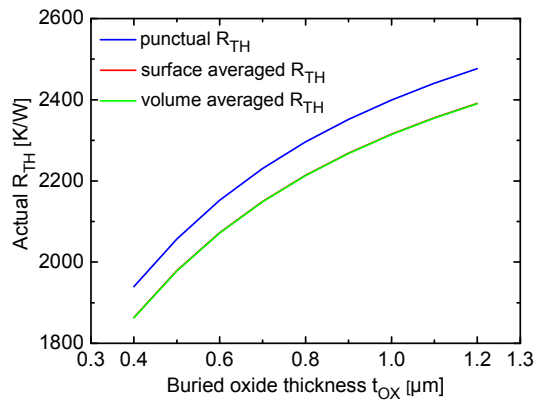
Fig. 2.12. Self-heating thermal resistance of the actual structure. All the introduced approaches for the evaluation of R_{TH} are illustrated: punctual (blue line), surface-averaged (red), and volume-averaged (green).

All the introduced approaches (punctual, surface-, and volume-averaged) are exploited for the evaluation of R_{TH}. The punctual procedure provides larger values, since the temperature increase over ambient spotted in the projection of the MGC is close to the maximum value in the overall domain. It is noteworthy that the surface and volume-averaged strategies give almost identical results due to the heat source proximity with the top silicon surface and the thin heat source height.

Fig. 2.13 depicts the behavior of the punctual (a), surface- (b), and volume-averaged (c) R_{TH} as t_{OX} increases. A comparison is performed between the thermal resistances of (i) the actual structure (blue curves), (ii) the fictitious reduced silicon domain with convective b.c. determined by the h values extracted at the MGC projections (green curves), and (iii) the fictitious domain with b.c. established by the *averaged h* (red curves). Let us note that the geometry of heat source and silicon domain surrounded by oxide remains unchanged as the buried oxide thickness changes; as a consequence, the thermal

behavior of the fictitious structures only depends on the *h* values adopted for the convective b.c.. Fig. 2.13 shows that, independently of the approach adopted to evaluate the self-heating thermal resistance, the *punctual-h* R_{TH} noticeably overestimates the actual thermal resistance (the error amounts to around 7%), while the *averaged-h R_{TH}* provides an excellent agreement (a maximum error of 0.7% is found). It will be shown that such a discrepancy reduces when the b.c. influence on the self-heating thermal resistance decreases (i.e., for low t_{OX} values).

a   **b**   **c**
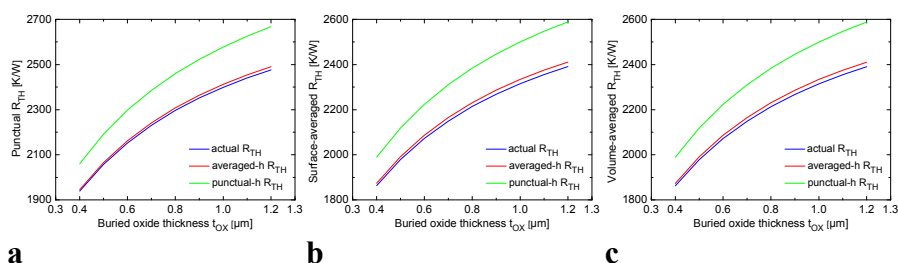
Fig. 2.13. The exploited approaches for the evaluation of R_{TH} are depicted: (a) punctual, (b) surface-averaged, and (c) volume-averaged. For all the approaches the self-heating thermal resistance of the actual structure (blue lines), the *averaged-h* (red), and *punctual-h* (green) R_{TH} are reported.

The following figures show the temperature increase over ambient $\Delta T(x,y,z)$ normalized to dissipated power P_D[5] along the *x*, *y*, and *z* axis as a function of buried oxide thickness.

In the real domain the normalized temperature field can be numerically evaluated in the silicon island, oxide layers (both trenches and buried oxide), and silicon substrate. Conversely, in the fictitious cases (both for the *punctual* and *averaged h*), such a quantity is – obviously – defined only in the silicon island.

The analysis is performed for three t_{OX} values, i.e., 0.4, 0.8, and 1.2 µm, respectively.

Fig. 2.14 provides the normalized temperature distribution in the actual (complete) domain over the top surface ($z = 0$) for $y = y_c$.

As can be observed, it rapidly decreases over the oxide trench, due to the extremely low (1.4×10^{-6} W/µmK) thermal conductivity of the oxide itself. Furthermore, a figure inspection shows that the

---

[5] Such a quantity can be reviewed as a thermal resistance field, and is only dependent upon the geometric and material parameters of the analyzed domain.

normalized temperature distribution tends to be flat nearby the oxide trench interface, that is, such a surface is almost adiabatic.
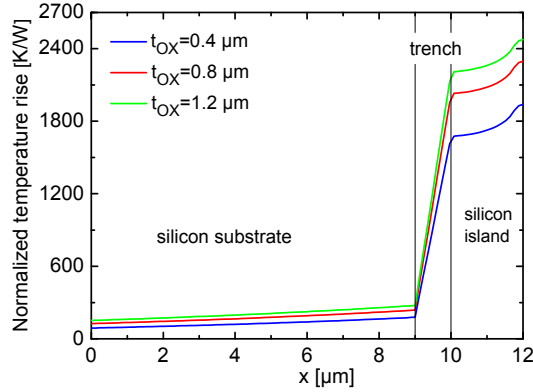
Fig. 2.14. Numerically evaluated normalized temperature distribution of the actual structure along *x* over the top surface for three values of buried oxide thickness: 0.4 µm (blue line), 0.8 µm (red), and 1.2 µm (green). The cut is taken through the MGC heat source projection on the top surface.

Fig. 2.15 illustrates the normalized temperature field along the *x* axis within the silicon island for the same t_{OX} values (0.4, 0.8, and 1.2 µm). For each thickness value, a comparison is performed between the normalized temperature fields of (i) the actual structure (blue curves), (ii) the fictitious reduced silicon domain with convective b.c. determined by the *h* values extracted on the MGC projections (green curves), and (iii) the fictitious domain with b.c. established by the *averaged h* (red curves).

a　　　　　　**b**　　　　　　**c**
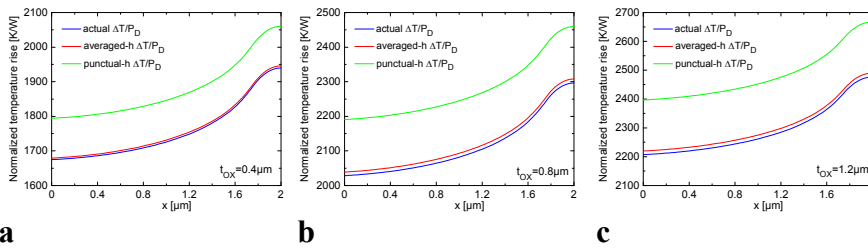
Fig. 2.15. Normalized temperature fields along *x* over the top surface for three values of buried oxide thickness: (a) 0.4 µm, (b) 0.8 µm, and (c) 1.2 µm. The temperature is evaluated numerically by 3-D FEM simulations: for the actual structure (blue lines), through the *averaged-h* approach (red), and the *punctual-h* one (green). The cut is taken through the projection of the MGC of the heat source on the top surface.

As can be observed, the *punctual-h* normalized temperature rise significantly overestimates the actual one, while the *averaged-h* temperature provides an admirable agreement also in these cases. Note that the discrepancies between the fictitious *punctual h* and *averaged h* cases with the actual ones are almost independent of the t_{OX} value.

3-D numerical simulations also proved that the normalized temperature behavior along the y axis is quite similar to the one along the x axis.

Fig. 2.16 provides the normalized temperature distribution in the actual domain along z over a straight line that crosses the MGC as evaluated through 3-D numerical simulations. An insight into the normalized temperature behavior within the silicon substrate reveals that the thinner t_{OX}, the higher the temperature distribution, since the heat spreads more effectively toward the substrate itself.
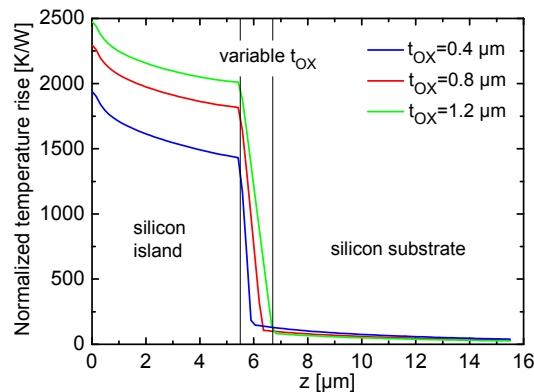
Fig. 2.16. Numerically evaluated normalized temperature distribution of the actual structure along z through the MGC of the heat source for three values of buried oxide thickness: 0.4 μm (blue line), 0.8 μm (red), and 1.2 μm (green).

Fig. 2.17 illustrates once more the normalized temperature field along the z axis within the silicon island for t_{OX} equating 0.4, 0.8, and 1.2 μm, respectively. All considerations are similar to those expressed for the behavior along the x axis.
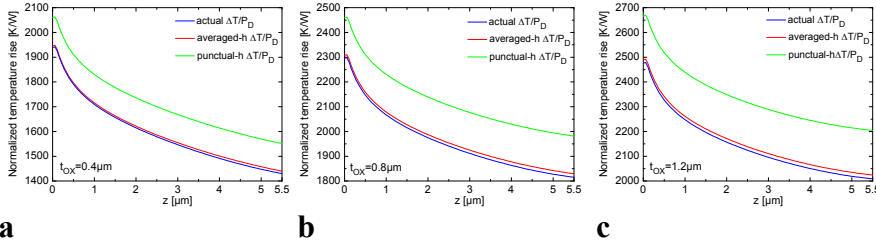
Fig. 2.17. Normalized temperature fields along *z* through the MGC of the heat source for three values of buried oxide thickness: (a) 0.4 µm, (b) 0.8 µm, and (c) 1.2 µm. The temperature is evaluated numerically by 3-D FEM simulations: for the actual structure (blue lines), through the *averaged-h* approach (red), and the *punctual-h* one (green).

2.1.4. Trench depth variation

Now, let us analyze the influence of the trench depth on the heat transfer capability of the silicon island sidewalls.

In the reference structure the trench depth (i.e., the depth of the interface between silicon island and buried oxide) amounts to 5.5 µm. In this investigation such a quantity spans from 1.0 to 10 µm (see Fig. 2.18)
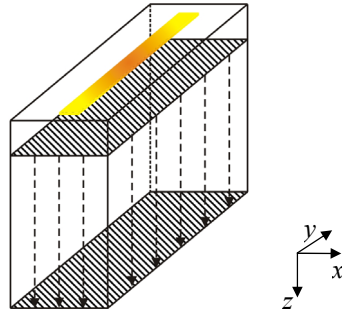
Fig. 2.18. Trench depth variation in the simplified domain.

It is to be noted that – contrarily to the former analysis – the area of the surfaces corresponding to $x = 0$ and $y = 0$ varies (that is, it increases with increasing the trench depth). By converse, the area of the surface $z = d_t$ (d_t changing from 1.0 to 10 µm) remains constant.

As concerns the lateral sidewalls, numerical simulations evidenced that:

➢ for any d_t:

1. the maximum temperature is reached on the MGC projection, while the minimum is located in correspondence of the corners between trench and buried oxide layer;

2. the heat flux increases toward the surface boundaries (particularly high values are reached at the interface with the buried oxide), whereas it is low and almost uniform far from such boundaries;

3. the heat transfer coefficient rapidly grows nearby the wall boundaries reaching a maximum where the temperature is minimum (i.e., at trench-buried oxide corners), while being constant elsewhere. Again, this *plateau* can be explained by considering that, far from the edges, the surface exhibits everywhere uniform features, and, therefore, an uniform proneness to transfer heat;

➢ as the trench becomes deeper (i.e., d_t increases):

1. the temperature values diminish due to the larger silicon volume surrounded by oxide that facilitates the heat spreading;

2. the heat flux distribution reaches lower values, since the silicon domain enlarges and the outgoing heat for unit area decreases;

3. the *plateau* value of the heat transfer coefficient (which coincides with the *punctual h*) remains unchanged, nearly independent of the trench depth, since the features of the "internal" wall portion do not vary;

4. the *h* values along the borders are almost constant, since also the border features do not change;

5. the area of the regions nearby the borders where coefficient *h* rapidly increases remains unchanged.

On the basis of these observations, we can easily explain the *punctual* and *averaged h* behavior (red and blue lines in Fig. 2.19a and b, respectively) of the heat transfer coefficient over lateral sidewalls of the silicon island as a function of trench depth.
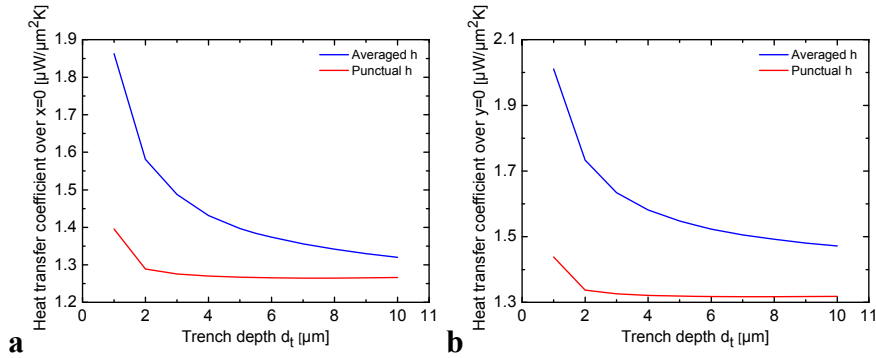
Fig. 2.19. Heat transfer coefficient as a function of trench depth over lateral sidewalls of the silicon island: (a) $x = 0$, and (b) $y = 0$. Both the *punctual* (red lines) and *averaged h* (blue) are depicted.

As can be seen:

1. the *averaged h* decreases with increasing trench depth (rapidly for low depth values and slowly for high ones) and tends to the *plateau* value; the region where h sharply increases is indeed characterized by same area and coefficient values, while the *plateau* area enlarges and plays a more important role;
2. the *punctual h*, on the contrary, remains almost unchanged over the whole trench depth range;
3. also in this analysis, the *punctual h* is lower than the *averaged* one, even if the discrepancy reduces for large trench depth values.

As concerns the bottom surface ($z = d_t$), numerical simulations evidenced that:

1. the maximum temperature is located on the MGC projection (i.e., the center of the silicon island/buried oxide interface), while the minimum occurs in the corner between trench and buried oxide layer;
2. the flux is larger on the surface boundaries while being low and almost constant far from them;
3. with increasing trench depth, the silicon island volume enlarges so that the temperature peak lowers;
4. the heat transfer coefficient distribution remains almost identical on the overall surface as trench depth changes, since

both area and features of the bottom surface are insensitive to buried oxide depth and consequently also the proneness of the surface itself to transfer heat outside does not vary. Therefore both *punctual* and *averaged h* are expected to be almost constant over all the range of trench depth as substantiated by Fig. 2.20.

Fig. 2.20 shows the *punctual* and *averaged h* behavior as a function of trench depth over the bottom surface (silicon/buried oxide interface).

It can be plainly seen that:

1. also in this analysis, the *averaged h* is larger than the *punctual* one;
2. the *punctual h* raises for small trench depths. This can be intuitively explained as follows: when the bottom interface is extremely close to the heat source bottom, a localized "hill" in the *h* distribution arises over the heat source projection on the bottom surface and the hill peak increases with lowering trench depth (and, therefore, reducing the vertical spacing between heat source and bottom interface).
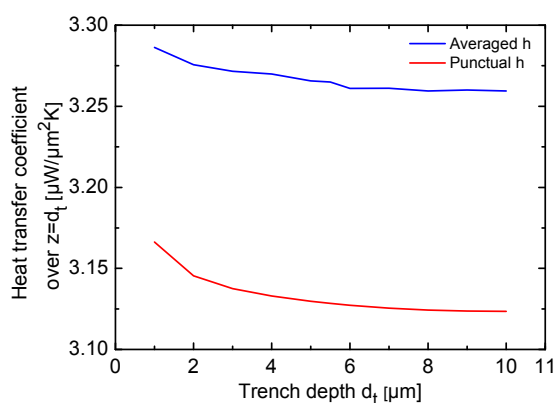
Fig. 2.20. Heat transfer coefficient as a function of trench depth over the bottom surface of the silicon island. Both the *punctual* (red line) and *averaged h* (blue) are depicted.

An interesting phenomenon was noted as the trench depth increases. Let us consider $d_t = 10$ µm. Fig. 2.21 depicts the heat flux distribution over the lateral sidewall $x = 0$ of the silicon island.
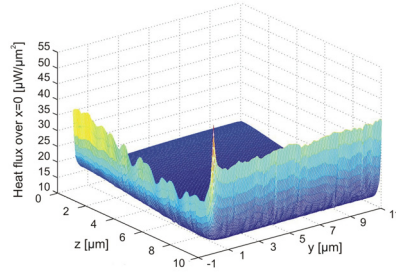
Fig. 2.21. Heat flux distribution over half of the lateral surface of the silicon island $x = 0$ as evaluated by numerical simulations for $d_t = 10$ µm.

As one can see, far from the lateral and bottom borders, the heat flux distribution is not uniform any longer (there is no *plateau* region), but decreases with increasing distance from the top surface. This mechanism can be explained as follows: the heat generated from the active device (which is located in the close proximity of the top surface) reaches more easily the lateral sidewalls that are nearer to the heat source itself.

As concerns the heat transfer coefficient distribution, the usual expected behavior is detected: h sharply increases nearby the wall borders (reaching a maximum in the corner), while being constant elsewhere.

Fig. 2.22 shows the behavior of the self-heating thermal resistance R_{TH} of the actual domain as the trench depth d_t increases.
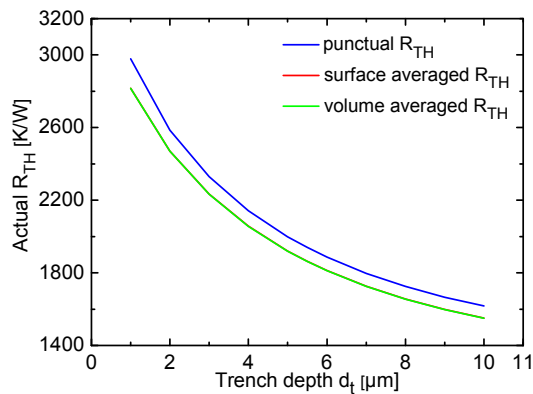
Fig. 2.22. Self-heating thermal resistance of the actual structure vs. trench depth. All the introduced approaches for the evaluation of R_{TH} are depicted: punctual (blue line), surface-averaged (red), and volume-averaged (green).

As can be seen, R_{TH} reduces with d_t since the silicon domain becomes larger, thus making the heat removal from the region surrounding the heat source easier.

All the approaches (punctual, surface-, and volume-averaged) are exploited for the evaluation of R_{TH}. Also in this analysis:

1. the punctual R_{TH} provides larger values than the other ones, since the temperature ΔT at the MGC projection is close to the maximum ΔT value in the overall domain;
2. the surface- and volume-averaged R_{TH} exhibit almost identical values. For this reason in the following investigations only the surface-averaged R_{TH} will be analyzed.

Fig. 2.23 depicts the behavior of the punctual (a) and surface-averaged (b) R_{TH} as d_t increases. A comparison is performed between the thermal resistances of (i) the actual structure (blue curves), (ii) the fictitious reduced silicon domain with convective b.c. determined by the h values extracted in the MGC projections (green curves), and (iii) the fictitious domain with b.c. established by the *averaged h* (red curves).
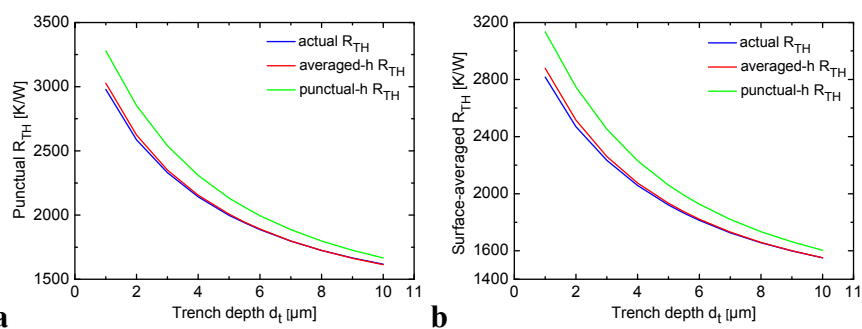
Fig. 2.23. The exploited approaches for the evaluation of R_{TH} are depicted: (a) punctual, and (b) surface-averaged. For all the analyzed approaches the self-heating thermal resistance of the actual structure (blue lines), the *averaged-h* (red), and *punctual-h* (green) R_{TH} are reported.

As can be seen, the *punctual-h R_{TH}* significantly overestimates the actual thermal resistance for low/medium trench depth values, while the *averaged-h R_{TH}* provides an excellent agreement. However, as lucidly discussed before, the *averaged h* approaches the *punctual h* for deeper trenches. As a consequence, adopting *punctual h* boundary conditions for the fictitious case for relatively deep silicon islands does not lead to significant inaccuracy any longer.

2.1.5. Trench thickness variation

Let us investigate the effect of the trench thickness on the device thermal behavior. In the reference domain, the trench thickness amounts to 1 μm. In this analysis such a thickness spans from 0.5 to 1.5 μm.

Fig. 2.24 details the h behavior over the $x = 0$, $y = 0$ and $z = d_t$ walls, respectively.

a   **b**   **c**
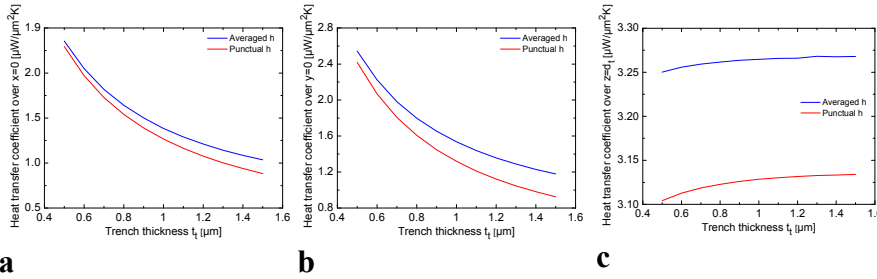
Fig. 2.24. Heat transfer coefficient as a function of trench thickness over the silicon island sidewalls: (a) $x = 0$, (b) $y = 0$, and (c) $z = d_t$. Both the *punctual* (red lines) and *averaged h* (blue) are depicted.

As can be seen, the proneness of the lateral surfaces to transfer heat outside the silicon domain decreases with increasing trench thickness, both in the *punctual* and in the *averaged* case (see Fig. 2.24a and b). Furthermore, the *punctual h* reduction in function of trench thickness is slightly faster than the *averaged h* one. This is due to the fact that the *punctual h* refers only to the *plateau* region that substantially depends on trench thickness. On the contrary, the *averaged h* also accounts for the wall features along the bottom edge which are also affected by the buried oxide thickness, that does not change in this analysis. As a consequence, coefficient h on this edge, and therefore also the *averaged h*, reduces with a slightly lower rate than that corresponding to the *plateau* region (i.e., the *punctual h*).

Fig. 2.24c shows that the *averaged* (blue line) and *punctual* (red) heat transfer coefficients on the bottom surface are almost independent of the trench thickness variation. This behavior was expected since in this analysis the area and the other features of such

surface are kept constant, so that its proneness to transfer heat outside (which determines the h value) does not basically change.

Fig. 2.25 depicts the behavior of the punctual (a) and surface-averaged (b) R_{TH} as t_t increases. A comparison is performed between the thermal resistances of (i) the actual structure (blue curves), (ii) the fictitious reduced silicon domain with convective b.c. determined by the h values extracted in the MGC projections (green curves), and (iii) the fictitious domain with b.c. established by the *averaged h* (red curves). It can be seen that R_{TH} increases with trench thickness since a larger oxide thickness makes the heat removal harder.
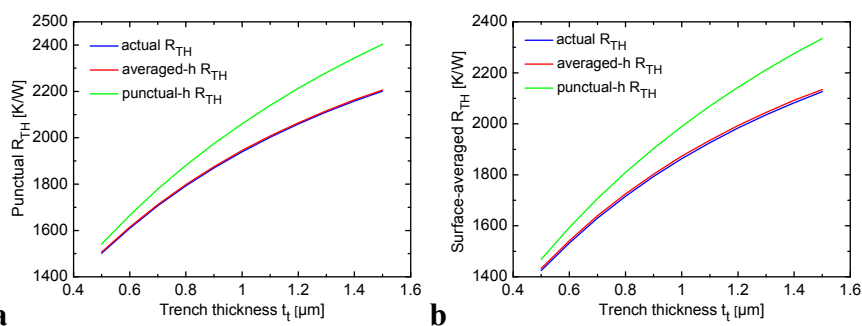
Fig. 2.25. The employed approaches for the evaluation of R_{TH} are depicted: (a) punctual, and (b) surface-averaged. For all the approaches the self-heating thermal resistance of the actual structure (blue lines), the *averaged-h* (red), and *punctual-h* (green) R_{TH} are reported.

Note that, like in the analysis concerning the buried oxide thickness variation, the geometry of the silicon domain surrounded by oxide is kept constant as the trench thickness changes. As a consequence, the thermal behavior of the fictitious structures only depends on the h values adopted for the convective boundary conditions.

Another interesting effect that should be highlighted is that the *punctual-h* R_{TH} increases faster than the *averaged-h* one, thus leading to a larger and larger discrepancy with respect to the actual R_{TH}, while the *averaged-h* R_{TH} provides a perfect agreement. In fact, as it was explained, the *punctual h* grows faster that the *averaged h* (see Fig. 2.24) since the latter includes the unchanging influence of the buried oxide. As a consequence, the *punctual-h* R_{TH} more and more overestimates the actual (and *averaged-h*) R_{TH}, thus leading to an increasing inaccuracy as the trench thickness increases.

Fig. 2.26a provides the normalized temperature distribution in the

actual domain through the MGC projection on the top surface as evaluated through 3-D numerical simulations. As can be seen, the normalized temperature field rapidly decreases over the oxide trench (due to the extremely low thermal conductivity of the oxide). Furthermore, the thinner the trench thickness, the higher the normalized temperature field in the silicon substrate, since the heat spreads more effectively toward the substrate itself through the trench. On the contrary, along z axis, the normalized temperature distribution outside the silicon island is larger for larger trench thickness, since for larger trench thickness, the heat tends to spread more and more through the buried oxide (which is characterized – as repeatedly mentioned – by unchanging features in this investigation). This is evidenced in Fig. 2.26b that depicts the normalized temperature field over a straight line that crosses the mass gravity center.
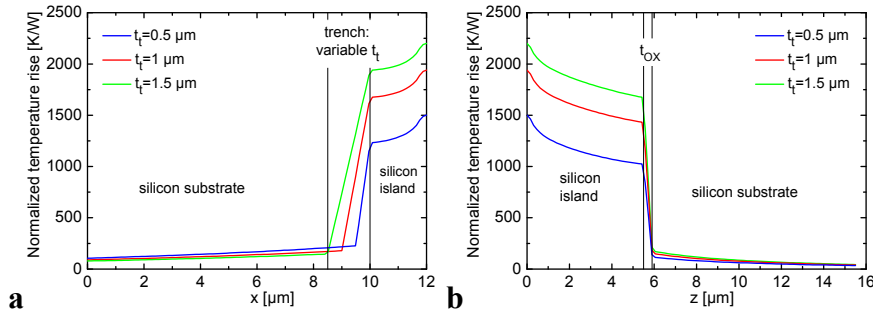
Fig. 2.26. Normalized temperature field in the actual structure (a) along x and (b) z axes for three values of trench thickness: 0.5 µm (blue lines), 1 µm (red), and 1.5 µm (green). (a) is taken on the top surface for $y = y_c$ while (b) through the MGC heat source.

2.1.6. Silicon island size variation

Let us analyze the influence of the silicon island width (Fig. 2.27a) and length (Fig. 2.27b) on the heat transfer capability of the silicon island sidewalls.

In the reference domain the silicon island width W and length L amount to 4 and 22 µm, respectively. In our analysis, these parameters vary from 2 to 20 µm and from 22 to 40 µm, respectively.

Note that the area of the surfaces $y = 0$ ($x = 0$) and $z = d_t$ enlarges with increasing the silicon island width W (length L). On the contrary,

the area of the surface $x = 0$ ($y = 0$) remains constant.

a   **b**
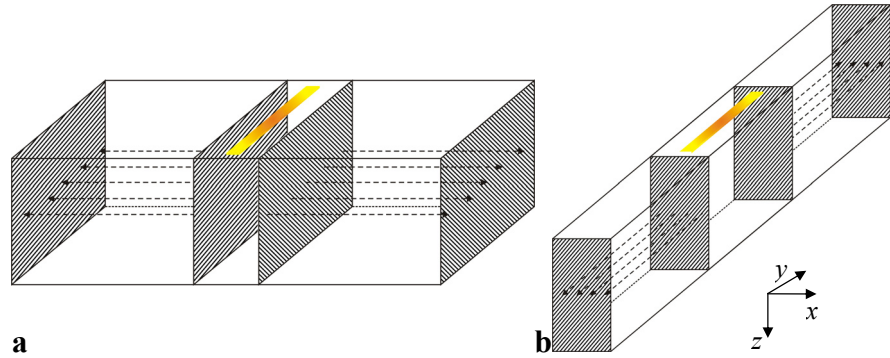
Fig. 2.27. Silicon island width (a) and length (b) variations.

In Fig. 2.28 the behavior of *averaged* and *punctual h* in function of the silicon island width (i.e., the distance between trenches along x) and length (i.e., the distance between trenches along y) on the bottom surface $z = d_t$ and lateral surfaces $y = 0$ and $x = 0$, respectively, are investigated.
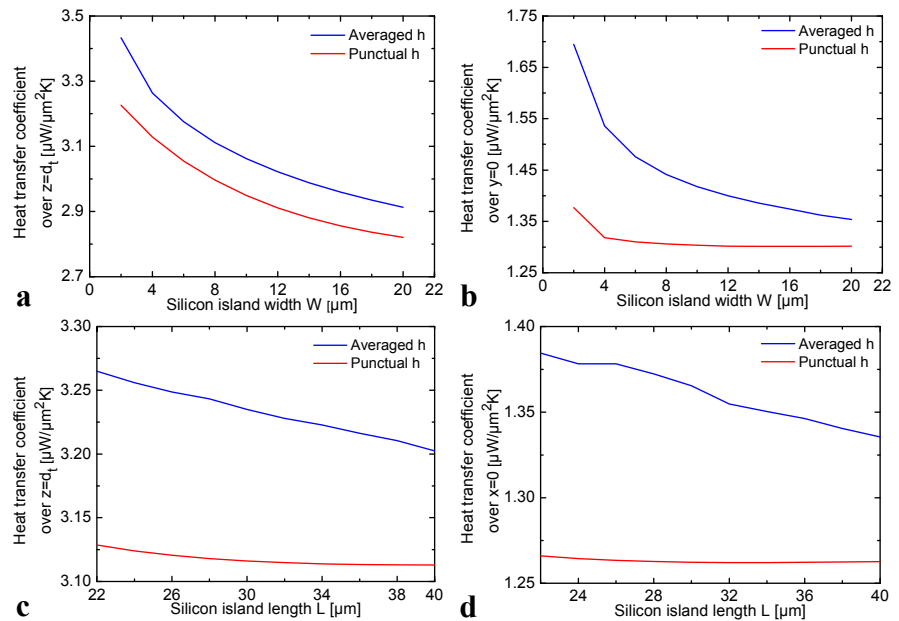
Fig. 2.28. Heat transfer coefficient over the sidewalls (a) $z = d_t$, and (b) $y = 0$ as a function of silicon island width, and over the sidewalls (c) $z = d_t$, and (d) $x = 0$ as a function of silicon island length. Both the *punctual* (red lines) and *averaged h* (blue) are depicted.

Let us focus on the case in which *W* changes (Fig. 2.28a and b). In this case, the *averaged h* (blue lines) decreases with increasing the silicon island width (rapidly for low values and slowly for high ones), while the *punctual h* (red lines) decreases only over $z = d_t$ (Fig. 2.28a). In fact, by increasing the silicon island width, the physical features of the trench sidewalls $z = d_t$ and $y = 0$ remain unchanged so that the *h* value on the MGC projection (i.e., on the center of the *plateau* zone) does not vary. On the contrary, the area of these surfaces enlarges leading to a reduction of the *medium h* since the *plateau* region (characterized by a lower *h* value) plays a more important role.

Fig. 2.29a shows the *punctual* (red line) and *averaged* (blue) *h* behavior over the sidewalls $x = 0$ in function of the silicon island width. As can be seen, both *h* values decrease. In particular, the *averaged h* reduces slowly while the *punctual* one rapidly for low values and slowly for high ones. The *averaged h* slow reduction is due to the fact that in this analysis the area and the other features of the surface are kept constant, so that its proneness to transfer heat outside does not significantly change. The *punctual h* behavior, instead, can be easily explained as follows. When the silicon island width is short, the $x = 0$ wall is close to the long heat source side. This implies the occurrence of a localized *h* hill over the projection of the heat source on the surface itself, which makes the *punctual h* higher. Since all the border features do not vary in this analysis, the *h* distribution remains unchanged along the wall edge, so that the hill occurrence influences significantly the *punctual h*, which increases when reducing the width, and inappreciably the *averaged h* value, which is almost constant.
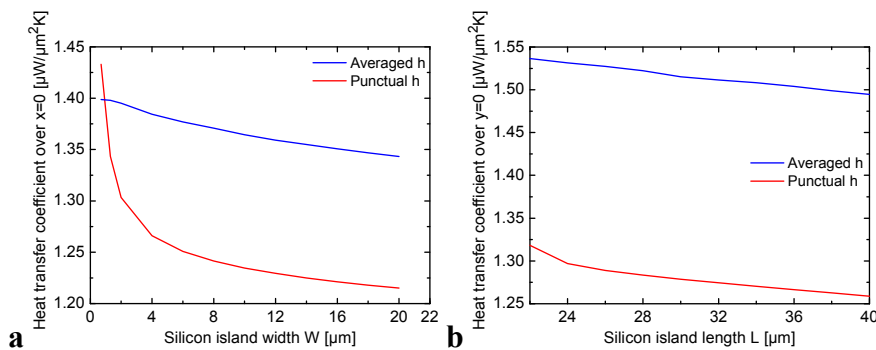
Fig. 2.29. Heat transfer coefficient over the sidewalls (a) $x = 0$ and (b) $y = 0$ as a function of silicon island width and length, respectively. Both the *punctual* (red lines) and *averaged h* (blue) are depicted.

Analogous considerations can be made for the *h* behavior as the silicon island length varies (Fig. 2.28c and d and Fig. 2.29b).

Fig. 2.30 depicts the behavior of the punctual (Fig. 2.30a and c) and surface-averaged (Fig. 2.30b and d) R_{TH} as *W* and *L* increase. A comparison is performed between the thermal resistances of (i) the actual structure (blue curves), (ii) the fictitious reduced silicon domain with convective b.c. determined by the *h* values extracted in the MGC projections (green curves), and (iii) the fictitious domain with b.c. established by the *averaged h* (red curves).
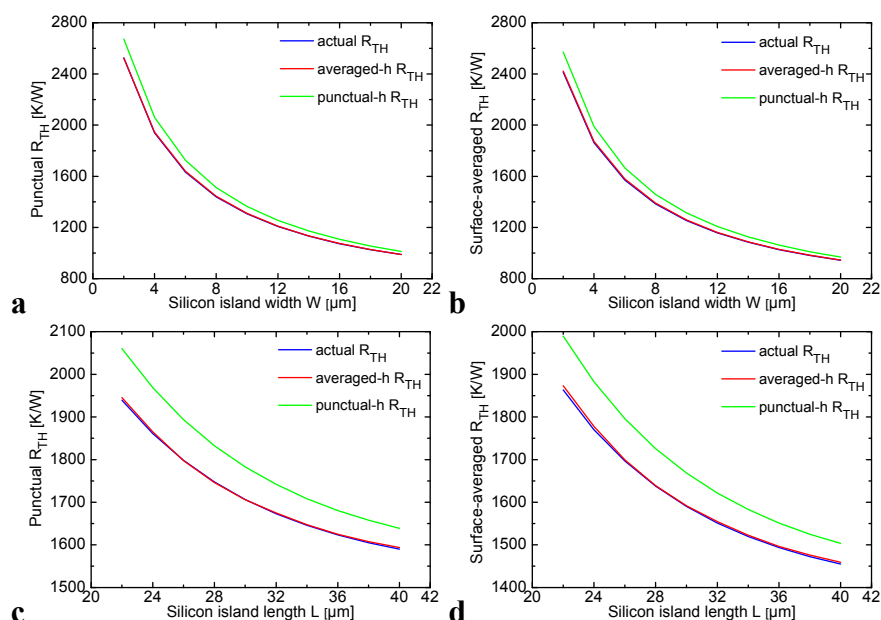
Fig. 2.30. The exploited approaches for the evaluation of R_{TH} are illustrated: (a) and (c) punctual as a function of silicon island width and length, respectively, and (b) and (d) surface-averaged. For all the analyzed approaches the self-heating thermal resistance of the actual structure (blue lines), the *averaged-h* (red), and *punctual-h* (green) R_{TH} are reported.

It can be observed that:

1. R_{TH} decreases with silicon island width and length since the silicon domain volume becomes larger, thus making the heat removal from the heat source easier;
2. also in this analysis the *punctual-h* R_{TH} significantly overestimates the actual thermal resistance, while the *averaged-h* R_{TH} guarantees an excellent agreement;

3. the higher the silicon island size (i.e., as width and length increase), the lower the discrepancy between the *punctual-h* R_{TH} and the actual one due to a twofold reason: (1) the *averaged h* on the changing-area surfaces (i.e., $y = 0$ and $z = d_t$ when *W* changes, and $x = 0$ and $z = d_t$ when *L* changes) decreases with increasing the domain size, so that the error generated by the low *punctual h* values is lower; (2) the error due to the *punctual h* corresponding to $x = 0$ and $y = 0$ (as width and length change, respectively) plays a lower and lower role, since such boundaries are moving far from the heat source.

2.1.7. Heat source size variation

Let us now investigate the effects of heat source width and length (clarified in Fig. 2.31a and b respectively).
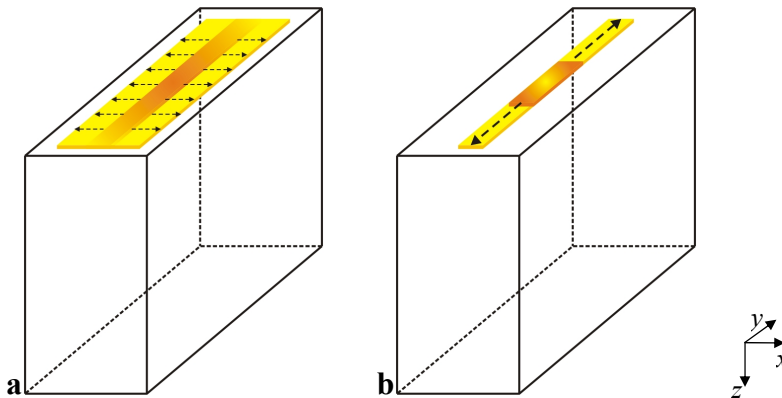
Fig. 2.31. Heat source width (a) and length (b) variations.

In the reference structure, the heat source width and length amount to 0.5 and 20 µm, respectively. In this analysis such quantities span from 0.5 to 3 µm and from 9 to 21 µm, respectively.

The investigation is performed by adjusting the volumetric power density in order to keep the total dissipated power constant.

The behavior of the *punctual* and *averaged* heat transfer coefficients as heat source width changes is depicted in Fig. 2.32. It is evident that both the *averaged* (blue lines) and the *punctual h* (red) are almost independent of heat source width. This can be explained by the

fact that the area and the other features of the boundary surfaces are constant in this investigation, so that their proneness to transfer heat outside does not considerably change. Moreover, it can be observed that, also in this case, the *punctual h* is lower than the *averaged* one.
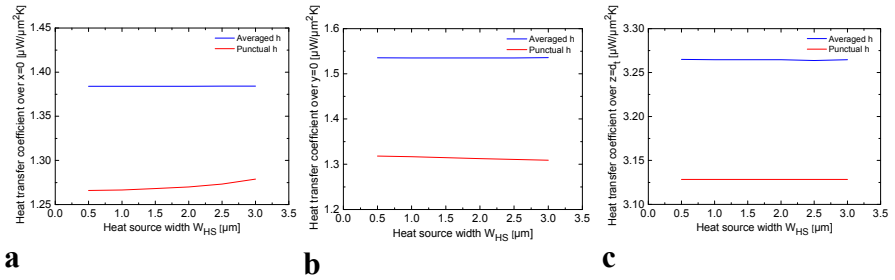
Fig. 2.32. Heat transfer coefficient as a function of heat source width over the silicon island sidewalls: (a) $x = 0$, (b) $y = 0$, and (c) $z = d_t$. Both the *punctual* (red lines) and *averaged h* (blue) are depicted.

The slight increase of the *punctual h* with source width on the wall $x = 0$ (see red line in Fig. 2.32a) is basically due to the reduction of the spacing between the long heat source side and the wall itself that produces a localized *h* increase. Conversely, a small reduction in *punctual h* over $y = 0$ is observed, due to the short heat source side enlargement by keeping constant the distance from the surface itself.

Analogous results were achieved for the heat source length variation. In this case, when the heat source length raises, a slight increase is observed in the *punctual h* evaluated on surface $y = 0$, since the short side of the heat source approaches it. This behavior could be explained as follows. In principle, the heat transfer coefficient distribution over surface $y = 0$ should be independent of the heat source length (the features of such a surface do not vary indeed). However, the numerical simulation results show a somewhat different behavior: when the short side of the heat source is extremely close to the wall, the outgoing heat flux evaluated over the area corresponding to the heat source side projection on the wall grows faster than the temperature increase above ambient, that is, coefficient *h* over such a circumscribed area becomes higher than in the remaining *plateau* region. Such a mechanism enhances with decreasing the distance between heat source edge and wall.

Fig. 2.33 depicts the behavior of the punctual (a) and surface-averaged (b) R_{TH} as the active region width chances. A comparison is

performed between the thermal resistances of (i) the actual structure (blue curves), (ii) the fictitious reduced silicon domain with convective b.c. determined by the *h* values extracted in the MGC projections (green curves), and (iii) the fictitious domain with b.c. established by the *averaged h* (red curves). As can be seen, R_{TH} decreases due to the volume enlargement of the dissipating region.
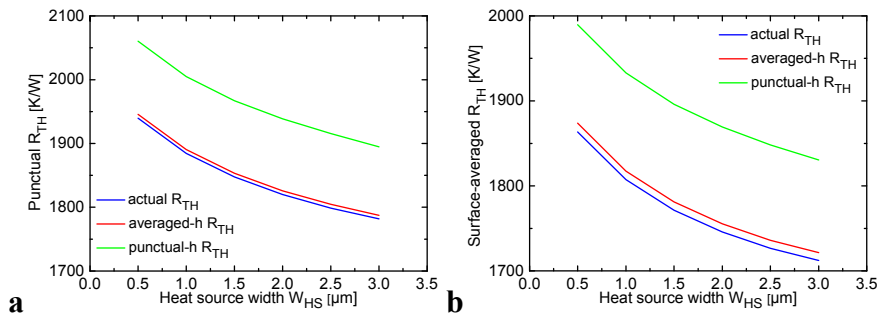
Fig. 2.33. The adopted approaches for the evaluation of R_{TH} as a function of the heat source width are depicted: (a) punctual, and (b) surface-averaged. For all the analyzed approaches the self-heating thermal resistance of the actual structure (blue lines), the *averaged-h* (red), and *punctual-h* (green) R_{TH} are reported.

Fig. 2.34 provides the normalized temperature distribution in the real domain over the top surface through the MGC heat source projection (i.e., for $z = 0$ and $y = y_c$) for heat source width equal to 0.5, 2.0, and 3.0 μm, respectively.
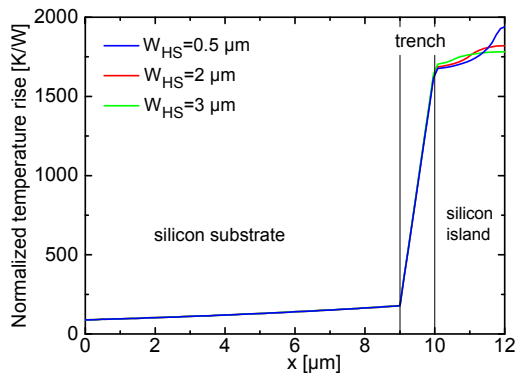
Fig. 2.34. Numerically evaluated normalized temperature distribution of the actual structure along *x* for three values of heat source width: 0.5 μm (blue line), 2 μm (red), and 3 μm (green). The cut is taken through the MGC heat source projection on the top surface.

It must be noted that the normalized temperature on the silicon-trench border increases by increasing the source width (green curve), since the heat emerges easily out of the generating region.

Analogous results were obtained by increasing the heat source length.

2.1.8. Variation of the heat source position along x axis

The influence of the distance between trench and heat source (along x axis) is investigated (Fig. 2.35). It is noteworthy that the reference domain has been properly modified by increasing the silicon island width (up to 10 μm) to allow a wide heat source "movement" along x. The distance between the silicon/trench interface and the heat source edge along x spans from 0.25 to 4.75 μm.
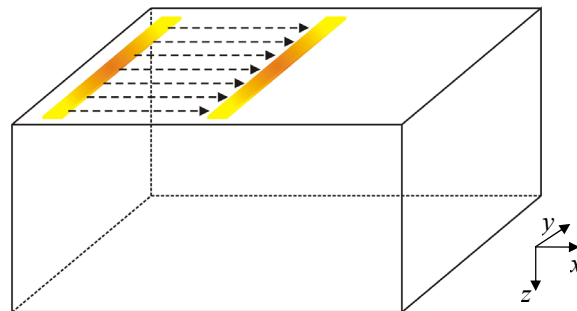
Fig. 2.35. Silicon/trench interface - heat source distance variation.

Since the symmetry along x does not hold any longer, half a domain has been simulated.

Firstly, the impact on the lateral faces $x = 0$ and $x = W$ is analyzed.

As evidenced in Fig. 2.36a, the *averaged h* (blue line) remains almost constant with increasing distance, while the *punctual h* (red) decreases. Conversely, over the face $x = W$ (Fig. 2.36b) both h coefficients remain almost constant since the heat source is rather far from this wall.
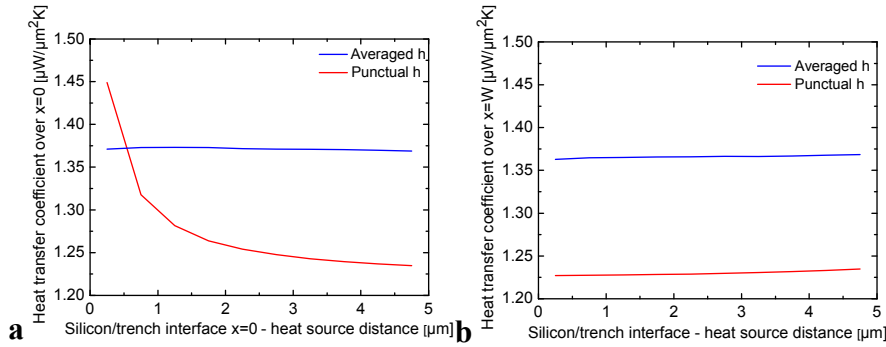
Fig. 2.36. Heat transfer coefficient over the lateral surfaces (a) $x = 0$ and (b) $x = W$ as the distance between the silicon/trench interface $x = 0$ and heat source varies: both the *punctual* (red lines) and *averaged h* (blue) are depicted.

In principle, the heat transfer distribution on the walls $x = 0$ and $x = W$ should be identical (the features of such surfaces are exactly the same). However, the numerical simulation results lead to a different conclusion: it is shown indeed that, when the long side of the heat source is extremely close to the wall, the outgoing heat flux evaluated over the area corresponding to the heat source side projection on the wall grows faster than the temperature increase above ambient, that is, coefficient h over such an area becomes higher than in the remaining *plateau* region. Such a mechanism enhances with decreasing the distance between the heat source and the wall and will be further evidenced shortly.

Fig. 2.37 represents the heat transfer coefficient as a function of depth z crossing the MGC projection over the $x = 0$ wall for two different distances between the heat source side and the lateral surface, i.e., 0.05 (red line) and 4.75 μm (blue line).

It can be seen that in the latter case the *punctual h* equates the *plateau* value, while in the first one the *punctual h* is evaluated in an area where a local h peak is spotted, as an evidence of the previously explained mechanism. In both cases, a sharp h increase can be observed nearby the border between trench ($x = 0$) and buried oxide ($z = 5.5$).
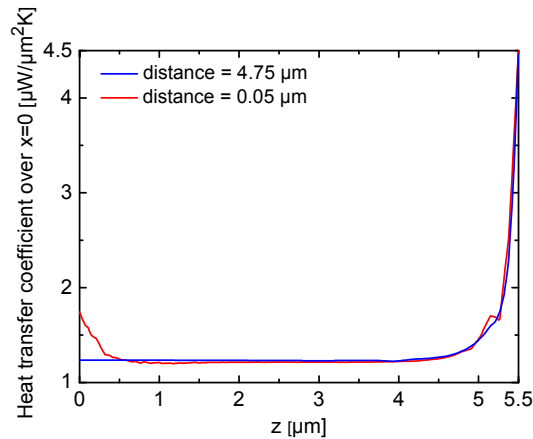
Fig. 2.37. Heat transfer coefficient over the lateral surface $x = 0$ for two distances between the silicon/trench interface $x = 0$ and heat source: 0.05 μm (red lines) and 4.75 μm (blue). The cut is taken through the MGC projection on surface $x = 0$.

Let us now analyze the heat transfer coefficient behavior over the other surfaces. In Fig. 2.38 the *averaged* and *punctual h* on the bottom surface $z = d_t$ and lateral face $y = 0$ are reported. As can be seen, for both cases, the *averaged h* values are almost constant, whereas the *punctual h* decreases (quickly for a low spacing and then more slowly).
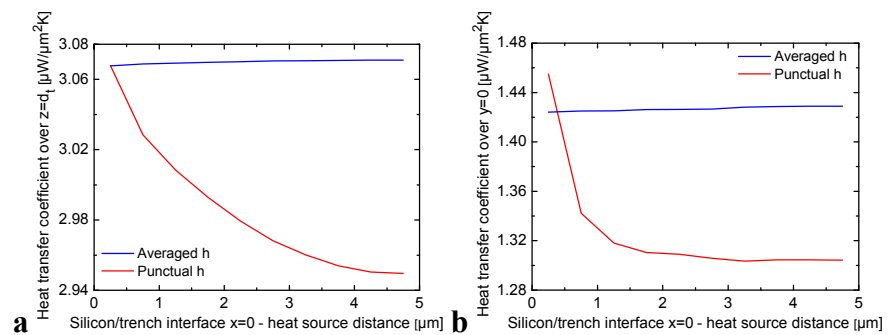
Fig. 2.38. Heat transfer coefficient over (a) the bottom surface $z = d_t$ and (b) lateral sidewall $y = 0$ as a function of the distance between the silicon/trench interface $x = 0$ and heat source. Both the *punctual* (red lines) and *averaged h* (blue) are depicted.

It is interesting to understand the *punctual h* behavior over the $y = 0$ wall as the heat source moves along the x axis. For low distances

the MGC projection on the lateral $y = 0$ surface lies in the close proximity of the trench-trench border corresponding to $x = 0$. This implies that such a point is in the region where h sharply increases so that the *punctual h* reaches higher values. Conversely, when the heat source moves toward the domain center, the projection is located within the *plateau* region, and the *punctual h* becomes independent of the distance (Fig. 2.38b).

Analogous considerations hold when considering the heat transfer coefficient distribution over the surface $z = d_t$. When the heat source is located in the close proximity of the $x = 0$ wall, the MGC projection on the $z = d_t$ plane lies in the "border area" where h sharply increases, so that the *punctual h* value is high. Conversely, when the heat source moves toward the domain center, the projection is located in the *plateau* zone, so that the h value becomes constant as the distance increases. (Fig. 2.38a).

Fig. 2.39 details the behavior of the self-heating thermal resistance R_{TH} of the actual domain as the distance between trench and heat source increases.
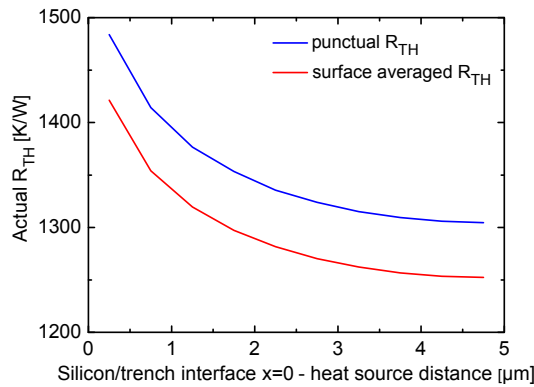
Fig. 2.39. Self-heating thermal resistance of the actual structure as a function of the distance between the silicon/trench interface $x = 0$ and heat source. Two approaches for the evaluation of R_{TH} are depicted: punctual (blue line) and surface-averaged (red).

As can be seen, R_{TH} decreases with increasing distance since the influence of the - almost adiabatic - silicon/trench interface located at $x = 0$ does not affect significantly the temperature peak any longer.

Fig. 2.40 provides the distribution of the temperature field normalized to the dissipated power in the actual domain over the top

surface ($z = 0$) at $y = y_c$ for distances between trench and heat source amounting to 0.25, 2.25, and 4.75 µm.

It is evident that, when the heat source is located very close to the lateral $x = 0$ wall (blue line), the normalized temperature field is strongly affected by the proximity of such a surface, which results in a higher peak value.
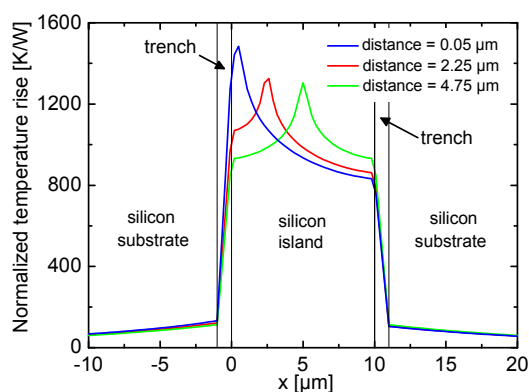
Fig. 2.40. Normalized temperature of the actual structure along x over the top surface for three values of the distance between the silicon/trench interface $x = 0$ and heat source edge: 0.05 µm (blue line), 2.25 µm (red), and 4.75 µm (green). The cut is taken through the MGC heat source projection on the top surface.

2.1.9. Conclusions

The h behavior as a function of all technological parameters involved has been extensively analyzed through a large number of 3-D numerical simulations.

The most relevant results obtained are reported in the following.

1. By assuming that the heat dissipating region is relatively far from the surface under analysis, the h distribution exhibits a uniform *plateau* value far from the face edges.
2. Independently of the heat source proximity with the surface, the h distribution sharply grows nearby the above mentioned edges, where the heat flux attains higher values with respect to the internal wall region.
3. Similar nonuniform distributions arise independently of the domain geometry.

4. The h behavior over a given silicon-insulator interface is primarily dependent on the features of the latter (e.g., interface area, thickness and thermal conductivity of the associated insulating material), while being essentially insensitive to heat source geometry/position within the silicon island.

5. The heat transfer coefficient peak always arises in correspondence of the trench-trench-buried oxide corner, where the heat flux reaches the maximum value.

6. When the heat source is located in the close proximity of the wall, the heat transfer distribution exhibits a local peak within the region corresponding to the projection of the heat source side on the wall. This mechanism is due to the faster growth of the heat flux with respect to the temperature increase above ambient as the source approaches the surface itself (even if such a region is located far from the edges).

7. The *punctual-h* R_{TH} significantly overestimates the actual thermal resistance, while the *averaged-h* R_{TH} provides an excellent agreement.

2.2. Heat transfer coefficients empirical model

Unfortunately, the occurrence of an uneven h distribution over the silicon/insulator interfaces makes the development of analytical models rather cumbersome, since a unique h value should be associated with each surface. In the analysis proposed in [6] for trench devices, the h values to be included in the analytical model were determined so as to obtain the best fit with numerical results. However, since preliminary numerical simulations are required for any domain under analysis, the model is not predictive. In order to overcome this drawback, we conceived a strategy to evaluate analytical laws that empirically relate the heat transfer coefficients to all technological parameters playing a role. Such procedure is based on a preliminary numerical analysis that can be described as follows.

➢ For a given trench SOI domain, a 3-D numerical simulation is employed to obtain the h distributions over the lateral and bottom silicon-insulator interfaces.

➢ Starting from the numerical h distributions, a custom routine is adopted to automatically calculate the average h values for each interface.

The results detailed in the previous Paragraph, in fact, show that the heat transfer mechanisms across the trench and SOI sidewalls can be well approximated by simplified convective boundary conditions with uniform heat transfer coefficients obtained by averaging the actual h distributions. This implies that the thermal behavior of the silicon-only domain with convective boundary conditions described by the average heat transfer coefficients nearly coincides with that of the actual trench SOI structure. Hence, it can be concluded that the original problem – characterized by a high intrinsic complexity – can be turned into a simplified one, which can be easily handled analytically.

As stated before, the average h values are a function of the geometrical and physical parameters of the actual structure. Since the h distributions were numerically found to be almost insensitive to the heat source length/width and position, the same value of averaged heat transfer coefficient can be assigned to the interfaces $x = 0$ and $x = W$ (long silicon island sidewalls); we will denote as h_x this common value. Similar considerations hold for the surfaces $y = 0$ and $y = L$ (short sidewalls); in this case, the common value is designated as h_y. Lastly, the average heat transfer coefficient associated with the interface $z = d_t$ is referred to as h_z. It was shown that:

1. h_x (h_y) is essentially dependent upon trench depth d_t, trench thickness t_t, and silicon island length L (width W), while being almost insensitive to buried oxide thickness t_{OX} and silicon island width W (length L).
2. h_z is sensitive to buried oxide thickness t_{OX}, and silicon island length L and width W, while being almost independent of the trench features.

2.2.1. The model

An extensive dataset for h_x, h_y, and h_z values was numerically evaluated by varying d_t, t_t, t_{OX}, L, and W. Based on these data, the

following empirical dependence laws were determined for the average heat transfer coefficients:

$$h_x = \left(A_x \cdot e^{-a \cdot d_t} + B_x \cdot e^{-b_x \cdot L} + C_x \right) \cdot t_t^{-c} \tag{2.3}$$

$$h_y = \left(A_y \cdot e^{-a \cdot d_t} + B_y \cdot e^{-b_y \cdot W} + C_y \right) \cdot t_t^{-c} \tag{2.4}$$

$$h_z = \left(A_z \cdot e^{-a_z \cdot L} + B_z \cdot e^{-b_z \cdot W} + C_z \right) \cdot t_{OX}^{-c_z} \tag{2.5}$$

The fitting parameter values have been adjusted through *least-squares* optimization routines and are reported in Table 2.2.

Table 2.2
Geometrical parameters of the trench SOI structure.

symbol	value	symbol	value
a	0.627	A_y	9.53×10^{-7}
a_z	0.0113	A_z	1.96×10^{-7}
b_x	0.0141	B_x	3.1×10^{-7}
b_y	0.257	B_y	5.345×10^{-7}
b_z	0.145	B_z	3.29×10^{-7}
c	0.73	C_x	1.13×10^{-6}
c_z	0.843	C_y	1.318×10^{-6}
A_x	9.56×10^{-7}	C_z	1.174×10^{-6}

As shown in Fig. 2.41, Eqs. (2.3)-(2.5) provide a very good agreement with the numerical values. Fig. 2.41a reports the h_x behavior as a function of d_t, t_t, and L as obtained from Eq. (2.3) and numerical simulations. Some observations are in order:

1. h_x rapidly reduces with widening trench thickness, which increasingly inhibits the heat removal from the silicon island;
2. h_x decreases as the trench depth and silicon island length grow since the *plateau* area – which is characterized by a uniformly low h value in the actual structure – enlarges, thus playing a more and more important role when averaging over the whole surface.

Similar considerations hold for the average coefficient h_y, as can be evinced from Fig. 2.41b, which details the h_y behavior as a function of d_t, t_t, and W. Lastly, Fig. 2.41c illustrates the h_z dependence upon t_{OX}, L, and W. As can be seen, a noticeable h_z lowering arises when the buried oxide thickness increases, while a less marked reduction occurs

when increasing the horizontal dimensions of the silicon island, which again is a consequence of the enlarging *plateau* region.[6]

a

b

c
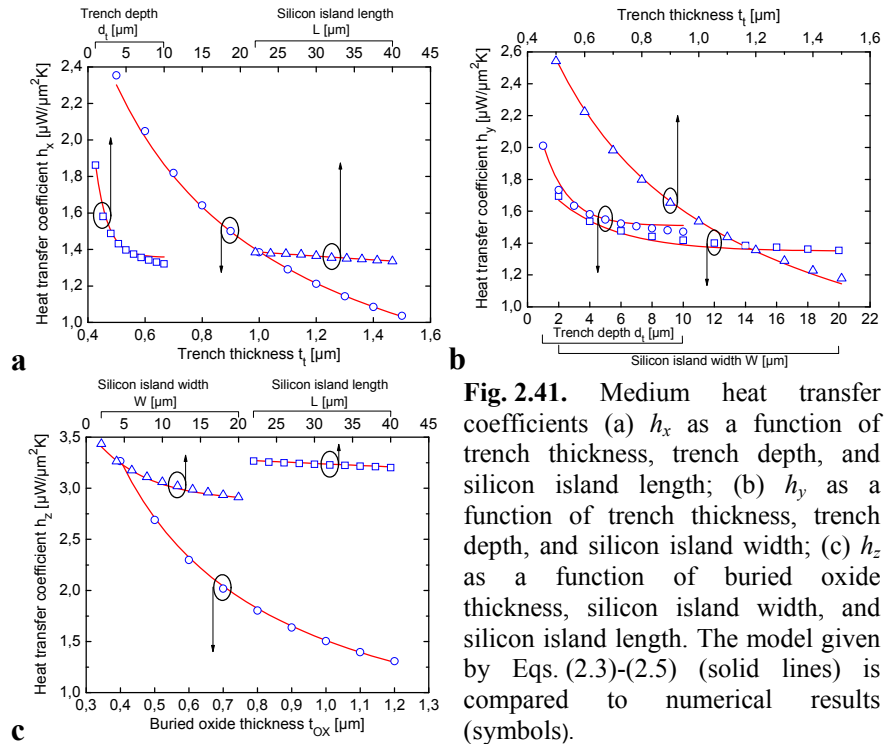
Fig. 2.41. Medium heat transfer coefficients (a) h_x as a function of trench thickness, trench depth, and silicon island length; (b) h_y as a function of trench thickness, trench depth, and silicon island width; (c) h_z as a function of buried oxide thickness, silicon island width, and silicon island length. The model given by Eqs. (2.3)-(2.5) (solid lines) is compared to numerical results (symbols).

2.2.2. Modeling the heat transfer coefficients dependence on thermal conductivity of the trench filling material

In the above analysis, the trenches have been considered to be entirely filled with oxide. However, deep trenches are often fabricated, with polysilicon as a filling material surrounded by thin oxide layers as liners so as to form an oxide-polysilicon-oxide sandwich (see Figs. 2.1a and 2.1b) [11], [17]-[19]. The heat transfer coefficient

---

[6] Although the average coefficients h_x and h_z appear to be almost insensitive to the silicon island length L (see Fig. 2.41a and Fig. 2.41c), accounting for this dependence in the model through an exponential law allows almost halving the error obtained in the evaluation of the thermal resistances for most trench SOI bipolar transistors of interest.

model given by Eqs. (2.3)-(2.5) can be straightforwardly adapted to account for poly-filled trenches by means of the following procedure:

➢ The trenches are assumed to be filled with a homogeneous material (Fig. 2.42) with thermal conductivity k_m determined by a weighted average of polysilicon and oxide layers as

$$k_m = t_t \cdot \left(\frac{2 \cdot t_{OX,t}}{k_{OX}} + \frac{t_{poly}}{k_{poly}} \right)^{-1} \tag{2.6}$$

where t_{OX} and k_{OX} are the thickness and thermal conductivity of the oxide layers, respectively, and t_{poly} and k_{poly} are the thickness and thermal conductivity of the polysilicon layer.
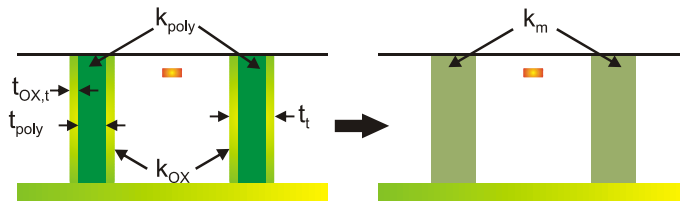
Fig. 2.42. The trench fabricated with polysilicon as a filling material surrounded by thin oxide layers as liners (left) is replaced by a trench filled with a homogeneous material (right).

The accuracy of Eq. (2.6), which exactly works for a 1-D problem, was verified by performing a large number of 3-D numerical simulations of the actual domain and a simplified structure obtained by substituting the trench sandwich with a homogeneous material with thermal conductivity equal to k_m. It is to be noted that k_{poly} can assume a wide range of values, depending upon various factors, e.g., deposition temperature, average grain size, dopant type and concentration [20]-[22]. In our analysis, we have covered a wide range of values spanning from 1×10^{-5} to 5×10^{-5} W/μmK. Fig. 2.43 shows the self-heating thermal resistance as a function of the trench filling material. Three different trench thicknesses are considered. As can be seen, an excellent agreement is obtained between the behaviors of the real structure and the simplified one.
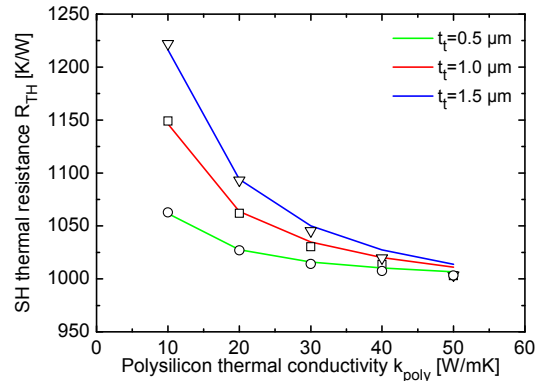
Fig. 2.43. Self-heating thermal resistance as a function of the thermal conductivity of the polysilicon filling the trench. The real structure (symbols) is compared with the simplified one (solid line), obtained by substituting the trench sandwich with a homogeneous material, for three different trench thicknesses.

> Eqs. (2.3) and (2.4) were modified by simply multiplying their RHS by $\left(k_m/k_{OX}\right)^{\alpha}$, without the need of a further optimization for $A_{x,y}$, $B_{x,y}$, and $C_{x,y}$, whose values were extracted for the oxide-filled trench case. Parameter α has been tuned to 0.766 through *least-square* optimization routines. As shown in Fig. 2.44, the properly modified versions of Eqs. (2.3) and (2.4) provide a very good agreement with the numerical values.
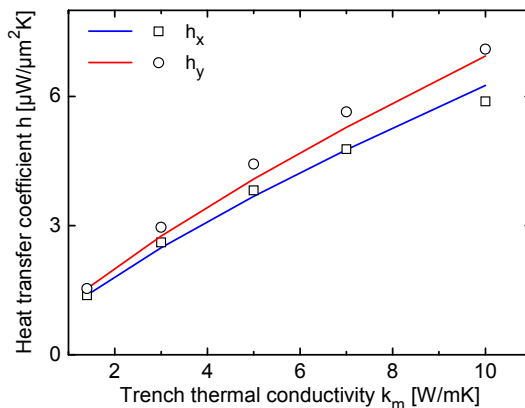
Fig. 2.44. Medium heat transfer coefficients h_x and h_y as a function of medium trench filling material k_m. The model given by Eqs. (2.3) and (2.4) modified (solid lines) is compared to numerical results (symbols).

2.3. The analytical thermal model

In this Paragraph, the steady-state analytical solution of the heat flow equation in the silicon-only domain with convective boundary conditions at lateral and bottom faces and adiabatic top surface is derived via conventional procedures. Both the cases of a rectangular indefinitely thin heat source (THS) embedded within the silicon domain and of a volumetric heat source (VHS) shaped as a rectangular parallelepiped are discussed.[7] Let us denote as x_1, x_2, y_1, y_2 the heat source coordinates along the x and y axis, respectively. As far as the THS case is concerned, the heat source is assumed to be placed at depth $z = d_{HS}$. For the VHS case, z_1 and z_2 represent the heat source coordinates along the z axis. As for the numerical analysis, a uniform dissipation is assumed within the heat generating region.

2.3.1. The temperature field

The temperature rise above ambient $\vartheta(\vec{r}) = \Delta T = T(\vec{r}) - T_{AMB}$ at any point $\vec{r} = (x, y, z)$ within the silicon-only domain can be described by the following equation [Eq. (B.8)]:

$$\nabla^2 \vartheta(\vec{r}) + \frac{g(\vec{r})}{k} = 0 \qquad (2.7)$$

where k is the thermal conductivity of silicon, and $g(\vec{r})$ is the power dissipated per unit volume by the heat source. The convective boundary conditions on the lateral and bottom surfaces are expressed as follows [Eqs. (B.9)-(B.11) in Appendix B]:

---

[7] As detailed in [23], the commonly adopted modeling solution of a THS located at the top surface (i.e., at zero depth) appears to be unjustified for many devices, such as VDMOSTs operated in quasi-saturation and vertical BJTs where heat generation occurs far from the top surface. Conversely, using a THS or a VHS with a proper depth allows describing more accurately the actual temperature field.

$$k \frac{\partial \vartheta(\vec{r})}{\partial n}\bigg|_S + h\,\vartheta(\vec{r})\big|_S = 0 \tag{2.8}$$

where h is the heat transfer coefficient associated with the S surface and n denotes the outward-drawn normal at the boundary surface S. The adiabatic condition at the top surface is given by [Eq. (B.12)]:

$$\frac{\partial \vartheta(\vec{r})}{\partial z}\bigg|_{z=0} = 0 \tag{2.9}$$

Resorting to the separation of variables method, the temperature increase over ambient can be expressed in terms of a double Fourier series

$$\vartheta(\vec{r}) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} X_n(x)\,Y_m(y)\,Z_{nm}(z) \tag{2.10}$$

where the eigenfunctions $X_n(x)$, $Y_m(y)$, and $Z_{nm}(z)$ are evaluated by means of a standard procedure [24] and depend upon coefficients h_x, h_y, and h_z, respectively. In particular, $X_n(x)$ and $Y_m(y)$ are defined as follows:

$$X_n(x) = \frac{\beta_n \overline{X}_n(x) + A \cdot \overline{\overline{X}}_n(x)}{D_n} \tag{2.11}$$

$$Y_m(y) = \frac{\alpha_m \overline{Y}_m(y) + B \cdot \overline{\overline{Y}}_m(y)}{E_m} \tag{2.12}$$

being $\overline{X}_n(x) = \cos(\beta_n x)$, $\overline{\overline{X}}_n(x) = \sin(\beta_n x)$, $\overline{Y}_m(y) = \cos(\alpha_m y)$, $\overline{\overline{Y}}_m(y) = \sin(\alpha_m y)$, and

$$D_n = \left[\left(\beta_n^2 + A^2\right)\cdot\frac{W}{2} + A\right]^{1/2} \tag{2.13}$$

$$E_m = \left[\left(\alpha_m^2 + B^2\right)\cdot\frac{L}{2} + B\right]^{1/2} \tag{2.14}$$

where $A = h_x/k$, $B = h_y/k$.

In the THS case, the eigenfunctions $Z_{nm}(z)$ are given by

$$Z_{nm}(z) = \frac{P_D}{\Gamma} \cdot \frac{G_{nm}}{\gamma_{nm}k} \cdot \overline{Z}_{nm}(z) \times \tag{2.15}$$

$$\times \frac{k\gamma_{nm}\overline{Z}_{nm}(d_t - d_{HS}) + h_z\overline{\overline{\overline{Z}}}_{nm}(d_t - d_{HS})}{k\gamma_{nm}\overline{\overline{\overline{Z}}}_{nm}(d_t) + h_z\overline{Z}_{nm}(d_t)} +$$

$$+ \begin{cases} 0 & z < d_{HS} \\ \dfrac{P_D}{\Gamma} \cdot \dfrac{G_{nm}}{\gamma_{nm}k} \cdot \overline{\overline{\overline{Z}}}_{nm}(d_{HS} - z) & z \geq d_{HS} \end{cases}$$

while for the VHS case they are expressed as

$$Z_{nm}(z) = -\frac{P_D}{\Gamma} \cdot \frac{G_{nm}}{\gamma_{nm}^2 k} \cdot \frac{\overline{Z}_{nm}(z)}{k\gamma_{nm}\overline{\overline{\overline{Z}}}_{nm}(d_t) + h_z\overline{Z}_{nm}(d_t)} \times \tag{2.16}$$

$$\times \begin{cases} k\gamma_{nm}\left[\overline{\overline{\overline{Z}}}_{nm}(d_t - z_2) - \overline{\overline{\overline{Z}}}_{nm}(d_t - z_1)\right] + \\ + h_z\left[\overline{Z}_{nm}(d_t - z_2) - \overline{Z}_{nm}(d_t - z_1)\right] \end{cases} +$$

$$+ \begin{cases} 0 & z < z_1 \\ \dfrac{P_D}{\Gamma} \cdot \dfrac{G_{nm}}{\gamma_{nm}^2 k} \cdot \left[1 - \overline{Z}_{nm}(z_1 - z)\right] & z_1 \leq z \leq z_2 \\ \dfrac{P_D}{\Gamma} \cdot \dfrac{G_{nm}}{\gamma_{nm}^2 k} \cdot \left[\overline{Z}_{nm}(z_2 - z) - \overline{Z}_{nm}(z_1 - z)\right] & z > z_2 \end{cases}$$

where $\overline{Z}_{nm}(z) = \cosh(\gamma_{nm}z)$, $\overline{\overline{\overline{Z}}}_{nm}(z) = \sinh(\gamma_{nm}z)$, $\gamma_{nm}^2 = \beta_n^2 + \alpha_m^2$, P_D [W] is the overall power dissipated by the heat source, Γ represents the heat source area ($W_{HS} \cdot L_{HS}$) for the THS case or the heat source volume ($W_{HS} \cdot L_{HS} \cdot t_{HS}$) for the VHS case, and the G_{nm} terms are expressed as

$$G_{nm} = \frac{1}{D_n \cdot E_m} \times \tag{2.17}$$

$$\times \left\{ \bar{\bar{X}}_n(x_2) - \bar{\bar{X}}_n(x_1) - \frac{A}{\beta_n} \left[\bar{X}_n(x_2) - \bar{X}_n(x_1) \right] \right\} \times$$

$$\times \left\{ \bar{\bar{Y}}_m(y_2) - \bar{\bar{Y}}_m(y_1) - \frac{B}{\alpha_m} \left[\bar{Y}_m(y_2) - \bar{Y}_m(y_1) \right] \right\}$$

The eigenvalues β_n and α_m can be found by solving the transcendental equations given by

$$\tan(\beta_n W) = \frac{2\beta_n A}{\beta_n^2 - A^2} \tag{2.18}$$

$$\tan(\alpha_m L) = \frac{2\alpha_m B}{\alpha_m^2 - B^2} \tag{2.19}$$

The derivation of Eqs. (2.10)-(2.19) is discussed in detail in Appendix B[8].

Adopting Eqs. (2.3)-(2.5) in order to analytically describe the heat transfer coefficients makes the proposed model fully predictive, namely, applicable to any trench SOI bipolar transistor without the need of further numerical simulations and coefficient optimizations.

2.3.2. The self-heating thermal resistance

The self-heating thermal resistance R_{TH} is evaluated as the average of the temperature rise above ambient normalized to the dissipated power over the heat source projection on the top surface, i.e.,[9]

$$R_{TH} = \frac{1}{P_D \cdot W_{HS} \cdot L_{HS}} \cdot \int\limits_{x_1}^{x_2} \int\limits_{y_1}^{y_2} \vartheta(x, y, 0)\, dy\, dx \tag{2.20}$$

---

[8] The equations derived in Appendix B must be particularized for $h_{x0} = h_{xW} = h_x$, $h_{y0} = h_{yL} = h_y$, $B_1 = B_2 = A$, and $C_1 = C_2 = B$.

[9] The self-heating thermal resistance can be also defined as the value of the normalized temperature rise at the projection of the heat source center on the top surface (as in e.g., [25], [26]). However, this may lead to an overestimation of thermal effects from the modeling point of view. On the other hand, the accuracy of the proposed model was demonstrated to be independent of the thermal resistance definition.

Substituting Eq. (2.10) into Eq. (2.20), we obtain:

$$R_{TH} = \frac{1}{P_D \cdot W_{HS} \cdot L_{HS}} \times$$
$$\times \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} Z_{nm}(z=0) \cdot \int_{x_1}^{x_2} X_n(x)\,dx \cdot \int_{y_1}^{y_2} Y_m(y)\,dy \qquad (2.21)$$

From Eq. (2.11), we have:

$$\int_{x_1}^{x_2} X_n(x)\,dx = \int_{x_1}^{x_2} \frac{\beta_n \bar{X}_n(x) + A \cdot \bar{\bar{X}}_n(x)}{D_n}\,dx = \qquad (2.22)$$

$$= \frac{1}{D_n} \cdot \left[\bar{\bar{X}}_n(x) - \frac{A}{\beta_n} \bar{X}_n(x) \right]_{x=x_1}^{x=x_2} =$$

$$= \frac{1}{D_n} \cdot \left\{ \bar{\bar{X}}_n(x_2) - \bar{\bar{X}}_n(x_1) - \frac{A}{\beta_n} \left[\bar{X}_n(x_2) - \bar{X}_n(x_1) \right] \right\}$$

Analogously, it can be found that:

$$\int_{y_1}^{y_2} Y_m(y)\,dy = \int_{y_1}^{y_2} \frac{\alpha_m \bar{Y}_m(y) + B \cdot \bar{\bar{Y}}_m(y)}{E_m}\,dy = \qquad (2.23)$$

$$= \frac{1}{E_m} \cdot \left[\bar{\bar{Y}}_m(y) - \frac{B}{\alpha_m} \bar{Y}_m(y) \right]_{y=y_1}^{y=y_2} =$$

$$= \frac{1}{E_m} \cdot \left\{ \bar{\bar{Y}}_m(y_2) - \bar{\bar{Y}}_m(y_1) - \frac{B}{\alpha_m} \left[\bar{Y}_m(y_2) - \bar{Y}_m(y_1) \right] \right\}$$

Substituting Eqs. (2.22) and (2.23) combined with Eq. (2.17) into Eq. (2.21), we have:

$$R_{TH} = \frac{1}{P_D \cdot W_{HS} \cdot L_{HS}} \cdot \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} G_{nm} \cdot Z_{nm}(z=0) \qquad (2.24)$$

where from Eqs. (2.15) and (2.16)

$$Z_{nm}\left(z=0\right)=\frac{P_D}{\Gamma}\cdot\frac{G_{nm}}{\gamma_{nm}k}\times$$

$$\times\frac{k\gamma_{nm}\overline{Z}_{nm}\left(d_t-d_{HS}\right)+h_z\overline{\overline{Z}}_{nm}\left(d_t-d_{HS}\right)}{k\gamma_{nm}\overline{\overline{Z}}_{nm}\left(d_t\right)+h_z\overline{Z}_{nm}\left(d_t\right)}$$

(2.25)

and

$$Z_{nm}\left(z=0\right)=-\frac{P_D}{\Gamma}\cdot\frac{G_{nm}}{\gamma_{nm}^2k}\cdot\frac{1}{k\gamma_{nm}\overline{\overline{Z}}_{nm}\left(d_t\right)+h_z\overline{Z}_{nm}\left(d_t\right)}\times$$

$$\times\left\{\begin{array}{l}k\gamma_{nm}\left[\overline{\overline{Z}}_{nm}\left(d_t-z_2\right)-\overline{\overline{Z}}_{nm}\left(d_t-z_1\right)\right]\\+h_z\left[\overline{Z}_{nm}\left(d_t-z_2\right)-\overline{Z}_{nm}\left(d_t-z_1\right)\right]\end{array}\right\}$$

(2.26)

in the THS and VHS cases, respectively.

2.3.3. Remarks

It should be remarked that this approach allows for considerably short CPU times[10] due to a twofold reason:

1. Since only the steady-state case was analyzed, we resorted to the double Fourier series expansion, which allows achieving convergence with a much lower number of terms as compared to the Green's function approach (adopted in e.g., [27] for bulk silicon devices and [6] for trench transistors). As far as the reference structure is concerned, the summations are to be performed up to $(n, m) = (40, 25)$ to converge within 0.02%.
2. In principle, Eqs. (2.18) and (2.19) should be solved numerically (as in e.g., [6]), but this step would require an additional simulation time. In our strategy, this was avoided by resorting to approximate, yet accurate analytical closed-form solutions obtained by properly modifying those available in [24].

---

[10] The simulation time for the evaluation of a self-heating thermal resistance value is about 0.1 s on a PC with a 2 GHz processor.

Furthermore, it should be noted that in the above treatment we have neglected nonlinear thermal effects due to the silicon thermal conductivity dependence on temperature as well as the cooling action due to metallization layers. However, the proposed model can be effortlessly generalized to account for both effects: the nonlinear thermal effects can be taken into account by resorting to the Kirchhoff transformation [28] (see Appendix F), whilst the metallization influence can be included by following the approach proposed in [6], namely, by adding a parallel thermal resistance to describe the heat flow through the metal path.

In particular, as concerns a multifinger structure, the cooling/coupling effect due to the metal lines can be easily accounted for. Let us refer to Fig. 2.45. It shows two fingers, denoted by 1 and 2, respectively, embedded in a silicon island surrounded by trenches and buried oxide. Accounting for metallization layers would have a twofold effect: first, the self-heating thermal resistance of the elementary fingers will reduce due to the additional path through the metal; second, the mutual thermal resistance (i.e., the thermal coupling degree) will increase. Let us indicate the self-heating thermal resistances as R_{11} and R_{22} and the mutual thermal resistance as R_m in the absence of metal lines. Let us remember that differently from the heat fluxes, the heat transfer coefficients are primarily dependent on the physical nature of the surface; as a consequence, they are independent of metal terminals and insensitive to the presence of neighboring fingers and to the heat source geometry/position. Furthermore, R_{11}, R_{22}, and R_m remain unchanged when accounting for the presence of neighboring fingers and/or metallization so that we are able to evaluate them via the proposed model. As concerns the metallization, 3-D numerical simulations of actual structures demonstrated that the metallization effect can be modeled by considering two additional parallel thermal resistances associated with the individual devices and an extra mutual resistance between them (referred to as $R_{11,Metal}$, $R_{22,Metal}$, and $R_{m,Metal}$, respectively, in Fig. 2.45).
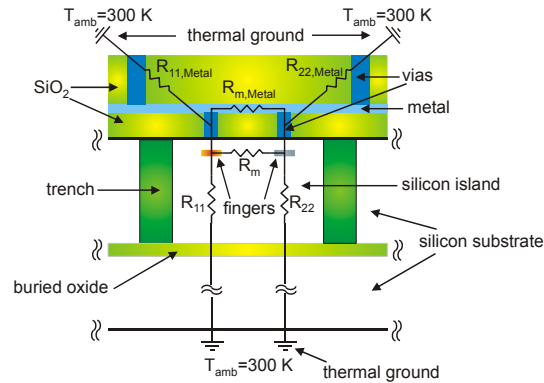
Fig. 2.45. Cooling effects in a multifinger structure.

2.4. Simulation results

The proposed model has been extensively compared to fully 3-D numerical results obtained for the actual trench SOI structure in a wide range of values for all technological parameters of interest. The analysis was performed by varying a chosen parameter while keeping the others equal to the reference ones.

2.4.1. Self-heating thermal resistance dependence on technological parameters

First, the impact of enlarging the thickness of the insulating layers surrounding the silicon island was analyzed. Fig. 2.46 shows that the self-heating thermal resistance R_{TH} grows with both t_{OX} and t_t since the heat removal from the silicon island becomes increasingly hard. As can be seen, the analytical model agrees well with numerical results. A small discrepancy is observed for large t_{OX} values since coefficients h_x and h_y associated with the lateral walls exhibit a slight dependence upon the features of the buried oxide, which has been neglected in Eqs. (2.3) and (2.4) for the sake of simplicity. It was indeed verified that such an approximation does not appreciably affect the model accuracy: an error amounting to less than 3% is found to occur at $t_{OX} = 1.2$ μm.

Fig. 2.46. Self-heating thermal resistance of the trench SOI structure as a function of trench and buried oxide thicknesses. The model given by Eq. (2.24) (solid lines) is compared to numerical results (symbols).

Fig. 2.47 shows the influence of the variation of the silicon island dimensions. As can be seen, R_{TH} decreases with both W and L due to the larger silicon volume where the heat can easily spread from the active transistor area. Increasing the silicon island width results in a faster thermal resistance decrease since the trench walls are moving away from the long side of the emitter stripe. In this case, an excellent agreement is obtained between model and numerical data.
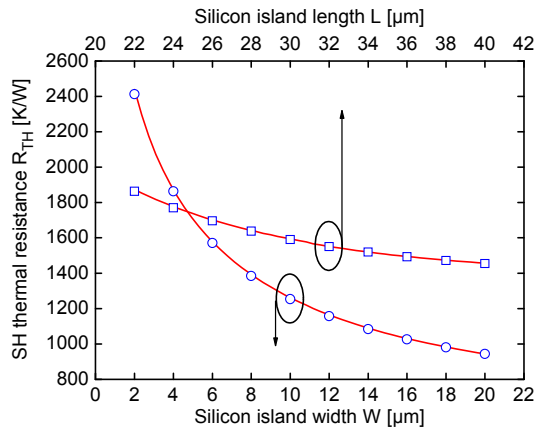
Fig. 2.47. Self-heating thermal resistance of the trench SOI structure as a function of silicon island width and length. The model given by Eq. (2.24) (solid lines) is compared to numerical results (symbols).

Lastly, Fig. 2.48 illustrates the thermal resistance behavior as the trench depth changes for various trench materials, i.e., pure silicon dioxide and oxide-polysilicon-oxide sandwich with two different polysilicon thermal conductivities.
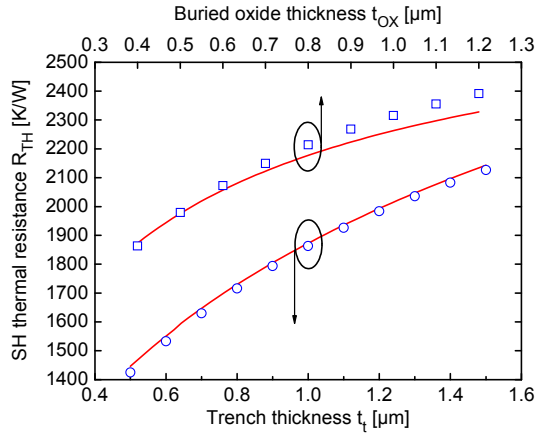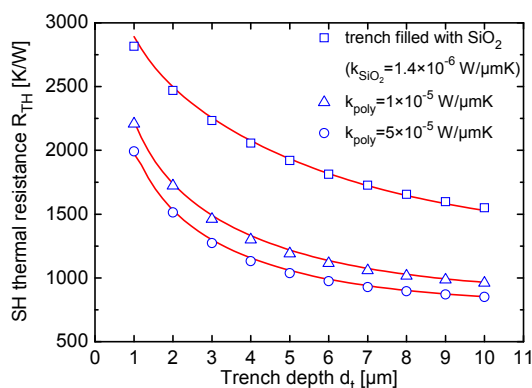

Fig. 2.48. Self-heating thermal resistance of the trench SOI structure as a function of trench depth for the cases of oxide-filled trench and oxide-polysilicon-oxide trench for two values of the thermal conductivity of polysilicon. The model given by Eq. (2.24) (solid lines) is compared to numerical results (symbols).

R_{TH} lowers as the trench depth increases due to the silicon island volume enlargement, and tends to a constant value for high trench depth values since the influence of the bottom interface on the temperature distribution in the heat dissipating region becomes negligible. In a similar fashion, R_{TH} decreases when increasing the average thermal conductivity of the trenches, which is an expected result.

Let us note that when considering a trench SOI structure with trenches uniformly filled with oxide, the analytical model provides an overall excellent agreement with numerical results. A maximum error amounting to about 3% has been found by simultaneously varying all geometrical parameters in the ranges of interest. On the other hand, the accuracy slightly reduces when considering a more complex domain with trenches filled with an oxide-polysilicon-oxide sandwich, which was accounted for through the approximated formula (2.6). In this case, we found that the maximum error grows to 5% by varying all technology parameters in a wide range of k_{poly} values.

2.4.2. Scaling effects on the self-heating thermal resistance

Another important feature of the proposed model is the capability of quantitatively predicting scaling-induced thermal effects in a trench SOI technology. Fig. 2.49 shows the R_{TH} behavior with varying the heat source length for various width values. The thermal resistance increase as the device shrinks is easily observable. As can be seen, R_{TH} spans from 1810 K/W for a 0.8×20 µm^2 emitter area to 8380 K/W for a 0.2×0.5 µm^2 one, both embedded in a $4 \times 22 \times 5.5$ µm^3 silicon island. It can be also seen that:

1. the influence of the source width on the thermal resistance reduces for longer sources;
2. the discrepancy between the thermal behaviors of a trench SOI device and the bulk-silicon counterpart (i.e., that obtained by removing all the insulating layers) diminishes for small heat sources; this is an expected result, since the silicon-insulator borders are located far away from the active transistor area, thereby slightly affecting the junction temperature.
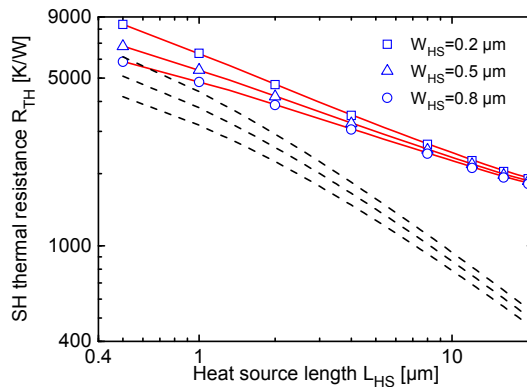
Fig. 2.49. Self-heating thermal resistance of the trench SOI structure as a function of heat source length for various values of heat source width. The model (solid lines) is compared to numerical results (symbols). Dashed lines refer to devices fabricated on conventional silicon-only substrates.

Fig. 2.50 shows the thermal resistance behavior as a function of heat source area for various values of the aspect ratio L_{HS}/W_{HS}. The figure reveals that – for an assigned source area – the thermal

resistance reduces by increasing the aspect ratio, while reaching the maximum value for a square source.
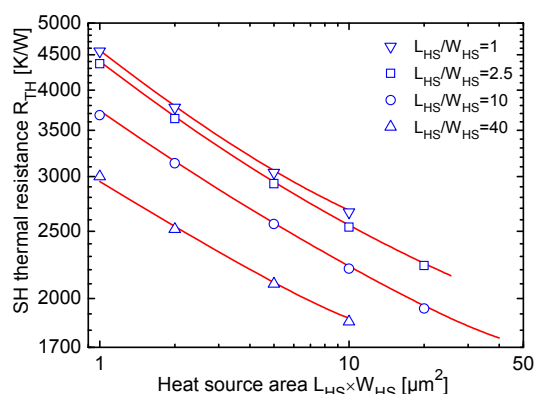
Fig. 2.50. Self-heating thermal resistance of the trench SOI structure as a function of heat source area for various aspect ratio values. The model (solid lines) is compared to numerical results (symbols).

Once again, the model matches numerical data with high accuracy. This suggests its adoption to predict the device scaling effects on the thermal behavior of a trench SOI structure.

All the obtained results show that the concurrent adoption of trenches and buried oxide drastically affects the thermal characteristics of the devices.

2.4.3. Temperature distributions evaluation

It should be remarked that, similarly to the approach developed in [6] for trench-only devices, the proposed model also allows evaluating the temperature distribution within the silicon island, a capability absent in other works dealing with *either* trench [5], [8], [9] *or* SOI structures [5]. As a main benefit, the mutual thermal coupling between transistors integrated in the same island can be estimated. This represents a key feature, since the thermal interaction between individual transistors has been demonstrated to play an important role in the electrothermal behavior of multifinger devices [29] as well as of basic analog circuits [30].

The following figures show the temperature rise field normalized to the dissipated power in the reference domain as evaluated by the model and 3-D numerical simulations.

Fig. 2.51 illustrates the contour curves over the cross-section of the silicon island, while Fig. 2.52 and Fig. 2.53 show the normalized temperature rise distribution along the x and z axis, respectively.
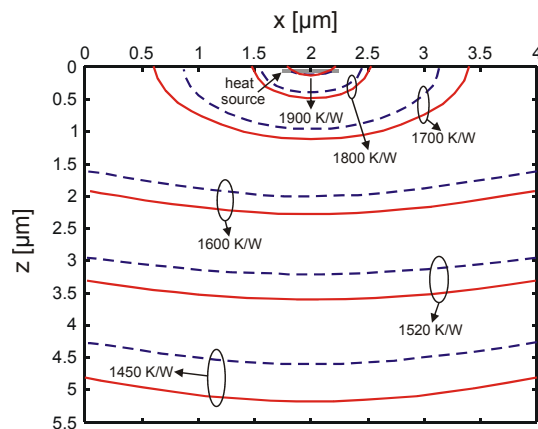
Fig. 2.51. Temperature rise normalized to dissipated power in the reference domain. The model (red lines) is compared with 3-D numerical data (blue): contour plots over the cross-section of the silicon island.
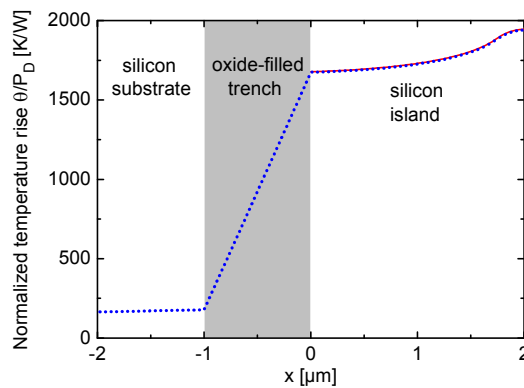
Fig. 2.52. Temperature rise normalized to dissipated power in the reference domain. The model (red lines) is compared with 3-D numerical data (blue): normalized temperature rise field vs. x axis. The horizontal cut is taken through the heat source center.
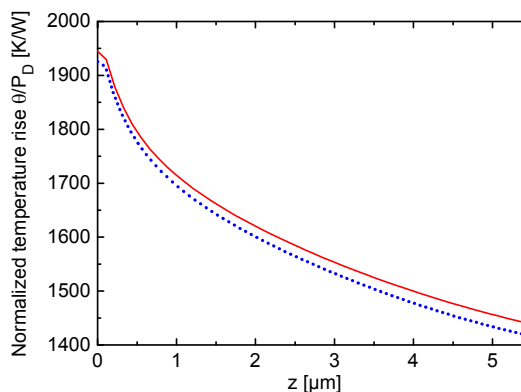
Fig. 2.53. Temperature rise normalized to dissipated power in the reference domain. The model (red lines) is compared with 3-D numerical data (blue): normalized temperature rise field vs. z axis. The vertical cut is taken through the heat source center.

An inspection of the figure reveals that:

1. an excellent agreement is obtained between the analytical model and numerical results within the silicon island, especially in the heat generating region;
2. a moderate temperature gradient occurs in both the island and substrate due to the large thermal conductivity of silicon, whereas a significant variation arises inside the trench.

References

[1]   Davis C, Bajor G, Butler J, Crandell T, Delgado J, Jung T, et al. UHF-1: A high-speed complementary bipolar analog process on SOI. IEEE BCTM Proc 1992;260-3.

[2]   Harame DL, Comfort JH, Cressler JD, Crabbè EF, Sun JYC, Meyerson BS, el al. Si/SiGe epitaxial-base transistors – Part II: Process integration and analog applications. IEEE Trans Electron Dev 1995;42(3):469-82.

[3]   Ueno S, Watanabe K, Kato T, Shinohara T, Mikami K, Hashimoto T, et al. A single-chip 10 Gb/s transceiver LSI using SiGe SOI/BiCMOS. IEEE ISSCC Tech. Dig. Proc 2001;82-3.

[4] Wei L, Zhang R, Roy K, Chen Z, Janes DB. Vertically integrated SOI circuits for low-power and high-performance applications. IEEE Trans Very Large Scale Integration (VLSI) Systems 2002;10(3):351-62.

[5] Pacelli A, Palestri P, Mastrapasqua M. Compact modeling of thermal resistance in bipolar transistors on bulk and SOI substrates. IEEE Trans Electron Dev 2002;49(6):1027-33.

[6] Walkey DJ, Smy TJ, Reimer C, Schröter M, Tran H, Marchesan D. Modeling thermal resistance in trench-isolated bipolar technologies including trench heat flow. Solid-State Electron 2002;46(1):7-17.

[7] Walkey DJ, Smy TJ, Marchesan D, Tran H, Schröter M. A scalable thermal model for trench isolated bipolar devices. Solid-State Electron 2000; 44(8):1373-9.

[8] Rieh JS, Johnson J, Furkay S, Greenberg D, Freeman G, Subanna S. Structural dependence of the thermal resistance of trench-isolated bipolar transistors. IEEE BCTM Proc 2002;100-3.

[9] Vanhoucke T, Hurkx GAM. A new analytical model for the thermal resistance of deep-trench bipolar transistors. IEEE Trans Electron Dev 2006;53(6):1379-88.

[10] Palestri P, Pacelli A, Mastrapasqua M. Thermal resistance in $Si_{1-x}Ge_x$ HBTs on bulk-Si and SOI substrates. IEEE BCTM Proc 2001;98-101.

[11] Ganci PR, Hajjar JJJ, Clark T, Humphries P, Lapham J, Buss D. Self-heating in high performance bipolar transistors fabricated on SOI substrates. IEEE IEDM Proc 1992;417-20.

[12] Pinardi K, Heinle U, Bengtsson S, Olsson J, Colinge JP. High-power SOI vertical DMOS transistors with lateral drain contacts: Process developments, characterization, and modeling. IEEE Trans Electron Dev 2004;51(5):790-6.

[13] Malm BG, Haralson E, Johansson T, Östling M. Self-heating effects in a BiCMOS on SOI technology for RFIC applications. IEEE Trans Electron Dev 2005;52(7):1423-8.

[14] Brodsky JS, Fox RM, Zweidinger DT. A physics-based dynamic thermal impedance model for vertical bipolar transistors on SOI substrates. IEEE Trans Electron Dev 1999;46(12):2333-9.

[15] Walkey DJ, Smy TJ, Reimer C, Schröter M, Tran H, Marchesan D. Modeling thermal resistance in trench-isolated bipolar

technologies including trench heat flow. Solid-State Electron 2002;46(1):7-17.

[16] Comsol Multiphysics 3.3, User's guide, Comsol AB, 2007.

[17] Reid AR, Kleckner TC, Jackson MK, Marchesan D, Kovacic SJ, Long JR. Thermal resistance in trench-isolated Si/SiGe heterojunction bipolar transistors. IEEE Trans Electron Dev 2001;48(7):1477-9.

[18] Nigrin S, Wilson MC, Thomas S, Connor S, Osborne PH. A complementary bipolar technology on SOI featuring 50GHz NPN and 35GHz PNP devices for high performance RF applications. IEEE International SOI Conference Proc 2002;155-7.

[19] Heinle U, Vestling L, Olsson J. Modeling and characterization of capacitive coupling in trench-isolated structures on SOI substrates. Solid-State Electron 2004;48(1):43-9.

[20] McConnell AD, Uma S, Goodson KE. Thermal conductivity of doped polysilicon layers. Journal of Microelectromechanical Systems 2001;10(3):360-9.

[21] Tai YC, Mastrangelo CH, Muller RS. Thermal conductivity of heavily doped LPCVD polysilicon. IEEE IEDM Proc 1987;33:278-81.

[22] Xu GB, Huang QA. An online test microstructure for thermal conductivity of surface-micromachined polysilicon thin films.IEEE Sensors Journal 2006;6(2):428-33.

[23] d'Alessandro V, Rinaldi N. A critical review of thermal models for electro-thermal simulation. Solid-State Electron 2002;46(4):487-96.

[24] Beck JV, Cole D, Haji-Sheikh A, Litkouhi B. Heat conduction using Green's functions. London: Hemisphere Publishing Corporation; 1992.

[25] Rinaldi N. Thermal analysis of solid-state devices and circuits: an analytical approach. Solid-State Electron 2000;44(10):1789-98.

[26] Walkey DJ, Celo D, Smy TJ, Surridge RK. A thermal design methodology for multifinger bipolar transistor structures. IEEE Trans Electron Dev 2002;49(8):1375-83.

[27] Haji-Sheikh A. Peak temperature in high-power chips. IEEE Trans Electron Dev 1990;37(4):902-7.

[28] Heasell EL. The heat-flow problem in silicon: an approach to an analytical solution with application to the calculation of thermal instability in bipolar devices. IEEE Trans Electron Dev 1978;ED-25(12):1382-8.

[29] Rinaldi N, d'Alessandro V. Theory of electrothermal behavior of bipolar transistors: Part II – Two-finger devices. IEEE Trans Electron Dev 2005;52(9):2022-33.

[30] d'Alessandro V, Nanver LK, Zampardi PJ, Rinaldi N. Analysis of electrothermal effects in bipolar current mirrors. IEEE BCTM Proc 2007;127-30.

Chapter 3

Trench-isolated bipolar transistors on bulk substrates

Nowadays many bipolar processes are based on deep trench isolation to reduce parasitic capacitances, minimizing cross-talk interference, and favor latch-up immunity [1]-[3]. Unfortunately, due to the poor thermal conductivity of the trench-filling materials, the heat flow coming from the active transistor area is mostly confined within the silicon-only region enclosed by the trench (also referred to as *trench box* or *trench well* throughout the Chapter) before spreading into the substrate, thereby leading to exacerbated thermal issues with respect to bulk-silicon transistors of comparable size (Fig. 3.1).
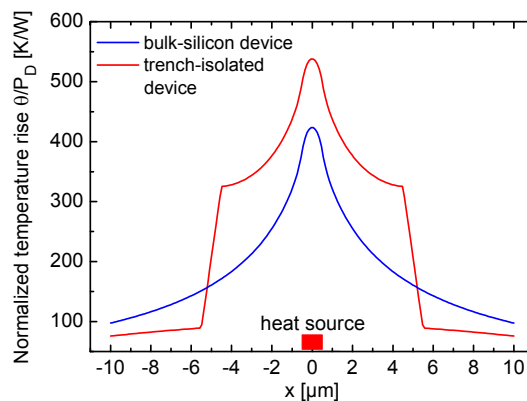
Fig. 3.1. Temperature rise above ambient normalized to dissipated power along the *x* axis as obtained by 3-D numerical simulations. An active region of 1×20 μm^2 is considered. The cut is taken through the heat source center projection on the top surface. The cases of a bulk-silicon transistor (blue line) and a trench-isolated device (red) are compared.

Various approaches are therefore sought in order to predict the impact of all technological parameters on the thermal behavior of DTI devices. Numerical finite-element solutions [4] are predictive but

typically demanding in terms of (i) pre-computational time, since the mesh is to be properly designed to obtain a reasonable accuracy, (ii) computational time, and (iii) memory storage; moreover, any change in domain geometry would need the repetition of the meshing process, thus making parametric analyses rather laborious. An alternative – generally preferred – approach involves the development of analytical models relating power dissipation to temperature at any point of the structure. However, an exact analytical evaluation of the temperature field is only feasible for oversimplified device geometries like transistors embedded in conventional bulk substrates (e.g., [5], [6]). Consequently, simplifying assumptions are to be necessarily adopted when dealing with DTI transistors due to their inherent geometrical complexity. On the other hand, the resulting approximate models should be (i) predictive, namely, suited to evaluate the temperature distribution starting only from technological data, (ii) accurate enough, and (iii) easy to be included into device/circuit simulation programs.

In this scenario, a number of analytical approaches have been conceived and published in the literature to describe the thermal behavior of trench-isolated bipolar transistors [7]-[10]. The limitations of such strategies will be discussed later.

The aim of this Chapter is to present a detailed investigation of the thermal behavior of trench-isolated bipolar transistors under steady-state conditions. The Chapter is organized as follows.

First, accurate thermal-only 3-D numerical simulations are performed to analyze the heat transfer capability of the trench lateral walls as well as of the interface between trench box and silicon substrate.

Subsequently, starting from numerical results, a novel modeling approach is developed to evaluate the temperature field in a DTI structure, which employs convective boundary conditions to describe the finite heat leakage through the trench and a partitioning strategy to model the heat transfer from the trench box to the substrate.

Afterward, the details of the proposed analytical model, that results fully predictive and requires extremely short simulation time, are provided.

Finally, a plain and detailed overview of the thermal behavior of DTI transistors is given for a wide range of geometrical/material parameters typical of bipolar technologies by means of both the model

and numerical results. Moreover, the model usefulness to improve the thermal device design is discussed and the comparison with the other models is presented. It will be seen that the resulting model is more accurate than the other models available from the literature.

3.1   Numerical analysis and modeling strategy

The domain under analysis is shown in Fig. 3.2a and b, and is comprised of a silicon box surrounded by DTI embedded in a 300-μm-thick silicon substrate, with bottom surface assumed to be in intimate contact with an ideal heat sink at temperature $T_{AMB} = 300$ K. The heat source is represented as a rectangular parallelepiped with length and width assumed equal to those of the emitter window, and thickness vertically coinciding with that of the base-collector depletion region, where the heat dissipation takes place. The heat generated by the source is assumed to be due to a uniform power dissipation.
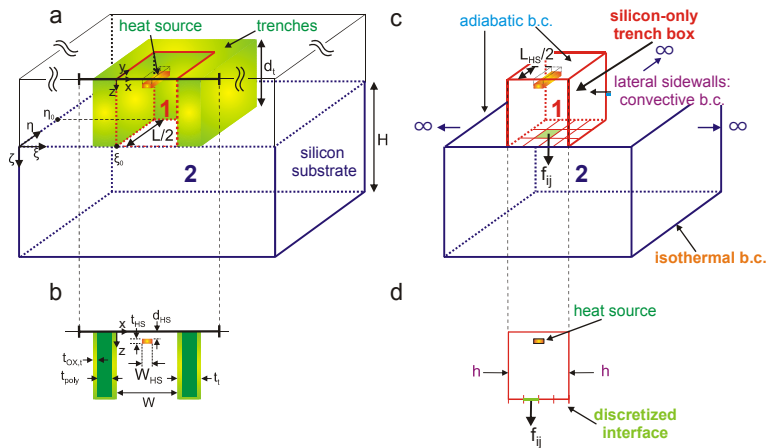
Fig. 3.2. (a) Analyzed trench domain and (b) cross-section corresponding to the trench region; (c) simplified silicon-only domain partitioned into subdomains 1 and 2 and (d) cross-section of the related trench box. Also evidenced are the boundary conditions (b.c.) adopted in the proposed modeling strategy.

As a first step, 3-D thermal-only simulations were performed through the commercial tool Comsol, which is based on the finite

element method [11]. The numerical investigation was aimed at better understanding the thermal process in trench-isolated bipolar transistors, with particular emphasis to the heat transfer capability of trench walls and bottom of the trench box (i.e., the interface between trench box and substrate located at $z = d_t$, also referred to as *trench bottom* in the following). The analysis was carried out as follows.

A reference DTI structure, with geometrical parameters listed in Table 3.1, was defined. The numerical simulations were performed by varying an assigned parameter while keeping all other parameters constant and equal to the reference ones. All geometrical quantities were varied, i.e., width/length of the trench box, trench depth/thickness, width/length and position of the heat source (horizontally centered within the trench box in the reference structure). The variations were chosen within ranges typical of bipolar technologies (see Table 3.1). The trench was initially assumed to be filled only with silicon dioxide (as in e.g., [3]), whose thermal conductivity was chosen to be 1.4×10^{-6} W/µmK, while 1.4×10^{-4} W/µmK was assumed for silicon.

Table 3.1
Geometrical parameters of the trench-isolated structure.

parameter	description	reference domain [µm]	variation range [µm]
W	trench box width	9	$5 \div 21$
L	trench box length	23	$22 \div 34$
t_t	trench thickness	1	$0.4 \div 2.5$
d_t	trench depth	6	$2 \div 12$
$t_{OX,t}$	trench oxide thickness	0.1	—
t_{poly}	thickness of the trench polysilicon layer	$t_t – 2t_{OX,t}$	—
W_{HS}	heat source width	1	$0.15 \div 3.15$
L_{HS}	heat source length	20	$1 \div 20$
t_{HS}	heat source thickness	0.2	—
d_{HS}	heat source depth	0.4	—

For the structures exhibiting geometrical symmetries, only a portion of the domain was simulated, with adiabatic boundary

conditions to virtually restore the missing parts.[11] This allowed reducing the number of elements to be accounted for within the program environment, thus decreasing the CPU time/memory storage requirements. As far as the reference domain is concerned, a self-heating thermal resistance amounting to 481 K/W was evaluated, whilst 362 K/W was obtained for the bulk-silicon counterpart (i.e., the corresponding trench-free device). An increase of 33% was therefore observed, as a consequence of the heat confinement within the trench well. Numerical simulations also evidenced that the contribution to the overall thermal resistance due to the heat flow within the trench box (i.e., the flow along the path from heat source to trench bottom) amounts to about 60% in the reference transistor.

In this investigation, the heat transfer capability of the trench sidewalls was analyzed by numerically evaluating the distribution of the corresponding heat transfer coefficient, which is defined as[12]

$$h(x,y,z)\big|_S = \frac{f(x,y,z)\big|_S}{T(x,y,z)\big|_S - T_{AMB}} \tag{3.1}$$

where $f(x,y,z)\big|_S$ [W/μm^2] and $T(x,y,z)\big|_S$ [K] are the normal heat flux distribution and temperature field over the sidewall S, respectively, and T_{AMB} is the ambient temperature.

The main results of the numerical investigation are in order:

1. The assumption of adiabatic trench walls (as in [7], [8]) leads to an error amounting to 10% when evaluating the self-heating thermal resistance of the reference structure. Moreover, such a discrepancy increases for DTI devices with deeper and/or poly-filled trenches, where the heat loss through the trench

---

[11] For trench-isolated transistors with heat source centered within the trench box (i.e., located symmetrically between the trench sidewalls, as for the reference domain) only one quarter of the structure was simulated.

[12] The heat transfer coefficient represents an indicator of the surface capability to transfer heat. In an electrical analogy, with voltage drop and current density corresponding with temperature increase over ambient and heat flux, respectively, the heat transfer coefficient can be reviewed as a specific conductance.

plays a more important role.[13] This demonstrates that the lateral heat dissipation via trench cannot be safely neglected with respect to the downward heat flow in modeling approaches.

2. The distribution of heat transfer coefficient over the trench sidewalls is actually nonuniform, as evidenced in Fig. 3.3. It can be observed that: (i) a sharp growth occurs along the edges between lateral trench surfaces; (ii) a lower, and almost constant, value is reached far away the borders; (iii) both the (low) *plateau* and the (high) edge values reduce in the proximity of the bottom of the silicon-only trench box.
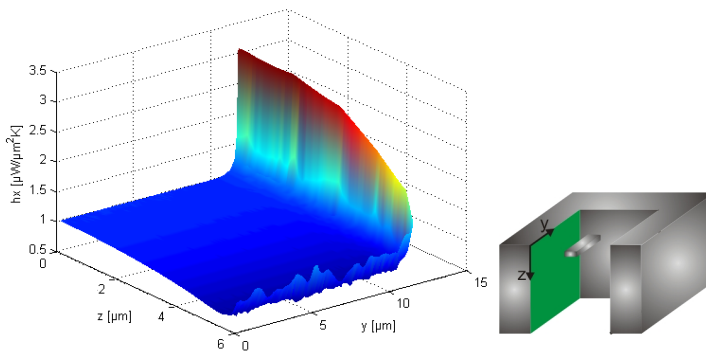
Fig. 3.3. Heat transfer coefficient distribution over half of the trench sidewall as evaluated by numerical simulations for the reference domain.

A large number of 3-D numerical simulations evidenced that this qualitative behavior is independent of the domain geometry.

3. Contrarily to the simplifying assumption adopted in [7], the temperature and heat flux distributions over the bottom of the trench box may be significantly nonuniform in various cases. As an evidence, Fig. 3.4 shows the distribution of the temperature rise above ambient normalized to dissipated power over the trench bottom of the reference domain. As can be

---

[13] When replacing the silicon dioxide trench with a poly-filled one in the reference domain, the error exceeds 15%.

seen, the normalized temperature ranges from 140 to more than 210 K/W, which occurs at the projection of the heat source. An even larger temperature gradient is observed for small trench depths (i.e., small heights of the trench box) and high box-to-source size ratios.[14]
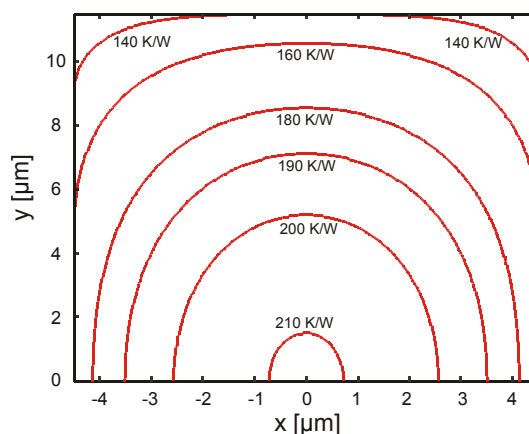
Fig. 3.4. Contour plots of the temperature rise above ambient normalized to dissipated power over half of the trench bottom (located at $z = d_t$) for the reference domain, as obtained by 3-D numerical simulations.

In principle, an analytical model predicting the temperature field in a DTI transistor should accurately describe the heat loss through the trench and the heat flow from the trench box toward the substrate. However, this is undeniably not a trivial task due to the numerical analysis results. In fact, it was observed that:

1. the trench sidewalls exhibit an uneven capability to transfer heat out of the trench box;
2. the temperature and flux distributions arising over the trench bottom are nonuniform.

In order to properly account for these features in a mathematically treatable problem, we conceived a modeling approach that can be summarized as follows.

---

[14] As concerns a DTI structure with $d_t = 3$ μm and all other technological parameters equal to those of the reference transistor, the normalized temperature over the bottom of the trench box is numerically evaluated to span from 115 to 250 K/W.

1. First, we represent the actual DTI structure under analysis with a simplified one (Fig. 3.2c and d) that is partitioned into two subdomains, namely, one corresponding to the silicon box surrounded by the trench (i.e., the trench box, also referred to as *subdomain 1*) and another corresponding to the underlying silicon substrate (also indicated as *subdomain 2*). In the following, all the quantities related to subdomains 1 and 2 are denoted by subscripts 1 and 2, respectively.

2. Let us refer to subdomain 1. Similarly to the approaches exploited in [12] for trench-isolated transistors and in [13] for fully-isolated DTI devices on silicon-on-insulator substrates, we assume convective boundary conditions[15] at the lateral sidewalls to describe the heat propagation that takes place through the trench in the actual structure. In principle these conditions should account for the nonuniform distribution of the heat transfer coefficients. Nevertheless, an extensive numerical analysis was performed, which demonstrated that the thermal behavior of subdomain 1 can be accurately reproduced by associating an optimized h value to the four lateral sidewalls of the trench box. This implies that the heat loss through the trench can be conveniently described by adopting convective boundary conditions that simply involve this common h value.

3. In order to accurately model the uneven heat flow through the trench bottom, we resort to a procedure similar to that recently proposed for the thermal analysis of flip-chip mounted semiconductor optical amplifiers [14]: the interface is partitioned into a given number of elementary rectangles, each of them characterized by a uniform heat flux.

4. Subdomain 2 is modeled as a laterally infinite domain with isothermal bottom surface at ambient temperature, and top surface adiabatic everywhere except for the interface with subdomain 1.

---

[15] As already discussed in Chapter 2 for the case of trench-isolated bipolar transistors on SOI substrates, the *convective* condition is used to describe a heat *conduction* phenomenon, namely, the heat transfer through the trench sidewalls.

5. The temperature expressions are evaluated in both subdomains as a function of the unknown fluxes at the interface using standard procedures. Subsequently, the temperature continuity is imposed at the centers of all the elementary rectangles in which the interface is discretized. This allows calculating the fluxes, and, consequently, the temperature field in both subdomains.

3.2   Heat transfer coefficients empirical model

The proposed approach obviously requires a proper choice of the h value (uniform and common to the four lateral surfaces) to be included in the model for simulating an assigned trench-isolated transistor, since h represents a tuning parameter to describe the outward flux through the trench sidewalls. In [12], an approach is proposed, which involves the optimization of such a parameter so as to guarantee the best fit with numerical results. However, the resulting model is not predictive due to the need for a 3-D numerical simulation for any domain under analysis. In order to overcome this drawback, we evaluated an analytical law that empirically relates the heat transfer coefficient to all technological parameters playing a role. The derivation of this law is based on a preliminary analysis that can be summarized as follows.

➢ A custom routine to automatically extract the h value that yields the best agreement with the numerical temperature field corresponding to a given domain was developed.
➢ This extraction was performed for a large number of DTI devices in order to cover the parameter ranges reported in Table 3.1.

It was evidenced that h is dependent upon trench thickness t_t and depth d_t, while being almost insensitive to width W and length L of the trench box.

Based on the evaluated dataset, the following empirical law was determined for the heat transfer coefficient:

$$h = (A \cdot e^{-a \cdot d_t} + B) \cdot t_t^{-b} \tag{3.2}$$

where the fitting parameters *A, B, a,* and *b* were adjusted through *least-squares* optimization routines for the case of fully oxide-filled trenches. The values are listed in Table 3.2.

Table 3.2
Optimized values for the fitting parameters adopted in Eq. (3.2).

symbol	value
a	0.409
b	0.54
A	3.84×10^{-6}
B	1.19×10^{-6}

Eq. (3.2) can be straightforwardly extended to the case of silicon dioxide lined trenches with polysilicon fill (as in e.g., [1], [2]) by means of the procedure adopted in Chapter 2 for the case of DTI SOI bipolar transistors [13]. It relies on the assumption of trenches filled with a homogeneous material with thermal conductivity k_m obtained by a weighted average of the polysilicon and oxide layers as

$$k_m = t_t \cdot \left(\frac{2 \cdot t_{OX,t}}{k_{OX}} + \frac{t_{poly}}{k_{poly}} \right)^{-1} \tag{3.3}$$

where $t_{OX,t}$ and k_{OX} are the thickness and thermal conductivity of the oxide layers, respectively, and t_{poly} and k_{poly} are the thickness and thermal conductivity of the polysilicon layer.

Also in this case the accuracy of Eq. (3.3), which exactly works for a 1-D problem, was verified by performing a large number of 3-D numerical simulations of the actual trench-isolated transistor and a simplified structure obtained by filling the trench with a homogeneous material with thermal conductivity equal to k_m. This analysis was carried out by covering the wide k_{poly} range spanning from 1×10^{-5} to 5×10^{-5} W/μmK, in which this parameter, as it was claimed in Chapter 2, can vary depending on various factors, e.g., deposition temperature, average grain size, dopant type and concentration [15]-[17].

In conclusion, in order to account for the case of silicon dioxide lined trenches with polysilicon fill, Eq. (3.2) was modified by simply multiplying the RHS by $\left(k_m / k_{OX} \right)^{\alpha}$ with $\alpha = 0.216 \cdot d_t^{0.5}$, while keeping all other empirical parameters equal to those extracted for oxide-filled trenches:

$$h = (A \cdot e^{-a \cdot d_t} + B) \cdot t_t^{-b} \left(\frac{k_m}{k_{OX}} \right)^{0.216 \cdot \sqrt{d_t}} \tag{3.4}$$

Fig. 3.5 shows the heat transfer coefficient behavior as a function of d_t, t_t, and k_m as obtained by the above model and by extracting the optimum h values from the numerical temperature field. As can be seen, the heat transfer capability of the trench sidewalls reduces with increasing trench thickness and depth, and grows with increasing the average thermal conductivity associated with the trench. An inspection of the figure also reveals that the empirical relationships presented above are fairly accurate within the ranges of technological parameters playing a role, thus avoiding the need for further numerical h extractions.
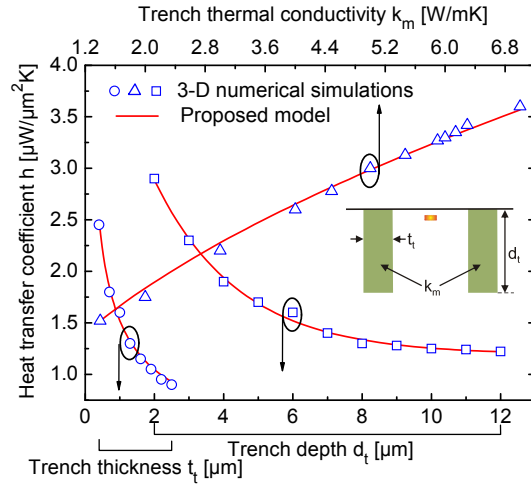
Fig. 3.5. Heat transfer coefficient as a function of trench thickness, trench depth, and average thermal conductivity of the material filling the trenches. The model (solid lines) is compared to the optimized values extracted from numerical simulations (symbols).

3.3   The analytical thermal model

In this Paragraph, the expressions of the temperature field under steady-state conditions in subdomains 1 and 2 are derived.

3.3.1 The temperature field in subdomain 1

Subdomain 1 is represented as a silicon-only rectangular parallelepiped – coinciding with the trench box – with adiabatic top surface, convective boundary conditions at lateral faces, and bottom surface characterized by a nonuniform outward heat flux (Fig. 3.6).
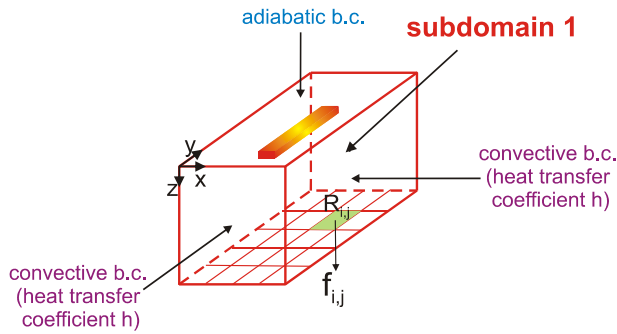
Fig. 3.6. Subdomain 1 with the adopted boundary conditions.

By resorting to the *effects superposition principle* (ESP), the temperature rise above ambient at an arbitrary point $\vec{r} = (x, y, z)$ can be calculated as

$$\vartheta_1(\vec{r}) = T_1(\vec{r}) - T_{AMB} = \vartheta_{1,P}(\vec{r}) + \vartheta_{1,f}(\vec{r}) \tag{3.5}$$

where the terms $\vartheta_{1,P}(\vec{r})$ and $\vartheta_{1,f}(\vec{r})$ account for the power dissipated by the heat source and the (uneven) outward flux through the partitioned bottom interface, respectively.

The contribution $\vartheta_{1,P}(\vec{r})$ (Fig. 3.7) satisfies the steady-state heat flow equation given by [Eq. (C.7)]:

$$\nabla^2 \vartheta_{1,P}(\vec{r}) + \frac{g(\vec{r})}{k} = 0 \tag{3.6}$$

where k is the thermal conductivity [W/μmK] of silicon, and $g(\vec{r})$ is the nonzero power density [W/μm^3] dissipated by the heat source.
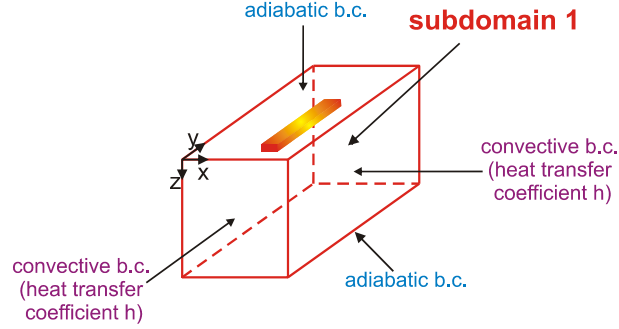
Fig. 3.7. Subdomain 1: $\vartheta_{1,P}(\vec{r})$ contribution.

The power dissipation region is modeled as either a rectangular indefinitely thin heat source (THS) embedded within the silicon domain or a volumetric heat source (VHS) shaped as a rectangular parallelepiped.[16] Let us denote as x_1, x_2, y_1, y_2 the heat source coordinates along the x and y axis, respectively. As far as the THS case is concerned, the heat source is assumed to be placed at depth $z = d_{HS}$. For the VHS case, z_1 and z_2 represent the heat source coordinates along the z axis. As for the numerical analysis, a uniform dissipation is assumed within the heat source region.

The convective boundary conditions at the lateral surfaces are expressed as follows [Eqs. (C.8) and (C.9)]:

$$k \left. \frac{\partial \vartheta_{1,P}(\vec{r})}{\partial n} \right|_S + h \vartheta_{1,P}(\vec{r}) \big|_S = 0 \qquad (3.7)$$

where h is the heat transfer coefficient associated with the surface S and n denotes the outward-drawn normal to S. According to the results of the preliminary numerical analysis, h is nonuniform over the sidewalls, so that this parameter should be in principle considered as a function of the arbitrary point of S in Eq. (3.7). However, as discussed in Paragraph 3.2, the heat evacuation through the lateral sidewalls of

---

[16] As discussed in [18] for bulk-silicon devices, the modeling solution of a THS located at a proper nonzero depth d_{HS} (e.g., at the base-collector junction) allows accurately describing the temperature field except for $z \to d_{HS}$, where the peak predicted is higher than the numerical data due to the volumetric nature of the power dissipation region.

subdomain 1 can be suitably described by adopting the *h* value given by Eq. (3.2).

The adiabatic conditions at the top and bottom surfaces are given by [Eq. (C.10)]:

$$\frac{\partial \vartheta_{1,P}(\vec{r})}{\partial z}\bigg|_{z=0,d_t} = 0 \tag{3.8}$$

The above defined heat flow problem can be solved by resorting to the separation of variables technique; as a result, the temperature increase over ambient $\vartheta_{1,P}(\vec{r})$ can be expressed in terms of a double Fourier series

$$\vartheta_{1,P}(\vec{r}) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} X_n(x) Y_m(y) Z_{nm,P}(z) \tag{3.9}$$

where the eigenfunctions $X_n(x)$, $Y_m(y)$, and $Z_{nm,P}(z)$ can be evaluated by means of a standard procedure [19] and depend upon the heat transfer coefficient *h*. In particular, $X_n(x)$ and $Y_m(y)$ are defined as follows:

$$X_n(x) = \frac{\beta_n \cdot \overline{X}_n(x) + A \cdot \overline{\overline{X}}_n(x)}{D_n} \tag{3.10}$$

$$Y_m(y) = \frac{\alpha_m \cdot \overline{Y}_m(y) + A \cdot \overline{\overline{Y}}_m(y)}{E_m} \tag{3.11}$$

being $\overline{X}_n(x) = \cos(\beta_n x)$, $\overline{\overline{X}}_n(x) = \sin(\beta_n x)$, $\overline{Y}_m(y) = \cos(\alpha_m y)$, $\overline{\overline{Y}}_m(y) = \sin(\alpha_m y)$, $A = h/k$, and

$$D_n = \left[\left(\beta_n^2 + A^2 \right) \cdot \frac{W}{2} + A \right]^{1/2} \tag{3.12}$$

$$E_m = \left[\left(\alpha_m^2 + A^2 \right) \cdot \frac{L}{2} + A \right]^{1/2} \tag{3.13}$$

In the THS case, the eigenfunctions $Z_{nm,P}(z)$ are given by

$$Z_{nm,P}(z) = \frac{P_D}{\Gamma} \cdot \frac{G_{nm}}{\gamma_{nm} \cdot k} \cdot \frac{\bar{\bar{Z}}_{nm}(d_t - d_{HS})}{\bar{\bar{Z}}_{nm}(d_t)} \cdot \bar{Z}_{nm}(z) + \tag{3.14}$$

$$+ \begin{cases} 0 & z < d_{HS} \\ \dfrac{P_D}{\Gamma} \cdot \dfrac{G_{nm}}{\gamma_{nm} \cdot k} \cdot \bar{\bar{Z}}_{nm}(d_{HS} - z) & z \geq d_{HS} \end{cases}$$

while for the VHS case they are expressed as

$$Z_{nm,P}(z) = \frac{P_D}{\Gamma} \cdot \frac{G_{nm}}{\gamma_{nm}^2 \cdot k} \cdot \frac{\bar{\bar{Z}}_{nm}(z_2 - d_t) - \bar{\bar{Z}}_{nm}(z_1 - d_t)}{\bar{\bar{Z}}_{nm}(d_t)} \times \tag{3.15}$$

$$\times \bar{Z}_{nm}(z) + \begin{cases} 0 & z < z_1 \\ \dfrac{P_D}{\Gamma} \cdot \dfrac{G_{nm}}{\gamma_{nm}^2 \cdot k} \cdot \left[1 - \bar{Z}_{nm}(z_1 - z) \right] & z_1 \leq z \leq z_2 \\ \dfrac{P_D}{\Gamma} \cdot \dfrac{G_{nm}}{\gamma_{nm}^2 \cdot k} \times & z > z_2 \\ \qquad \times \left[\bar{Z}_{nm}(z_2 - z) - \bar{Z}_{nm}(z_1 - z) \right] \end{cases}$$

where $\bar{Z}_{nm}(z) = \cosh(\gamma_{nm} z)$, $\bar{\bar{Z}}_{nm}(z) = \sinh(\gamma_{nm} z)$, $\gamma_{nm}^2 = \beta_n^2 + \alpha_m^2$, P_D [W] is the overall power dissipated by the heat source, Γ represents the heat source area ($W_{HS} \cdot L_{HS}$) for the THS case or the heat source volume ($W_{HS} \cdot L_{HS} \cdot t_{HS}$) for the VHS case, and the G_{nm} terms are expressed as

$$G_{nm} = \frac{1}{D_n \cdot E_m} \times \tag{3.16}$$

$$\times \left\{ \bar{\bar{X}}_n(x_2) - \bar{\bar{X}}_n(x_1) - \frac{A}{\beta_n} \left[\bar{X}_n(x_2) - \bar{X}_n(x_1) \right] \right\} \times$$

$$\times \left\{ \bar{\bar{Y}}_m(y_2) - \bar{\bar{Y}}_m(y_1) - \frac{A}{\alpha_m} \left[\bar{Y}_m(y_2) - \bar{Y}_m(y_1) \right] \right\}$$

The eigenvalues β_n and α_m can be found by solving the transcendental equations given by

$$\tan\left(\beta_n \cdot W\right) = \frac{2 \cdot A \cdot \beta_n}{\beta_n^2 - A^2} \tag{3.17}$$

$$\tan\left(\alpha_m \cdot L\right) = \frac{2 \cdot A \cdot \alpha_m}{\alpha_m^2 - A^2} \tag{3.18}$$

The derivation of Eqs. (3.9)-(3.18) is discussed in detail in Appendix C[17].

The (negative) contribution $\vartheta_{1,f}\left(\vec{r}\right)$ [see Eq. (3.5)] represents the solution of the heat flow equation with zero power dissipation (Fig. 3.8), i.e. [Eq. (D.7)]:

$$\nabla^2 \vartheta_{1,f}\left(\vec{r}\right) = 0 \tag{3.19}$$
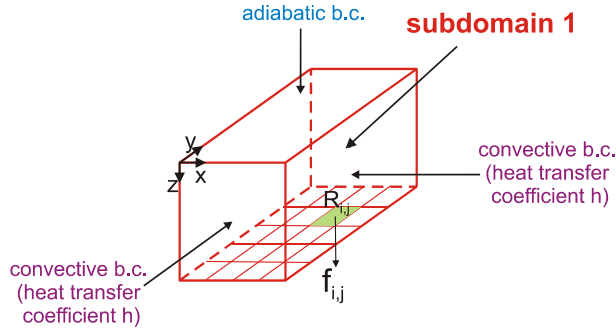
Fig. 3.8. Subdomain 1: $\vartheta_{1,f}\left(\vec{r}\right)$ contribution.

The boundary conditions at the lateral sidewalls and top surface are expressed by Eqs. (3.7) and (3.8), respectively, while a nonzero – and nonuniform – outward heat flux $\overline{f}\left(x,y\right)$ is assumed at the bottom surface (i.e., the interface with subdomain 2), that is,

$$-k \left.\frac{\partial \vartheta_{1,f}\left(\vec{r}\right)}{\partial z}\right|_{z=d_t} = \overline{f}\left(x,y\right) \tag{3.20}$$

---

[17] The equations derived in Appendix C must be particularized for $h_{x0} = h_{xW} = h_{y0} = h_{yL} = h$ and $B_1 = B_2 = C_1 = C_2 = A$.

As mentioned in Paragraph 3.2, the uneven heat flow from the trench box to the substrate is described by partitioning the trench bottom into $R_x \times R_y$ elementary rectangles, each of them characterized by a uniform outward heat flux f_{ij}, namely, the nonuniform heat flux distribution is approximated as

$$\overline{f}(x,y) = f_{ij} \qquad \forall (x,y) \in R_{ij} \tag{3.21}$$

being R_{ij} an arbitrary rectangle. Consequently, $\vartheta_{1,f}(\vec{r})$ can be evaluated by ESP as the sum of individual contributions $\vartheta_{1,f_{ij}}(\vec{r})$ (Fig. 3.9), each obtained by enabling one of the fluxes f_{ij} and keeping the others equal to zero (i.e., considering all the elementary rectangles adiabatic except for one), that is,

$$\vartheta_{1,f}(\vec{r}) = \sum_{i=1}^{R_y} \sum_{j=1}^{R_x} \vartheta_{1,f_{ij}}(\vec{r}) \tag{3.22}$$
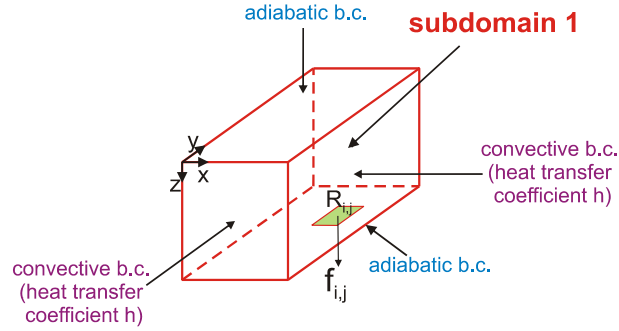
Fig. 3.9. Subdomain 1: $\vartheta_{1,f_{ij}}(\vec{r})$ contribution.

Analogously to $\vartheta_{1,f}(\vec{r})$, the elementary terms $\vartheta_{1,f_{ij}}(\vec{r})$ must satisfy the heat flow equation given by Eq. (3.19) and the boundary conditions expressed by Eqs. (3.7) and (3.8) for the lateral and top surfaces, respectively, whereas the boundary condition at the trench bottom becomes [Eq. (D.11)]:

$$-k \left. \frac{\partial \vartheta_{1,f_{ij}}(\vec{r})}{\partial z} \right|_{z=d_t} = \begin{cases} f_{ij} & \forall (x,y) \in R_{ij} \\ 0 & \text{elsewhere} \end{cases} \tag{3.23}$$

As for $\vartheta_{1,P}(\vec{r})$, the temperature rises $\vartheta_{1,f_{ij}}(\vec{r})$ can be expressed as a double Fourier series

$$\vartheta_{1,f_{ij}}(\vec{r}) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} X_n(x)Y_m(y)Z_{nm,f_{ij}}(z) \qquad (3.24)$$

where the eigenfunctions $X_n(x)$ and $Y_m(y)$ are given by Eqs. (3.10) and (3.11), respectively. The eigenfunctions $Z_{nm,f_{ij}}(z)$ are linearly dependent on the unknown heat fluxes f_{ij} and are given by

$$Z_{nm,f_{ij}}(z) = \frac{F_{nm,f_{ij}}}{\gamma_{nm} \cdot \overline{\overline{Z}}_{nm}(d_t)} \cdot \overline{Z}_{nm}(z) \qquad (3.25)$$

where

$$F_{nm,f_{ij}} = -\frac{f_{ij}}{k \cdot D_n \cdot E_m} \times \qquad (3.26)$$

$$\times \left\{ \overline{\overline{X}}_n(x_{jF}) - \overline{\overline{X}}_n(x_{j0}) - \frac{A}{\beta_n}\left[\overline{X}_n(x_{jF}) - \overline{X}_n(x_{j0})\right] \right\} \times$$

$$\times \left\{ \overline{\overline{Y}}_m(y_{iF}) - \overline{\overline{Y}}_m(y_{i0}) - \frac{A}{\alpha_m}\left[\overline{Y}_m(y_{iF}) - \overline{Y}_m(y_{i0})\right] \right\}$$

The derivation of Eqs. (3.24)-(3.26) is discussed in detail in Appendix D[18].

Fig. 3.10 shows the interface between subdomains 1 and 2.

Let us note that:

$$x_{j0} = \frac{j-1}{R_x}W = \frac{j}{R_x}W - \frac{W}{R_x} = x_{jF} - \frac{W}{R_x}$$

therefore, recalling that:

➢ $\sin(\alpha - \beta) = \sin\alpha\cos\beta - \cos\alpha\sin\beta$

➢ $\cos(\alpha - \beta) = \cos\alpha\cos\beta + \sin\alpha\sin\beta$

---

[18] The equations derived in Appendix D must be particularized for $h_{x0} = h_{xW} = h_{y0} = h_{yL} = h$ and $B_1 = B_2 = C_1 = C_2 = A$.
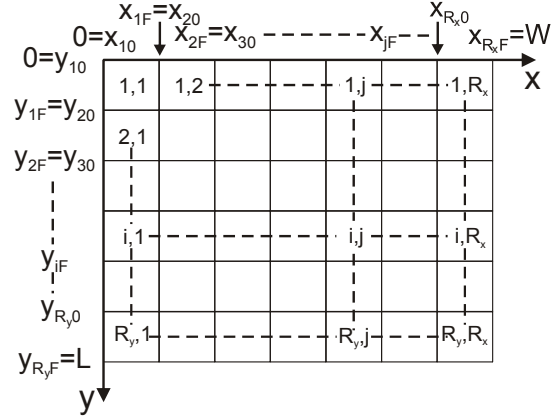
Fig. 3.10. Partitioned interface between subdomain 1 and subdomain 2.

> $\sin\alpha = 2\sin\dfrac{\alpha}{2}\cos\dfrac{\alpha}{2}$

> $\cos\alpha = 1 - 2\sin^2\dfrac{\alpha}{2}$

we can observe that:

$$\bar{\bar{X}}_n\left(x_{jF}\right) - \bar{\bar{X}}_n\left(x_{j0}\right) = \sin\left(\beta_n x_{jF}\right) - \sin\left(\beta_n x_{j0}\right) =$$

$$= \sin\left(\beta_n x_{jF}\right) - \sin\left(\beta_n x_{jF} - \beta_n\frac{W}{R_x}\right) =$$

$$= \sin\left(\beta_n x_{jF}\right) - \sin\left(\beta_n x_{jF}\right)\cos\left(\frac{\beta_n W}{R_x}\right) + \cos\left(\beta_n x_{jF}\right)\sin\left(\frac{\beta_n W}{R_x}\right) =$$

$$= \sin\left(\beta_n x_{jF}\right) - \sin\left(\beta_n x_{jF}\right)\left[1 - 2\sin^2\left(\beta_n\frac{W}{2R_x}\right)\right] +$$

$$+ \cos\left(\beta_n x_{jF}\right)2\sin\left(\beta_n\frac{W}{2R_x}\right)\cos\left(\beta_n\frac{W}{2R_x}\right) =$$

$$= 2\sin\left(\beta_n x_{jF}\right)\sin^2\left(\beta_n\frac{W}{2R_x}\right) +$$

$$+ 2\cos\left(\beta_n x_{jF}\right)\sin\left(\beta_n\frac{W}{2R_x}\right)\cos\left(\beta_n\frac{W}{2R_x}\right) =$$

$$= 2\sin\left(\beta_n \frac{W}{2R_x}\right)\left[\sin\left(\beta_n x_{jF}\right)\sin\left(\beta_n \frac{W}{2R_x}\right)+\right.$$

$$\left.+\cos\left(\beta_n x_{jF}\right)\cos\left(\beta_n \frac{W}{2R_x}\right)\right]=$$

$$= 2\sin\left(\beta_n \frac{W}{2R_x}\right)\cos\left[\beta_n\left(x_{jF}-\frac{W}{2R_x}\right)\right]$$

$$= 2\bar{\bar{X}}_n\left(\frac{W}{2R_x}\right)\bar{X}_n\left(x_{jF}-\frac{W}{2R_x}\right)= 2\cdot\bar{\bar{X}}_n\left(\bar{x}\right)\cdot\bar{X}_n\left(x_j\right) \qquad (3.27)$$

where $\bar{x}=W/\left(2\cdot R_x\right)$, and $x_j=\bar{x}\cdot\left(2\cdot j-1\right)$;

and:

$$\bar{X}_n\left(x_{jF}\right)-\bar{X}_n\left(x_{j0}\right)=\cos\left(\beta_n x_{jF}\right)-\cos\left(\beta_n x_{j0}\right)=$$

$$= \cos\left(\beta_n x_{jF}\right)-\cos\left(\beta_n x_{jF}-\beta_n \frac{W}{R_x}\right)=$$

$$= \cos\left(\beta_n x_{jF}\right)-\cos\left(\beta_n x_{jF}\right)\cos\left(\beta_n \frac{W}{R_x}\right)-$$

$$-\sin\left(\beta_n x_{jF}\right)\sin\left(\beta_n \frac{W}{R_x}\right)=$$

$$= \cos\left(\beta_n x_{jF}\right)-\cos\left(\beta_n x_{jF}\right)\left[1-2\sin^2\left(\beta_n \frac{W}{2R_x}\right)\right]+$$

$$-\sin\left(\beta_n x_{jF}\right)2\sin\left(\beta_n \frac{W}{2R_x}\right)\cos\left(\beta_n \frac{W}{2R_x}\right)=$$

$$= 2\cos\left(\beta_n x_{jF}\right)\sin^2\left(\frac{\beta_n W}{2R_x}\right)-$$

$$-2\sin\left(\beta_n x_{jF}\right)\sin\left(\frac{\beta_n W}{2R_x}\right)\cos\left(\frac{\beta_n W}{2R_x}\right)=$$

$$= 2\sin\left(\frac{\beta_n W}{2R_x}\right)\left[\cos\left(\beta_n x_{jF}\right)\sin\left(\frac{\beta_n W}{2R_x}\right) - \right.$$

$$\left. -\sin\left(\beta_n x_{jF}\right)\cos\left(\frac{\beta_n W}{2R_x}\right)\right] =$$

$$= -2\sin\left(\beta_n \frac{W}{2R_x}\right)\sin\left[\beta_n\left(x_{jF} - \frac{W}{2R_x}\right)\right]$$

$$= -2\bar{\bar{X}}_n\left(\frac{W}{2R_x}\right)\bar{\bar{X}}_n\left(x_{jF} - \frac{W}{2R_x}\right) = -2\cdot\bar{\bar{X}}_n\left(\bar{x}\right)\cdot\bar{\bar{X}}_n\left(x_j\right) \qquad (3.28)$$

Analogously:

$$\bar{\bar{Y}}_m\left(y_{iF}\right) - \bar{\bar{Y}}_m\left(y_{i0}\right) = 2\cdot\bar{\bar{Y}}_m\left(\bar{y}\right)\cdot\bar{Y}_m\left(y_i\right) \qquad (3.29)$$

$$\bar{Y}_m\left(y_{iF}\right) - \bar{Y}_m\left(y_{i0}\right) = -2\cdot\bar{Y}_m\left(\bar{y}\right)\cdot\bar{\bar{Y}}_m\left(y_i\right) \qquad (3.30)$$

where $\bar{y} = L/\left(2\cdot R_y\right)$, and $y_i = \bar{y}\cdot\left(2\cdot i - 1\right)$.

Therefore, substituting Eqs. (3.27)-(3.30) into Eq. (3.25) combined with Eq. (3.26), we have:

$$Z_{nm,f_{ij}}\left(z\right) = -\frac{4\cdot f_{ij}\cdot\bar{\bar{X}}_n\left(\bar{x}\right)\cdot\bar{\bar{Y}}_m\left(\bar{y}\right)}{k\cdot\gamma_{nm}\cdot D_n\cdot E_m\cdot\bar{\bar{Z}}_{nm}\left(d_t\right)}\cdot\bar{Z}_{nm}\left(z\right)\times \qquad (3.31)$$

$$\times\left[\bar{X}_n\left(x_j\right) + \frac{A}{\beta_n}\cdot\bar{\bar{X}}_n\left(x_j\right)\right]\cdot\left[\bar{Y}_m\left(y_i\right) + \frac{A}{\alpha_m}\cdot\bar{\bar{Y}}_m\left(y_i\right)\right]$$

3.3.2   The temperature field in subdomain 2

As stated in Paragraph 3.2, subdomain 2 is represented as a laterally infinite domain[19] with isothermal bottom surface at ambient

---

[19] The assumption of a laterally infinite domain does not affect the model accuracy since the DTI device is assumed to be embedded in a silicon chip, whose edges – typically located far away from active area and trench bottom – negligibly influence the temperature field. Nevertheless, the model can be straightforwardly extended to account for adiabatic lateral faces by horizontally applying the image method, namely, adding lateral fictitious sources.

temperature and top surface adiabatic everywhere except for the interface with subdomain 1, where a nonuniform inward flux is assumed (Fig. 3.11).
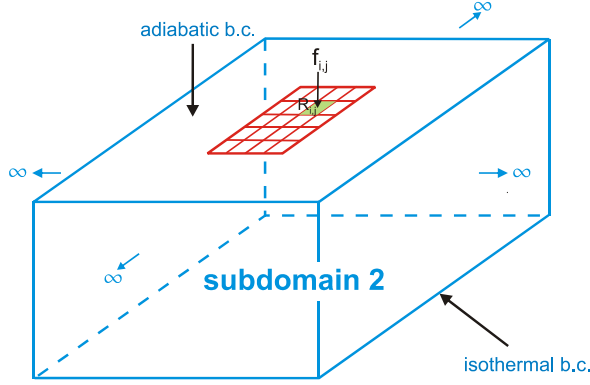
Fig. 3.11. Subdomain 2 with the adopted boundary conditions.

As for $\vartheta_{1,f}(\vec{r})$, the temperature increase above ambient at an arbitrary point $\vec{r}$ can be evaluated via ESP by summing the elementary contributions due to the unknown heat fluxes f_{ij} as

$$\vartheta_2(\vec{r}) = \sum_{i=1}^{R_y}\sum_{j=1}^{R_x} \vartheta_{2,f_{ij}}(\vec{r}) \tag{3.32}$$

The expressions of terms $\vartheta_{2,f_{ij}}(\vec{r})$ (Fig. 3.12) are derived through the technique adopted in e.g., [6], [20], (see Appendix E for the details).
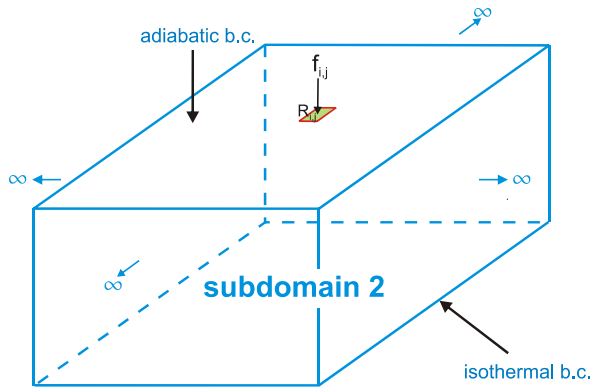
Fig. 3.12. Subdomain 1: $\vartheta_{2,f_{ij}}(\vec{r})$ contribution.

If the boundary condition at the bottom surface is disregarded by considering the simplified problem of a semi-infinite homogeneous medium with adiabatic top surface and a THS coinciding with the elementary rectangle R_{ij} and dissipating a power density equal to f_{ij}, the expression of the temperature field is given by

$$\vartheta_{20,ij}(x,y,z) = \frac{f_{ij}}{2 \cdot \pi \cdot k} \times \tag{3.33}$$

$$\times \begin{bmatrix} \psi(\delta x_j, \delta y_i, \delta z) - \psi(\delta x_j, \delta y_{i-1}, \delta z) \\ -\psi(\delta x_{j-1}, \delta y_i, \delta z) + \psi(\delta x_{j-1}, \delta y_{i-1}, \delta z) \end{bmatrix}$$

where

$$\psi(\delta x, \delta y, z) = -\delta z \cdot \arctan \frac{\delta x \cdot \delta y}{\delta z \cdot \sqrt{\delta x^2 + \delta y^2 + \delta z^2}} + \tag{3.34}$$

$$+ \delta x \cdot \log\left[\delta y + \sqrt{\delta x^2 + \delta y^2 + \delta z^2} \right] +$$

$$+ \delta y \cdot \log\left[\delta x + \sqrt{\delta x^2 + \delta y^2 + \delta z^2} \right]$$

being $\delta x_j = x - 2 \cdot j \cdot \overline{x}$, $\delta y_i = y - 2 \cdot i \cdot y_i$, and $\delta z = z - d_t$.

Eq. (3.33), also referred to as 0th-order solution [6], does not account for the finite thickness of the chip (300 μm for the case under analysis), i.e., the temperature field $\vartheta_{20,ij}(x,y,z)$ is not influenced by the isothermal boundary condition at the bottom surface. In order to include this effect without affecting the adiabatic condition at the top, a series of vertical fictitious mirror sources can be added [6], [20]. The pth-order solution is given by [6]

$$\vartheta_{2,f_{ij}}(x,y,z) = \sum_{v=1}^{p} \begin{bmatrix} (-1)^{v-1} \cdot \vartheta_{20,ij}(x,y,z+2\cdot(v-1)\cdot H) \\ +(-1)^v \cdot \vartheta_{20,ij}(x,y,z-2\cdot v\cdot H) \end{bmatrix} \tag{3.35}$$

being H the thickness of subdomain 2 (see Fig. 3.2a).

The derivation of Eqs. (3.33)-(3.35) is discussed in detail in Appendix E.

3.3.3 The temperature field in the overall domain

Once the temperature expressions have been evaluated in both subdomains as a function of the unknown fluxes f_{ij}, the temperature continuity is imposed at the centers of all the elementary rectangles R_{ij}, that is,

$$\vartheta_1\left(x_j, y_i, d_t\right) = \vartheta_2\left(x_j, y_i, d_t\right) \tag{3.36}$$

Solving the resulting linear system of $R_x \times R_y$ equations allows determining the fluxes f_{ij} so that the temperature field can be evaluated in both subdomains.

3.3.4 The self-heating thermal resistance

Having determined the temperature distribution in subdomain 1, we are in a position to evaluate the self-heating thermal resistance R_{TH}, that is, also in this analysis, calculated as the average of the temperature rise above ambient normalized to the dissipated power over the heat source projection on the top surface, i.e.,

$$R_{TH} = \frac{1}{P_D \cdot W_{HS} \cdot L_{HS}} \cdot \int_{x_1}^{x_2} \int_{y_1}^{y_2} \vartheta_1\left(x, y, 0\right) dy dx \tag{3.37}$$

Substituting Eq. (3.5) into Eq. (3.37), and using Eqs. (3.9), (3.22), and (3.24), we obtain

$$R_{TH} = \frac{1}{P_D \cdot W_{HS} \cdot L_{HS}} \times \tag{3.38}$$

$$\times \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \left\{ \begin{bmatrix} Z_{nm,P}\left(z=0\right) + \sum_{i=1}^{R_y} \sum_{j=1}^{R_x} Z_{nm,f_{ij}}\left(z=0\right) \end{bmatrix} \times \\ \times \int_{x_1}^{x_2} X_n\left(x\right) dx \cdot \int_{y_1}^{y_2} Y_m\left(y\right) dy \right\}$$

Combining Eq. (3.38) with Eqs. (3.10), (3.11), and (3.16) yields

$$R_{TH} = \frac{1}{P_D \cdot W_{HS} \cdot L_{HS}} \times \tag{3.39}$$

$$\times \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} G_{nm} \cdot \left[Z_{nm,P}(z=0) + \sum_{i=1}^{R_y} \sum_{j=1}^{R_x} Z_{nm,f_{ij}}(z=0) \right]$$

where from Eqs. (3.14) and (3.15)

$$Z_{nm,P}(z=0) = \frac{P_D}{\Gamma} \cdot \frac{G_{nm}}{\gamma_{nm} \cdot k} \cdot \frac{\bar{Z}_{nm}(d_t - d_{HS})}{\bar{\bar{Z}}_{nm}(d_t)} \tag{3.40}$$

and

$$Z_{nm,P}(z=0) = \frac{P_D}{\Gamma} \cdot \frac{G_{nm}}{\gamma_{nm}^2 \cdot k} \cdot \frac{\bar{\bar{Z}}_{nm}(z_2 - d_t) - \bar{\bar{Z}}_{nm}(z_1 - d_t)}{\bar{\bar{Z}}_{nm}(d_t)} \tag{3.41}$$

for the THS and VHS cases, respectively, and from Eq. (3.31)

$$Z_{nm,f_{ij}}(z=0) = -\frac{4 \cdot f_{ij} \cdot \bar{\bar{X}}_n(\bar{x}) \cdot \bar{\bar{Y}}_m(\bar{y})}{k \cdot \gamma_{nm} \cdot D_n \cdot E_m \cdot \bar{\bar{Z}}_{nm}(d_t)} \times \tag{3.42}$$

$$\times \left[\bar{X}_n(x_j) + \frac{A}{\beta_n} \bar{\bar{X}}_n(x_j) \right] \cdot \left[\bar{Y}_m(y_i) + \frac{A}{\alpha_m} \cdot \bar{\bar{Y}}_m(y_i) \right]$$

It must to be remarked that using Eq. (3.2) – or its modified version accounting for silicon dioxide lined trenches with polysilicon fill – to analytically describe the heat transfer coefficients as a function of technological parameters in Eq. (3.5) makes the proposed model *fully predictive,* namely, applicable to any trench-isolated bipolar transistor without the need of further numerical simulations and coefficient optimizations.

3.3.5 Remarks

Some considerations concerning the proposed modeling strategy are in order.

1. Let us refer to subdomain 1. Since only the steady-state case is described, we resorted to the Fourier series expansion, which

requires a lower number of terms to converge within a given accuracy compared to the Green's function method (adopted in e.g., [12] for trench-isolated transistors and suggested in [18], [21] for bulk-silicon devices with VHS and THS, respectively).

2. The proposed approach involves a proper choice of the interface discretization level as well as of the number of terms to be accounted for in Eq. (3.5). An in-depth convergence analysis was therefore performed. A 4×8 discretization was found to converge within 1% over the whole range of technological parameters by taking into account a high number of terms in Eqs. (3.9) and (3.24).[20] Fig. 3.13 shows the convergence analysis for the reference domain. As can be seen, finer discretizations exponentially increase the simulation times without sensibly improving the accuracy.
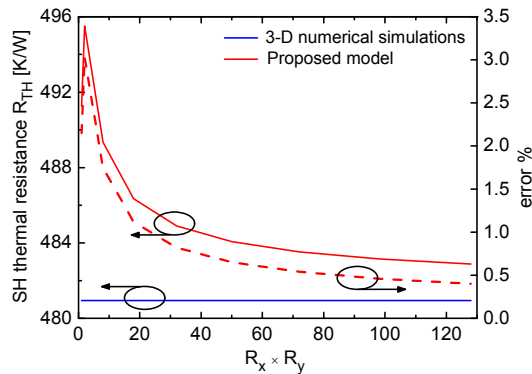
Fig. 3.13. Self-heating thermal resistance of the trench-isolated transistor as a function of discretization level chosen at the interface. The model (solid red line) is compared to the numerically calculated value (blue line). Dashed line corresponds to the percentage error.

---

[20] As concerns the reference structure, the error is relatively low even when accounting for a coarse interface discretization: a 1×2 partitioning implies an error amounting to about 3%. However, higher errors are obtained when considering reduced trench depths (i.e., with shortened vertical spacing between heat source and trench bottom) and/or a higher box-to-source size ratio. As an example, if a 1×2 discretization is adopted, the error increases to (i) 8% when simulating a structure with $d_t = 3$ μm and all other technological parameters equal to those of the reference transistor and (ii) 12% when a 1×3 μm^2 emitter stripe is considered concurrently with $d_t = 3$ μm.

Fig. 3.14 shows the 12×24 discretization effect on the heat flux distribution for the reference domain over the bottom of the silicon trench box. In Fig. 3.14a the heat flux distribution above one quarter of the bottom evaluated by the proposed model is compared with the actual one obtained through a 3-D FEM simulation, while Fig. 3.14b shows the same comparison along the y axis crossing the center of a column of elementary rectangles R_{ij}. The figure shows the good agreement between the model and numerical results.
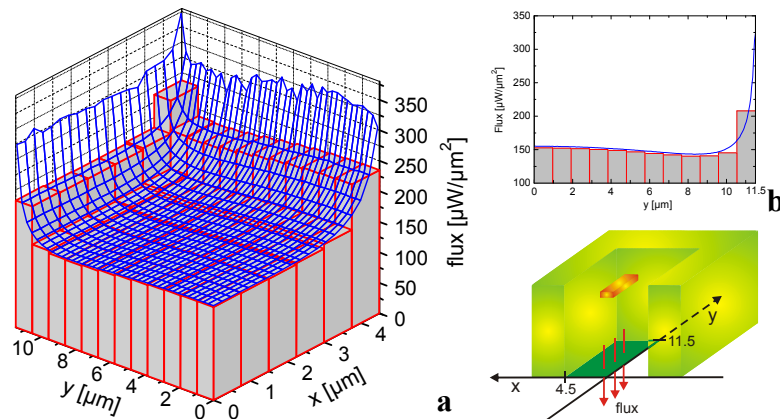
Fig. 3.14. Heat flux distribution for the reference domain over the bottom of the trench box (a) above one quarter of the surface (b) along $x = 0.375$ μm (cut line crossing the center of a column of individual rectangles R_{ij}). A 12×24 discretization was chosen. The model (grey) is compared to numerical results (blue) as obtained through a 3-D FEM simulation by assuming a dissipated power density of 10 mW/μm^3.

3. If a 4×8 discretization is chosen, the summations of Eqs. (3.9) and (3.24) were shown to converge within 0.2% when performed up to $(n, m) = (15, 9)$ for the reference domain (Fig. 3.15), while $(30, 20)$ can be safely considered when dealing with downscaled devices (i.e., with emitter stripes shrunk up to 0.5×1 μm^2).

4. In principle, Eqs. (3.17) and (3.18) should be solved numerically (as in e.g., [12]), but this step would require a considerable extra simulation time. In our strategy, this is avoided by resorting to approximate, yet accurate analytical

closed-form solutions obtained by properly modifying those available in [19].

Fig. 3.15. Convergence analysis for the reference domain: self-heating thermal resistance calculated by the proposed model as a function of the number of the terms accounted for in Eq. (3.5).
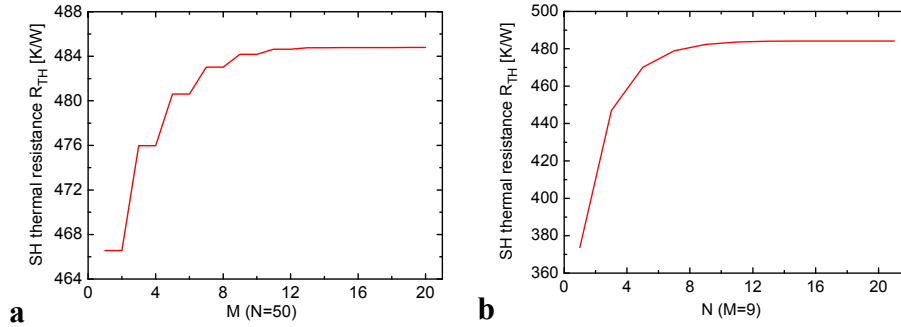
5. Let us consider subdomain 2. In this case, exploiting the double Fourier expansion technique would require a prohibitively high number of terms to ensure convergence within an acceptable accuracy due to the large chip-to-source size ratio. This, in turn, would drastically increase the CPU time needed for the simulation.[21] Conveniently, using the approach described in Paragraph 3.3.2 allows tackling this issue (see e.g., [6] for further considerations). It is worth noting that, as far as the reference device is concerned, the 3rd-order solution (corresponding with 11 fictitious heat sources to be accounted for concurrently with the "real" one [see Eq. (3.35)]) accurately satisfies the boundary conditions at top and bottom surface of this subdomain. Nevertheless, it was found that the self-heating thermal resistance R_{TH} can be also evaluated by adopting the 0th-order solution given by Eq. (3.33) for the temperature field in subdomain 2 without appreciable loss of accuracy.[22]

---

[21] An interesting evaluation of the increase in CPU time with the number of terms accounted for in the double Fourier series solution for a multilayered structure is performed in [22].

[22] Self-heating resistance values amounting to 485 and 487 K/W are calculated by considering the 3rd- and 0th-order solutions for subdomain 2, respectively.

6. The time elapsed to calculate a self-heating thermal resistance value amounts to a few seconds on a PC with a 2 GHz CPU, which proves the effectiveness of the proposed model. The details concerning the accuracy will be given in the next Paragraph.

7. It is worth noting that in the above treatment we have disregarded the cooling effect due to metallization, that is, the proposed modeling approach allows predicting only the so-called *intrinsic* thermal resistance of the devices. Nevertheless, it can be effortlessly generalized to account for the cooling effect due to metallization layers by following the strategy illustrated in [12], namely, by adding a parallel thermal resistance depending upon the metal geometry to describe the heat flow along the metal path.

8. Another effect neglected in this analysis is the dependence of the thermal conductivity on temperature. As well-known, this effect can be easily accounted for by means of the Kirchhoff transform in homogeneous domains [23]-[25] (see Appendix F). On the other hand, the Kirchhoff transform is in principle not applicable to inhomogeneous structures where the materials exhibit different functional forms for the thermal conductivity dependence on temperature [26], e.g., in the case of trench-isolated silicon transistors with oxide-filled trenches. In fact, the thermal conductivity of silicon reduces with temperature according to the power law $k(T) = k_0 (T/T_0)^{-m}$ where T_0 is a reference temperature, $k_0 = k(T_0)$, and the power factor m has been estimated to be in the range $1.25 \div 1.33$ (see e.g., [24], [25]), whilst that of silicon dioxide films slightly increases with temperature [27]. Nevertheless, we showed that the Kirchhoff transform can be successfully applied also to DTI devices by assuming for silicon dioxide the same thermal conductivity dependence law of silicon. In fact, the comparison between model results and "realistic" 3-D numerical simulations carried out by associating to silicon dioxide its actual functional form was found to be excellent up to a dissipated power of about 0.2 W for the reference structure (Fig. 3.16).
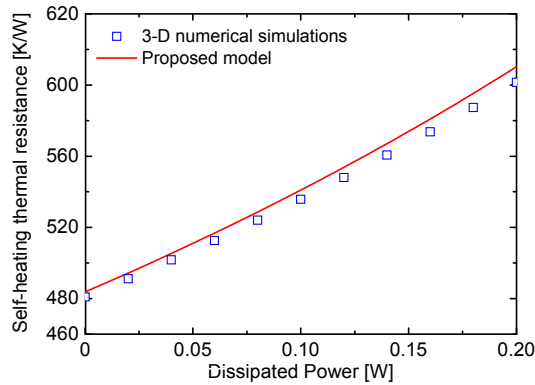
Fig. 3.16. Self-heating thermal resistance of the trench-isolated transistor as a function of dissipated power. The model (solid line) is compared to numerical results (symbol).

3.4   Simulation results

The purpose of this Paragraph is threefold:

1. it is intended to offer a complete overview of the thermal behavior of a single-emitter DTI device as a function of all technological parameters playing a role;
2. it provides evidence of the model accuracy by an extensive comparison to fully 3-D numerical simulations and all the predictive models available from the literature;
3. it demonstrates that the model can be effectively adopted to enhance the thermal design of single- and multi-finger trench-isolated bipolar transistors.

3.4.1 Analysis of the single-finger DTI transistor

This analysis was performed by varying a chosen parameter while keeping the others equal to the reference ones (Table 3.1).

First, the impact of the trench features (i.e., trench depth and thickness) on the thermal behavior of the DTI transistor was analyzed. Fig. 3.17 shows that the self-heating thermal resistance R_{TH} of the

device grows almost linearly with trench depth due to the lengthening of the path where the heat flow is trench-confined. The figure also illustrates that R_{TH} slightly increases with trench thickness for thin trenches (i.e., with $t_t < 1.0$ μm), while nearly saturating to a constant value for thicker trenches, that is, above a certain value the normalized temperature field nearby the heat source becomes insensitive to trench thickness.

Fig. 3.17. Self-heating thermal resistance of the trench-isolated transistor as a function of depth and thickness of the trench. The model (solid lines) is compared to numerical results (symbols).

Fig. 3.18 depicts the thermal resistance behavior as the dimensions of the trench box vary. As can be seen, R_{TH} decreases with both W and L due to the larger silicon volume where the heat can easily spread from the active transistor area. Enlarging the width of the trench box results in a faster thermal resistance lowering since the trench walls are increasingly far away from the long side of the emitter stripe.

All the above results hold as far as the case of oxide-filled trench is concerned. As can be seen, the proposed model provides an excellent agreement with numerical data: a maximum error amounting to about 1% was found by simultaneously varying all parameters in the ranges of interest.
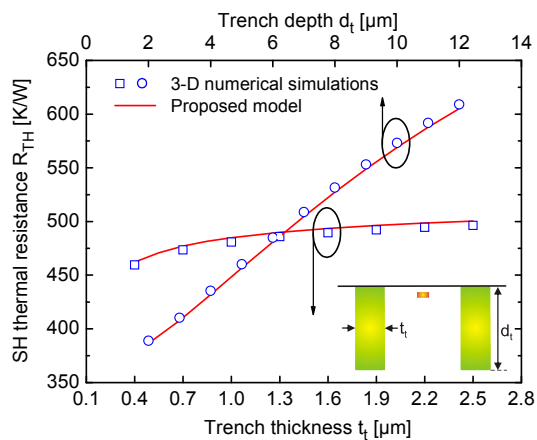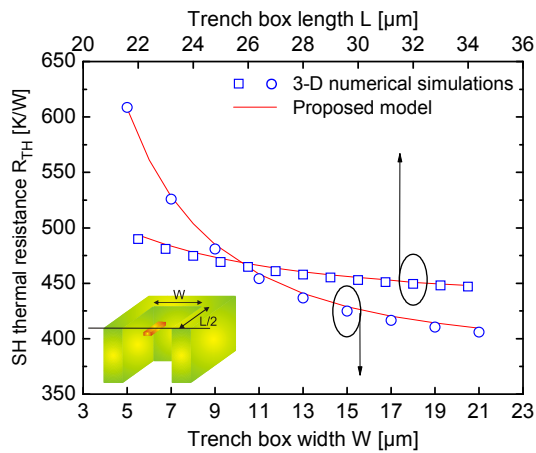
Fig. 3.18. Self-heating thermal resistance of the trench-isolated transistor as a function of width and length of the trench box. The model (solid lines) is compared to numerical results (symbols).

Fig. 3.19 shows the thermal resistance behavior as the trench depth changes for various trench materials, namely, pure silicon dioxide and oxide-polysilicon-oxide sandwich with two different polysilicon thermal conductivities.

Fig. 3.19. Self-heating thermal resistance of the trench-isolated transistor as a function of trench depth for the cases of oxide-filled trench and oxide-polysilicon-oxide trench for two values of thermal conductivity of polysilicon. The model (solid lines) is compared to numerical results (symbols).

As can be observed, R_{TH} increases for all the cases, with growth rates rising with lowering the average thermal conductivity of the trench-filling material. It should be noted that the thermal behavior of the structure is independent of the trench material when the trench depth is approaching 2 μm, since the heat flow becomes mostly radial in all cases; conversely, the trench material increasingly affects the thermal resistance as the trench depth grows, which is an expected result. Also when describing the more complex case of bipolar transistors with poly-filled trenches, the model exhibits a good degree of accuracy: a peak error of about 2% in comparison with numerical data was found by concurrently varying all technological parameters.

The model can be conveniently exploited to accurately quantify scaling-induced thermal effects in trench technology. Fig. 3.20a shows the self-heating thermal resistance behavior as the heat source length (i.e., the emitter stripe length) varies for various values of heat source width. The increase in thermal resistance as the device shrinks is plainly illustrated. As can be seen, R_{TH} spans from 450 K/W for a 2×20 μm^2 emitter area to 1920 K/W for a 0.5×1 μm^2 one, both embedded in a $9 \times 23 \times 6$ μm^3 silicon-only trench box.
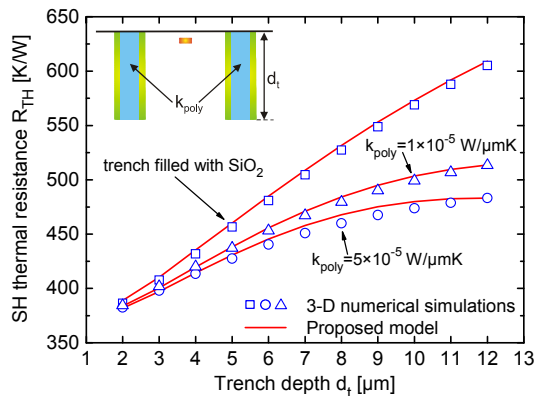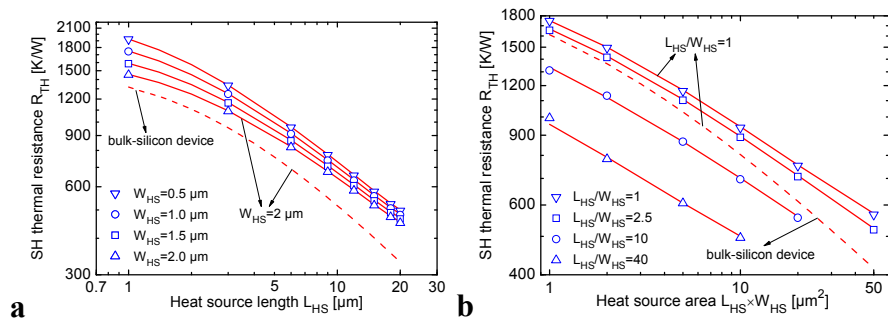

Fig. 3.20. Self-heating thermal resistance of the trench-isolated transistor as a function of: (a) heat source length for various values of heat source width and (b) heat source area for various aspect ratio values. The model (solid lines) is compared to numerical results (symbols). Dashed lines correspond to conventional bulk-silicon devices.

Fig. 3.20b depicts the thermal resistance behavior as a function of the heat source area for various values of the aspect ratio L_{HS}/W_{HS}. It can be observed that the thermal resistance diminishes by considering a high aspect ratio for the heat source, while reaching the maximum value for a square heat source by keeping the area constant.

Consequently, strongly asymmetrical emitter stripes (i.e., stripes characterized by a high perimeter/area ratio) are to be preferred from a thermal viewpoint. The figure also illustrates the thermal resistance curve corresponding to a square heat source embedded in a bulk-silicon substrate. An inspection of the figure reveals that the thermal resistance dependence on the heat source area in a trench-isolated device is reduced with respect to the bulk-silicon case since the heat flow process is also dependent on the trench features. It is worth noting that the analytical and numerical results can be considered virtually identical.

3.4.2 Comparison with other approaches

A few analytical approaches have been conceived and published in the literature to describe the thermal behavior of trench-isolated bipolar transistors.

1. Walkey *et al.* [7] assume ideal thermally-insulating trenches (i.e., with zero outgoing heat flux) and a 1-D heat flow at the bottom of the trench box. Based on these approximations, the structure is divided into two subdomains, namely, the silicon-only region enclosed by the trench (i.e., the above defined *trench box*) with top/lateral faces adiabatic and bottom surface isothermal, and the silicon substrate, which is modeled as a semi-infinite medium with a plate source located at the top surface to account for the inward flux coming from the trench box. The individual thermal resistances of both subdomains are evaluated via the well-known Joy and Schlig expression [5] coupled with the image method (see e.g., [6], [20], [22]) to satisfy the adiabatic conditions associated with the thermally insulating trench sidewalls (i.e., the silicon/trench interfaces). The thermal resistance of the overall structure is then computed as the series of the aforementioned individual resistances.
2. Rieh *et al.* [8] evaluate the self-heating thermal resistance of the trench-isolated transistor as the summation of partial thermal resistances associated with elementary portions of the heat path. The strategy is based on a twofold simplifying

hypothesis: first, the heat flux emerging from the active area is assumed to be confined within a 45°-angled cone; second, similarly to the approach proposed in [7], the trench is considered as a perfect thermal insulator that entirely guides the heat flow. It will be shown that simultaneously making these assumptions leads to a considerable overestimate of the thermal resistance.

3. Pacelli *et al.* [9] provide a closed-form expression for the thermal resistance that – differently from [7], [8] – accounts for a finite heat flow through the trench. In particular, the authors evaluate the thermal resistance as the combination of individual resistances, which describe (i) the radial heat flow coming from the active area and the one spreading into the silicon substrate from the bottom of the trench box, (ii) the vertical 1-D heat flow along the trench box, and (iii) the lateral heat loss through the trench sidewalls.

4. Vanhoucke and Hurkx [10] propose an approach similar to that presented in [9]. In particular, they (i) assume that the heat flow originating from the bottom of the trench box to radially spread into the substrate is determined by the geometrical features of the trench rather than by the emitter area, and (ii) use conformal mapping techniques to derive the analytical expressions for the thermal resistances corresponding with (ii-a) the heat vertically flowing along the trench well and (ii-b) that leaving the power dissipation region; for the latter, similarly to [8], they assume a 45° spreading angle.

In this Paragraph, the proposed model was compared with all the predictive models above presented [7]-[10]. For this purpose, the self-heating thermal resistance was evaluated by means of all models and 3-D numerical simulations by varying trench depth and heat source length. Results are depicted in Fig. 3.21a and b, respectively, while Table 3.3 addresses the values – and the corresponding percentage errors – obtained for the reference domain.
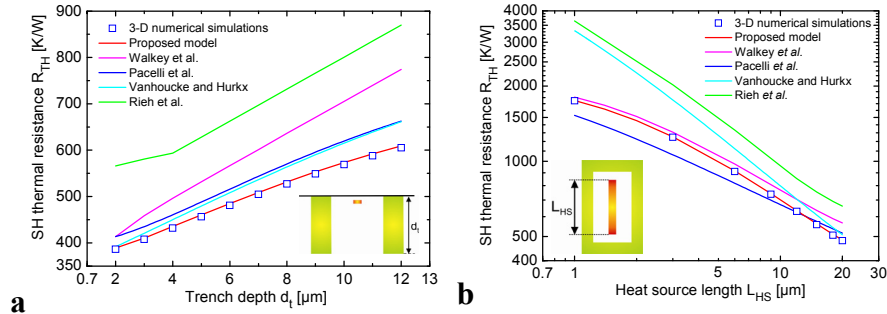
Fig. 3.21. Comparison between the proposed model and all predictive models available from the literature by varying (a) trench depth and (b) heat source length. Numerical results are also reported (symbols).

Table 3.3
Self-heating thermal resistance of the reference domain.

	R_{TH} [K/W]	error %
3-D FEM simulation	481	-
Proposed model	485	0.8
Walkey *et al*.	567	17.9
Pacelli *et al*.	516	7.3
Vanhoucke and Hurkx	508	5.6
Rieh *et al*.	663	37.8

As can be plainly observed, the proposed model guarantees a higher degree of accuracy with respect to all other approaches. The model of Rieh *et al.* [8] gives rise to a significant overestimate (i.e., up to more than 100%) of the thermal resistance, mainly due to the twofold approximation of a 45° spreading angle around the heat source and of adiabatic trench sidewalls. Similarly to [8], the approach from Walkey *et al.* [7] ignores the amount of heat flowing out of the silicon box through the trench, thereby becoming rather inaccurate when the impact of the trench on the temperature distribution is stronger, e.g., for large trench depths and long heat sources (errors up to 28% are observed with respect to numerical data). Contrarily to the above approaches, the models developed by Pacelli *et al.* [9] and Vanhoucke and Hurkx [10] account for the finite heat loss through the trench. However, the latter strongly deviates from numerical values as the heat source length reduces (i.e., for downscaled devices), which can be explained as follows. When the heat source shrinks, the

thermal resistance contribution due to the heat leaving the source (referred to as $R_{TH,radial}$ in [10]) dominates; unfortunately, this term suffers from the severe assumption of a 45° spreading angle for the heat flow, which was numerically proved to be less realistic than the uniformly-diffusing heat model. Conversely, the model by Pacelli *et al.* [9] provides an acceptable degree of accuracy over the range of parameters considered (a maximum error of about 15% is obtained), and can be in principle adopted when a fast, yet approximate evaluation of the thermal resistance value of a trench-isolated single-finger transistor is required.

3.4.3 Thermal design optimization

Similarly to the approaches developed in [7], [12], the proposed model allows also evaluating the temperature distribution within both the silicon trench box and substrate, a capability absent in other formulations [8], [9]. As an evidence, Fig. 3.22 shows the temperature rise over ambient normalized to dissipated power in the reference domain, as evaluated by the model and 3-D numerical simulations. In particular, Fig. 3.22a illustrates the contour curves over the cross-section of subdomain 1, while Fig. 3.22b depicts the normalized temperature rise field along the *x* axis. The graphs clearly show that the model agrees well with numerical data in the overall silicon domain.
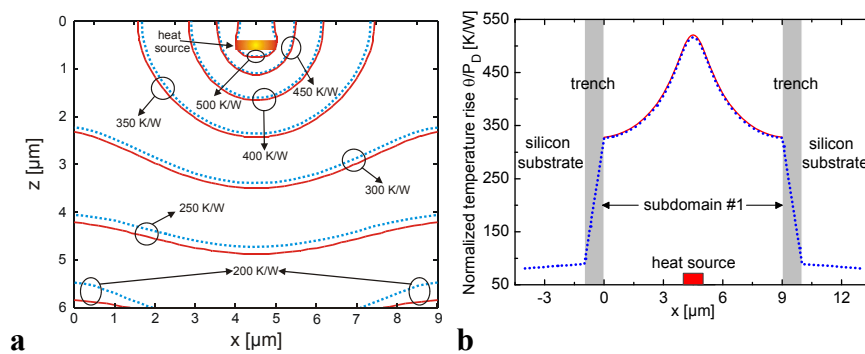

Fig. 3.22. Temperature rise normalized to dissipated power in the reference domain. The model (solid red lines) is compared with 3-D numerical data (dotted blue): (a) contour plots over the cross-section of the silicon box and (b) temperature rise field vs. *x* axis (cut taken through the heat source center).

As a main benefit of this feature, the mutual thermal coupling between elementary heat sources (i.e., emitter stripes) integrated within the same trench can be estimated, thereby allowing the analysis of design solutions to counteract thermal effects without affecting the current handling capability of the device, such as the emitter finger segmentation and the layout optimization of multi-finger transistors.

The positive effect of emitter segmentation from a thermal standpoint has been already shown experimentally for a trench-isolated SiGe HBT with a single-emitter finger [28] and numerically for a multi-finger device [29]. The proposed model was exploited to analyze the effect of this technique on a 1×12 μm^2 emitter stripe lying within a $9\times21\times6$ μm^2 silicon box surrounded by a 1-μm-thick oxide-filled trench. As can be seen in Fig. 3.23a, the emitter segmentation was applied so as to obtain two segmented-emitter (SE) configurations characterized by two 1×6 μm^2 (structure SE2) and four 1×3 μm^2 (structure SE4) emitter pieces, respectively, by keeping unchanged the total emitter length and the trench geometry, as well as the spacing between the emitter segments. Fig. 3.23b illustrates the temperature rise normalized to dissipated power along the y axis as obtained by the model and 3-D numerical simulations for all the layouts shown in Fig. 3.23a. The normalized temperature peak reduces from 710 K/W for the single-emitter finger to about 650 and 590 K/W for structures SE2 and SE4, respectively.

a   **b**
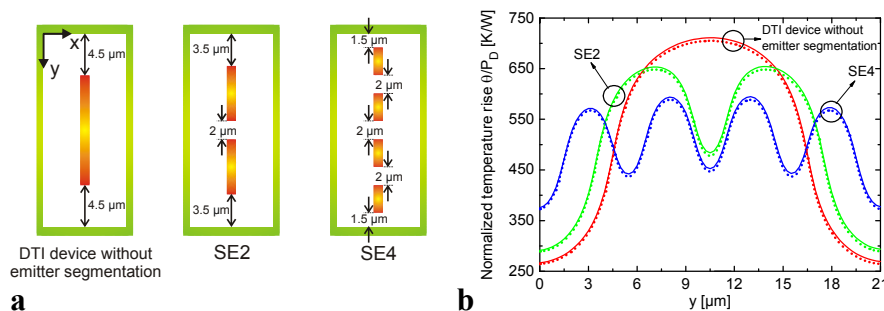
Fig. 3.23. (a) Layouts of trench-isolated transistors without and with segmented emitter (SE) finger. For the SE case, devices with two (SE2) and four (SE4) segments are represented; (b) temperature rise normalized to dissipated power vs. y axis as evaluated by model (solid lines) and 3-D numerical simulations (dotted) for the considered structures (cuts taken through the centers of the heat sources). Note that the total emitter length (and area) as well as the silicon area enclosed by the trench are fixed for all cases analyzed.

Multi-finger transistors, in which various emitter fingers located in close proximity are connected in parallel, are commonly used to allow a large power handling capability in small areas. Some works have been presented, which analyze the thermal behavior of bipolar transistors with multiple emitter fingers (e.g., [30], [31]). All these papers show that the maximum temperature increase takes place over the fingers lying at the center of the array, which suffer from the power dissipation of the neighboring emitter stripes more than the outer ones (i.e., those located in the periphery of the array). A particularly improper layout design may exacerbate this effect, thus favoring electrothermal instability phenomena such as the *collapse of current gain* occurring in multi-finger GaAs-based HBTs [32]. A possible strategy to potentially weaken thermal issues in these structures involves the adoption of configurations with nonuniform – and optimized – spacing between emitter fingers or finger length (see e.g., [33]). In this scenario, the proposed model was adopted to analyze the layout influence on the thermal behavior of a multi-finger bipolar transistor with five $0.5{\times}20$ μm^2 emitter stripes that lie within a $34.5{\times}23{\times}6$ μm^3 silicon box surrounded by a 1-µm-thick oxide-filled trench (Fig. 3.24).
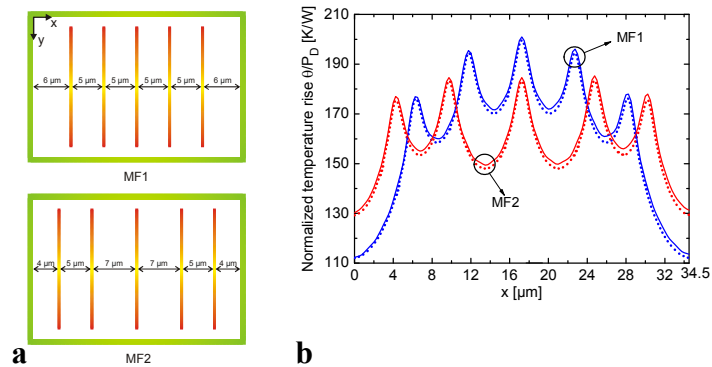
Fig. 3.24. (a) Five-finger trench-isolated transistors with different layouts and (b) temperature rise normalized to dissipated power vs. *x* axis as evaluated by model (solid lines) and 3-D numerical simulations (dotted) for the considered structures (cuts taken through the centers of the heat sources). Both the total emitter width (and area) and the silicon area enclosed by the trench are fixed.

Two DTI structures are considered, whose top-views with the corresponding geometrical parameters are evidenced in Fig. 3.24a. Fig. 3.24b shows the temperature rise normalized to dissipated power

along the *x* axis as obtained by the model and 3-D numerical simulations for both devices. As can be observed, a more uniform (and lower) temperature rise distribution occurs over the structure denoted with MF2, where the lateral emitter fingers are located further away from the central one with respect to the uniformly-spaced transistor MF1.

It is worth noting that the proposed model compares favorably with numerical data for all the design solutions analyzed.

References

[1] Harame DL, Comfort JH, Cressler JD, Crabbè EF, Sun JYC, Meyerson BS, Tice T. Si/SiGe epitaxial-base transistors – Part II: Process integration and analog applications. IEEE Trans Electron Dev 1995;42(3):469-82.

[2] Forsberg M, Björmander C, Johansson T, Ko T, Liu W, Vellaikal M, Cheshire A. Shallow and deep trench isolation for use in RF-Bipolar ICs. IEEE ESSDERC Proc 2000:212-5.

[3] Ohue E, Oda K, Hayami R, Washio K. A 7.7-ps CML using selective-epitaxial SiGe HBTs. IEEE BCTM Proc 1998:97-100.

[4] Reid AR, Kleckner TC, Jackson MK, Marchesan D, Kovacic SJ, Long JR. Thermal resistance in trench-isolated Si/SiGe heterojunction bipolar transistors. IEEE Trans Electron Dev 2001;48(7):1477-9.

[5] Joy RC, Schlig ES. Thermal properties of very fast transistors. IEEE Trans Electron Dev 1970;ED-17(8):586-94.

[6] Rinaldi N. Thermal analysis of solid-state devices and circuits: an analytical approach. Solid-State Electron 2000;44(10):1789-98.

[7] Walkey DJ, Smy TJ, Marchesan D, Tran H, Schröter M. A scalable thermal model for trench isolated bipolar devices. Solid-State Electron 2000;44(8):1373-9.

[8] Rieh JS, Johnson J, Furkay S, Greenberg D, Freeman G, Subanna S. Structural dependence of the thermal resistance of

trench-isolated bipolar transistors. IEEE BCTM Proc 2002:100-3.

[9]   Pacelli A, Palestri P, Mastrapasqua M. Compact modeling of thermal resistance in bipolar transistors on bulk and SOI substrates. IEEE Trans Electron Dev 2002;49(6):1027-33.

[10]   Vanhoucke T, Hurkx GAM. A new analytical model for the thermal resistance of deep-trench bipolar transistors. IEEE Trans Electron Dev 2006;53(6):1379-88.

[11]   Comsol Multiphysics 3.3. User's Guide. Comsol AB, 2007.

[12]   Walkey DJ, Smy TJ, Reimer C, Schröter M, Tran H, Marchesan D. Modeling thermal resistance in trench-isolated bipolar technologies including trench heat flow. Solid-State Electron 2002;46(1):7-17.

[13]   Marano I, d'Alessandro V, Rinaldi N. Analytical modeling and numerical simulations of the thermal behavior of trench-isolated bipolar transistors on SOI substrates. Solid-State Electron 2008;52(5):730-9.

[14]   De Paola FM, d'Alessandro V, Tamigi F, Rinaldi N. Analytical thermal modeling of flip-chip mounted semiconductor optical amplifiers. EMPS Proc 2004:207-12.

[15]   McConnell AD, Uma S, Goodson KE. Thermal conductivity of doped polysilicon layers. Journal of Microelectromech Syst 2001;10(3):360-9.

[16]   Tai YC, Mastrangelo CH, Muller RS. Thermal conductivity of heavily doped LPCVD polysilicon. IEEE IEDM Proc 1987;33:278-81.

[17]   Xu GB, Huang QA. An online test microstructure for thermal conductivity of surface-micromachined polysilicon thin films.IEEE Sensors J 2006;6(2):428-33.

[18]   d'Alessandro V, Rinaldi N. A critical review of thermal models for electro-thermal simulation. Solid-State Electron 2002;46(4):487-96.

[19]   Beck JV, Cole KD, Haji-Sheikh A, Litkouhi B. Heat conduction using Green's functions. London: Hemisphere Publishing Corporation; 1992.

[20]   Leturcq P, Dorkel JM, Napieralski A, Lachiver E. A new approach to thermal analysis of power devices. IEEE Trans Electron Dev 1987;ED-34(5):1147-1156.

[21] Haji-Sheikh A. Peak temperature in high-power chips. IEEE Trans Electron Dev 1990;37(4):902-7.

[22] Lee CC, Palisoc AL. Real-time design of integrated circuit devices. IEEE Trans Components, Hybrids, and Manufacturing Technology 1988;11(4):485-92.

[23] Joyce WB. Thermal resistance of heat sinks with temperature dependent conductivity. Solid-State Electron 1975;18(4):321-2.

[24] Negus KJ, Franklin RW, Yovanovich MM. Thermal modeling and experimental techniques for microwave bipolar devices. IEEE Trans Components, Hybrids, Manuf Technol 1989;12(4):680-9.

[25] Lee SS, Allstot DJ. Electrothermal simulation of integrated circuits. IEEE J. Solid-State Circuits 1993;28(12):1283-93.

[26] Bonani F, Ghione G. On the application of the Kirchhoff transformation to the steady-state thermal analysis of semiconductor devices with temperature-dependent and piecewise inhomogeneous thermal conductivity. Solid-State Electron 1995;38(7):1409-12.

[27] Kleiner MB, Kühn SA, Weber W. Thermal conductivity measurements of thin silicon dioxide films in integrated circuits. IEEE Trans Electron Dev 1996;43(9):1602-9.

[28] Rieh JS, Greenberg D, Liu Q, Joseph AJ, Freeman G, Ahlgren DC. Structure optimization of trench-isolated SiGe HBTs for simultaneous improvements in thermal and electrical performances. IEEE Trans Electron Dev 2005;52(12):2744-52.

[29] Wang Y, Zhang WR, Xie HY, Zhang W, He LJ, Sha YP, Thermal analysis of power SiGe heterojunction bipolar transistor with novel segmented multi-emitter structure. IEEE ICMMT Proc 2007:1-4.

[30] Liu W, Bayraktaroglu B. Theoretical calculations of temperature and current profiles in multi-finger heterojunction bipolar transistors. Solid-State Electron 1993;36(2):125-32.

[31] Walkey DJ, Celo D, Smy TJ, Surridge KS. A thermal design methodology for multifinger bipolar transistor structures. IEEE Trans Electron Dev 2002;49(8):1375-83.

[32] Liu W, Nelson S, Hill DG, Khatibzadeh A. Current gain collapse in microwave multifinger heterojunction bipolar

transistors operated at very high power densities. IEEE Trans Electron Dev 1993;40(11):1917-27.

[33] Lee JG, Oh TK, Kim B, Kang BK. Emitter structure of power heterojunction bipolar transistor for enhancement of thermal stability. Solid-State Electron 2001;45(1):27-33.

Chapter 4

SiGe heterojunction bipolar transistors

This Chapter is focused on the thermal behavior of state-of-the-art SiGe heterojunction bipolar transistors (HBTs) for high frequency applications.

First, a brief introduction to SiGe HBT technology is presented.

Then, an accurate numerical analysis of the SiGe HBT thermal behavior is performed to analyze the influence of each element (i.e., shallow trench, metal slot contacts, deep trench) forming a part of the overall structure. Subsequently, a sensitivity analysis is presented that allows evaluating the influence on the thermal resistance of all technological parameters of interest (i.e., emitter length, deep and shallow trench depths, heat source thickness, distance between the active region and trench, trench geometry). The scaling effects on thermal resistance are also analyzed as well as the nonlinear effects due to the dependence of the thermal conductivity of some materials (e.g., silicon and tungsten) on temperature.

Finally, a comparison with 3-D numerical simulations has allowed proving that the model developed for trench-isolated bipolar transistors (see Chapter 3) can be conveniently extended to predict the thermal behavior of "complete" (i.e., not only confined to the *intrinsic* semiconductor domain) SiGe HBT structures.

4.1. SiGe bipolar technology: a historical perspective

The operating speed of a transistor strongly depends on the velocity of the carriers to be transported through the device in assigned operating voltages. Unfortunately, the carriers' mobility in Si

is rather limited as well as the maximum velocity that they can reach forced by high electric fields.

The III–V compound semiconductors (e.g., GaAs and InP) might solve these problems. In fact, they exhibit higher mobilities and saturation velocities. Furthermore, due to their direct gap nature, they are much more versatile. Unfortunately, their employment is very complex: for instance, it is not possible to attain a robust thermally grown oxide for GaAs or InP, wafers are smaller with much higher defect densities, break more easily, and are worse heat conductors. These drawbacks lead to lower levels of integration as well as more difficult and expensive fabrication processes [1].

Therefore, it would be attractive to improve Si transistors performance so as to be competitive with III–V devices for high-performance applications, while keeping their low costs and manufacturing advantages. This is possible thanks to the progress in epitaxial deposition techniques, that allows realizing thin base layers of SiGe[23] on silicon substrate without significantly affecting the lattice constant.

Fig. 4.1 shows a SEM SiGe HBT cross section.
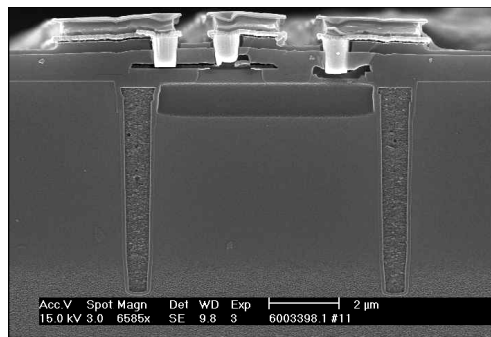
Fig. 4.1. SEM view of a SiGe HBT.

SiGe bipolar transistors are able to reach larger current gains and cutoff frequencies, due to the wider bandgap of Ge that limits the minority-carrier injection into the emitter region. In fact, Ge content in SiGe layers changes with position so as to realize a graded base, i.e., a base region in which the bandgap diminishes from the emitter to

---

[23] Let us recall that germanium (Ge) was the earliest semiconductor used by the Bell Laboratories.

collector [2]. This generates an electric field that reduces the base transit time while increasing cutoff frequency [3], [4].

The first study of SiGe alloys was performed in 1958 [5]. However, only around 1960 the epitaxy allowed fabricating more robust and controllable transistors [6]. In order to obtain a chemically pure and pristine interface Si/Si-epi, early Si epitaxy was conducted under high-temperature processing conditions, in the range of 1100°C. High-temperature Si-epi has been widely used for over 40 years. Nowadays, epitaxial depositions of thin Si layers on large Si substrates, for both p- and n-type doping, and with very high precision and doping control, are required. These goals are pursued only through low-temperature Si-epi (around 500-600°C) that also improves the compatibility between elements of different bandgaps [1].

Subsequently, in 1975, the first SiGe strained layer was grown in Germany [7]. [24]

In 1996 an unexpected discovery was made: incorporating small amounts of carbon into a SiGe epi layer strongly limits the diffusion of the boron base layer during subsequent thermal cycles [8]. This discovery was very important since an accurate control of the thin base profile during fabrication is a fundamental aspect in SiGe technology process.

The first high-power SiGe HBTs were presented in 1996 using thick collector doping profiles [9], [10]. The boundary of 200 GHz in f_T peak was overcome in November 2001 for a nonself-aligned device [11], and in February 2002 for a self-aligned one [12]. A SiGe HBT technology with a peak f_T of 350 GHz was presented in December 2002 that is a record for room temperature operation [13] (while at cryogenic temperatures f_T can go above 500 GHz). Finally, in June 2004, an optimized SiGe HBT with both f_T and f_{max} above 300 GHz was presented, that is still a record [14].

Further details can be found in [1].

---

[24] Since Si and Ge exhibit different lattice constants, a strain is inevitably induced in the composite film so that the notion of *critical thickness* of a film beyond which strain relaxation occurs was introduced.

4.1.1. The state-of-the-art Infineon SiGe technology

A significant progress in the high-speed performance of SiGe HBTs has been allowed due to the accurate control of impurity profile in the SiGe base – improving transit time and base resistance – and the development of self-aligned transistor architectures – reducing parasitic capacitances and extrinsic series resistances [1].

Infineon's high-frequency SiGe bipolar technology is based on a double-polysilicon self-aligned (DPSA) transistor configuration, in which the shallow and highly boron-doped SiGe base layer is integrated by means of selective epitaxial growth (SEG) [15]-[18]. Let us note that SEG is not the only suitable technique for the integration of the SiGe base; other technologies use, in fact, nonselective epitaxial growth (NSEG).

When, in 1999, Infineon presented its first DPSA HBT, it exhibited transit and maximum oscillation frequencies of about 75 GHz [19]. Then, thanks to the adoption of SEG technique for the SiGe base fabrication, Infineon's HBT performance improved considerably, achieving transit and maximum oscillation frequencies of 200 GHz or above [20]-[23]. SEG, in fact, allows improving shallow base formation technology, which leads to reduced base thickness even for high base boron doping levels, and minimizing transistors size, which results in a decrease of base resistance and emitter–base/base–collector capacitances.

As concerns Infineon's actual high-frequency SiGe bipolar technology, it provides a transit frequency of 200 GHz, a maximum oscillation frequency of 275 GHz, and a ring oscillator gate delay time of 3.5 ps [23].

Fig. 4.2 shows a transmission electron microscopy (TEM) cross section of a NPN transistor in SiGe technology.

As can be seen, the transistor size can be kept small due to the completely planar surface topography of transistor isolation that allows decreasing feature sizes and lithographic alignment tolerances.

Both deep and shallow trench are employed, in order to increase transistor packing densities in circuits and reduce subcollector dimensions and consequently the collector–substrate capacitances.

Fig. 4.2. TEM view of a SiGe HBT.

As previously detailed, the transistor has a DPSA emitter–base configuration, with highly boron-doped and silicided polysilicon layers for contacting the SiGe base of the active transistor. A thin oxide spacer separates, by means of a self- alignment process, the base P^+-polysilicon from the emitter heavily-doped arsenic. The self-alignment of the emitter–base structure allows reaching values of base resistance and base–collector capacitance lower than in a transistor where the separation of the emitter from the extrinsic base regions is made by a proper photolithographic step [1]. Moreover, the SiGe base layer is integrated by SEG, which also allows fabricating a self-aligned base–collector structure [15]-[18], [24], [25].

Other features of this technology are:

1. the presence of carbon in SiGe base to obtain very thin and highly boron-doped base layers with vertical doping profile gradients [26], [27];
2. the realization of heavily arsenic-doped monocrystalline emitter contacts, that reduce the emitter resistance as compared to conventional polysilicon emitters [23], [28], [29];
3. the use of copper metallizations that improve electromigration hardness and lifetime at high operating current densities with respect to conventional aluminum metallizations [1].

4.2. Numerical analysis

The SiGe HBT under analysis, that will be denoted as *reference structure*, is depicted in Fig. 4.3 and Fig. 4.4. In particular, Fig. 4.3

shows the cross-section along x axis as well as the details of the active region. The top-views corresponding to prescribed depths are depicted in Fig. 4.4.

In the reference structure the heat source is represented as a rectangular parallelepiped with length and width assumed equal to those of the emitter window (i.e., $0.2 \times 2.67 \ \mu m^2$) and thickness vertically coinciding with that of the base-collector depletion region of the transistor, where the power dissipation takes place (see e.g., [30], [31]). As illustrated in Fig. 4.5, we assume a 0.06 µm-thick depletion region within the self-aligned ion-implanted collector (SIC), i.e., the SIC is assumed to be partially-depleted. In conclusion, a $0.2 \times 2.67 \times 0.06 \ \mu m^3$ heat source is considered. The dependence of the thermal behavior of the structure upon the heat source thickness[25] will be discussed in the following.
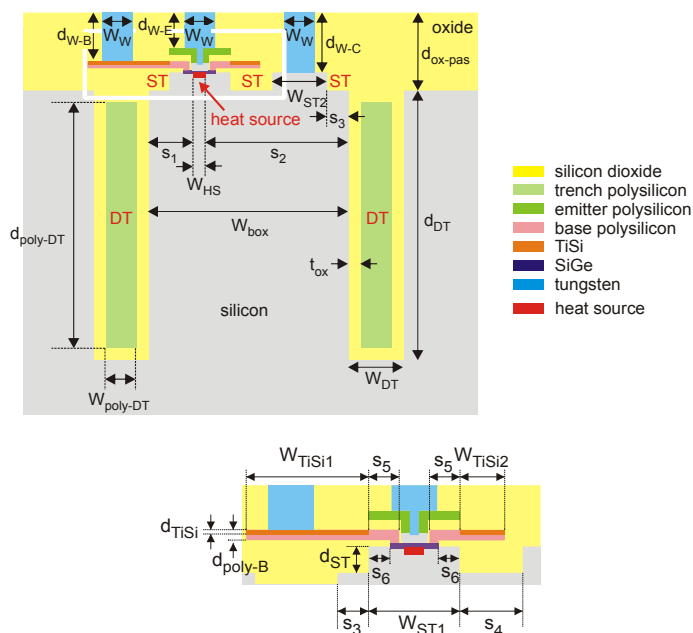

Fig. 4.3. Structure under analysis.

---

[25] The geometrical variation of the depletion region with biasing conditions leads to a heat source thickness modulation, which, in turn, affects the thermal behavior of the transistor [31].
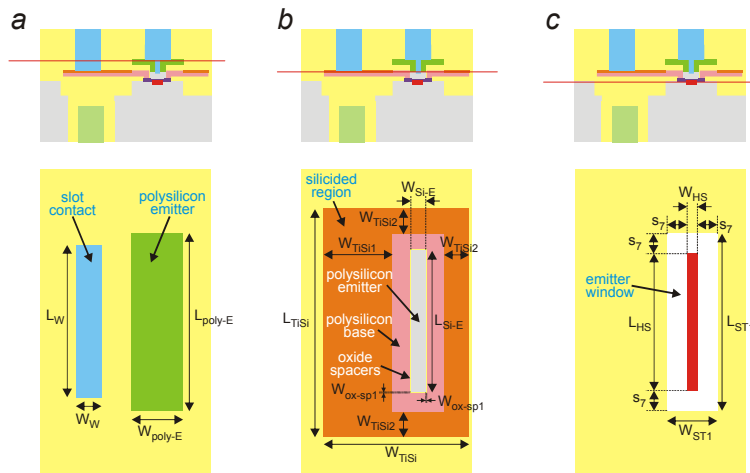
Fig. 4.4. Top-views.
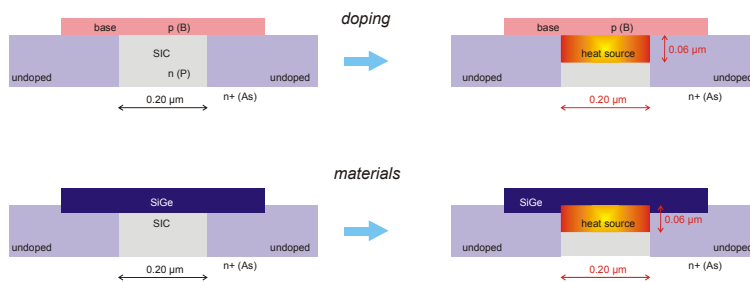
Fig. 4.5. 2-D heat source representation.

The silicon box where the transistor lies is laterally enclosed by a poly-filled deep trench (DT). In addition, the active region is surrounded by a shallow trench (ST).

All geometrical parameters corresponding to the reference domain will be designated with the subscript "ref" in the following.

Top-view *a* is taken along the top of the polysilicon emitter; the resulting figure also evidences the tungsten slot contacting the polysilicon base. Top-view *b* is cut along the top of the polysilicon base, and shows the whole P$^+$ polysilicon ring with silicided regions at the top. Lastly, top-view *c* gives an insight into the heat source and the surrounding ST.

4.2.1. The reference domain

Fully 3-D thermal-only simulations were performed through the commercial software Comsol [32] in order to evaluate the self-heating thermal resistance R_{TH} of the device. The analysis was carried out as follows. First, a simplified structure comprising only the DT and the heat source embedded in a silicon substrate with adiabatic top surface and isothermal bottom[26] was considered. Then, increasingly complex domains were obtained by adding elementary portions (so as to "gradually" build the actual structure, namely, the *reference* one represented in Fig. 4.1) and simulated. Such an analysis was performed in order to understand the individual contribution of each element of the actual structure to the overall thermal resistance.

The values of the thermal conductivities adopted for the numerical simulations are reported in Table 4.1.

Table 4.1
Thermal conductivities at $T = 300$ K.

material	thermal conductivity @ $T = 300$ K [W/μmK]
bulk silicon	1.48×10^{-4}
silicon dioxide	1.40×10^{-6}
tungsten	1.77×10^{-4}
titanium silicide	2.15×10^{-4}
emitter polysilicon (heavily doped with arsenic)	4.0×10^{-5}
trench polysilicon (undoped)	2.0×10^{-5}
base polysilicon (doped with boron)	3.0×10^{-5}
germanium	6.0×10^{-5}

The heat generated by the source is assumed to be due to a uniform power dissipation. The self-heating thermal resistance R_{TH} was evaluated by averaging the temperature rise above ambient over

---

[26] The bottom surface of the domain under analysis is assumed to be in intimate contact with an ideal heat sink at temperature $T_{AMB} = 300$ K. Such an assumption will be adopted for all the structures investigated.

the base-emitter junction and dividing the result by the dissipated power.[27]

Basic (simplified) structure: rectangular vs. round bottom of the deep trench

Let us consider the simplified structure with top surface adiabatic, bottom surface isothermal, and heat source located in a silicon box laterally enclosed by DT. As a first step, we carried out a numerical analysis to understand the influence of the shape of the trench bottom (that is round-shaped in the actual structure) by simulating two HBT domains, namely, one with a "rectangular" trench, denoted as Structure 1 (the 2-D representation is reported in Fig. 4.6), and another with a round trench bottom, designated as Structure 2 (Fig. 4.8). As concerns Structure 1, a self-heating thermal resistance R_{TH1}[28] amounting to 4148 K/W was numerically evaluated. The corresponding temperature rise normalized to dissipated power along the vertical z axis crossing the heat source center (dashed line in Fig. 4.6) is shown in Fig. 4.7.

Conversely, when considering the actual round shape of the DT bottom (Fig. 4.8), $R_{TH2} = 4118$ K/W was numerically determined.

Fig. 4.6. Structure 1: cross-section.
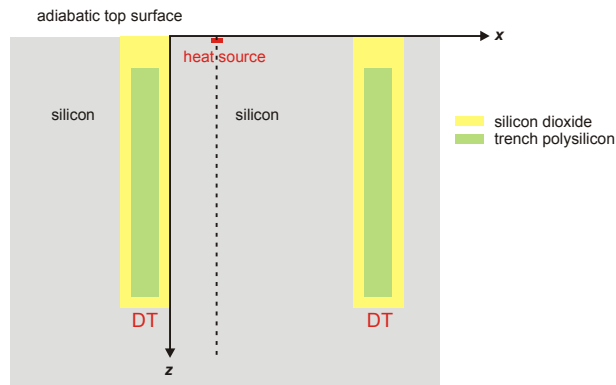
---

[27] As concerns the simplified structures where emitter is not present (i.e., Structures 1 and 2), the thermal resistance is calculated by averaging the temperature rise above ambient over the projection of the heat source on the top surface.

[28] In the following treatment, R_{THi} will designate the self-heating thermal resistance associated with the i-th HBT structure.
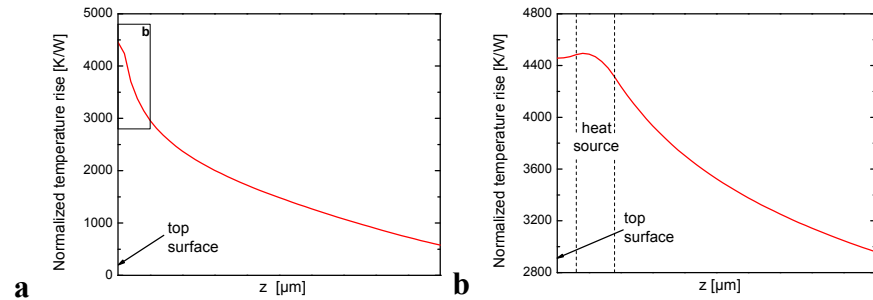
Fig. 4.7. Structure 1: (a) temperature rise normalized to the overall dissipated power vs. *z* axis and (b) detail of the heat source region.
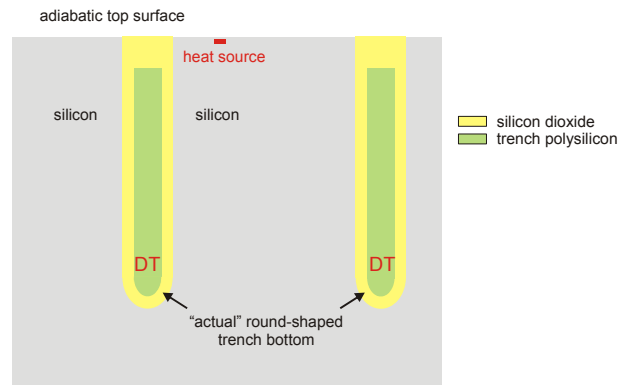
Fig. 4.8. Structure 2 (accounting for the round-shaped DT bottom): cross-section.

Emitter structure

As an additional step, the domain is "enriched" (with respect to Structure 1) by replacing the adiabatic condition at the top surface with an oxide layer containing the actual T-shaped emitter structure, which is composed by heavily arsenic-doped polysilicon and mono-crystalline silicon (the latter in the active transistor region), as shown in Fig. 4.9 and Fig. 4.10. The resulting domain is denoted as Structure 3. The self-heating thermal resistance was calculated to be $R_{TH3} = 3968$ K/W. Thus, a reduction of 4.34% in the thermal resistance is found with respect to Structure 1 due to the finite heat propagation through the polysilicon and – in a lower amount – through the oxide layer. The normalized temperature rise above

ambient along the dashed line crossing the heat source center (depicted in Fig. 4.9) is shown in Fig. 4.11.

Fig. 4.9. Structure 3 (accounting for the T-shaped poly-Si/mono-Si emitter structure): cross-section.
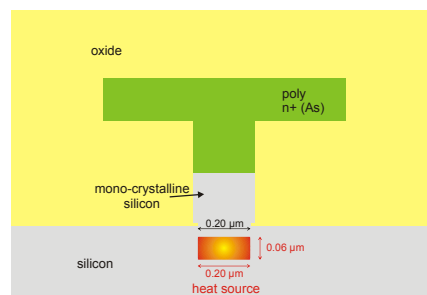
Fig. 4.10. Structure 3: detail of the emitter/heat source region.

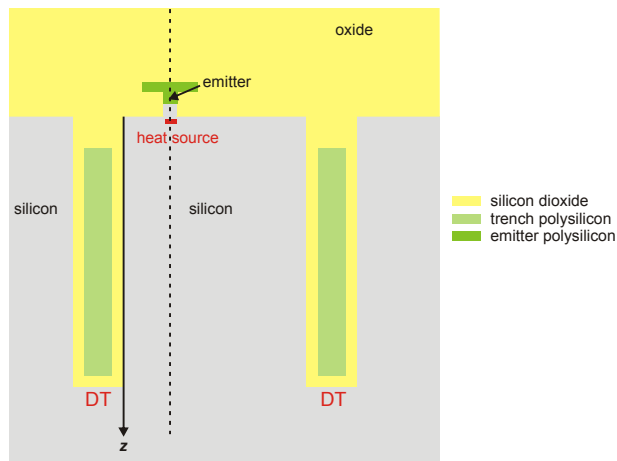**Fig. 4.11.** Structure 3: (a) normalized temperature rise vs. z axis and (b) magnification illustrating the emitter/heat source region. Also shown is the comparison with the oversimplified Structure 1 (blue curve).

Shallow trench (ST)

Subsequently, the shallow oxide trench is accounted for, as depicted in Fig. 4.12 (the domain is referred to as Structure 4).

In this case, a thermal resistance R_{TH4} = 4265 K/W was evaluated. As a consequence, an increase amounting to 7.48% with respect to the ST-free Structure 3 is obtained, since ST represents an obstacle for the heat to flow away from the heat source. Besides, an increase of 2.82% arises with respect to the oversimplified Structure 1. This demonstrates that the ST "barrier" to the radial heat flow (a positive contribution to R_{TH}) prevails over the upward heat propagation (a negative contribution to R_{TH}), which is zero in Structure 1. In conclusion, it is found that the shallow trench plays a significant role from the thermal viewpoint.
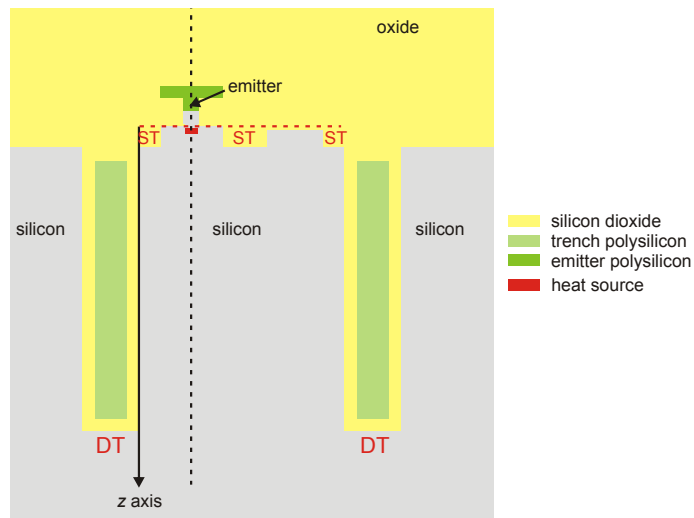
Fig. 4.12. Structure 4 (accounting for ST): cross-section.

Fig. 4.13 and Fig. 4.14 show the temperature rise normalized to dissipated power along the red (horizontal) and black (vertical) dashed lines depicted in Fig. 4.12, respectively.

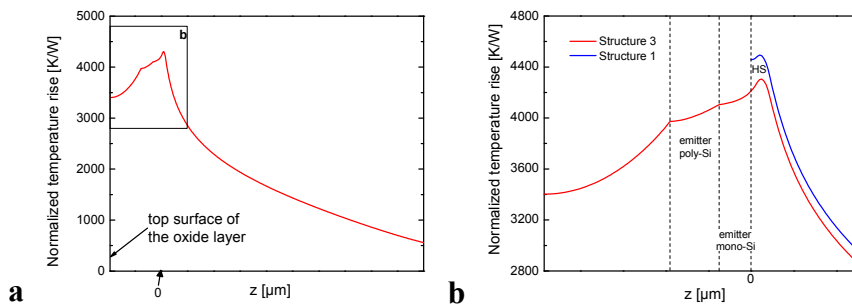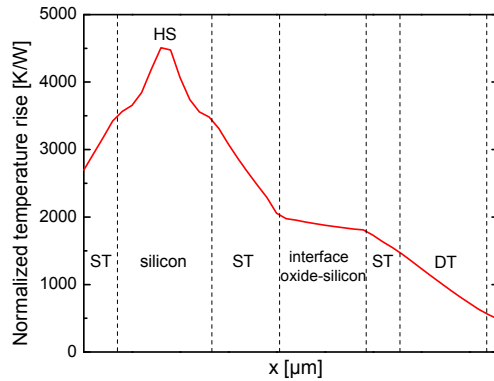**Fig. 4.13.** Structure 4: normalized temperature rise vs. *x* axis along the (horizontal) red line depicted in Fig. 4.12.
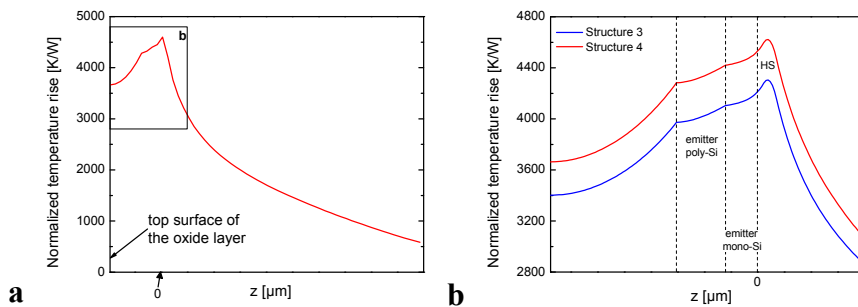
Fig. 4.14. Structure 4: (a) normalized temperature rise vs. *z* axis and (b) detail of the emitter/heat source region. Also shown is the comparison with the ST-free Structure 3 (blue curve).

Base region geometry refinement

As a further step, the base region is finely defined by inserting an oxide layer that surrounds the silicon intrinsic base region (Structure 5 in Fig. 4.15). In this case, a thermal resistance R_{TH5} equal to 4285 K/W was numerically calculated. A slight increase (0.47%) is therefore obtained with respect to R_{TH4}, as a consequence of the small effect of such a layer on the heat propagation. By converse, a significant increase (about 8%) is achieved with respect to Structure 3 due to the concurrent influence of ST and the aforementioned thin oxide layer.
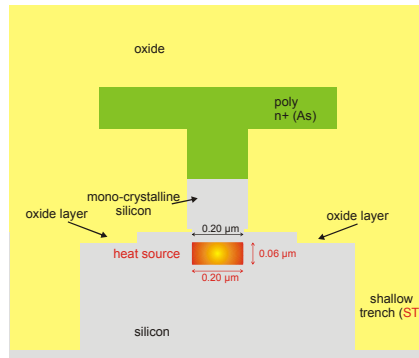
Fig. 4.15. Structure 5 (accounting for the oxide layer surrounding the base region): cross-section.

Germanium influence

In the previous analysis, the base is assumed to be entirely composed by silicon. In this section, we account for the SiGe base (Structure 6 represented in Fig. 4.16).
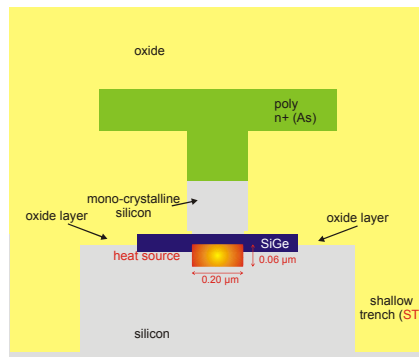
Fig. 4.16. Structure 6 (accounting for SiGe): cross-section.

The real SiGe structure is less thermally conductive than the Si counterpart since germanium exhibits a thermal conductivity lower (i.e., more than halved) than that of silicon (see Table 4.1). In order to properly describe the SiGe base from a thermal standpoint, we implemented within the numerical simulator the following analytical law, which describes the thermal conductivity as a function of depth z and mole fraction of germanium in silicon [33]:

$$k_{SiGe}(z) = \cfrac{1}{\cfrac{1 - x_{SiGe}(z)}{k_{Si}} + \cfrac{x_{SiGe}(z)}{k_{Ge}} + \cfrac{\left[1 - x_{SiGe}(z)\right] \cdot x_{SiGe}(z)}{c_k}} \quad (4.1)$$

where $c_k = 2.8 \cdot 10^{-6}$ W/μmK and $x_{SiGe}(z)$ is the Ge mole fraction, whose profile can be approximated as the sum of three Gaussians[29]

$$x_{SiGe}(z) = N_{p1} \cdot e^{-\left(\frac{z - R_{p1}}{\sigma_1}\right)^2} + N_{p2} \cdot e^{-\left(\frac{z - R_{p2}}{\sigma_2}\right)^2} + N_{p3} \cdot e^{-\left(\frac{z - R_{p3}}{\sigma_3}\right)^2} \quad (4.2)$$

It was found that $R_{TH6} = 4346$ K/W. Hence, the thermal resistance remains almost unchanged compared to Structure 5 (which exhibits a pure silicon base): an increase of only 1.42% is observed.

Fig. 4.17 shows the temperature rise normalized to dissipated power along the vertical line crossing the heat source center. It can be observed that the normalized temperature corresponding to Structure 6 is higher than that of Structure 5 within the low-thermal-conductivity base region, while remaining relatively unchanged over the B-E junction.

Unsilicided base polysilicon ring

The base P^+ polysilicon ring is then accounted for in a simplified form, namely, it is assumed to be entirely unsilicided (Structure 7 in Fig. 4.18). In this case, a self-heating thermal resistance $R_{TH7} = 4171$ K/W was evaluated, that is, a reduction of 4.03% is obtained compared to Structure 6 due to the heat propagation through the polysilicon ring (that operates as a heat spreader).

In Fig. 4.19, the normalized temperature rise along the vertical line crossing the heat source center is represented. It can be observed that

---

[29] As an alternative, one can describe the thermal behavior of the SiGe base by adopting an effective (and space-independent) thermal conductivity k_{eff}, which is evaluated as $(z_2 - z_1) \Big/ \displaystyle\int_{z_1}^{z_2} \frac{dz}{k_{SiGe}(z)}$, where $k_{SiGe}(z)$ is expressed by (4.1). Such a simplified approach could be employed without significant loss of accuracy: as concerns the "complete" domain with slot contacts thermally floating (Structure 9 in Fig. 4.21) a discrepancy of 2.8% was found by using k_{eff} instead of (4.1).

the normalized temperature corresponding to Structure 7 is lower than that of Structure 6 due to the heat spreading effect favored by the P^+ base polysilicon ring.
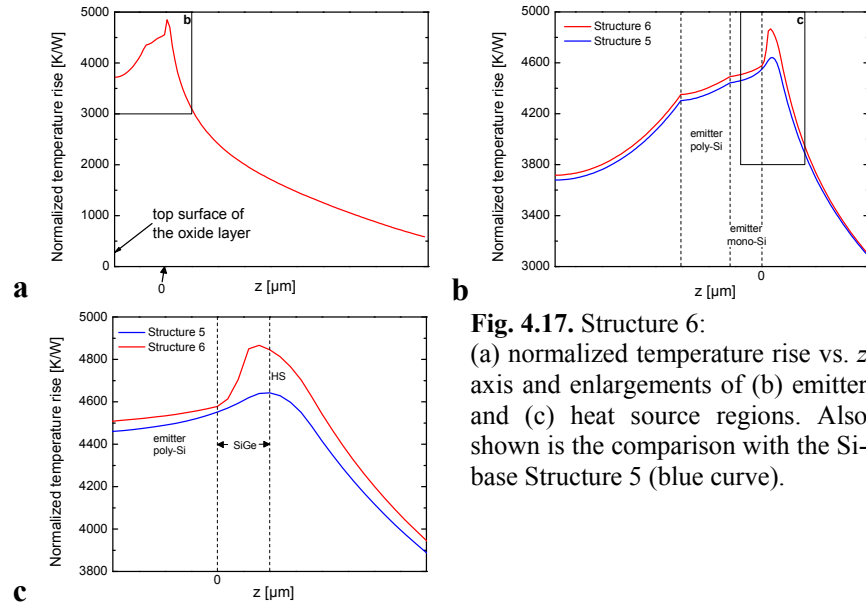
Fig. 4.17. Structure 6: (a) normalized temperature rise vs. z axis and enlargements of (b) emitter and (c) heat source regions. Also shown is the comparison with the Si-base Structure 5 (blue curve).
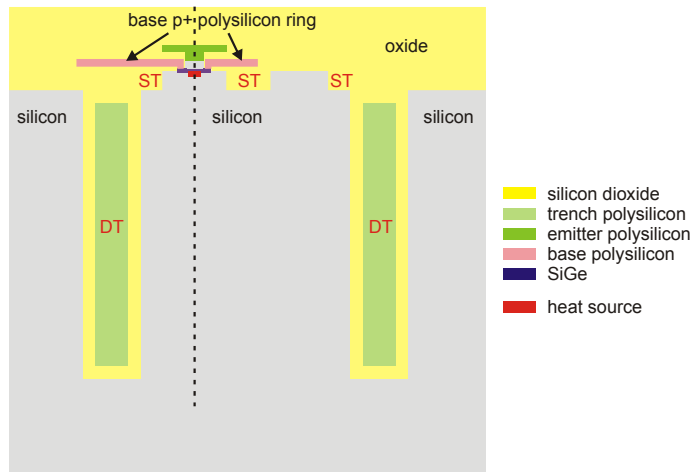
Fig. 4.18. Structure 7 (accounting for the base P^+ polysilicon ring): cross-section.
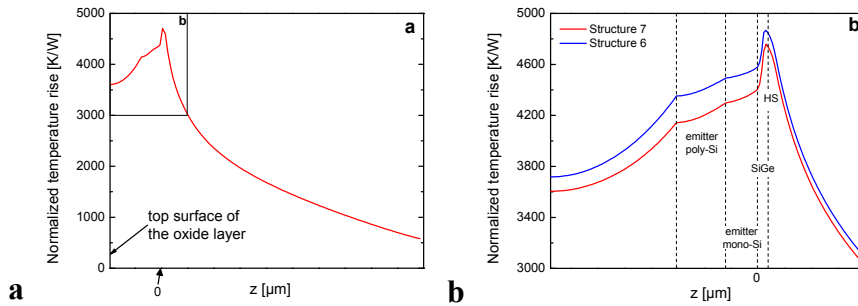
Fig. 4.19. Structure 7: (a) normalized temperature rise vs. *z* axis and (b) detail of the emitter/heat source region. Also shown is the comparison with Structure 6 (blue curve).

Silicided base polysilicon ring

Afterward, the presence of TiSi in the silicided regions of the polysilicon base is accounted for (Structure 8 in Fig. 4.20).[30] A self-heating thermal resistance $R_{TH8} = 4122$ K/W was calculated, which implies a 1.17% reduction with respect to Structure 7 due to the higher thermal conductivity of TiSi compared to the base polysilicon one.
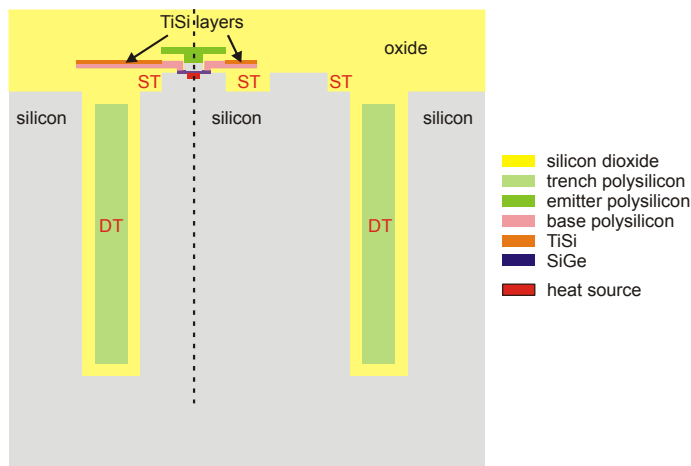
Fig. 4.20. Structure 8 (accounting for the TiSi layers): cross-section.

---

[30] As concerns the thermal conductivity of the TiSi layer, 2.15×10^{-4} W/μmK was adopted for the 3-D numerical simulations (see Table 4.1); such a value was calculated as the average of the values reported in the literature.

Tungsten slot contacts

As a final step, the analysis was carried out on the real (complete) structure, which is obtained by adding the base/emitter/collector tungsten slot contacts (Structure 9 in Fig. 4.21). The simulations were performed by adopting a threefold approach to describe the boundary conditions at the top of the contacts:

1. The top surfaces of the contacts are assumed to be all "thermally floating" (adiabatic boundary condition), that is, they operate as heat spreader. In this case, a self-heating thermal resistance $R_{TH9\text{-}floating}$ amounting to 4068 K/W was numerically found, which corresponds to a negligible reduction (1.31%) compared to the metallization-free Structure 8.

2. The top surfaces of the contacts are assumed to be all "thermally grounded", i.e., in an ideal contact with a heat sink at temperature $T_{AMB} = 300$ K (isothermal boundary condition). In this case, a self-heating thermal resistance $R_{TH9\text{-}grounded}$ amounting to 1940 K/W was numerically found. Contrarily to the *floating* case, the *grounded* metallization plays a role of major importance: simulations show indeed that the heat massively flows toward the isothermal top surfaces of the contacts, thereby leading to a reduction in the thermal resistance of 52.94% compared to Structure 8.

3. Only the top surface of the emitter contact is assumed to be thermally *grounded*, whereas those of base and collector contacts are thermally *floating*. In this case, a self-heating thermal resistance $R_{TH9\text{-}Egrounded}$ amounting to 2149 K/W was numerically evaluated. An increase of only 10.77% is therefore obtained with respect to $R_{TH9\text{-}grounded}$, thereby proving that most of the upward heat propagates through the emitter tungsten slot.
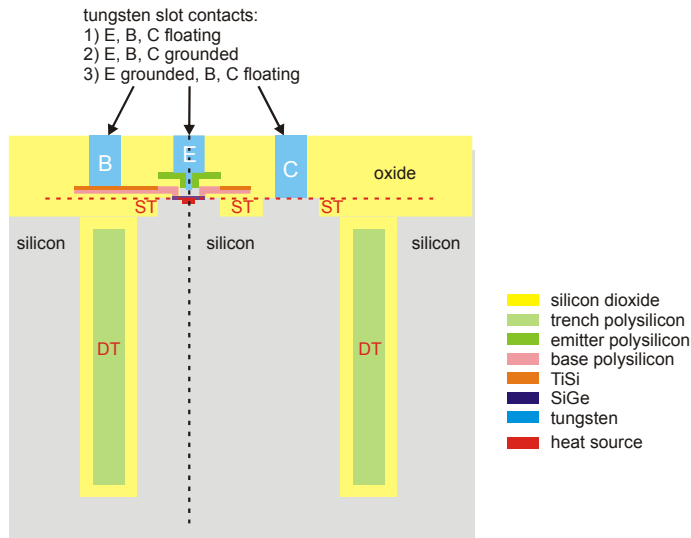
Fig. 4.21. Structure 9 (accounting for the E/B/C tungsten slot contacts): cross-section.

In the following, some distributions of the temperature rise normalized to dissipated power are shown for the "complete" Structure 9, in order to provide a comprehensive overview of the thermal behavior of the SiGe HBT devices under analysis. In particular, the comparison between the *floating*, *grounded*, *only emitter grounded*, and Structure 8 (i.e., the one without the tungsten slot contacts) is shown. The horizontal temperature rise distribution along the dashed red line of Fig. 4.21 (which crosses the B-E junction) is illustrated in Fig. 4.22. Such a figure is represented 4 times to insert more labels that help to plainly understand the influence of the elementary portions of the domain on the temperature field. Fig. 4.23 shows the normalized temperature rise along *y* axis, i.e., that orthogonal to the cross-sections illustrated throughout the investigation. The vertical temperature rise field along the dashed black line of Fig. 4.21 (which crosses the heat source center) is depicted in Fig. 4.24.
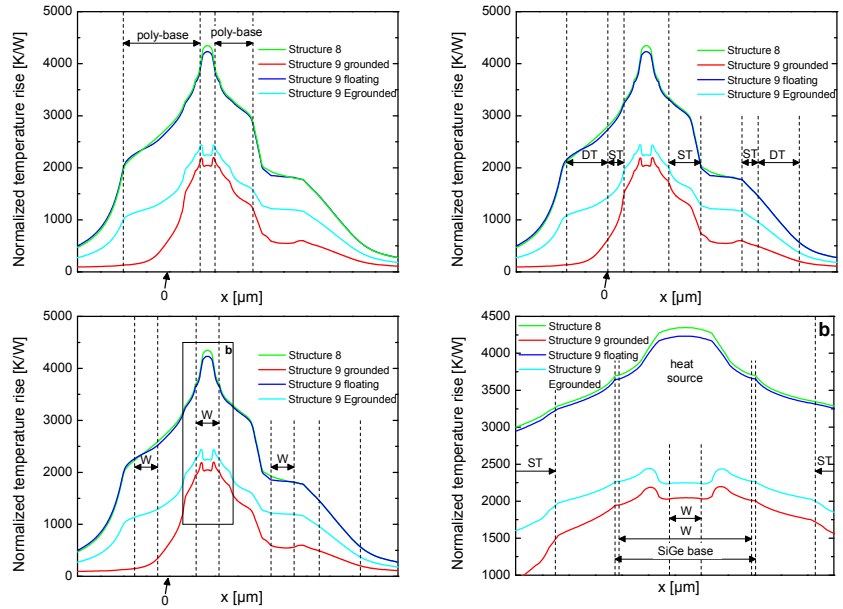
Fig. 4.22. Structure 9: normalized temperature rise along the horizontal red dashed line of Fig. 4.21 (which crosses the B-E junction). Also shown is the comparison with the metallization-free Structure 8.
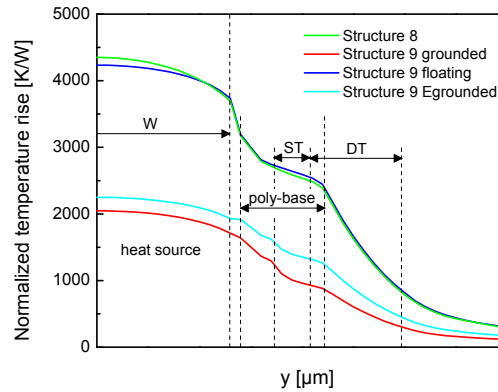
Fig. 4.23. Structure 9: normalized temperature rise along *y* axis (which is orthogonal to the cross-section represented in Fig. 4.21 and crosses the B-E junction). Also shown is the comparison with the metallization-free Structure 8.
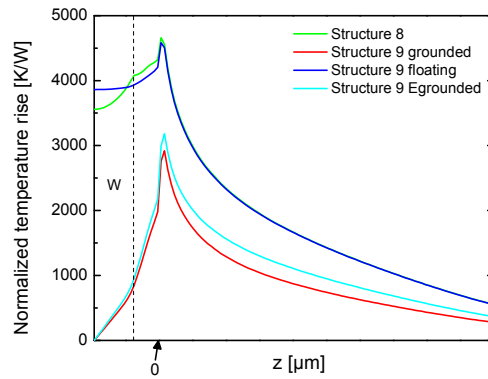
Fig. 4.24. Structure 9: normalized temperature rise along *z* axis (i.e., the black dashed line in Fig. 4.21). Also shown is the comparison with the metallization-free Structure 8.

The thermal behavior of the totally *grounded* SiGe HBT structure (characterized by a self-heating thermal resistance equal to 1940 K/W) was thoroughly analyzed by evaluating the individual *cooling* contributions of the B, E, and C slot contacts since the thermal behavior of the entirely *grounded* HBT can be described as the parallel of 4 thermal resistances (Fig. 4.25), namely:

1. thermal resistance R_{TH8} associated to the path heat source–substrate bottom, namely, that of the metallization-free HBT (Structure 8) estimated to be equal to 4122 K/W;
2. thermal resistance R_{TH-E} associated to the path heat source–emitter contact top;
3. thermal resistance R_{TH-B} associated to the path heat source–base contact top;
4. thermal resistance R_{TH-C} associated to the path heat source–collector contact top.
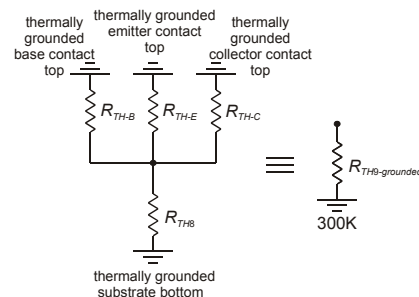
Fig. 4.25. Thermal resistance paths in Structure 9 with entirely *grounded* contacts.

The thermal resistances associated to the paths heat source–top of the contacts B/E/C were evaluated by applying the *superposition principle*, namely, by "eliminating" the slot contacts corresponding to two terminals and evaluating the effect of the remaining one. The thermal resistances corresponding to the HBT structures with only emitter contact, only base contact, and only collector contact were evaluated to be 2152 ($R_{TH8\text{-}E}$), 3772 ($R_{TH8\text{-}B}$), and 3672 K/W ($R_{TH8\text{-}C}$), respectively. Hence, the thermal resistances associated to the paths heat source–contact top can be finally calculated:

> ➤ thermal resistance associated to the path heat source–emitter contact top:

$$R_{TH-E} \, / / \, R_{TH8} = R_{TH8-E} \quad \Rightarrow$$

$$\Rightarrow \quad R_{TH-E} = \frac{R_{TH8-E} R_{TH8}}{R_{TH8} - R_{TH8-E}} = 4501.3 \ \text{K/W}$$

> ➤ thermal resistance associated to the path heat source–base contact top:

$$R_{TH-B} \, / / \, R_{TH8} = R_{TH8-B} \quad \Rightarrow$$

$$\Rightarrow \quad R_{TH-B} = \frac{R_{TH8-B} R_{TH8}}{R_{TH8} - R_{TH8-B}} = 44331 \ \text{K/W}$$

> ➤ thermal resistance associated to the path heat source–collector contact top:

$$R_{TH-C} \, / / \, R_{TH8} = R_{TH8-C} \quad \Rightarrow$$

$$\Rightarrow \quad R_{TH-C} = \frac{R_{TH8-C} R_{TH8}}{R_{TH8} - R_{TH8-C}} = 33597 \ \text{K/W}$$

Lastly, we can evaluate $R_{TH9\text{-}grounded}$ as:

$$R_{TH9-grounded} = R_{TH-E} // R_{TH-B} // R_{TH-C} // R_{TH8} =$$
$$= 1934 \ \mathrm{K/W}$$

that almost coincides to the value extracted by the numerical simulation (1940 K/W).

Summary

All results obtained by the 3-D thermal simulations as well as the domain portions accounted for in each structure are included in Table 4.2.

Table 4.2
Self-heating thermal resistance of the analyzed structures.

	rectangular trench	round trench	poly emitter	shallow trench	oxide layer	SiGe base	poly base	TiSi	tungsten slot contacts	R_{TH} [K/W]
Structure 1	×									4148
Structure 2		×								4118
Structure 3	×		×							3968
Structure 4	×		×	×						4265
Structure 5	×		×	×	×					4285
Structure 6	×		×	×	×	×				4346
Structure 7	×		×	×	×	×	×			4171
Structure 8	×		×	×	×	×	×	×		4122
Structure 9 *floating* E/B/C contacts										4068
Structure 9 *grounded* E/B/C contacts	×		×	×	×	×	×	×	×	1940
Structure 9 *grounded* E contact; B/C *floating*										2149

A pictorial representation of the self-heating thermal resistance behavior as elementary portions of the domain are added is given by histogram 4.1. Histogram 4.2 illustrates the percentage variation in the thermal resistance of domain "i" with respect to that of domain "i-1".
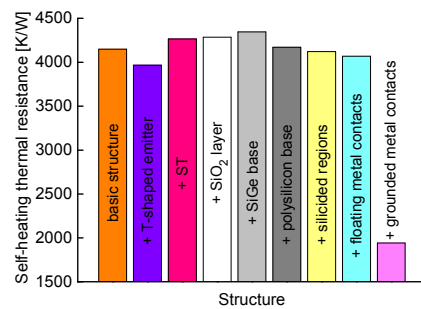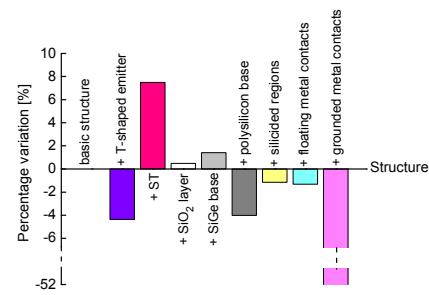
Histogram 4.1.   **Histogram 4.2.**

4.2.2. Parametric analyses

Let us consider the *complete* Structure 9. The self-heating thermal resistance variations are evaluated by changing the values of the following geometrical parameters:

1 emitter length (i.e., heat source length) L_{HS};
2 heat source thickness;
3 emitter width (i.e., heat source width) W_{HS};
4 deep trench depth d_{DT};
5 shallow trench depth d_{ST};
6 deep trench oxide thickness t_{OX};
7 shorter distance between the active device region and deep trench s_3;
8 spacing between long emitter side and shallow trench s_7.

Heat source length

The emitter length was varied over the range 1÷10 μm for three d_{DT} values (d_{DTref}, which corresponds to the reference domain, and other two given by $d_{DTref}/3$ and $5d_{DTref}/3$). The self-heating thermal

resistance behavior as L_{HS} changes at $d_{DT} = d_{DTref}$ is shown in Fig. 4.26.
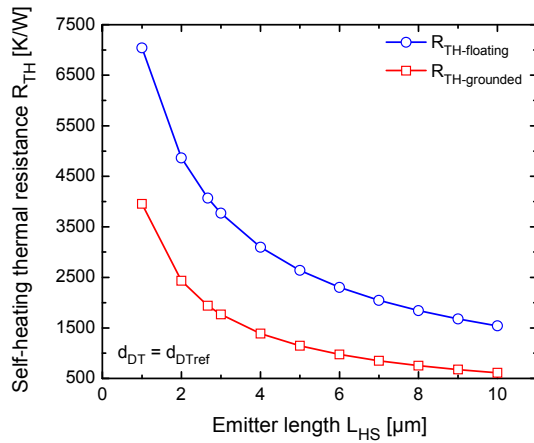
Fig. 4.26. Self-heating thermal resistance vs. emitter length for $d_{DT} = d_{DTref}$.

As the *floating* case is concerned, $R_{TH\text{-}floating}$ reduces from 7042 K/W ($L_{HS} = 1.0$ μm) to 1542 K/W ($L_{HS} = 10$ μm), namely, a decrease of 78% is observed. For the entirely *grounded* case, $R_{TH\text{-}grounded}$ lowers from 3955 K/W to 613 K/W, with a reduction of about 85%.

The $R_{TH\text{-}floating}$ and $R_{TH\text{-}grounded}$ variations vs. L_{HS} for the chosen DT depths are depicted in Fig. 4.27.
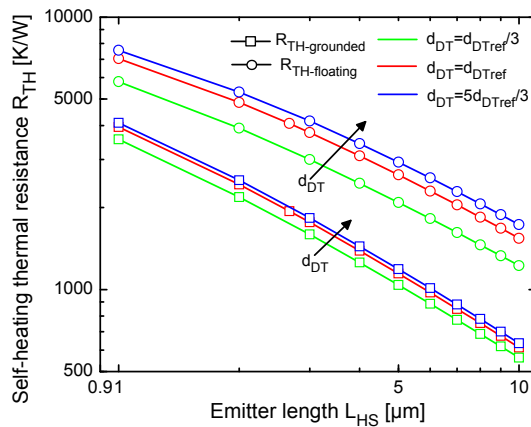
Fig. 4.27. Self-heating thermal resistance vs. emitter length for three d_{DT} values. Both the *floating* and *grounded* cases are represented.

Heat source thickness

The overall analysis is based on the assumption of a partially-depleted SIC, which implies choosing a 0.06 μm-thick heat source. However, the thickness of the depletion region within SIC actually depends upon the device operating conditions. In this section, we analyze the effect on the self-heating thermal resistance of the vertical heat source modulation due to the thickness variation of the depletion region [31]. The analysis was performed on both the *floating* and *grounded* versions of the reference structure by varying the thickness of the heat source within the range 0.03÷0.12 μm. Results are shown in Fig. 4.28. It can be observed that $R_{TH\text{-}floating}$ varies from 4210 to 3888 K/W (with an 8.3% reduction), whilst $R_{TH\text{-}grounded}$ spans from 2027 to 1832 K/W (with a 10.6% reduction).
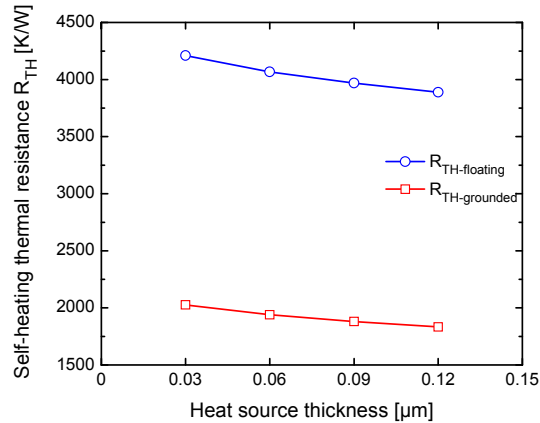
Fig. 4.28. Self-heating thermal resistance vs. heat source thickness for both *floating* and *grounded* versions of Structure 9.

Heat source width

The emitter width was varied over the range 0.05÷0.2 μm (the value in the reference transistor is 0.2 μm). Note that all the distances s_i (i=1, 2, …, 7) are kept constant and equal to the reference ones, while W_{SiGe}, W_{STI}, and W_{BOX} vary (due to the W_{HS} change). The self-heating thermal resistance as a function of W_{HS} is shown in Fig. 4.29.

$R_{TH\text{-}floating}$ linearly reduces from 4438 K/W (at W_{HS} = 0.05 μm) to 4064 K/W (at W_{HS} = 0.2 μm), namely, a decrease of 8.4% is observed

over the analyzed W_{HS} range.
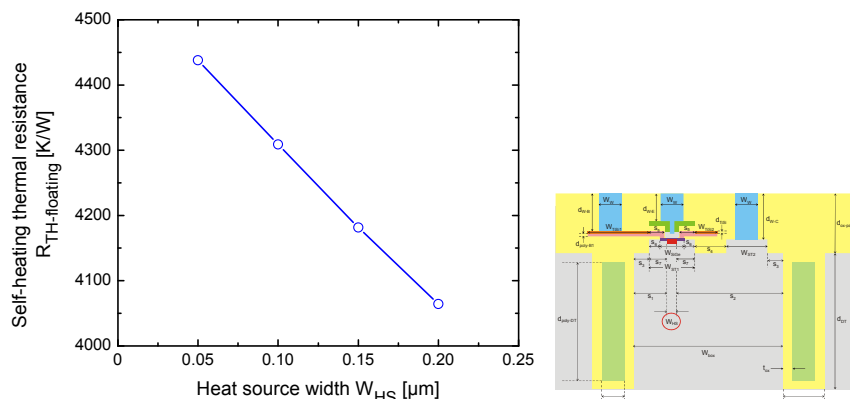
Fig. 4.29. Self-heating thermal resistance vs. emitter (heat source) width.

Deep trench depth

The deep trench depth d_{DT} (see Fig. 4.3) was varied over the range 0 μm÷5d_{DTref}/3 for assigned L_{HS} values, i.e., 2.67 (the emitter length of the reference structure) 1.0, 4.0, 7.0, and 10 μm. The self-heating thermal resistance behavior as a function of trench depth d_{DT} is shown in Fig. 4.30a (for the *floating* case) and b (for the totally *grounded*). It is worth noting that a similar analysis was performed for trench-isolated silicon bipolar transistors in [34] (see also Chapter 3).
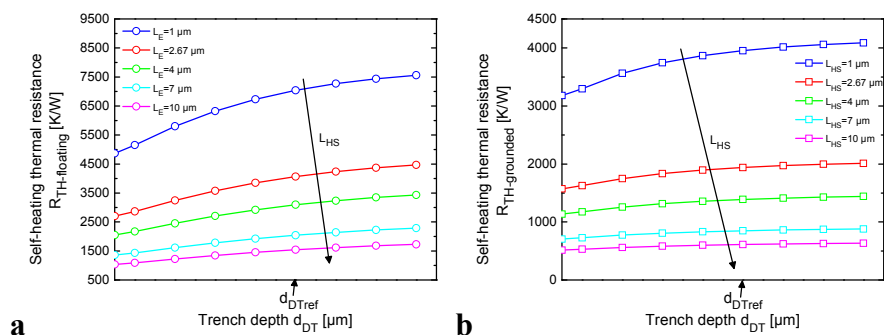
Fig. 4.30. Self-heating thermal resistance vs. DT depth for various L_{HS} values (2.67 μm is the length corresponding to the reference structure). Both the *floating* case (a) and the *grounded* one (b) are analyzed.

As the reference L_{HS} value (2.67 μm) is concerned, $R_{TH\text{-}floating}$ spans from 2706 K/W (absence of DT) to 4471 K/W ($d_{DT} = 5d_{DTref}$/3)

with an increase of about 65%, while $R_{TH\text{-}grounded}$ varies from 1572 to 2013 K/W, with a relatively low increase of 28%. In conclusion, it can be observed that the thermal behavior of a device with thermally *grounded* tungsten contacts is less sensitive to deep trench depth.

Shallow trench depth

The shallow trench depth d_{ST} (see Fig. 4.3) was varied over the range $d_{STref}/3 \div 6d_{STref}$. The sum of d_{DT} (deep trench depth) and d_{ST} is kept constant in the analysis. The self-heating thermal resistance as a function of d_{ST} is shown in Fig. 4.31.
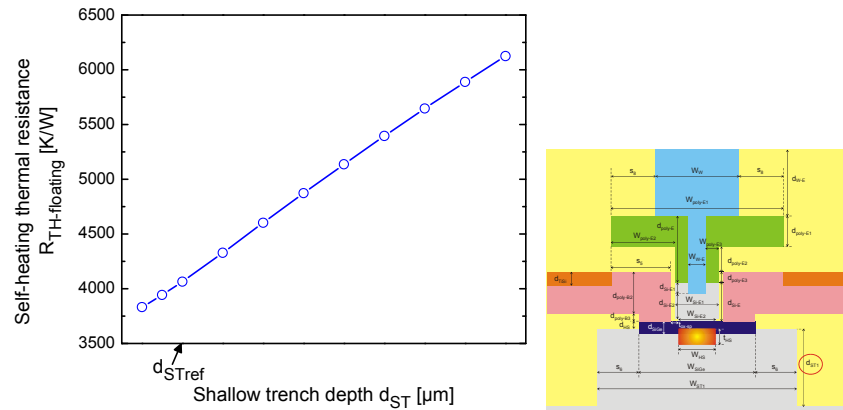
Fig. 4.31. Self-heating thermal resistance vs. shallow trench depth.

$R_{TH\text{-}floating}$ grows from 3831 K/W ($d_{ST} = d_{STref}/3$) to 6124 K/W ($d_{ST} = 6d_{STref.}$), namely, an increase of about 60% is detected. This can be explained by observing that the shallow trench becomes deeper and deeper, thus increasingly counteracting the spreading action of the heat emerging from the base-collector region (see Fig. 4.32).
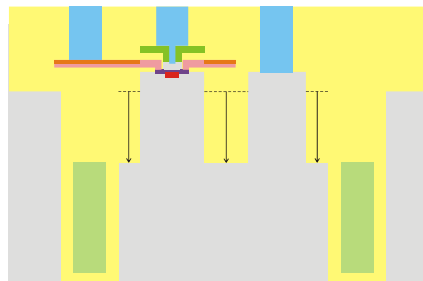
Fig. 4.32. Illustrative draw showing the increase of shallow trench depth.

Deep trench oxide thickness

The deep trench oxide thickness t_{OX} was varied from $t_{OXref}/4$ to $9t_{OXref}/4$ by keeping the deep trench width (W_{DT}) constant (note that the deep trench polysilicon width $W_{poly\text{-}DT}$ reduces). All the other parameters were kept equal to the reference ones. The self-heating thermal resistance behavior as t_{OX} changes is shown in Fig. 4.33.
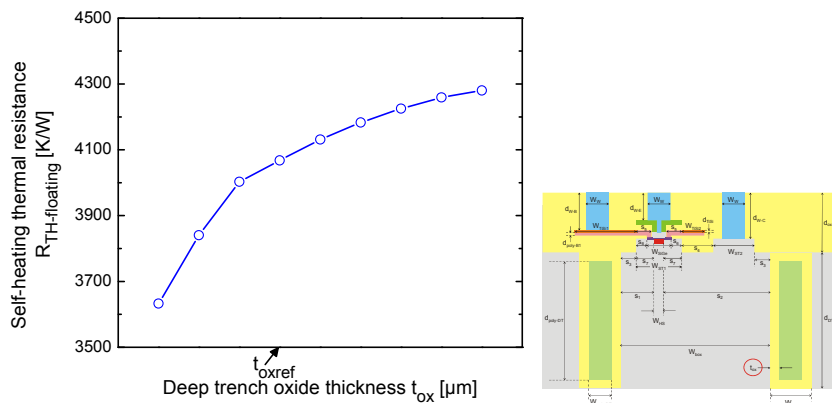
Fig. 4.33. Self-heating thermal resistance vs. deep trench oxide thickness.

It can be seen that $R_{TH\text{-}floating}$ spans from 3633 K/W ($t_{OX} = t_{OXref}/4$) to 4280 K/W ($t_{OX} = 9t_{OXref}/4$, which corresponds to deep trench totally filled with silicon dioxide), with an increase of about 18%. This is the consequence of a decreased medium thermal conductivity of the deep trench.

Shorter distance between the active device region and deep trench

The distance s_3 between active area and deep trench was varied over the range $0 \div 7s_{3ref}/2$. All the other parameters were kept equal to the reference ones, except for W_{BOX} and L_{BOX}. The behavior of the self-heating thermal resistance as a function of s_3 is depicted in Fig. 4.34.
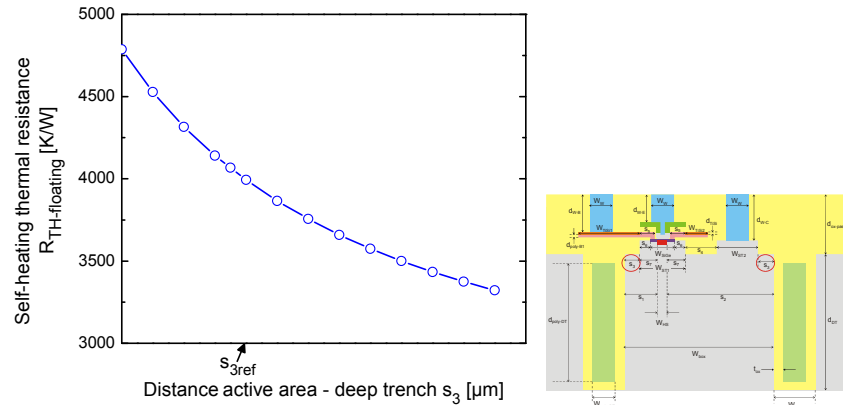
Fig. 4.34. Self-heating thermal resistance vs. distance between active area and deep trench.

$R_{TH\text{-}floating}$ spans from 4787 K/W (for $s_3 = 0$ µm) to 3322 K/W (for $s_3 = 7s_{3ref}/2$); this means that the s_3 increase leads to a significant 31% reduction.

Spacing between long emitter side and shallow trench

In order to vary parameter s_7, we actually modify s_6 (i.e., the spacing between the SiGe base and shallow trench, as shown in Fig. 4.3) by keeping unchanged the SiGe-base width W_{SiGe}. Distance s_6 was varied over the range $0 \div 5s_{6ref}/2$. Two cases were considered:

1. Spacing s_6 (and therefore s_7) was varied by keeping s_3 unchanged. This means that the width (W_{BOX}) and length (L_{BOX}) of the silicon box (surrounded by deep trench) vary. In a similar fashion, some distances as e.g., W_{ST1}, s_1, s_2 are modified;

2. Spacing s_6 (and consequently s_7) was varied by keeping the silicon box size (i.e., W_{BOX} and L_{BOX}) unchanged. Therefore s_3[31] and s_4 decrease as s_6 increases.

The self-heating thermal resistance as a function of s_7 is depicted in Fig. 4.35 for both cases.

---

[31] By carefully observing Fig. 4.3, one can note that there are two distances identified with "s_3". The s_3 spacing we are referring to in the text actually is that nearer to the active device region.
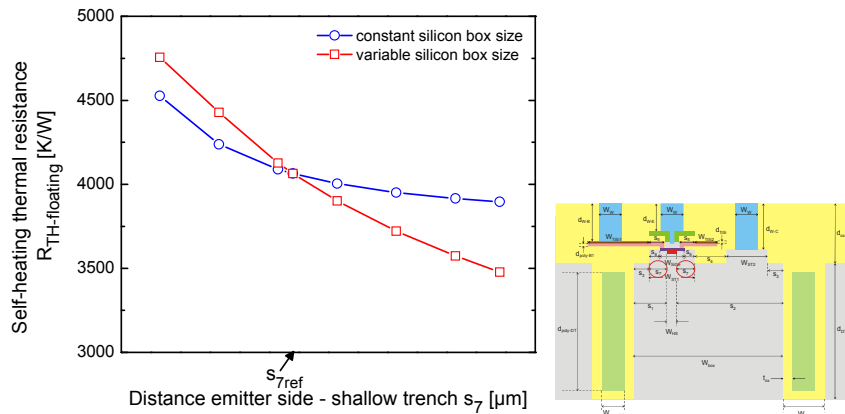
Fig. 4.35. Self-heating thermal resistance vs. distance between emitter side and shallow trench.

$R_{TH\text{-}floating}$ decreases from 4756 K/W (for $s_7 = 2s_{7ref}/5$) to 3478 K/W (for $s_7 = 2s_{7ref}$) and from 4527 K/W to 3896 K/W, for the cases 1 and 2, respectively. Reductions of about 27% and 14% were therefore observed. The higher decrease corresponds to the case in which the silicon box size increases, thereby leading to a larger silicon volume in which the heat can easily spread.

4.2.3. Downscaling analysis

Let us consider the analysis of the downscaling influence on the thermal resistance. We basically "emulated" an aggressive downscaling process by (linearly) reducing the values of all geometrical parameters (starting from those related to the reference structure); the downscaling action on the most relevant layout parameters is illustrated in Table 4.3.

Table 4.3
Downscaled geometrical parameters of the SiGe HBT structure.

parameter	value [μm]
W_{BOX}	$W_{BOXref} \rightarrow 40\% \ W_{BOXref}$
L_{BOX}	$L_{BOXref} \rightarrow 50\% \ L_{BOXref}$
W_{HS}	$0.2 \rightarrow 0.12$

We have performed a twofold investigation:

1. The emitter length L_{HS} is kept constant (i.e., it does not shrink) while scaling all other geometrical parameters. This means that the aspect ratio W_{HS}/L_{HS} of the emitter stripe decreases with downscaling. In this case, the emitter stripe area downscales up to 0.32 µm^2 (starting from the reference 0.534 µm^2 area).
2. The emitter length L_{HS} is reduced by the same factor as the width W_{HS}, thereby leading to a constant aspect ratio during the downscaling process. In this case, L_{HS} lowers up to 1.602 µm (starting from 2.67 µm in the reference device), leading to a downscaled emitter area equal to 0.192 µm^2.

Let us first consider case 1. Fig. 4.36a shows the self-heating thermal resistance increase as the downscaling process evolves. As can be seen, $R_{TH\text{-}floating}$ increases up to 7596 K/W. An increase of about 88% is therefore obtained with respect to the reference structure.

As far as case 2 is concerned, the thermal resistance increases up to 10844 K/W (Fig. 4.36b). A larger increase amounting to 168% is obtained with respect to the reference structure.
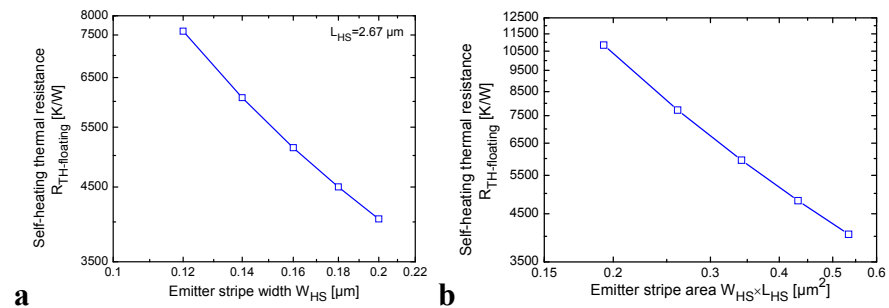
Fig. 4.36. Self-heating thermal resistance as a function of: (a) emitter width in case 1, and (b) emitter area in case 2.

Finally, the emitter length was varied from 0.12 (in order to analyze a square heat source) to 10 µm by keeping all the other parameters equal to the ones of the aggressively scaled structure, for d_{DT} equal to d_{DTref}, $d_{DTref}/3$, and $5d_{DTref}/3$. The self-heating thermal resistance behavior as L_{HS} varies for the chosen DT depths is depicted in Fig. 4.37.
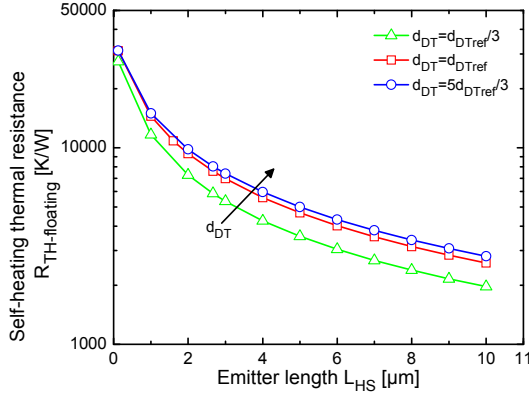
Fig. 4.37. Self-heating thermal resistance of the aggressively scaled structure as a function of emitter length for three d_{DT} values. Only the *floating* case is represented.

As it was expected, the self-heating thermal resistance decreases by increasing the aspect ratio (i.e., increasing L_{HS} by keeping W_{HS} constant) and reaches a maximum for a square source. In particular, for $d_{DT} = d_{DTref}$, $R_{TH\text{-}floating}$ reduces from 31190 K/W ($L_{HS} = 0.12$ µm) to 2596 K/W ($L_{HS} = 10$ µm), namely, a decrease of 92% is observed.

4.2.4. Nonlinear thermal effects

All previous results were obtained by disregarding nonlinear thermal effects, i.e., the thermal conductivities of all materials were assumed to be equal to their values at $T = 300$ K and temperature-insensitive. This implies that the self-heating thermal resistance is independent of dissipated power. In this analysis, we account for nonlinear thermal effects by adopting the following temperature dependence laws for the thermal conductivities of Si, SiGe, and W:

$$k_{Si} = k_{Si}^{300} \cdot \left(\frac{T}{300} \right)^{-1.33} \quad [35]$$

$$k_{SiGe} = k_{SiGe}^{300} \cdot \left(\frac{T}{300} \right)^{-\alpha} \text{ where } \alpha = -1.33 \cdot \left(1 - x_{SiGe} \right) - 1.25 \cdot x_{SiGe} \quad [33]$$

$$k_W = k_W^{300} \cdot \left(\frac{T}{300} \right)^{-0.319} \quad [36]$$

while assuming the thermal conductivities of silicon dioxide [37], polysilicon (regardless of doping level) [38], and TiSi as temperature-insensitive.

The analysis was carried out as follows. After including the above dependence laws in the simulator environment, 3-D simulations were performed by varying the dissipated power from almost 0 to 20 mW and evaluating the corresponding thermal resistance (solid lines in Fig. 4.38). It can be seen that $R_{TH9\text{-}floating}$ rises from 4067 to 4738 K/W (with a 16.5% increase), whereas the thermal resistance $R_{TH9\text{-}grounded}$ varies from 1940 to 2054 K/W (with an increase of about 5.9%). Also shown in the figure are the curves obtained by enabling only the silicon dependence law, namely, assuming k_{SiGe} and k_W as temperature independent (dashed lines).[32]
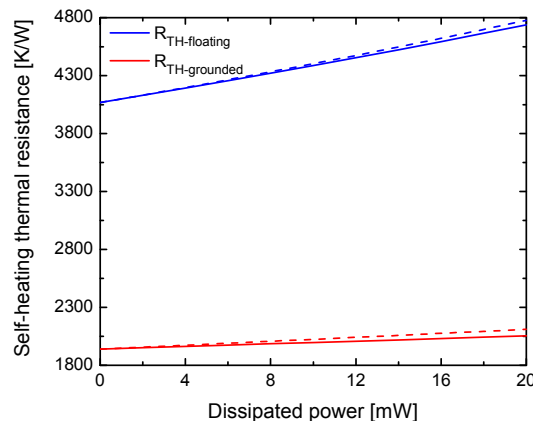
Fig. 4.38. Self-heating thermal resistance vs. dissipated power by enabling the thermal conductivity dependence on temperature for Si, SiGe, W (solid lines) and only for Si (dashed). Both the *floating* (blue curves) and the *grounded* (red) versions of Structure 9 are analyzed.

---

[32] Fig. 4.38 evidences that the thermal resistance is higher when disregarding the thermal conductivity dependence on temperature of SiGe and W (which is negligible). At a first glance, this result seems to be unjustified; however, one should consider that the SiGe layer is located in between heat source and B-E junction (where the thermal resistance is evaluated), so that a decrease in thermal conductivity for such a layer turns into a "cooling effect" for the B-E junction, thereby slightly lowering the thermal resistance.

4.2.5. 2-D vs. 3-D analysis

In this analysis, we compared the self-heating thermal resistances as obtained by fully 3-D numerical simulations for the *grounded* and *floating* cases to those evaluated by simply simulating the 2-D structure corresponding to the cross-section in the *x-z* plane and dividing by the actual emitter length L_{HS}. The comparison was performed over the whole range of emitter lengths analyzed. Results are reported in Fig. 4.39. It can be observed that the 2-D approximation, often employed in the literature, may lead to a significant overestimation of the thermal resistance, especially for reduced emitter lengths, for which the 3-D nature of the heat conduction plays a role of major importance. As far as the case $L_{HS} = 1$ μm is concerned, $R_{TH\text{-}floating\text{-}2D}$ and $R_{TH\text{-}grounded\text{-}2D}$ are equal to 26372 and 7094 K/W, with overestimates of about 275 and 79% compared to the 3-D counterparts, respectively.
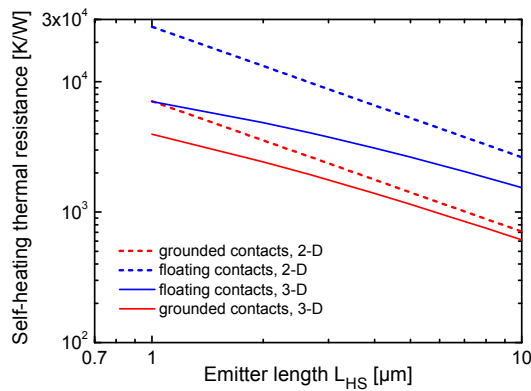
Fig. 4.39. Self-heating thermal resistance vs. emitter length as obtained by fully 3-D (solid lines) and 2-D (short-dashed lines) numerical simulations. Both the *grounded* (red) and *floating* (blue) cases are shown.

4.2.6. Numerical vs. experimental results

Lastly, we compared the self-heating thermal resistances as evaluated by fully 3-D numerical simulations for both the *grounded* and *floating* cases to measurements performed on devices fabricated

in a similar technology (e.g., comparable design rules, about 0.2 μm-wide emitter, same metallization) obtained by varying L_{HS} through the method described in [39]. Results are reported in Fig. 4.40.

It is worth noting that the measurements compare favorably with numerical data as far as $R_{TH\text{-}floating}$ is concerned.
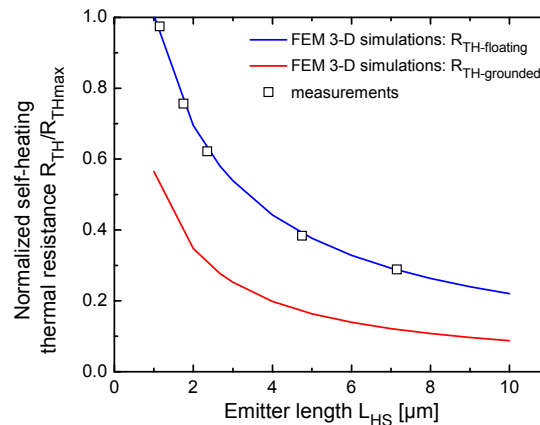
Fig. 4.40. Self-heating thermal resistance normalized to the maximum attained value vs. emitter length as obtained by fully 3-D numerical simulations (solid lines) and measurements (symbols). Both the *grounded* (red) and *floating* (blue) cases are shown.

4.3. Analytical results

Developing an analytical thermal model suited to accurately predict the thermal behavior of trench-isolated SiGe HBT devices is a cumbersome task due to their inherent geometrical complexity. However, the 3-D numerical investigation allowed showing that the thermal behavior of the actual domains is almost identically exhibited by simplified structures (Structure 1) due to the "balance" between the effects of various device portions (which can be therefore removed without loss of accuracy). As a consequence, the thermal behavior of "complete" SiGe structures can be conveniently analyzed by simply referring to analytically manageable (*intrinsic*) deep-trench isolated domains (such as those investigated in Chapter 3). This allows

employing the analytical model developed in Chapter 3 for DTI bipolar transistors fabricated on bulk-silicon substrates.

The model was found indeed to be fairly suited to describe "complete" SiGe transistors through a comparison with 3-D numerical data: a maximum error amounting to about 12% was indeed found by concurrently varying all parameters within the ranges of interest.

Fig. 4.41 depicts the comparison between the analytical and numerical simulations performed by varying the deep trench depth d_{DT} over the range $0 \div 5d_{DTref}/3$ for assigned L_{HS} values, i.e., 2.67 (the emitter length for the reference structure) 1.0, 4.0, 7.0, and 10 µm. As concerns the numerical simulations, only the *floating* case is reported. It can be seen that the error increases as the emitter length decreases.
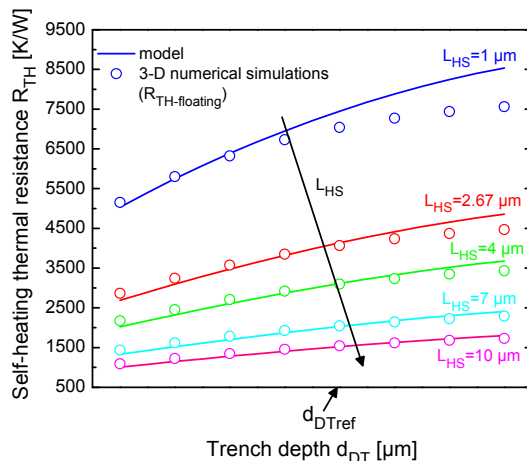
Fig. 4.41. Self-heating thermal resistance vs. DT depth for various L_{HS} values (2.67 µm is the length corresponding to the reference structure). The model (solid lines) is compared to numerical results (symbols).

Fig. 4.42 and Fig. 4.43 show the self-heating thermal resistance by varying the heat source thickness and length, respectively. As can be seen, the analytical model shows a good agreement with numerical results: a maximum error of 1.8% is obtained.
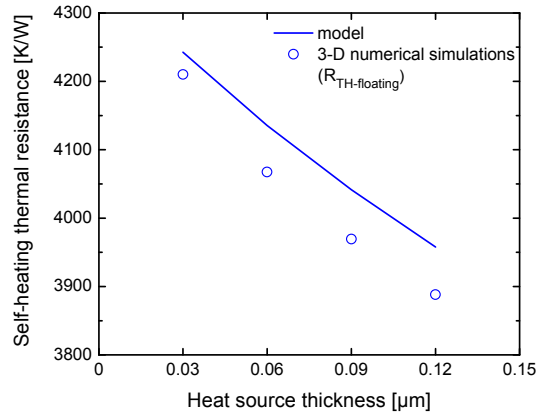
Fig. 4.42. Self-heating thermal resistance vs. heat source thickness. The model (solid lines) is compared to numerical results (symbols).
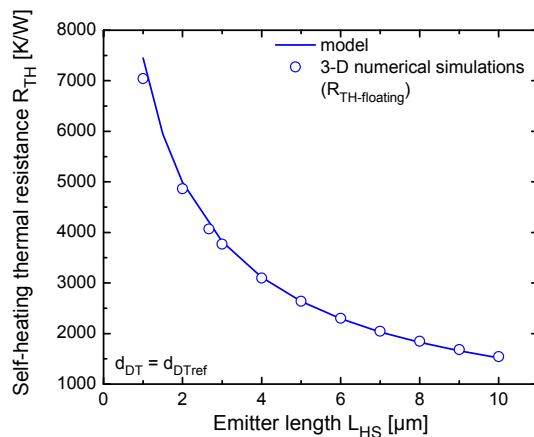
Fig. 4.43. Self-heating thermal resistance vs. emitter length for $d_{DT} = d_{DTref}$. The model (solid lines) is compared to numerical results (symbols).

References

[1]   Cressler JD et al. Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits, and Applications of SiGe and Si Strained-Layer Epitaxy. Taylor & Francis Group; 2006.

[2]   Reisch M. High-frequency Bipolar Transistors: Physics, Modelling, Applications. Springer; 2003

[3]   Harame DL, Comfort JH, Cressler JD, Crabbè EF, Sun JYC, Meyerson BS, et al. Si/SiGe epitaxial-base transistors – Part I: Materials, physics, and circuits. IEEE Trans Electron Dev 1995;42(3):455-68.

[4]   Harame DL, Comfort JH, Cressler JD, Crabbè EF, Sun JYC, Meyerson BS, et al. Si/SiGe epitaxial-base transistors – Part II: Process integration and analog applications. IEEE Trans Electron Dev 1995;42(3):469-82.

[5]   Braunstein R, Moore AR, Herman F. Intrinsic optical absorption in germanium–silicon alloys. Physical Review B 1958;109(3):695-710.

[6]   Theuerer HC, Kleimack JJ, Loar HH, Christensen H. Epitaxial diffused transistors. IEEE IRE Proc 1960;48(9):1642-3.

[7]   Kasper E, Herzog HJ, Kibbel H. A one-dimensional SiGe superlattice grown by UHV epitaxy. Journal Appl Physics 1975;8(3):1541-8.

[8]   Lanzerotti L, Amour A , Liu CW, Sturm JC, Watanabe JK, Theodore ND. Si/Si$_{1-x-y}$Ge$_x$C$_y$ /Si heterojunction bipolar transistors. IEEE Electron Dev Lett 1996;17(7):334-7.

[9]   Schüppen A, Gerlach S, Dietrich H, Wandrei D, Seiler U, König U. 1-W SiGe power HBTs for mobile communications. IEEE Microwave and Guided Wave Lett 1996;6(9):341-3.

[10]   Potyraj PA, Petrosky KJ, Hobart KD, Kub FJ, Thompson PE. A 230-Watt S-band SiGe heterojunction bipolar transistor. IEEE Trans on Microwave Theory and Techniques 1996; 44(12):2392-7.

[11]   Jeng SJ, Jagannathan B, Rieh JS, Johnson J, Schonenberg KT, Greenberg D, et al. A 210-GHz f_T SiGe HBT with nonself-aligned structure. IEEE Electron Dev Lett 2001;22(11):542-4.

[12]   Joseph A, Coolbaugh D, Harame D, Freeman C, Subbarma S, Doherty M, et al. 0.13 µm 210 GHz f_T SiGe HBTs — expanding the horizons of SiGe BiCMOS. IEEE ISSCC 2002:180-2.

[13]   Rieh JS, Jagannathan B, Chen H, Schonenberg KT, Angell D, Chinthakindi A, et al. SiGe HBTs with cut-off frequency of 350 GHz. IEEE IEDM Proc 2002;771-4.

[14] Rieh JS, Greenberg D, Khater M, Schonenberg KT, Jeng JJ, Pagette F, et al. SiGe HBTs for millimeter-wave applications with simultaneously optimized f_T and f_{max} of 300 GHz. IEEE RFIC Proc Symp 2004;395-8.

[15] Sato F, Hashimoto T, Tatsumi T, Kitahata H, Tashiro T. Sub-20 psec ECL circuits with 50 GHz f_{max} self-aligned HBTs. IEEE IEDM Proc 1992;397-400.

[16] Meister TF, Schäfer H, Franosch M, Molzer W, Aufinger K, Scheler U, et al. SiGe base bipolar technology with 74 GHz f_{max} and 11 ps gate delay. IEEE IEDM Proc 1995;739-42.

[17] Pruijmboom A, Terpstra D, Timmering CE, de Boer WB, Theunissen MJJ, Slotboom JW, et al. Selective-epitaxial base technology with 14 ps ECL-gate delay for low power wide-band communication systems. IEEE IEDM Proc 1995;747-50.

[18] Washio K, Ohue E, Oda K, Tanabe M, Shimamoto H, Onai T. A selective-epitaxial SiGe HBT with SMI electrodes featuring 9.3-ps ECL-gate delay. IEEE IEDM Proc 1997;795-8.

[19] Klein W, Klepser BUH. 75 GHz Bipolar production technology for the 21st century. IEEE ESSDERC Proc 1999;88-94.

[20] Tominari T, Wada S, Tokunaga K, Koyu K, Kubo M, Udo T, et al. Study on extremely thin base SiGe:C HBTs featuring sub 5-ps ECL gate delay. IEEE BCTM Proc 2003;107-10.

[21] Hashimoto T, Nonaka Y, Tominari T, Fujiwara H, Tokunaga K, Arai M, et al. Direction to improve SiGe BiCMOS technology featuring 200-GHz SiGe HBT and 80-nm gate CMOS. IEEE IEDM Proc 2003;129-32.

[22] Meister TF, Schäfer H, Aufinger K, Stengl R, Boguth S, Schreiter R, et al. SiGe bipolar technology with 3.9 ps gate delay. IEEE BCTM Proc 2003;103-6.

[23] Böck J, Schäfer H, Aufinger K, Stengl R, Boguth S, Schreiter R, et al. SiGe bipolar technology for automotive radar applications. IEEE BCTM Proc 2004;84-7.

[24] Sato F, Takemura H, Tashiro T, Hirayama H, Hiroi M, Koyama K, et al. A self-aligned selective MBE technology for high-performance bipolar transistors. IEEE IEDM Proc 1990;607-10.

[25] Meister TF, Stengl R, Meul HW, Weyl R, Packan P, Felder A, et al. Sub-20 ps silicon bipolar technology using selective epitaxial growth. IEEE IEDM Proc 1992;401-4.

[26] Lanzerotti LD, Sturm JC, Stach E, Hull R, Buyuklimanli T, Magee C. Suppression of boron outdiffusion in SiGe HBTs by carbon incorporation. IEEE IEDM Proc 1996;249-52.

[27] Osten HJ, Heinemann B, Knoll D, Lippert G, Rücker H. Effects of carbon on boron diffusion in SiGe: principles and impact on bipolar devices. Journal of Vacuum Science and Technology B 1998;16(3):1750-53.

[28] Jouan S, Planche R, Baudry H, Ribot P, Chroboczek JA, Dutartre D, et al. A high-speed low 1/f noise SiGe HBT technology using epitaxially-aligned polysilicon emitters. IEEE Trans Electron Dev 1999;46:1525-29.

[29] Joseph A, Geiss P, Liu X, Johnson J, Schonenberg K, Chakravarti A, et al. Emitter resistance improvement in high-performance SiGe HBTs. ISTDM Proc 2003:53-4.

[30] Rinaldi N. Thermal analysis of solid-state devices and circuits: an analytical approach. Solid-State Electron 2000;44(10):1789-98.

[31] d'Alessandro V, Rinaldi N. A critical review of thermal models for electrothermal simulation. Solid-State Electron 2002;46(4):487-96.

[32] Comsol Multiphysics 3.4, *User's Guide*, Comsol AB, 2007.

[33] Palankovski V. Ph.D. dissertation. Technical University of Vienna, 2000.

[34] Marano I, d'Alessandro V, Rinaldi N. Analytical modeling and numerical simulations of the thermal behavior of trench-isolated bipolar transistors. Submitted to Solid-State Electron.

[35] Negus KJ, Franklin RW, Yovanovich MM. Thermal modeling and experimental techniques for microwave bipolar devices. IEEE Trans on Components, Hybrids, and Manufacturing Technology 1989;12(4):680-9.

[36] Lassner E, Schubert WD. Tungsten: Properties, chemistry, Technology of the element, alloys, and chemical compounds. Plenum Publishers, 1999.

[37] Kleiner MB, Kühn SA, Weber W. Thermal conductivity measurements of thin silicon dioxide films in integrated circuits. IEEE Trans Electron Dev 1996;43(9):1602-9.

[38] McConnell AD, Uma S, Goodson KE. Thermal conductivity of doped polysilicon layers. Journal of Microelectromechanical Systems 2001;10(3):360-9.

[39] Reisch M. Self-Heating in BJT Circuit Parameter Extraction. Solid-State Electron 1992;35(5):677-9.

Appendix A

The heat equation

In this Appendix, the differential equation of heat conduction for a stationary, homogeneous, isotropic solid with heat generation within the region is derived [1], [2].

A.1 The heat equation

Let us consider a stationary, homogeneous, isotropic solid having volume V and bounding surface A with inner heat generation. The energy-balance equation for volume V can be written as:

$$\begin{pmatrix} rate\ of\ energy \\ storage\ in\ V \end{pmatrix} = \begin{pmatrix} rate\ of\ heat \\ entering\ V\ through\ its \\ bounding\ surfaces \end{pmatrix} + \begin{pmatrix} rate\ of\ heat \\ generation\ in\ V \end{pmatrix} \quad (A.3)$$

where:

➢ $$\begin{pmatrix} rate\ of\ energy \\ storage\ in\ V \end{pmatrix} = \int_V \rho c_p \frac{\partial T(\vec{r},t)}{\partial t} dV \quad (A.4)$$

being ρ [Kg/μm^3] the mass density and c_p [J/KgK] the specific heat of the material.

➢ $$\begin{pmatrix} rate\ of\ heat \\ entering\ V\ through\ its \\ bounding\ surfaces \end{pmatrix} = -\int_A \vec{q}(\vec{r},t) \cdot \hat{u}\ dA = \quad (A.5)$$

$$= -\int_V \nabla \cdot \vec{q}(\vec{r},t)\ dV$$

being $-\vec{q} \cdot \hat{u}$ the heat entering V through a small area dA on the bounding surface, $\hat{u}$ the outward normal unit direction vector and $\vec{q}$ the heat flux vector at dA.

➤ $$\begin{pmatrix} rate\ of\ heat \\ generation\ in\ V \end{pmatrix} = \int_V g(\vec{r},t)\,dV \tag{A.6}$$

being $g(\vec{r},t)$ [W/μm^3] the heat generation within volume V that can be function of position and time.

Substituting Eqs. (A.4)-(A.6) into Eq. (A.3) yields:

$$\int_V \left[\rho c_p \frac{\partial T(\vec{r},t)}{\partial t} + \nabla \cdot \vec{q}(\vec{r},t) - g(\vec{r},t) \right] dV = 0 \tag{A.7}$$

and therefore:

$$\rho c_p \frac{\partial T(\vec{r},t)}{\partial t} + \nabla \cdot \vec{q}(\vec{r},t) - g(\vec{r},t) = 0 \tag{A.8}$$

The basic law that relates the heat flow and the temperature gradient $\nabla T(\vec{r},t)$ for a stationary, homogeneous, isotropic solid is given by:

$$\vec{q}(\vec{r},t) = -k(\vec{r},t) \cdot \nabla T(\vec{r},t) \tag{A.9}$$

being k [W/μm^{2}K] the thermal conductivity.

Substituting Eq. (A.9) into Eq. (A.8), finally one obtains:

$$\rho c_p \frac{\partial T(\vec{r},t)}{\partial t} = \nabla \cdot \left[k(\vec{r},t) \cdot \nabla T(\vec{r},t) \right] + g(\vec{r},t) \tag{A.10}$$

that is the differential *equation of heat conduction* for a stationary, homogeneous, isotropic solid with heat generation within the solid itself.

Special cases of Eq. (A.10) can be considered.

1. Uniform thermal conductivity, i.e., independent of position and temperature:

$$\rho c_p \frac{\partial T(\vec{r},t)}{\partial t} = k_0 \nabla^2 T(\vec{r},t) + g(\vec{r},t)$$

which can be rewritten as:

$$\frac{1}{\alpha}\frac{\partial T(\vec{r},t)}{\partial t} = \nabla^2 T(\vec{r},t) + \frac{g(\vec{r},t)}{k} \qquad (A.11)$$

being $\alpha = k_0/\rho c_p$ the thermal diffusivity of the medium.

2. Uniform thermal conductivity and no heat generation within the solid:

$$\frac{1}{\alpha}\frac{\partial T(\vec{r},t)}{\partial t} = \nabla^2 T(\vec{r},t) \qquad (A.12)$$

which is called *Fourier equation of heat conduction*.

3. Uniform thermal conductivity under steady-state conditions:

$$\nabla^2 T(\vec{r}) + \frac{g(\vec{r})}{k_0} = 0 \qquad (A.13)$$

which is *Poisson's equation*.

4. Steady state and no heat generation within the solid:

$$\nabla^2 T(\vec{r},t) = 0 \qquad (A.14)$$

which is *Laplace equation*.

A.2 The boundary conditions

The differential equation of heat conduction will have infinite solutions unless a set of boundary conditions and an initial condition (for the time-dependent problem) are prescribed. The boundary conditions can be both linear and nonlinear. In this Paragraph we will consider only problems involving linear boundary conditions. Such conditions can be subdivided into the following three groups:

1. *Boundary condition of the first kind or Dirichlet condition*
   A temperature, that can be function both time and position, is imposed at the boundary S_i:

$$T(\vec{r},t)\big|_{S_i} = f(\vec{r},t) \tag{A.15}$$

Special cases can be considered, in which the temperature at the boundary surface is a function of position only:

$$T(\vec{r},t)\big|_{S_i} = f(\vec{r}) \tag{A.16}$$

or of time:

$$T(\vec{r},t)\big|_{S_i} = f(t) \tag{A.17}$$

Finally, a homogeneous boundary condition of the first kind is imposed when the temperature at the boundary is kept equal to zero:

$$T(\vec{r},t)\big|_{S_i} = 0 \tag{A.18}$$

Let us note that a boundary surface at constant temperature T_0 (i.e., an isothermal surface) satisfies a homogeneous boundary condition of the first kind if the temperature rise on T_0 is considered.

2. *Boundary condition of the second kind or Neumann condition*
   A heat flux, that can be function both time and position, is imposed at the boundary S_i:

$$k\frac{\partial T(\vec{r},t)}{\partial n_i}\bigg|_{S_i} = f(\vec{r},t) \tag{A.19}$$

where the flux f is directed outward since $\partial/\partial n_i$ denotes differentiation along the outward normal at surface S_i. Also for this boundary condition there are special cases in which f is function only of position or time.
A homogeneous boundary condition of the second kind is imposed when the flux normal at the boundary vanishes:

$$\frac{\partial T(\vec{r},t)}{\partial n_i}\bigg|_{S_i} = 0 \tag{A.20}$$

If Eq. (A.20) is verified, boundary S_i does not allow the flux to leave the solid and it is called *adiabatic.*

3. *Boundary condition of the third kind or Robin condition.*
   A linear combination of temperature and its normal derivative (i.e., the flux going out of S_i) is assigned at the boundary S_i:

$$k \left. \frac{\partial T(\vec{r},t)}{\partial n_i} \right|_{S_i} + h_i \, T(\vec{r},t) \big|_{S_i} = f(\vec{r},t) \qquad (A.21)$$

where term h_i is called the *heat transfer coefficient* [W/μm²K]. A homogeneous boundary condition of the third kind is imposed when:

$$k \left. \frac{\partial T(\vec{r},t)}{\partial n_i} \right|_{S_i} + h_i \, T(\vec{r},t) \big|_{S_i} = 0 \qquad (A.22)$$

Let us point out that these three types of boundary conditions cover most cases of practical interest.

References

[1] Ozisik MN. Boundary value problems of heat conduction. New York: Dover Publications; 1989.
[2] Beck JV, Cole KD, Haji-Sheikh A, Litkouhi B. Heat conduction using Green's functions. London: Hemisphere Publishing Corporation; 1992.

Appendix B

The steady-state analytical solution of the heat flow equation: CASE 1

In this Appendix, the steady-state analytical solution of the heat flow equation in the silicon-only domain with convective boundary conditions at lateral and bottom faces and adiabatic top surface is derived via conventional procedures [1].

The problem to be analyzed is shown in Fig. B.1.
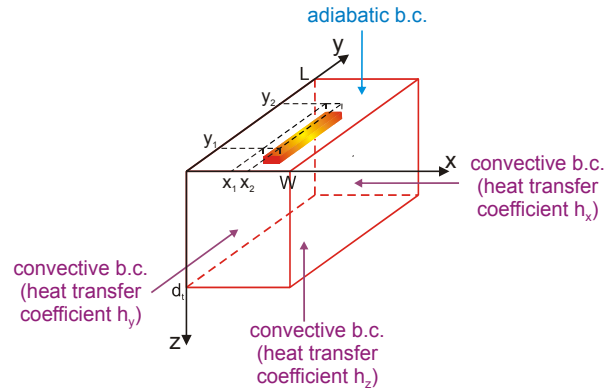
Fig. B.1. Domain under analysis. The boundary conditions are marked.

The substrate is assumed to be a rectangular parallelepiped defined by:

$$0 \leq x \leq W \quad 0 \leq y \leq L \quad 0 \leq z \leq d_t \tag{B.1}$$

As concerns the heat source, both the cases of a rectangular indefinitely thin heat source (THS) embedded within the silicon domain and of a volumetric heat source (VHS) shaped as a rectangular parallelepiped are discussed. The heat source is defined by:

$$x_1 \leq x \leq x_2 \quad y_1 \leq y \leq y_2 \tag{B.2}$$

and $z_1 \leq z \leq z_2$ in the VHS case, while in the THS case it is assumed to be placed at depth $z = d_{HS}$.

As can be seen in Fig. B.1, the boundary conditions are of 3rd kind [Eq. (A.21)] at all surfaces except at $z = 0$ where a boundary condition of 2nd kind [Eq. (A.20)] is assumed:

$$\pm k \left. \frac{\partial T(\vec{r})}{\partial x} \right|_{\substack{x=W \\ x=0}} + h_{xi} \left. T(\vec{r}) \right|_{\substack{x=W \\ x=0}} = h_{xi} T_{AMB} \qquad i = W, 0 \qquad (B.3)$$

$$\pm k \left. \frac{\partial T(\vec{r})}{\partial y} \right|_{\substack{y=L \\ y=0}} + h_{yj} \left. T(\vec{r}) \right|_{\substack{y=L \\ y=0}} = h_{yj} T_{AMB} \qquad j = L, 0 \qquad (B.4)$$

$$k \left. \frac{\partial T(\vec{r})}{\partial z} \right|_{z=d_t} + h_z \left. T(\vec{r}) \right|_{z=d_t} = h_z T_{AMB} \qquad (B.5)$$

$$\left. \frac{\partial T(\vec{r})}{\partial z} \right|_{z=0} = 0 \qquad (B.6)$$

If one considers:

$$\vartheta(\vec{r}) = T(\vec{r}) - T_{AMB} \qquad (B.7)$$

Eq. (A.13) reduces to:

$$\nabla^2 \vartheta(\vec{r}) + \frac{g(\vec{r})}{k} = 0 \qquad (B.8)$$

and Eqs. (B.3)-(B.6) become:

$$\pm k \left. \frac{\partial \vartheta(\vec{r})}{\partial x} \right|_{\substack{x=W \\ x=0}} + h_{xi} \left. \vartheta(\vec{r}) \right|_{\substack{x=W \\ x=0}} = 0 \qquad i = W, 0 \qquad (B.9)$$

$$\pm k \left. \frac{\partial \vartheta(\vec{r})}{\partial y} \right|_{\substack{y=L \\ y=0}} + h_{yj} \left. \vartheta(\vec{r}) \right|_{\substack{y=L \\ y=0}} = 0 \qquad j = L, 0 \qquad (B.10)$$

$$k \left. \frac{\partial \vartheta(\vec{r})}{\partial z} \right|_{z=d_t} + h_z \left. \vartheta(\vec{r}) \right|_{z=d_t} = 0 \qquad (B.11)$$

$$\left. \frac{\partial \vartheta(\vec{r})}{\partial z} \right|_{z=0} = 0 \tag{B.12}$$

We assume that $\vartheta(\vec{r})$ can be expressed as a product of a function of x, a function of y and a function of z:

$$\vartheta(\vec{r}) = X(x)Y(y)Z(z) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} X_n(x)Y_m(y)Z_{nm}(z) \tag{B.13}$$

where $X(x)$ and $Y(y)$ satisfy the following differential equations:

$$\frac{d^2 X(x)}{dx^2} + \beta^2 X(x) = 0 \tag{B.14}$$

$$\frac{d^2 Y(y)}{dy^2} + \alpha^2 Y(y) = 0 \tag{B.15}$$

By substituting Eq. (B.13) into Eq. (B.9), it is straightforward to obtain:

$$\pm k \left. \frac{\partial \vartheta(\vec{r})}{\partial x} \right|_{\substack{x=W \\ x=0}} + h_{xi} \left. \vartheta(\vec{r}) \right|_{\substack{x=W \\ x=0}} = 0 \;\Rightarrow$$

$$\Rightarrow \pm k \left. \frac{\partial \left[X(x)Y(y)Z(z) \right]}{\partial x} \right|_{\substack{x=W \\ x=0}} + h_{xi} \left[X(x)Y(y)Z(z) \right]_{\substack{x=W \\ x=0}} = 0 \Rightarrow$$

$$\Rightarrow \; Y(y)Z(z) \left[\pm k \left. \frac{dX(x)}{dx} \right|_{\substack{x=W \\ x=0}} + h_{xi} \left. X(x) \right|_{\substack{x=W \\ x=0}} \right] = 0 \;\Rightarrow$$

$$\Rightarrow \left[\begin{array}{l} -k \left. \dfrac{dX(x)}{dx} \right|_{x=0} + h_{x0} \left. X(x) \right|_{x=0} = 0 \\[3mm] k \left. \dfrac{dX(x)}{dx} \right|_{x=W} + h_{xW} \left. X(x) \right|_{x=W} = 0 \end{array} \right. \tag{B.16}$$

In the same fashion, the boundary conditions (B.10)-(B.12) can be rewritten in the form:

$$-k\frac{dY(y)}{dy}\bigg|_{y=0} + h_{y0}\,Y(y)\big|_{y=0} = 0$$

$$k\frac{dY(y)}{dy}\bigg|_{y=L} + h_{yL}\,Y(y)\big|_{y=L} = 0$$

(B.17)

$$k\frac{dZ(z)}{dz}\bigg|_{z=d_t} + h_z\,Z(z)\big|_{z=d_t} = 0$$

$$\frac{dZ(z)}{dz}\bigg|_{z=0} = 0$$

(B.18)

By combining Eqs. (B.14) and (B.15) with Eqs. (B.16) and (B.17), respectively, $X(x)$ and $Y(y)$ become the solutions of following one-dimensional problems having homogeneous boundary conditions:

$$\begin{cases} \dfrac{d^2X(x)}{dx^2} + \beta^2 X(x) = 0 \\[2mm] -k\dfrac{dX(x)}{dx}\bigg|_{x=0} + h_{x0}\,X(x)\big|_{x=0} = 0 \\[2mm] k\dfrac{dX(x)}{dx}\bigg|_{x=W} + h_{xW}\,X(x)\big|_{x=W} = 0 \end{cases}$$

(B.19)

$$\begin{cases} \dfrac{d^2Y(y)}{dy^2} + \alpha^2 Y(y) = 0 \\[2mm] -k\dfrac{dY(y)}{dy}\bigg|_{y=0} + h_{y0}\,Y(y)\big|_{y=0} = 0 \\[2mm] k\dfrac{dY(y)}{dy}\bigg|_{y=L} + h_{yL}\,Y(y)\big|_{y=L} = 0 \end{cases}$$

(B.20)

Let us determine the solution of problem (B.19). A general solution of Eq. (B.14) is:

$$X(x) = a\cos(\beta x) + b\sin(\beta x)$$

(B.21)

where a and b can be evaluated by imposing the boundary conditions at surfaces $x = 0$ and $x = W$.

It is straightforward to obtain from Eq. (B.21)[33]:

$$\dot{X}(x) = -a\beta \sin(\beta x) + b\beta \cos(\beta x) \tag{B.22}$$

Therefore, combining Eqs. (B.21) and (B.22) with Eq. (B.16), one obtains:

$\quad\triangleright\quad -k\,\dot{X}(x)\Big|_{x=0} + h_{x0}\,X(x)\Big|_{x=0} = 0 \quad\Rightarrow$

$$\Rightarrow \quad -k\beta\big[-a\sin(\beta x) + b\cos(\beta x)\big]_{x=0} +$$
$$+h_{x0}\big[a\cos(\beta x) + b\sin(\beta x)\big]_{x=0} = 0 \quad\Rightarrow$$
$$\Rightarrow \quad -k\beta b + h_{x0}a = 0 \quad\Rightarrow \quad \frac{b}{a} = \frac{h_{x0}}{k\beta} \tag{B.23}$$

$\quad\triangleright\quad k\,\dot{X}(x)\Big|_{x=W} + h_{xW}\,X(x)\Big|_{x=W} = 0 \quad\Rightarrow$

$$\Rightarrow \quad k\beta\big[-a\sin(\beta x) + b\beta\cos(\beta x)\big]_{x=W} +$$
$$+h_{xW}\big[a\cos(\beta x) + b\sin(\beta x)\big]_{x=W} = 0 \quad\Rightarrow$$
$$\Rightarrow \quad \big[-ka\beta + h_{xW}b\big]\sin(\beta W) =$$
$$= -\big[kb\beta + h_{xW}a\big]\cos(\beta W) \quad\Rightarrow$$
$$\Rightarrow \quad \tan(\beta \cdot W) = \frac{kb\beta + h_{xW}a}{ka\beta - h_{xW}b} = \frac{k\beta\, b/a + h_{xW}}{k\beta - h_{xW}\, b/a} \tag{B.24}$$

Substituting Eq. (B.23) into Eq. (B.24) leads to:

$$\tan(\beta \cdot W) = \frac{h_{x0} + h_{xW}}{k\beta - h_{xW}h_{x0}/k\beta} \tag{B.25}$$

If we consider:

$\quad\triangleright\quad B_1 = h_{x0}/k \tag{B.26}$

$\quad\triangleright\quad B_2 = h_{xW}/k \tag{B.27}$

---

[33] Throughout the overall treatment we will denote with $\dot{X}$ and $\ddot{X}$ the first and second derivative of function $X(x)$ respect to x, respectively.

Eq. (B.25) reduces to:

$$\tan(\beta \cdot W) = \frac{B_1 + B_2}{\beta - B_1 B_2 / \beta} \qquad (B.28)$$

Therefore, substituting Eq. (B.23) combined with Eq. (B.26), into Eq. (B.21), $X(x)$ can be rewritten as:

$$X_n(x) = a\left[\cos(\beta_n x) + \frac{B_1}{\beta_n}\sin(\beta_n x)\right] \qquad (B.29)$$

where β_n are the positive eigenvalues of:

$$\tan(W \cdot \beta_n) = \frac{\beta_n(B_1 + B_2)}{\beta_n^2 - B_1 B_2} \qquad (B.30)$$

We can determine a of Eq. (B.29) by imposing equal to 1 the norm of eigenfunctions $X_n(x)$.

Let us evaluate norm N of eigenfunctions $X_n(x)$:

$$N = \int_0^W X_n^2(x)\, dx \qquad (B.31)$$

From Eq. (B.29) we have:

$$\left.\begin{array}{l} X_n^2 = a^2\left[\cos(\beta_n x) + \dfrac{B_1}{\beta_n}\sin(\beta_n x)\right]^2 \\[2ex] \left(\dfrac{\dot{X}_n}{\beta_n}\right)^2 = a^2\left[-\sin(\beta_n x) + \dfrac{B_1}{\beta_n}\cos(\beta_n x)\right]^2 \end{array}\right\} \Rightarrow$$

$$\Rightarrow \quad X_n^2 + \frac{\dot{X}_n^2}{\beta_n^2} = a^2\left(1 + \frac{B_1^2}{\beta_n^2}\right) \quad \Rightarrow$$

$$\Rightarrow \quad X_n^2 = a^2\left(1 + \frac{B_1^2}{\beta_n^2}\right) - \frac{\dot{X}_n^2}{\beta_n^2} \qquad (B.32)$$

Therefore Eq. (B.31) can be rewritten as:

$$N = a^2 \left(1 + \frac{B_1^2}{\beta_n^2} \right) W - \frac{1}{\beta_n^2} \int_0^W \dot{X}_n^2 dx \qquad (B.33)$$

Recalling Eq. (B.14), Eq. (B.31) becomes:

$$N = -\frac{1}{\beta_n^2} \int_0^W X_n \cdot \ddot{X}_n dx = -\frac{1}{\beta_n^2} \left[X_n \cdot \dot{X}_n \right]_0^W + \frac{1}{\beta_n^2} \int_0^W \dot{X}_n^2 dx \qquad (B.34)$$

Now, adding Eq. (B.33) to Eq.(B.34), we have:

$$2N = a^2 \left(1 + \frac{B_1^2}{\beta_n^2} \right) W - \frac{1}{\beta_n^2} \left[X_n \cdot \dot{X}_n \right]_0^W \qquad (B.35)$$

Combining Eq. (B.16) with Eq. (B.26) and (B.27) yields:

$$\dot{X}_n \big|_{x=0} = B_1 X_n \big|_{x=0} \Rightarrow X_n \big|_{x=0} \cdot \dot{X}_n \big|_{x=0} = B_1 X_n \big|_{x=0}^2 = B_1 \cdot a^2 \quad (B.36)$$

$$\dot{X}_n \big|_{x=W} = -B_2 X_n \big|_{x=W} \Rightarrow \begin{cases} X_n \big|_{x=W} \cdot \dot{X}_n \big|_{x=W} = -B_2 X_n \big|_{x=W}^2 & (i) \\ \dot{X}_n \big|_{x=W}^2 = B_2^2 X_n \big|_{x=W}^2 & (ii) \end{cases} \quad (B.37)$$

Substituting Eq. (B.37)(*ii*) into Eq. (B.32) leads to:

$$X_n \big|_{x=W}^2 = a^2 \left(1 + \frac{B_1^2}{\beta_n^2} \right) - \frac{B_2^2 \cdot X_n \big|_{x=W}^2}{\beta_n^2} \Rightarrow$$

$$\Rightarrow \left(1 + \frac{B_2^2}{\beta_n^2} \right) X_n \big|_{x=W}^2 = a^2 \left(1 + \frac{B_1^2}{\beta_n^2} \right) \Rightarrow$$

$$\Rightarrow X_n \big|_{x=W}^2 = a^2 \frac{1 + B_1^2 / \beta_n^2}{1 + B_2^2 / \beta_n^2} \qquad (B.38)$$

Substituting Eqs. (B.36) and (B.37)(*i*) combined with Eq. (B.38) into Eq. (B.35), one obtains:

$$2N = a^2 \left(1 + \frac{B_1^2}{\beta_n^2} \right) W + \frac{a^2}{\beta_n^2} \left[B_2 \frac{1 + B_1^2 / \beta_n^2}{1 + B_2^2 / \beta_n^2} + B_1 \right]$$

Now, by equating the norm of eigenfunctions $X_n(x)$ to 1, a can be evaluated:

$$N = 1 \implies \frac{a^2}{2}\left\{\left(1+\frac{B_1^2}{\beta_n^2}\right)W + \frac{1}{\beta_n^2}\left[B_2\frac{1+B_1^2/\beta_n^2}{1+B_2^2/\beta_n^2}+B_1\right]\right\} = 1 \implies$$

$$\implies a = \frac{\sqrt{2}}{\left[\left(1+\frac{B_1^2}{\beta_n^2}\right)W + \frac{1}{\beta_n^2}\left(B_2\frac{1+B_1^2/\beta_n^2}{1+B_2^2/\beta_n^2}+B_1\right)\right]^{1/2}} \tag{B.39}$$

Finally, substituting Eq. (B.39) into Eq. (B.29), we can evaluate the expression of eigenfunctions $X_n(x)$:

$$X_n(x) = \frac{\beta_n\cos(\beta_n x)+B_1\sin(\beta_n x)}{D_n} \tag{B.40}$$

where:

➢ $B_1 = h_{x0}/k$

➢ $B_2 = h_{xW}/k$

➢ β_n are the positive eigenvalues of:

$$\tan(\beta_n \cdot W) = \frac{\beta_n(B_1+B_2)}{\beta_n^2-B_1 B_2}$$

➢ $D_n = \left[\dfrac{\beta_n^2+B_1^2}{2}\cdot\left(W+\dfrac{B_2}{\beta_n^2+B_2^2}\right)+\dfrac{B_1}{2}\right]^{1/2}$ \tag{B.41}

Analogously, it can be found that:

$$Y_m(y) = \frac{\alpha_m\cos(\alpha_n y)+C_1\sin(\alpha_m y)}{E_m} \tag{B.42}$$

where:

➢ $C_1 = h_{y0}/k$

➢ $C_2 = h_{yL}/k$

➢ α_m are the positive eigenvalues of:

$$\tan(\alpha_m \cdot L) = \frac{\alpha_m(C_1+C_2)}{\alpha_m^2-C_1 C_2} \tag{B.43}$$

$$\succ \quad E_m = \left[\frac{\alpha_m^2 + C_1^2}{2} \cdot \left(L + \frac{C_2}{\alpha_m^2 + C_2^2} \right) + \frac{C_1}{2} \right]^{1/2} \tag{B.44}$$

Let us evaluate $Z_{nm}(z)$ so as to satisfy the problem (B.8) with the boundary conditions (B.18).

Substituting Eq. (B.13) into Eq. (B.8) gives rise to:

$$\nabla^2 \vartheta(\vec{r}) + \frac{g(\vec{r})}{k} = 0 \Rightarrow \nabla^2 \left[\sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) Z_{nm}(z) \right] + \frac{g(\vec{r})}{k} = 0 \Rightarrow$$

$$\Rightarrow \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \ddot{X}_n(x) Y_m(y) Z_{nm}(z) + \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) \ddot{Y}_m(y) Z_{nm}(z) +$$

$$+ \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) \ddot{Z}_{nm}(z) + \frac{g(\vec{r})}{k} = 0 \tag{B.45}$$

From Eq. (B.40) we have:

$$X_n(x) = \frac{\beta_n \cos(\beta_n x) + B_1 \sin(\beta_n x)}{D_n} \quad \Rightarrow$$

$$\Rightarrow \dot{X}_n(x) = \frac{-\beta_n^2 \sin(\beta_n x) + B_1 \beta_n \cos(\beta_n x)}{D_n} \quad \Rightarrow$$

$$\Rightarrow \ddot{X}_n(x) = \frac{-\beta_n^3 \cos(\beta_n x) - B_1 \beta_n^2 \sin(\beta_n x)}{D_n} = \tag{B.46}$$

$$= -\beta_n^2 \frac{\beta_n \cos(\beta_n x) - B_1 \sin(\beta_n x)}{D_n} = -\beta_n^2 X_n(x)$$

Analogously, it can be found that:

$$\ddot{Y}_m(y) = -\alpha_m^2 Y_m(y) \tag{B.47}$$

Substituting Eqs. (B.46) and (B.47) into Eq. (B.45) leads to:

$$-\sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \left(\beta_n^2 + \alpha_m^2 \right) X_n(x) Y_m(y) Z_{nm}(z) +$$

$$+ \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) \ddot{Z}_{nm}(z) + \frac{g(\vec{r})}{k} = 0 \quad \Rightarrow$$

$$\Rightarrow \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} X_n(x)Y_m(y)\left[-\left(\beta_n^2+\alpha_m^2\right)Z_{nm}(z)+\ddot{Z}_{nm}(z)\right]+$$

$$+\frac{g(\vec{r})}{k}=0 \quad\Rightarrow$$

$$\Rightarrow \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} X_n(x)Y_m(y)\left[-\gamma_{nm}^2 Z_{nm}(z)+\ddot{Z}_{nm}(z)\right]+\frac{g(\vec{r})}{k}=0 \quad \text{(B.48)}$$

where:

$$\gamma_{nm}^2 = \beta_n^2 + \alpha_m^2 \tag{B.49}$$

Multiplying Eq. (B.48) by $X_i(x)Y_j(y)$ and integrating in x and y over $[0, W]$ and $[0, L]$, respectively, we have:

$$-\gamma_{ij}^2 Z_{ij}(z)+\ddot{Z}_{ij}(z)=-\int_0^W\int_0^L \frac{g(x,y,z)}{k} X_i(x)Y_j(y)\,dy\,dx \tag{B.50}$$

In order to simplify the problem, we assume that $g(\vec{r})$ can be expressed as a product of a function of x, a function of y and a function of z:

$$g(\vec{r}) = p(x)q(y)r(z) \tag{B.51}$$

Therefore Eq. (B.50) reduces to:

$$\ddot{Z}_{ij}(z)-\gamma_{ij}^2 Z_{ij}(z)=-\frac{1}{k}G_{ij}\cdot r(z) \tag{B.52}$$

where we defined:

$$G_{ij} \triangleq \int_0^W p(x)X_i(x)\,dx\int_0^L q(y)Y_j(y)\,dy \tag{B.53}$$

Therefore the problem to solve is:

$$
\begin{cases}
\dfrac{d^2 Z_{ij}(z)}{dz^2} - \gamma_{ij}^2 Z_{ij}(z) = -\dfrac{1}{k} G_{ij} \cdot r(z) & (i) \\[2ex]
\left.\dfrac{dZ_{ij}(z)}{dz}\right|_{z=0} = 0 & (ii) \\[2ex]
k\left.\dfrac{dZ_{ij}(z)}{dz}\right|_{z=d_t} + h_z\, Z_{ij}(z)\big|_{z=d_t} = 0 & (iii)
\end{cases}
\qquad \text{(B.54)}
$$

Note that the results obtained are valid both in both THS and VHS cases.

The general solution of the homogeneous equation associated to Eq. (B.52) is:

$$
Z_{ij0}(z) = A_{ij}\cosh(\gamma_{ij}z) + B_{ij}\sinh(\gamma_{ij}z)
\qquad \text{(B.55)}
$$

while its particular solution is:

$$
u(z) = w_1(z)\cosh(\gamma_{ij}z) + w_2(z)\sinh(\gamma_{ij}z)
\qquad \text{(B.56)}
$$

that will be evaluated by means of Lagrange method. Therefore:

$$
\begin{cases}
w_1'(z)\cosh(\gamma_{ij}z) + w_2'(z)\sinh(\gamma_{ij}z) = 0 & (i) \\[2ex]
w_1'(z)\sinh(\gamma_{ij}z) + w_2'(z)\cosh(\gamma_{ij}z) = -\dfrac{1}{k} G_{ij}\cdot r(z) & (ii)
\end{cases}
\Rightarrow \text{(B.57)}
$$

$$
\Rightarrow
\begin{cases}
w_1'(z) = \dfrac{1}{k}\dfrac{G_{ij}\cdot r(z)}{\gamma_{ij}}\sinh(\gamma_{ij}z) \\[2ex]
w_2'(z) = -\dfrac{1}{k}\dfrac{G_{ij}\cdot r(z)}{\gamma_{ij}}\cosh(\gamma_{ij}z)
\end{cases}
\Rightarrow
$$

$$
\Rightarrow
\begin{cases}
w_1(z) = \dfrac{G_{ij}}{k}\displaystyle\int_0^z \sinh(\gamma_{ij}\zeta)\dfrac{r(\zeta)}{\gamma_{ij}}\,d\zeta & (i) \\[3ex]
w_2(z) = -\dfrac{G_{ij}}{k}\displaystyle\int_0^z \cosh(\gamma_{ij}\zeta)\dfrac{r(\zeta)}{\gamma_{ij}}\,d\zeta & (ii)
\end{cases}
\qquad \text{(B.58)}
$$

Substituting Eqs. (B.58) into Eq. (B.56) yields:

$$u(z) = \frac{G_{ij}}{k} \left[\begin{array}{l} \cosh(\gamma_{ij}z) \int_0^z \sinh(\gamma_{ij}\zeta) \frac{r(\zeta)}{\gamma_{ij}} d\zeta - \\ -\sinh(\gamma_{ij}z) \int_0^z \cosh(\gamma_{ij}\zeta) \frac{r(\zeta)}{\gamma_{ij}} d\zeta \end{array} \right] \qquad \text{(B.59)}$$

Therefore, from Eqs. (B.55) and (B.59), we have:

$$\begin{aligned} Z_{ij}(z) &= Z_{ij0}(z) + u(z) = \\ &= A_{ij} \cosh(\gamma_{ij}z) + B_{ij} \sinh(\gamma_{ij}z) - \\ &\quad - \frac{G_{ij}}{k} \left[\begin{array}{l} \sinh(\gamma_{ij}z) \int_0^z \cosh(\gamma_{ij}\zeta) \frac{r(\zeta)}{\gamma_{ij}} d\zeta - \\ -\cosh(\gamma_{ij}z) \int_0^z \sinh(\gamma_{ij}\zeta) \frac{r(\zeta)}{\gamma_{ij}} d\zeta \end{array} \right] \end{aligned} \qquad \text{(B.60)}$$

A_{ij} and B_{ij} can be determined by satisfying the boundary conditions at surfaces $z = 0$ and $z = d_t$.

Combining Eq. (B.54)(*ii*) with Eq. (B.60), we have:

$$\frac{dZ_{ij}(z)}{dz}\bigg|_{z=0} = 0 \ \Rightarrow \ \frac{dZ_{ij0}(z)}{dz}\bigg|_{z=0} + \frac{du(z)}{dz}\bigg|_{z=0} = 0 \ \Rightarrow \ B_{ij} = 0 \ \text{ (B.61)}$$

since:

> $$\begin{aligned} \frac{dZ_{ij0}(z)}{dz} &= \frac{d}{dz}\left[A_{ij} \cosh(\gamma_{ij}z) + B_{ij} \sinh(\gamma_{ij}z) \right] = \\ &= \gamma_{ij}\left[A_{ij} \sinh(\gamma_{ij}z) + B_{ij} \cosh(\gamma_{ij}z) \right] \ \Rightarrow \end{aligned}$$
>
> $$\Rightarrow \ \frac{dZ_{ij0}(z)}{dz}\bigg|_{z=0} = \gamma_{ij} B_{ij}$$

> $$\begin{aligned} \frac{du(z)}{dz} &= \frac{d}{dz}\left[w_1(z) \cosh(\gamma_{ij}z) + w_2(z) \sinh(\gamma_{ij}z) \right] = \\ &= \left[w_1'(z) \cosh(\gamma_{ij}z) + w_2'(z) \sinh(\gamma_{ij}z) \right] + \\ &\quad + \gamma_{ij}\left[w_1(z) \sinh(\gamma_{ij}z) + w_2(z) \cosh(\gamma_{ij}z) \right] = \end{aligned}$$

$$= \gamma_{ij} \left[w_1(z)\sinh(\gamma_{ij}z) + w_2(z)\cosh(\gamma_{ij}z) \right] \quad \Rightarrow \quad \text{(B.62)}$$

$$\Rightarrow \quad \left. \frac{du(z)}{dz} \right|_{z=0} = \gamma_{ij} w_2(0) = 0$$

being $w_1'(z)\cosh(\gamma_{ij}z) + w_2'(z)\sinh(\gamma_{ij}z) = 0$ by Eq. (B.57)(*i*)

and $w_2(0) = 0$ by Eq. (B.58)(*ii*).

Substituting Eq. (B.61) into Eq. (B.60), we have:

$$Z_{ij}(z) = A_{ij}\cosh(\gamma_{ij}z) + u(z) \tag{B.63}$$

From Eq. (B.54)(*iii*), combined with Eqs. (B.63), (B.62) and (B.56), one obtains:

$$k\gamma_{ij}A_{ij}\sinh(\gamma_{ij}d_t) + k\,\dot{u}(z)\big|_{z=d_t} + h_z A_{ij}\cosh(\gamma_{ij}d_t) + h_z u(z)\big|_{z=d_t} = 0 \Rightarrow$$

$$\Rightarrow k\gamma_{ij}A_{ij}\sinh(\gamma_{ij}d_t) + k\gamma_{ij}\left[w_1(d_t)\sinh(\gamma_{ij}d_t) + w_2(d_t)\cosh(\gamma_{ij}d_t) \right] +$$

$$+ h_z A_{ij}\cosh(\gamma_{ij}d_t) + h_z\left[w_1(d_t)\cosh(\gamma_{ij}d_t) + w_2(d_t)\sinh(\gamma_{ij}d_t) \right] = 0 \Rightarrow$$

$$\Rightarrow \left[k\gamma_{ij}\sinh(\gamma_{ij}d_t) + h_z\cosh(\gamma_{ij}d_t) \right] A_{ij} +$$

$$+ k\gamma_{ij}\left[w_1(d_t)\sinh(\gamma_{ij}d_t) + w_2(d_t)\cosh(\gamma_{ij}d_t) \right] +$$

$$+ h_z\left[w_1(d_t)\cosh(\gamma_{ij}d_t) + w_2(d_t)\sinh(\gamma_{ij}d_t) \right] = 0 \Rightarrow$$

$$\Rightarrow A_{ij} = -\frac{\left(\begin{array}{l} k\gamma_{ij}\left[w_1(d_t)\sinh(\gamma_{ij}d_t) + w_2(d_t)\cosh(\gamma_{ij}d_t) \right] + \\ + h_z\left[w_1(d_t)\cosh(\gamma_{ij}d_t) + w_2(d_t)\sinh(\gamma_{ij}d_t) \right] \end{array} \right)}{k\gamma_{ij}\sinh(\gamma_{ij}d_t) + h_z\cosh(\gamma_{ij}d_t)} \tag{B.64}$$

B.1   THS case

Assuming a uniform dissipation within the heat generating region in Eq. (B.51), we have:

$$
\blacktriangleright \quad p(x)q(y) = \begin{cases} q_s & \forall (x,y): \begin{bmatrix} x_1 \le x \le x_2 \\ y_1 \le y \le y_2 \end{bmatrix} \\ 0 & \text{elsewhere} \end{cases} \tag{B.65}
$$

$$
\blacktriangleright \quad r(z) = \delta(z - d_{HS}) \tag{B.66}
$$

Substituting Eq. (B.65) into Eq. (B.53), combined with Eqs. (B.40) and (B.42), it is straightforward to obtain:

$$
G_{nm} = \frac{q_s}{D_n \cdot E_m} \int_{x_1}^{x_2} \left[\beta_n \cos(\beta_n x) + B_1 \sin(\beta_n x) \right] dx \times
$$

$$
\times \int_{y_1}^{y_2} \left[\alpha_m \cos(\alpha_m y) + C_1 \sin(\alpha_m y) \right] dy =
$$

$$
= \frac{q_s}{D_n \cdot E_m} \left[\sin(\beta_n x) - \frac{B_1}{\beta_n} \cos(\beta_n x) \right]_{x_1}^{x_2} \times
$$

$$
\times \left[\sin(\alpha_m y) - \frac{C_1}{\alpha_m} \cos(\alpha_m y) \right]_{y_1}^{y_2} =
$$

$$
= \frac{q_s}{D_n \cdot E_m} \times
$$

$$
\times \left\{ \sin(\beta_n x_2) - \sin(\beta_n x_1) - \frac{B_1}{\beta_n} \left[\cos(\beta_n x_2) - \cos(\beta_n x_1) \right] \right\} \times \tag{B.67}
$$

$$
\times \left\{ \sin(\alpha_m y_2) - \sin(\alpha_m y_1) - \frac{C_1}{\alpha_m} \left[\cos(\alpha_m y_2) - \cos(\alpha_m y_1) \right] \right\}
$$

From Eqs. (B.58), combined with Eq. (B.66), we have:

$$
\blacktriangleright \quad w_1(z) = \begin{cases} 0 & z < d_{HS} \\ \dfrac{G_{nm}}{\gamma_{nm} k} \sinh(\gamma_{nm} d_{HS}) & z \ge d_{HS} \end{cases} \tag{B.68}
$$

$$
\blacktriangleright \quad w_2(z) = \begin{cases} 0 & z < d_{HS} \\ -\dfrac{G_{nm}}{\gamma_{nm} k} \cosh(\gamma_{nm} d_{HS}) & z \ge d_{HS} \end{cases} \tag{B.69}
$$

Substituting Eqs. (B.68) and (B.69) into Eqs. (B.56) and (B.64), we have:

$$\blacktriangleright \quad u(z) = \begin{cases} 0 & z < d_{HS} \\ \dfrac{G_{nm}}{\gamma_{nm} k} \sinh\left[\gamma_{nm}\left(d_{HS} - z\right)\right] & z \geq d_{HS} \end{cases} \tag{B.70}$$

$$\blacktriangleright \quad A_{nm} = \frac{G_{nm}}{\gamma_{nm} k} \times \tag{B.71}$$

$$\times \frac{k\gamma_{nm} \cosh\left[\gamma_{nm}\left(d_{HS} - d_t\right)\right] + h_z \sinh\left[\gamma_{nm}\left(d_t - d_{HS}\right)\right]}{k\gamma_{nm} \sinh\left(\gamma_{nm} d_t\right) + h_z \cosh\left(\gamma_{nm} d_t\right)}$$

Finally, we can evaluate the expression of $Z_{nm}(z)$ by substituting Eqs. (B.70) and (B.71) into Eq. (B.63).

B.2   VHS case

Assuming, also in this case, a uniform dissipation within the heat generating region, Eq. (B.51) becomes:

$$g(x, y, z) = q_v \cdot p(x) q(y) r(z) \tag{B.72}$$

where:

$$\blacktriangleright \quad p(x) = q(y) = r(z) = \begin{cases} 1 & \forall (x, y): \begin{bmatrix} x_1 \leq x \leq x_2 \\ y_1 \leq y \leq y_2 \\ z_1 \leq z \leq z_2 \end{bmatrix} \\ 0 & \text{elsewhere} \end{cases} \tag{B.73}$$

Substituting Eq. (B.73) into Eq. (B.53) combined with Eqs. (B.40) and (B.42), it is straightforward to obtain:

$$G_{nm} = \frac{1}{D_n \cdot E_m} \times$$

$$\times \left\{ \sin\left(\beta_n x_2\right) - \sin\left(\beta_n x_1\right) - \frac{B_1}{\beta_n}\left[\cos\left(\beta_n x_2\right) - \cos\left(\beta_n x_1\right)\right] \right\} \times \quad \text{(B.74)}$$

$$\times \left\{ \sin\left(\alpha_m y_2\right) - \sin\left(\alpha_m y_1\right) - \frac{C_1}{\alpha_m}\left[\cos\left(\alpha_m y_2\right) - \cos\left(\alpha_m y_1\right)\right] \right\}$$

Combining Eqs. (B.58) with Eq. (B.73) yields:

$$\triangleright \quad w_1(z) = \begin{cases} 0 & z < z_1 \\[2mm] \dfrac{G_{nm}}{\gamma_{nm}^2 k}\left[\cosh\left(\gamma_{nm} z\right) - \cosh\left(\gamma_{nm} z_1\right)\right] & z_1 \le z \le z_2 \\[3mm] \dfrac{G_{nm}}{\gamma_{nm}^2 k}\left[\cosh\left(\gamma_{nm} z_2\right) - \cosh\left(\gamma_{nm} z_1\right)\right] & z > z_2 \end{cases} \quad \text{(B.75)}$$

$$\triangleright \quad w_2(z) = \begin{cases} 0 & z < z_1 \\[2mm] -\dfrac{G_{nm}}{\gamma_{nm}^2 k}\left[\sinh\left(\gamma_{nm} z\right) - \sinh\left(\gamma_{nm} z_1\right)\right] & z_1 \le z \le z_2 \\[3mm] -\dfrac{G_{nm}}{\gamma_{nm}^2 k}\left[\sinh\left(\gamma_{nm} z_2\right) - \sinh\left(\gamma_{nm} z_1\right)\right] & z > z_2 \end{cases} \quad \text{(B.76)}$$

Substituting Eqs. (B.75) and (B.76) into Eqs. (B.56) and (B.64), we have:

$$\triangleright \quad u(z) = \begin{cases} 0 & z < z_1 \\[2mm] \dfrac{G_{nm}}{\gamma_{nm}^2 k}\left\{1 - \cosh\left[\gamma_{nm}\left(z_1 - z\right)\right]\right\} & z_1 \le z \le z_2 \\[3mm] \dfrac{G_{nm}}{\gamma_{nm}^2 k}\left\{ \begin{matrix} \cosh\left[\gamma_{nm}\left(z_2 - z\right)\right] - \\ -\cosh\left[\gamma_{nm}\left(z_1 - z\right)\right] \end{matrix} \right\} & z > z_2 \end{cases} \quad \text{(B.77)}$$

➤ $A_{nm} = -\dfrac{G_{nm}}{\gamma_{nm}^2 k} \dfrac{1}{k\gamma_{nm}\sinh(\gamma_{nm}d_t) + h_z\cosh(\gamma_{nm}d_t)} \times$

$$\times \begin{pmatrix} k\gamma_{nm}\left\{\sinh\left[\gamma_{nm}(d_t - z_2)\right] - \sinh\left[\gamma_{nm}(d_t - z_1)\right]\right\} + \\ +h_z\left\{\cosh\left[\gamma_{nm}(d_t - z_2)\right] - \cosh\left[\gamma_{nm}(d_t - z_1)\right]\right\} \end{pmatrix} \quad \text{(B.78)}$$

Finally, we can evaluate the expression of $Z_{nm}(z)$ in the VHS case by substituting Eqs. (B.77) and (B.78) into Eq. (B.63).

References

[1]   Beck JV, Cole KD, Haji-Sheikh A, Litkouhi B. Heat conduction using Green's functions. London: Hemisphere Publishing Corporation; 1992.

Appendix C

The steady-state analytical solution of the heat flow equation: CASE 2

In this Appendix, the steady-state analytical solution of the heat flow equation in the domain with convective boundary conditions at lateral faces and adiabatic top and bottom surfaces is derived via conventional procedures [1].

The problem to be analyzed is shown in Fig. C.1.
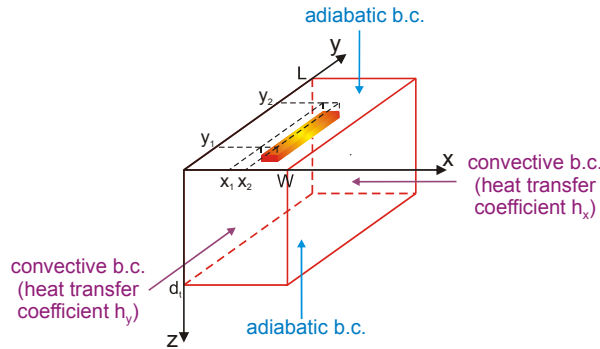
Fig. C.1. Domain under analysis. The boundary conditions are evidenced.

The substrate is assumed to be a rectangular parallelepiped defined by:

$$0 \le x \le W \quad 0 \le y \le L \quad 0 \le z \le d_t \qquad (C.1)$$

As concerns the heat source, both the cases of a rectangular indefinitely thin heat source (THS) embedded within the silicon domain and of a volumetric heat source (VHS) shaped as a rectangular parallelepiped are discussed. The heat source is defined by:

$$x_1 \le x \le x_2 \quad y_1 \le y \le y_2 \qquad (C.2)$$

and $z_1 \leq z \leq z_2$ in the VHS case, while in the THS case it is assumed to be placed at depth $z = d_{HS}$.

As can be seen in Fig. C.1, the boundary conditions are of 3rd kind [Eq. (A.21)] at all lateral surfaces ($x = 0$, W and $y = 0$, L) while at $z = 0$ and $z = d_t$, boundary conditions of 2nd kind [Eq. (A.20)] are assumed:

$$\pm k \left. \frac{\partial T(\vec{r})}{\partial x} \right|_{\substack{x=W \\ x=0}} + h_{xi} \left. T(\vec{r}) \right|_{\substack{x=W \\ x=0}} = h_{xi} T_{AMB} \qquad i = W,0 \qquad \text{(C.3)}$$

$$\pm k \left. \frac{\partial T(\vec{r})}{\partial y} \right|_{\substack{y=L \\ y=0}} + h_{yj} \left. T(\vec{r}) \right|_{\substack{y=L \\ y=0}} = h_{yj} T_{AMB} \qquad j = L,0 \qquad \text{(C.4)}$$

$$\left. \frac{\partial T(\vec{r})}{\partial z} \right|_{\substack{z=0 \\ z=d_t}} = 0 \qquad \text{(C.5)}$$

If we consider:

$$\vartheta(\vec{r}) = T(\vec{r}) - T_{AMB} \qquad \text{(C.6)}$$

Eq. (A.13) reduces to:

$$\nabla^2 \vartheta(\vec{r}) + \frac{g(\vec{r})}{k} = 0 \qquad \text{(C.7)}$$

and Eqs. (C.3)-(C.5) become:

$$\pm k \left. \frac{\partial \vartheta(\vec{r})}{\partial x} \right|_{\substack{x=W \\ x=0}} + h_{xi} \left. \vartheta(\vec{r}) \right|_{\substack{x=W \\ x=0}} = 0 \qquad i = W,0 \qquad \text{(C.8)}$$

$$\pm k \left. \frac{\partial \vartheta(\vec{r})}{\partial y} \right|_{\substack{y=L \\ y=0}} + h_{yj} \left. \vartheta(\vec{r}) \right|_{\substack{y=L \\ y=0}} = 0 \qquad j = L,0 \qquad \text{(C.9)}$$

$$\left. \frac{\partial \vartheta(\vec{r})}{\partial z} \right|_{\substack{z=0 \\ z=d_t}} = 0 \qquad \text{(C.10)}$$

We assume that $\vartheta(\vec{r})$ can be expressed as a product of a function of x, a function of y, and a function of z:

$$\mathcal{G}(\vec{r}) = X(x)Y(y)Z(z) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} X_n(x)Y_m(y)Z_{nm}(z) \qquad \text{(C.11)}$$

where the unknown functions $X_n(x)$ and $Y_m(y)$ are solutions of one-dimensional problems (B.19) and (B.20).

Therefore (see Appendix B), we have:

> $X_n(x) = \dfrac{\beta_n \cos(\beta_n x) + B_1 \sin(\beta_n x)}{D_n}$ \qquad (C.12)

> $Y_m(y) = \dfrac{\alpha_m \cos(\alpha_n y) + C_1 \sin(\alpha_m y)}{E_m}$ \qquad (C.13)

where:

  ✓ $B_1 = h_{x0}/k$ \qquad (C.14)
  ✓ $B_2 = h_{xW}/k$ \qquad (C.15)
  ✓ β_n are the positive eigenvalues of:

  $$\tan(\beta_n \cdot W) = \frac{\beta_n(B_1 + B_2)}{\beta_n^2 - B_1 B_2} \qquad \text{(C.16)}$$

  ✓ $D_n = \left[\dfrac{\beta_n^2 + B_1^2}{2}\cdot\left(W + \dfrac{B_2}{\beta_n^2 + B_2^2}\right) + \dfrac{B_1}{2}\right]^{1/2}$ \qquad (C.17)

  ✓ $C_1 = h_{y0}/k$ \qquad (C.18)
  ✓ $C_2 = h_{yL}/k$ \qquad (C.19)
  ✓ α_m are the positive eigenvalues of:

  $$\tan(\alpha_m \cdot L) = \frac{\alpha_m(C_1 + C_2)}{\alpha_m^2 - C_1 C_2} \qquad \text{(C.20)}$$

  ✓ $E_m = \left[\dfrac{\alpha_m^2 + C_1^2}{2}\cdot\left(L + \dfrac{C_2}{\alpha_m^2 + C_2^2}\right) + \dfrac{C_1}{2}\right]^{1/2}$ \qquad (C.21)

By assuming, as in Appendix B, that $g(\vec{r})$ can be expressed as a product of a function of x, a function of y, and a function of z:

$$g(\vec{r}) = p(x)q(y)r(z) \qquad \text{(C.22)}$$

and defining:

> $\gamma_{nm}^2 = \beta_n^2 + \alpha_m^2$ (C.23)

> $G_{nm} \triangleq \int\limits_0^W p(x) X_n(x) dx \int\limits_0^L q(y) Y_m(y) dy$ (C.24)

$Z_{nm}(z)$ becomes the solution of the following one-dimensional problem:

$$\begin{cases} \dfrac{d^2 Z_{nm}(z)}{dz^2} - \gamma_{ij}^2 Z_{nm}(z) = -\dfrac{1}{k} G_{nm} \cdot r(z) & (i) \\[3mm] \left. \dfrac{dZ_{nm}(z)}{dz} \right|_{z=0} = 0 & (ii) \\[3mm] \left. \dfrac{dZ_{nm}(z)}{dz} \right|_{z=d_t} = 0 & (iii) \end{cases}$$ (C.25)

where:

$$Z_{nm}(z) = Z_{nm0}(z) + u(z)$$ (C.26)

and:

> $Z_{nm0}(z) = A_{nm} \cosh(\gamma_{nm} z) + B_{nm} \sinh(\gamma_{nm} z)$ (C.27)

> $u(z) = w_1(z) \cosh(\gamma_{nm} z) + w_2(z) \sinh(\gamma_{nm} z)$ (C.28)

with:

✓ $w_1(z) = \dfrac{G_{nm}}{k_t} \int\limits_0^z \sinh(\gamma_{nm} \zeta) \dfrac{r(\zeta)}{\gamma_{nm}} d\zeta$ (C.29)

✓ $w_2(z) = -\dfrac{G_{nm}}{k_t} \int\limits_0^z \cosh(\gamma_{nm} \zeta) \dfrac{r(\zeta)}{\gamma_{nm}} d\zeta$ (C.30)

Also in this case, A_{nm} and B_{nm} can be determined by satisfying the boundary conditions at surfaces $z = 0$ and $z = d_t$.

From Eq. (C.25)(*ii*), we have:

$$\left. \frac{dZ_{nm}(z)}{dz} \right|_{z=0} = 0 \implies B_{nm} = 0$$

so that Eq. (C.26) becomes:

$$Z_{nm}(z) = A_{nm}\cosh(\gamma_{nm}z) + u(z) \tag{C.31}$$

Combining Eq. (C.25)(*iii*) with Eq. (B.62) leads to:

$$\left.\frac{dZ_{nm}(z)}{dz}\right|_{z=d_t} = 0 \;\Rightarrow\; A_{nm}\left.\frac{d\left[\cosh(\gamma_{nm}z)\right]}{dz}\right|_{z=d_t} + \left.\frac{du(z)}{dz}\right|_{z=d_t} = 0 \;\Rightarrow$$

$$\Rightarrow\; A_{nm}\gamma_{nm}\sinh(\gamma_{nm}d_t) + \gamma_{nm}\left[\begin{matrix}w_1(z)\sinh(\gamma_{nm}z) + \\ +w_2(z)\cosh(\gamma_{nm}z)\end{matrix}\right]_{z=d_t} = 0 \;\Rightarrow$$

$$\Rightarrow\; A_{nm} = -\frac{w_1(d_t)\sinh(\gamma_{nm}d_t) + w_2(d_t)\cosh(\gamma_{nm}d_t)}{\sinh(\gamma_{nm}d_t)} \tag{C.32}$$

C.1 THS case

Assuming a uniform dissipation within the heat generating region in Eq. (C.22) we have:

➢ $$p(x)q(y) = \begin{cases} q_s & \forall(x,y): \begin{bmatrix} x_1 \le x \le x_2 \\ y_1 \le y \le y_2 \end{bmatrix} \\ 0 & \text{elsewhere} \end{cases} \tag{C.33}$$

➢ $$r(z) = \delta(z - d_{HS}) \tag{C.34}$$

Substituting Eq. (C.33) into Eq. (C.24) combined with Eqs. (C.12) and (C.13), it is straightforward to obtain:

$$G_{nm} = \frac{q_s}{D_n \cdot E_m} \times$$

$$\times\left\{\sin(\beta_n x_2) - \sin(\beta_n x_1) - \frac{B_1}{\beta_n}\left[\cos(\beta_n x_2) - \cos(\beta_n x_1)\right]\right\} \times \tag{C.35}$$

$$\times\left\{\sin(\alpha_m y_2) - \sin(\alpha_m y_1) - \frac{C_1}{\alpha_m}\left[\cos(\alpha_m y_2) - \cos(\alpha_m y_1)\right]\right\}$$

From Eqs. (C.29) and (C.30), combined with Eq. (C.34), we have:

$$\blacktriangleright \quad w_1(z) = \begin{cases} 0 & z < d_{HS} \\ \dfrac{G_{nm}}{\gamma_{nm}k}\sinh\left(\gamma_{nm}d_{HS}\right) & z \geq d_{HS} \end{cases} \quad (C.36)$$

$$\blacktriangleright \quad w_2(z) = \begin{cases} 0 & z < d_{HS} \\ -\dfrac{G_{nm}}{\gamma_{nm}k}\cosh\left(\gamma_{nm}d_{HS}\right) & z \geq d_{HS} \end{cases} \quad (C.37)$$

Substituting Eqs. (C.36) and (C.37) into Eqs. (C.28) and (C.32), we have:

$$\blacktriangleright \quad u(z) = \begin{cases} 0 & z < d_{HS} \\ \dfrac{G_{nm}}{\gamma_{nm}k}\sinh\left[\gamma_{nm}\left(d_{HS}-z\right)\right] & z \geq d_{HS} \end{cases} \quad (C.38)$$

$$\blacktriangleright \quad A_{nm} = \frac{G_{nm}}{\gamma_{nm}k}\frac{\cosh\left[\gamma_{nm}\left(d_{HS}-d_t\right)\right]}{\sinh\left(\gamma_{nm}d_t\right)} \quad (C.39)$$

Finally, we can evaluate the expression of $Z_{nm}(z)$ by substituting Eqs. (C.38) and (C.39) into Eq. (C.31).

C.2 VHS case

Assuming, also in this case, a uniform dissipation within the heat generating region, Eq. (C.22) becomes:

$$g(x,y,z) = q_v \cdot p(x)q(y)r(z) \quad (C.40)$$

where:

$$\blacktriangleright \quad p(x) = q(y) = r(z) = \begin{cases} 1 & \forall(x,y): \begin{cases} x_1 \leq x \leq x_2 \\ y_1 \leq y \leq y_2 \\ z_1 \leq z \leq z_2 \end{cases} \\ 0 & \text{elsewhere} \end{cases} \quad (C.41)$$

Substituting Eq. (C.41) into Eq. (C.24), combined with Eqs. (C.12) and (C.13), it is straightforward to obtain:

$$G_{nm} = \frac{1}{D_n \cdot E_m} \times$$

$$\times \left\{ \sin(\beta_n x_2) - \sin(\beta_n x_1) - \frac{B_1}{\beta_n} \left[\cos(\beta_n x_2) - \cos(\beta_n x_1) \right] \right\} \times \quad \text{(C.42)}$$

$$\times \left\{ \sin(\alpha_m y_2) - \sin(\alpha_m y_1) - \frac{C_1}{\alpha_m} \left[\cos(\alpha_m y_2) - \cos(\alpha_m y_1) \right] \right\}$$

Combining Eqs. (C.29) and (C.30) with Eq. (C.34), we have:

$$\blacktriangleright \quad w_1(z) = \begin{cases} 0 & z < z_1 \\ \dfrac{G_{nm}}{\gamma_{nm}^2 k} \left[\cosh(\gamma_{nm} z) - \cosh(\gamma_{nm} z_1) \right] & z_1 \le z \le z_2 \\ \dfrac{G_{nm}}{\gamma_{nm}^2 k} \left[\cosh(\gamma_{nm} z_2) - \cosh(\gamma_{nm} z_1) \right] & z > z_2 \end{cases} \quad \text{(C.43)}$$

$$\blacktriangleright \quad w_2(z) = \begin{cases} 0 & z < z_1 \\ -\dfrac{G_{nm}}{\gamma_{nm}^2 k} \left[\sinh(\gamma_{nm} z) - \sinh(\gamma_{nm} z_1) \right] & z_1 \le z \le z_2 \\ -\dfrac{G_{nm}}{\gamma_{nm}^2 k} \left[\sinh(\gamma_{nm} z_2) - \sinh(\gamma_{nm} z_1) \right] & z > z_2 \end{cases} \quad \text{(C.44)}$$

Substituting Eqs. (C.43) and (C.44) into Eqs. (C.32) and (C.28) yields:

$$\blacktriangleright \quad A_{nm} = \frac{G_{nm}}{\gamma_{nm}^2 k} \frac{\sinh\left[\gamma_{nm}(z_2 - d_t) \right] - \sinh\left[\gamma_{nm}(z_1 - d_t) \right]}{\sinh(\gamma_{nm} d_t)} \quad \text{(C.45)}$$

$$
\blacktriangleright \quad u(z) = \begin{cases} 0 & z < z_1 \\[3mm] \dfrac{G_{nm}}{\gamma_{nm}^2 k}\left\{1 - \cosh\left[\gamma_{nm}(z_1 - z)\right]\right\} & z_1 \leq z \leq z_2 \\[4mm] \dfrac{G_{nm}}{\gamma_{nm}^2 k}\left\{\begin{aligned} &\cosh\left[\gamma_{nm}(z_2 - z)\right] - \\ &-\cosh\left[\gamma_{nm}(z_1 - z)\right] \end{aligned}\right\} & z > z_2 \end{cases} \quad \text{(C.46)}
$$

Finally, we can evaluate the expression of $Z_{nm}(z)$ in the VHS case by substituting Eqs. (C.45) and (C.46) into Eq. (C.31).

References

[1]   Beck JV, Cole KD, Haji-Sheikh A, Litkouhi B. Heat conduction using Green's functions. London: Hemisphere Publishing Corporation; 1992.

Appendix D

The steady-state analytical solution of the heat flow equation: CASE 3

In this Appendix, the steady-state analytical solution of the heat flow equation in the domain with convective boundary conditions at lateral faces, adiabatic top surface and bottom surface adiabatic except for elementary rectangle R, that is characterized by a uniform heat flux, is derived via conventional procedures [1].

The problem to be analyzed is shown in Fig. D.1.
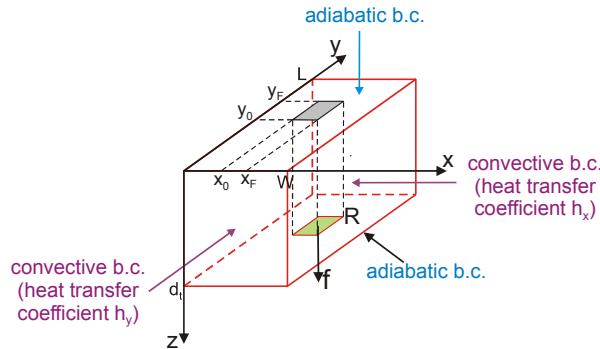

Fig. D.1. Domain under analysis. The boundary conditions are evidenced.

The substrate is assumed to be a rectangular parallelepiped defined by:

$$0 \leq x \leq W \quad 0 \leq y \leq L \quad 0 \leq z \leq d_t \qquad \text{(D.1)}$$

As can be seen in Fig. D.1, no heat is generated within the domain and the boundary conditions are of 3rd kind [Eq. (A.21)] at all lateral surfaces $(x = 0, W$ and $y = 0, L)$, of 2nd kind [Eq. (A.20)] at $z = 0$, while the bottom surface $(z = d_t)$ is adiabatic (b.c. of 2nd kind) everywhere except for rectangle R, characterized by a uniform outward heat flux:

$$\pm k \left.\frac{\partial T(\vec{r})}{\partial x}\right|_{\substack{x=W \\ x=0}} + h_{xi} \left. T(\vec{r})\right|_{\substack{x=W \\ x=0}} = h_{xi} T_{AMB} \qquad\qquad i = W,0 \qquad (D.2)$$

$$\pm k \left.\frac{\partial T(\vec{r})}{\partial y}\right|_{\substack{y=L \\ y=0}} + h_{yj} \left. T(\vec{r})\right|_{\substack{y=L \\ y=0}} = h_{yj} T_{AMB} \qquad\qquad j = L,0 \qquad (D.3)$$

$$\left.\frac{\partial T(\vec{r})}{\partial z}\right|_{z=0} = 0 \qquad\qquad\qquad\qquad (D.4)$$

$$-k \left.\frac{\partial T(\vec{r})}{\partial z}\right|_{z=d_t} = \begin{cases} f & \forall (x,y): \begin{bmatrix} x_0 \le x \le x_F \\ y_0 \le y \le y_F \end{bmatrix} \\ 0 & \text{elsewhere} \end{cases} \qquad (D.5)$$

If we consider:

$$\mathcal{G}(\vec{r}) = T(\vec{r}) - T_{AMB} \qquad\qquad\qquad\qquad (D.6)$$

Eq. (A.14) reduces to:

$$\nabla^2 \mathcal{G}(\vec{r}) = 0 \qquad\qquad\qquad\qquad (D.7)$$

and Eqs. (D.2)-(D.5) become:

$$\pm k \left.\frac{\partial \mathcal{G}(\vec{r})}{\partial x}\right|_{\substack{x=W \\ x=0}} + h_{xi} \left. \mathcal{G}(\vec{r})\right|_{\substack{x=W \\ x=0}} = 0 \qquad\qquad i = W,0 \qquad (D.8)$$

$$\pm k \left.\frac{\partial \mathcal{G}(\vec{r})}{\partial y}\right|_{\substack{y=L \\ y=0}} + h_{yj} \left. \mathcal{G}(\vec{r})\right|_{\substack{y=L \\ y=0}} = 0 \qquad\qquad j = L,0 \qquad (D.9)$$

$$\left.\frac{\partial \mathcal{G}(\vec{r})}{\partial z}\right|_{z=0} = 0 \qquad\qquad\qquad\qquad (D.10)$$

$$-k \left.\frac{\partial \mathcal{G}(\vec{r})}{\partial z}\right|_{z=d_t} = \begin{cases} f & \forall (x,y): \begin{bmatrix} x_0 \le x \le x_F \\ y_0 \le y \le y_F \end{bmatrix} \\ 0 & \text{elsewhere} \end{cases} \qquad (D.11)$$

Analogously to the treatments reported in the previous Appendixes, we assume that $\vartheta(\vec{r})$ can be expressed as a product of a function of x, a function of y, and a function of z:

$$\vartheta(\vec{r}) = X(x)Y(y)Z(z) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} X_n(x)Y_m(y)Z_{nm}(z) \qquad (D.12)$$

where $X_n(x)$ and $Y_m(y)$ are solutions of one-dimensional problems (B.19) and (B.20).

Therefore (see Appendix B), we have:

➢ $\quad X_n(x) = \dfrac{\beta_n \cos(\beta_n x) + B_1 \sin(\beta_n x)}{D_n}$ \qquad\qquad (D.13)

➢ $\quad Y_m(y) = \dfrac{\alpha_m \cos(\alpha_n y) + C_1 \sin(\alpha_m y)}{E_m}$ \qquad\qquad (D.14)

where:

✓ $\quad B_1 = h_{x0}/k$ \qquad\qquad\qquad\qquad\qquad\qquad (D.15)

✓ $\quad B_2 = h_{xW}/k$ \qquad\qquad\qquad\qquad\qquad\qquad (D.16)

✓ $\quad \beta_n$ are the positive eigenvalues of:

$$\tan(\beta_n \cdot W) = \frac{\beta_n(B_1 + B_2)}{\beta_n^2 - B_1 B_2} \qquad\qquad (D.17)$$

✓ $\quad D_n = \left[\dfrac{\beta_n^2 + B_1^2}{2} \cdot \left(W + \dfrac{B_2}{\beta_n^2 + B_2^2} \right) + \dfrac{B_1}{2} \right]^{1/2}$ \qquad (D.18)

✓ $\quad C_1 = h_{y0}/k$ \qquad\qquad\qquad\qquad\qquad\qquad (D.19)

✓ $\quad C_2 = h_{yL}/k$ \qquad\qquad\qquad\qquad\qquad\qquad (D.20)

✓ $\quad \alpha_m$ are the positive eigenvalues of:

$$\tan(\alpha_m \cdot L) = \frac{\alpha_m(C_1 + C_2)}{\alpha_m^2 - C_1 C_2} \qquad\qquad (D.21)$$

✓ $\quad E_m = \left[\dfrac{\alpha_m^2 + C_1^2}{2} \cdot \left(L + \dfrac{C_2}{\alpha_m^2 + C_2^2} \right) + \dfrac{C_1}{2} \right]^{1/2}$ \qquad (D.22)

Substituting Eq. (D.12) into Eq. (D.7), and recalling Eqs. (B.46) and (B.47), we have:

$$\nabla^2 \vartheta(\vec{r}) = 0 \quad \Rightarrow \quad \nabla^2 \left[\sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) Z_{nm}(z) \right] = 0 \quad \Rightarrow$$

$$\Rightarrow \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \ddot{X}_n(x) Y_m(y) Z_{nm}(z) + \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) \ddot{Y}_m(y) Z_{nm}(z) +$$

$$+ \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) \ddot{Z}_{nm}(z) = 0 \quad \Rightarrow$$

$$\Rightarrow - \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \left(\beta_n^2 + \alpha_m^2 \right) X_n(x) Y_m(y) Z_{nm}(z) +$$

$$+ \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) \ddot{Z}_{nm}(z) = 0 \quad \Rightarrow$$

$$\Rightarrow \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) \left[-\left(\beta_n^2 + \alpha_m^2 \right) Z_{nm}(z) + \ddot{Z}_{nm}(z) \right] = 0 \quad \Rightarrow$$

$$\Rightarrow \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} X_n(x) Y_m(y) \left[-\gamma_{nm}^2 Z_{nm}(z) + \ddot{Z}_{nm}(z) \right] = 0 \quad \Rightarrow$$

$$\Rightarrow \ddot{Z}_{nm}(z) - \gamma_{nm}^2 Z_{nm}(z) = 0 \tag{D.23}$$

where we defined

$$\gamma_{nm}^2 = \beta_n^2 + \alpha_m^2 \tag{D.24}$$

A general solution of Eq. (D.23) is:

$$Z_{nm}(z) = w_{nm} \cosh(\gamma_{nm} z) + d_{nm} \sinh(\gamma_{nm} z) \tag{D.25}$$

From Eq. (D.10) combined with Eq. (D.25), one obtains:

$$\frac{dZ_{nm}(z)}{dz} \bigg|_{z=0} = 0 \quad \Rightarrow$$

$$\Rightarrow w_{nm} \gamma_{nm} \sinh(\gamma_{nm} z) \big|_{z=0} + d_{nm} \gamma_{nm} \cosh(\gamma_{nm} z) \big|_{z=0} = 0 \quad \Rightarrow$$

$$\Rightarrow d_{nm} \gamma_{nm} = 0 \quad \Rightarrow \quad d_{nm} = 0 \tag{D.26}$$

so that Eq. (D.25) becomes:

$$Z_{nm}(z) = w_{nm} \cosh(\gamma_{nm} z) \tag{D.27}$$

where coefficients w_{nm} can be evaluated so as to satisfy the boundary condition (D.11).

Let us define the function $F(x,y)$ as:

$$F(x,y) = \left.\frac{\partial \vartheta(\vec{r})}{\partial z}\right|_{z=d_t} = \begin{cases} -f/k & \forall (x,y): \begin{bmatrix} x_0 \leq x \leq x_F \\ y_0 \leq y \leq y_F \end{bmatrix} \\ 0 & \text{elsewhere} \end{cases} \quad (D.28)$$

and assume that $F(x,y)$ can be expressed as a linear combination, by means of suitable coefficients F_{nm}, of the products of eigenfunctions $X_n(x)Y_m(y)$:

$$F(x,y) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} F_{nm} X_n(x) Y_m(y) \quad (D.29)$$

where coefficients F_{nm} are to be evaluated.

Multiplying Eq. (D.29) by $X_i(x)Y_j(y)$ and integrating in x and y over $[0, W]$ and $[0, L]$, respectively, we have:

$$\int_0^W \int_0^L X_i(x) Y_j(y) F(x,y) \, dx \, dy = F_{ij} \quad (D.30)$$

where we accounted for the orthonormality of $X_n(x)$ and $Y_m(y)$.

Substituting Eq. (D.28) into Eq.(D.30):

$$F_{ij} = -\frac{f}{k} \int_{x_0}^{x_F} \int_{y_0}^{y_F} X_i(x) Y_j(y) \, dx \, dy = -\frac{f}{k} \int_{x_0}^{x_F} X_i(x) \, dx \int_{y_0}^{y_F} Y_j(y) \, dy$$

which can be rewritten in the form:

$$F_{nm} = -\frac{f}{k} \int_0^{x_F} X_n(x) \, dx \int_0^{y_F} Y_m(y) \, dy \quad (D.31)$$

Substituting Eqs. (D.13) and (D.14) into Eq. (D.31) yields:

$$F_{nm} = -\frac{f}{k \cdot D_n \cdot E_m} \times$$

$$\times \left\{ \sin\left(\beta_n x_F\right) - \sin\left(\beta_n x_0\right) - \frac{B_1}{\beta_n}\left[\cos\left(\beta_n x_F\right) - \cos\left(\beta_n x_0\right)\right] \right\} \times \quad \text{(D.32)}$$

$$\times \left\{ \sin\left(\alpha_m y_F\right) - \sin\left(\alpha_m y_0\right) - \frac{C_1}{\alpha_m}\left[\cos\left(\alpha_m y_F\right) - \cos\left(\alpha_m y_0\right)\right] \right\}$$

Therefore the function $F\left(x,y\right) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} F_{nm} X_n\left(x\right) Y_m\left(y\right)$ is totally known.

Substituting Eqs. (D.29) and (D.12) combined with Eqs. (D.32) and (D.27) into Eq.(D.28), we have:

$$F\left(x,y\right) = \left.\frac{\partial \vartheta\left(\vec{r}\right)}{\partial z}\right|_{z=d_t} \quad \Rightarrow$$

$$\Rightarrow \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} F_{nm} X_n\left(x\right) Y_m\left(y\right) = \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} X_n\left(x\right) Y_m\left(y\right) \left.\frac{dZ_{nm}\left(z\right)}{dz}\right|_{z=d_t} \quad \Rightarrow$$

$$\Rightarrow F_{nm} = w_{nm}\gamma_{nm} \sinh\left(\gamma_{nm}d_t\right) \quad \Rightarrow$$

$$\Rightarrow w_{nm} = \frac{F_{nm}}{\gamma_{nm} \sinh\left(\gamma_{nm}d_t\right)} \quad \text{(D.33)}$$

Finally, substituting Eq. (D.33) into Eq. (D.27), the expression of functions $Z_{nm}(z)$ can be evaluated:

$$Z_{nm}\left(z\right) = \frac{F_{nm}}{\gamma_{nm} \sinh\left(\gamma_{nm}d_t\right)} \cosh\left(\gamma_{nm}z\right) \quad \text{(D.34)}$$

where F_{nm} are given by Eq. (D.32).

References

[1]   Beck JV, Cole KD, Haji-Sheikh A, Litkouhi B. Heat conduction using Green's functions. London: Hemisphere Publishing Corporation; 1992.

Appendix E

The steady-state analytical solution of the heat flow equation: CASE 4

In this Appendix, the steady-state analytical solution of the heat flow equation in a laterally infinite domain with isothermal bottom surface at ambient temperature and top surface adiabatic everywhere except for elementary rectangle R, where a uniform inward flux is assumed, is derived through the effective approach adopted in e.g., [1]-[3].

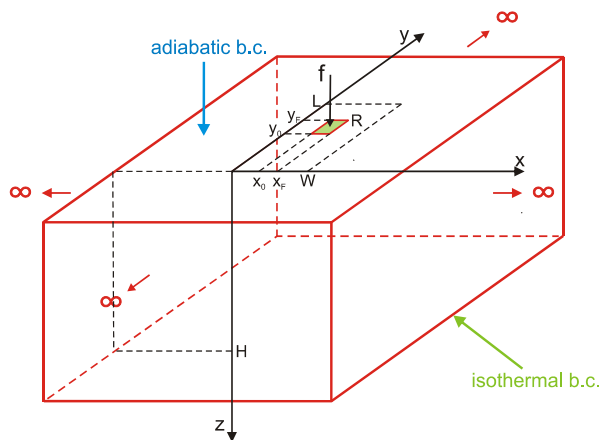The problem to be analyzed is shown in Fig. E.1.

Fig. E.1. Domain under analysis. The boundary conditions are marked.

First, the simplified problem of an infinite homogeneous medium with a THS coinciding with the elementary rectangle R and dissipating a power density equal to f is considered (Fig. E.2). Therefore, at this step we do not account for the boundary conditions at the top and bottom surfaces.
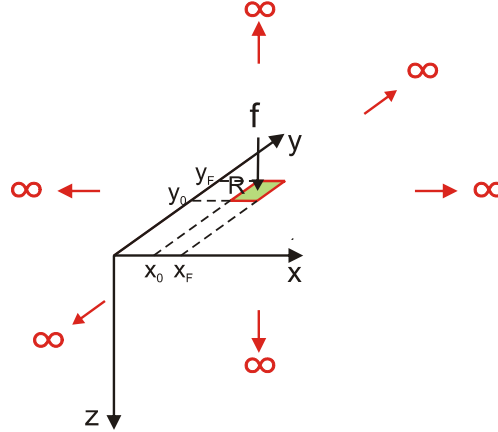
Fig. E.2. A THS in an infinite homogeneous medium.

The expression of the temperature field within this infinite domain is evaluated by integrating the contribution due to an elementary source over the rectangle R [3]:

$$\vartheta_0(x,y,z) = \frac{f}{2 \cdot \pi \cdot k} \cdot \begin{bmatrix} \psi(\delta x_F, \delta y_F, z) - \psi(\delta x_F, \delta y_0, z) - \\ -\psi(\delta x_0, \delta y_F, z) + \psi(\delta x_0, \delta y_0, z) \end{bmatrix} \quad \text{(E.1)}$$

where:

$$\psi(\delta x, \delta y, z) = -\delta z \cdot \arctan \frac{\delta x \cdot \delta y}{\delta z \cdot \sqrt{\delta x^2 + \delta y^2 + z^2}} +$$

$$+ \delta x \cdot \log\left[\delta y + \sqrt{\delta x^2 + \delta y^2 + z^2}\right] + \quad \text{(E.2)}$$

$$+ \delta y \cdot \log\left[\delta x + \sqrt{\delta x^2 + \delta y^2 + z^2}\right]$$

being $\delta x_i = x - x_i$, and $\delta y_i = y - y_i$.

Subsequently, the method of images (i.e., the adoption of vertical fictitious mirror sources) can be invoked to satisfy the adiabatic condition at the top surface (except for rectangle R, where a nonzero uniform inward flux f is present) and the isothermal condition at the bottom face. In particular, accounting for one additional source geometrically coinciding with the "real" one (i.e., rectangle R) ensures that the adiabatic condition at the upper surface is satisfied (Fig. E.3).
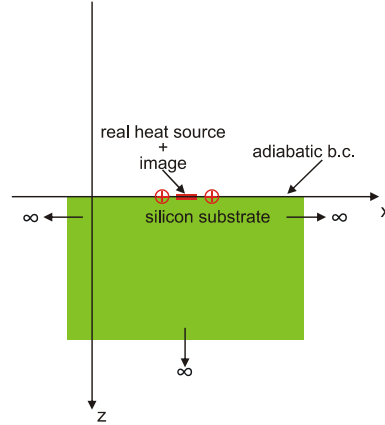
Fig. E.3. Image method: a semi-infinite space with adiabatic top surface is analyzed.

The temperature distribution generated by the superposition of the two (real and fictitious) sources in the resulting semi-infinite space is expressed in a closed form and is given by:

$$\vartheta_{20}(x,y,z) = \frac{f}{2 \cdot \pi \cdot k} \times$$
$$\times \begin{bmatrix} \psi(\delta x_F, \delta y_F, \delta z) - \psi(\delta x_F, \delta y_0, \delta z) \\ -\psi(\delta x_0, \delta y_F, \delta z) + \psi(\delta x_0, \delta y_0, \delta z) \end{bmatrix} \quad \text{(E.3)}$$

Then, if an isothermal boundary condition at the bottom surface is forced, another negative source must be added (Fig. E.4a). Finally, in order to take into account both the adiabatic boundary condition at the top surface and the isothermal one at the bottom, a series of vertical fictitious mirror sources can be added (Figs. E.4b and c) [2], [3].

The pth-order solution is given by:

$$\vartheta_{2,f}(x,y,z) = \sum_{v=1}^{p} \begin{bmatrix} (-1)^{v-1} \cdot \vartheta_{20}(x,y,z+2\cdot(v-1)\cdot H) \\ +(-1)^{v} \cdot \vartheta_{20}(x,y,z-2\cdot v\cdot H) \end{bmatrix} \quad \text{(E.4)}$$
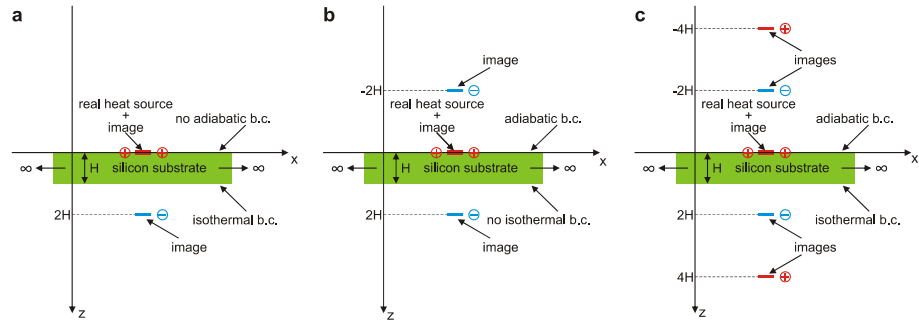
being H the thickness of domain.

Fig. E.4. Image method. (a) Two image sources: the isothermal b.c. at bottom surface is satisfied. (b) Three image sources: the adiabatic b.c. at top surface is satisfied. (c) *N* image sources: both the adiabatic and isothermal b.c. are satisfied at top and bottom surfaces, respectively.

References

[1]   Smith D, Fraser A, and O'Neil J. Measurement and prediction of operating temperatures for GaAs ICs. IEEE Semi-Therm Symp Proc 1986:1-20.

[2]   Leturcq P, Dorkel JM, Napieralski A, Lachiver E. A new approach to thermal analysis of power devices. IEEE Trans Electron Dev 1987; 34(5):1147-1156.

[3]   Rinaldi N. Thermal analysis of solid-state devices and circuits: an analytical approach. Solid-State Electron 2000;44(10):1789-98.

Appendix F

The Kirchhoff transform

In semiconductor materials (e.g., Si) the thermal conductivity k is dependent on temperature. In order to account for this effect, that makes the heat flow equation nonlinear [see Eq. (A.10)], the so-called *Kirchhoff Transform* [1]-[3] can be effectively invoked.

By means of this approach, the heat flow problem can be linearized and the actual temperature rises can be easily related with the ones evaluated by considering a temperature-insensitive thermal conductivity.

Let us define the *linearized temperature*:

$$U(T) = \int_{T_0}^{T} \frac{k(\tau)}{k_0} d\tau \qquad\qquad (F.5)$$

where $k_0 = k(T_0)$ and T_0 is a reference temperature.

As we will see, U is called *linearized temperature* because it is the solution of the linear differential equation of the heat flow [Eq. (A.11)].

From Eq. (F.5) we have:

$$\nabla U = \frac{dU}{dT} \nabla T = \frac{k(T)}{k_0} \nabla T \quad \Rightarrow \quad \nabla T = \frac{k_0}{k(T)} \nabla U \qquad (F.6)$$

Substituting Eq. (F.6) into the nonlinear term $\nabla \cdot \left[k(T) \cdot \nabla T \right]$ yields:

$$\nabla \cdot \left[k(T) \cdot \nabla T \right] = k_0 \nabla^2 U \qquad\qquad (F.7)$$

so that the linearized temperature U can be regarded as the solution of the linear heat equation in the ideal case of a thermal conductivity independent of temperature and equal to its actual value k_0 at the reference temperature T_0.

Let us see now, how we can relate the linearized temperature U to the actual one T.

The temperature-dependence of thermal conductivity is often expressed as:

$$k(T) = k(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{F.8}$$

For silicon, by assuming $T_0 = 300$ K, we can consider $k(T_0)=1.4\times10^{-4}$ W/μm K, and $m = 4/3$.

Substituting Eq. (F.8) into Eq. (F.5), we obtain:

$$U(T) = \int_{T_0}^{T}\left(\frac{\tau}{T_0}\right)^{-m} d\tau = \frac{T_0^{\,m}}{1-m}\left[\tau^{1-m}\right]_{T_0}^{T} = \frac{T_0^{\,m}}{1-m}\left[T^{1-m}-T_0^{\,1-m}\right] =$$
$$= \frac{T_0}{m-1}\left[1-\left(\frac{T}{T_0}\right)^{1-m}\right] \tag{F.9}$$

Eq. (F.9) allows evaluating the actual temperature T from the linearized temperature U:

$$T = T_0\left[1-\frac{(m-1)}{T_0}U\right]^{\frac{1}{1-m}} \tag{F.10}$$

References

[1]   Burghartz JN, McIntosh RC, Stanis CL. A low-capacitance bipolar/BiCMOS isolation technology, Part I - Concept, fabrication process and characterization. IEEE Trans Electron Dev 1994;42(8):1379-87.

[2]   Ganci PR, Hajjar J-JJ., Clark T, Humphries P, Lapham J, Buss D. Selfheating in high-performance bipolar transistors fabricated on SOI substrates. IEEE IEDM Proc 1992:417-20.

[3]   Gray PR, Meyer RG. Analysis and design of analog integrated circuits. New York: Wiley; 3rd edition, 1993.