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FABRICATION AND CHARACTERIZATION OF ADVANCED ORGANIC THIN FILM TRANSISTORS

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Introduction

In recent years, organic electronics is receiving a great attention from both academic and industrial research due to the serious improvement in the performances of organic materials when used in Organic Thin Film Transistors (OTFTs), in Organic Light Emitting Diodes (OLED), in solar cells, etc. On the other hand, the development of *Post Silicon Technologies* based on organic materials addresses to a new era of devices and applications thanks to unusual properties such as flexibility, light weight, and disposability. Accordingly in the last decades [1] much effort has been dedicated to the improvement of materials properties and devices processing. Organic materials have been tailored to obtain appropriate features for electronic applications, as for example improved lifetime, environmental stability, solution processability, and reasonable charge mobility. The possibility to modify both the composition and material preparation is the strongest issue of the *Post Silicon Technologies*. Moreover, innovative processing techniques have been developed to deposit and pattern organic materials without compromising their properties.

The key component of the organic electronic is the Organic Thin Film Transistor (OTFT) that is a Field Effect Transistor (FET) usually based on organic semiconductors and on organic dielectrics. OTFTs can be assembled on plastic substrates at room temperatures, becoming potentially inexpensive for manufacturing and mechanically flexible, and promising low-cost and large area electronics applications.

Nevertheless, lots of properties are yet unexplored or should be more deeply understood, so that different aspects need to be improved. In particular, the low mobility of organic semiconductors does not allow their use in electronic applications where fast response (ns) speed and low size (nm) are required. In this field, Silicon technology is still having, and it will continue to have a prominent role. On the other hand, different merging application fields could be identified where low cost devices are required and slow responses are accepted: for example smart tag, displays,

photovoltaics, radio-frequency identification (RFID) circuitry, and chemical sensors. Within this framework, this thesis demonstrates the possibility to manufacture transistors and more complex circuits with innovative polymers and technologies, leading to an experimental validation of the possibility to realize all-organic devices.
The proposed work has been fully integrated within an industrial project aiming to the development of an *All Organic Technological Platform*, involving organic memories, transistors, resistors, capacitors and logic devices for realising a cheap and disposable 4-bit microprocessor.

Thesis outline

The thesis has been organized in five chapters: the first two contain the basic aspects concerning the working principles of OTFTs, while the other three describe the experimental work. In particular, Chapter 1 gives an overview of the OTFT operation and the basic properties related to the charge transport in organic semiconductor. The role of the interfaces is carefully analysed. Chapter 2 reports on the properties, taken from literature, of organic materials to be potentially used in OTFTs and on the main parameters usually considered in device analysis (mobility, threshold voltage, On/Off ratio). Chapter 3 presents the experimental results obtained on hybrid OTFT structures with an organic semiconductor deposited directly on silicon templates; this analysis allowed first screening on possible organic semiconductors to be used for advanced electronics.
Chapter 4 reports on the details of a manufacturing process developed for the realization of all devices on glass substrates. The use of innovative technologies, such as Inkjet Printing for devices improvement is also described. Moreover, the electrical properties of realized OTFTs and Inverter prototypes are also outlined.
Finally, Chapter 5 describes the electrical characteristics of devices realized on plastic substrates up to the first demonstration of an organic Inverter prototype, together with a quite preliminary description of “what next” in terms of more complex circuits (Full Adder, Multiplexer, etc.).

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Chapter 1
Organic Thin Film Transistors

Since their discovery [1], transistors have dominated microelectronics industry as fundamental building blocks for basic analytical circuits. A transistor is a semiconductor device commonly used as an amplifier or an electrically controlled switch. An Organic Thin Film Transistor (OTFT) is a transistor based on organic semiconductors as active material. The interest in organic semiconductors originates from the demonstration of field-effect conduction in small organic molecules [1] and conjugated polymers [3]. From the first Organic Field Effect Transistor (OFET) reported by Tsumara in 1986 [4] a huge improvement in materials performances and development of new fabrication techniques took place [5]. Recently, all Organic TFTs became technologically attractive due to the possibility to be realized by low temperature and low cost manufacturing, on large area and flexible substrates [6]. These properties allow identifying their possible use in innovative fields, such as in electronic paper or in flexible displays [7], in sensors [8], and in low-cost radiofrequency identification cards (RFIDs) [9].

The performances of OTFTs are still lower than the Silicon devices, due to different limits, but the increasing of the charge carrier's mobility of semiconductor could represent an important step to obtain more efficient OTFTs. In the last decade, more interesting results were obtained, in particular, hole mobilities of the order of 1 cm^2/Vs were detected on devices with small molecules [10] and 0.1 cm^2 /Vs with

conjugated polymers [11]. However, the highest mobility in organic semiconductors are observed in crystalline materials: hole mobility up to 20 cm^2/Vs was observed in rubrene [12]. Since the need of high mobility materials, materials scouting, for p and n-channel transistors, continue to be a major area of research. Other important requirements are the stability under ambient conditions and bias stress, device reproducibility and easy processing. To this aim both scientific community and private investors focus on the synthesis of new materials able to achieve better and better performances so that they can be marketable. Though many advances have been already achieved, a better control of the performances must be still achieved for any realistic applications of organic electronics.

1.1 OTFT: Device description

An OTFT device is constituted by three electrodes (Source, Drain and Gate), an organic semiconductor (OS) as active layer, and an insulating layer. As for MOSFETs, the Source terminal allows to inject carriers, the Drain to extract carriers, and the Gate to control the conductivity of the Source-to-Drain channel.

Device operation

OTFT is a three-terminal device, in which a voltage applied to a gate electrode controls the current flow between the source and drain electrodes via an imposed bias. A basic scheme is shown in Figure 1.1 where Vg and Vds are the applied gate and source-drain voltages, respectively.
Basically, the thin film transistor operates like a capacitor. When a voltage is applied between Source and Gate, a charge is induced at the insulator-semiconductor interface. This charge forms a conducting channel whose conductance is directly related to Vg.

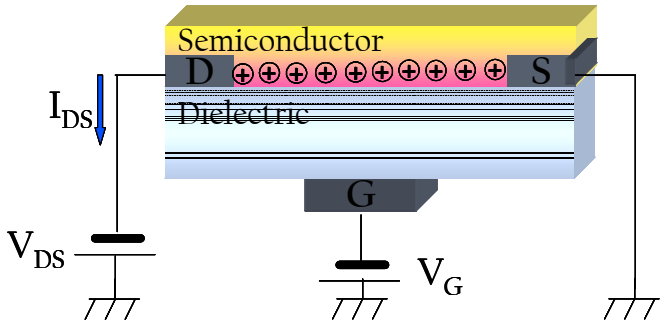

Figure 1.1 Schematic view of Bottom-Gate Bottom Contacts thin film transistor**.**

At low drain voltages, the current increases linearly with drain voltage, according to the Ohm's law. When the drain voltage approaches the gate voltage, the voltage drop at the drain contact falls to zero, and the conducting channel is pinched off. This corresponds to the so-called *saturation regime*, and the current becomes independent of the drain voltage. The operating mode of the organic-thin film transistor produce two typical current-voltage characteristics as shown in Figure 1.2 a and b.

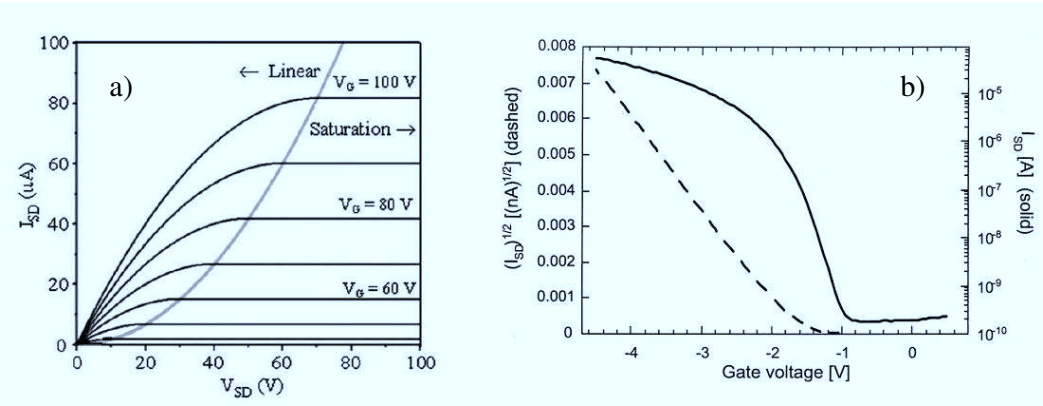

Figure 1.2 Typical electrical characteristics obtained in a field effect transistor: (a) Output, the boundary between linear and saturation regime is indicated by a grey curve, and (b) Saturated transfer characteristic in different representation.

Organic FETs work in the *accumulation mode* differently from the inorganic devices that operate in the *inversion mode*. The conduction mainly occurs, in the on-state, due to the layer of charge carriers which forms in the semiconductor within few angstroms

from the insulator/semiconductor interface, and after the application of a suitable Vg. These charges are of the same type of the majority charge carriers responsible of the current in the off state. A small fraction of the total drain current is therefore determined by the free carriers in the semiconductor, which can be thermally generated or produced by unintentional doping. Despite this fundamental difference, the characteristic equations of the inorganic MOSFET transistors [13] can be applied, as a first approximation, also to an Organic FET, that is

$$I_{DS} = \frac{1}{2}\mu C_i\left(\frac{W}{L}\right)\left[2\left(V_G - V_T\right)V_{DS} - V_{DS}^2\right] \tag{1.1}$$

in the linear zone, where $V_{DS} < \left(V_{GS} - V_T\right)$ and

$$I_{DS} = \frac{1}{2}\mu C_i\left(\frac{W}{L}\right)\left[\left(V_G - V_T\right)^2\right] \tag{1.2}$$

in the saturation zone, where $V_{DS} \geq \left(V_{GS} - V_T\right)$.

Here, L is the channel length of the transistor from source to drain in the direction of the current flow, W is the channel width of the transistor, C_i is the capacitance per unit area of the insulating layer, and μ is the field effect mobility.

The nature and quality of the organic semiconductor is crucial for achieving high OFET performances, which are mainly determined by the charge carrier mobility (e.g. μ) that represents a measure of the charge carrier drift velocity per unit of electric field. The mobility μ is also directly related to the switching time of the device. Other important parameters are the On/Off ratio, which is the ratio between the current in the accumulation mode and the current in the depletion mode, and the threshold voltage (V_T), that is the gate voltage corresponding to the opening of the conduction channel [14]. The On/Off ratio is indicative of the switching performance of OTFTs, ratios as high as 10^6, suitable for most applications, can be reached by current generation OTFTs [15].

1.2 Charge Transport Mechanisms in organic semiconductors

The electrical performances of OTFT are dramatically affected by the chemical properties and the charge transport mechanisms of organic semiconductors. The organic semiconductor can be a highly conjugated small molecule or polymer. Differently from inorganic materials, through organics current flows by majority carriers, so that OTFTs cannot work in inversion regime as MOSFETs. This fundamental difference is related to the nature of the charge transport in these semiconductors. In well-ordered inorganics, such as single-crystal Si, the delocalization of electrons over equivalent sites leads to a band-type mode of transport, with charge carriers moving through a continuum of energy levels in the solid. In organic materials, hopping between discrete, localized states of individual molecules [16] is mostly indicated as the conduction mechanism. .

Highly conjugated organic materials have the potential to work as semiconductors because of their strong π orbital overlap. In fact, in organic conjugated solids, the carbon atom in double bond has the configuration of sp^2-$2p_z$. The intra-molecular interactions between two carbon atoms lead to the overlapping of sp^2 orbitals that form the σ bond, while the two p_z orbitals form a bonding and anti-bonding molecular π orbitals. The overlapping of the energy levels of all the atoms leads to an energy diagram of organic solid that allows defining a Highest Occupied Molecular Orbital (HOMO) and a Lowest Unoccupied Molecular Orbital (LUMO) separated by an energy gap. Accordingly, when an electron is added or a hole is injected, the resultant charge becomes delocalized across the conjugated system, and it acts as a carrier for current through the molecule.

An effective organic semiconductor must have a redox potential that allows charge injection by a small applied voltage. In other words, the HOMO for hole injection or the LUMO for electron injection must be energetically accessible. On the other hand, the orbitals should not be so easily accessible so that the conduction in the semiconductor can be effectively turned off. One of the more important factors for FET application is the capacity of the organic materials to form a continuous thin film

that, when turned on, allows charge to move through quickly enough as requested by electronic applications.

Organic thin films are amorphous or crystalline collections of molecules interacting through weak Van der Waals forces. Charge carriers move via hopping between localized molecular π orbital (slow process), so that charge transport is relatively easy within a molecule, but due to the disordered molecular structure of the most organic semiconductors, it becomes much more difficult between molecules.

A model often used to describe organic semiconductors explains transport between molecules (or more generally between localized states) as a thermally activated charge carrier tunneling (hopping). Hopping occurs between localized states that are disordered both in space and energy [17]. With the intermolecular structure more ordered, the hopping between molecules will be easier, and mobility higher [18].

1.3 Working principles of organic FETs

The operating principle of FETs based on p-type organic semiconductors can be demonstrated by the simplified energy level diagram of Figure 1.3.

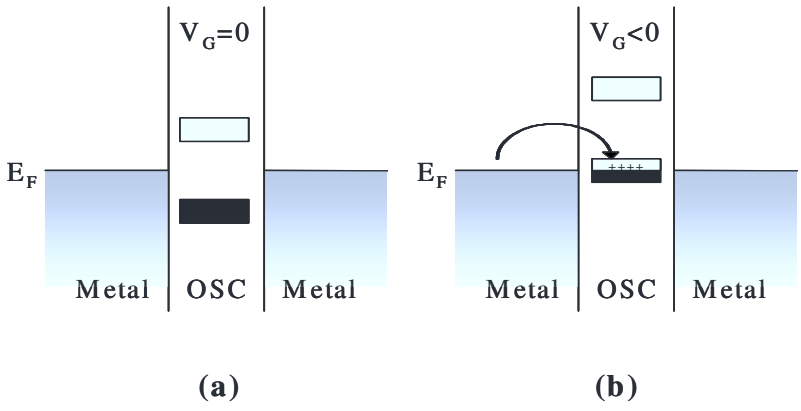

Figure 1.3 Illustration of an OFET working principle with respect to the applied Vg.

If there is no Gate voltage applied (Fig. 1.3a), the organic semiconductor, which is intrinsically undoped, will not show any current. Direct injection from the Source/Drain electrodes is the only way to create current flow in the organic

semiconductor. This current will be relatively small owing to the high resistance of the organic semiconductors and large distance between Source and Drain electrodes. When a negative (positive) gate voltage is applied (Fig.1.3 b), positive (negative) charges are induced at the organic semiconductors interface with the Gate dielectric (a p-type conducting channel is formed). If the Fermi level of the Source/Drain metal is close to the HOMO (LUMO) level of the organic semiconductor, then positive (negative) charges can be extracted by the electrodes through the application of a voltage, Vds, between the drain and source. Organic semiconductors which have the ability to conduct only positive (negative) charge carriers are named p-type (n-type) semiconductors.

In some organic semiconductors, both electrons and holes can be injected and responsible of charge transport realising ambipolar transistors. Moreover, n-type organic semiconductors are less common due to the difficulty of synthesizing materials with a large electron affinity that allows the injection of electrons from stable electrodes in air [19].

Together with the intrinsic properties of the semiconductor and electrodes, also device configuration influences its electronic properties as illustrated in the following sections.

1.4 OTFT basic structures

OTFTs are based on a multilayer structure whose properties are affected both by the characteristics of the components layers and the interface between them. Moreover, depending on the position of the electrodes with respect to the semiconductor and dielectric layer, there are three most common device structures:

bottom gate - bottom contact (Figure 1.4a), *bottom gate - top contact* (Figure 1.4b) and *top gate - bottom contact* (Figure 1.4c).

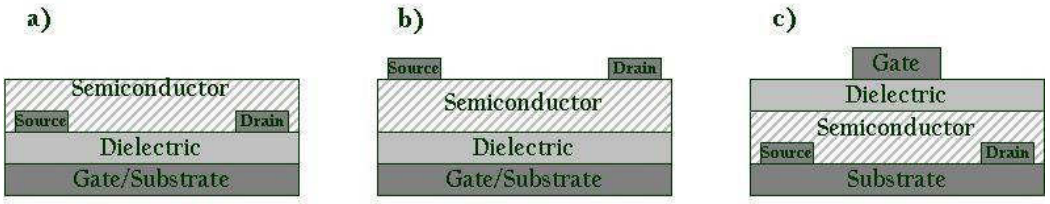

Figure 1.4 OFET configurations: (a) bottom contact - bottom gate, (b) top-contact bottom-gate, (c) bottom-contact top-gate.

We consider the *top gate-top contact* structure as mirror geometry of the BG-BC, and hence we'll not discuss it. In the following we'll sketch both advantages and limitations of each structure. In the *bottom gate - bottom contact* (BG-BC) three interfaces affect device performances: OS/contacts, contacts/dielectric and OS/dielectric. In the bottom gate - top contact configuration (BG-TC), the gate contact works also as substrate and the injection zone (contacts/OS) is well separated from the conducting zone (OS/dielectric).

In the *top gate – bottom contact* (TG-BC), two interfaces determine device performances: the OS/contacts zone and the OS/dielectric zone. In this thesis we used the BG-BC and TG-BC configurations. Then, the performance of OTFTs strongly depends on the device structure and the materials properties.

1.5 Functional interfaces

In the past, the nature of charge carrier microscopic motion in organic devices was related only to the quality and purity of the OS. In recent years, it became clear that the electrical response is not only determined by the chemical structure and the purity of the OS. The identification of the crucial role of the interfaces in determining device performances was a key discovery that promoted many fundamental studies on the interface physical properties and characteristics.

Metal/OS interface

One of the most important factors affecting the electrical properties of a device is the charge injection that in OTFT happens at OS/metal contact interface. Usually this problem is treated as a Mott-Schottky barrier [20].

The barrier is formed after the contact between the metal and the semiconductor, and physically consists of a "space charge" region that causes a voltage drop at the interface.

According to the energy diagram, there is a bending of the energetic levels of the semiconducting material at the interface, as metal creates a gap with respect to the metal work function (ϕ_m). When ϕ_m and the electronic levels of the semiconductor are energetically closer, since the injection is highly favored the contact is defined as *ohmic*. In the case of non-*ohmic* contacts, a high potential barrier is formed, thus leading to poorly efficient charge injection. Beyond the energy levels matching, other parameters play important roles: the grain boundaries which are present at the metal/semiconductor interface, the penetration of metal clusters inside the organic soft material during the metal deposition, the local oxidation and the traps presence at the interface. All these factors produce high contact resistances and device irreproducibility that cannot be explained by the simple Mott-Schottky model. Therefore, many models were proposed to complete this theory such as thermally assisted tunneling from the metal to localized states [21], tunneling into polaron levels [22], thermally assisted injection into an energetically disordered dielectric [23], or diffusion-limited thermoionic emission [24].

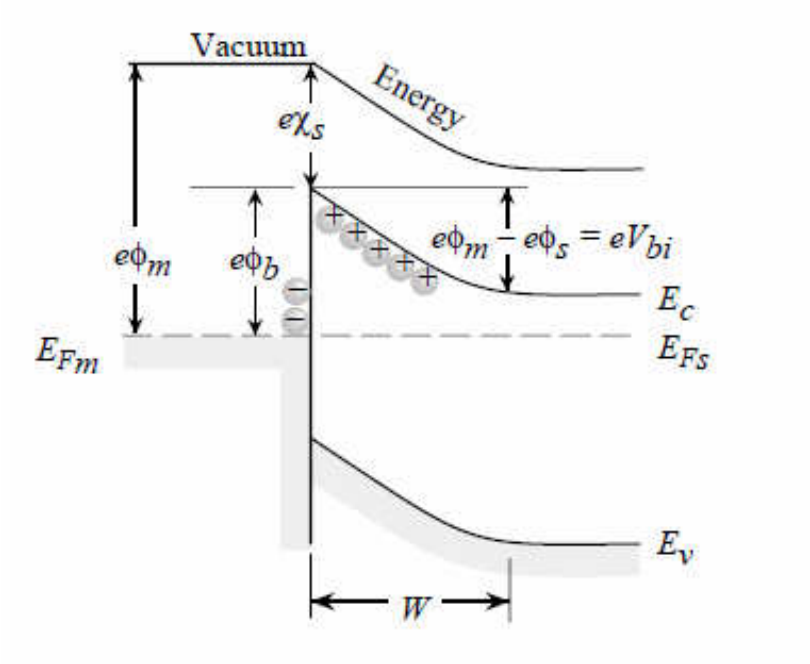

Figure 1.5 Metal-semiconductor junction at equilibrium.

Dielectric/OS interface

Field-effect conduction is well-known to occur in a narrow region of the active material, at the interface with the dielectric layers [25]. The crucial process of charge accumulation and transport takes place very close to the interface, between the gate dielectric and the semiconductor. Therefore, the interface and the dielectric properties have a crucial influence on the device characteristics.

Gate dielectrics to be used in FETs should have high dielectric break-down strength, should be environmentally stable, easily processable and compatible with the other processing steps. Beyond these obvious features, the choice of the dielectric species in OTFTs involves many other effects which can influence the carrier transport and mobility with respect to inorganic materials. First, the dielectric can affect the *morphology* and/or the *molecular organization* of the OS thin film. Second, the interface with the organic material can be rich of *traps* that are detrimental for charge transport. Finally, different dielectric species present different *dielectric constant* (ε) values that influence the OFET response.

Interfacial traps

There is an almost total lack of knowledge regarding the nature of traps and of the trapping mechanism. A typical example for electron traps are the hydroxyl groups (Si-OH), normally present on the silicon dioxide surface. Therefore, a careful control of physical and chemical characteristics of the dielectric/OS interface is crucial to improve OFET performances.
The use of surface treatments or different polymeric insulator films reducing trap density has been investigated by different research groups [26].

Polarity of the dielectric

The insulator can also change the density of states in the semiconductor by local polarization effects. Remember that transport takes place by hopping between localized states, formed by individual molecules or by a number of interacting molecules. Localization may be enhanced by local polarization effects that can distort these states. Random dipoles present at the interface with the OS can modulate the energies of localized states, leading to increased energetic disorder [27] when more polar insulators are used. In absence of disorder, states would be totally isoenergetic. The dipoles present locally are randomly oriented and the intermolecular interactions among their energy fluctuations caused the broadening of the Density Of States (DOS). The more polar the interface, the more severe the DOS broadening, thus more tail states are present. Carriers in equilibrium with temperature and field will, on average, face a higher potential barrier (higher of ΔE) for hopping into denser sites lying close, resulting therefore more localized (Figure 1.6). This is clearly detrimental for transport properties.

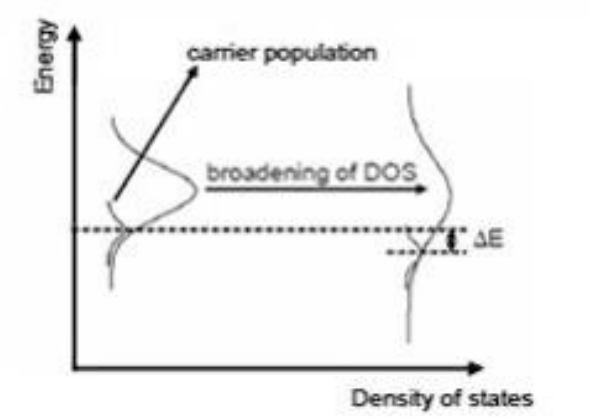

Figure 1.6 Scheme of the enhancement of carrier localization due to polar insulator interface.

1.6 Device configurations: advantages and breakthroughs

As specified before, the electrical performances of the final device were also affected by the structure configuration. Depending on the materials choice and on processing conditions each configuration has advantages and breakthroughs.

Bottom Gate-Bottom Contact

The BG-BC TFT structure is commonly used for fabricating organic TFTs since the organic semiconductor is deposited at least, without limit prior processing steps. For this reason, photolithographic patterning of gate and source/drain electrodes is possible, and the gate insulator can be deposited from a wide range of methods (e.g. plasma-enhanced chemical vapor deposition, RF magnetron sputtering).

One major disadvantage of this structure is the large contact resistance due to the very small effective area for charge injection into the channel (see red arrows in Figure 1.7). Moreover, this configuration has the disadvantage that the organic semiconductor is deposited on two different materials simultaneously (i.e., the gate dielectric and the source/drain contacts), so that the morphology of the organic thin film can be disrupted by the non-uniformity of the substrate.

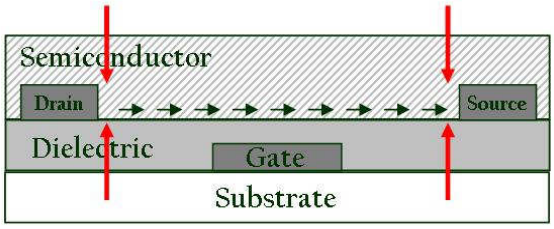

Figure 1.7 Bottom Gate Bottom Contact structure, the dark arrows indicate the current flow, while red arrow indicate the channel area in the device.

The differences in surface energy and surface roughness between the electrodes and the dielectric cause the organic film to adapt different microstructures in the two regions, resulting in regions of disorder at the source/drain contacts. As a result, BC structures typically suffer from larger source and drain contact barriers and contact resistance.

Bottom Gate Top Contact

Usually, the TC structure exhibits much better performance than the BC structure with source and drain contacts below the semiconductor layer.

The advantage of this structure is low contact resistance, due to the large effective area for injecting charge into the semiconductor channel (red arrows in Figure 1.8) and corresponds to the gate/drain and gate source overlap areas.

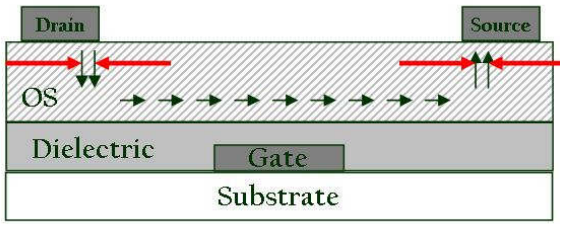

Figure 1.8 Bottom Gate Top Contact structure: red arrows indicate the channel area, black arrows show the current flow.

In this structure the induced channel occurs on the opposite side of the deposited channel material compared to where the source and drain contacts are located. Thus, the main disadvantage of this configuration is that the charges have to transport from the source to the channel through an undoped highly resistive semiconductor layer. Thus, the experimentally obtained mobility and threshold voltage of OTFTs can exhibit thickness dependence. On the other hand, since photolithographic patterning of the source and drain contacts is not possible due to solvents damage of organic layer they should be deposited on top of the organic semiconductor typically through a shadow mask, limiting lithographic resolution.

Top Gate Top Contact

The TG-TC is rarely used due to the very small effective area for charge injection into the channel that determines very large contact resistance. In this configuration, since the organic layer should be deposited before other processing steps, the gate insulator could not be compatible with physical deposition methods such as sputtering, due to the damage to the organic material caused by energetic ions during deposition.
Moreover, photolithographic patterning of the source and drain contacts is not possible. On the other hand gate insulator material can act also as an encapsulation layer protecting device from oxygen and air exposure.

Top Gate Bottom Contact

Also in the case of TG structure, the gate insulator and gate electrode can act as an encapsulation layer protecting the organic material from moisture or oxygen degradation. Nevertheless, there is a number of process integration challenges associated with this configuration. First, the gate dielectric and gate electrode have to be deposited and structured on top of the organic semiconductor layer, and this process must preserve the organic material. Secondly, vertical interconnections and vias between the conductive layers have to be built through the organic semiconductor needing the development of compatible etching process for the organic layer.

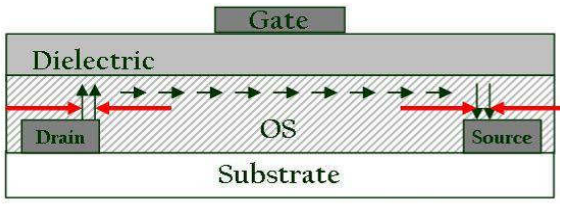

Figure 1.9 Top Gate Bottom Contact structure.

While this configuration allows that the channel forms independently from substrate-induced interactions, the roughness of the semiconductor-insulator interface in this geometry is determined by the organic thin film, and it's typically much worse than thermal SiO_2 or spun-polymer dielectrics. In addition, the subsequent deposition of the dielectric material can either damage or unintentionally dope the underlying organic semiconductor compromising the Ion/Ioff ratio. On the other hand, a fundamental advantage of this structure is represented by the low contact resistance, due to the large effective area for injecting charge into the semiconductor channel (red arrows in Figure 1.7), which corresponds to the gate/drain and gate source overlap areas.

Since photolithographic patterning of gate and source/drain electrodes is possible, the BC structure allows high-resolution and integration of OTFTs.

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Chapter 2

OTFT: Materials and Device Physics

OTFT performances are affected by materials properties and the resulting interfaces between them. As an example, organic conductors characterized by large conductivities are required for the realization of source and drain contacts; while organic semiconductors with high charge carrier mobility are needed to obtain high current values, *high-k* dielectrics materials are indicated as gate insulators to obtain low leakages, and *low-k* dielectrics are used as organic insulating materials.
Moreover, since the interface among gate dielectric and semiconductor is the active area where charge transport takes place, the presence of defects acting as traps induce a mobility decrease, and hence lower device performances. Accordingly, the control of the morphology of organic films and the processing conditions represent a critical step in OTFTs applied research. Due to the cooperation of such different factors it is essential to define a set of parameters able to quantify the OTFT performances. Their optimization should indicate the way for more efficient and stable devices. According to Chapter 1, good working OTFTs should be characterized by:

- large field effect mobility
- large on/off current ratio (I_{on}/I_{off})
- small sub-threshold slope
- threshold voltage close to zero

While the first two issues are crucial for a right device working, low sub-threshold slope and near zero threshold voltage are desirable to reduce the power consumption

of the integrated circuit. Moreover, depending on the particular application, devices could be requested to show fast operation speeds. In this Chapter, the main properties of single materials and interfaces are sketched, and their role on main working OTFT parameters is also outlined.

2.1 Materials

The complexity of interactions in multilayer structures of OTFTs, as described in the previous Chapter, suggests considering each of the constituent materials as a principal character. Each OTFT was basically composed by a substrate, an organic semiconductor a dielectric and three electrodes.

2.1.1 Substrate

TFT needs a substrate to support the structure and in organic devices it could be a glass or a plastic foil, with different advantages. The use of these materials allows a reduction of material costs and parasitic capacitances, which are unavoidable in Silicon MOSFETs, where a semiconducting substrate is used.

2.1.2 Organic Semiconductors

Up to now the most used OSs are *p-type* materials [1] due to the need of improvement in *n-type* materials performances [2]. Among *p-type* organic semiconductors, small molecules, as oligothiophenes, phthalocyanines, pentacene and tetracene (see Figure 2.1), generally present good electrical performances thanks to their high molecular order. To date, the best carrier field-effect mobility values were detected in OTFTs based on rubrene (Figure 2.1e) single crystals [3]. However, since they are almost insoluble, expensive evaporation or vacuum deposition processes are required. On the other hand, conjugated polymers, characterized by π-conjugated backbone structures with semiconducting features are well suited for the solution-processing because of their excellent film-forming characteristics.

The most studied OS polymers belong principally to three families: poly(phenylenevinylene), poly-thiopene, and poly-fluorenes; some example of polymers of these classes are shown in Figure 2.2.

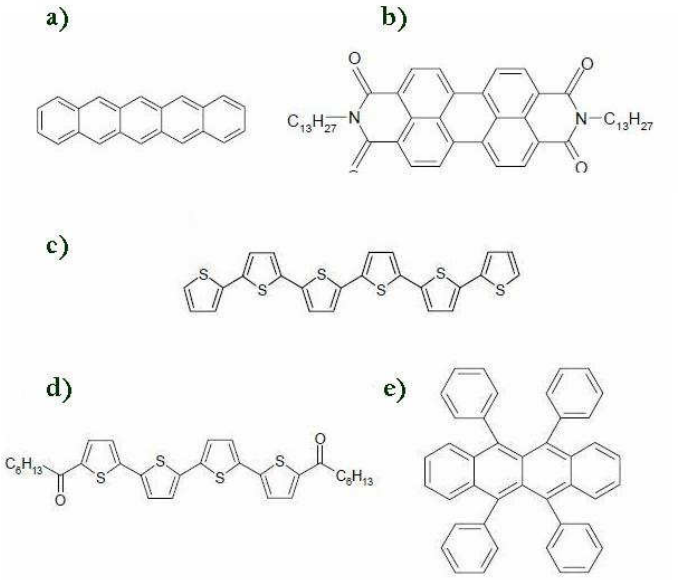

Figure 2.1 Chemical structure of a) Pentacene; b) N,N - ditrydecylperylene - 3,4,9,10 - tetracarboxylic diimmide (PTCDI-C13H27); c) α sexyl-thiophene (T6); d) α,ω-dihexylcarbonylquaterthiophene (DHCO4T); e) Rubrene.

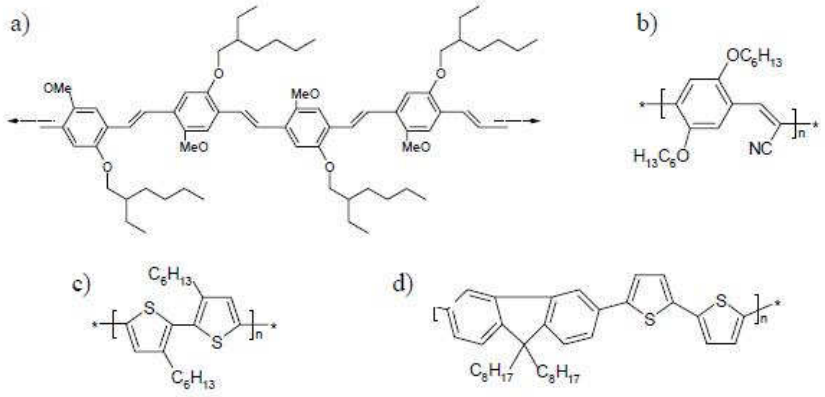

Figure 2.2 Chemical structure of polymer organic semiconductors. a) Poly[2- methoxy-5-(2-ethylhexyloxy)-1,4-phenylene-vinylene] (MEH-PPV); b) Poly[2,5,2',5'-tetrahexyloxy-7,8'- dicyano-di-*p*-phenylenevinylene] (CN-PPV); c) Poly[3-hexylthiophene] (P3HT); d) Poly[9,9'-dioctyl-fluorene*co*- bithiophene] (F8T2).

Most of these materials are soluble in common organic solvents so that can be deposited by different solution processing techniques. In contrast to vacuum techniques, solution processing does not need high deposition temperatures, and it allows the deposition on flexible low cost substrates (PET and polymides).

Nevertheless, semiconducting polymer films usually present a limited charge carrier mobility (<0.3 cm^2/V s) and poor performance stability, most likely due to the low crystallinity and the resultant high permeability of moisture and oxidizing species.

The supra-molecular organization of the semiconductor on the underlying layer (e.g. dielectric) can be a crucial factor for achieving good device performance [4]. In fact, it has been observed that field-effect mobility for P3HT is strongly dependent on the orientation of its lamellar structure with two-dimensional conjugated sheets formed by inter-chain stacking [5].

In order to improve semiconductor conduction properties controlling the morphology or the molecular organization, it needs to maximize the π–π orbital overlapping making easier the carrier hopping. In principle, this is possible by packing the organic molecules in a defined and ordered way. Furthermore, a homogeneous coverage of the substrate is required to achieve good mobility values.

There is no particular reason for the majority of polymers to be not ambipolar [6]; however, the most are *p-type*, and only a few are *n-type*. It was recently demonstrated that the principal reason for such a condition is the interaction with the substrate where they are grown [7].

2.1.3 Dielectric

Organic field effect transistors are truly interfacial devices: the region where the charge transport takes place at the OS/dielectric interface is only few nanometers thick. The interplay between dielectric and active material is complex and probably not yet completely understood.

The dielectric influences carrier transport and mobility in different ways. First, the dielectric can affect the morphology of the active layer and the orientation of small molecules or polymer segments. Transport properties are, in fact, strongly related to the molecules' orientation, because hopping conduction is determined by the length of the π-delocalization. Second, the OS/dielectric interface roughness modulates the

mobility of charge carriers. Commonly, the higher the roughness, the lower the device performances are [8].

Finally, a crucial role for the conduction is played by the value of the dielectric constant that is related to the capacitance per unit area, C_i, defined as:

$$C_i = \varepsilon_0 \frac{k}{d}$$

where k is the dielectric constant and d is the insulator thickness. Following eq.1.1, the current flowing in the semiconductor channel is proportional to C_i and to the voltage applied between drain and source. For this reason, a strategy to increase the current at low biases is to enhance the capacitance of the dielectric. High k materials allow high Ci values also if the film is enough thick to prevent *leakage currents* (currents flowing from the OS to the gate contact). Inorganic dielectric such as classic SiO_2 (low dielectric constant ε ~3.9), Al_2O_3 (ε~7), Ta_2O_5 (ε around 24), nitrides, titanates [9] were used for this aim. Unfortunately, these materials present many trap sites at the surface and therefore, not surprisingly, they lead to low transport properties. For example, the SiO_2 surface is rich in Si–OH defects that strongly influence the performances of the device. Moreover, when inorganic dielectrics are used, OFETs lose flexibility and low-cost processing. Inorganic dielectrics are usually grown by sputtering or chemical vapor deposition (CVD) more expensive than spin-coating or printing from solutions. Anyhow, considering the diffuse commercial availability of silicon dioxide, and the possible integration of the organic (or hybrid) materials in inorganic transistors, many efforts have been spent in improving performances of SiO_2 based OTFTs. In particular, good results were obtained treating the SiO_2 surface in order to reduce traps density. Surface treatments could involve self assembled monolayer (SAM) of hexamethyldisilazene (HMDS) but also octadecyltrichlorosilane (OTS) [10].

On the other hand, in the last years, solution-processable polymers have been widely used as dielectric in OFETs, partly because films with good characteristics can be obtained by spin-coating or printing, but also because they allow realizing flexible devices with good performances. Polymers having different chemical structures and physical properties are available. The films obtained have very smooth surfaces and a wide range of possible dielectric constants. Theoretically, *high k* values should be preferred, but there are literature works [11] showing that the use of *low-k* polymers with amorphous OS ensure better mobility and lower threshold voltages due to low

polar interface between the dielectric and the OS. Obviously, using *low-k* insulators the required operating voltage may be higher. Typical widely used dielectric polymers are reported in Figure 2.3.

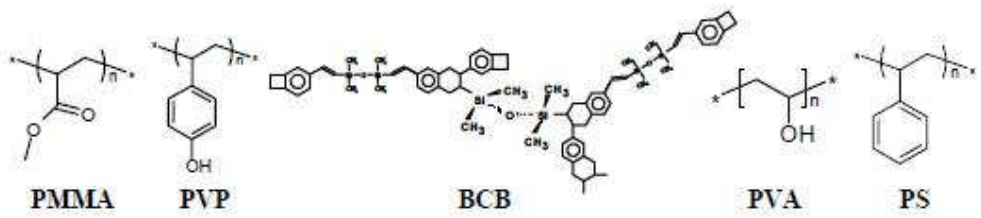

Figure 2.3 Chemical structure of dielectric polymers: PMMA (polymethylmethacrylate); PVP (polyvinylphenol); BCB (benzocyclobutene); PVA (polyvinylalcohol); PS (polystyrene).

Summarizing, the choice of the dielectric and the careful control of its characteristics in an OFET is crucial to optimize the most important device characteristics, such as: mobility, threshold voltage, current hysteresis and device to device reproducibility.

2.1.4 Electrodes

In the OTFT operation, Source and Drain electrodes have an injecting role, while the Gate should control the current flow. Gate electrode can be a metal or a conducting polymer, but also doped Silicon in some cases was employed.
Source and Drain electrodes are very important for device operation since to ensure efficient current injection their work functions should match very well with HOMO and LUMO levels of the OS. In fact, when non-ohmic contacts were present at the interface electrode/OS due to the presence of a potential barrier, there is a big contact resistance, Rc, and a substantial voltage drop at the contacts. In this case, suitable self-assembled monolayers dipoles could be introduced at the interface to enhance charge injection and metal adhesion to the organic material. Usually Source and Drain electrodes are high work function metals, such as Platinum and Au, for p-channel OTFTs. Moreover, also conducting polymers such as Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) and Polyaniline (PANI) may be used.

2.2 Physical parameters

The extraction of key parameters of OTFT operation is a high debated point. In most cases the basic equations (Eq. 1.1 and 1.2) of standard MOSFET describe quite well the experimental Transfer and Output Current-Voltage curves, but there are many doubts about their validity for organic TFT. These equations, in fact, cannot take into account bias dependence of mobility evidenced by experimental results and the presence of contact resistance, so that there is not yet an accepted method for parameter extraction even if an IEEE Standard for OTFT Characterization has been released [12]. Based on this standard, to completely characterize OTFTs, it needs to define the mobility value, the threshold voltage, the I_{on}/I_{off} ratio and the contact resistance as outlined in Figure 2.4.

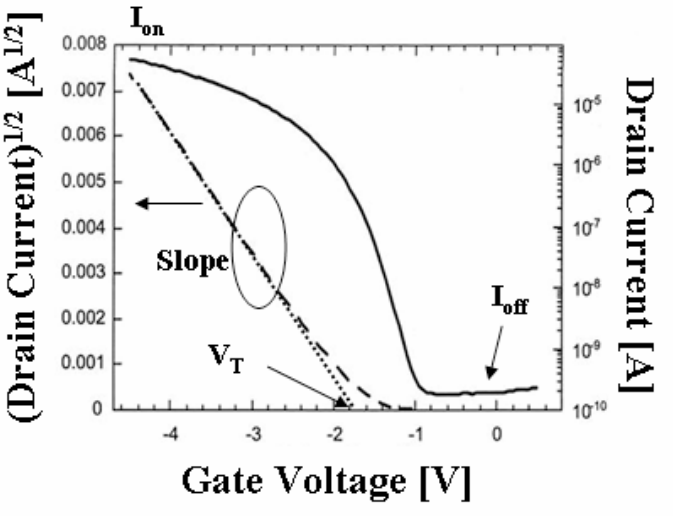

Figure. 2.4 $\sqrt{I_d}$ as a function of V_g (red circles) and transfer curve of a typical device with the main working parameters outlined.

Field-Effect Mobility -- μ

Charge mobility in OFET is gate voltage dependent [13], due to the presence of traps localized near the transport band-edge that limit the charge transport. When the gate voltage is applied, the Fermi level at the insulator-semiconductor interface moves towards the band edge leading to trap filling. After filling the traps the mobility increases, so that the determination of charge mobility is difficult. The gate-bias dependence of the mobility can be described by the following equation:

$$\mu=K\,(Vg-V_T)^{\gamma}$$

where K and γ are empirical constants.

Due to this dependence, usually mobility value is estimated by the Transfer characteristic under the lowest possible value of Vd, so that the mobility remains practically constant along the channel.

Moreover, since it has been demonstrated that field effect mobility in polycrystalline organic films increases with the grain size, a model has been formulated to take also into account the charge transport limited by grain boundaries [14]. The model consists in considering that the material was made by high and low conductivity regions, respectively the grains and the boundaries, that are connected in series so that the mobility can be expressed as:

$$\frac{1}{\mu} = \frac{1}{\mu_g} + \frac{1}{\mu_b}$$

where μ_g and μ_b are the mobility in the grain and in the boundaries.

Contact resistance -- R_C

As the performance of OTFTs improves the limitations due to contact resistance become crucial.

This contact resistance is accounted for by introducing a voltage drop R_cI_d in the equation 1.1, replacing the drain voltage by V_d-I_dR_c:

$$Id = \frac{W}{L}\mu C_i (V_g - V_T)(V_d - I_d R_C)$$

The channel conductance g_m is then given by:

$$g_m = \frac{\partial I_d}{\partial V_d} = \left(\frac{1}{\frac{W}{L}\mu C_i \left(V_g - V_T\right)} + R_C^{-1} \right)$$

Considering the dependence of the current/voltage characteristics on channel length, the parasitic resistances can be extracted by the following equation:

$$R_{on}(L) = R_{ch}(L) + R_C = \frac{L}{W\mu C_i \left(V_g - V_T\right)} + R_C$$

While the contact resistance is independent on channel length, the channel resistance is proportional to it. Consequently, R_C can be extracted by the transistor characteristics in linear regime for different values of L. In particular, it could be extracted by the linear fit of R_{on} versus L named *Transfer Line Method*.

Threshold Voltage -- V_T

Threshold voltage V_T is often extracted from $\sqrt{I_d}$ vs V_g plot and its value is often large because of large amount of the traps at the interface between semiconductor and dielectric. Traps were filled when the gate voltage is applied, so that larger gate voltage needs to induce the current channel near the interface.

For a solution-processed active interface, in which either the gate-dielectric material is deposited from solution onto a solution-processable semiconducting material or vice versa, it is critical to avoid dissolution or swelling effects during deposition of the upper layer, which can lead to increased interface roughness and traps. Moreover, the presence of defects in the semiconductor, at the interface can cause instabilities of the threshold voltage. For practical applications, the V_T stability is an important factor because it is closely related to the operational and lifetimes of the device. In most *p-type* organic semiconductors a negative shift of the threshold voltage is observed upon prolonged operation generally attributed to charge trapping in the organic semiconductor and/or at the active interface.

It has been reported that in films of *p-type*, solution processed pentacene in contact with an organic photoresist dielectric, the threshold voltage shifts to more positive values for negative gate bias stress during operation in air. The V_T shift was attributed to mobile ions drifting in the gate dielectric in the presence of water, causing accumulation of positive counter-charges in the semiconducting layer. Despite that, several groups have recently reported encouraging results on temperature stress and lifetime data for solution-processed OFETs measured and stored in air without special encapsulation.

Although there is still, of course, significant work to assess and improve the operational of OFETs under realistic application conditions and to understand degradation mechanisms in much more detail, the experimental results strongly suggest that solution-processed OFETs in the next future could exhibit similar device stability and reliability to their Si counterparts [15].

On/Off Current Ratio -- I_{on}/I_{off}

Current modulation is the ratio of the current in the accumulation mode over the current in the depletion mode. It is an important parameter for transistor applications and it depends on the mobility, charge density, conductivity and thickness of the semiconductor layer.

I_{off} is defined as the case of little or no current flowing between the Source and Drain electrodes at a given Source-Drain voltage, while I_{on} refers to the substantial source-drain current flow for the given Source-Drain voltage.

This parameter is highly susceptible to the off-current level and in all organic devices can be highly compromised. In fact, in contrast to inorganic materials, organics pass current by majority carriers and an inversion regime does not exist. Then, the off-condition is more difficult to achieve. Moreover, the off-current is a function of the chosen insulating polymer since any subsequent processing after its deposition can damage it. On the other hand also the noise level of the measurement equipment can affect the measured value of such a current. Obviously since the lower current is desired in the off state it needs to minimize leakage problems in the inactive state. For many memory and display applications, a high on/off ratio exceeding 10^8 is a quite important requirement than the high mobility. An on/off ratio that is greater than 10^6 can be achieved by using organic semiconductors, which is high enough for transistor applications.

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Chapter 3

OTFT: Experimental results on Bottom Gate devices

The experimental activity reported in this Chapter concerns with the characterization of different polymer semiconductors in the Bottom Gate - Bottom Contact OTFTs architecture. The final OTFT consists of a hybrid structure where the unique organic part was the semiconductor layer.

3.1 Devices structures

Single gate devices were realized on silicon substrates for organic semiconductors testing. The device structure has bottom a gate-bottom contact architecture, with the advantage that the organic semiconductor films was deposited in the last process step, see Figure 3.1.

The templates for these OTFT devices were developed at the University of Wurzburg (Germany) within a European project named NA.I.M.O ("NAnoscale Integrated processing of self-organizing Multifunctional Organic materials" N. NMP4-CT-2004-500355). Metal contacts were realized by lithography on a thin layer of SiO_2 gate barrier deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD).

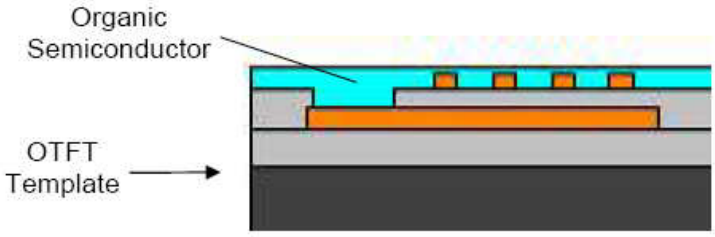

Figure 3.1 OTFT Template architecture developed at Wurzburg University.

The detailed fabrication process of templates is reported schematically in Figure 3.2.

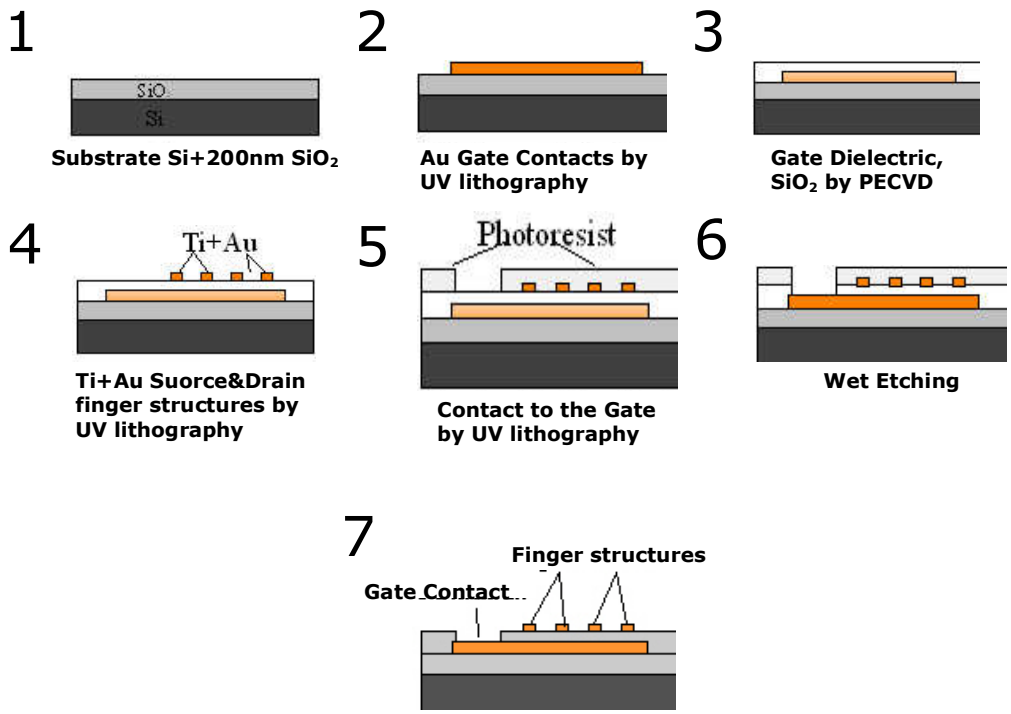

Figure 3.2 Fabrication flow chart for OTFT test bed.

Three different OTFT templates were developed including OTFT test structures with different geometrical features, and two of them are reported in Figure 3.3. For all the structures, Source and Drain electrodes have the interdigitated structure as shown in Figure 3.4 where L is the channel length and W the channel width, given by $N*w_{finger}$ where w_{finger} is the overlapping of the fingers and N the number of spaces between the fingers.

Figure 3.3 Optical Images of two of the Wurtzuburg templates, in the first L varies with W keeping constant their ratio W/L; in the second W is fixed and L varies

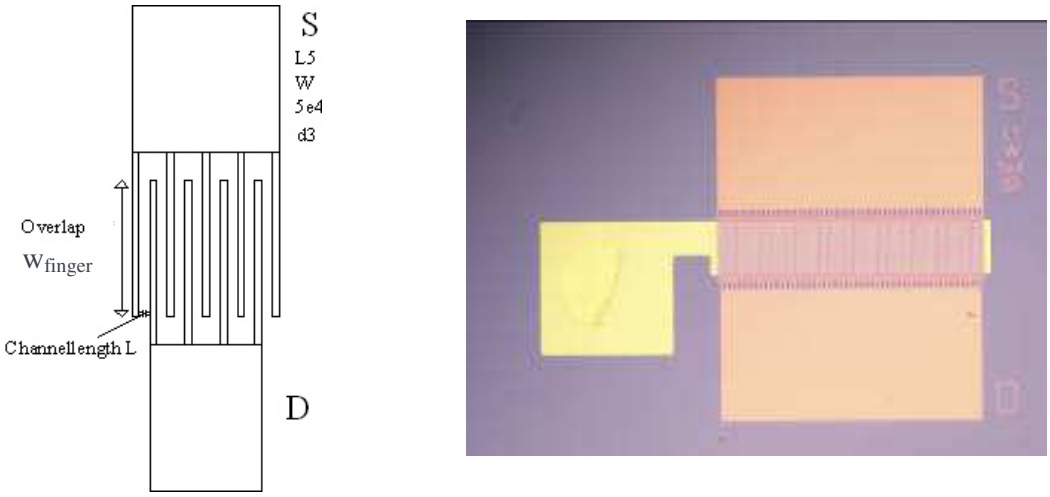

Figure 3.4 Geometry of OTFT test structure and optical microscopy image of a test device on template, d being the finger width.

Devices with different geometries have been realized by varying both the channel length in the range L=0.5÷100μm, and the width W=1÷100 mm, corresponding to a change in the form factor W/L=20÷10000.

Moreover, pads and *vias* have been designed to guarantee easy electrical contacts to the characterization electronics by means of a probing system.

Both device configuration and layout influence the electrical properties, and these test beds should be considered only as a starting point for selecting organic materials according to their performances and processing properties.

3.2 Experimental set-up

Testing devices were prepared in the Clean Room of the STMicroelectronics labs (Portici, Naples). The organic semiconductor (OS) solutions were deposited on the Wurzburg templates by spin-coating or casting both in air and glove box (Labstar MBraun in Figure 3.5) to control the gas exposure.

Figure 3.5 Glove boxes system for devices preparation.

The device electrical characteristics were measured by a Probe Station (PM5 Karl Suss) equipped with micrometric manipulators provided of metallic tips to contact devices electrodes, and a Parameter Analyzer to measure the IVCs. A photograph of the electrical set-up is shown in Figure 3.6.

Figure 3.6 PM5 Karl Suss Probe Station and 4155C Agilent Parameter Analyzer.

3.3 Selected Organic Semiconductors

Both low weight molecules and polymers able to be processed by liquid phase have been considered as organic semiconductor. Different classes of materials have been tested. An opportunely functionalized pentacene (TIPS-Pentacene) and a tetrathiafulvalene derivate (DB-TTF) have been studied as small molecules. Concerning semiconductor polymers, different thiophene derivates have been characterized but also a promising derivative of poly-(triarylamine). In particular this analysis, performed on bottom gate test structures, furnished important indications about the selection of the semiconductors to be used in all organic OTFT.

a) ***TIPS Pentacene***

Functionalized pentacene, 6,13-bis_triisopropyl-silylethynyl_pentacene (TIPS-pentacene) has been prepared and supplied by the HOLST Center (Eindhoven, Netherland), as soluble organic semiconductor for OTFT fabrication. The functionalized small molecules have permanently attached groups that modify the solubility of the material and its processing properties, designed to minimize the impact on the electronic properties of the material, or potentially to improve them. Because there is no need to remove the functional groups, no high-temperature steps are required 0.

The electrical test devices were prepared by drop casting a solution at 2%wt: (0.03g TIPS pentacene/1.5g solution) obtained dissolving 30 mg of TIPS-pentacene powder in toluene and stirring for 24 hours. After solution deposition the sample was dried in solvent environment for one night. An example of realized samples is showed in Figure 3.7.

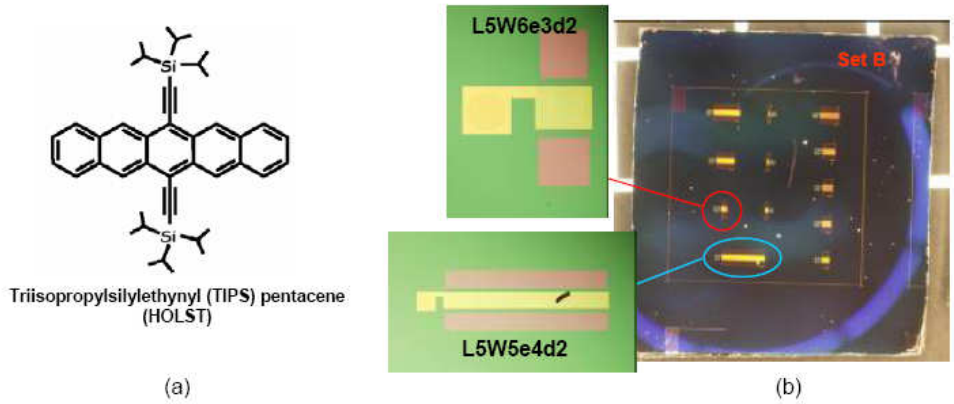

Figure 3.7 Chemical symbol of TIPS Pentacene (a) and microscope image of device under test realized by the template Set B with fixed value of L and different W (b).

Devices of different sizes have been characterized and most representative Transfer and Output Characteristics are reported in Figures 3.8 and 3.9.

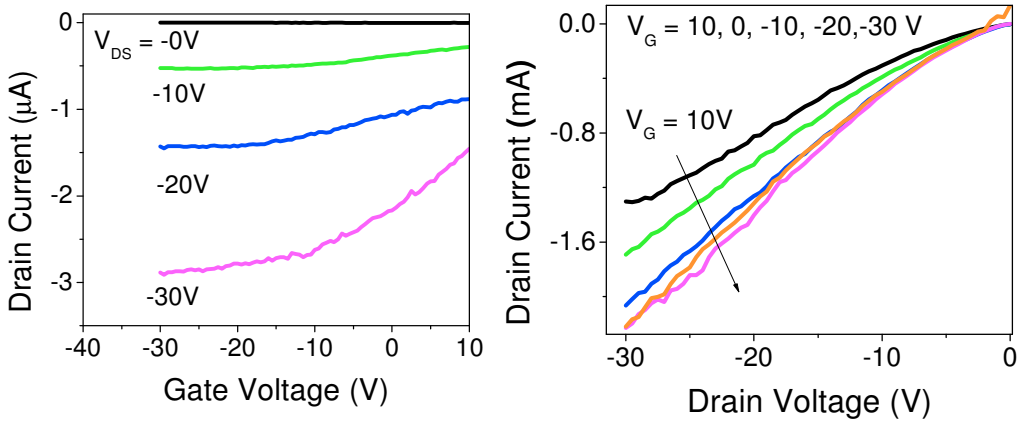

Figure 3.8 Transfer and Output characteristics of a TIPS-Pentacene device of size L=1µm and W=1e4µm .

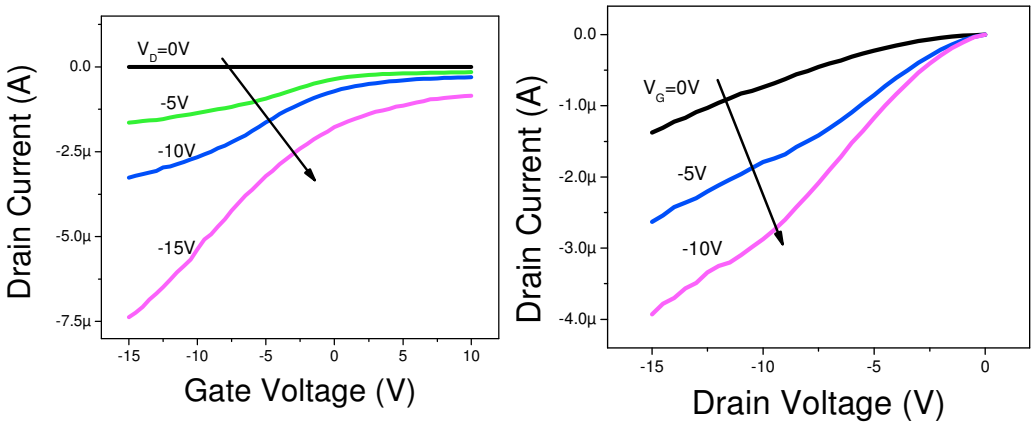

Figure 3.9 Transfer and Output curves of a TIPS-Pentacene device of size L=5µm and W=5e4µm.

These I-V characteristics show the presence of high leakage currents especially in the larger length devices. The comparison between the transfer characteristic of different devices normalized to the aspect ratio is shown in Figure 3.10, where a clear dependence of the electrical performances of the devices on the geometrical characteristics is quite evident.

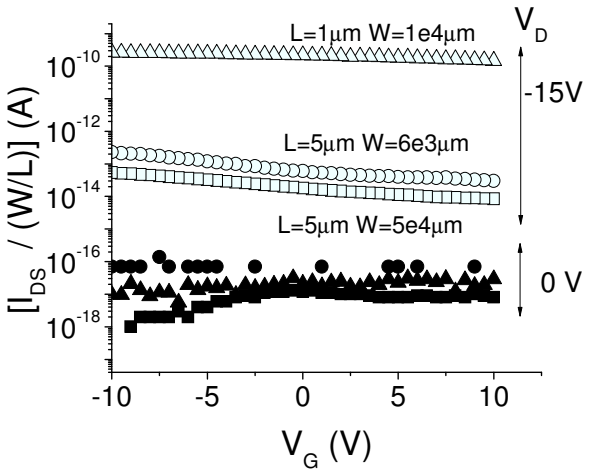

Figure 3.10 Transfer curves of different devices normalised to the aspect ratio in the assumed OFF and ON conditions.

Moreover, regardless to the size, the devices do not reach the depletion condition when Vg assumes positive values. The reasons of this behavior probably lie in the

high conductivity of the OS, and in the properties of the OS - SiO_2 dielectric interface which produces large contact resistances.

A not efficient interface OS/dielectric can be responsible for an insufficient charge induction in the semiconductor, which can explain the low modulation of the Drain current with the Gate voltage. Moreover, observing the experimental results at low channel lengths where the contact resistances effects are more effective due to the reduced channel resistance, it is possible to estimate a contact resistance close to 1MΩ that hides any channel modulation effect. On the other hand, observing the output characteristics the absence of a saturation region confirms the presence of this contact resistance, and according to literature it indicates the difficulties to reach the pinch-off condition with organic semiconductors.

In order to solve the encountered problems different strategies can be adopted such as treatments of the SiO_2 by Silanes solutions to improve the semiconductor adhesion or modification of the device structure.

b) ***DB-TTF (CSIC)***

Fabrication of single crystal OFETs based on dibenzo-tetrathiafulvalene (DB-TTF), is reported in literature [2]. Moreover, it is possible to prepare good quality DB-TTF crystals with very high mobilities from solution [3] which makes this material very interesting for potential applications in low-cost electronics.

DB-TTF has been prepared and supplied by the "Institut de Ciencia de Materials de Barcelona" (CSIC), for deposition on Wurzburg test beds. Testing devices were prepared by dissolving 1 mg of DB-TTF powder in 1 ml of toluene and stirring the solution for 2 hours.

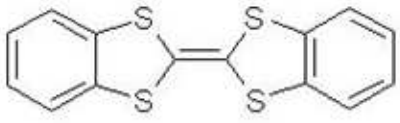

Figure 3.11 Chemical symbol of DB-TTF.

Then, the DB-TTF solution was deposited by drop casting on test beds and dried in solvent environment, finally the samples were annealed on hot plate at 90 C for 20'.

Devices of different size were characterized by Transfer and Output measurements as shown in Figure 3.12 for a device with L=30 µm and W=2mm.

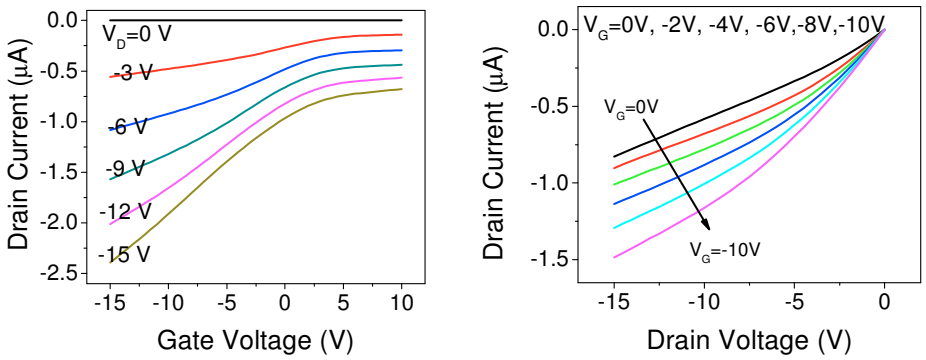

Figure 3.12 Transfer and Output curve of device L=30µmW=2e3µm.

Device characterization under different light conditions evidenced a photo-induced effect that has been only recently reported on similar works [3]. As shown in Figure 3.14, at L=5 µm and W=6mm in dark environment the OTFT does not work, the effects of Gate voltage modulation appears only in sufficient light conditions.

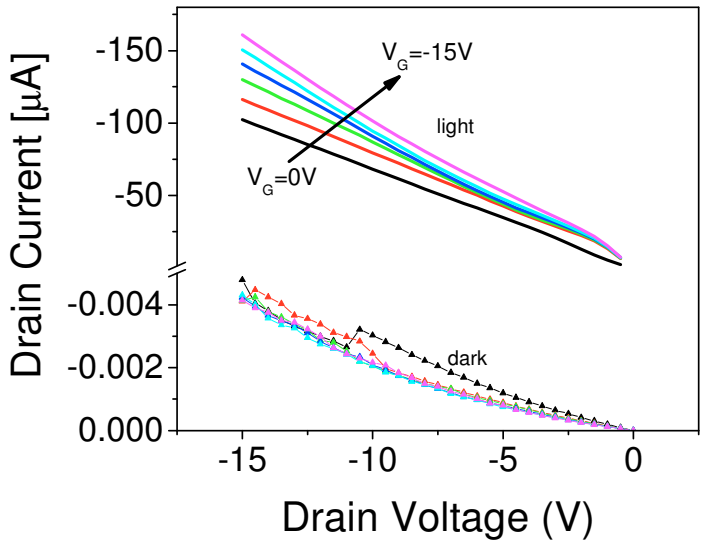

Figure 3.13 Transfer characteristics of device L5W6e3d2 under dark and light conditions.

The analysis of the experimental data showed that DB-TTF based OTFTs are characterized by mobility values close to 10^{-3} cm^2/V s under light conditions and performance degradation with working cycles. The detected mobility is nearby two

orders of magnitude lower than the values reported in literature for the same material [4]. Moreover, V_T values close to 10V and Ion/Ioff ratios lower than 10 have been detected showing that the devices are affected by noteworthy leakage problems not only through the Gate dielectric.

Since the devices seem to be affected by the same inconveniences of the TIPS pentacene devices, it could be possible that the material performances were screened by the presence of defects in the organic film and at the interface with the insulating layer of SiO_2.

c) ***Poly(triarylamine)***

Triarylamine based devices were prepared by spin-coating a toluene solution of poly(triarylamine) on the templates and drying it at room temperature for 10 minutes and at 100°C for 30 minutes. Device testing showed reproducible results on different testing cycles, but low performances. In particular, mobility values lower than 10^{-3} cm^2/V s were detected and I_{on}/I_{off} ratios lower than 10^2. Such unsatisfactory values could be ascribed to the coupling of the Silicon oxide with such organic semiconductor. On the other hand, it was already demonstrated that this material exhibits very good performances when coupled with low-k dielectric [5].

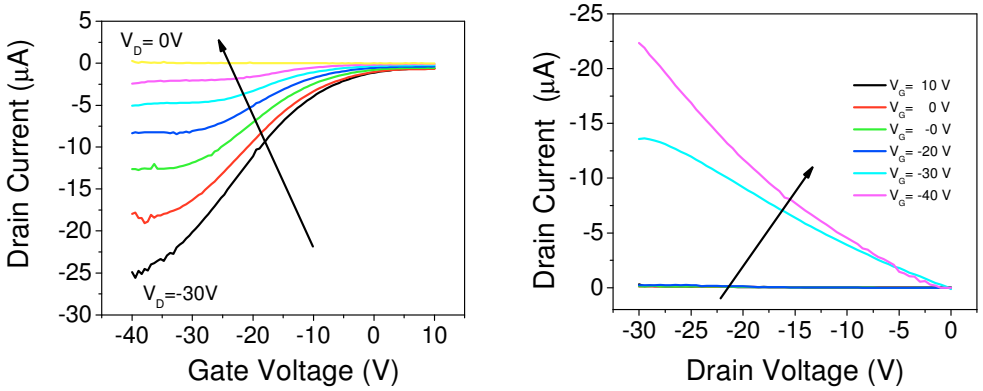

Figure 3.14 Transfer and Output characteristics of device L1.5W1.5E4d3.

d) ***High performance thiophene-based semiconductor polymers***

The above mentioned results on the TIPS-Pentacene and DB-TTF can be improved by suitable treatments to get better interfaces between the different materials, but nevertheless they are well far from the industrial requirements of reproducibility.

There is in fact evidence that both the materials can guarantee the best performances only in particular conditions i.e. when their large organic crystals form a conducting channel between Source and Drain [6]. This condition cannot be fulfilled on large area devices with an acceptable degree of reproducibility.

On the other hand, many papers have been published about Thiophene derivatives, the most famous being poly3-hexylthiophene (P3HT), that has the only inconvenient to be degradable in air. In the last years many researchers worked to chemically modify it in order to save its performance and avoid any instability [9].

According to literature, a Thiophene blend supplied by FlexInk has been tested in the Wurzburg templates including L=100μm structures. Due to the complexity of the material structure, a morphology dependence on the template surface treatment has been found as shown in Figure 3.15. In particular, Figure 3.15.a refers to a deposition after plasma O_2 treatment (O_2 flow = 100 sccm, Power = 30W, Pressure = 1 x 10^{-1} mbar, Time = 30s), while Figure 3.15.b to a deposition after SAM treatment and Figure 3.15.c shows the materials deposited on template treated by both plasma O_2 and SAM. In particular, the SAM treatment was performed by soaking the templates in 1 mM Isopropanol solution of Pentafluorobenzenthiol for 24 hours at room temperature.

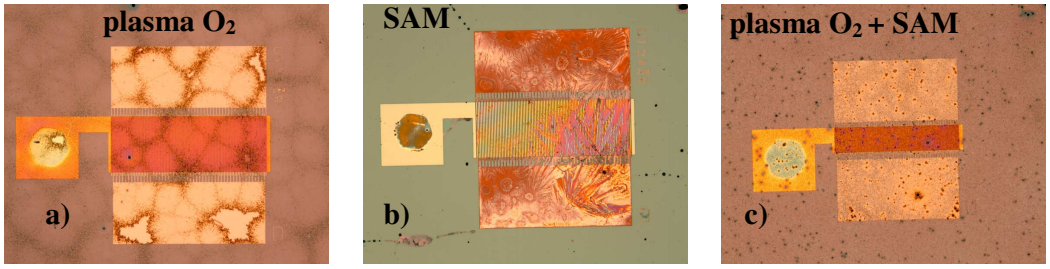

Figure 3.15 Images by optical microscope of the experimental polymer deposited after different template treatments as indicated in the text box.

After washing the sample in Isopropanol in ultrasonic bath for 5 minutes and drying it in Nitrogen flow, the semiconductor has been deposited by spin coating at 600 rpm for 15 s and 2000 rpm for 30 s and annealed at 80°C for 2 minutes.

Conditions of Figure 3.15.c are the achieved one even if material aggregates are visible by optical microscope. This can be avoided filtering the solution (pore dimension 0.2 µm). The electrical tests for optimized device L100W2e3d2 (L = 100µm; W = 2mm; W/L = 20) are reported in Figure 3.16.

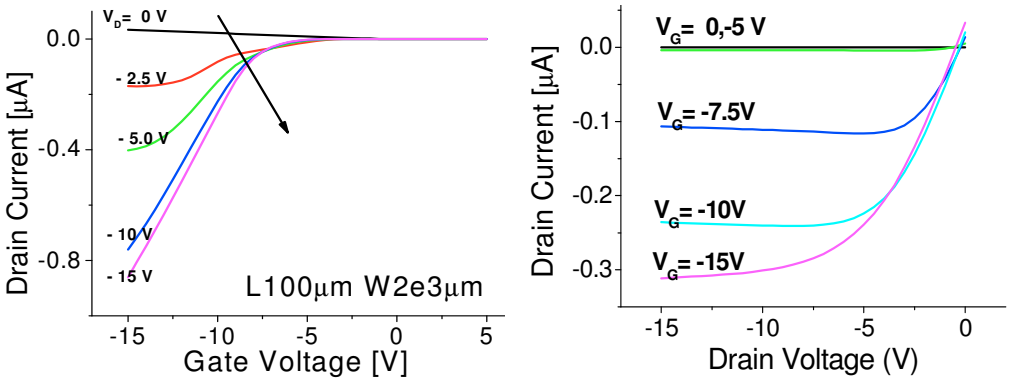

Figure 3.16 Transfer and Output curves of experimental polymer device L100W2e3d2.

The electrical performances of devices based on this material can be considered satisfactory. Mobility values of 0.154 cm^2/Vs were in fact measured and Ion/Ioff higher than 10^2, with threshold values V_T=-1.4V. Moreover, devices performances seem to be quite stable and reproducible at air exposure.

On the other hand, the analysis of the mobility values with the channel length, reported in Figure 3.17, showed an abrupt increase when channel length is higher than 5µm confirming that at L<5 µm the presence of short-channel effect severely affect device performances, and leads to an underestimation of the mobility values according to recent literature on P3HT [10].

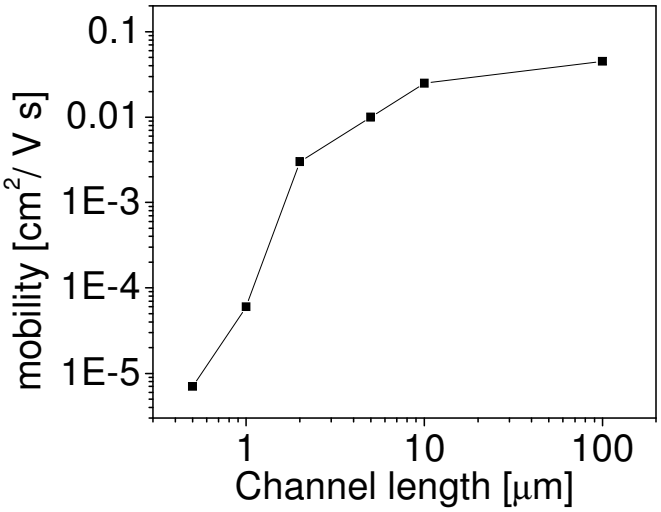

Figure 3.17 Mobility behaviour varying L.

Final Remarks

According to the previous characterization of organic semiconductor materials, we found results apparently in contrast with current literature. Of course, more appropriate deposition conditions could be required in the case of low weight molecules for obtaining as expected results. A possibility could be represented by a treatment of the template surface by octadecyltrichlorosilane (OTS) or hexamethyldisilazane (HDMS) to form hydrophobic thin layer on silicon oxide. Moreover, the control of the slow solvent evaporation during deposition can help in improving the formation of crystals. Unfortunately, a well oriented crystal between source and drain necessary to achieve the best performances is quite challenging. These materials are very sensitive to deposition conditions and do not guarantee desiderate uniformity. So they have been considered not easily processable especially in top gate architectures. On the other hand new generation high performance polymers have been analyzed that joint the electrical properties of Thiophene to the advantages of a polymeric structure as will be demonstrated by the experimental results in the following chapters.

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Chapter 4

OTFT: Top Gate Bottom Contact devices

In this Chapter the experimental work concerning both the fabrication and characterization of the Top Gate-Bottom Contact devices was reported. The final goal of the thesis is to demonstrate the feasibility of all Organic Thin Film Transistor devices with micrometric and sub-micrometric feature sizes. To this aim, Top-Gate Bottom Contact OTFT prototypes have been developed and characterized. This configuration offers the fundamental advantage that, depending on the desired channel length L, different patterning techniques can be selected since the Source and Drain contacts are deposited as the first layer on the substrate. Due to the versatility of the manufacturing process, there are different possibilities of innovation in realizing flexible and low cost organic devices.

4.1 OTFT Design

In this thesis work, Top Gate Bottom Contact (TG-BC) OTFT devices were realized with Source and Drain electrodes having a multi-finger structure for minimizing device size and preserving current performances.

According to Eq. 1.2, the current I_{DS} in the saturation regime increases with mobility μ, with the aspect ratio W/L and the capacitance Ci per unit area of the insulating layer according to the relation:

$$I_{DS} = \frac{1}{2}\mu \; Ci\left(\frac{W}{L}\right)\left[(V_G - V_T)^2\right]$$

=

Moreover, the speed of logic circuits made by OTFTs is determined by the mobility values according the following equation:

$$\frac{1}{\tau} = f_{\max} = \frac{g_m}{2\pi C} = \frac{\mu_{FET} V_D}{2\pi L^2}$$

where g_m is the transconductance and $C = C_i LW$ is the total gate capacitance. Then, high carrier mobilities are fundamental both for high drain current at low V_G and V_D voltages, and for fast switching. The minimum mobility value for OTFT device depends on the application as well as on device geometry. However, materials with mobilities less than 10^{-3} cm^2/V s are generally considered unsuitable for TFT applications. Moreover, the permittivity of the insulator influences both the current and the speed of OTFTs, since the capacitance per unit area of the gate insulator, C_i, is described by the following equation:

$$Ci = \frac{\varepsilon_0 \varepsilon_r}{d}$$

where ε_0 is the permittivity of free space, ε_r the relative permittivity (dielectric constant), and d the thickness of the insulator.

Usually, organic dielectrics need high thicknesses to be uniform, and they are characterized by low relative permittivity as compared to inorganic dielectrics. On the other hand, for good device performances high trans-conductance is desirable too so that the W/L ratio should be maximized. In conclusion, due to both the reduced values of mobility of organic semiconductors and the limited values of capacitance, the only way to increase OTFT performance is to reduce channel length L.

For these reasons test structures have been designed with inter-digitated electrodes (see Figure 4.1) according to the following rules: L has been scaled from 10μm down to 1nm and for each value of L (1μm, 2μm, 3μm, 5μm, 10μm), W = (20, 40, 60) L. In this way the scalability of fabrication processes and material properties has been studied.

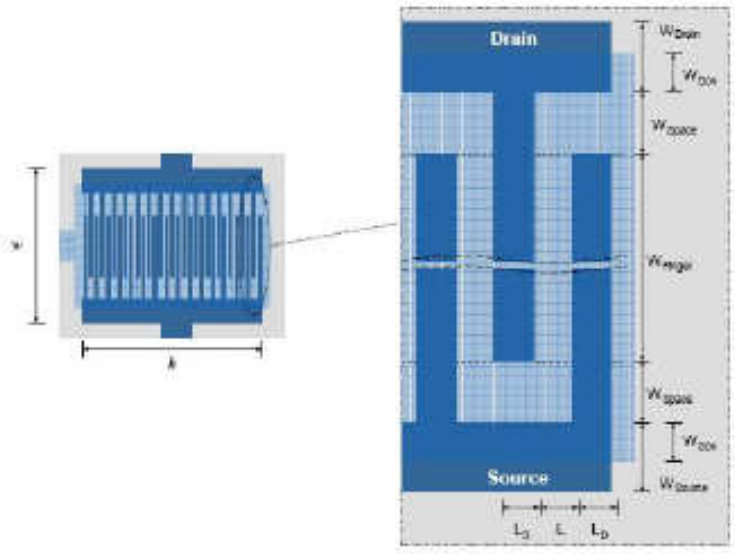

Figure 4.1 Geometrical features of multifinger structure for source and drain electrodes.

4.2 Process Flow Chart

The simplest way to fabricate the Top Gate Bottom Contact OTFT device is to deposit the organic semiconductor and the dielectric everywhere on patterned source and drain electrodes, and finally to align the gate electrode on the top (see Figure 4.2).

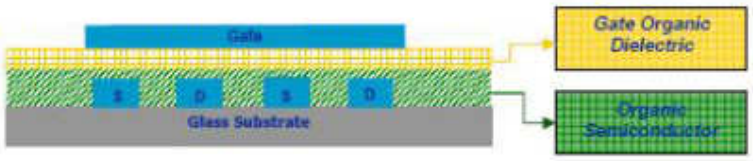

Figure 4.2 Schematic picture of OTFT structure

According to this architecture, the flow chart for devices preparation was stated by the following steps:

1. Patterning of Source and Drain electrodes on substrate.
2. Deposition of organic semiconductor by spin-coating.
3. Deposition of organic dielectric polymer by spin-coating.
4. Fabrication of aligned Gate electrode

4.2.1 Source and Drain Fabrication

Optical lithography has been used to define micrometric structures of OTFT devices: Mask Aligner (Karl Suss MA6) has been used to align the photo mask and expose the sample. Only one 7" photo-mask including all the structures to be patterned has been used, composed by sub-units 2:5 cm x 2:5 cm (see Figure 4.3) and the layout of a single sub-unit with the enlarged detail of structures is shown in Figure 4.4.

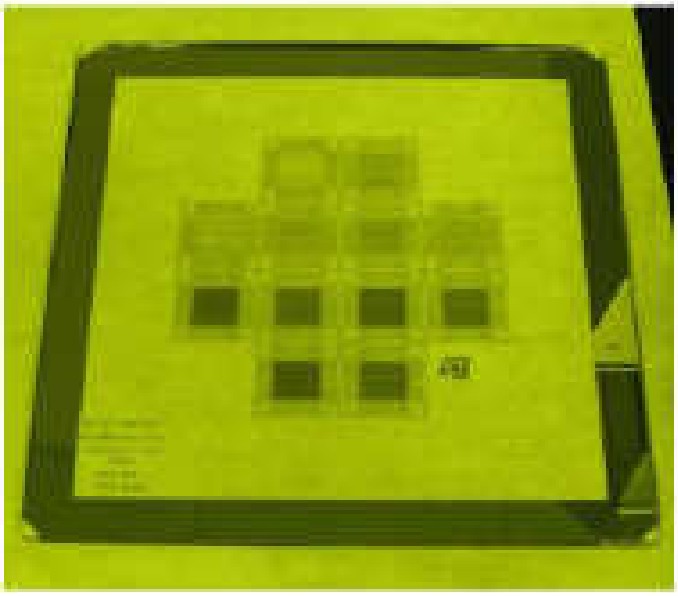

Figure 4.3 Picture of 7" photo-mask including all the structures to be patterned.

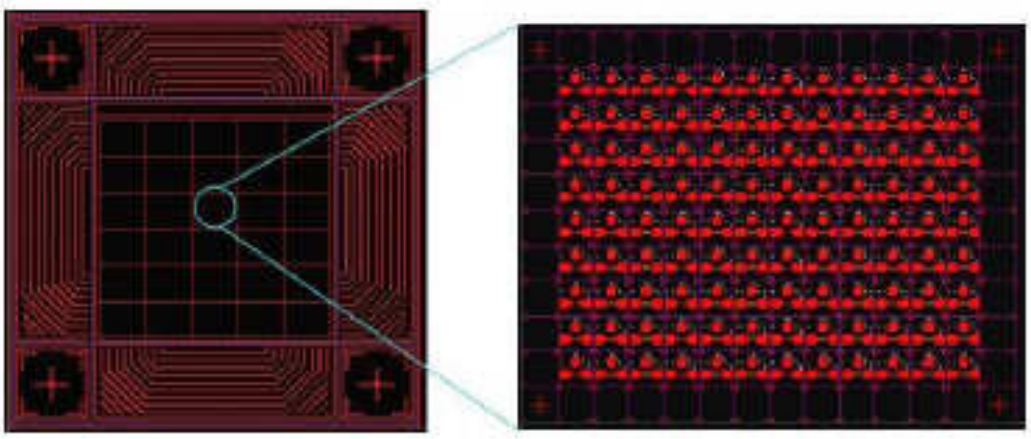

Figure 4.4 Layout of transistor array with L value ranging from 2μm to 10μm.

The lithographic process requires the following steps:

1-Cleaning of glass substrate

1 inch borosilicate glasses were immersed in acetone, then in Isopropanol both for 10 minutes in ultrasonic bath and finally dried by nitrogen flow. A further cleaning by O_2 plasma (O_2 flow = 10 sccm, Power = 150W, Pressure = $1{:}3x10^{-1}$ mbar, Time = 50 minutes) has been performed in Sentech Etchlab 200 system.

2 Resist deposition

The resist (Allresist AR-N 4340) was deposited by spin coating at 900 rpm for 10s and at 5000 rpm for 30s, to obtain a nearby 1.6μm thick layer. Coated substrates have been pre-baked on a hot plate at 85 C for 2 minutes.

3 Resist exposure

The deposited resist was exposed by Mask Aligner @ 365nm in hard contact mode with energy intensity (15mW/cm2 x 4.0 s). After exposure, post bake at 95 C for 5 minutes on hot plate was performed

.

4 Resist development

The samples were immersed in pure developer (Allresist AR 300-475) for 60s and rinsed in deionized water immediately after developing process.

5 Au deposition

A thin layer of gold was deposited by thermal evaporation[1] in Emitech K975X Turbo evaporator.

6 Lift-off

Au contacts are patterned on the substrate by lift-off of the photoresist after metallization. The resist mask was removed putting the sample in a beaker with acetone or remover (Allresist AR 300-70) in ultrasonic bath for few minutes. The thickness of gold structures is near to 30nm as measured by profilometer.

[1] Thermal evaporation is used to deposit materials with relatively low melting points under high vacuum. Solid source material is placed in a conductive filament or boat and subsequently heated by passing large currents through the source holder. Evaporation occurs when the source material melts and subsequently evaporates or directly sublimes.

The same process has been used to deposit Source ad Drain electrodes on plastic 1 inch square substrates made of Poly(ethylene naphthalate) (PEN) (HCQ6Z1 DuPont Teijin Films).

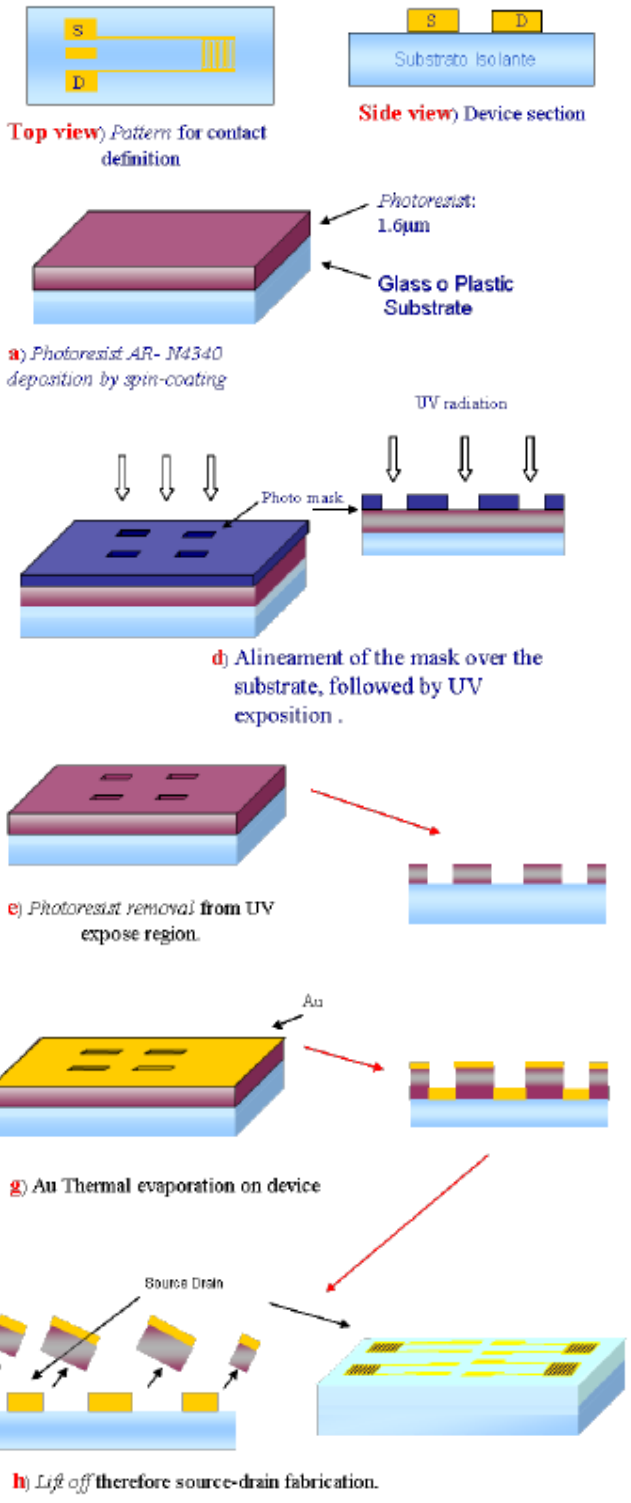

Figure 4.5 Process Flow Chart for Source-Drain contacts deposition.

4.2.2 Semiconductor and Dielectric deposition

Different OS have been tested but the best performances were obtained by using an experimental high performance Thiophene blend in bottom Gate devices. In Top Gate devices this material has been coupled with a suitable dielectric polymer tailored on the semiconductor, and OTFT manufacturing process has been optimized. Before the deposition of the semiconductors on Source and Drain electrodes, a surface treatment with Self-Assembly-Monolayer (SAM) was done to improve the adhesion and charge injection. To this aim a pre-treatment by O_2 plasma (O_2 flow = 100 sccm, Power = 30W, Pressure = $1x10^{-1}$ mbar, Time = 30s) has been performed. Then, the sample has been soaked in Isopropanol solution of Pentafluorobenzenthiol (10mM) for 24 h at room temperature. It has been washed in IPA in ultrasonic bath for 5 minutes and dried by nitrogen flow. Then the semiconductor has been deposited by spin coating at 600 rpm for 15 s and 2000 rpm for 30 s and annealed at 80C for 2 minutes. Afterwards the dielectric has been deposited at 500 rpm for 10 s and 2000 rpm for 30 s.

4.2.3 Gate Electrode Fabrication

To complete the OTFT devices, Gate electrodes have been patterned by standard photolithographic techniques using mask aligner. This method allowed patterning gate electrodes opportunely aligned.

The procedure is the same as described for patterning Source and Drain electrodes; the only difference is the treatment before depositing resist. Again, a treatment by plasma O_2 is necessary to make hydrophilic its surface without damaging. Using this lithographic process on the top of device is not obvious because the solvent used for both development and removal of resist could damage the underlying layer.

However, it was found that the chosen dielectric is a Fluoro-polymer that resists and protects also the semiconductor layer. A picture of the device after Au gate is reported in Figure 4.6.

Sometimes the following alternative process has been used to pattern gate electrodes:

1 Au deposition

A thin layer (around 20nm) of gold has been deposited by thermal evaporation on gate dielectric.

2 Resist deposition.

The positive resist (Fuji Film Oir 906-12) has been deposited by spin coating at 900 rpm for 10s and at 5000 rpm for 30s, to obtain around 1.6 μm as layer thickness. Coated substrates have been pre baked on hot-plate at 90C for 1 minutes.

3 Resist exposure.

The deposited resist has been exposed by mask aligner @365nm in hard contact mode with energy intensity (15mW/cm2 x 3.0 s).

Resist development.

The sample has been immersed in pure developer OPD 4642 for 50s and rinsed in deionized water immediately after developing process.

4 Wet etching.

The Au was etched by wet etching in a water solution based on HCl and NHO_3. At the end the resist mask has been exposed to UV light and removed by developer solution.

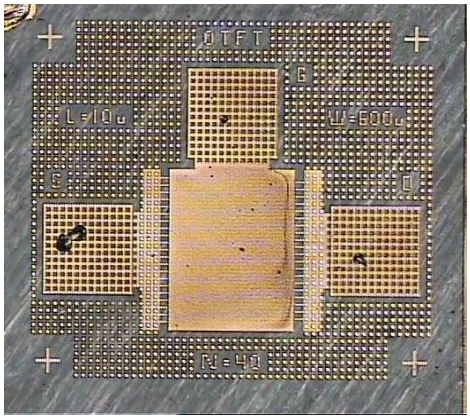

Figure 4.6 Photo of an OTFT device realized on glass substrate by the described flow-chart.

4.3 Glass OTFT

The devices and the single steps of fabrication process were characterized by the electrical measurements. In particular, the highest number of devices was characterized on glass substrates and different depositions processes were tested measuring also the electrical properties of the single deposited layers.

This step-by-step characterization allowed identifying the main breakthroughs of each process in the fabrication flow-chart. As an example, in the Figures below the Transfer and Output characteristics for devices with L=5µm and L=10µm are showed.

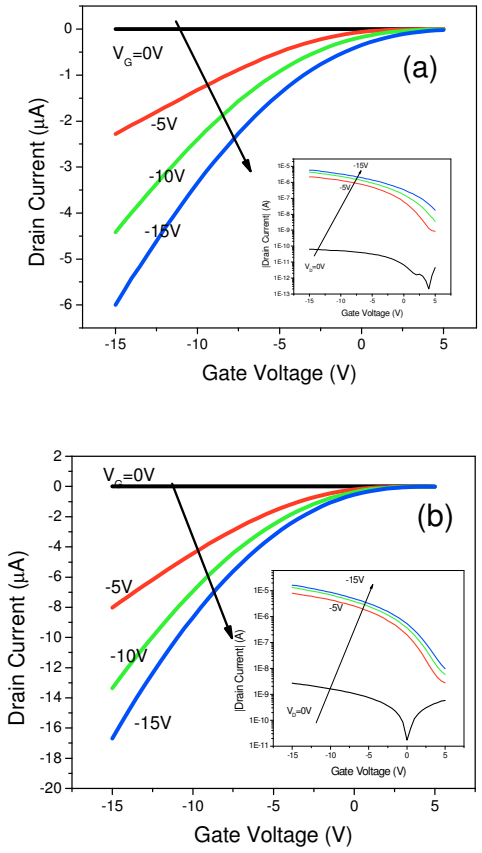

Figure 4.7 Transfer characteristics at different Drain voltages for a device with L=10µmW=600µm (a) and L=5µmW=200µm (b) deposited on Glass substrate. In the insets the logarithmic graph is reported.

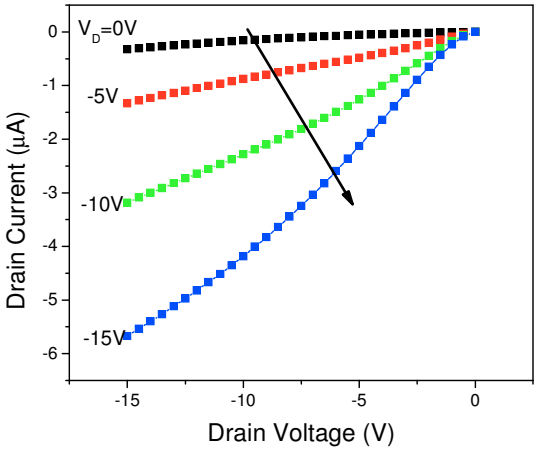

Figure 4.8 Output characteristics at different Drain voltages for a device with L=5μmW=200μm deposited on Glass substrate.

The comparison of the two previous graphs shows that these devices were also affected by the contact resistances. As expected, this effect is less pronounced on L=10μm devices, that reach the depletion condition also for V_D values different from zero and only a shift in the V_T value is observed.

The analysis of the experimental data of Transfer and Output characteristics allows deriving the working properties as summarized in Table 4.1 for different devices. The mobility trend evidences that only in the case of the samples named as Glasses the mobility increases with channel length, while for others the data are strongly scattered and it is difficult to derive a fit law. This behaviour can be ascribed to the critical condition of the deposition process. The mobility variation at different channel lengths for devices on the same substrate is reported in Figure 4.9. Data confirm the results obtained on Bottom Gate structures but the observation of the sample with the Optical Microscope evidenced the presence of crystalline aggregates (see Figure 4.10) that can contribute to the abrupt increase of the mobility [2].

[2] 1) H. Jiang, X.Yang, Z.Cui,Y.Liu, H. Li, and W. Hu, App.Phys. Lett. 94, 123308 (2009);
2) R. L. Headrick, S. Wo, F. Sansoz, J. E. Anthony, App. Phys. Lett. 92, 063302 (2008);
3) Y. Chen I.Shih, J Mater Sci (2009) 44:280–284;
4) M.Mas-Torrent, C. Rovira, Chem. Soc. Rev., 2008, 37, 827–838

Device		L [µm]	W [µm]	N	Idsat [A]	Idoff [A]	Ion/Ioff	Vt [V]	µ [cm2/Vs]
SAMPLE 08		2	80	25	6.95E-07	3.95E-09	1.76E+02	/	2.58E-03
		5	100	5	1.07E-08	1.57E-09	6.78E+00	/	1.23E-04
		10	200	30	1.02E-07	4.80E-11	2.13E+03	/	4.66E-04
SAMPLE 15	GATE BY EVAPORATION	5	100	5	1.08E-06	1.27E-08	8.44E+01	-2.269	2.61E-02
		10	600	20	0.0000322	1.07E-08	3000	-1.313	0.0581
		5	200	35	2.47E-06	4.04E-08	6.11E+01	-2.677	5.57E-03
GLASS 57		2	40	20	4.76E-08	4.64E-09	1.03E+01	/	2.09E-04
		2	120	45	1.88E-08	1.74E-09	1.08E+01	/	1.39E-05
		2	120	45	1.81E-08	1.51E-09	12	-3.056	1.42E-4
		5	200	25	0.0000192	1.56E-07	1.23E+02	-1.502	0.0528
SHADOW MASK 03	GATE BY SPUTTERING	100	2000	1	1.07E-06	2.35E-09	4.55E+02	-1.443	1.54E-01
		100	2000	1	5.38E-07	1.38E-09	3.89E+02	-1.154	0.0847
		100	1000	1	1.15E-07	9.72E-10	1.18E+02	/	4.26E-02
		100	1000	1	1.51E-07	1.65E-09	9.13E+01	/	5.26E-02

Table 4.1: Working parameters of different OTFTs deposited on glass substrates.

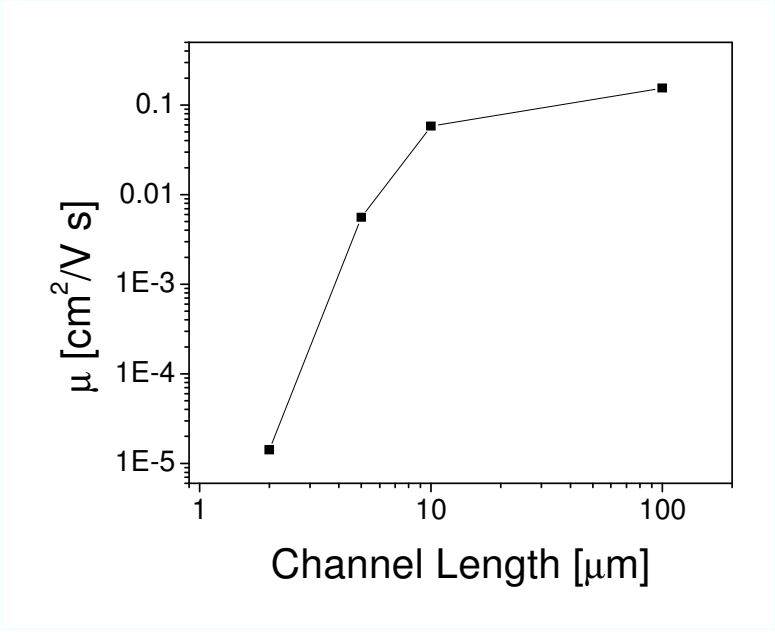

Figure 4.9 Mobility values at different channel length for devices on the same substrate, realized in the same process.

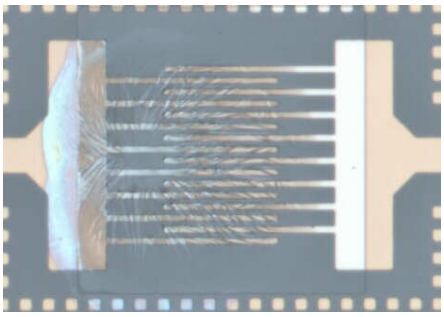

Figure 4.10 Optical image of OS deposited on Source and Drain electrodes L=10µm.

To test materials durability, the device response both to the electrical and thermal stress was investigated. Electrical stress was verified by measuring the Drain and Gate currents keeping constant the Drain and Gate Voltages. As shown in Figure 4.11, Drain current in the device remains nearby constant, and Gate losses can be considered independent on the time so that doesn't correspond to device degradation.

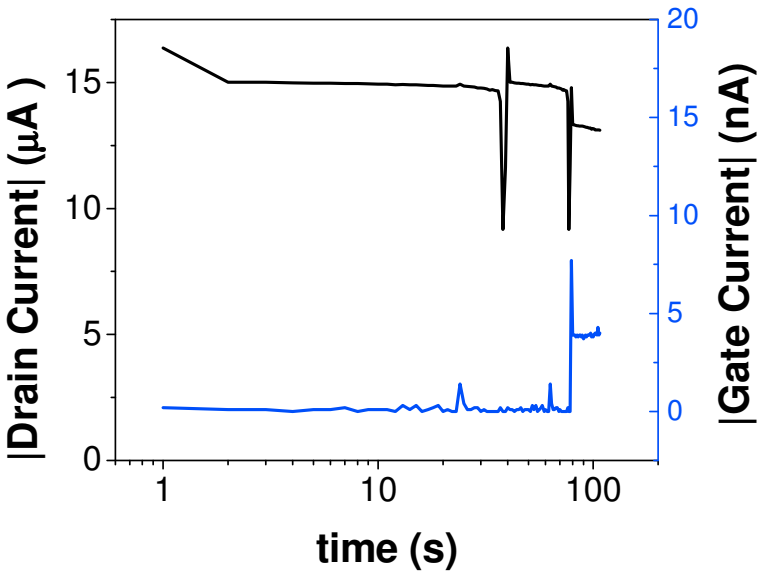

Figure 4.11 Sampling measurements of Drain Current and Gate Current with time at V_D=V_G=-15V.

The analysis of the thermal stress was made by increasing the temperature from 25C to 75C and then coming back to 25C; transfer and output characteristics were recorded at each heating step. These measurements, reported in Figure 4.12, were done in the ST Labs at Castelletto (MI) by a probe station equipped by a Thermo-Chuck and a Termo-Inducing Vacuum Platform (Microtech Cascade Probe Station).

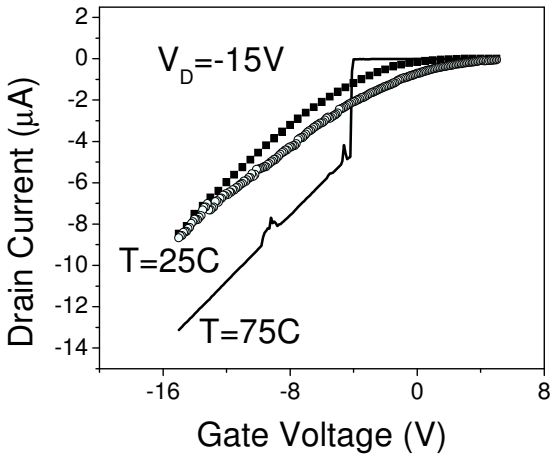

Figure 4.12 Transfer characteristics acquired at different temperature conditions fixed the Drain voltage.

4.4 Logic Gates

Together with the single OTFTs devices, first prototypes of Inverter were also prepared and characterized. An inverter consists of a single control transistor operating as a switch in series with a load. Its function is to provide an output that is the digital opposite of the input signal as showed in a standard Voltage Transfer Characteristic (VTC) reported in Figure 4.13.

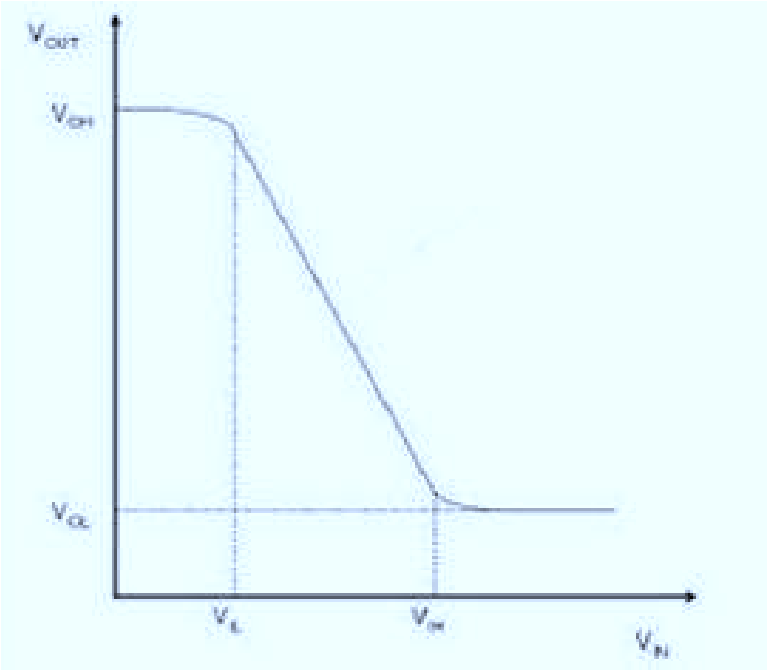

Figure 4.13 Voltage Transfer Characteristic of an Inverter.

Organic Gates are often based on the *organic ratioed logic* that uses only p-type organic transistors by adopting conventional pseudo-pmos architecture. One of the possible architectures is shown in Figure 4.14 where the Inverter is formed by a driver circuit implementing the logic function and a load transistor operating in the saturation region.

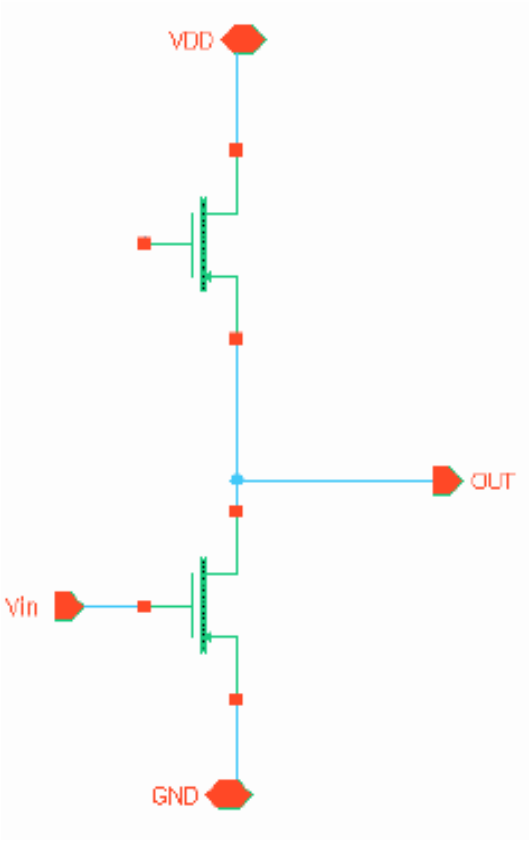

Figure 4.14 Pseudo-pmos organic NOT electrical scheme.

The fabrication of these logic gates is more complex than OTFTs due to the need of vertical interconnections between the Gate and Drain electrodes of the Load transistor. In the first prototypes the interconnection was realized by scratching the polymers with the Probe tips and short-circuiting the two electrodes by external cables. In order to verify the correct work of all the components of the device, firstly the drive and load OTFTs were characterized by the measure of the Transfer and Output characteristics, then the Inverter was tested as reported for example in Figure 4.15.

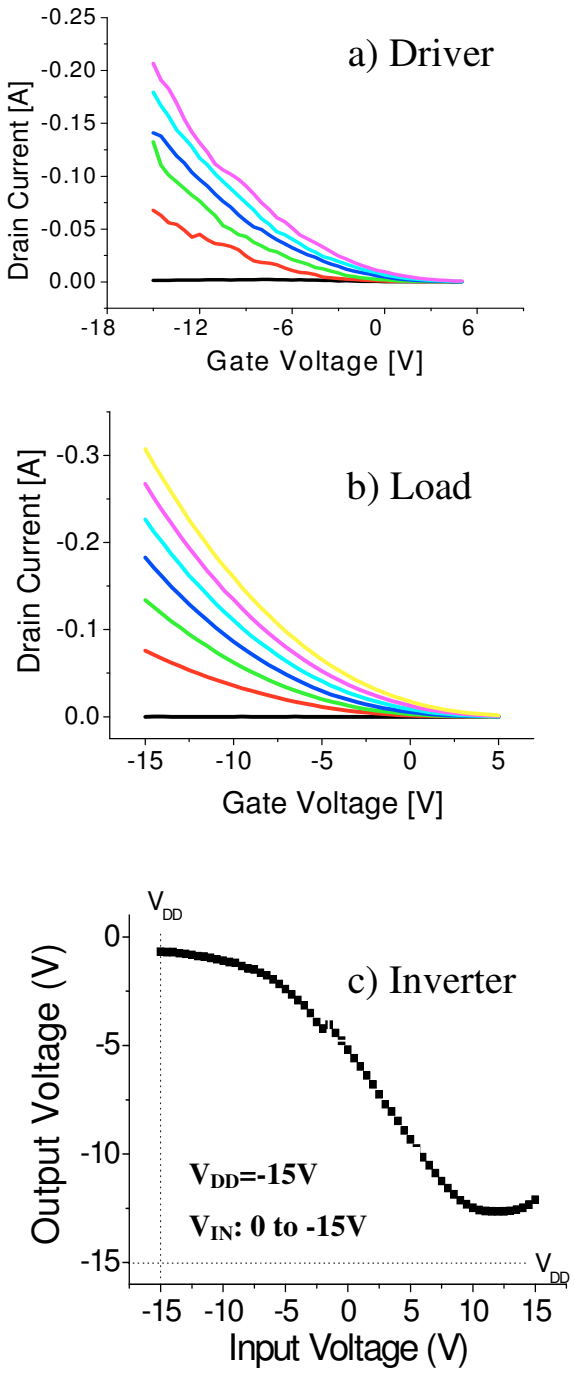

Figure 4.15 a) Transfer characteristic of L=5µm W=200 µm Driver OTFT; b) Transfer characteristic of L=5µm W=200 µm Load OTFT; c) Voltage Transfer characteristic of the Inverter.

As shown in the graphs, the inverter characteristic is affected by a voltage drop due to leakage in the device. This problem is related to the well analyzed problems of contact resistance that also affect the OTFTs performances. For this problem two solutions have been adopted: the localized deposition of semiconductor by Inkjet Printing and the opening of *vias* to realize interconnections.

4.5 Innovative solutions

Both the vias opening and the localized deposition of semiconductor layer involve the use of the InkJet technique. In the ST labs this solution has been implemented by Ink Jet Jetlab II Altatech Semiconductor equipment and updating the process flow-chart with the steps illustrated in Figure 4.16.

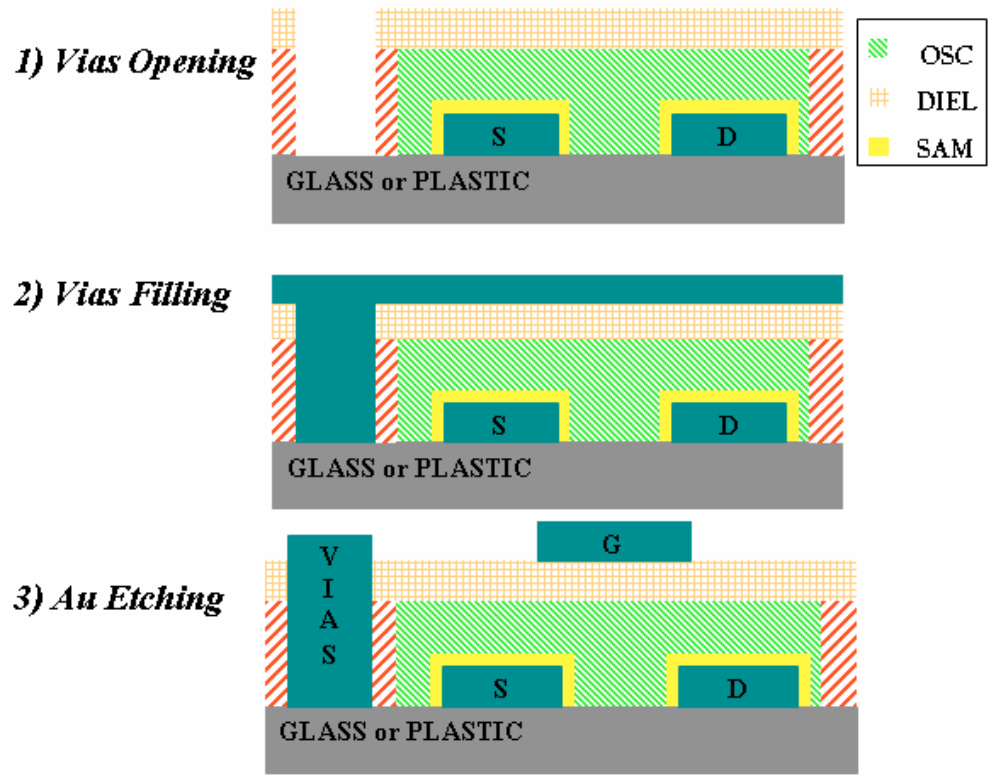

Figure 4.16 Flow-chart steps for vias opening.

By these process steps it is possible to open *vias* and fill them by conductive material. In Figure 4.17 the *vias* filling by PEDOT:PSS is showed, while in Figure 4.18 a final device with Au gate electrodes is reported.

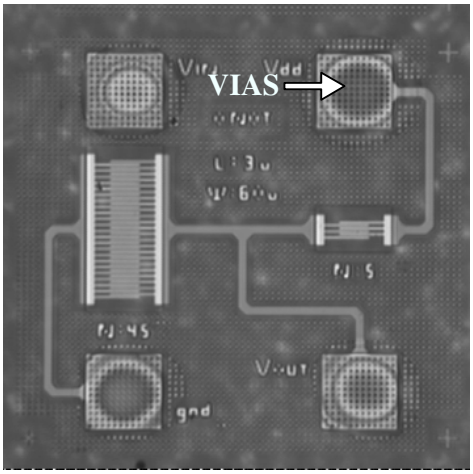

Figure 4.17 Optical image of inverter prototype with *vias* filled by PEDOT:PSS and before Gate electrodes deposition.

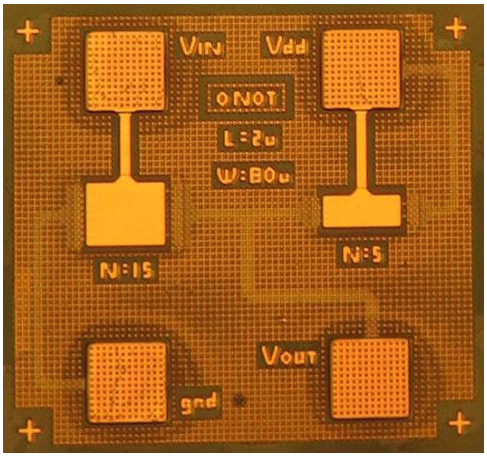

Figure 4.18 Optical image of inverter prototype with *vias* of PEDOT:PSS and gate electrodes of Gold.

On the other hand, in order to minimize the leakage due to undesired current paths through the semiconductor, the adopted solution is to deposit the semiconductor only on the fingers of the Source and Drain electrodes as reported in Figure 4.19.

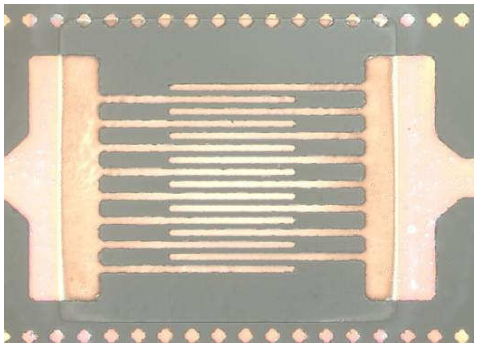

Figure 4.19 Optical image of OS deposited by Inkjet Printing on the fingers of Source and Drain electrodes.

The analysis of conductivity of the OS deposited only on the fingers evidenced low leakages due to the reduced overlapping of the active area with the area out of the channel.

Final remarks

The experimental activity described in this chapter outlined the main steps of the manufacturing process. Devices performances seem to be quite satisfactory and the optimized processing conditions can be adapted also to plastic substrates.

Chapter 5

OTFTs and derivatives on plastic substrates

In this Chapter the experimental work concerning the results on devices fabricated on plastic substrates is reported. In particular, OTFT and more complex circuits have been realized and characterized, as for example inverter and logic adder and multiplexer prototypes.

5.1 OTFT on Plastic substrates

Devices on plastic substrates were realized by the same manufacturing process as described in Chapter 4. The manufacturing process has been implemented and optimized to PEN (polyethylene naphthalate) and PET (polyethylene terephthalate) substrates. The best performances were obtained on planarized PEN substrates supplied by Dupont: an example is shown in Figure 5.1.

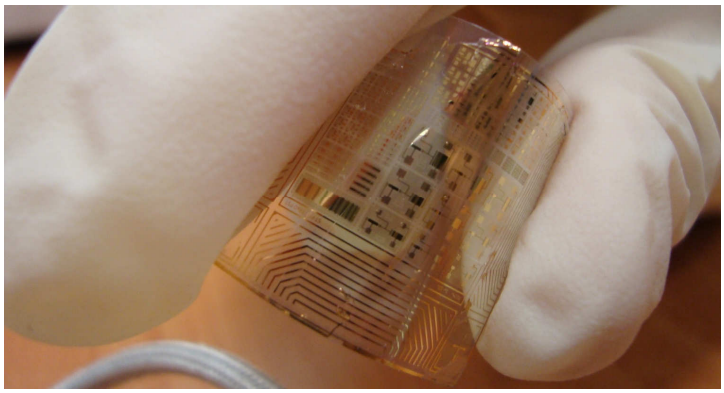

Figure 5.1 OTFT's array deposited on a PEN substrate.

Devices characterized by different sizes have been fabricated with channel lengths, e.g. L, in the range 1÷100 μm and channel widths, e.g. W, in the range 40÷2000 μm. OTFTs samples were characterized by means of the Probe Station (PM5 Karl Suss) for contacting devices and a Parameter Analyzer (4155C Agilent) for measuring the electrical characteristics at normal conditions. The device damage due to the contact between the Probe Station tips and metal electrodes on a soft substrate has been avoided by vacuum locking the plastic substrates on the chuck. As explained in the previous chapters, the electrical properties have been tested by measuring the Transfer and Output characteristics with the Source electrode as ground reference. In Figure 5.2 the Transfer and Output characteristics of a typical device are showed. Surprisingly, the electrical performances detected on plastic devices seem quite comparable to those observed for Glass substrates. Initially, large scale devices, L=100μm, showed promising performances due to high mobility values, close to 0.06 cm^2/Vs, but low I_{on}/I_{off} ratios, close to 50 because of high off currents. The optimization of the manufacturing process and the confined deposition of polymers allowed a reduction of the leakages through the substrate.

Moreover, in order to reduce the off current and to ensure the best off condition, plastic devices were characterized step by step. First of all, the substrate insulation was tested and resistance higher than 10TΩ measured between the Au Source and the Drain electrodes on a PEN substrate: such a resistance corresponds to the bulk PEN resistance. Afterward, the resistance between the two electrodes was measured after each manufacturing step as shown in Figure 5.3. In particular, an increase of one order of magnitude was found after the device was treated by the SAM (Self

Assembled Monolayer) solution, and a more than three orders increase after organic semiconductor deposition by spin-coating.

This step by step characterization allowed us to identify the reasons of limited I_{on}/I_{off} ratios as due to the high conductivity of the semiconductor that introduces a significant OFF current also when the channel is not yet influenced by any Gate voltages.

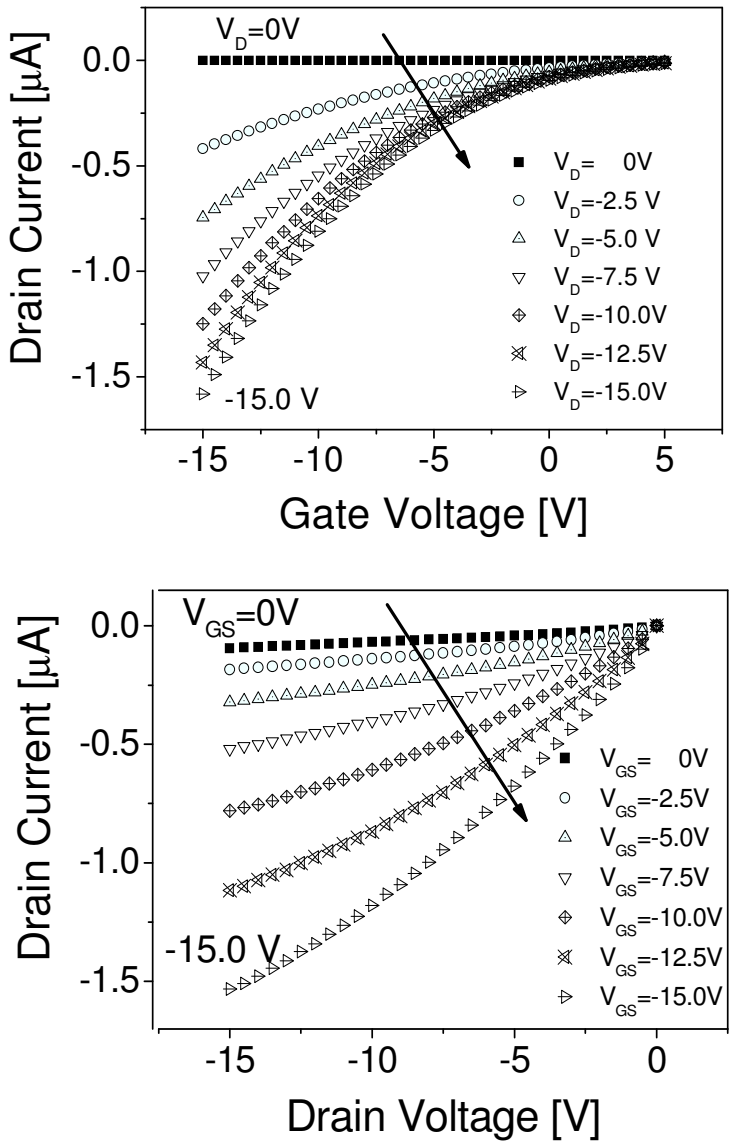

Figure 5.2 Transfer and output characteristics of an OTFT with L=5μm W=100μm deposited on PEN substrate.

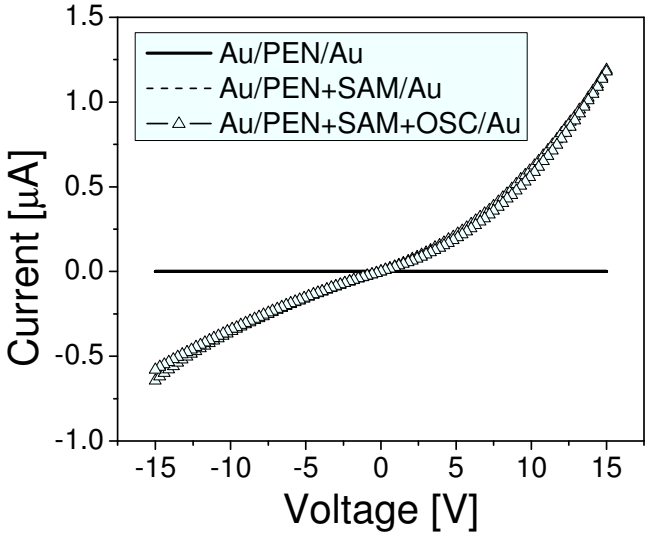

Figure 5.3 Current-Voltage characteristic of Source-Drain channel during the different manufacturing steps.

Moreover, the morphological analysis of devices, performed before the Gate electrode deposition, evidenced the presence of crystalline aggregates in the semiconductor film that destroy the uniformity of the film surface with peaks and defects that can contribute to the device current leakage. Finally, the complete devices were characterized in standard conditions. In Table 5.1 the averaged working parameters obtained from the electrical characterization of devices with different size are reported for comparison.

L [µm]	**I_{Dm}/I_{Doff}**	**µ [cm^2/Vs]**	**V_T [V]**
10	1e3	2e-2	1 V
5	3e2	1.5e-2	3V
3	20	2e-2	2.5

Table 5.2 List of the electrical parameters characterizing the averaged OTFTs performance.

Experimental results evidenced that devices with lower feature sizes were more affected by losses, and this was probably due to the lack of control on the processing

conditions when the resolution size of patterned areas is lower than 5μm. Accordingly, the devices with L=5μm have been selected to realize more complex circuits employing different OTFTs stages.

5.2 Innovative solutions

To optimize the electrical performances of the smaller devices different strategies have been adopted. First of all, different materials have been tested for the electrodes, and the best performances were obtained in the case of Gold. As described in Chapter 4, to obtain the best interfaces coupling with polymeric materials also Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) electrodes were employed. In particular, their use as bottom electrodes has been tested in different geometries to verify the possibility of using this material in the realization of interconnections between different devices. The electrical characterization of long wires and vertical paths allowed us to select the PEDOT:PSS blend as the best polymeric material to realize interconnections, both in planar and vertical configurations. In Figure 5.4 an example of interdigitated Source and Drain electrodes realized by Inkjet Printing of PEDOT:PSS ink (Bytron PJET HC) with a distance between two adjacent lines of 80μm.

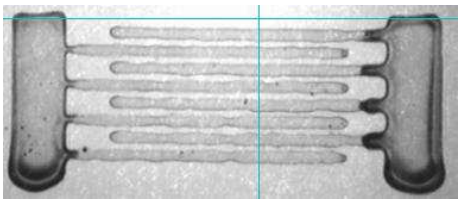

Figure 5.4 Optical image of P Jet HC deposition be IJP.

On the other hand, the use of Micro-Contact Printing has been also successfully tested in fabricating sub-μm devices. Micro-Contact Printing (μCP) is a non-photolithographic method that routinely forms patterned SAMs containing regions terminated by different chemical functionalities with submicron lateral dimensions (see Figure 5.5).

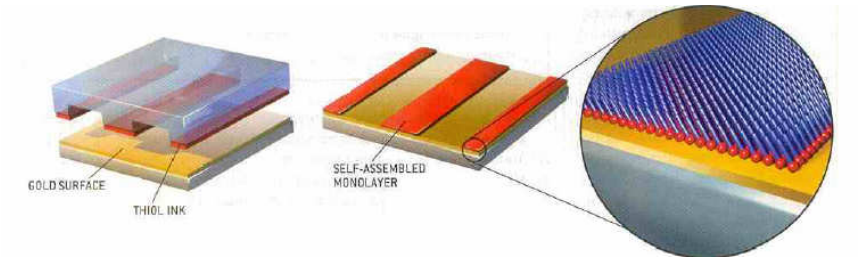

Figure 5.5 Micro Contact Printing [3].

Basically, contact printing allows pattern transfer by conformal contact between a stamp and a substrate. It is an additive process that can be used for patterning large areas. Figure 5.6 shows the flow-chart for a μ-contact process: after replication (1, 2) of a patterned elastomeric stamp from a master, the elastic stamp (3) can be inked with a monolayer-forming ink using either wet inking (4) or contact inking (5). The inked stamp is then used to print (6) a pattern that selectively protects the noble-metal substrate during the subsequent process. Otherwise, after printing, a different SAM can be formed on the underivatized regions by washing the patterned substrate with a dilute solution containing the second molecule. A most used elastomeric stamp is made by Polydimethylsiloxane (PDMS). Figure 5.7 shows one example of the realized electrodes on PEN substrate.

[3] M. Uplaznik, "Review: Introduction to nanotechnology – soft lithography", (2002)

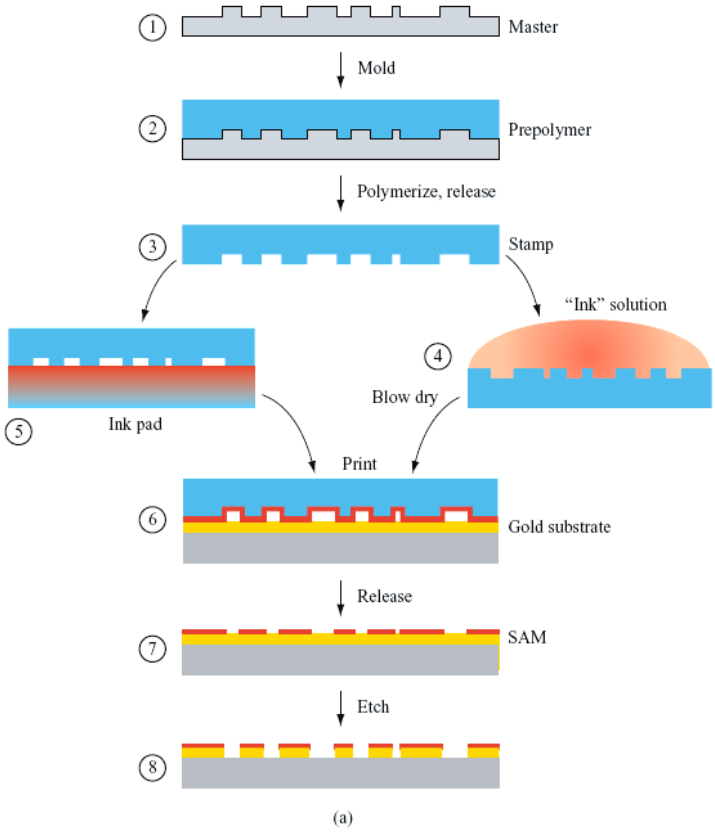

Figure 5.6 Diagram of μ-contact process.

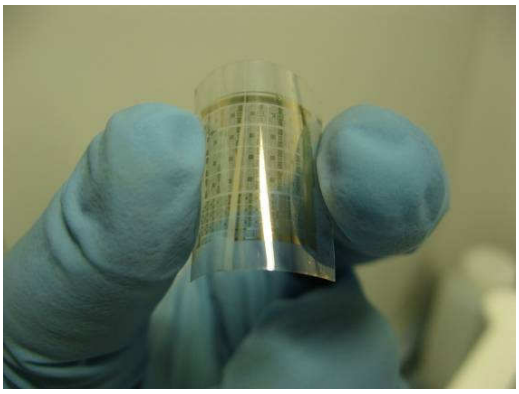

Figure 5.7 Optical image of Gold electrodes deposited by μ-contact printing.

5.3 Plastic Inverter

Reproducing the same process as described in Chapter 4, Inverter prototypes with two OTFTs were fabricated on PEN substrates and characterized. A typical array of Inverter prototypes on PEN substrate is showed in Figure 5.8.

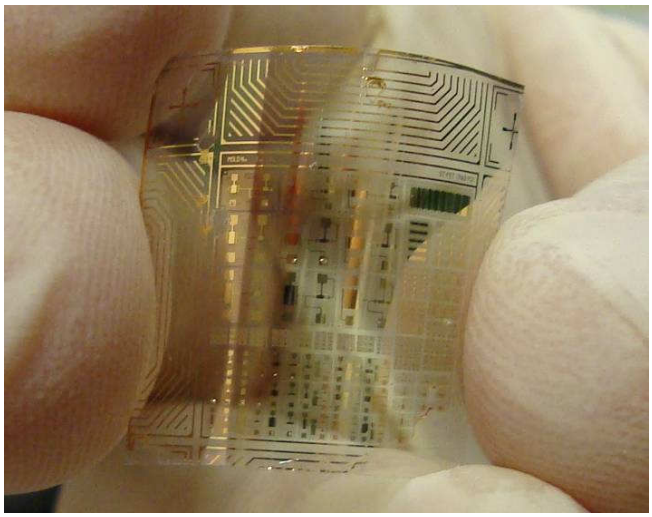

Figure 5.8 Inverters array deposited on PEN substrate.

Firstly, the two OTFTs were separately characterized, and then the Inverter characteristic was measured. Taking in mind that the Inverter is a NOT gate that reverses the input signal value at the device output, i.e. the Drain of the second transistor, an inverter signal is expected. Figure 5.9 shows a typical output characteristic measured on a plastic device.

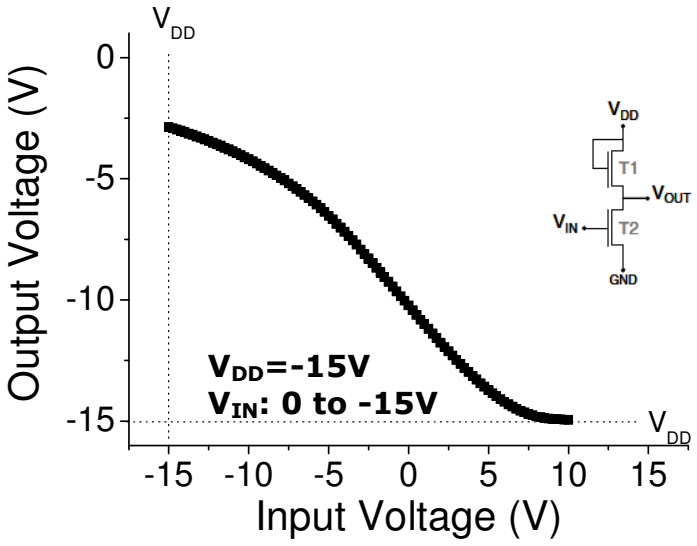

Figure 5.9 Output characteristic of an L=5µm W=300 µm Inverter.

As shown in Figure 5.9, the inverter characteristic is affected by losses that introduce a threshold in the device characteristic. Moreover, plastic devices showed electrical performances similar to the devices on glass together with comparable losses. This result is independent on sizes, with higher losses on L=3µm devices, evidencing that device processing should be yet improved.

5.4 Innovative devices

Based on the performances obtained on L=5µm OTFTs, more complex circuits were developed. The main goal of this activity was the realization of a 4-bit microprocessor made by different blocks: a Logic Unit, a Full Adder and a Multiplexer. The realization of this kind of device is at an earlier stage, so that processing and testing should be yet optimized. Nevertheless, a prototype and its layout are shown in Figure 5.11 and 5.10, respectively. A 4-bit microprocessor requires a large number of OTFTs to be fabricated with a cascade connection, introducing many losses if the layout is

not properly designed. At this first stage, only small parts of different blocks have been tested to verify the interconnections between different parts of the circuits.

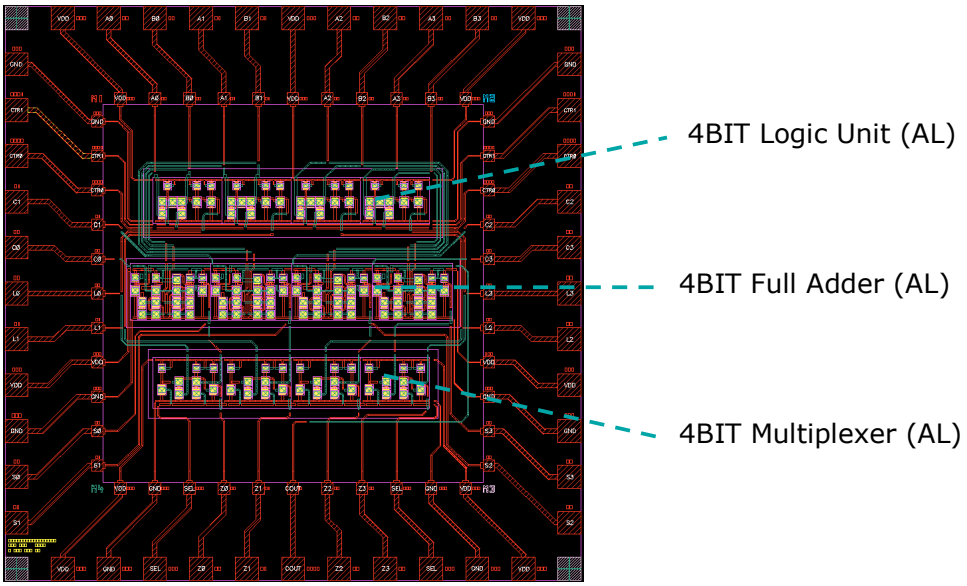

Figure 5.10 Layout of 4BIT blocks.

Figure 5.11 4BIT blocks deposited on PEN substrate.

Final remarks

The experimental activity described in this chapter demonstrates the positive assessment of a technological platform for complex circuits manufacturing by organic materials. Plastic devices performances seem to be quite satisfactory to be employed in more complex circuits even if the road toward this goal is still full of work to be done.

Conclusions

Accomplishments

In summary, the proposed work validates the possibility to realize Organic Thin Film Transistors by using both innovative technologies and advanced organic materials. Organic field effect transistors of micrometric sizes with a Thiophene blend as a polymeric semiconductor and a Fluoro-polymer dielectric have been realised both on glass and plastic substrates. After the optimisation of all the manufacturing processes, the electrical characterization of fabricated devices evidenced good performances in terms of charge mobility, threshold voltage and I_{ON}/I_{OFF} ratio. Moreover, the properties of polymeric electrodes deposited by innovative technologies such as Microcontact Printing and Inkjet Printing have been analysed and validated. The main experimental results have been presented in the last three chapters. In particular, in Chapter 3 the electrical characterization of different polymeric semiconductors in Silicon OTFT templates was presented. Thin films of Pentacene and Thiophene derivatives were characterized in OTFTs structures, by Silicon based templates developed at University of Wurtzburg (DE). Best results were obtained by an experimental Thiophene blend, in terms of mobility ($0.045 cm^2/Vs$), threshold voltage (V_T=-2V), and Ion/Ioff ratio (10^2); then this material has been selected to be employed in the final devices. In Chapter 4 the manufacturing process that allows realising polymeric OTFTs and more complex devices has been described, and the details on the electrical characterization of realised samples on glass substrates reported. OTFTs, with micrometric feature size, based on the Thiophene blend as semiconductor and a Fluoro-polymer as dielectric, were fabricated and characterized. Devices showed very good electrical performances: for example mobility values up to 0.06 cm^2/Vs, and Ion/Ioff ratios close to 10^3. Also the use of polymeric interconnection between different device's layers was described, together with the localised deposition of the polymers by InkJet Printing. Finally, in Chapter 5 the experimental results on the electrical characterization of OTFTs and Inverter

prototypes realised on plastic substrates was described and the first preliminary results on the manufacturing of more complex devices, such a Multiplexer and a Full Adder reported. Devices on plastic substrates exhibited electrical performances comparable to the ones deposited on glass indicating that manufacturing process can be fully adapted to realise all organic and flexible devices. The experimental results of this thesis work gave evidence of the possibility to build up an all-organic technological platform, employing polymeric devices such as OTFTs, memories, logic gates and so on. As a supporting action for this project, a wide experimental activity on innovative materials and devices has also performed, even if it is not completely reported inside the presented text. In fact, the experimental work is part of a much more articulated project aiming to realize a 4-bit microprocessor by using all organic devices.

Future works

While the main objectives of the thesis work were successfully demonstrated there are different tasks that could be conducted to improve devices performances including:

- Realizing and optimizing of polymeric electrodes
- Improving devices' efficiency
- Reducing the Off current
- Improving the performances of OTFTs interconnections

All the aforementioned aspects will represent the basis of future research activity along the organic electronics roadmap. In particular, different advanced devices will be realised, including also all organic resistors, capacitors and memories by employing such innovative technologies. Moreover, the validation of the presented results in more complex devices and circuits together with the analysis of the advantages introduced by plastic electronics will be also a first step through the realization of the all-organic technological platform. On the other hand, the use of innovative technologies to scale-down devices' dimensions should be a next future goal, in line with the requirements of semiconductors industry.