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DOTTORATO DI RICERCA IN INGEGNERIA ELETTRONICA E DELLE TELECOMUNICAZIONI

DESIGN OF POWER/ANALOG/DIGITAL SYSTEMS THROUGH MIXED-LEVEL SIMULATIONS

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To the memory of my father

Quello che ci tocca e così facendo ci indirizza è ciò che ha una applicazione. Sento incombere l'arrivo di un'ondata di grande pulizia, un'imminente precisione che già schiuma a tutti gli angoli del significato. Sento l'odore del cambiamento, di un sollievo pagato a caro prezzo, come l'odore di muffa che preannuncia la pioggia estiva. Una nuova era e una nuova concezione della bellezza come vasta gamma, non come luogo preciso. Basta con i concetti unioggettivi, le contemplazioni, il caldo respiro di trifoglio, i petti ansimanti, la storia come simbolo, i colossi; basta con l'uomo - pugno alla fronte o palmo al décollté - inteso come palpitante, scalpitante, surriscaldata Natura, essa stessa a sua volta immaginata come colorata, dotata di forma, carica di odore, attributrice di significato grazie alle sue qualità. Basta con le qualità. Basta con le metafore. Numeri di Gödel, grammatica svincolata dal contesto, automi finiti, funzioni e spettri di correlazione. Non si tratterà più di essere sensibilmente qui, ma casualmente, efficacemente qui. Qui nella maniera più intima possibile...

"Da una parte e dall'altra"

David Foster Wallace
21/2/1962 – 12/9/2008

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Introduction

I.1 Research Aims and Objectives

In recent years the development of the applications in the field of telecommunications, data processing, control, renewable energy generation, consumer and automotive electronics determined the need for increasingly complex systems, also in shorter time to meet the growing market demand.

The increasing complexity is mainly due to the mixed nature of these systems that must be developed to accommodate the new functionalities and to satisfy the more stringent performance requirements of the emerging applications. This means a more complex design and verification process.

The key to managing the increased design complexity is a structured and integrated design methodology which allows the sharing of different circuit implementations that can be at transistor-level and/or at a higher level. This latter complies with the possibility of using hardware description languages (HDL) such as *Verilog* and *VHDL* for the digital blocks, *VerilogA* (the analog language patterned after *Verilog*) for the analog part and *Verilog-AMS* that combines *Verilog* and *Verilog-A* into an Mixed Signal-HDL that is a super-set of both seed languages.

In order to expedite the mixed systems design process it is necessary to provide: an integrated design methodology; a suitable supporting tool able to manage the entire design process and design complexity and its successive verification. It is essential that the different system blocks (power, analog, digital), described at different level of abstraction, can be co-simulated in the same design context. This capability is referred to as mixed-level simulation and permits to establish that the blocks function as designed in the overall system allowing to verify their effect on the overall performance. Hence, the use of mixed-level simulation dramatically improves the designer ability to verify complex circuits and also reduces the time-to-market.

One of the objectives of this research is to design a mixed system application referred to the control of a coupled step-up dc-dc converter. In this case it is very important that the different system

blocks are developed in an integrated design context. This latter consists of a power stage designed at transistor-level, also including accurate power device models, and the analog controller implemented using *VerilogA* modules. Since digital controllers are becoming very attractive in dc-dc converters for their inherently lower sensitivity to process and parameter variations, programmability, ability to implement sophisticated control schemes, and ease of integration with other digital systems, a digital controller has been also implemented using *VerilogA*-*VerilogAMS* modules. In fact, in the current literature, the research focus has moved to more sophisticated control approaches, where the design of custom integrated digital controllers is presented like a viable solution for the next generation of high performance power supplies.

Thus, in this dissertation it will be presented a detailed design of a Flash Analog-to-Digital Converter (ADC). Generally, an ADC plays a crucial role in mixed system because of its ability to link analog with digital world. The designed ADC provides medium-high resolution associated to high-speed performance. This makes it useful not only for the control application aforementioned but also for applications with huge requirements in terms of speed and signal bandwidth.

The entire design flow of the overall system has been conducted in the Cadence Design Environment that also provides the ability to mixed-level simulations. Furthermore, the technology process used for the ADC design is the IHP BiCMOS 0.25 μm by using 50 *GHz* NPN HBT devices.

This dissertation is a study into integrated circuit design, mixed signal architecture, power electronics design, and control strategy implementation. The study is an attempt to address the ever evolving challenges of integration that affects the mixed-systems design and verification.

I.2 Thesis Organization

This thesis is organized into four chapters.

Subsequent to the Introduction, Chapter 1 presents an overview of the analog-to-digital conversion process. Then, the most relevant ADC performance metrics are reported; their accurate knowledge is fundamental in order to evaluate and to compare the ADCs

performance. Next, a brief description of the most popular ADC topologies is reported, with their advantages and disadvantages. Additionally, the fundamental theoretical limitations to ADC's performances are detailed. Finally, a comparison of different ADC topologies, with an extensive survey of the state-of-the-art, is presented.

Chapter 2 looks at the gateway between analog and digital domain, the ADC. The detailed design of the ADC's basic circuits, and their main specifications, in order to better understand their impact on the overall performances, are presented. Two different architectures of the track-and-hold amplifier are described and designed by using two classical switch topologies: diode-bridge and switched-emitter-follower. Then, an improved bipolar implementation of a clocked comparator is presented. Next, it is described a novel high-speed resistor ladder architecture whose improved performances, in terms of increased speed and reduced non-linearity, when compared to the conventional topology are highlighted. Finally, four ADCs using the Flash topology, and also the Folding/Interpolating, are designed and appropriately tested by using not only the proposed resistor ladder but also the conventional and the one proposed by Kobayashi (i.e. the state-of-the-art for bipolar implementation). Numerical simulation results highlight the effectiveness of the proposed solution in increasing the effective resolution bandwidth (ERB) of the different ADC circuits that have been designed.

Chapter 3 discusses the design of a coupled-inductors step-up dc-dc converter and its benefits with respect to a conventional topology in terms of both voltage gain and efficiency. Then, an efficiency analysis of the converter is presented, providing a detailed analytical model of the power losses. Numerical results are in good agreement with the proposed analytical model showing that the proposed approach is promising for the analytical optimization of converter design.

Chapter 4 presents the implementation and verification of a suitable control strategy for dc-dc converters. The sliding mode control technique, derived from the variable structure systems theory, offers an alternative way to implement a control action which exploits the inherent variable structure nature of dc-dc converters. This chapter also presents the various aspects concerning the sliding mode controller, which includes the choice of state space variables and

sliding surface, the existence properties and the selection of the control parameters.

Moreover, a constrained optimization problem is formulated in order to derive from a single algorithm the characteristic parameters of both coupled-inductor converter and sliding surface for guaranteeing the stability requirements, even in presence of large load variations.

Furthermore, the implementation of both analog and digital controllers in high-level modules, using hardware description language, is described. Finally, the full system derived from a single design flow, including power, analog, digital circuits is verified through mixed-level simulations, in order to confirm the validity of the proposed converter analysis and design methodology. Numerical simulation results confirm the good performance of the analog and digital controller and makes promising the use of IC ADC developed in this work.

Finally, the conclusions of this work are drawn, and the possibility of future work ensuing this dissertation is discussed.

Chapter 1

Analog to Digital Converter (ADC)

Analog-to-digital converters (ADCs) provide the gateway between analog domain and digital world [1]. ADCs translate analog quantities, which are characteristic of most phenomena in the "real world," to digital language, used in information processing, computing, data transmission, and control systems [2]. The relationships between inputs and outputs ADC's are shown in Fig. 1.1.

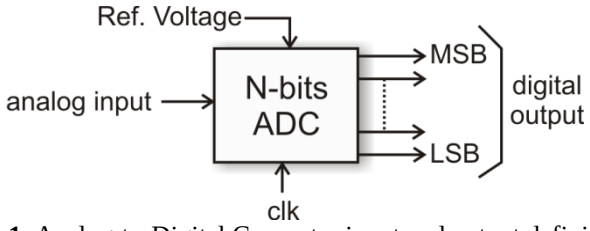

Fig. 1.1. Analog-to-Digital Converter input and output definitions.

A data converter performs a transformation of signals: from continuous-time and continuous-amplitude to discrete-time and quantized-amplitude [3]. Hence, a basic operation of the ADC is described by the four elementary blocks in Fig. 1.2. The analog input is firstly filtered to avoid aliasing, then the filter output is sampled, producing a discrete-time signal. The amplitude of this last signal is quantized with a level selected from a set of fixed references, thus generating a quantized-amplitude signal. Next, a digital representation of that level is available to the output.

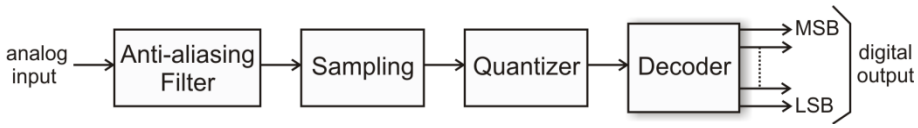

Fig. 1.2. Block diagram of the basic functions of an ADC.

Hence, an ADC produces a digital output as a function of the analog input. The input can assume an infinite number of values,

while the output is selected from only a finite set of codes depending on the converter's output word length (the ADC's resolution).

1.1 Sampling

A sampler transforms a continuous-time signal into its sampled-data equivalent. An ideal sampler yields a sequence of delta functions whose amplitude equals the signal at the sampling times. For ideal uniform sampling with period T_s the output of a sampler is

$$x_s(t) = x_s(nT_s) = \sum_{n=-\infty}^{n=+\infty} x(t)\delta(t - nT_s) \tag{1.1}$$

Eq.(1.1) is the mathematical description of the sampled signal and outlines the inherent non-linearity of the sampling process (the input is multiplied by an impulse train). So, as shown in Fig. 1.3, sampling a signal is equivalent to the mixing of the signal with a train of deltas [3].

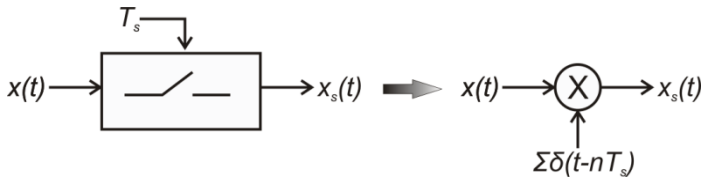

Fig. 1.3. Ideal sampler and its non-linear equivalent processing.

The pulses represent the input only at the exact sampling times (nT_s) as shown in Fig. 1.4.

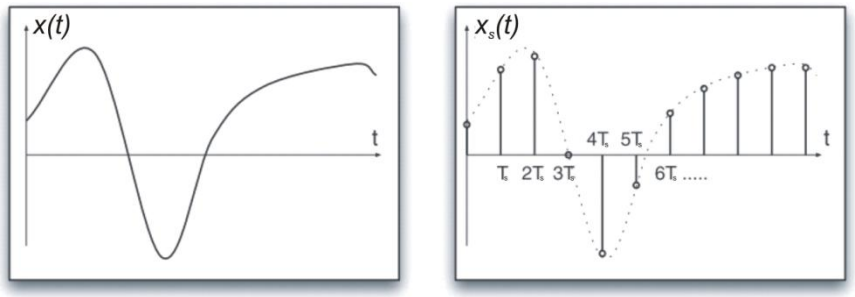

Fig. 1.4. Continuous time signal (left) and its sampled data representation (right).

Moreover, using the description of the sampling signal in the frequency domain, the time sequence of samples $x_s(t)$ of the continuous function $x(t)$ is described in the frequency domain as $X_s(f)$:

$$X_s(f) = \frac{1}{T_s}\sum_{k=-\infty}^{k=+\infty} X(f - \frac{k}{T_s}) = \frac{1}{T_s}\sum_{k=-\infty}^{k=+\infty} X(f - kf_s) \qquad (1.2)$$

A band-limited (f_B is referred as signal bandwidth, BW) input signal is connected to only one spectrum band in the frequency domain $X(f)$ as shown in Fig. 1.5.a. By sampling this signal with a sequence of Dirac-pulses with a repetition rate ($f_s = 1/T_s$) a number of replica of the original spectral band $X(f)$ are created on either side of each multiple of the sampling rate f_s (Fig. 1.5.b). Note that from one input spectrum a set of infinite spectra is created so disclosing once more the non-linearity of the sampling operation.

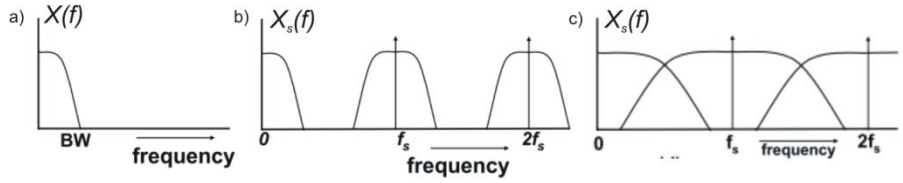

Fig. 1.5. a) Analog signal and **b), c)** its sampled version in the frequency domain.

A significant target is the possibility to recovery the original continuous-time input signal from his sampled version without loss of information.

Assume that the spectrum of the input signal is the one of Fig. 1.5.a, while the sampled spectrum is shown in Fig. 1.5.b.

Half the sampling frequency, $f_s/2=1/2T_s$, is often named the Nyquist frequency. The frequency interval $[0, f_s/2]$ is referred to as the Nyquist band (or band-base) while frequency intervals, $[f_s/2, f_s]$, $[f_s, 3f_s/2]$, are named the second and third Nyquist zones, and so forth. Since the spectrum in all Nyquist zones is the same it is sufficient to focus only on the band-base, $[0, f_s/2]$. When bilateral spectra are considered the frequency range of interest at becomes $[-f_s/2, f_s/2]$.

If the sampling frequency is at least twice the signal bandwidth, $f_s>2f_B$, then the scaled replicas of $X(f)$ shifted by the multiples of f_s will not overlap (Fig. 1.5.b), so assuring an accurate representation of the original analog signal through a low-pass filtering action.

If the sampling frequency is lower than twice the signal bandwidth, then the replicas of $X(f)$ will partially overlap and modify the resulting spectrum, as shown in Fig. 1.5.c. This is the well-known phenomenon called "aliasing". A bandwidth larger than half of the sample rate will cause the alias-band to mix up with the base band, so it is no more possible to reconstruct uniquely the original signal.

The limitation on the value of the sampling frequency is known as the "Nyquist criterion":

"If a function contains no frequencies higher than BW cycles per second, it is completely determined by giving its ordinates at a series of points spaced 1/2 BW seconds apart" [4].

As beforehand, the mathematical relation between signal bandwidth f_B and sampling rate f_s resulting from the "Nyquist criterion" is:

$$f_s > 2 f_B \tag{1.3}$$

Eq. (1.3) outlines that the signal bandwidth is limited by the sample rate. Furthermore, it is possible to consider a sampled signal band that is entirely located in a higher Nyquist zone (see Fig. 1.6). If this sampled signal band is bounded inside one of the Nyquist zones, the various spectrum replicas do not overlap one another.

Thus, the sampled signal frequencies may lie in any unique Nyquist zone, and the image falling into the first Nyquist zone is still an accurate representation of the original signal (with the exception of the frequency reversal that occurs when the signals are located in even Nyquist zones).

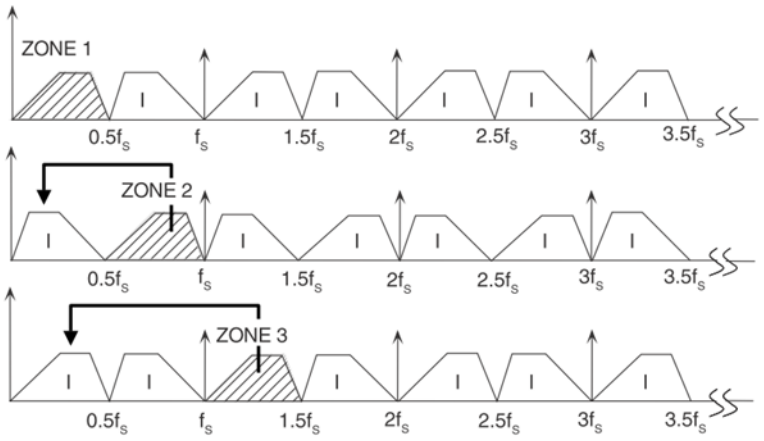

Fig. 1.6. Frequency translation between Nyquist zones.

The property that also a frequency range above the sample rate is properly sampled and generates copies around all multiples of the sample rate, is in some communication systems used to down-modulate or down-sample signals. This technique is normally used to bring high-frequency spectra into the band-base and this method is also known as under-sampling, harmonic sampling, IF sampling. Finally, it can be stated a new version of the "Nyquist criterion":

"A signal must be sampled at a rate equal to or greater than twice its bandwidth in order to preserve all the information content."

It is worth to highlight that there is no constraint on the absolute location of the band of sampled signal within the frequency spectrum relative to the sampling frequency. The only constraint is that the band of sampled signal be restrict to a single Nyquist zone, so avoiding the replicas overlap.

In conclusion, the extended "Nyquist criterion" only forces the input signal to be band-limited and strictly enclosed in a single Nyquist zone. Therefore, an ADC is preceded by a band-limiting filter: the anti-aliasing filter. This filter prevents the components outside the desired frequency range to be sampled and to mix up with the signals. This condition must be verified not only for the signal, but also for noise and interferences. Noise has an unpredictable spectrum and can have components at any frequency. The same is true for interferences. Therefore, it is necessary to remove out of band interferences whose folding would corrupt the signal band. A filter

action effected before the sample action achieves this result. The frequency response of the filter should not modify the signal band and reject the out-of-band interferences.

An implicit assumption for the Nyquist criterion is that the bandwidth of interest is filled with relevant information.

1.2 Quantization

A quantizer converts a sampled data signal from continuous level to discrete level. In particular, the quantizer converts a continuous range of input amplitude levels into a finite set of discrete digital code words. Thus, the ADC must approximate each input level with one of these codes. Firstly, it is generated a finite set of reference levels corresponding to each code, then the input signal is compared with each reference, next it is selected the reference (and the corresponding code) closest to the input level.

Fig. 1.7.a depicts the ideal 3-bits ADC input/output characteristic. The transfer characteristic therefore consists of eight horizontal steps. The quantizing process means that a straight line representing the relationship between the input and the output of a linear analog system is replaced by a transfer characteristic that is staircase-like.

The dynamic range of the quantizer is divided into a number of equal quantization intervals (uniform quantization), each of which is represented by a given analog amplitude. The quantizer modifies the input amplitude into a value that represents which quantization interval it resides in. Often the value representing a quantization interval is the mid-point of the interval. In this case, the output is assigned to a discrete value selected from a finite set of representation levels aligned with the treads of the staircase. In Fig. 1.7.a is shown the transfer characteristic of uniform quantizer for mid-tread type.

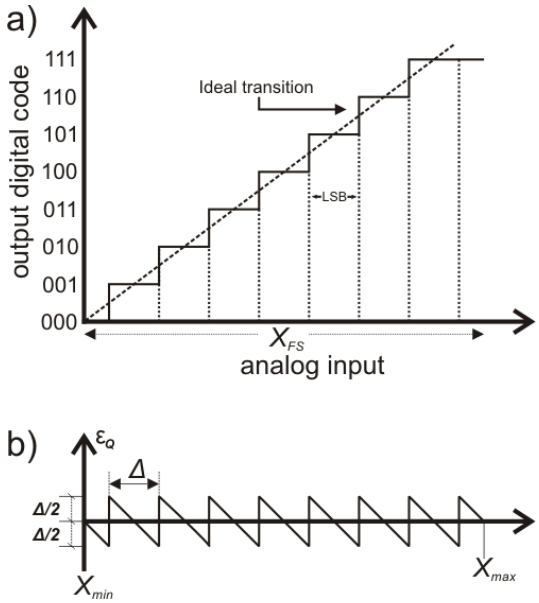

Fig. 1.7. a) Ideal input-output characteristics for a 3-bit quantizer. b) Quantization error for a 3-bit quantizer.

The range of the quantizer is $X_{FS}=X_{max}-X_{min}$, the analog full-scale. Assuming M as the number of representation levels, it can be defined the quantization step $\Delta = X_{FS}/M$. This last is the separation between the decision thresholds (separation between the representation levels).

Usually, the number of levels is a power of the base number "2". The power N is the resolution of a conversion, and defines the number of levels to which an amplitude continuous signal can be rounded as 2^N.

The step $\Delta = X_{FS}/2^N$ is the Least Significant Bit (LSB). It means that the LSB of the digital output code changes when the analog input changes by $X_{FS}/2^N$.

The ideal ADC transitions take place at *1/2* LSB above zero (Fig. 1.7.a), and thereafter every LSB, until *1/2* LSB below analog full-scale. Since the analog input to an ADC can take any value, but the digital output is quantized, there may be a difference of up to *1/2* LSB between the actual analog input and the exact value of the digital output. This difference is called "quantization error" and is denoted here as ε_Q. The quantization error spans from $-\Delta/2$ to $+\Delta/2$ (Fig. 1.7.b), while outside the input dynamic range the output of the quantizer saturates to the two bounds and the quantization error

increases linearly in the positive or negative direction. Moreover, this error decreases as the resolution increases and its effect can be studied as an additive noise viewed at the output assuming that ε_Q is a random variable uniformly distributed between $-\Delta/2$ and $+\Delta/2$ (eq. (1.4)), and not correlated to the analog input [1]-[3].

$$p(\varepsilon_Q) = \begin{cases} 1/\Delta & if\ \varepsilon_Q \in (-\Delta/2, +\Delta/2) \\ 0 & otherwise \end{cases} \tag{1.4}$$

According to the above statement, even an ideal analog to digital conversion introduces a noise due to the quantization process. The power associated with this quantization noise is a fundamental limit to the quality of the process of analog-to-digital conversion. The impact of this error on the conversion can be stated by calculating the quantization noise power

$$P_Q = \int_{-\infty}^{+\infty} \varepsilon_Q^2 p(\varepsilon_Q) d\varepsilon_Q = \int_{-\Delta/2}^{+\Delta/2} \frac{\varepsilon_Q^2}{\Delta} d\varepsilon_Q = \frac{\Delta^2}{12} \tag{1.5}$$

since $\Delta = X_{FS}/2^N$, it can be written

$$P_Q = \frac{X_{FS}^2}{12 \cdot 2^{2N}} \tag{1.6}$$

The power of the quantization noise decreases when the number of bits increases. Ideally, the quantization error goes to zero when the number of bits goes up to infinite.

1.3 ADC performance metrics

The design of an ADC requires an accurate knowledge of its specifications since a large set of parameters describe the features of the static and dynamic operation of an ADC.

Therefore, in the following it will be defined a number of the fundamental metrics most frequently used for testing the ADCs.

1.3.1 Static Specifications

The input- output characteristic represents the static behavior of an ADC, and in the ideal case, as shown in Fig. 1.7, is a staircase with steps uniformly distributed over the input dynamic range of the converter. An actual transfer characteristic (Fig. 1.8) shows deviations from the ideal transfer characteristic resulting in a distorted response.

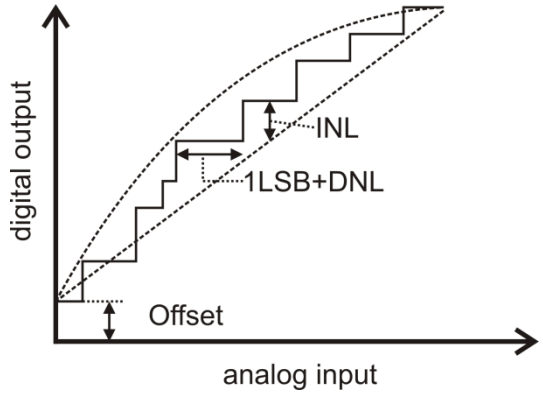

Fig. 1.8. Static ADC's metrics.

The following definitions describe the static behavior of ADC.

- *Offset*: the offset is a shift for zero input or rather a shift from zero of the actual transfer characteristic with respect the ideal one. The offset can be measured in LSB, absolute value (volts or amperes) or as % of full-scale.
- *Gain*: the gain error is the amount by which the slope of the straight line through the transfer characteristic deviates from the ideal value equal to 1.

Linearity error refers to the deviation of the actual threshold levels from their ideal values after offset and gain errors have been removed.

- *Differential Non-Linearity (DNL)*: the *DNL* error is the deviation of the actual step size from the ideal one (LSB size). Assuming that X_k is the transition point between successive codes $k-1$ and k, then the width of the bin k is $\Delta_r(k) = (X_{k+1} - X_k)$; the differential non-linearity is

$$DNL(k) = \frac{\Delta_r(k) - \Delta}{\Delta} \tag{1.7}$$

The maximum value of DNL characterizes the differential non-linearity error of the ADC. This error is the maximum deviation, on the analog input axis, in the difference between two consecutive code transitions and the ideal width of 1 LSB.

- *Integral Non-Linearity (INL)*: the *INL* error is the measure of the deviation of the actual ADC's transfer characteristic from a straight line passing through its end points (endpoint-fit line). It can be write [3]:

$$INL(k) = (1+G)\sum_{i=1}^{k} DNL(i) \tag{1.8}$$

where *G* is the gain error.

The overall plot is called *INL* profile. The maximum value of *INL* curve characterizes the integral non-linearity error of the ADC. When the *INL* is less than ±*0.5*LSB, the converter behavior is monotonic. This last condition guarantees that no missing codes will be present in the conversion process [5]. Both the *INL* and the *DNL* can be measured in LSB, absolute value (volts or amperes) or as % of full-scale.

1.3.2 Dynamic Specifications

Dynamic converter parameters provide information regarding noise, distortion, dynamic linearity, etc. These parameters depend on both signal frequency and amplitude, thus they are usually obtained with a full-scale input signal. The following metrics are the principal terms used to determine the dynamic behavior of the converter.

- *Signal-to-Noise Ratio (SNR)*: the *SNR* is the ratio of the signal power to the noise power (noise produced by the quantization error and the noise of circuit). It can be expressed in decibel (dB) as

$$SNR_{dB} = 10\log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) \tag{1.9}$$

Usually the *SNR* is measured for a sinusoidal input. Assuming that the maximum signal amplitude is equal to half the full-scale ($X_{FS}/2$) over the entire analog range (X_{FS}):

$$P_{signal} = \frac{1}{T_s}\int_0^{T_s} \frac{X_{FS}^2}{4}\sin^2(2\pi f_s t)dt = \frac{X_{FS}^2}{8} = \frac{(\Delta \cdot 2^N)^2}{8} \qquad (1.10)$$

If the noise source is the inherent quantization noise, recalling eq.(1.6), (1.10), eq.(1.9) can be easily rewritten in the theoretical formula

$$SNR_{dB} = (6.02N + 1.76)dB \qquad (1.11)$$

This last represents a fundamental relation between the maximum reachable *SNR* and the number of bits of the quantizer. In other words, the maximum *SNR* represented by a digital word of *N* bits is *(6.02·N+1.76)dB*.

It's clear that for every added bit (corresponding to a doubling of the number of quantization levels), the *SNR* increases of *6.02dB* while the quantization noise power decrease of a factor *4*.

- *Total Harmonic Distortion (THD)*: the *n-th* component HD_n is equal to the ratio between the component at frequency $n \cdot f$ and the fundamental at frequency *f*. Thus, it can be defined the *THD* as

$$THD = \sqrt{\sum_n HD_n^2} \qquad (1.12)$$

the total harmonic distortion describes the degradation of the signal-to-distortion ratio caused by the harmonic distortion. It is usually expressed in dB.

- *Signal-to-Noise and Distortion Ratio (SNDR)*: the *SNDR* is the ratio of the signal power to the total error power including all spurs and harmonics. It is usually expressed in dB.
- *Spurious Free Dynamic Range (SFDR)*: the *SFDR* is the ratio between the signal fundamental component power and the largest spurious component power, within a certain frequency band. It takes into account an information similar to the *THD*, but with attention to the worst tone.
- *Effective Number Of Bits (ENOB)*: the *ENOB* can be easily obtained by reversing eq. (1.11) in which the *SNR* is replaced with the *SNDR*:

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \qquad (1.13)$$

The *ENOB* allows an easy comparison of the real performance of the converters.

- *Effective Resolution Bandwidth (ERB)*: the *ERB* is the maximum analog input bandwidth at which the *SNDR* degrades of 3 dB, or equivalently at which the *ENOB* degrades of 0.5 LSB, with respect to its low frequency value. As a consequence, the *ERB* is a measure of the maximum analog input bandwidth that the converter can handle without a significant degradation of its performances.
- *Figure of Merit (FoM)*: the *FoM* was introduced to take into account the power dissipation, the resolution and the sampling frequency of a converter. In other words, it would be a parameter useful to measure the "power efficiency" of an ADC. A formulation was suggested in [6]

$$F = \frac{2^{ENOB} f_s}{P_D} \tag{1.14}$$

where Walden introduces the *ENOB* instead of the stated number of bits as before (P_D is the power dissipation). Walden's figure of merit correctly includes the performance limitation of signal-to-noise-and-distortion ratio (*SNDR*), but in most applications, A/D converters are expected to faithfully convert all input-signal frequencies below the Nyquist frequency (one half of the sampling rate f_s), but many ADCs exhibit severe degradation of *SNDR* at frequencies well below the Nyquist frequency. For this reason, the literature has recently started using the *ERB* instead of the sampling rate in the equation for the figure of merit [7], [8]. This new figure of merit is

$$FoM = \frac{P_D}{2^{ENOB} 2ERB} \tag{1.15}$$

which represents energy for conversion step and it is usually expressed in *pJ/conv-step*. Generally, effective solution shows a *FoM* below *1 pJ/conv-step*.

1.4 ADC's architectures

There are several well-known ADC architectures with different properties making them more or less suitable for a certain application. To choose the proper architecture, in the following only a brief description of the most popular topologies will be reported.

1.4.1 Flash ADC

The flash circuit topology is conceptually the simplest one. In fact, an analog-to-digital converter must identify the quantization interval that contains the input signal and a direct way to achieve this operation is to compare the input signal with all the transition points between adjacent quantization intervals.

The circuit (for a generic N bits converter) consists of 2^N-1 comparators, a resistor ladder of 2^N segments, and an encoder (see Fig. 1.9). For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a "0" logic output. The 2^N-1 comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code is sometimes called a thermometer code.

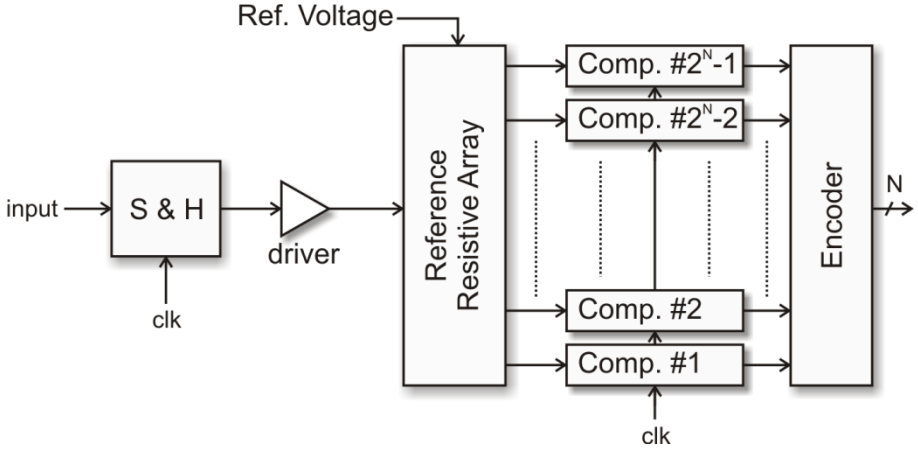

Fig. 1.9. Basic block diagram of N-bits Flash ADC.

The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input. This last consideration emphasizes the parallel nature and the one-step operation of the flash converter, whose name comes from the fact that the output is available in just one clock cycle, like a "flash".

It follows from the above discussion that a full-flash architecture has the advantage of inherently good high frequency behavior.

The main drawback is the increase of complexity with the resolution. In fact, the number of comparators increases exponentially with resolution, and as a consequence increasing power dissipation and area occupation. Other drawbacks such as large non linear input capacitance, dc and ac deviation of the reference voltages generated by the ladder, etc can occur due to the extreme parallelism.

1.4.2 Two-step and sub-ranging ADC

The two-step and sub-ranging (Fig. 1.10) circuits (see also [9], [10]) provide a more relaxed trade-off between power, area, input capacitance with respect to a flash configuration, because they use a smaller number of comparators. Thus, multi-step topologies can be useful to achieve higher resolution.

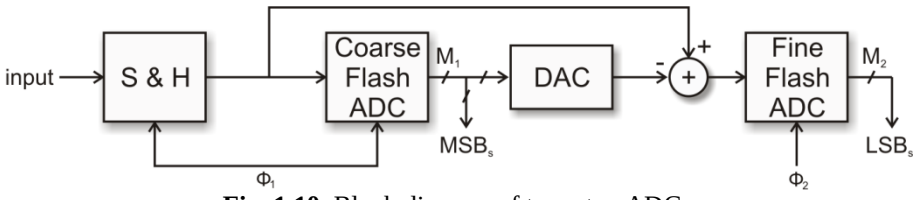

Fig. 1.10. Block diagram of two-step ADC.

Fig. 1.10 shows the block scheme of a sub-ranging or a two-step architecture. It uses a sample-and-hold at the input to drive an M_1 bits flash ADC which estimates the MSBs (coarse conversion). The DAC then converts the M_1 bits back to an analog signal which is subtracted from the held input to give the coarse quantization error (also called the residue). Next, the residue is converted into digital code by a second M_2 bits flash ADC which yields the LSB (fine conversion). The digital logic combines coarse and fine results to obtain the $N=M_1+M_2$ bits output. The difference between the two systems is that in

sub-ranging fashion no gain stage (gain equal to 1) is used between first and second converter.

It could be noted that in two-step and sub-ranging converters the number of comparators is much smaller than a flash converter. In fact, if we consider $M_1 = M_2$, then the number of comparators is $2(2^{M1}-1) << 2^N-1$.

The drawback of these topologies is the need of more than one step (one clock cycle) to complete the conversion, so determining a reduced speed.

1.4.3 Pipelined ADC

A variant of multi-stage ADC is the one that uses a pipeline technique [1]. In Fig. 1.11 a block diagram of general pipeline architecture is presented. Each stage includes an ADC and an arithmetic unit called the multiplying digital-to-analog converter (MDAC) that performs a sample-and-hold (S/H) operation, coarse D/A conversion, subtraction, and amplification.

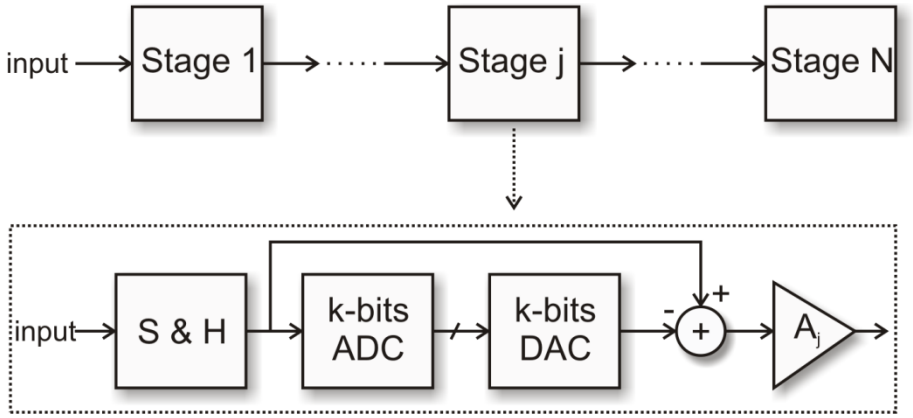

Fig. 1.11. Block diagram of pipelined ADC.

Usually, each stage performs a 1-bit conversion. Thus, a pipeline converter can be seen as the extreme form of sub-ranging, where the number of bits per subrange is reduced to just one. Thus, typically, a pipeline *N* bits converter has *N* stages. However, the number of bits at each stage can differ from one depending on design trade-offs. In fact, the pipeline can also generate multiple bits per stage [12], and the total

resolution of the pipeline architecture is given by the sum of the bits at each stage.

From the above discussion, it is clear that the main advantage of pipeline configuration is the possible increase of resolution paid with a greater latency (associated with the output data).

1.4.4 Folding/Interpolating ADC

Better performances than full-flash topology can be achieved by using folding/interpolating technique [13]-[22]. This technique alleviates the problems of flash configuration (large area, high power dissipation), while maintaining the one-step nature of flash converter.

Fig. 1.12 shows a standard block diagram of a folding ADC. It consists of a parallel operating coarse flash converter and a fine flash converter. The coarse flash converter directly quantizes the input signal, whereas the fine flash converter is preceded by the analog folding preprocessing (folder circuit).

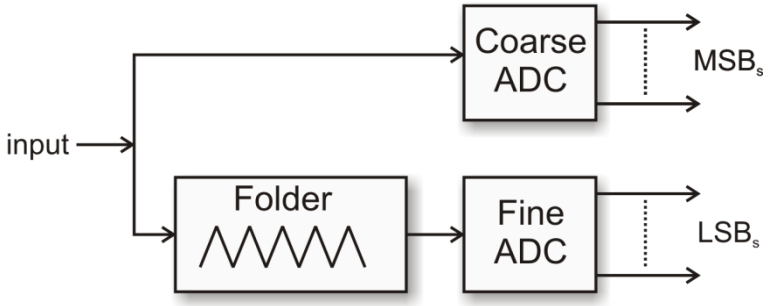

Fig. 1.12. Block diagram of Folding ADC.

The folding architecture can be considered as an evolution of flash and two-step architectures. In a two-step the signal conversion is split into two or more clock cycles, while in a folding converter, the signal conversion consists of a coarse and a fine conversion stage, but these conversions are conducted in parallel. This gives a folding ADC the same maximum clock frequency that can be achieved with full-flash ADC.

The total resolution of the folding ADC is $N = N_{MSB} + N_{LSB}$, where N_{MSB} and N_{LSB} are the numbers of bits resolved in coarse and fine quantizers, respectively. This partitioning reduces the total

number of comparators. An ADC that employs the folding technique only requires $2^N/FF$ comparators where *FF* is the number of folds in each folding signal (folding factor) or rather the number of zero-crossing for each folder.

The basic function performed by the folder is the conversion of the input signal into a number of sinusoid-like output signals. Each folding amplifier generates a number *FF* of zero-crossings, equidistantly spaced over the input range. The polarity of the output signal changes each time the input voltage reaches a reference voltage value. In this way, the input signal is "folded" at each reference voltage. Thus, only the signs of the folding signals are used to determine the value of the least significant bits. To ensure that the ADC achieves the required resolution, accurate zero-crossing points must be generated by the folding circuits.

It is obvious that if the input signal goes from zero to full-scale, the output goes from minimum to maximum *FF* times. Thus, the output frequency of the folder is *FF* times the input frequency. Consequently, a high folding factor results in a reduced number of comparators, but it lowers the maximum input frequency of the converter. Thus, the choice of the degree of folding is a tradeoff between the reduction in the number of comparators and the increased speed of the folding signals.

The folding amplifier is frequently built with differential pair in an wired-OR configuration [1] and higher performance are achieved in fully-differential structure.

In order to reduce the amount of input circuitry, interpolation can be performed between the folding signals. The reduction in the input circuitry is equal to the interpolation factor (*I*), or the number of interpolations.

Interpolation is employed to generate large quantity of folding waveforms. Folding A/D converters utilizing interpolation are called folding/interpolating ADC (Fig. 1.13).

The interpolation technique can be used in a folding architecture by allowing multiple interpolators to take the place of the fine flash converter. The most common and simpler interpolation technique is based on resistive voltage division.

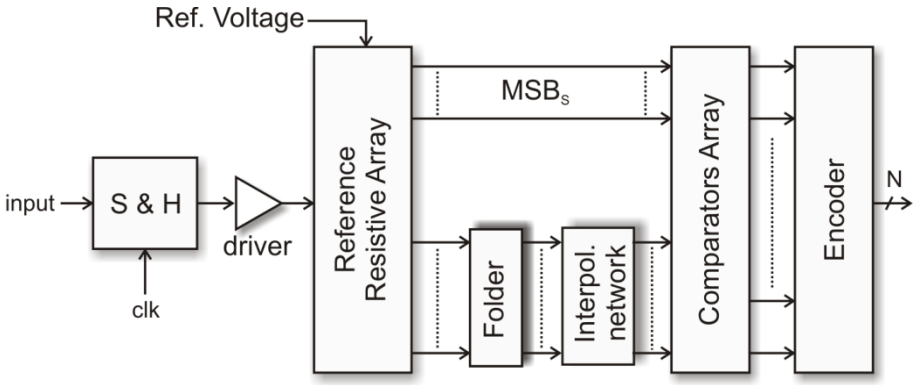

Fig. 1.13. Block diagram of Folding/Interpolating ADC.

It is important that the shape of the sinusoid-like folded waveforms must exhibit high linearity around the zero-crossing points because linear interpolation between two adjacent folding signals is necessary. In fact, the linear portion of two interpolating folding waveforms must extend to the zero crossing point of each other to avoid error in the interpolated folding waveforms. The interpolatable region is half of the linear region of folding waveforms.

It is important to have the zero crossings midway between the two zero crossings of the generating signals.

The interpolation can be implemented using a resistive string because of its simplicity and power efficiency. Moreover, differential interpolation, applying the differential outputs of the folding amplifiers to a differential resistive strings, improves the accuracy of the converter.

The advantage of interpolation in a folding converter is the reduced number of folding signals because deriving the needed further folding signals by interpolation itself.

As an example, assume an *N*-bits converter. Suppose that it has chosen to obtain the *K* MSB and the residue (*N-K)* LSB by employing a coarse flash ADC and a folding/interpolating circuit, respectively. Then, a number of folders $NF=2^K/I$ is necessary. It is clear that the number of folders is reduced by a factor *I* with respect to a conventional folding technique. Each folder has a number of reference voltages equal to $FF=2^N/(I \cdot NF)$ and distant from each other V_{FS} $I \cdot NF/2^N$.

In conclusions, by using folding technique an ADC can be designed in which each comparator detects the zero transitions of the input signal through a number of quantization levels, thus reducing the total number of comparators required for a given resolution.

The number of comparators is reduced by the number of times (*FF*) that the input signal is folded by the folding stages. However, each comparator requires its own folding signal, and each folding signal requires as many folding stages as the number of times the signal has been folded. The more efficient use of comparators is therefore offset by an increasing number of folders in a standard folding system. The number of folding stages can be reduced by interpolating between the outputs of folding stages to generate additional folding signals without the need for more folding stages. The interpolation stage in this way reduces the number of folding stages by the interpolation factor [23]. Thus, the folding/interpolating architecture results in a more compact low-power system than flash configuration.

1.4.5 Time-interleaved ADC

Time-interleaved techniques increase the conversion rate of an ADC by using a number of converters working in parallel for a simultaneous quantization of input samples [1], [3], [24]-[29]. A suitable combination of the results makes the operation equivalent to a single converter whose speed has been increased by a factor equal to the number of parallel elements.

Fig. 1.14 shows a general block diagram of a time-interleaved architecture. It consists of N ADCs of K bits in parallel, an analog demultiplexer at the input side, and a digital multiplexer at the output. Thus, the overall sampling frequency is f_s while each channel (sub-ADC) operates at a frequency equal to f_s/N.

During operation, the analog demultiplexer selects each channel in turn to process the analog input signal. The corresponding digital multiplexer selects the digital output of the selected channel and forms an effectively high-speed ADC.

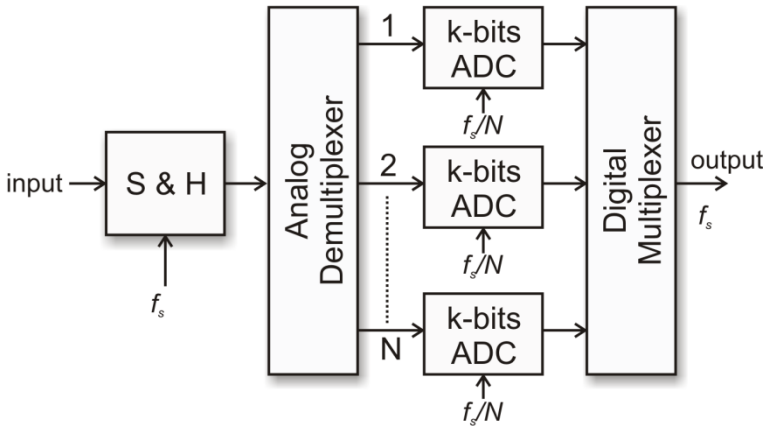

Fig. 1.14. Block diagram of Time-interleaved ADC.

An advantage of this structure is that the overall sampling rate increases by a factor of *N*.

The main drawback is that the performance of time-interleaved ADCs is sensitive to mismatches (offset, gain) among the channels.

1.5 Limitations to ADC's performances

In addition to the quantization noise, the fundamental theoretical limitations to ADC performances are:

- Sampling time jitter
- Thermal noise
- Comparator ambiguity
- Heisenberg uncertainty principle

1.5.1 Sampling time jitter

In Section 1.1 it has been assumed that the sampling process was ideal. As a consequence, the sampled-data signal reproduces the input at the exact sampling-times. In real operation, sampling is affected by uncertainty in the clock. Also, the delay between the logic that generates the sampling phase and the effective sampling is in some

extent unpredictable. The combination of the two effects determines jitter in the actual sampling instants (see Fig. 1.15).

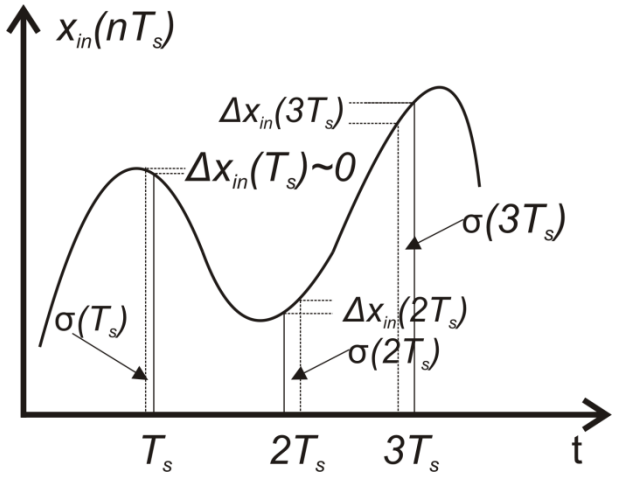

Fig. 1.15. Sampling time jitter error.

This phenomenon is known as "aperture jitter", "aperture uncertainty" or "sampling jitter", which is, in other words, the sample-to-sample variation in the instant the switch opens [1], [5], [31]-[34]. This error affects the value of the sampled signal by an error that depends on both the jitter, and the rate-of-change of the input signal.

For any given value of aperture jitter, the corresponding error increases as the input slew-rate increases. The effects of phase jitter on the external sampling clock (or the analog input for that matter) produce exactly the same type of error.

Assuming a sinusoidal input $x_{in}(t) = A\sin(\omega_{in}t) = A\sin(2\pi f_{in}t)$ where A is amplitude from zero to peak (half the full-scale).

The error is

$$\Delta x_{in}(nT_s) = \sigma(nT_s)A\omega_{in}\cos(\omega_{in}nT_s) = \sigma(nT_s)\left.\frac{dx_{in}(t)}{dt}\right|_{t=nT_s} \qquad (1.16)$$

which is a sampled-data quantity $\sigma(nT_s)$ amplified by A and modulated by a cosine at the input frequency [3]. The maximum error occurs when the input slope is maximum or rather at the zero crossing (cosine is equal to 1).

For a given rms jitter σ_t, the rms error is [30]

$$\sigma_t \left.\frac{dx_{in}}{dt}\right|_{rms} = \sigma_t \sqrt{2}\pi f_{in} A \tag{1.17}$$

and the *SNR* purely due to the jitter is

$$SNR_{dB} = -20\log_{10}(\sigma_t 2\pi f_{in}) \tag{1.18}$$

while the corresponding *ENOB* is

$$ENOB = \frac{-20\log_{10}(\sigma_t 2\pi f_{in}) - 1.76}{6.02} \tag{1.19}$$

From eq. (1.19), it can be seen that "aperture jitter" places a fundamental limit on achievable resolution. In fact, fixing a jitter value, relation (1.19) states the maximum *ENOB* reachable at a certain input frequency. The worst case for the input frequency is equal to $f_s/2$ for base-band sampling, while is equal to $f_{max}=f_{IF} + f_s/2$ for IF sampling. Thus, eq. (1.19) can be rewritten as

$$ENOB = \frac{-20\log_{10}(\sigma_t 2\pi f_{max}) - 1.76}{6.02} \tag{1.20}$$

This relationship, plotted in Fig. 1.16 for two different values of jitter (1 *ps*, blue line; 100 *fs*, red line), shows that to achieve *ENOB* about 7 the rms jitter must be keep lower than *1 ps*.

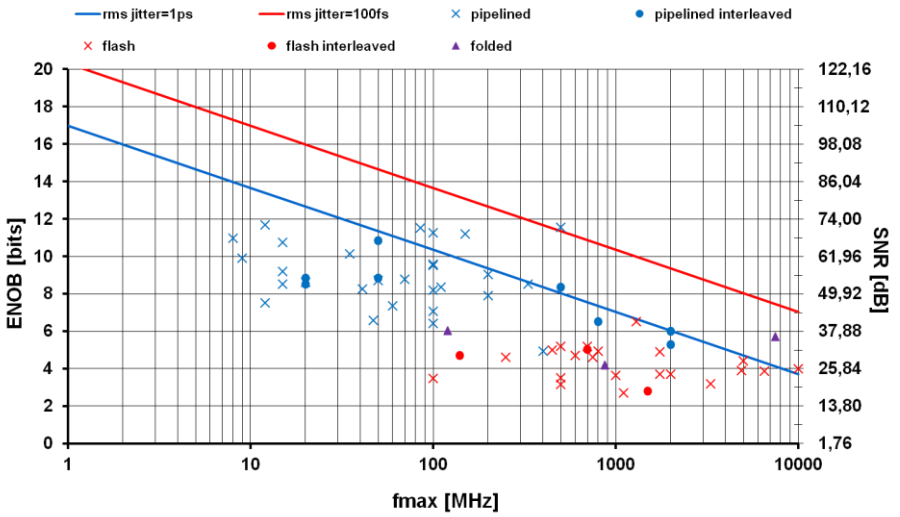

Fig. 1.16. ENOB versus f_{max} and jitter limitations. Blue line: jitter equal to 1 *ps*; red line: jitter equal to 100 *fs*.

It is worth highlighting that for low-frequency applications the effect of jitter is not relevant. If the input frequency increases, also the

noise referred to the jitter increases and the effect of jitter is no more negligible.

It should be noted that increasing f_{max}, *ENOB* decreases about *1bit/octave* (more than *3 bits/decade*). Furthermore, a jitter equal to 100 *fs* (red line in Fig. 1.16) imposes that in the GHz range of frequencies the maximum achievable resolution is lower than 10 bits.

Moreover, the three most important ADC architectures (flash, folded, pipeline) are labeled in Fig. 1.16. The ADC's data reported in the *IEEE Custom Integrated Circuits Conference (CICC), International Solid-State Circuits Conference (ISSCC), Journal of Solid-Sate Circuits (JSSC), Transactions on Circuits and Systems (TCAS), BiCMOS Circuits and Technology Meeting (BCTM), and Symposium on VLSI Circuits* during the last decade, and where available, are plotted in Fig. 1.16 at the aim of comparison between different converter topologies.

1.5.2 Thermal noise

Thermal noise is another unavoidable limit to the ADC's performances.

In order to simplify the analysis, the sampling circuit presented in Fig. 1.17.a can be considered, an input voltage V_{in} charges a capacitor through a switch. At the sampling time the switch opens and the input voltage is held across the capacitor.

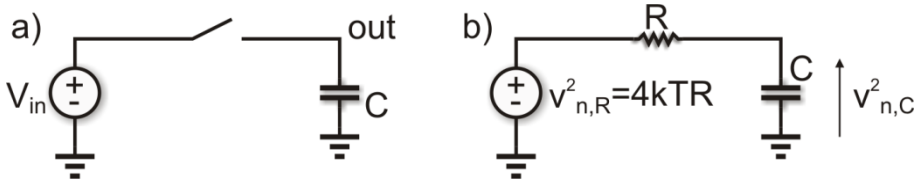

Fig. 1.17. a) Basic model of a sampler, and **b)** noise circuit.

In Fig. 1.17.b is shown the circuit including noise generator [3], [35]. The resistance *R* includes the on-resistance of the switch and the output resistance of the signal generator. The spectrum of the thermal noise due to *R* is white, $v_{n,R}^2 = 4kTR$ (where *k* is the Boltzmann's constant and *T* is the Kelvin temperature). The *RC* series provides a low-pass filter, thus the noise spectrum across the capacitor is colored

$$v_{n,C}^2(\omega) = \frac{4kTR}{1+(\omega RC)^2} \tag{1.21}$$

Note that for a correct operation the time constant $\tau=RC$ must be much smaller than the sampling time T_s. As a consequence, when the switch is open, the capacitor holds not only the input voltage but also the noise. Thus, being the noise spectrum across C not band-limited, the aliasing phenomenon folds noise components from the higher Nyquist zones into base-band. As previously discussed, the cut-off frequency of the low-pass filter must be much larger than $f_s/2$ and many spectrum components of relevant power are superimposed giving rise to an almost white resulting spectrum. Therefore, the total noise power stored on C when the switch goes off is

$$P_{n,C} = 4kTR\int_0^\infty \frac{df}{1+(2\pi fRC)^2} = \frac{kT}{C} \tag{1.22}$$

Observe that $P_{n,C}$ does not depend on R. Increasing R raises the white noise floor but also improves the low-pass filtering action. The two effects compensate each other thus canceling the R dependency [3].

Taking into account the equation related to the capacitor charge, it can be easily derived the circuit settling time

$$e^{-t/\tau} = \frac{V_{LSB}}{2\Delta V} \tag{1.23}$$

where V_{LSB} is the LSB expressed in volts and ΔV in the worst case can be considered equal to the full-scale input voltage V_{FS}, thus eq. (1.23) can be rewritten as

$$e^{-t_{sett}/\tau} = \frac{V_{LSB}}{2V_{FS}} = \frac{V_{FS}/2^{ENOB}}{2V_{FS}} \Leftrightarrow t_{sett} = (ENOB+1)RC\ln 2 \tag{1.24}$$

The settling time to guarantee the correct sampler operation must be at most equal to half the sampling time

$$(ENOB+1)RC\ln 2 = \frac{1}{2f_s} \tag{1.25}$$

Substituting eq. (1.25) in (1.22) the noise power is

$$P_{n,C} = 2kT\cdot R\cdot f_s\cdot\left(ENOB+1\right)\cdot\ln 2 \tag{1.26}$$

Thus, equating the thermal noise power (1.26) to the quantization noise power (1.6) it can be obtained a relationship between *ENOB* and sampling frequency f_s

$$(ENOB+1)\cdot 2^{2ENOB} = \frac{V_{FS}^2}{12}\cdot\frac{1}{2kT\cdot R\cdot f_s\cdot \ln 2} \tag{1.27}$$

1.5.3 Comparator ambiguity

The comparator is a key element in the A/D conversion process. A comparator is essentially a pre-amplifier followed by a latch (see Fig. 1.18). During the first phase the comparator amplifies the differential input voltage while during the latch phase the comparator multiplies the amplified input voltage by a growing exponential until the amplifier saturation, or until the end of the latch phase.

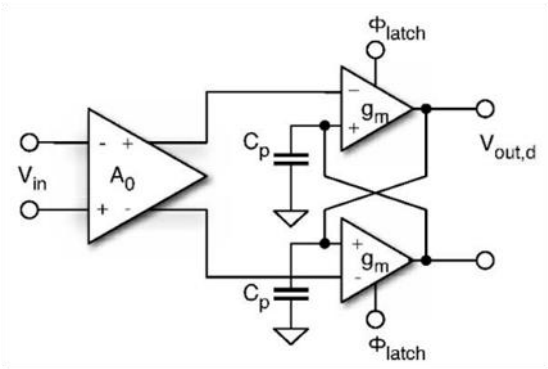

Fig. 1.18. Typical comparator topology for A/D Converters.

A metastability error occurs when the comparator output is ambiguous. It means that if the differential input is small, making the comparator takes a long time to produce a well-defined logic level, the output, at the end of the regenerative phase, cannot be interpreted unambiguously by the following digital circuit, thus determining an error in the output code.

The equivalent gain of a regenerative comparator can be assumed to be

$$A_{eq} = A_0\cdot e^{t/\tau_{latch}} \tag{1.28}$$

where t is the time duration of the latch phase while τ_{latch} is the regenerative time constant. Neglecting the parasitic effects, the regenerative time constant can be approximated by

$$\tau_{latch} = \frac{C_p}{g_m} = \frac{1}{2\pi f_T} \tag{1.29}$$

where C_p is the capacitance at the regenerative node, and g_m is the transconductance of the latch, while f_T is the maximum obtainable unity gain bandwidth of the transconductance amplifier . Typically the latch period at most equals half of the sampling frequency

$$t = f_s/2 \tag{1.30}$$

thus producing a metastable error if the latch does not provide a well-defined output in the required time.

In the case of an uniform input over the voltage range of the comparator, the metastability error probability can be approximated by [31]

$$p_i = \frac{V_{FS} / A_{eq}}{V_{FS}} 2^{ENOB} = \frac{2^{ENOB}}{A_0} \cdot e^{-\frac{\pi f_T}{f_s}} \tag{1.31}$$

and the corresponding metastability error power (whatever output in metastable state) can be easily obtained as

$$P_m = \frac{V_{LSB}^2}{12} \cdot p_i \cdot 2^{2ENOB+1} \tag{1.32}$$

Thus, considering $A_0=1$ and equating P_m to the quantization noise power (eq. (1.6)), it can be obtained a relationship, due to the comparator ambiguity, between the *ENOB* and the sampling frequency

$$ENOB = \frac{\log_2(e^{\pi f_T / f_s}) - 1}{3} \tag{1.33}$$

Thus, the metastable behavior of the comparator poses another fundamental limit on achievable resolution. It can be noted that when sampling frequency increases the *ENOB* reduces.

1.5.4 Heisenberg uncertainty principle

Heisenberg uncertainty principle is the ultimate limit dictated by physical laws, leaving a relevant and attractive margin to improve the conversion implementations [6].

The mathematical expression of Heisenberg uncertainty principle is

$$\Delta E \cdot \Delta t \geq \frac{\hbar}{2} \tag{1.34}$$

This relation states that the product of the uncertainties in position and momentum is always equal to or greater than one half of the reduced Planck constant ($\hbar = h/2\pi$=1.054e-34 *Js*). The minimum energy that we want to resolve, in a time period of half the sampling period $T_s/2$, is referred to a signal with amplitude equal to half *LSB*. Thus, the corresponding energy can easily obtained

$$\Delta E = \frac{V_{FS}^2}{R} \cdot 2^{-2ENOB-2} \cdot \frac{1}{2 f_s} \tag{1.35}$$

Substituting (1.35) in (1.34) it can be derived the following relation:

$$2^{2ENOB} = \frac{V_{FS}^2}{4R\hbar \cdot f_s^2} \tag{1.36}$$

that is another trade-off between maximum allowable resolution and the sampling frequency. It is worth to highlight that the Heisenberg limit is well beyond the current state-of-art.

1.5.5 Comparison of converter topologies

As discussed in the previous sections, thermal noise, comparator ambiguity, and Heisenberg uncertainty principle establish three fundamental upper limits to the converter performances. These limits, as seen, dictate a trade-off between the resolution, in terms of the effective number of bits (*ENOB*), and sample rate (f_s).

In Fig. 1.19 are depicted the relations (1.27), (1.33), (1.36) for a full-scale voltage $V_{FS}=1$, and, as in section 1.5.1, are also labeled the ADCs. Moreover, in Fig. 1.19 are also depicted the limitations imposed by the thermal noise (1.27) for R=50 Ω (green line) and R=1 *k*Ω (blue line), the comparator ambiguity (1.33) for f_T=50 *GHz* (orange dashed line) and f_T=250 *GHz* (purple dashed line), and the Heisenberg principle (1.36) (brown dashed line).

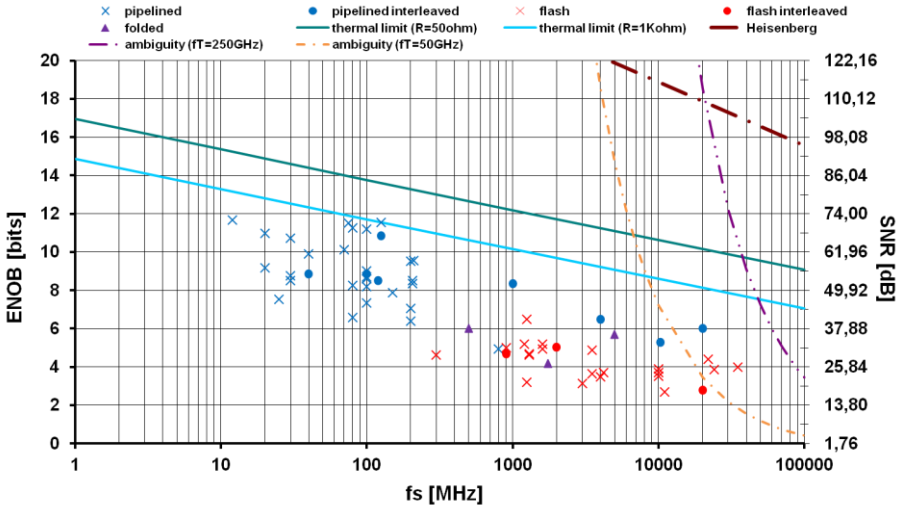

Fig. 1.19. ENOB versus sampling frequency, and limitations imposed by thermal noise (solid lines), comparator ambiguity (orange and purple dashed lines), and Heisenberg principle (brown dashed line).

It can be note that for sample rates in the range of gigahertz frequencies, the maximum resolution is below 8 bits and the most popular topology is the flash one. It is even more visible in Fig. 1.20 that shows the BiCMOS circuits only.

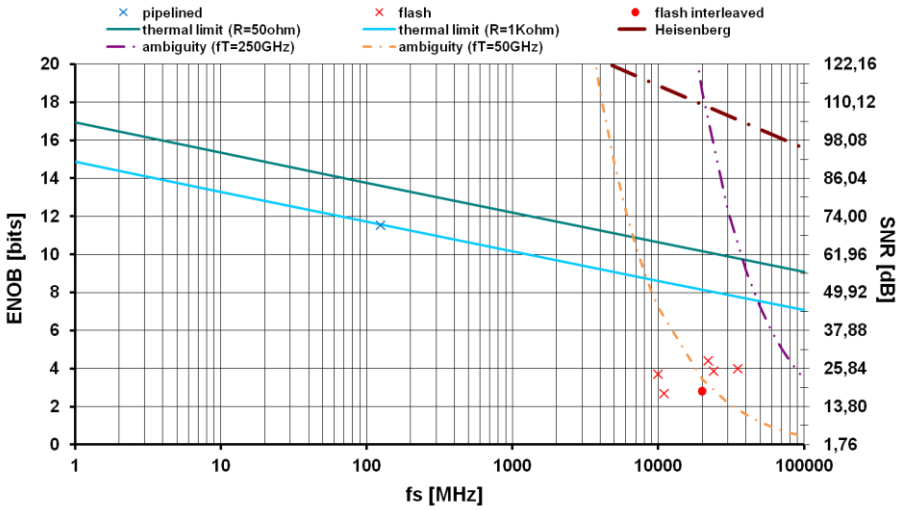

Fig. 1.20. ENOB versus sampling frequency for BiCMOS circuits only.

Thus, the choice of the flash topology is justified by the possibility to provide high resolution and high speed with high frequency input signal. Moreover, the flash circuit is a basic block in other converter implementations, such as folding&interpolating, that can improve the overall ADC's performances.

Additionally, it must be considered that the technology process used for this work is the IHP 0.25 µm BiCMOS Si/SiGe, with a unity gain frequency of 50 *GHz* and supply voltage of 3.3-3.6 *V*.

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Chapter 2

Flash ADC Design

A generic block diagram of an 8-bits flash converter is shown in Fig. 2.1.

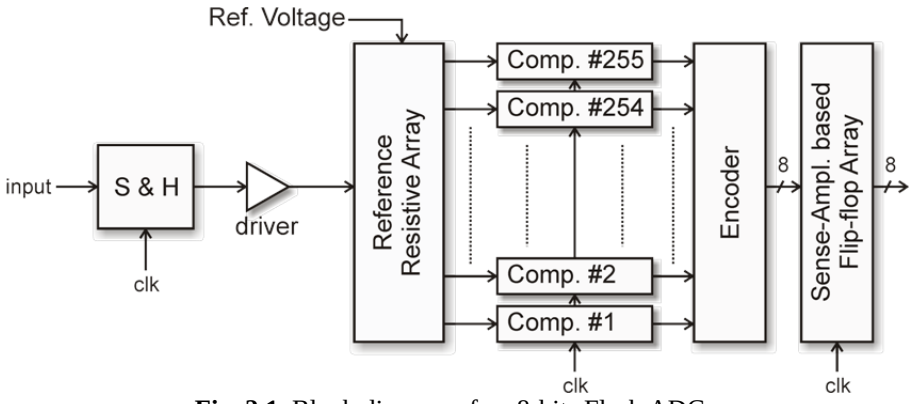

Fig. 2.1. Block diagram of an 8-bits Flash ADC.

It comprises a sample-and-hold amplifier (SHA, or S&H), the resistive ladder generating the suitable reference voltages, the comparators array and the logical circuits providing the digital output.

In the following sections, it will be described in details each one of the ADC's basic circuits and their main specifications in order to better understand their impact on the overall performances.

2.1 Sample-and-Hold and Track-and-Hold Amplifier

Sample-and-hold amplifier plays a crucial role in the design of data acquisition interfaces, particularly analog-to-digital converters [1]-[3].

The design of SHAs is not simple because they must operate in the extreme conditions of performance envelope, thus achieving

simultaneously high linearity, high speed, large voltage swings, high drive capability, and low power dissipation. Moreover, in low-voltage design the analog sampling becomes more challenging because the limited headroom tightens the trade-offs between the performance metrics.

A sample-and-hold (SHA) or track-and-hold (THA, or T&H) amplifier is a circuit frequently required in the ADC front-end to capture rapidly varying input signals. The function of the SHA is to sample the analog input signal and to hold that value while subsequent circuitry digitizes it. Although a SHA refers to a device which spends an infinitesimal time acquiring signals and a THA refers to a device which spends a finite time in this mode, common practice will be followed and the two terms will be used interchangeably throughout this discussion as well the terms sample and track.

The main difference between SHA and THA is that the first holds the signal over a full period of sampling, while the THA holds the input signal only over a part of the sampling period (usually half the period) as shown in Fig. 2.2.

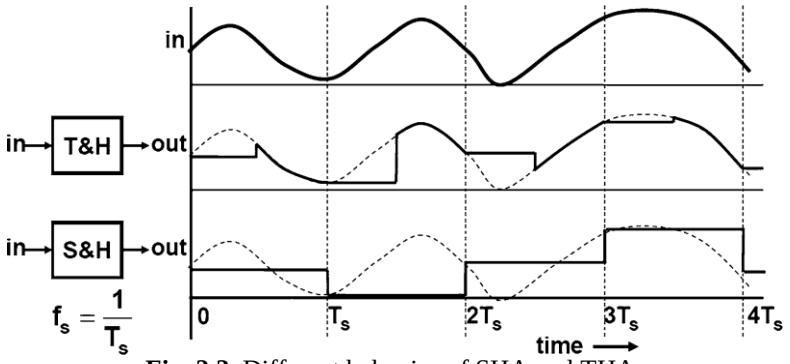

Fig. 2.2. Different behavior of SHA and THA.

The basic circuit diagram of a THA is shown in Fig. 2.3. It consists of an input amplifier, a switch, an hold capacitor, and an output buffer.

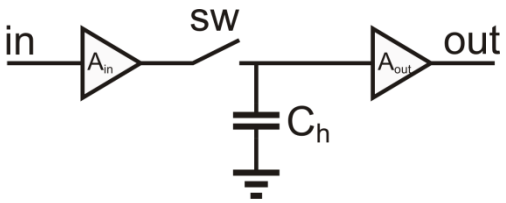

Fig. 2.3. Basic block diagram of THA.

The track-and-hold function is realized through two different phases: the first phase is for the signal acquisition, the voltage on the capacitor follows the input signal (track phase), in the second phase the signal value remains fixed at its value at the moment of opening the switch and the capacitor retains the voltage present before it was disconnected from the input buffer (hold phase).

The input buffer is useful to reduce the input load, so avoiding that the capacitance charge/discharge current could give rise to input disturbance.

The output buffer decouples the following circuit from the hold capacitor C_h that retains dynamically the acquired voltage. Furthermore, it offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely.

Several error sources are linked to the THA operation, depending on both static and dynamic behavior. The specifications, useful to understand the THA performances, are referred to its different operation modes (see Fig. 2.4). Harmonic distortion, hold mode feed-through, and settling time essentially depend on the switch and input buffer performances. On the other hand, the output buffer performances impact on the droop-rate and the static non-linearity, besides on the circuit hold-time.

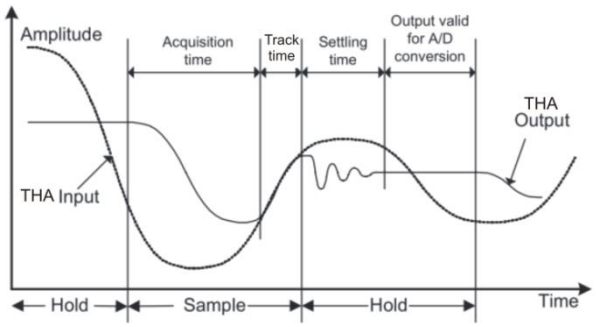

Fig. 2.4. THA terminologies.

These specifications will be treated in more details in the following.

Next sections are devoted to the study, analysis and design of two main THA circuit solutions that use the bipolar technology: diode-bridge (DB) and switched emitter follower (SEF).

2.2 Diode-Bridge (DB)

A schematic diagram of the diode-bridge circuit in the single-ended configuration is presented in Fig. 2.5.

From now on we consider a peak-to-peak input voltage equal to $1\ V$ ($\pm 0.5\ V$), which means a full-scale input voltage $V_{FS}=1$ corresponding to a $V_{LSB}=974\mu V$ for a 10-bits converter. The considered signal input frequency is 1 *GHz*.

The switch design uses an improved high-speed Schottky diode-bridge to disconnect the output from the input and a hold capacitor to maintain that voltage [1], [3] (see Fig. 2.5).

The bridge consists of four Schottky diodes (labeled as #1 in Fig. 2.5). Furthermore, between nodes X and Y are present two other Schottky diodes (labeled as #2 in Fig. 2.5). These last two diodes are

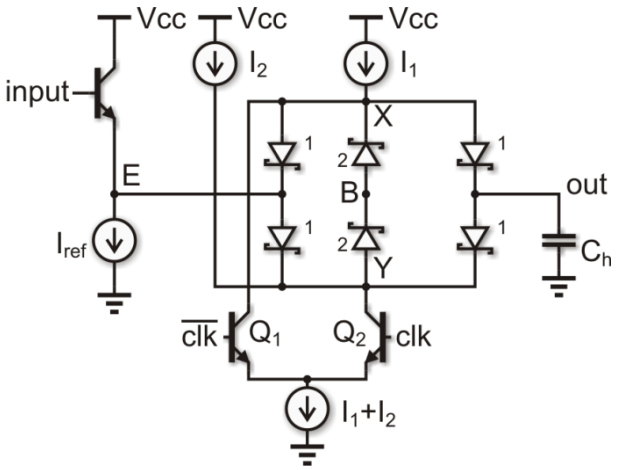

Fig. 2.5. Schematic diagram of the diode-bridge with emitter-follower input buffer.

off during the track phase, while during the hold phase are forward-biased so assuring a "clamping" action on the X and Y nodes. This action improves the circuit behavior in terms of hold feed-through, as it will be explained in details in the following sub-sections.

In the track mode

$$clk = 1 \Rightarrow \begin{cases} Q_2 \text{ is on} \\ Q_1 \text{ is off} \end{cases} \Rightarrow \begin{cases} V_X = V_{inDB} + V_{D1} \\ V_Y = V_{inDB} - V_{D1} \end{cases} \tag{2.1}$$

where $V_{inDB}=V_E$ is the voltage at the bridge input and V_{D1} is the voltage drop on the bridge's diodes. In order to guarantee that clamp diodes are reverse-biased during the track mode, the following constraints must be verified

$$\begin{cases} V_X \geq V_B - 0.1V \\ V_Y \leq V_B + 0.1V \end{cases} \tag{2.2}$$

where 0.1 *V* represents a suitable margin obtaining the desired goal.

Substitution of eq. (2.1) in (2.2) gives

$$\begin{cases} V_{inDB} \geq V_B - V_{D1} - 0.1V \\ V_{inDB} \leq V_B + V_{D1} + 0.1V \end{cases} \tag{2.3}$$

From eq. (2.3), it results

$$V_B - (V_{D1} + 0.1V) \leq V_{inDB} \leq V_B + (V_{D1} + 0.1V) \tag{2.4}$$

while from eq. (2.4) it can be seen that the maximum input swing is

$$V_{swi\max} = 2(V_{D1} + 0.1V) \tag{2.5}$$

Assuming that the voltage drop on the Schottky diodes is equal to 0.4 *V*, and substituting in eq. (2.5), the maximum input swing becomes $V_{swi\ max}=1\ V$.

In the hold mode

$$clk=0\Rightarrow\begin{cases}Q_2 \text{ is off}\\ Q_1 \text{ is on}\end{cases}\Rightarrow\begin{cases}V_X=V_B-V_{D2}\\ V_Y=V_B+V_{D2}\end{cases} \tag{2.6}$$

where V_{D2} is the voltage drop on the clamp diodes. In order to guarantee that the bridge's diodes are reverse-biased during the hold mode, the following constraints must be verified

$$\begin{cases}V_{inDB}\geq V_X-0.1V\\ V_{inDB}\leq V_Y+0.1V\end{cases} \tag{2.7}$$

where 0.1 *V* represents a suitable margin obtaining the desired goal.

Substituting eq. (2.6) in (2.7)

$$\begin{cases}V_{inDB}\geq V_B-V_{D2}-0.1V\\ V_{inDB}\leq V_B+V_{D2}+0.1V\end{cases} \tag{2.8}$$

and so results

$$V_B-\left(V_{D2}+0.1V\right)\leq V_{inDB}\leq V_B+\left(V_{D2}+0.1V\right) \tag{2.9}$$

From eq. (2.9) it can be seen that the maximum input swing is

$$V_{swi\max}=2\left(V_{D2}+0.1V\right) \tag{2.10}$$

Assuming that the voltage drop on the Schottky diodes is equal to 0.4 *V*, and substituting in eq. (2.10), the maximum input swing becomes $V_{swi\ max}=1\ V$.

Half the input full swing is equal to the input dc level, thus from eqs. (2.4), (2.9) it can be stated that the input dc level is $V_{inDBDC}=V_B$.

During the track phase (clock is high), the transistor Q_1 is off, while the transistor Q_2 is on. In order to assure a proper circuit operation, avoiding the saturation of Q_2 the following condition is imposed

$$V_{clkH}\leq V_Y+0.3V \tag{2.11}$$

where 0.3 *V* is the base-collector voltage drop and V_{clkH} is the high voltage of the clock signal. Recalling eq. (2.1), eq. (2.11) becomes

$$V_{clkH}\leq V_{inDB}-V_{D1}+0.3V \tag{2.12}$$

The worst case is when the input is at its minimum value $V_{inDB}= V_{inDBDC} - V_{swi}/2= V_B - V_{swi}/2$, thus substituting this value eq. (2.12) can be rewritten as

$$V_{clkH} \le V_B - \frac{V_{swi}}{2} - V_{D1} + 0.3V \tag{2.13}$$

During the hold phase (clock is low), the transistor Q_1 is on, while the transistor Q_2 is off. In order to assure a proper circuit operation, avoiding the saturation of Q_1, the following condition is imposed

$$V_{clkH} \le V_X + 0.3V \tag{2.14}$$

recalling eq. (2.1), eq. (2.14) becomes

$$V_{clkH} \le V_B - V_{D2} + 0.3V \tag{2.15}$$

The relations (2.13), (2.15) establish a constraint on the maximum value of the clock signal assuring the non-saturation of the transistors Q_1, Q_2 during the hold and track phase, respectively. Furthermore, the constraint, expressed by (2.13), is dominant, thus the value of V_{clkH} must be obtained from eq. (2.13).

Now it can be analyze the input dc range by referring to Fig. 2.5. Thus, we have

$$V_{inDC} - V_{BE} = V_{EDC} = V_{inDBDC} \tag{2.16}$$

where V_{BE} is the base-emitter voltage of the input buffer, and $V_{inDBDC}=V_{EDC}$ is the dc voltage of the bridge input.

During track mode, it can be at most

$$\begin{cases} V_{inDB\max} = V_X - V_{D1} \\ V_{inDB\min} = V_Y + V_{D1} \end{cases} \tag{2.17}$$

where $V_X=V_{CC}-V_m$, $V_Y=V_m+V_{CE2}$, V_{CE2} is the voltage drop across the collector-emitter junction of Q_2 , and V_m is the minimum voltage drop on the current mirror here replaced by ideal current source. By substituting, eq. (2.17) becomes

$$\begin{cases} V_{inDB\max} = V_{CC} - V_m - V_{D1} \\ V_{inDB\min} = V_m + V_{CE2} + V_{D1} \end{cases} \tag{2.18}$$

Considering that we can written

$$\begin{cases} V_{inDB\max} = V_{inDBDC\max} + V_{swi}/2 \\ V_{inDB\min} = V_{inDBDC\min} - V_{swi}/2 \end{cases} \tag{2.19}$$

and substituting in eq. (2.18), it follows

$$\begin{cases} V_{inDBDC\max} = V_{CC} - V_m - V_{D1} - \dfrac{V_{swi}}{2} \\ V_{inDBDC\min} = V_m + V_{CE2} + V_{D1} + \dfrac{V_{swi}}{2} \end{cases} \tag{2.20}$$

Assuming $V_{inDBDC\ \max} = V_{inDBDC\ \min} = V_{inDBDC}$ and substituting in eq. (2.20), V_m can be expressed by

$$V_m = \frac{V_{CC} - V_{swi} - 2V_{D1} - V_{CE2}}{2} \tag{2.21}$$

Assuming V_{D1}=0.4 *V*, V_{CE2}=0.8 *V* and V_{CC} equal to the minimum supply voltage (3.3 *V*) and considering that $V_{swi\ \max}$=1 *V*, thus V_{swi}=0.5 *V* in a differential configuration, the value of V_m , complying with the constraint due to eq. (2.17), is given by

$$V_m = 0.6\,V \tag{2.22}$$

Substituting (2.22) in (2.20) the dc level at the bridge input is

$$V_{inDBDC} = 2.05\,V \tag{2.23}$$

So recalling eq. (2.16), and considering V_{BE}=0.85 *V* (as resulting from simulation), the dc input is

$$V_{inDC} = 2.9\,V \tag{2.24}$$

Now it is possible to estimate the high clock value by referring to the condition (2.13) and by keeping in mind that V_{CE2}=0.8 *V*. Thus, if we consider V_{BE2}=0.8 *V*, the base-collector voltage V_{BC2}=0 *V*. This last means that in eq. (2.13) it must not consider the voltage drop of 0.3 *V*, and so (2.13) becomes

$$V_{clkH} \le 1.4\,V \tag{2.25}$$

Finally, it can be assumed that V_{clkH}=1.4 *V*, while the low voltage level of the clock signal is V_{clkL}=1.0 *V*. Thus, the clock signal swing is 400 *mV* corresponding to 800 *mV* for the differential configuration.

2.2.1 DB Track Mode Performance: Distortion Analysis

Since a THA in the track mode is simply an amplifier, both the static and dynamic specifications in this mode are similar to those of any amplifier. The principle track mode specifications are offset, gain, nonlinearity, bandwidth, settling time, distortion, and noise.

A distortion analysis introduced by the THA is useful to determine its dependence on the circuit bias currents, the amplitude and frequency of the input signal, the hold capacitance, and to define some crucial design choices. The main contribution is dynamic and is due to the current flowing through C_h (see Fig. 2.6).

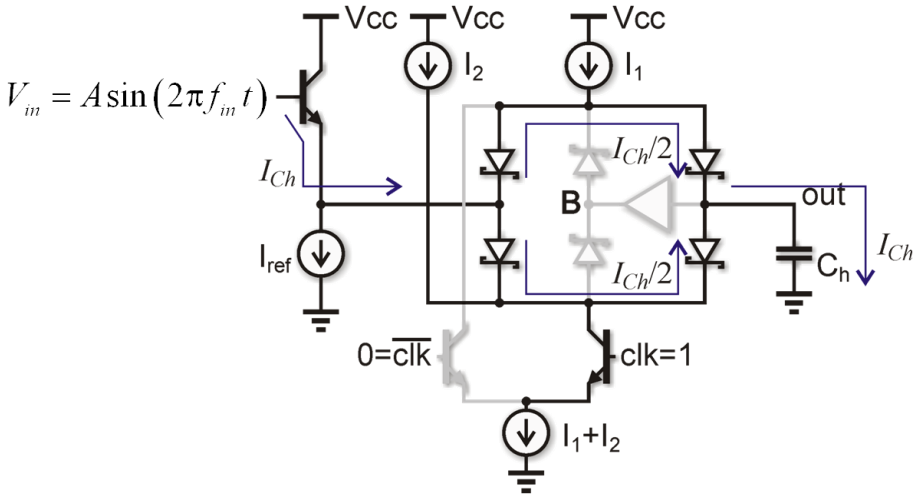

Fig. 2.6. Diode-bridge: equivalent circuit for distortion analysis.

The current I_{Ch} can be expressed as follows

$$I_{Ch} \approx C_h \frac{dV_{in}}{dt} = 2\pi f_{in} \cdot C_h \cdot A\sin\left(2\pi f_{in} t\right) \tag{2.26}$$

Recalling the analysis reported in the Appendix A, the harmonic distortion introduced by the diode-bridge, neglecting the higher order contributions, is

$$\begin{cases} HD_2 = \dfrac{H_2}{H_1} = \dfrac{1}{4}\left(\dfrac{i_{c\max}}{I_{ref}}\right)^2 \cdot \dfrac{V_T}{A} \\ HD_3 = \dfrac{H_3}{H_1} = \dfrac{1}{12}\left(\dfrac{i_{c\max}}{I_1}\right)^3 \cdot \dfrac{V_T}{A}\left[1+2\left(\dfrac{I_{ref}}{I_1}\right)^3\right] \end{cases} \tag{2.27}$$

where $i_{C\,max}=2\pi f_{in}C_hA$.

It can be noted that the distortion depends on the input signal amplitude and frequency, the bias currents I_1, I_{ref} and the hold capacitance.

The diode-bridge in a differential fashion can be obtained by using two identical single-ended circuits, as shown in Fig. 2.7, to process a differential input signal. This configuration has the advantage avoiding distortion of even harmonics ($HD_2 \approx 0$) [4] and the single input and output signals (in_+, in_-, out_+, out_-) have a swing equal to the half the swing of the differential signal.

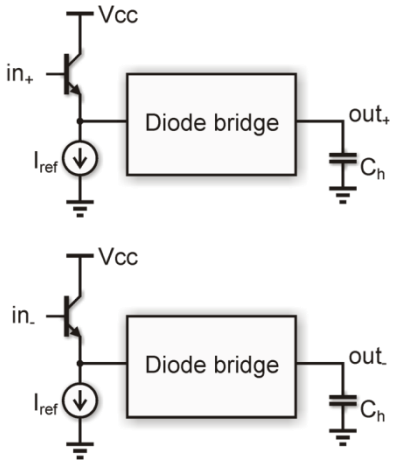

Fig. 2.7. Block diagram of diode-bridge in differential configuration.

These advantages are lost in a single-ended configuration, while it is important that the THA introduces very little distortion, since the distortion incurred in the analog part of ADC is difficult to remove by the subsequent circuits.

Another very important issue is the bandwidth. In fact, the THA must have a bandwidth greater than that of the maximum expected input signal and it must settle to the specified accuracy in a short amount of time, usually much less than half a clock cycle.

As the distortion, the bandwidth also depends on the input stage bias current (I_{ref}) and the diodes bias current (I_1), the amplitude and frequency of the input signal (f_{in}), the hold capacitance (C_h). It is possible to establish the optimal trade-off based on the required performance in terms of maximum input frequency and resolution.

2.2.2 DB Track Mode Performance: Noise Analysis

The noise is an important figure of merit to evaluate the circuit behavior, since it imposes a lower limit on the signal that can be processed by the circuit avoiding degradation of the output signal quality. For this reason, the circuit noise performance is usually expressed by an equivalent input noise signal which provides the same output noise of the considered circuit [5].

An exact noise analysis is complex due to the large number of error sources. Thus, considering only the input buffer (the emitter-

follower), whose noise performance depending on the transistor, it can be shown (see [5]) that the noise on the hold capacitor is

$$V_{n,C_h}^2 = \gamma \cdot \frac{kT}{C_h} \qquad \gamma = \frac{1}{2} + \beta \cdot \frac{r_b}{r_\pi} \tag{2.28}$$

It can be noted that, in a first approximation, the noise (*SNR*) only depends on the hold capacitor. Furthermore, some numerical simulations have confirmed that the previous approximation also occurs for the DB.

2.2.3 Diode-Bridge Track Mode Performance: Design

At the aim of a correct sizing of C_h, I_{ref}, I_1, the relationships with the *SNR* and *THD* (reported in the previous sub-sections) must be taken into account.

The *SNR* depends on the capacitance of C_h, which should be sized to get a good margin on the *SNR* according to the design constraints. A parametric analysis has been performed, by varying the C_h value, obtaining the *SNR*, and the related *ENOB*, as function of C_h (see Fig. 2.8).

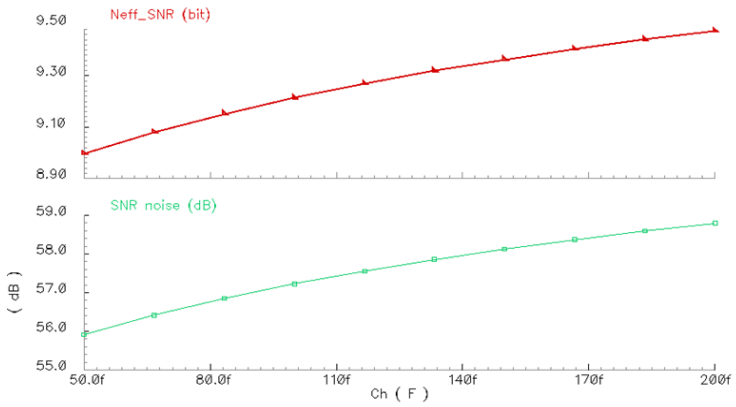

Fig. 2.8. *SNR* (below) and the related *ENOB* (above) versus C_h.

The choice of C_h is made for obtaining an *ENOB* beyond 9. In this case of a differential DB with ideal current sources, it has chosen a capacitance value (100 *fF*) corresponding to an *ENOB* equal to 9.2.

The *THD* depends on C_h, I_{ref}, I_1, thus fixing C_h=100 *fF* and considering in the worst case the maximum input frequency (f_{in}=1 *GHz*), a parametric analysis has been performed by varying the I_{ref} value for obtaining the behavior of the *THD* at the input of the DB as function of the current itself (see Fig. 2.9).

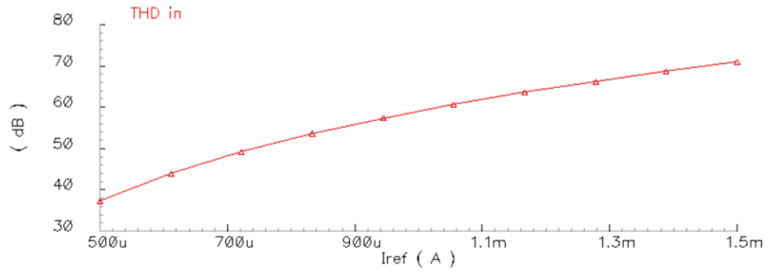

Fig. 2.9. *THD* at the input of diode-bridge as function of the bias current I_{ref}.

In order to meet the design constraints, the THD_{in} value to be considered is equal to 60 *dB* corresponding to a current I_{ref}=1 *mA*.

Once fixed the value of harmonic distortion at the DB input, the value at the output is consequently fixed by the distortion introduced by the DB. This last depends on the DB bias current I_1 that can be set through parametric analysis in order to obtain the desired value of 58 *dB* corresponding to a bias current I_1=1.4 *mA* (see Fig. 2.10).

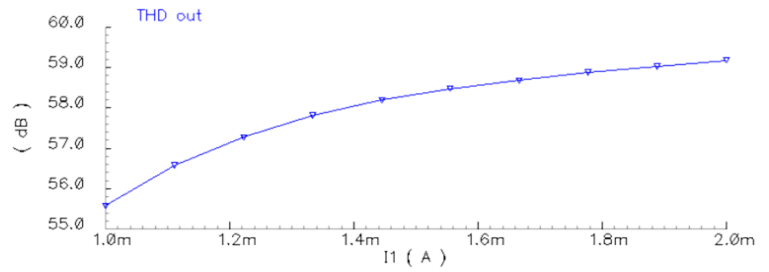

Fig. 2.10. *THD* at the output of diode-bridge as function of the bias current I_1.

2.2.4 DB Hold Mode Performance: Hold Feedthrough

The hold-mode feedthrough is the percentage of the input signal on the output signal during the hold phase. This effect is due to the inevitable parasitic coupling between input and output during hold

mode. The consequence is a perturbation of the voltage held on the capacitor due to imperfect insulation between the input and the output during the hold phase. This effect can be reduced in the DB by increasing the current I_2. The latter claim can be verified by analyzing the circuit during the hold phase, as shown in Fig. 2.11. In the circuit is also present a bootstrap buffer (whose usefulness in terms of pedestal will be discussed later) to take into account his effect in the estimation of hold feedthrough.

The bridge diodes (#1 in Fig. 2.11) are reverse biased, thus acting as capacitances (diode junction capacitance). On the other hand, the clamping diodes (#2 in Fig. 2.11) are forward biased, resulting in equivalent on-resistance. From this considerations it can be obtained the simplified equivalent circuit in Fig. 2.12, where the junction capacitance of the bridge diodes is modeled with C_j, and the on-resistance of the clamping diodes with r_d.

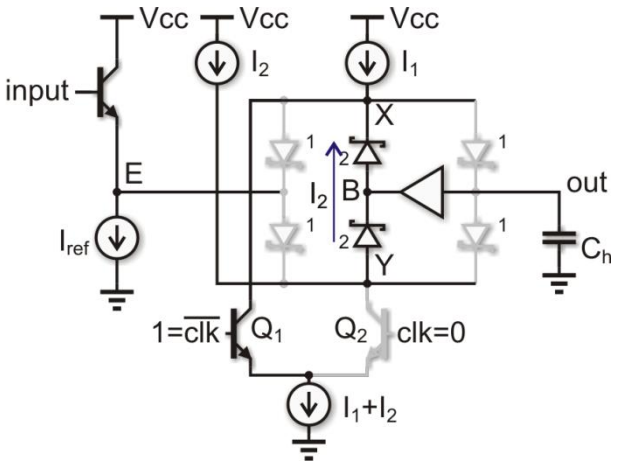

Fig. 2.11. Diode-bridge in the hold mode.

The buffer output resistance is also modeled with r_{out}. Now, it can be easily calculated the transfer characteristic in the hypothesis $C_j << C_h$

$$\left.\frac{V_{out}}{V_{in}}\right|_{hold} \simeq \frac{C_j}{C_h} \cdot \frac{2\left(r_d + 2r_{out}\right)C_j s}{1 + 2\left(r_d + 2r_{out}\right)C_j s} \tag{2.29}$$

Eq. (2.29) is an high pass filter response with gain equal to C_j/C_h and time constant equal to $2(r_d+2r_{out})C_j$. Thus, reducing the signal feedthrough means that C_j is much smaller than C_h and the filter cut-

off frequency is shifted to higher frequencies. This latter can be obtained reducing the resistance value r_d, r_{out}, so allowing $1/2\pi 2(r_d+2r_{out})C_j$ to be much larger than the maximum input frequency.

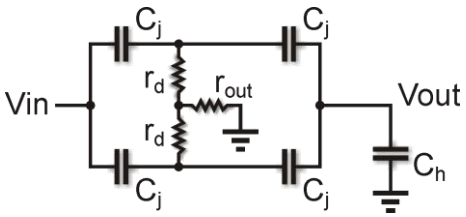

Fig. 2.12. Simplified diode-bridge circuit for estimating the hold feedthrough.

Furthermore, if we not consider the buffer (r_{out}=0) the signal feedthrough only depends on r_d (the capacitance C_j is related to the diode area size, and so fixed by the previous choice of the bias current I_1).

Finally, the hold feedthrough can be reduced by decreasing r_d or rather increasing the extra current I_2. Thus, it has been performed a parametric analysis, shown in Fig. 2.13, by varying the current I_2 in order to get a reasonable feedthrough. This means that the current value cannot be too high, so avoiding an increase of the size of the transistor Q_2 (see Fig. 2.11) leading to an increase of its capacitance. This latter is undesirable because introduces more distortion and forces the clock driving a larger capacitive load.

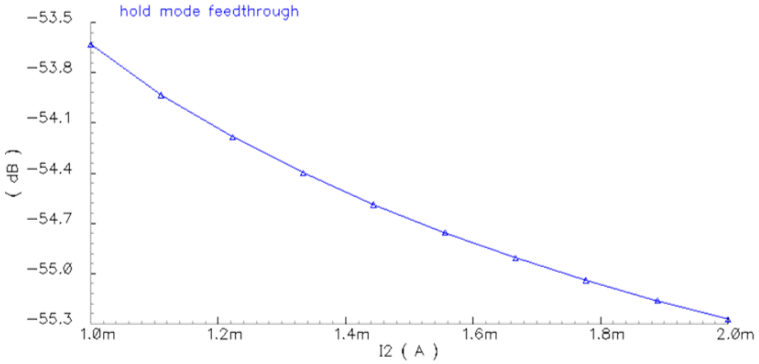

Fig. 2.13. Hold-mode feedthrough effect by varying the current I_2.

It is worth highlighting that the numerical simulation result, reported in Fig. 2.13, has been obtained in the hold mode operation (*clk=0*). Thus, it is necessary fixing the initial condition on the hold capacitor. In this case, the differential outputs have been considered equal to the maximum and minimum values corresponding to $V_{inDBDC}+V_{swi}/2$ and $V_{inDBDC}-V_{swi}/2$, respectively.

Observing Fig. 2.13, by varying the current I_2 from 1 *mA* to 2 *mA*, the hold feedthrough decreases by 2 *dB*. Basing on the above discussion, a good trade-off is I_2=1.5 *mA* corresponding to a feedthrough of -54.7 *dB*.

2.2.5 DB Track-to-Hold Performance: Pedestal Error

A main phenomenon is the error introduced on the THA output during the transition track-to-hold. This error is called "pedestal error voltage" or simply "pedestal" [1], [6], [7]. It is due to a charge injection on the hold capacitor, during the transition track-to-hold, so determining a perturbation of the voltage held on C_h, after the hold command (see Fig. 2.14).

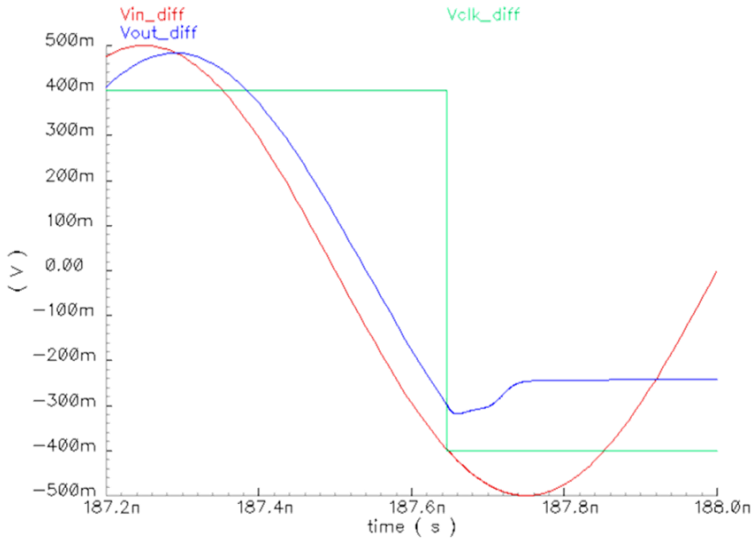

Fig. 2.14. Pedestal error during track-to-hold transition.

This phenomenon can be explained simply considering that during the track phase the bridge diodes are forward biased and so store a

charge that is later expelled while are reverse biased during the hold phase.

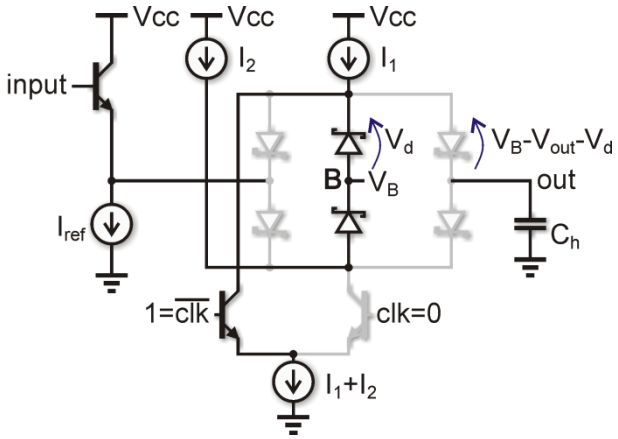

Fig. 2.15. Diode-bridge after the transition track-to-hold.

From the analysis of Fig. 2.15, it can be observed that the reverse biasing voltage on the bridge diodes is dependent on the output voltage as well the charge stored in the bridge diodes, and so also the charge injected onto the hold capacitor depends in non linear manner on the output voltage.

As a consequence, the pedestal determines gain error and, since the diode capacitances are highly non-linear, significant distortion of the signal voltage would also occur [8].

Both of these errors may be eliminated if in the hold mode the node B follows the voltage on the hold capacitor by the bootstrap buffer as shown in Fig. 2.16.

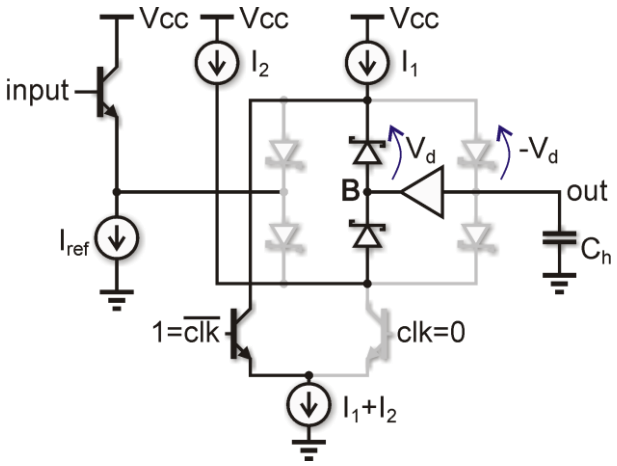

Fig. 2.16. Diode-bridge with bootstrap buffer.

The bootstrapping ensures that the voltage changes on the two diodes connected to the hold capacitor are equal and opposite during the track-to-hold transition and not dependent on the output voltage. Thus the pedestal is cancelled, and the gain and linearity of the THA is increased.

The main performances required to the bootstrap buffer can be summarized as follow:

- it must transfer the output voltage V_{out} to the node B (see Fig. 2.16) without a voltage shift, thus the emitter-follower is a no good solution.
- it must drawn a small current during the transient time avoiding to impact on the pedestal error.
- it must provide a small output resistance, because, as discussed in sub-section 2.2.4, the r_{out} can worsening the signal feedthrough.
- it must drawn a small dc current at the aim to reduce the droop-rate in the hold mode. The droop-rate is the rate of discharge of the hold capacitor during the hold mode [1]. This phenomenon is due to the leakage currents drawn by parasitic dc paths from output node to other nodes, and the value of C_h.
- it must provide a large bandwidth allowing fast track-to-hold transition.

In Fig. 2.17 are depicted three different buffer topologies whose performances have been compared to make the optimal choice with respect to the specifications aforementioned.

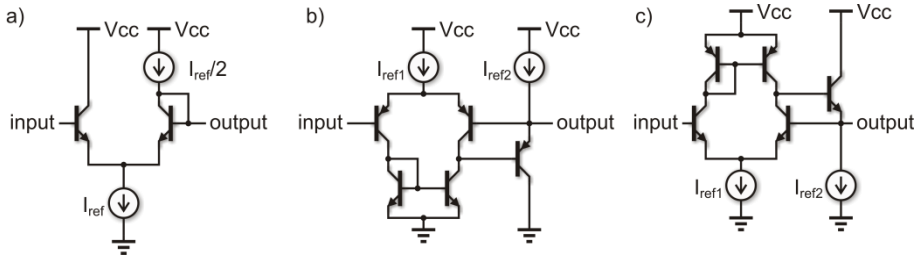

Fig. 2.17. Different unity-gain buffer topologies.

The circuit in Fig. 2.17.a is a simple unity-gain buffer, while in Fig. 2.17.b e Fig. 2.17.c is presented a two-stages voltage follower with PNP and NPN input, respectively.

The performance of the buffer of Fig. 2.17.a is reported in Table 2.I.

Table 2.I

Parameters	**Value**	
I_{ref}	100 μA	1 mA
r_{out}	1.1 $k\Omega$ (DC)	180 Ω (DC)
$I_{in\ DC}$	210 nA	2.8 μA

It can be noted that increasing the bias current decreases the r_{out} and worses the input dc current.

The performances of the circuits in Fig. 2.17.b and Fig. 2.17.c are reported in Table 2.II.

Table 2.II

Parameters	**Fig. 2.17.b**	**Fig. 2.17.c**
I_{ref1}	100 μA	100 μA
I_{ref2}	1 mA	1 mA
BW	15.7 GHz	15.8 GHz
$Gain$	0.999	0.999
$Offset$	18 mV	3.5 mV
r_{out}	24 Ω (DC)	4.3 Ω (DC)
$I_{in\ DC}$	840 nA	230 nA

Choosing $I_{ref1} < I_{ref2}$, allows to obtain a smaller r_{out} and $I_{in\ DC}$, but in the case of Fig. 2.17.b $I_{in\ DC}$ is not small enough due to the β not too high of the PNP transistor. Thus, the best trade-off is obtained with the circuit of Fig. 2.17.c, which is the topology used in the following.

During the transition track-to-hold the pedestal is not the only error source, in fact other sources are the aperture and the clock jitter as will explain in the following sub-sections.

As a consequence, it must be defined a suitable simulation set-up at the aim of observing only the pedestal error effect (see Fig. 2.18).

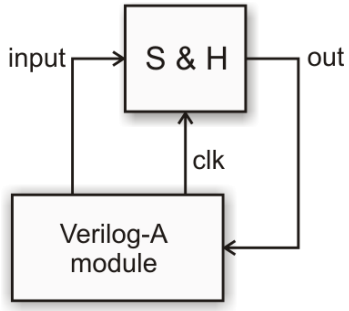

Fig. 2.18. Suitable simulation set-up for the analysis of pedestal.

The other two error sources can be cancelled by using a constant input during the transition track-to-hold. In Fig. 2.18, the *VerilogA* module applies a set of constant inputs, in each clock period, to the THA, then takes the output of THA after the transition to hold mode, next each pair input-output is stored in a data file, that is later processed in Matlab extracting *INL* and gain error.

The numerical simulation results for a DB without or with bootstrap buffer in single-ended and differential configuration for an 8-bits ADC are depicted in Fig. 2.19 and Fig. 2.20, respectively.

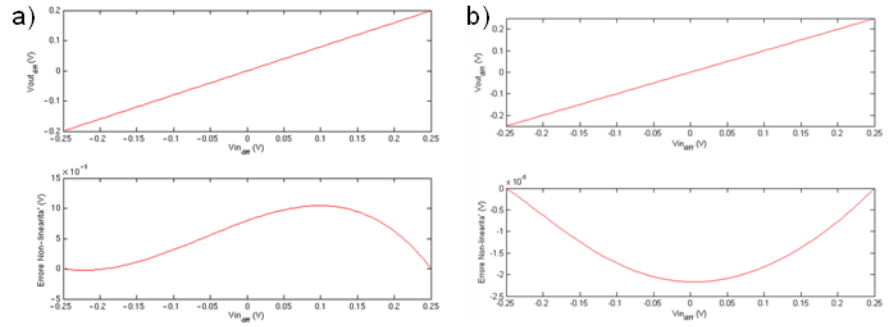

Fig. 2.19. INL and gain error for single-ended DB **a)** without or **b)** with bootstrap buffer.

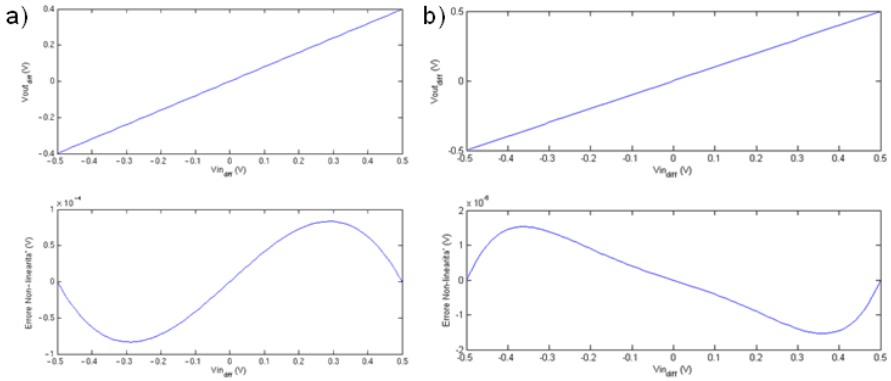

Fig. 2.20. INL and gain error for differential DB **a)** without or **b)** with bootstrap buffer.

The performances are summarized in Table 2.III.

Table 2.III

DB-THA	**Single-ended**		**Differential**	
Buffer	no	yes	no	yes
INL_{max}	104 μV (0.05 LSB)	22 μV (0.01 LSB)	83 μV (0.02 LSB)	1.5 μV (0.00 LSB)
Gain	0.80	0.997	0.80	0.997

It is worth to highlight that both in single-ended and differential configuration the gain error is practically cancelled by using the bootstrap buffer, while the INL_{max} is always better in the differential case, and almost negligible with the bootstrap buffer.

Thus, the DB improved differential circuit with bootstrap buffer has the better performance reducing the pedestal error.

2.2.6 DB Track-to-Hold Performance: Aperture Error

The most essential dynamic property of a SHA is its ability to quickly disconnect the hold capacitor from the input buffer amplifier. The short, but non-zero time interval over which the THA disconnects from the input signal, after the hold command, defines the aperture time or simply aperture (t_A) [6]. This time can be also defined as the time interval between the start of the hold phase and the instant when the bias current of the diode-bridge goes to zero.

In addition to the switching speed of the diode-bridge, the aperture time also sets the maximum rate allowed for the input signal, since if the aperture time is larger than a small fraction of a single period of the input signal, this latter cannot be resolved by the THA.

In other words, the aperture time establishes the highest allowable input frequency imposing an upper limit of approximately l/ t_A on the THA bandwidth.

The aperture time is not constant but is modulated (aperture modulation) by the input signal because it depends on the instantaneous slope of the input signal, so slight variations in the aperture can distort the held output signal.

Thus, the actual value of the voltage that is held at the end of aperture time interval is a function of both the input signal and the errors introduced by the switching operation itself. The value that finally gets held is a delayed version of the input signal, averaged over the aperture time of the switch. The finite time required for the switch to open (t_A) is equivalent to introducing a small delay in the sampling clock driving the THA.

To better understand this phenomenon, it can be considered the bridge response to a variable input signal ($v_{in}(t)=A\cos(2\pi f_{in}t)$). During the track phase the forward biased bridge diodes will make the output ($v_{out}(t)$) follows the input. During the transition track-to-hold the diode-bridge switches, leading the current flowing through it to zero in a finite time. In the presence of a variable input, the bridge aperture persists from the start of the track-to-hold transition until the bridge

current equals the instantaneous current flowing into the hold capacitor ($C_h dv_{in}(t)/dt$) as shown in Fig. 2.21.

Consequently, the aperture depends on the rate-of-change of the input signal. This implies that the input signal is sampled with different aperture, based on its instantaneous derivative, thus resulting in a non-uniform sampling and introducing distortion of the output signal.

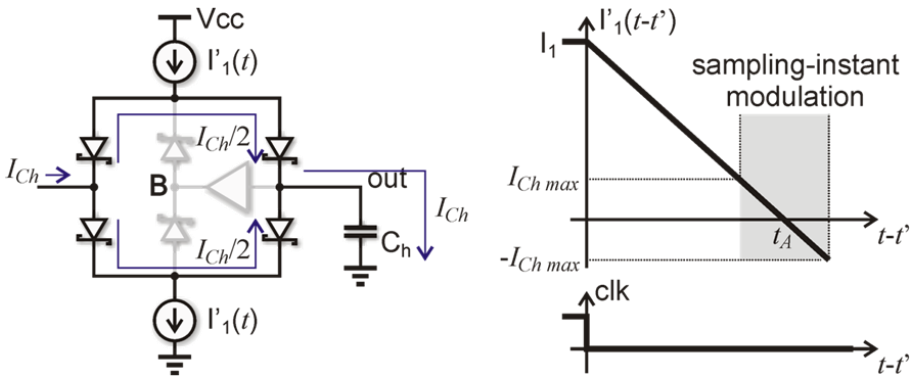

Fig. 2.21. Diode-bridge: aperture error

Now, it can be analyzed the perturbation introduced by the aperture, considering the equivalent circuit in Fig. 2.21, in the hypothesis that the bridge bias current decreases linearly as shown in Fig. 2.21.

The bridge diodes are turned-off and the voltage is held on the hold capacitor when the current entering the hold capacitor I_{Ch} equals the bridge bias current I_1 and it can be written

$$I_{Ch} \approx C_h \frac{dv_{in}}{dt} = -I_{Ch\,max} \sin(2\pi f_{in} t) \tag{2.30}$$

where $I_{Ch\,max}=2\pi f_{in} C_h A$.

The sampling time instant t_s changes deterministically as function of the input signal (see Fig. 2.21), and it follows

$$t_s = t' + t_A \left(1 - \frac{I_{Ch}(t_s)}{I_1}\right) \tag{2.31}$$

this relation defines implicitly the sampling time instant.

For sake of simplicity, I_{Ch} is supposed constant over the modulation time interval, it can be written

$$I_{Ch}(t_s) \simeq I_{Ch}(t'+t_A) \quad \Rightarrow \quad t_s = t'+t_A\left(1-\frac{I_{Ch}(t'+t_A)}{I_1}\right) \tag{2.32}$$

and the output voltage can be derived as

$$v_{out}(t_s) = A\cos(2\pi f_{in}t_s) = A\cos(2\pi f_{in}\tau + \beta\sin(2\pi f_{in}\tau)) \tag{2.33}$$

where $\tau = t' + t_A$ takes into account time delay and distortion, in fact the non uniform sampling in the time variable t becomes uniform in τ, but with a different function (see eq. (2.33)), in which the sine function modules the cosine, resulting in output distortion. Thus, the aperture modulation is analogous to phase modulation and can be analyzed identically. From eq. (2.33), we have

$$\beta = \frac{AC_h(2\pi f_{in})^2}{I_1}t_A \tag{2.34}$$

it can be represented as a Fourier series, whose coefficients do not have a closed-form expression, but, as Bessel functions, they are well-known, and after some calculations for a differential diode-bridge it can be written

$$\begin{cases} HD_2 = 0 \\ HD_3 \cong \mathrm{J}_2(\beta) \approx \beta^2/8 \end{cases} \tag{2.35}$$

where $J_2(\beta)$ is the Bessel coefficient.

In the following Table 2.IV are reported the parameters design values.

Table 2.IV

Parameters	Value
A	0.25 V
C_h	100 fF
f_{in}	1 GHz
I_1	1.4 mA
t_A	50 ps

It is worth to highlight that a simulation of the diode-bridge with a clock rise (fall) time of 100 *fs* results in aperture time about ten *ps*. Thus, the aperture distortion can be properly evaluated only if the aperture time is comparable with the clock rise time. For this reason, the diode-bridge was tested under dynamic conditions with a clock rise time value equal to 50 *ps* since in this case, the aperture time is

about 50 *ps*, and it is possible to observe the phenomenon of the aperture distortion as follows

$$HD_3 \approx 76\,dB \tag{2.36}$$

Recalling that the harmonic distortion introduced by the diode-bridge during the track phase (I_1=1.4 *mA*) is equal to 58 *dB*, the distortion introduced by the aperture error (eq. (2.36)) can be considered negligible with respect to that in the track mode.

At the aim to evaluate the effect of bandwidth limitation and distortion in track mode, pedestal and aperture error, hold-mode feedthrough and droop-rate on the THA performance, a transient simulation without noise (excluding other phenomena like jitter) has been performed. The suitable simulation set-up is described in Fig. 2.22.

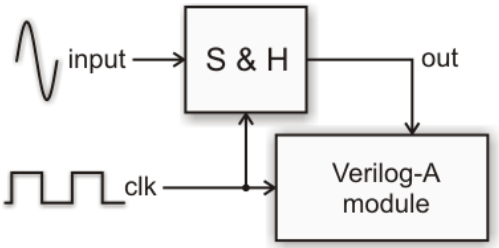

Fig. 2.22. Simulation set-up: diode-bridge overall performance without noise.

The samples provided by the sample-and-hold are the inputs of the *VerilogA* module that stores the samples in a data file for the subsequent processing in the Matlab tool. It is worth recalling that the test in down-sampling entails, according to the design constraints, an analog input signal at the frequency f_{in}=1 *GHz* with a sample rate f_s=200 *MHz* corresponding to a sampling (clock) period T_s=5 *ns*. In this case, it has been fixed a clock period equal to T_{clk}=5 *ns*+1 *ns*/N_{pt} where N_{pt}=256 is the number of simulation points. This implies that T_{clk}=5.004 *ns* corresponding to a sample rate f_s=199.8 *MHz* assuring that after N_{pt}=256 cycles it is obtained exactly a period of the input signal. The resulting frequency of the digital output is equal to f_{out}=781 *kHz*= f_s/256.

The simulation results are reported in Fig. 2.23.

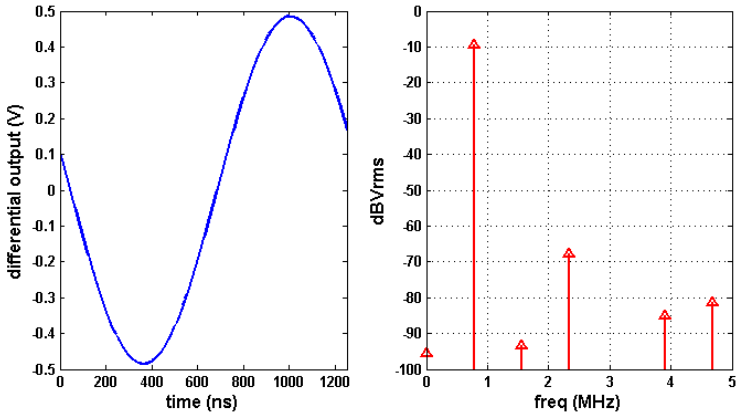

Fig. 2.23. Down-sampling test of the diode-bridge.

The resulting total harmonic distortion is 58 *dB* corresponding to an *ENOB*=9.34.

2.2.7 DB Track-to-Hold Performance: Clock Jitter

As discussed in the previous sub-section the fall-time of the clock signal impacts on the aperture time or rather if the clock fall-time is comparable with the aperture time, the aperture distortion becomes detectable, but, as seen, not significant.

From the Fig. 2.24 can be defined the clock fall-time as

$$t_{fall} \approx \frac{V_{sw}}{dv_{clk}/dt} \tag{2.37}$$

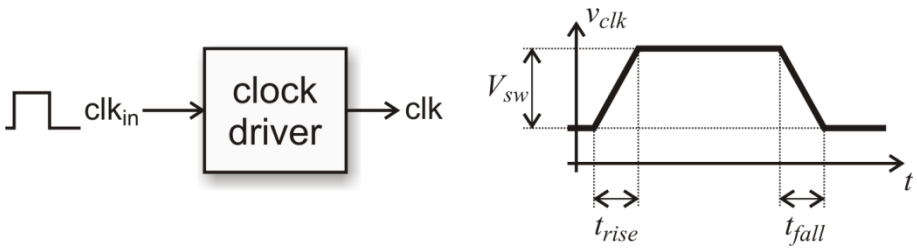

Fig. 2.24. Fall-time of the clock signal.

It can be noted that an increase of dv_{clk}/dt reducing the fall-time. The output noise σ_{Vclk} determines a sampling time jitter

$$\sigma_t \approx \frac{\sigma_{v_{clk}}}{dv_{clk}/dt} \tag{2.38}$$

worsening the *SNR*, so, once again, it is desirable to have dv_{clk}/dt as high as possible.

The clock jitter depends on the clock driver circuit. The clock driver designed and used in this work is an ECL circuit with a cross-coupled current biasing [9], as shown in Fig. 2.25.

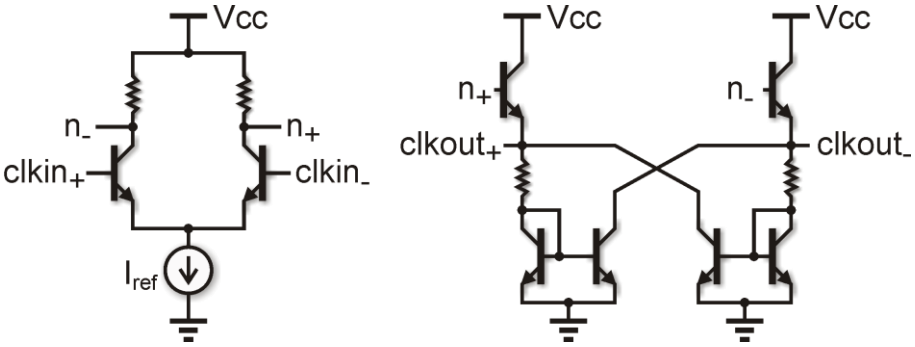

Fig. 2.25. Clock driver circuit

The input stage is an emitter-coupled pair whose input signals ($clkin_+$, $clkin_-$) assume the values V_{clkH}=1.4 *V* and V_{clkL}=1.0 *V* for their high and low voltage, respectively. This latter according to the design constraints, discussed in the section 2.2, assuring the correct circuit operation.

The outputs of this stage are the inputs of the subsequent stage, or rather are the inputs of two bipolar transistors in common collector fashion, on the emitters of which are taken the signals driving the THA.

Considering a capacitive load $C_{clk}=C_{clkout+}=C_{clkout-}$=170 *fF*, the transient response of the circuit is depicted in Fig. 2.26. The resulting fall-time is equal to 42 *ps*, the output noise σ_{Vclk}=1.159 mV_{rms}, while the signal slope is dv_{clk}/dt=17.3 *V/ns*, so determining the following rms jitter

$$\sigma_t \approx \frac{\sigma_{v_{clk}}}{dv_{clk}/dt} = 67 \ fs \tag{2.39}$$

The clock jitter translates in white noise at the THA output, worsening the overall *SNR*.

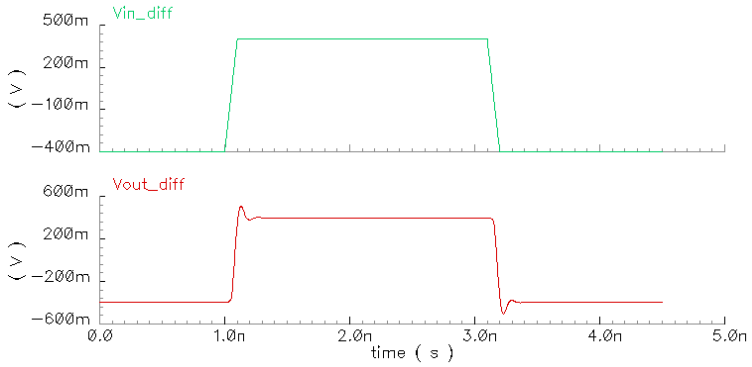

Fig. 2.26. Transient response (red line) of the clock driver to a differential input (green line).

This effect can be taken into account considering the *SNR* purely due to the jitter, as discussed in sub-section 1.5.1. Recalling eq. 1.18, reported below

$$SNR_{dB} = -20\log_{10}(\sigma_t 2\pi f_{in}) \tag{2.40}$$

substituting eq. (2.39) in (2.40) it follows

$$SNR(@1\,GHz) = 67.5\,dB \tag{2.41}$$

corresponding to an *ENOB*=10.9.

It is clear that this value for the time jitter is not relevant in terms of the overall converter performance.

2.2.8 Diode-Bridge Performance: Simulation Results

In this section are reported the simulation results related to the diode-bridge behavior taking into account the error sources whose effects have already been evaluated in sub-section 2.2.6, including also the sampling time jitter and the noise generated by the THA.

For this purpose, a transient simulation with generated noise has been performed, and its set-up is shown in Fig. 2.27.

The samples provided by the sample-and-hold are the inputs of the *VerilogA* module that stores the samples in a data file for the subsequent processing in the Matlab tool. It is worth recalling that the test in down-sampling entails, according to the design constraints, an analog input signal at the frequency f_{in}=1 *GHz* with a sample rate f_s=200 *MHz* corresponding to a sampling (clock) period T_s=5 *ns*. In

this case, it has been fixed a clock period equal to T_{clk}=5 *ns*+5 *ns*/N_{pt} where N_{pt}=256 is the number of simulation points. This implies that T_{clk}=5.019 *ns* corresponding to a sample rate f_s=199.22 *MHz*. The resulting frequency of the digital output is equal to f_{out}=3.89 *MHz*=5f_s/256.

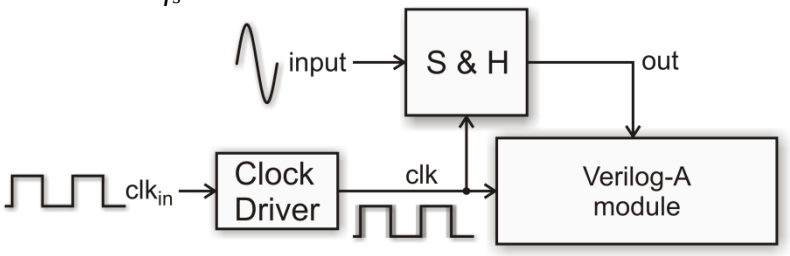

Fig. 2.27. Simulation set-up: diode-bridge overall performance.

The simulation results are reported in Fig. 2.28 and in Table 2.V. It can be noted that the value of the harmonic distortion is similar to that evaluated without clock driver and noise generator, confirming its not relevant impact on the THA overall performance.

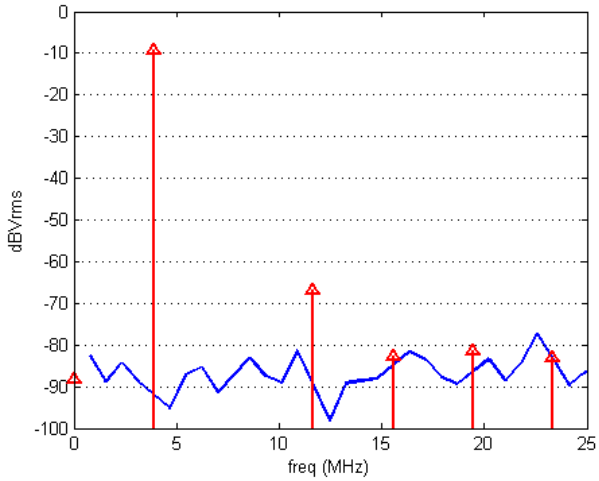

Fig. 2.28. Diode-bridge dynamic response in the frequency domain.

Table 2.V

Diode-Bridge	
THD	57.2 *dB* (9.21 bits)
SNR	55.0 *dB* (8.84 bits)
SNDR	53.0 *dB* (8.50 bits)

It worth highlighting that all the numerical simulation results presented previously have been obtained considering ideal current sources as biasing elements of THA circuit.

At the aim to evaluate the actual performance of the diode-bridge the ideal current sources have been replaced by suitable current mirrors made with active devices. A great attention has been devoted to minimize as much as possible the impact of the current mirrors on the THA performances.

In the following the results will include the effect of the current mirrors.

It will be shown the characteristic time intervals of the THA operation (see Fig. 2.29):

- *Settling track time (acquisition time)* is the non-zero time interval required, after the track command, for the THA output to recover tracking the input ensuring that the subsequent hold mode output will be within a specified error band of the input level that existed at the instant of the sample-and-hold conversion within a specified error band.
- *Settling hold time* is the non-zero time interval required, after the hold command, for the THA to settle within a specified error band around its final value.

These characteristic time intervals fix, in the worst case, an upper limit to the sampling frequency as follows

$$f_{s\max} = \frac{1}{2t_{w.c.}} \tag{2.42}$$

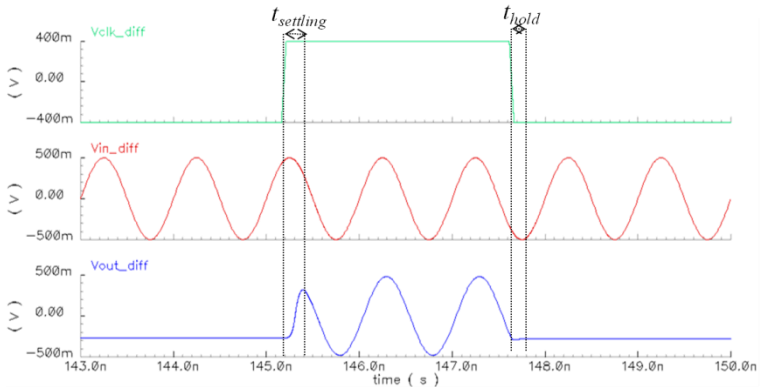

Fig. 2.29. Settling track and hold time of diode-bridge.

In this case we have

$$\begin{cases} t_{settling} = 430\ ps \\ t_{hold} = 100\ ps \end{cases} \Leftrightarrow \quad f_{s\max} = 1/2t_{w.c.} = 1/2t_{settling} = 1.2\ GHz \quad (2.43)$$

The diode-bridge frequency response, depicted in Fig. 2.30, highlights a bandwidth equal to 3.87 *GHz*.

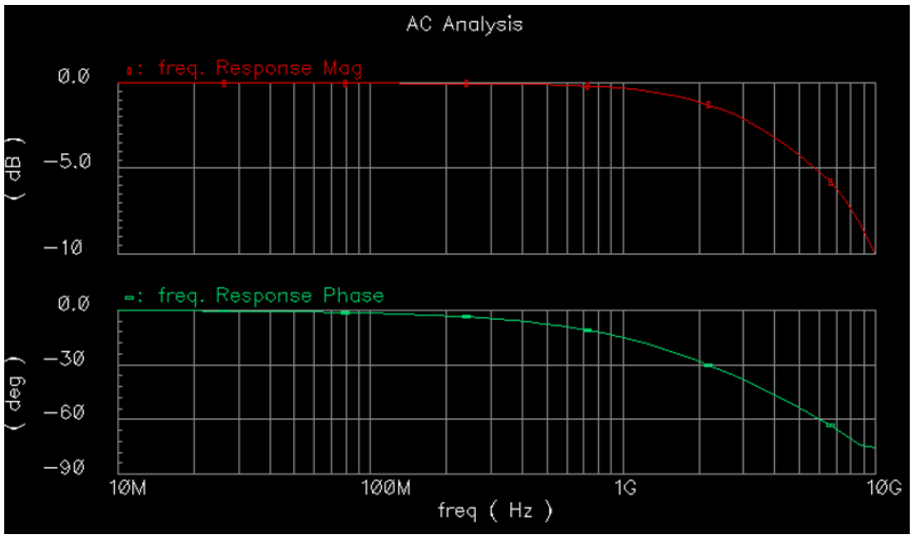

Fig. 2.30. Frequency response of the diode-bridge.

Now, the final results of the diode-bridge in both the differential and single-ended configurations can be reported and compared.

The behavior of the effective number of bits as function of the input frequency in both differential and single-ended configurations is shown in Fig. 2.31 and Fig. 2.32, respectively.

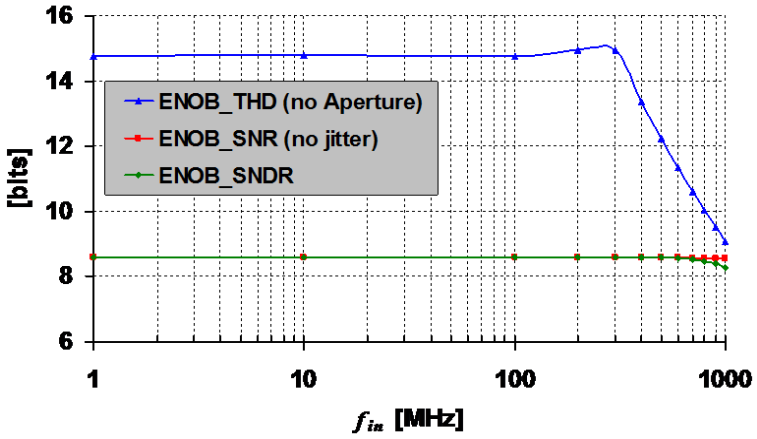

Fig. 2.31. ENOB versus f_{in} (diode-bridge differential mode).

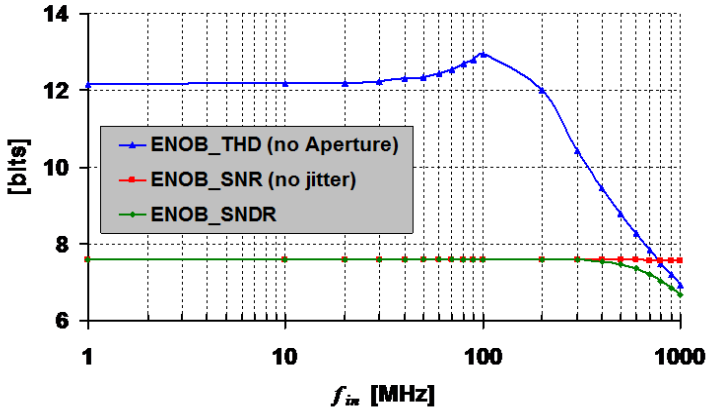

Fig. 2.32. ENOB versus f_{in} (diode-bridge single-ended mode).

The final performances are reported in Table 2.VI. It can be noted that the differential circuit configuration shows better performances with respect to the single-ended solution.

Table 2.VI

Diode-Bridge	Differential	Single-Ended
Supply voltage	3.6 *V*	3.6 *V*
THD(@1 GHz)	53.7 *dB* (8.63 *bits*)	42.0 *dB* (6.68 *bits*)
THD(@500 MHz)	66.6 *dB* (10.77 *bits*)	51.6 *dB* (8.28 *bits*)
SNR	52.3 *dB* (8.40 *bits*)	46.4 *dB* (7.42 *bits*)
SNDR(@1 GHz)	50.0 *dB* (8.01 *bits*)	40.6 *dB* (6.46 *bits*)
SNDR(@500 MHz)	52.7 *dB* (8.46 *bits*)	45.6 *dB* (7.28 *bits*)
hmf(@1 GHz)	-51.0 *dB*	-51.0 *dB*
hmf(@500 MHz)	-57.7 *dB*	-57.7 *dB*
Droop-rate	70 *μV/ns*	56 *μV/ns*
Bandwidth	3.87 *GHz*	3.86 *GHz*
Power Dissipation	47 *mW*	47 *mW*

2.3 Switched Emitter Follower (SEF)

This section is devoted to the analysis and design of a THA circuit using as switch a switched emitter follower (SEF) structure. This latter is a proven technique for high-speed analog switches using SiGe heterojunction bipolar transistor (HBT) technology [10]-[14]. Furthermore, with the use of SiGe HBT devices, SEF architecture takes advantage of the high linearity, cut-off frequency and superior mismatch performance shown by SiGe HBT devices [15].

A popular input stage implementation is the emitter degenerated differential pair with logarithmic loads [10], [16]. This solution suffers the bias voltage required across the diode connected bipolar loads, so limiting the use of low power supply. To overcome this limitation the SEF circuit designed in this work presents an input stage obtained with a differential pair with split emitter currents, while the collector series diodes have been omitted (see Fig. 2.33).

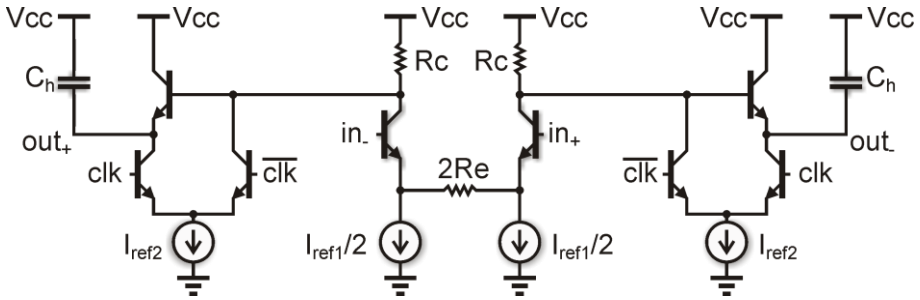

Fig. 2.33. Simplified schematic of the SEF circuit.

The first advantage of the SEF with respect to the diode-bridge is the differential configuration of the input stage that provides a common-mode rejection useful to obtain good performance also in the single-ended mode.

Fig. 2.34 shows the track mode configuration (*clk*=1). It can be noted that in this phase the circuit is essentially a differential pair followed by an emitter follower. The maximum output (out_1, out) signal swing is

$$V_{swout} = R_c I_{ref1} \tag{2.44}$$

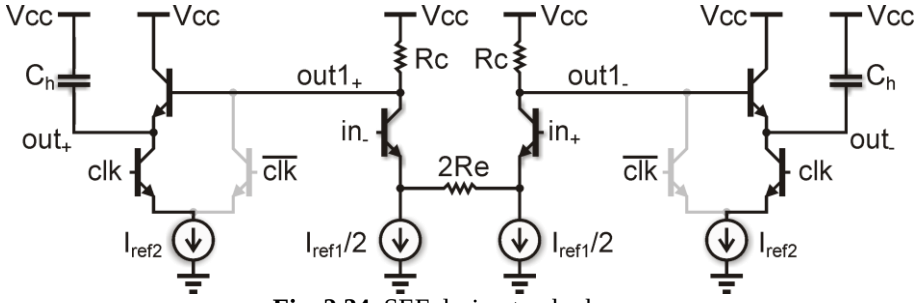

Fig. 2.34. SEF during track phase.

Fig. 2.35 shows the hold mode configuration (*clk*=0). During this phase the voltage of the nodes out_1 drops by an amount equal to

$$\Delta V_{out} = R_c I_{ref2} \tag{2.45}$$

The value of ΔV_{out} should assure that the emitter-follower transistors are off during this phase.

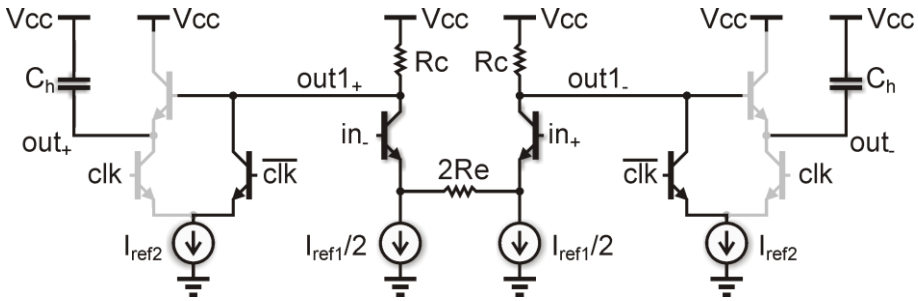

Fig. 2.35. SEF circuit in the hold mode.

From the above discussion, the correct operation of the circuit requires to fix some constraints on the different voltage levels present in the circuit itself (see Fig. 2.36).

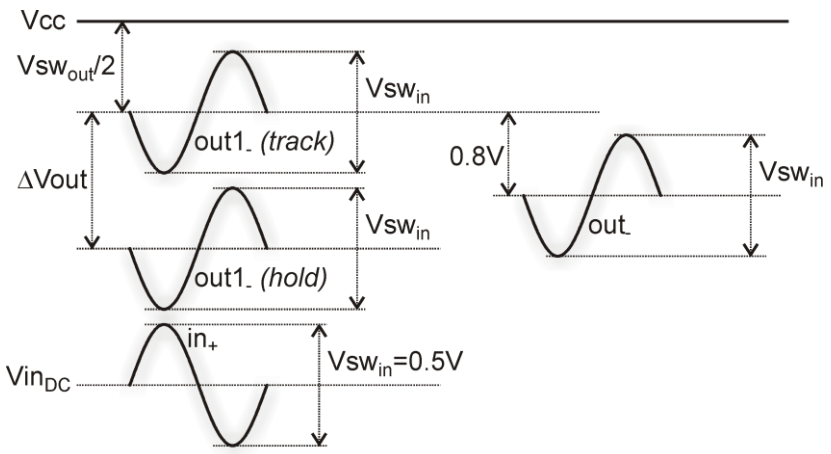

Fig. 2.36. SEF voltage levels relationships.

The two main constraints derive from the need that the input differential pair is never off and the output emitter follower are off during hold mode. In order to assure these constraints, the following relations must be satisfied

$$V_{swout} > V_{swin} \tag{2.46}$$

$$\Delta V_{out} > V_{swin} \tag{2.47}$$

The constraint established by eq. (2.46) is useful to guarantee that the voltage drop on the base-collector junction of the transistors of the input differential pair is such as to ensure non saturation of the input transistors.

The constraint established by eq. (2.47) is useful to guarantee that the base-collector junction of the emitter follower (see Fig. 2.35) is reverse biased during the hold mode. Thus, considering that the base voltage decreases by ΔV_{out} with respect to the value in the track mode, when the emitter voltage (out) is tracking the input voltage, ΔV_{out} must be larger than the full swing of the input signal.

2.3.1 SEF Track Mode Performance: Gain and Distortion Analysis

The analysis of the non linear behavior of the SEF circuit can start from the non linearity analysis of its input stage (Fig. 2.37). Thus, from a small signal point of view the gain A_v of the input differential pair can be easily expressed as

$$A_v = \frac{2\mathrm{Rc}}{g_{m1}^{-1} + g_{m2}^{-1} + 2\mathrm{Re}} \tag{2.48}$$

where $g_m = I_c/V_T$ (I_c, collector current; V_T, thermal voltage) is the BJT transconductance.

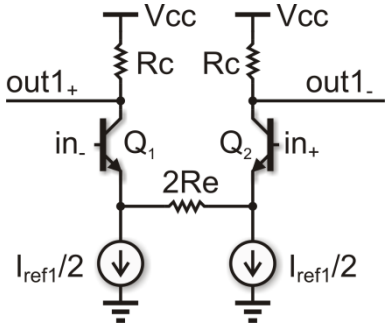

Fig. 2.37. SEF: input stage.

Eq. (2.48) suggests that the gain varies as function of the differential input voltage because I_{c1}, I_{c2} vary. It must be also noted that the gain is temperature dependent through the thermal voltage.

Hence, the non linearity expressed by (2.48) arises because the denominator is in part a current-dependent impedance.

The gain A_v becomes less input and temperature dependent as 2Re becomes much greater than $g_{m1}^{-1} + g_{m2}^{-1}$.

For a temperature analysis, considering $v_{in+} = v_{in-}$ it can be written

$$A_v = \frac{\mathrm{R\,c\,I_{ref\,1}}}{2V_T + \mathrm{Re\,I_{ref\,1}}} \tag{2.49}$$

suggesting that a reduced dependence on the temperature can be obtained if results

$$\mathrm{Re\,I_{ref\,1}} \gg 2V_T \quad \Leftrightarrow \quad V_{swout} >> 2V_T \frac{\mathrm{Rc}}{\mathrm{Re}} \tag{2.50}$$

the gain can be rewritten as

$$A_v = \frac{\mathrm{Rc}}{\mathrm{Re}} \tag{2.51}$$

determining a unity gain if

$$\frac{\mathrm{Rc}}{\mathrm{Re}} \approx 1 \quad \Leftrightarrow \quad A_v = 1 \tag{2.52}$$

The static linearity of the differential pair in the track mode can be analyze using the small-signal gain in (2.48) and considering that the bias current I_{ref1} is equally split into the two branches of the differential pair if the differential input voltage is zero, otherwise it can be written

$$\begin{cases} g_{m1} = \dfrac{I_{ref\,1}/2 + \Delta I}{V_T} \\ g_{m2} = \dfrac{I_{ref\,1}/2 - \Delta I}{V_T} \end{cases} \tag{2.53}$$

Hence, eq. (2.48) becomes

$$A_v = \frac{2\,\mathrm{Rc}}{\dfrac{V_T}{I_{ref\,1}/2 + \Delta I} + \dfrac{V_T}{I_{ref\,1}/2 - \Delta I} + 2\,\mathrm{Re}} = \\ = \frac{\mathrm{Rc}\,I_{ref\,1}}{\dfrac{V_T}{(1 + 2\dfrac{\Delta I}{I_{ref\,1}})} + \dfrac{V_T}{(1 - 2\dfrac{\Delta I}{I_{ref\,1}})} + \mathrm{Re}} \tag{2.54}$$

Considering that $\Delta I/I_{ref1}<<1$ and remembering that the Taylor series, stopped at the second order, of the function $1/(1+x)$ for $x<<1$ is $1/(1+x) \simeq 1-x+x^2$, eq. (2.54) can be easily rewritten as

$$A_v \simeq \frac{\mathrm{Rc}\, I_{ref1}}{2V_T + 2V_T \left(\frac{\Delta I}{I_{ref1}} \right)^2 + \mathrm{Re}\, I_{ref1}} \tag{2.55}$$

Considering that $\mathrm{Re} \gg 2V_T$, the linearity can be improved reducing the dependence on ΔI, hence obtaining the following constraint

$$2V_T \cdot \left(\frac{\Delta I}{I_{ref1}} \right)^2 \ll \mathrm{Re}\, I_{ref1} \tag{2.56}$$

and taking into account the maximum value of ΔI

$$\Delta I_{\max} = \frac{V_{swin}/2}{Rc} \tag{2.57}$$

substituting (2.57) in (2.56) and recalling eq. (2.44), it follows

$$V_{swout}^3 \gg 2V_T V_{swin}^2 \frac{\mathrm{Rc}}{\mathrm{Re}} \tag{2.58}$$

Eq. (2.58) tightens up the constraint on the output voltage swing discussed previously and reported in eq. (2.50).

In the hypothesis of unity gain of the differential input buffer (Rc/Re=1, see eq. (2.52)) the static non-linearity SEF behavior as function of the output voltage swing is depicted in Fig. 2.38. It can be noted that reducing the output voltage swing decreases the maximum circuit non-linearity.

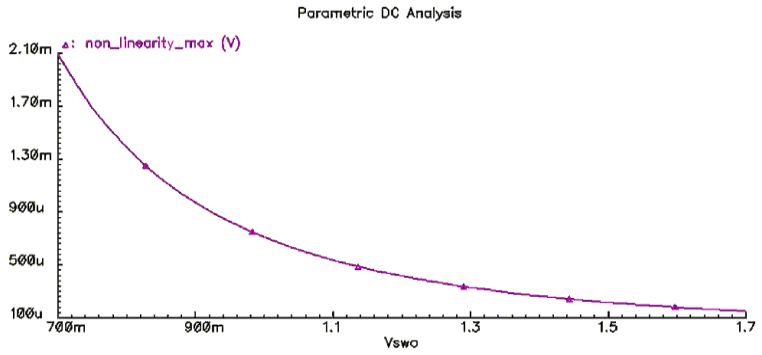

Fig. 2.38. Static non-linearity versus output voltage swing.

A rigorous study of the dynamic non-linearity of the differential stage in the track mode requires an huge analysis using complex mathematical approach. In this case, unlike what happens in the diode bridge, the *THD* does not depend on the hold capacitor C_h. In fact, the SEF performance in terms of harmonic distortion is limited by the input differential stage and the main contribution is due to the current flowing through C_μ (Fig. 2.39).

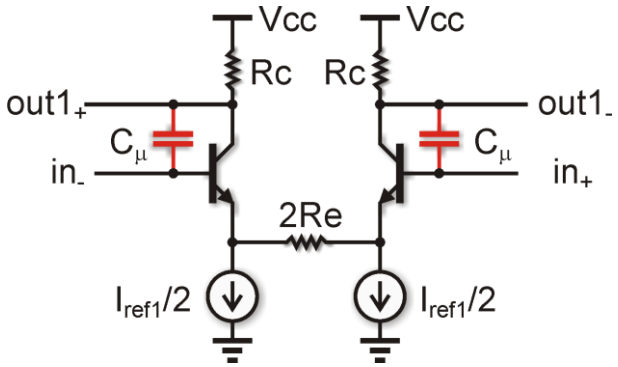

Fig. 2.39. Scheme of the input stage for dynamic distortion analysis.

The non-linearity arises because the dependence of C_μ on the collector-base voltage drop of the differential pair transistors. For sake of clarity it can be considered the simplified model of Fig. 2.40.

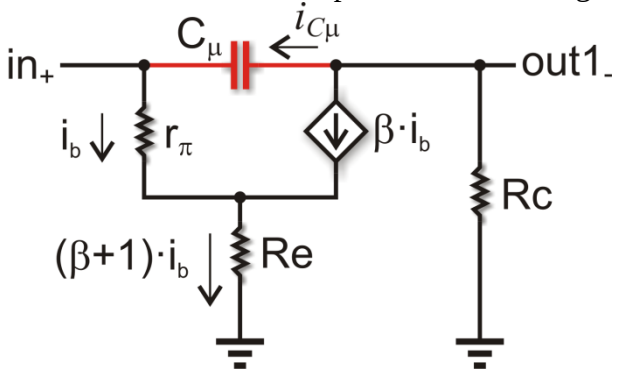

Fig. 2.40. Small-signal equivalent circuit for dynamic distortion analysis.

The current flowing through C_μ is

$$i_{C\mu} = \frac{d}{dt}\left[C_\mu V_{CB}\right] \tag{2.59}$$

while the capacitance C_μ can be easily expressed as

$$C_\mu(V_{CB}) = \frac{C_{j0}}{\sqrt{1+\frac{V_{CB}}{V_{j0}}}} \tag{2.60}$$

where $V_{CB} = V_{out-} - V_{in+}$ and assuming that the small-signal component of the input signal is equal to that of the output signal or rather $v_{out-} \simeq v_{in+}$, it can be written

$$V_{CB} \simeq 2V_{in+} + V_{swin} + \Delta V_{out} \tag{2.61}$$

The behavior of C_μ by varying V_{CB} is depicted in Fig. 2.41. If ΔV_{out} increases the linearity improves.

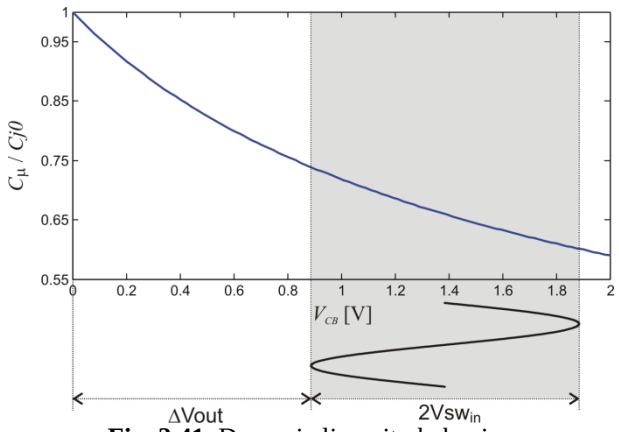

Fig. 2.41. Dynamic linearity behavior

Furthermore, the numerical simulation results (see Fig. 2.42) confirm that the harmonic distortion *THD* improves as ΔV_{out} increases.

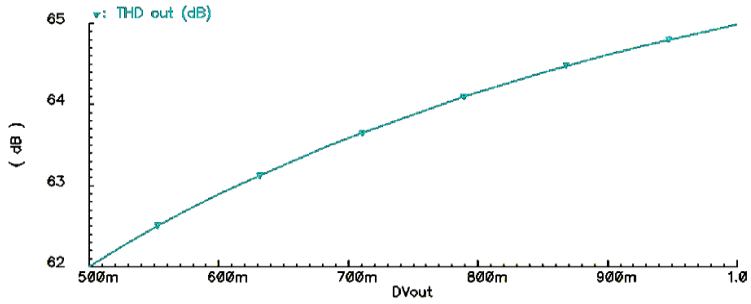

Fig. 2.42. SEF harmonic distortion as function of $\Delta Vout$ (f_{in}=1 *GHz*; Rc/Re=1).

From the above discussion it is now possible to establish a trade-off between static and dynamic linearity of the SEF circuit.

Firstly, it is important to recall the constraints imposed by eqs. (2.46), (2.47) and reported below for clarity

$$V_{swout} > V_{swin} \tag{2.62}$$

$$\Delta V_{out} > V_{swin} \tag{2.63}$$

then, the other constraints establishing the non-saturation of the circuit devices must be taken into account. Fig. 2.43 shows the SEF schematic circuit in which are also labeled the bias voltage values avoiding the device saturation.

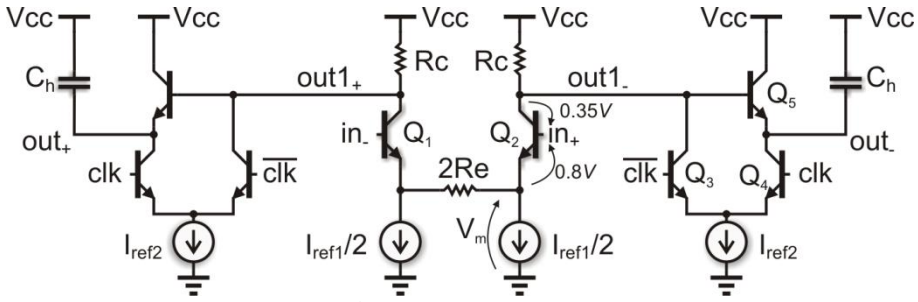

Fig. 2.43. SEF circuit

In order to assure a proper circuit operation, avoiding the saturation of Q_1, Q_2 the following condition is imposed

$$V_{in\max} - V_{out\min} \le 0.35V \;\Rightarrow\; V_{CE\min} = V_{BE} - V_{BC} = 0.45V \tag{2.64}$$

where the maximum input voltage and the minimum output voltage can be expressed as

$$\begin{aligned} V_{in\max} &= V_{inDC\max} + \frac{V_{swin}}{2} \\ V_{out\min} &= V_{CC} - \frac{V_{swout}}{2} - \frac{V_{swin}}{2} - \Delta V_{out} \end{aligned} \tag{2.65}$$

Recalling eq. (2.63) ΔV_{out} can be obtained as follows

$$\Delta V_{out} = V_{swin} + 0.1V \tag{2.66}$$

where 0.1 V represents a suitable margin to achieve the desired goal.

Recalling (2.64), (2.65), it follows

$$V_{inDC\max} \le V_{CC} - V_{swin} - \frac{V_{swout}}{2} - \Delta V_{out} - 0.35V \tag{2.67}$$

Now as shown in Fig. 2.43, considering V_m the minimum voltage drop across the current mirror, here replaced with an ideal current source, the following constraint on the emitter voltage (of Q_2) must be imposed

$$V_{E\min} \ge V_m \;\Rightarrow\; V_{inDC\min} \ge V_m + \frac{V_{swin}}{2} + 0.8V \tag{2.68}$$

From (2.67), (2.68) can be obtained the input dc range as

$$V_{inDC\max} - V_{inDC\min} = V_{CC} - 0.45V - \frac{V_{swout}}{2} - 3\frac{V_{swin}}{2} - V_m - \Delta V_{out} \tag{2.69}$$

Now, imposing that the dc input range is greater or equal to zero and $V_m = V_{CE\min} = 0.45V$, (2.69) becomes

$$V_{CC} - 0.9V - \frac{V_{swout}}{2} - 3\frac{V_{swin}}{2} - \Delta V_{out} \ge 0 \tag{2.70}$$

Relation (2.70) highlights a trade-off between "static" ($V_{sw\ out}$) and "dynamic" (ΔV_{out}) linearity, thus increasing ΔV_{out} to achieve better dynamic performance means reducing $V_{sw\ out}$, so worsening static performance.

Recalling the simulation results presented in Fig. 2.38 and Fig. 2.42, a compromise choice can be

$$\begin{aligned} \Delta V_{out} &= 0.9V \\ V_{swout} &= 1.5V \end{aligned} \tag{2.71}$$

corresponding to a *THD*, at the input frequency of 1 *GHz*, equal to 64.6 *dB* (10.44 bits) and a maximum static non-linearity of 233 μV. Furthermore, this choice assures the correct operation of the transistors Q_3, Q_4, Q_5 (see Fig. 2.43) and their counterpart on the left side of the circuit.

After the design of the SEF based on the sizing choices aforementioned, the output frequency spectrum of the SEF is reported in Fig. 2.44 and Fig. 2.45 (differential and single-ended configuration, respectively).

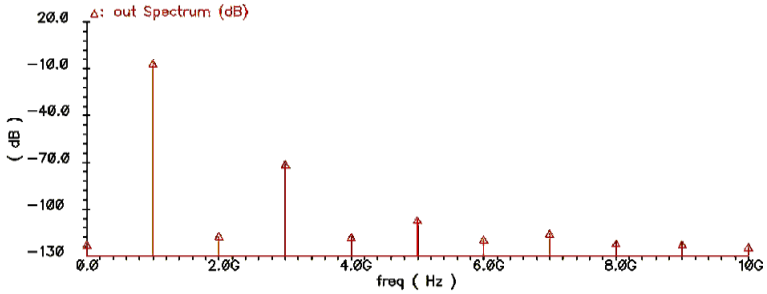

Fig. 2.44. SEF differential mode: output spectrum.

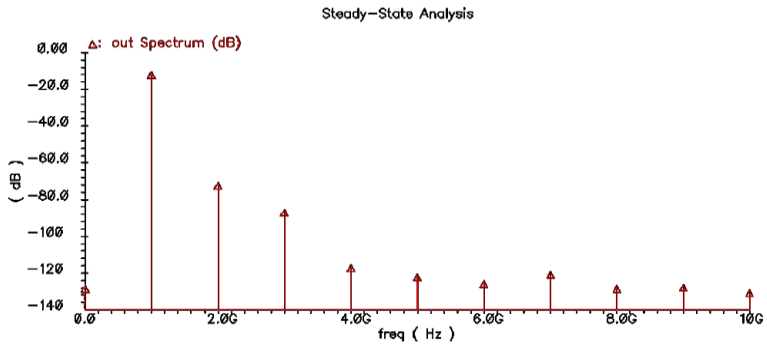

Fig. 2.45. SEF single-ended mode: output spectrum.

The resulting *THD* is equal to 64.6 *dB* (10.44 bits) in the differential mode and 60.4 *dB* (9.74 bits) in the single-ended mode. In both cases, under the same operating conditions, the switched emitter follower shows better performance than the diode-bridge (see sub-section 2.2.3).

2.3.2 SEF Track Mode Performance: Noise Analysis

As already discussed for the diode-bridge in sub-section 2.2.2, a rigorous noise analysis is very complex due to the large number of error sources. Thus, also for the switched emitter follower, considering only the emitter-follower, whose noise performance depending on the transistor, it can be shown (see [5]) that the noise on the hold capacitor is

$$V_{n,C_h}^2 = \gamma \cdot \frac{kT}{C_h} \qquad \gamma = \frac{1}{2} + \beta \cdot \frac{r_b}{r_\pi} \tag{2.72}$$

It can be noted that, in a first approximation, the noise (*SNR*) only depends on the hold capacitor. Furthermore, some numerical simulations have confirmed that this approximation also occurs for the SEF circuit.

At the aim of a correct sizing of C_h the relationship with the *SNR* must be taken into account.

The *SNR* depends on the capacitance of C_h, which should be sized to get a good margin on the *SNR* according to the design constraints. A parametric analysis has been performed, by varying the C_h value, obtaining the *SNR* as function of C_h (see Fig. 2.46).

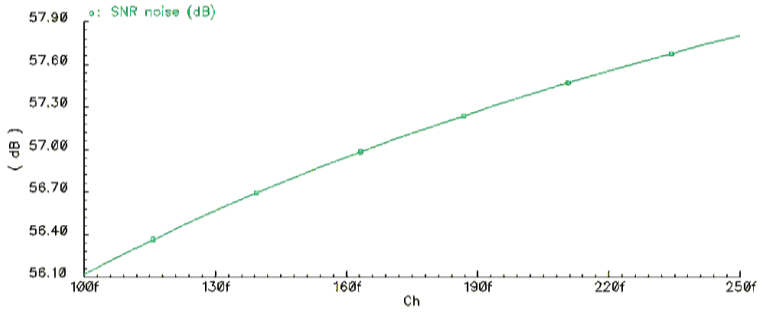

Fig. 2.46. *SNR* versus C_h.

The choice of C_h is made for obtaining an *ENOB* beyond 9. In this case of a differential SEF with ideal current sources, it has chosen a capacitance value (200 *fF*) corresponding to a *SNR*=57.4 *dB*, hence an *ENOB* equal to 9.2 (as in sub-section 2.2.3 for the DB).

2.3.3 SEF Track Mode Performance: Bandwidth

As discussed in sub-section 2.2.1, the THA must have a bandwidth greater than that of the maximum expected input signal and it must settle to the specified accuracy in a short amount of time, usually much less than half a clock cycle.

Unlike the diode-bridge, the SEF bandwidth depends only on the bias currents. In fact, once fixed the value of the hold capacitance too high as in this case (C_h=200 *fF*), the bandwidth is limited by the output circuit (i.e. emitter-follower) as shown in Fig. 2.47.

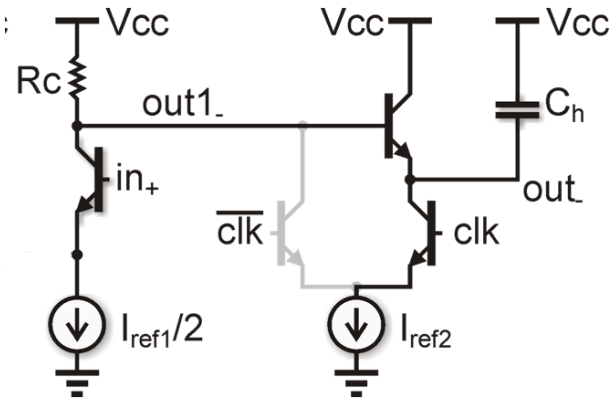

Fig. 2.47. SEF output circuit for bandwidth analysis.

From the analysis of the circuit in Fig. 2.47, it can be derived the bandwidth as

$$BW \simeq \frac{1}{2\pi C_h \frac{r_\pi + \mathrm{Rc}}{\beta + 1}} \tag{2.73}$$

where $r_\pi = \beta \frac{V_T}{I_{ref\,2}}$; $\mathrm{Rc} = \frac{V_{swout}}{I_{ref\,1}}$ and considering that $\frac{I_{ref\,1}}{I_{ref\,2}} = \frac{V_{swout}}{\Delta V_{out}}$, r_π can be rewritten as follows

$$r_\pi = \beta \frac{V_T}{I_{ref\,1}} \frac{\Delta V_{out}}{V_{swout}} \tag{2.74}$$

It is immediately apparent that the bandwidth depends on I_{ref1}, once fixed C_h, and increasing I_{ref1} improves the bandwidth. Thus, a parametric analysis has been performed, by varying the I_{ref1} value, obtaining the corresponding bandwidth as function of I_{ref1} (see Fig. 2.48). Therefore, a bias current I_{ref1}=4.5 *mA* has been chosen corresponding to a bandwidth of 5.5 *GHz*.

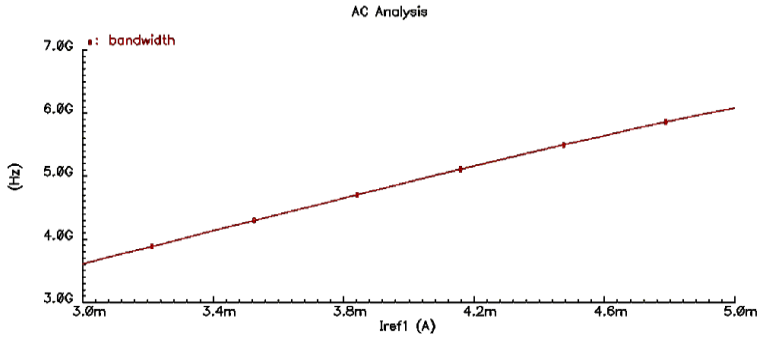

Fig. 2.48. Bandwidth behavior as function of *Iref1*.

2.3.4 SEF Hold Mode Performance: Hold Feedthrough

The hold-mode feedthrough phenomenon has been treated in sub-section 2.2.4. Thus, I don't report here the entire discussion. This section reports the possible solution that alleviates hold-mode feedthrough phenomenon for the SEF circuit.

Firstly, it is important to consider the SEF circuit in the hold mode (see Fig. 2.49).

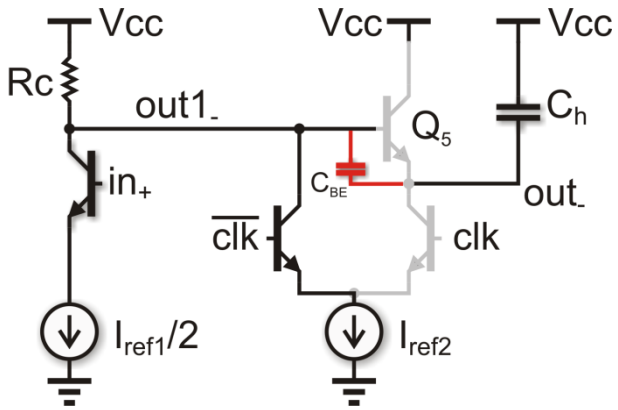

Fig. 2.49. SEF output circuit in hold mode.

When the circuit is in the hold mode, the sampling switch (transistor Q_5) presents finite impedance in its off state and so the parasitic capacitance C_{BE} causes feedthrough of the input voltage into the hold capacitor.

For sake of clarity, it can be considered the simplified equivalent circuit in Fig. 2.50.

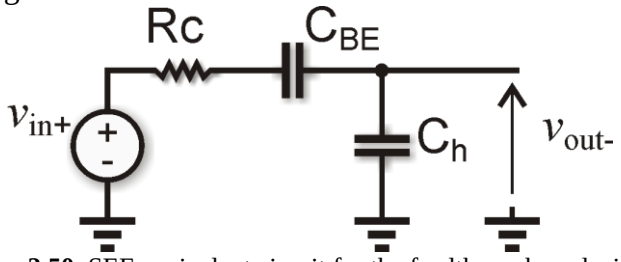

Fig. 2.50. SEF equivalent circuit for the feedthrough analysis.

Now, it can be easily calculated the transfer characteristic as low pass filter response

$$\left.\frac{v_{out-}}{v_{in+}}\right|_{hold} = \frac{C_{BE}}{C_{BE}+C_h} \cdot \frac{1}{1+s\,\mathrm{Rc}\cdot\dfrac{C_{BE}\cdot C_h}{C_{BE}+C_h}} \tag{2.75}$$

In order to minimize the feedthrough, C_h should be increased, but the value of C_h previously chosen to have the desired performance in terms of noise is already quite high. A further increase of C_h could worsening the bandwidth.

Considering the SEF circuit by using the design parameters as defined previously, it can be obtained a feedthrough effect as reported in Fig. 2.51. It can be noted a feedthrough at dc equal to 24 *dB*.

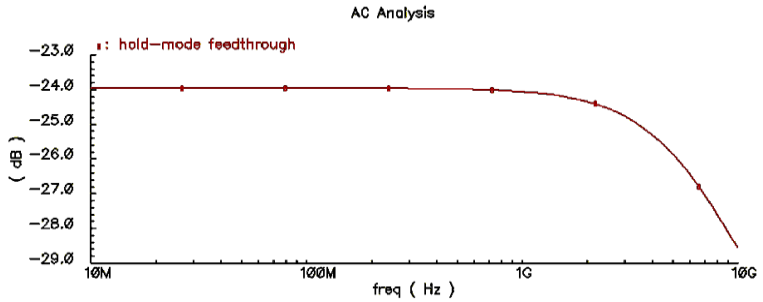

Fig. 2.51. Hold-mode feedthrough.

A more effective way to reduce the hold-mode feedthrough is accomplished by adding the cross-coupled feedforward capacitors C_C to the THA circuit [10], as shown in Fig. 2.52.

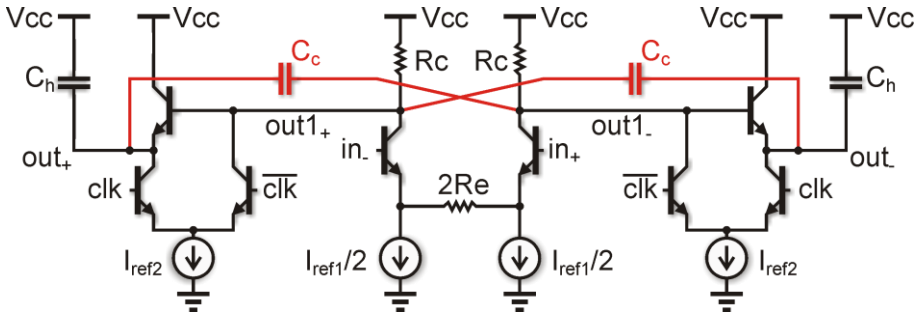

Fig. 2.52. SEF with hold-mode feedthrough compensation.

The compensation technique exploits the circuit property of symmetry for which $v_{out1+} \approx v_{out1-}$. The charge dump of the capacitor C_C is of opposite sign to the charge dump of the base-emitter capacitance of the switch transistor. The simplified equivalent circuit is depicted in Fig. 2.53.

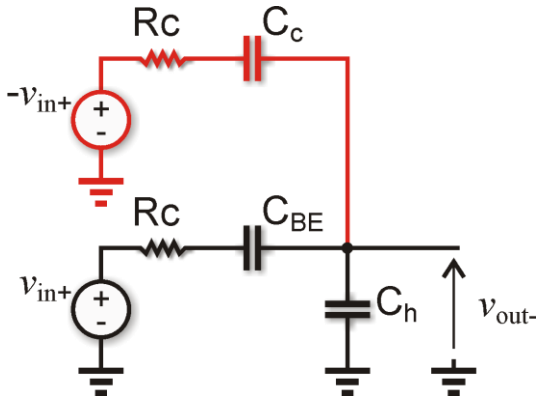

Fig. 2.53. SEF equivalent circuit with feedthrough compensation.

Now, in the hypothesis that $C_{BE} \approx C_C$, the circuit response is given by

$$\left.\frac{v_{out-}}{v_{in+}}\right|_{hold} \approx \frac{C_{BE}}{C_{BE}+C_h}\left(\frac{C_{BE}-C_c}{C_{BE}}\right)\frac{1}{1+s\,\mathrm{Rc}\cdot\dfrac{C_{BE}C_h}{C_{BE}+C_h}} \tag{2.76}$$

It can be noted that a complete cancellation of the feedthrough is not possible as C_{BE} varies with the operating point of the transistor. However, it can be strongly reduced by assuming C_{BE} to be constant and choosing C_C to be equal to C_{BE}.

The compensation capacitor C_C is realized a series-parallel connection of four diodes [10], as shown in Fig. 2.54.

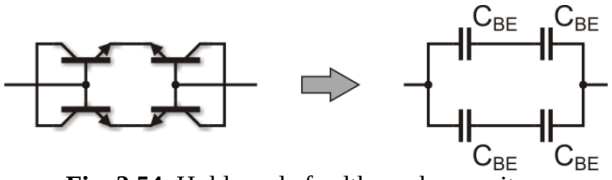

Fig. 2.54. Hold-mode feedthrough capacitor.

The condition $C_{BE} \approx C_C$ can be achieved unless the dependence of the BJT junction capacitance on the biasing voltage. The simulation result of Fig. 2.55 highlights the usefulness of the compensated circuit in reducing the hold-mode feedthrough.

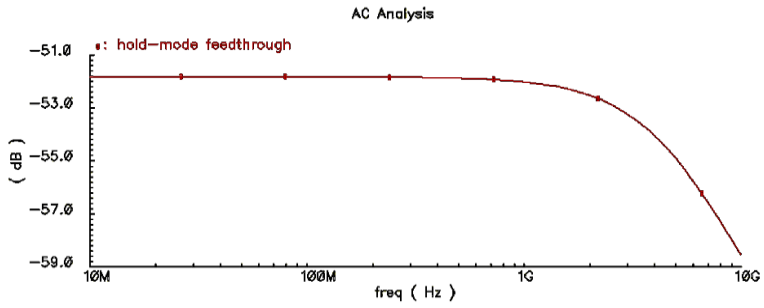

Fig. 2.55. Hold-mode feedthrough with compensation technique.

It is evident the better performance than the previous result of Fig. 2.51. Now, the hold-mode feedthrough at dc is -51.8 *dB*. It is more than double the value obtained with the circuit without compensation.

2.3.5 SEF Track-to-Hold Performance: Pedestal Error

The phenomenon called “pedestal error voltage” or simply “pedestal”, previously discussed in sub-section 2.2.5, affects a THA during the transition track-to-hold. It is due to a charge injection on the hold capacitor, during the transition track-to-hold, so determining a perturbation of the voltage held on C_h, after the hold command. In the SEF circuit the transition track-to-hold causes the distortion of the

holding voltage through the non-linear base-collector capacitance C_{BC} [17], as shown in Fig. 2.56.

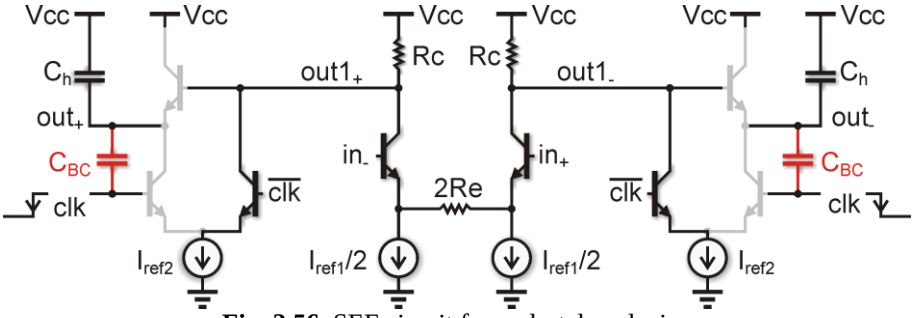

Fig. 2.56. SEF circuit for pedestal analysis.

The simulation set-up for observing the pedestal error is the same used for the diode-bridge (sub-section 2.2.5 - Fig. 2.18), obviously with the correct initial conditions (appropriate input dc voltage levels).

The numerical simulation results for a SEF in single-ended and differential configuration for an 8-bits ADC are depicted in Fig. 2.57 and Fig. 2.58, respectively.

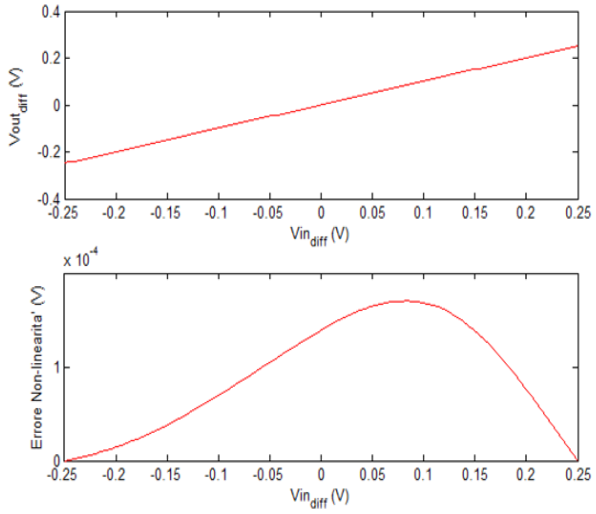

Fig. 2.57. INL and gain error for single-ended SEF.

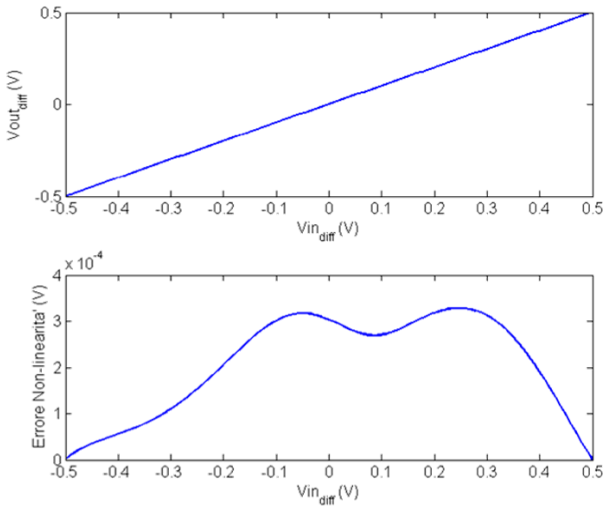

Fig. 2.58. INL and gain error for differential SEF.

The performances are summarized in Table 2.VII.

Table 2.VII

SEF-THA	Single-ended	Differential
INL_{max}	107 μV (0.09 LSB)	328 μV (0.08 LSB)
Gain	1	1

It is worth to highlight that both in single-ended and differential configuration the gain error is practically cancelled and the maximum non-linearity is good.

2.3.6 SEF Track-to-Hold Performance: Aperture Error

The opening discussion of sub-section 2.2.6 can be here wholly recovered. However, it must be analyzed the aperture phenomenon as occurs in the SEF circuit. To better understand this phenomenon, it can be considered the SEF response to a variable input signal ($v_{in}(t)=A\cos(2\pi f_{in}t)$). During the track phase the switched emitter-follower is on and will make the output ($v_{out}(t)$) follows the input. During the transition track-to-hold the switched emitter-follower switches, leading the current flowing through it to zero in a finite time. In the presence of a variable input, the SEF aperture persists from the

start of the track-to-hold transition until the SEF emitter current equals the sum of instantaneous current flowing into the hold capacitor ($C_h dv_{in}(t)/dt$) and I_2, as shown in Fig. 2.59.

Consequently, the aperture depends on the rate-of-change of the input signal. This implies that the input signal is sampled with different aperture, based on its instantaneous derivative, thus resulting in a non-uniform sampling and introducing distortion of the output signal.

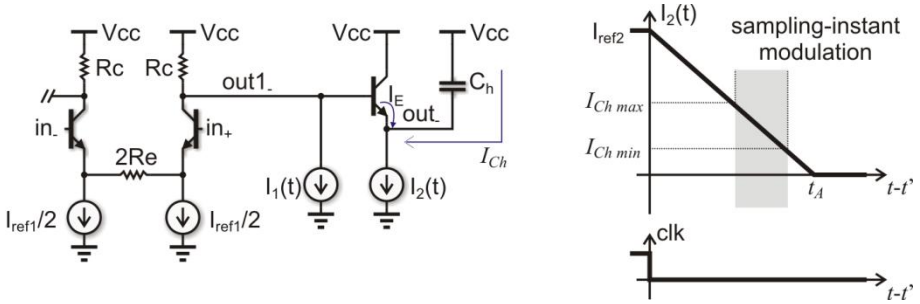

Fig. 2.59. SEF: simplified equivalent circuit for aperture analysis.

The perturbation introduced by the aperture can be analyzed, considering that the current decreases linearly as shown in Fig. 2.59.

The sampling condition is

$$I_E = I_2(t) - I_{Ch}(t) = 0 \quad \Leftrightarrow \quad I_2(t) = I_{Ch}(t) \tag{2.77}$$

The switch occurs when the current I_2 equals the current I_{Ch}.

The current I_{Ch} can be obtained through the superposition of the effect of v_{in+} and $I_1(t)$ (see Fig. 2.60, Fig. 2.61),and it can be written

$$I_{Ch} = I'_{Ch} + I''_{Ch} \tag{2.78}$$

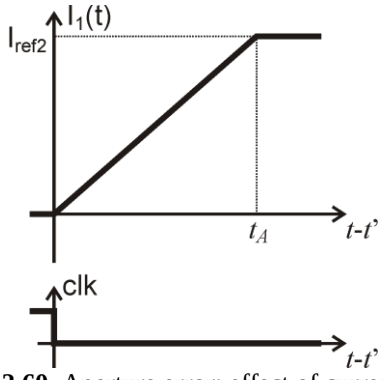

Fig. 2.60. Aperture error: effect of current I_1.

and I'_{Ch}, I''_{Ch} can be written as

$$\begin{cases} I'_{Ch} = -C_h \dfrac{dv_{in+}}{dt} = AC_h 2\pi f_{in} \sin\left(2\pi f_{in} t\right) \\ I''_{Ch} = C_h \mathrm{Rc} \dfrac{dI_1}{dt} = C_h \mathrm{Rc} \dfrac{I_{ref\,2}}{t_A} \end{cases} \tag{2.79}$$

Now, it can be rewritten the sampling condition expressed by (2.77) as follows

$$I_2(t_s) = I_{ref\,2}(1 - \frac{t_s - t'}{t_A}) = I_{Ch}(t_s) = I'_{Ch}(t_s) + I''_{Ch} \tag{2.80}$$

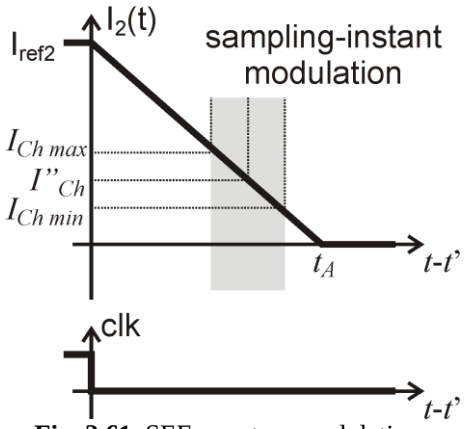

Fig. 2.61. SEF: aperture modulation.

As in the case of the diode-bridge, for sake of simplicity it can be assumed

$$I_{Ch}(t_s) \cong I_{Ch}(t' + t_A) \tag{2.81}$$

and the sampling instant can be derived from eq. (2.80) as follows

$$t_s = t' + t_A - C_h \mathrm{Rc} - \gamma \sin\left(2\pi f_{in}\,(t' + t_A)\right) \tag{2.82}$$

where $\gamma = t_A \dfrac{AC_h 2\pi f_{in}}{I_{ref2}}$.

A particular condition (see Fig. 2.61) is

$$I_{Ch\,min} > I_{ref2} \quad \Rightarrow \quad t_s = t' \tag{2.83}$$

in this case there is no modulation and the sampling is instantaneous (i.e. at the instant t', the current I_E is already smaller than zero).

Assuming that $I_{Ch\,min} \simeq I''_{Ch}$, eq. (2.83) can be rewritten as

$$C_h \mathrm{Rc} \frac{I_{ref\,2}}{t_A} > I_{ref\,2} \quad \Leftrightarrow \quad t_A < C_h \mathrm{Rc} \tag{2.84}$$

Eq. (2.84) establishes an upper limit for the aperture time t_A avoiding the aperture modulation.

If the aperture time is larger than $C_h \mathrm{R_C}$, a modulation effect arises due to the aperture error and, as in the case of the diode-bridge, the aperture modulation is analogous to phase modulation and can be analyzed identically. Eq. (2.34) can be rewritten for the switched emitter-follower circuit as

$$\beta = 2\pi f_{in} \gamma = \frac{AC_h \left(2\pi f_{in}\right)^2}{I_{ref2}} t_A \tag{2.85}$$

and following the same mathematical procedure used for the diode-bridge also for the differential SEF, the harmonic distortion is

$$\begin{cases} HD_2 = 0 \\ HD_3 \cong \mathrm{J}_2(\beta) \approx \beta^2 / 8 \end{cases} \tag{2.86}$$

This result agrees formally with that of the diode bridge (2.35) by only replacing the bridge current I_1 with I_{ref2}. The designed SEF circuit shows an aperture time t_A=40 *ps* while the product $C_h \mathrm{R_C}$=71 *ps*, whereby $t_A < C_h \mathrm{R_C}$. The effect of the aperture error should be strongly reduced.

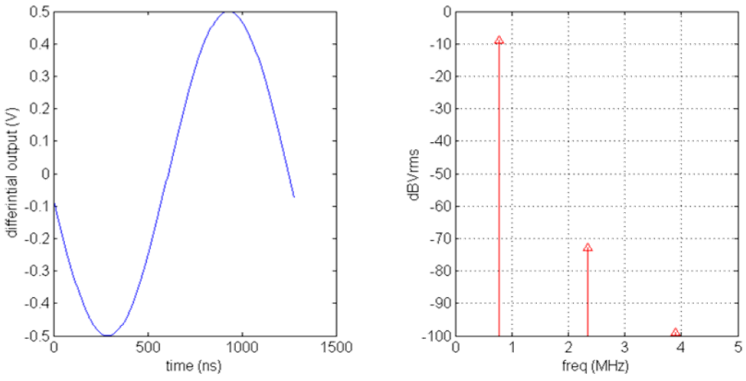

Fig. 2.62. Down-sampling test of differential SEF circuit.

At the aim to evaluate the effect of bandwidth limitation and distortion in track mode, pedestal and aperture error, hold-mode feedthrough and droop-rate on the THA performance, a transient simulation without noise (excluding other phenomena like jitter) has

been performed. The suitable simulation set-up is the same described in sub-section 2.2.6 (see Fig. 2.22). The simulation results are reported in Fig. 2.62. The resulting total harmonic distortion is 64 *dB* corresponding to an *ENOB*=10.34. This *THD* value is very closely to that obtained in the track mode (see Fig. 2.44), confirming that the aperture error is not very relevant.

2.3.7 SEF Track-to-Hold Performance: Clock Jitter

The opening discussion of the sub-section 2.2.7 can be here reported, because the clock driver used for the switched emitter-follower is the same used for the diode-bridge.

The transient response of the clock driver loaded with the SEF circuit is depicted in Fig. 2.63.

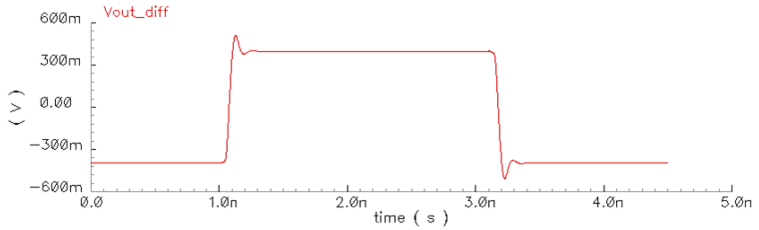

Fig. 2.63. Transient response of the clock driver to a differential input.

The resulting fall-time is equal to 40 *ps*, the output noise σ_{Vclk}=1.176 mV_{rms}, while the signal slope is dv_{clk}/dt=18 *V/ns*, determining the following rms jitter

$$\sigma_t \approx \frac{\sigma_{v_{clk}}}{dv_{clk}/dt} = 66 \ fs \tag{2.87}$$

Recalling eq. (2.39), it is immediately verified that the SEF performance in terms of clock jitter are comparable with that of the DB.

2.3.8 SEF Performance: Simulation Results

This section reports the simulation results related to the switched emitter-follower behavior taking into account the error sources whose

effects have already been evaluated in sub-section 2.3.6, including also the sampling time jitter and the noise generated by the THA.

For this purpose, a transient simulation with generated noise has been performed, and its set-up is shown in Fig. 2.64.

The samples provided by the sample-and-hold are the inputs of the *VerilogA* module that stores the samples in a data file for the subsequent processing in the Matlab tool. It is worth recalling that the test in down-sampling entails, according to the design constraints, an analog input signal at the frequency f_{in}=1 *GHz* with a sample rate f_s=200 *MHz* corresponding to a sampling (clock) period T_s=5 *ns*. In this case, it has been fixed a clock period equal to T_{clk}=5 *ns*+5 *ns*/N_{pt} where N_{pt}=256 is the number of simulation points. This implies that T_{clk}=5.019 *ns* corresponding to a sample rate f_s=199.22 *MHz*. The resulting frequency of the digital output is equal to f_{out}=3.89 *MHz*=5f_s/256.

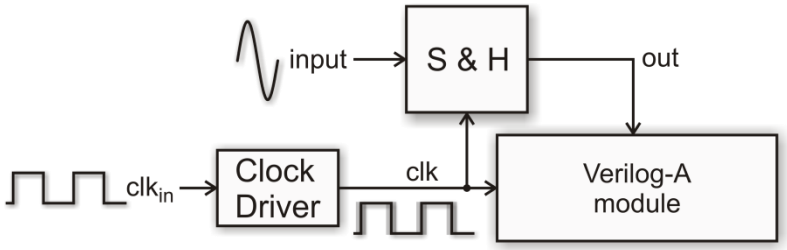

Fig. 2.64. Simulation set-up: switched emitter-follower overall performance.

The simulation results are reported in Fig. 2.65 and summarized in Table 2.VIII . It can be noted that the value of the *SNR* (57.3 *dB*) is very closely to that obtained in track mode (57.4 *dB*), confirming that the clock jitter does not have a significant impact on the THA noise performance. Furthermore, the value of the harmonic distortion is similar to that evaluated without clock driver and noise generator, confirming that these phenomena don't have a relevant impact on the THA overall performance.

It is worth highlighting that all the numerical simulation results presented previously have been obtained considering ideal current sources as biasing elements of THA circuit.

At the aim to evaluate the actual performance of the switched emitter-follower the ideal current sources have been replaced by suitable current mirrors made with active devices. A great attention

has been devoted to minimize as much as possible the impact of the current mirrors on the THA performances.

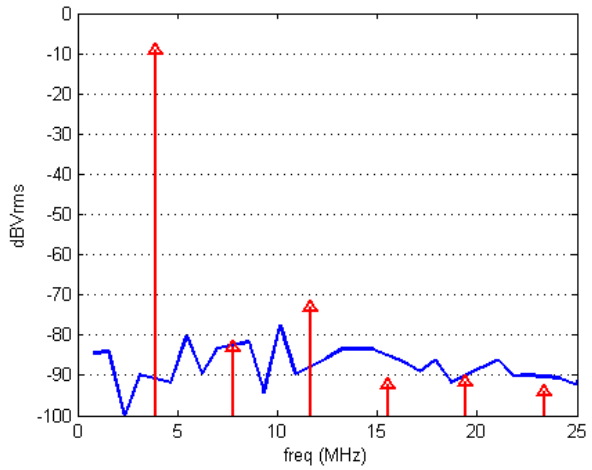

Fig. 2.65. SEF dynamic response in the frequency domain.

Table 2.VIII

Switched Emitter-Follower	
THD	63.4 *dB* (10.23 bits)
SNR	57.3 *dB* (9.18 bits)
SNDR	56.1 *dB* (9.03 bits)

In the following the results will include the effect of the current mirrors.

The characteristic time intervals (settling and hold time as defined in sub-section 2.2.8) of the THA operation are depicted in Fig. 2.66.

These characteristic time intervals fix, in the worst case, an upper limit to the sampling frequency as follows

$$f_{s\max} = \frac{1}{2t_{w.c.}} \tag{2.88}$$

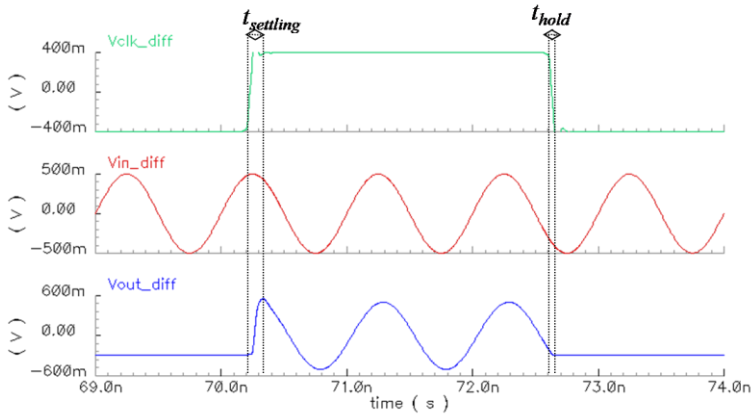

Fig. 2.66. Settling track and hold time of switched emitter-follower.

In this case we have

$$\begin{cases} t_{settling} = 245\ ps \\ t_{hold} = 50\ ps \end{cases} \quad \Leftrightarrow \quad f_{s\max} = 1/2t_{w.c.} = 1/2t_{settling} = 2\ GHz \qquad (2.89)$$

The switched emitter-follower frequency response, depicted in Fig. 2.67, highlights a bandwidth equal to 6.1 *GHz*.

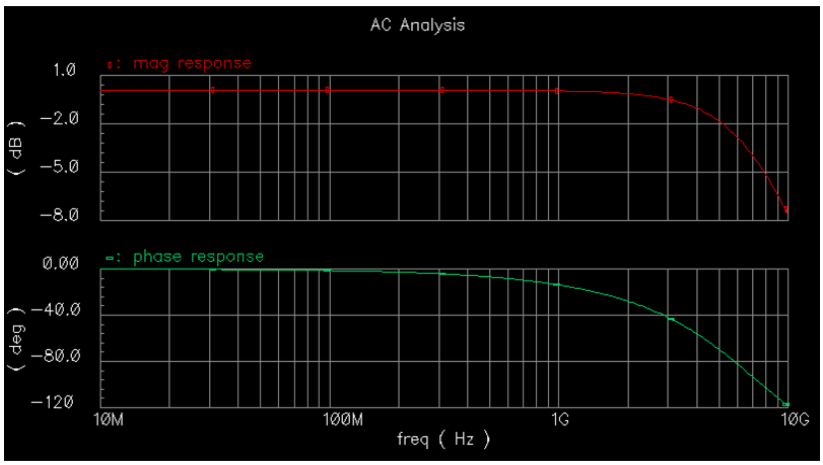

Fig. 2.67. Frequency response of the switched emitter-follower.

Now, the final results of the switched emitter-follower in the differential configuration can be reported.

The behavior of the effective number of bits as function of the input frequency is shown in Fig. 2.68.

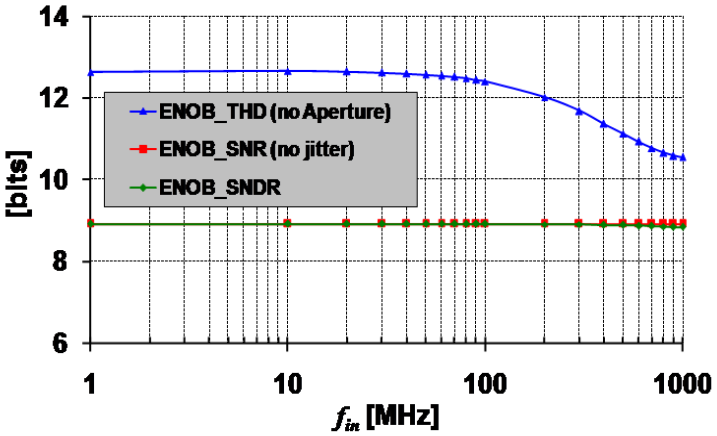

Fig. 2.68. ENOB versus f_{in} (SEF differential mode).

The final performances are summarized in Table 2.IX. It can be noted that the differential circuit configuration shows better performances with respect to the single-ended solution.

Table 2.IX

SEF	Differential	Single-Ended
Supply voltage	3.6 *V*	3.6 *V*
THD(@1 GHz)	65.1 *dB* (10.52 *bits*)	40.4 *dB* (6.42 *bits*)
THD(@500 MHz)	68.4 *dB* (11.07 *bits*)	39.9 *dB* (6.34 *bits*)
SNR	56.1 *dB* (9.03 *bits*)	50.0 *dB* (8.04 *bits*)
SNDR(@1 GHz)	55.6 *dB* (8.94 *bits*)	40.0 *dB* (6.35 *bits*)
SNDR(@500 MHz)	55.6 *dB* (8.94 *bits*)	39.5 *dB* (6.27 *bits*)
hmf(@1 GHz)	-53.9 *dB*	-53.9 *dB*
hmf(@500 MHz)	-53.8 *dB*	-53.8 *dB*
Droop-rate	8.4 *nV/ns*	3.32 *nV/ns*
Bandwidth	6.1 *GHz*	6.1 *GHz*
Power Dissipation	45 *mW*	47 *mW*

At the aim of comparison between the diode-bridge and the switched emitter-follower, the data in Table 2.VI referred to the

differential diode-bridge are recalled and reported in Table 2.X. In fact, in both cases the differential configuration exhibits the better performance than the single-ended solution.

Table 2.X

Differential	**SEF**	**Diode-Bridge**
Supply voltage	3.6 *V*	3.6 *V*
THD(@1 GHz)	65.1 *dB* (10.52 *bits*)	53.7 *dB* (8.63 *bits*)
THD(@500 MHz)	68.4 *dB* (11.07 *bits*)	66.6 *dB* (10.77 *bits*)
SNR	56.1 *dB* (9.03 *bits*)	52.3 *dB* (8.40 *bits*)
SNDR(@1 GHz)	55.6 *dB* (8.94 *bits*)	50.0 *dB* (8.01 *bits*)
SNDR(@500 MHz)	55.6 *dB* (8.94 *bits*)	52.7 *dB* (8.46 *bits*)
hmf(@1 GHz)	-53.9 *dB*	-51.0 *dB*
hmf(@500 MHz)	-53.8 *dB*	-57.7 *dB*
Droop-rate	8.4 *nV/ns*	70 *mV/ns*
Bandwidth	6.1 *GHz*	3.87 *GHz*
Settling time	245 *ps*	430 *ps*
$f_{s\,max}$	2 *GHz*	1.2 *GHz*
Power Dissipation	45 *mW*	47 *mW*

It is clearly visible that the THA SEF circuit provides better performance than the diode-bridge not only in terms of *SNDR*, but also in terms of bandwidth and maximum sampling frequency.

Thus, the switched emitter-follower circuit will be used in the final design of the complete ADC.

2.4 Comparator

Every analog-to-digital converter contains at least one comparator. There are as many comparator circuits as there are analog-to-digital converter designers. Many aspects need consideration when designing a comparator. These aspects may vary for every different application, for specific class of signals, a technology, etc. No universal “one design fits all converters” comparator exists [18].

The performance of a flash ADC strongly depends on that of its constituent comparators. For an N-bits flash ADC, 2^N-1 comparators

are needed, requiring great attention to the constraints imposed on the overall system by the large number of comparators [1]. They are true mixed signal devices, and play a very important part in the design of high speed data converters. Thus, the design and the implementation of the comparator and its subsequent performance is crucial to the overall successful implementation of the data converter system.

The ideal comparator transfer function is as shown below

$$V_{out} = \begin{cases} high \quad (\text{logic 1}) \quad if \;\; V_{in} > V_{ref} \\ low \quad (\text{logic 0}) \quad if \;\; V_{in} < V_{ref} \end{cases} \tag{2.90}$$

Comparison is in effect a binary phenomenon that produces a logic output of one or zero depending on the polarity of a given input.

Comparators can be classified into two types depending on architecture. Static comparators are those which perform threshold detection based on the input and reference without clocking mechanism. Dynamic comparators (also called latched comparators) on the other hand, make use of the clocking mechanism to perform the switching action. The typical comparator is analog-to-digital conversion device with two analog inputs and a single digital output. The dynamic comparator in essence is a clocked difference detection circuit with pre-amplification and output latching [19]. Often latched comparators employ strong positive feedback for a regeneration phase when the clock is high, and have a reset phase when the clock is low.

2.4.1 Comparator: Typical Bipolar Design

Typical comparator architecture consists of a pre-amplifier followed by a latch and has two modes of operation, namely, tracking and latching. A traditional bipolar implementation of this architecture is depicted in Fig. 2.69.

The pre-amplifier consists of the differential pair Q_1-Q_2 and the resistors R_C, while the latch comprises Q_3-Q_4 and shares the same resistors. Two clock signal clk (track) and its negated (latch) control the differential pair and the latch through Q_5 and Q_6, respectively.

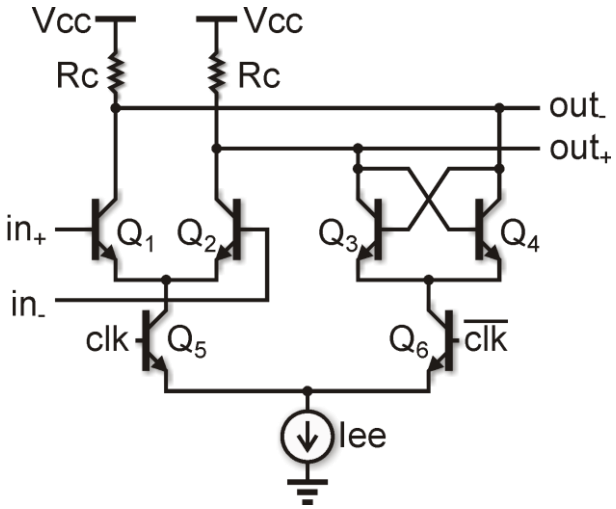

Fig. 2.69. Typical bipolar comparator implementation.

When clk is high, Q_5 is on and the differential pair tracks the input while Q_6 is off and the latch is disabled. On the other hand, when the clk is low, Q_5 turns off, disabling the input pair, while Q_6 turns on and the latch establishes a positive feedback loop and amplifies the difference between V_{out-} and V_{out+}.

An important figure of merit of the comparator performance is the resolution or rather the minimum input difference that can be resolved by the comparator itself. This minimum input is 1 LSB. The resolution is limited by the input-referred offset and noise of both the pre-amplifier and latch. The following sub-sections will be devoted to analyze these phenomena and how they impact on the overall comparator performance. Furthermore, some other considerations will be provided referring to the characteristic time intervals, and input currents and capacitances of the comparator.

2.4.2 Comparator: Offset Analysis

The comparator offset can be divided into two contributions, the pre-amplifier and latch offset. The input offset voltage arises from the mismatch between nominally identical devices Q_1-Q_2, Q_3-Q_4, and the two resistors R_C. In the case of the latch another source of offset error is the mismatch between the circuit capacitances due to phenomena of

charge redistribution. Since mismatch contributions of Q_3-Q_4, and the two resistors R_C appear at the output, they are divided by the voltage gain of the differential pair when referred to the input. Thus, the overall offset can be obtained as follows

$$V_{os} = V_{os\ pre} + \frac{1}{G_{pre}} \cdot V_{os\ latch} \tag{2.91}$$

where $V_{os\ pre}$ is the pre-amplifier offset, while $V_{os\ latch}$ is the lacth offset. This latter is the latch input voltage that leads the latch to the instable point, after the high to low clock transition.

Moreover, G_{pre} is the pre-amplifier voltage gain and can be written as

$$G_{pre} = g_{m12} R_C \tag{2.92}$$

where g_{m12} is the transconductance of Q_1 and Q_2.

Generally, G_{pre} is much greater than one, so eq. (2.91) can be rewritten as

$$V_{os} \simeq V_{os\ pre} \tag{2.93}$$

As discussed above the offset is due to the devices and resistors mismatch. In particular, it arises from the area mismatch of the active devices and resistors value mismatch. Considering the analysis reported in [5], it can be obtained

$$V_{os\ pre} \simeq V_T \frac{\Delta A_{12}}{A_{12}} + V_T \frac{\Delta Rc}{Rc} \tag{2.94}$$

that is an approximate expression for the input offset voltage, which is the linear superposition of the effects of the different components.

Eq. (2.94) relates the offset voltage to mismatches in the resistors (ΔR_C) and in the structural parameters (ΔA_{12}) of the transistors. Mismatch factors $\Delta A_{12}/A_{12}$ and $\Delta R_C/R_C$ are actually random parameters that take on a different value for each circuit fabricated, and the distribution of the observed values is described by a probability distribution.

A parameter of more interest to the circuit designer than the offset of one sample is the standard deviation of the total offset voltage.

Since the offset is the sum of two uncorrelated random parameters, the standard deviation of the sum is equal to the square root of the sum of the squares of the standard deviation of the two mismatch contributions, or

$$\sigma_{Vos} \simeq V_T \sqrt{\left(\frac{\sigma_{A_{12}}}{A_{12}}\right)^2 + \left(\frac{\sigma_{\mathrm{Rc}}}{\mathrm{Rc}}\right)^2} \tag{2.95}$$

Since comparator offset is added to the differential input it modifies the threshold transition. Therefore, in a flash architecture the offset of the j-th comparator alters the j-th threshold of the ADC (see Fig. 2.70).

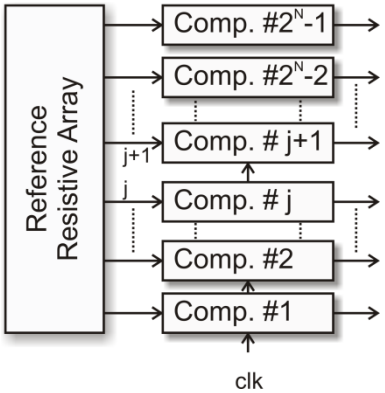

Fig. 2.70. Comparator offset.

A constant displacement of each threshold causes an offset error of the ADC. Neglecting the offset error, it is interesting to analyze the offset variation between the comparators within die.

Neglecting the offset and gain offset due to the comparators, in the worst case it is possible to write

$$INL_j \simeq V_{os\ j} \qquad DNL_j \simeq V_{os\ j+1} - V_{os\ j} \tag{2.96}$$

As $V_{os\ j}$ and $V_{os\ k}$ tend to be quite independent, the offset of the comparator appears to be a white noise component at the output of the ADC (worsening the *SNR*) rather than a distortion component (worsening the *THD*).

In order to ensure no missing codes or monotonicity the following constraint must be verified

$$|DNL| \le V_{LSB} \quad \Leftrightarrow \quad |V_{os}| \le V_{LSB}/2 \tag{2.97}$$

that is for a given yield the maximum value of the offset must be lower than ½ LSB divided by the number of sigma required to obtain that yield. Generally, from a statistical point of view it is imposed that (2.97) is verified ensuring a 99.9% yield. Thus, considering V_{os}

distribution as a Gaussian distribution, the following constraint must be verified

$$3.30\sigma_{Vos} \le \frac{V_{LSB}}{2} \quad \Leftrightarrow \quad \sigma_{Vos} \le \frac{V_{LSB}}{6.60} \tag{2.98}$$

Now, some design trade-offs can be taking into account. Eq. (2.95) shows that an offset reduction can be obtained by increasing the area of Q_1-Q_2 or the width of the resistors R_C. Increasing the area of the active devices increases the comparator input capacitances (increases the load effect of the comparator) and the capacitances on the output nodes. These latter capacitances can also increase increasing the width of the resistors R_C. The effect is a worsening of the characteristic times of the comparator.

Substituting in eq. (2.92) the BJT expression of g_{m12} it can be written

$$G_{pre} = \frac{1}{2}\frac{I_{ee}\mathrm{Rc}}{V_T} = \frac{1}{2}\frac{V_{sw}}{V_T} \tag{2.99}$$

If an high voltage gain is desired, the output voltage swing V_{sw} must be much greater than the thermal voltage V_T. This can be obtained by increasing the bias current I_{ee} worsening the input capacitance, or increasing R_C and, as already stated, worsening the comparator characteristic times.

2.4.3 Comparator: Noise Analysis

The comparator input-referred noise (when the clock is high) is added to the other noise sources of the ADC.

The comparator input-referred noise consists primarily of the thermal and shot noise of the transistors of the differential pair and the thermal noise of the resistors R_C. By using the noise analysis reported in [5], it can be obtained the noise spectral density of the comparator as

$$\frac{v_n^2}{\Delta f} \simeq 8KT\left(r_{b12} + \frac{1}{2g_{m12}} + \frac{\mathrm{Rc}}{G_{pre}^2}\right) \tag{2.100}$$

where r_{b12} is the base resistance of Q_1 and Q_2 (a physical resistor in series with the input), while $1/2g_{m12}$ is the effect of collector current shot noise and R_C/G^2_{pre} is the effect of thermal noise due to the collector resistors, both referred back to the input. In most cases the

noise component R_C/G^2_{pre} can be neglected. Furthermore, all the noise components are assumed to be uncorrelated.

The total input-referred noise can be written as

$$V_n^2 = \frac{v_n^2}{\Delta f} N_{BW} \tag{2.101}$$

where N_{BW} is the equivalent noise bandwidth and, in the case the pre-amplifier can be considered a single pole circuit, it is

$$N_{BW} = \frac{\pi}{2} f_{3dB} \tag{2.102}$$

where f_{3dB} is the -3 *dB* bandwidth and eq. (2.101) can be rewritten as

$$V_n^2 = \frac{4KT}{\pi}\left(r_{b12} + \frac{1}{2g_{m12}}\right) f_{3dB} \tag{2.103}$$

The noise can be reduced by reducing $1/2g_{m12}$ that is increasing I_{ee}. As a consequence, f_{3dB} increases and at the same time input capacitance increases. However, increasing the bias current I_{ee} a noise reduction is expected.

2.4.4 Comparator: Times Analysis

The settling and recovery time of the comparator are defined in Fig. 2.71.

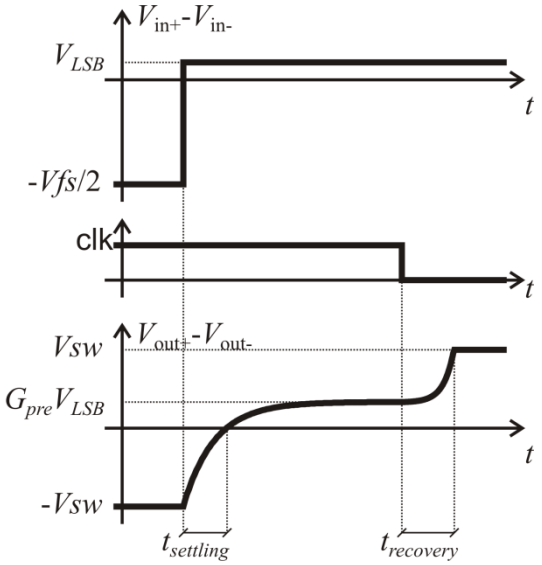

Fig. 2.71. Comparator characteristic times.

The time intervals in Fig. 2.71 are referred to the worst case transition of the comparator input.

The settling time depends on the dynamic behavior of the pre-amplifier. Assuming that the pre-amplifier is single pole system and considering the comparator differential output $V_{out}= V_{out+}- V_{out-}$, it can be written

$$V_{out}(t) = \left(G_{pre}V_{LSB} + V_{sw}\right)\left(1 - e^{-t/\tau}\right) \tag{2.104}$$

then, if $t=t_{settling}$ and assuming $V_{out}(t_{settling})=V_{sw}$, eq. (2.104) becomes

$$V_{sw} = \left(G_{pre}V_{LSB} + V_{sw}\right) - \left(G_{pre}V_{LSB} + V_{sw}\right)e^{-t_{settling}/\tau} \tag{2.105}$$

after some calculations it can be obtained

$$t_{settling} = \tau \ln\left(1 + \frac{V_{sw}}{G_{pre}V_{LSB}}\right) \tag{2.106}$$

where the time constant $\tau=\mathrm{R_C}C_{out(clk=1)}$ and $C_{out(clk=1)}$ is the output capacitance when the clock is high. By substituting in eq. (2.106) and recalling (2.99), it follows

$$t_{settling} = \mathrm{Rc}\,C_{out(clk=1)} \ln\left(1 + \frac{V_T}{2V_{LSB}}\right) \tag{2.107}$$

On the other hand, the recovery time depends on the dynamic behavior of the latch. During the regeneration phase (clk=0), it is [1]

$$V_{out}(t) = V_{out}(0) \cdot e^{t/\tau_{latch}} \tag{2.108}$$

where the time τ_{latch} is close to the transit time of the latch transistors Q_3-Q_4. This expression of the output voltage presumes the system linearity, thus it is verified until the latch reaches V_{sw} or rather when one of the transistors Q_3-Q_4 goes off.

Eq. (2.108) describes the latch behavior as that of two back to back connected identical single-pole inverting amplifiers each with a small-signal gain G_{latch} and a characteristic time constant equal to $\mathrm{R_C}C_{out(clk=0)}$. Thus, it can be written

$$\tau_{latch} = \frac{\mathrm{Rc}\,C_{out(clk=0)}}{G_{latch}} = \frac{C_{out(clk=0)}}{g_{m34}} \tag{2.109}$$

where $g_{m34}=G_{latch}/R_C$ is the transconductance of the transistors Q_3 and Q_4. This expression highlights that τ_{latch} could be reduced by increasing I_{ee}.

Assuming $V_{out}(t_{recovery})=V_{sw}$, eq. (2.108) becomes

$$V_{sw} = G_{pre} V_{LSB} e^{t_{recovery}/\tau_{latch}} \tag{2.110}$$

and after rearranging the terms, it follows

$$t_{recovery} = \tau_{latch} \ln\left(\frac{V_{sw}}{G_{pre} V_{LSB}}\right) \tag{2.111}$$

then recalling eqs. (2.99), (2.109), it can be written

$$t_{recovery} = \frac{1}{g_{m34}} C_{out(clk=0)} \ln\left(\frac{V_T}{2V_{LSB}}\right) \tag{2.112}$$

Referring to eqs. (2.107), (2.112), some useful design trade-offs can be derived. Thus, considering the same V_{sw}, both R_C and $1/g_{m34}$ depend on $1/I_{ee}$. This latter means that both settling and recovery time have the same trade-offs, so they can be improved (i.e. reduced) by increasing the bias current I_{ee} and decreasing C_{out} (with the difference that $C_{out(clk=0)}$ includes also the diffusion capacitances of Q_3-Q_4 which increase when I_{ee} increases).

Moreover, it is worth noting that both the settling and recovery time increase as V_{LSB} becomes smaller than V_T, and although the time dependence on V_{LSB} is logarithmic, V_{LSB} depends exponentially on the number of bits.

2.4.5 Comparator: Input Currents and Capacitances

The behavior of the comparator input currents is depicted in Fig. 2.72.

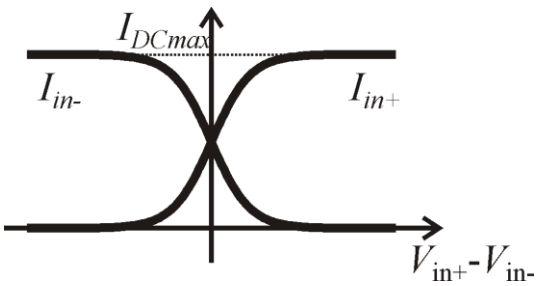

Fig. 2.72. Comparator input currents.

The maximum dc input current depends on the bias current I_{ee} as

$$I_{DCmax} = I_{ee} \Big/ \beta \tag{2.113}$$

and as we will see in the following, these currents have a relevant impact on the performance of the resistor ladder.

The comparator (see Fig. 2.69) exhibits a non-linear input capacitance as a function of the differential input [1]. Thus, we have three different cases:

- $V_{in+} - V_{in-} \ll -V_T$, this means that Q_1 is off and the input capacitance is

$$C_{IN\,diff+} \simeq C_{je1} \qquad C_{IN\,sended+} \simeq C_{jc1} \tag{2.114}$$

- $V_{in+} - V_{in-} \approx 0$, this implies that Q_1 turns on introducing a base-emitter diffusion capacitance C_{DE}, thus the input capacitance is

$$C_{IN\,diff} \simeq \frac{C_{de} + \left(1 + G_{pre}\right) C_{jc}}{2} \qquad C_{de} = g_{m12}\tau_F \tag{2.115}$$

  where τ_F is the base transit time.

- $V_{in+} - V_{in-} \gg V_T$, this implies Q_2 turns on and Q_1 operates as an emitter-follower, the input capacitance is

$$C_{IN\,diff+} \simeq 0 \qquad C_{IN\,sended+} \simeq C_{jc1} \tag{2.116}$$

It can be noted that when the differential input is about zero the capacitances on the nodes in_+ and in_- are symmetric, thus there is no difference between themselves. In the last case, when the differential input voltage is much greater than the thermal voltage, we consider only the capacitances on node in_+. In fact, the capacitances on node in_- are the same of node in_+ by symmetry provided that we change the sign of differential input or rather we consider the node in_- as node in_+ when differential input is much smaller than $-V_T$.

Next, it is worth noting that the input capacitances are larger when V_{in+} approaches V_{in-}, but in a flash ADC, for a given input voltage, most of the comparators operate with a differential input voltage away from zero. Thus, the comparator input capacitance arises primarily from the junction capacitances of the transistors.

Another important issue is that the comparator input capacitances impact on the speed of the resistor ladder, so worsening the maximum sampling frequency. From the converter point of view, the comparator input capacitance C_{IN} depends mainly on the devices area, hence there

is a trade-off between input capacitance and offset (see eq. (2.95)), while there is not a relevant dependence on the current I_{ee} (weak trade-off between input capacitance and characteristic times).

In conclusion, both comparator offset and input capacitance depend on the devices area. A better accuracy requires smaller offset, hence larger devices area, so increasing the input capacitance. As a consequence, the larger capacitance impacts on the overall performance by worsening the resistor ladder speed.

Furthermore, settling and recovery time, and input dc currents depend on the bias current I_{ee}. Smaller time requires higher bias current, thus increasing the input dc currents.

2.4.6 Comparator: Kickback noise

The kickback noise is a another phenomenon that affects the comparator behavior (see Fig. 2.73). This phenomenon can be detected at the input during the latch mode due to Q_1-Q_2 being suddenly shut-off. In fact, during the transition from latch to track, clock goes high and Q_5 turns on drawing current from Q_1 and Q_2 which are initially off, hence this current first flows through their base-emitter junction giving rise to a large current spike at the inputs.

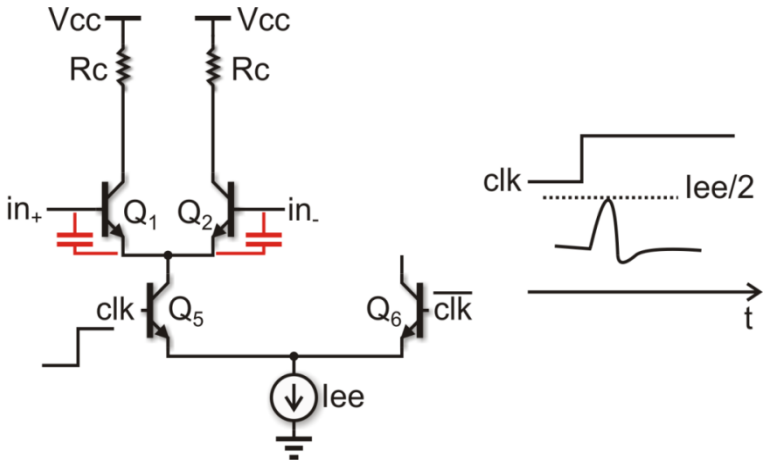

Fig. 2.73. Comparator kickback noise.

The magnitude of this spike is approximately half the I_{ee}, before Q_1 and Q_2 turn on and provide current gain [1], [20]. The kickback,

due to the back-injection of stored base-emitter charge into the base, can significantly distort the incoming signal and limit the performance of higher resolution converters. Moreover, this phenomenon can lengthen the switching time of the resistor ladder.

2.4.7 Comparator: Improved Architecture

In this sub-section, the comparator improved implementation employed in this work (see Fig. 2.74) will be presented, also highlighting the advantages with respect to the typical architecture discussed previously [1], [14]. In particular, the pre-amplifier can be preceded with another differential input stage to suppress the kickback noise and provide more gain, while the latch can use emitter-followers to enhance the regeneration speed.

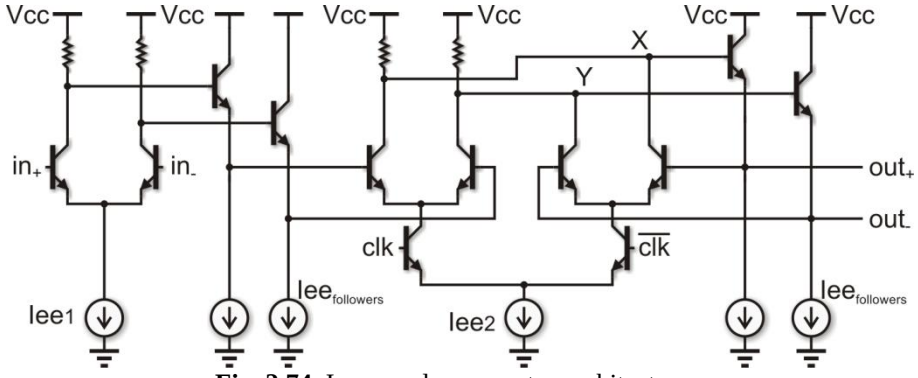

Fig. 2.74. Improved comparator architecture.

The differential input stage reduces the kickback noise to acceptable amount. Then, it increases the pre-amplifier gain (G_{pre}), thereby decreasing the latch offset, and improving the metastable behavior.

The emitter-followers between the first and second stage provide an ECL circuit allowing a larger voltage swing, hence increasing the voltage gain of the first stage. Another advantage is the capacitive decoupling of the second stage from the first stage, allowing the second stage bias current (I_{ee2}) to be increased without extending the propagation delay of the first stage.

Also the emitter-followers used in the latch section allow larger voltage swing, improving the voltage gain of the second stage. Moreover, they reduce the effect of the parasitic capacitances of the latch pair on the nodes X and Y, thus enhancing the regeneration speed.

Next, they provide a capacitive decoupling of the output capacitances from the nodes X, Y, thereby assuring that the comparator performance does not depend on the output load and additionally, during the latch phase, the capacitances of the latch transistors are not directly driven. As a consequence the bias current I_{ee2} can be increased without an increase of the capacitances driven by the latch pair transistors.

2.4.8 Comparator: Circuit Design and Simulation Results

The discussions presented in the previous sub-sections highlight the existence of a set of trade-offs between the different circuit parameters, their sizing is not easy. Taking into account these considerations, the design choices were made at the aim to achieve the desired comparator performance. The design parameters and their values are summarized in the following Table 2.XI.

Table 2.XI

Comparator	
Parameters	**Value**
V_{sw1}	300 mV
V_{sw2}	500 mV
I_{ee1}	200 μA
I_{ee2}	400 μA
$I_{ee\ followers}$	200 μA

The bias current of the first stage (I_{ee1}) is small at the aim to avoid the increase of the input currents. Thereby, V_{sw1} cannot be too high (i.e. R_C higher) otherwise worsening the settling time.

The emitter-followers between the first and second stage allow to increase the I_{ee2}, thus reducing the recovery time and enlarging the voltage swing V_{sw2}, improving the pre-amplifier gain. On the other

hand, the settling time is limited by the R_C value that cannot be so much reduced. Simulation results confirm this latter as shown in Fig. 2. 75. The settling and recovery time are

$$\begin{aligned} t_{settling} &= 156\ ps \\ t_{recovery} &= 62\ ps \end{aligned} \tag{2.117}$$

and, as expected, the settling time represents the worst case allowing a maximum sampling frequency equal to 3.2 *GHz*.

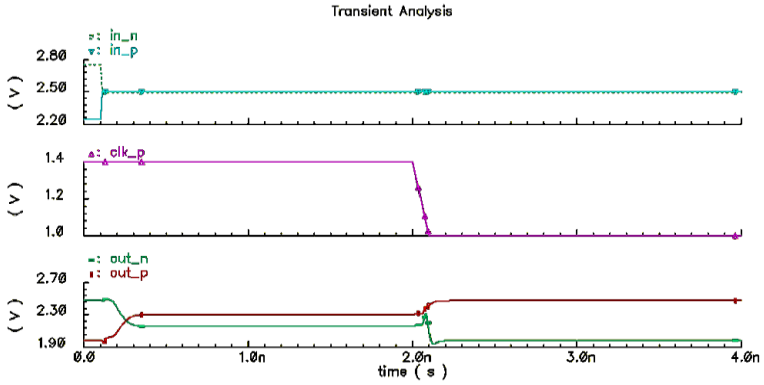

Fig. 2. 75. Comparator: settling and recovery time.

In Fig. 2.76 is depicted a dc Montecarlo simulation of the comparator offset. In particular this simulation takes into account only the pre-amplifier offset. Other simulation results have highlighted that the latch offset provides a negligible effect. The offset could be easily reduced by further increasing the size of the input devices, but worsening the input capacitances which heavily depend on the transistors area.

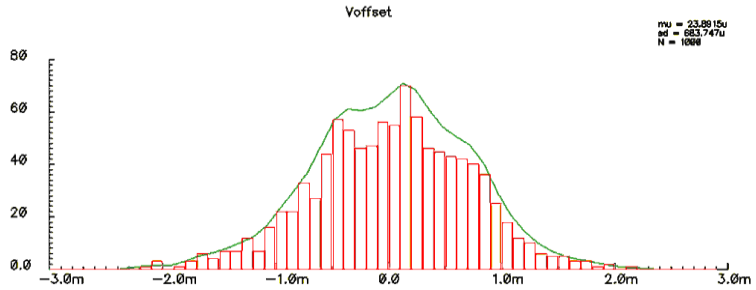

Fig. 2.76. Montecarlo simulation of comparator offset.

The resulting offset standard deviation is σ_{Vos}=684 μV corresponding to an *ENOB*=8.72 bits.

In Fig. 2.77 is depicted the input capacitance behavior as function of the differential input voltage. The resulting value of the input capacitance is

$$\begin{aligned} C_{INdiff+} &\cong 40\ fF \quad when\ \ V_{indiff} = 0 \\ C_{INdiff+} &\cong 16\ fF \quad when\ \ V_{indiff} = -0.5 \\ C_{INsended+} &\cong 10\ fF \quad when\ \ V_{indiff} = -0.5 \end{aligned} \tag{2.118}$$

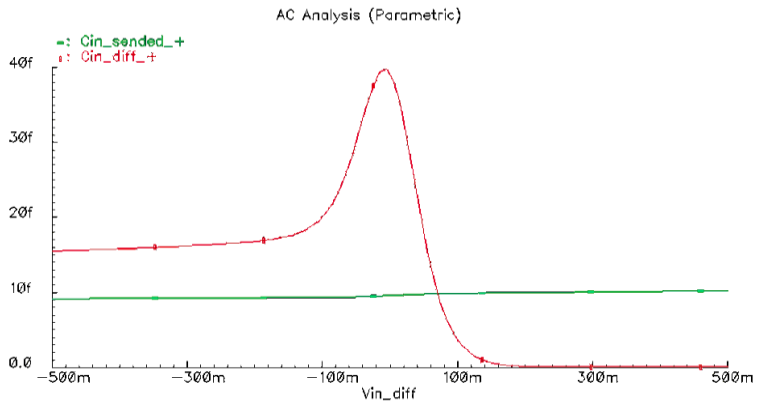

Fig. 2.77. Comparator input capacitance versus differential input voltage.

In a practical way, it can be considered

$$10\ fF < C_{IN} < 26\ fF \tag{2.119}$$

Moreover, the maximum dc input current is

$$I_{DC\max} = 896\ nA \tag{2.120}$$

that is a quite small value.

2.5 Resistor Ladder

The resistor ladder is one of the key elements in the development of high speed ADCs. In Flash ADC [1], [3], [21], [22], the resistor ladder is employed to generate the reference voltages which represent the ideal quantization thresholds of the converter.

Performances higher than Flash converters could be obtained by using Folding and Interpolating architectures [13], [14], [23]-[30]. The resistor ladder is still one of the basic elements of these converters,

where it generates the set of reference voltages required by the folders. Although in Folding and Interpolating ADCs the array length is reduced, the resistor ladder remains one of the main performance bottlenecks [30].

In a N-bits flash ADC, the resistor ladder provides N_R-1 thresholds, where $N_R=2^N$ is the number of resistors.

Basically it can be distinguished between two ladder topologies: single-ended and differential. In single-ended ladders, generally employed in CMOS converters [14], [21]-[24], the input voltage is compared with a set of N_R-1 voltages generated by a resistor divider.

In bipolar implementations this solution is generally not preferred since the *INL* of the converter becomes proportional to N_R^2, because of DC bowing effect [1]. Apparently the resistor divider voltages are static. However, due to capacitive feedthrough, the input signal switching excites a transient of the resistor divider voltages [1], [24].

This phenomenon (known as AC bowing effect) causes a settling behavior, so that the ADC speed becomes dependent on N_R^2. AC bowing effect can be alleviated by inserting decoupling capacitances or buffers, with an heavy price paid in terms of silicon area.

Differential ladders are generally the preferred choice in bipolar ADCs [13], [26]-[30]. In these circuits the differential input voltage propagates through two N_R resistors arrays, and the threshold voltages correspond to the zero crossing points of the differential voltages across the two arrays.

In addition to well known advantages of differential against single-ended topologies, like the rejection of common mode noise, the main advantage of differential resistor ladder is the reduced *INL* [31].

In fact, as it will be also seen in the following, in differential ladders the DC bowing effect, completely or partially, appears as a common mode and is therefore, in large part, cancelled by the differential nature of the circuit. The main drawback of differential ladders is the speed. In fact the maximum sampling frequency of the converter is limited by the settling time of the arrays, which is proportional to N_R^2.

Two techniques can be used to speed up bipolar ADCs: distributed sample & hold (SHA) [30], and high speed ladders [26], [27]. As an example the differential ladder proposed in [26], [27] can achieve up to a fourfold reduction of the array settling time, with respect to a

conventional differential array. However, as shown in the following, this improvement is paid with a worsening of the converter *INL*.

In this work a novel differential resistor ladder is proposed. The novel array achieves, in a first-order approximation, up to a sixteen-fold reduction of the settling time with respect to the conventional differential ladder. In addition, the novel array results also in a noticeable reduction of *INL* with respect to conventional differential ladder.

2.5.1 Resistor Ladder: Conventional Single-Ended Topology

A simplified schematic diagram of the conventional single-ended resistor ladder (for N_R=256, N=8) is depicted in Fig. 2.78.

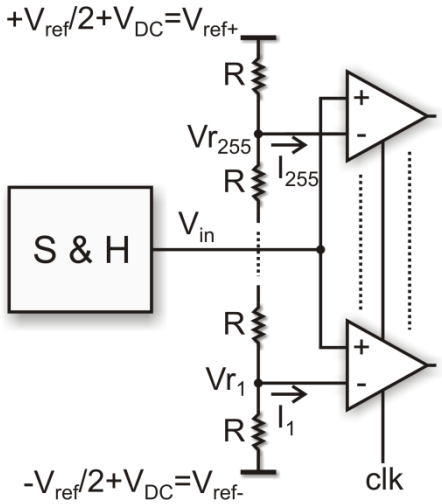

Fig. 2.78. Schematic diagram of conventional single-ended ladder.

The resistor ladder must provide the threshold voltages of the ADC, thus the single-ended configuration would appear an easy solution. Actually, some design drawbacks must be taken into account. The difference V_{ref+}-V_{ref-} must equal the required full-scale reference voltage (V_{ref}=V_{FS}), and the center tap voltage of the array $(V_{ref+}+V_{ref-})/2$ must equal the common-mode output level of the SHA

circuit. At the aim to achieve these design goals, a complex reference-voltage generator must be employed [32].

The simplified schematic circuit of the voltage-reference generator is shown in Fig. 2.79. It consists of SHA replica circuit that generates a signal equal to the common-mode level of the SHA output. From V_{cm}, the voltage V_{ref+} is derived by means of the amplifier A2 and resistor equal to half (128R) the total resistance of the ladder (256R), so assuring the correct value required at the top of the resistor ladder (i.e. $V_{ref+}=V_{cm}+V_{FS}/2$).

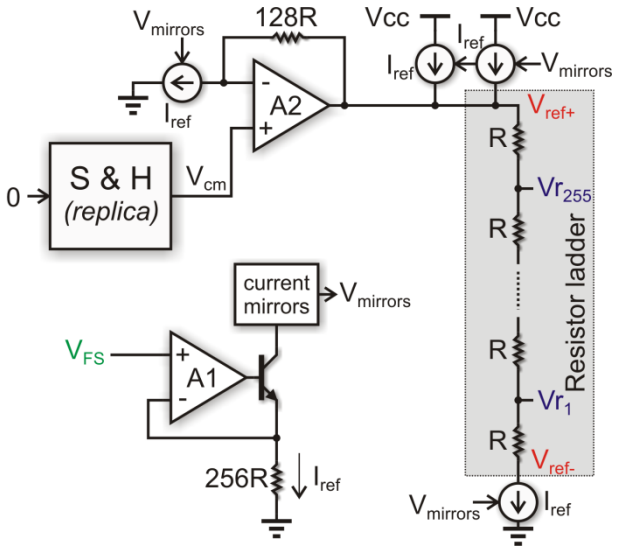

Fig. 2.79. Simplified block diagram of voltage-reference generator circuit.

Simultaneously, a current sink equal to I_{ref} is attached to the bottom of the ladder. This ensures that voltage across the ladder has the correct value. The current I_{ref} is derived from V_{FS} using a V-I converter made up of A1 and resistor equal to 256R, ensuring $I_{ref}R=V_{LSB}$.

The current output from this circuit is fed into a current mirror that generates the current sources and sinks that are required by the other parts of the reference generator.

From the above discussion, it is clear that the design of the resistor ladder in single-ended fashion in not easy, because of its complex reference generator circuit.

As aforementioned, the resistor ladder must provide the threshold voltages of the ADC. By neglecting the currents I_j, the voltages V_{rj} correspond to the ideal quantization thresholds of an N-bits ADC (see Fig. 2.78)

$$Vr_j = \frac{V_{ref}}{N_R}\left(j - \frac{N_R}{2}\right) + V_{DC} \tag{2.121}$$

depending on the dc voltage V_{DC}.

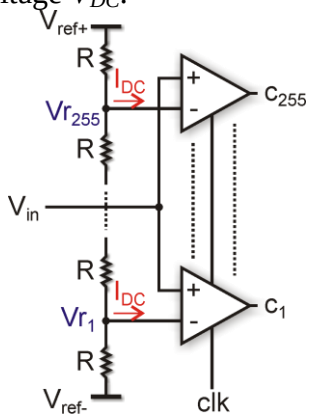

Fig. 2.80. Resistor ladder with all currents equal to I_{DC}.

Furthermore, the presence of currents I_j may substantially modify the ladder thresholds V_{rj}. Also in the simplest case in which the currents I_j are all equal to a given value (I_{DC}) (see Fig. 2.80), the resistive load seen by each current is different, therefore a non linear effect is introduced in the ladder thresholds (DC Bowing). The resulting *INL* can be easily computed (see [1]):

$$INL_j = \frac{1}{2} j\left(N_R - j\right) R I_{DC} \tag{2.122}$$

Eq. (2.122) is symmetric with respect to $j=N_R/2$, where it reaches its maximum value

$$INL_{max} = \frac{1}{8} N_R^2 R\, I_{DC} \tag{2.123}$$

Now, it is worth highlighting that the current depends on the comparator input stage. In this work, the comparator input stage is composed by a differential pair (see Fig. 2.74), depicted (with single-ended array) in Fig. 2.81.

In this case we cannot assume $I_1=I_2=...=I_{255}$, since I_j currents depend on input voltage of the comparators. Eq. (2.122), therefore, cannot be applied.

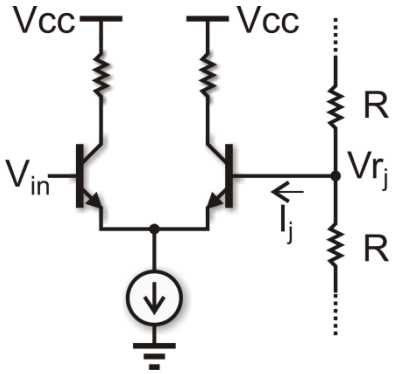

Fig. 2.81. Comparator input stage.

Furthermore, the property of symmetry around $j=N_R/2$ is no longer verified when the comparator of Fig. 2.74 is employed. In particular the non linearity is higher for low input voltages. In fact, for increasing input voltages, the I_j current shown in Fig. 2.81 decreases and becomes zero for $V_{in}>V_{rj}+4V_T$. However, as discussed in section 2.4, comparators designed according to Fig. 2.74 give the advantage of providing a low input offset voltage and a reduced recovery time.

2.5.2 Resistor Ladder: Conventional Differential Topology

The conventional resistor ladder architecture is depicted in Fig. 2.82. Firstly, it can be noted the advantages of this solution with respect to the single-ended implementation. In fact, in this case we have a differential input, thus avoiding the need of balance the common-mode output level of the SHA circuit. This latter means that the voltage-reference generator circuit is much simpler than that of the single-ended resistor ladder [13].

In this case, the full-scale quantization range is controlled by the replica bias circuit shown in Fig. 2.83. The high-gain op-amp A_1 in a positive feedback loop forces a current to a replica ladder with an externally applied voltage (V_{DC}). Unlike the single-ended configuration, the current I_{ref} is derived ensuring $I_{ref}R=V_{LSB}/2$.

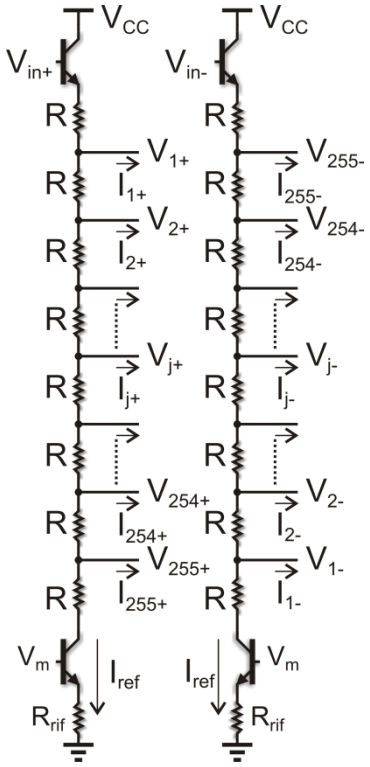

Fig. 2.82. Conventional differential resistor ladder.

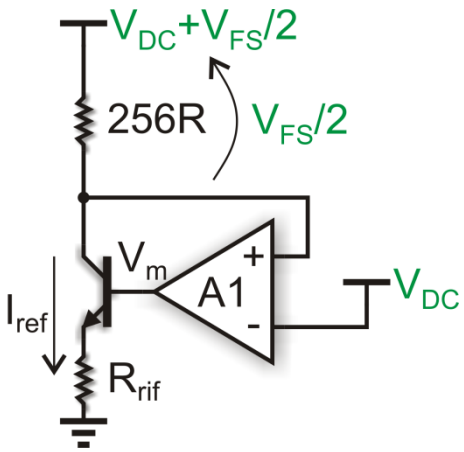

Fig. 2.83. Simplified block diagram of voltage-reference generator circuit for differential ladder.

Considering the circuit in Fig. 2.82, it can be defined the differential output voltage of the ladder (for a generic node *j*) as

$$V_{d\,j} = V_{j+} - V_{j-} \tag{2.124}$$

In this case the ladder threshold voltages V_{rj} (see Fig. 2.78) correspond to the differential input voltages for which V_{dj}=0. A simple analysis of the circuit reveals that, in the hypothesis I_{j+}=I_{j-}=0, the threshold voltages are

$$Vr_j = \frac{V_{ref}}{N_R}\left(j - \frac{N_R}{2}\right) \tag{2.125}$$

if the following polarization current I_{ref} is imposed

$$I_{ref} = \frac{1}{2}\frac{V_{ref}}{N_R R} \tag{2.126}$$

This equation can be easily verified by compensating process and temperature variation with the simple feedback circuit in Fig. 2.83.

An advantage of differential ladder is that threshold voltages are intrinsically independent from input dc voltage. This is not true for the single ended ladder (see eq. (2.121)), where a complicated feedback circuitry (see Fig. 2.79) is needed to adapt the dc value of V_{in} to the dc voltage of the ladder (V_{DC} in Fig. 2.78).

It is also interesting to observe that if the currents I_{j+}, I_{j-} are not equal, as in the case of the comparator designed in this work (see Fig. 2.74), the non linearity of each array is no longer symmetric. In this case, the non linearity of each single array, in the differential circuit, is not perfectly cancelled by the differential topology and a DC bowing effect arises.

A main drawback of the differential ladder is the long propagation delay (t_p) of the input signals through the two resistor arrays. In fact, the input signal goes through an RC delay line, where R is the unit resistor of the resistor ladder and C is the input capacitance of the comparator.

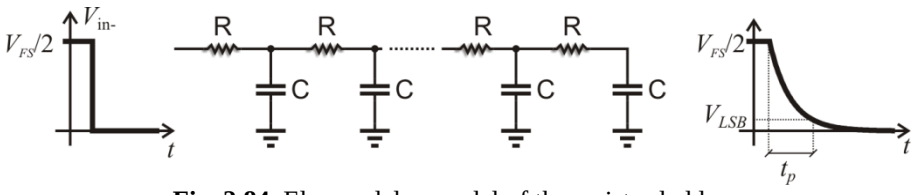

Fig. 2.84. Elmore delay model of the resistor ladder.

Consider the simplified equivalent circuit of the resistor ladder loaded with the comparators shown in Fig. 2.84. Next, by using the Elmore model for the delay calculation, in a first order approximation the propagation delay can be written as follows

$$t_p \approx \frac{N_R^2}{2}(R + r_e)\,C \;\Rightarrow\; t_p \propto \frac{N_R^2}{2}RC \tag{2.127}$$

where C is the load capacitance of each output node V_{j+} or V_{j-} , and r_e is the output resistance of the two BJTs in Fig. 2.82 ($r_e = V_T / I_{ref} + R_e$).

To overcome the speed limit of the conventional differential resistor ladder, it could be taken into account the circuit solution proposed by Kobayashi et al. [26], [27]. In Fig. 2.85 is depicted a simplified schematic of this high-speed ladder for N_R=256.

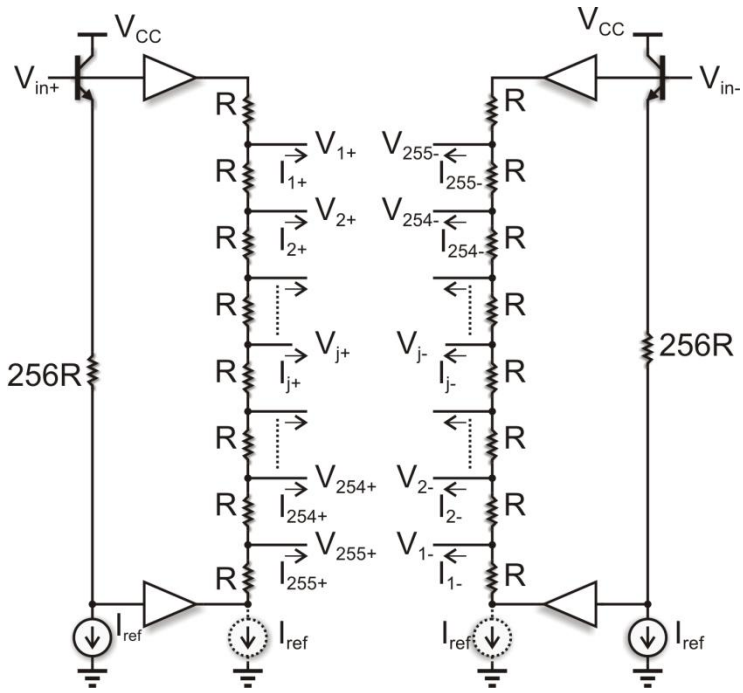

Fig. 2.85. Differential ladder proposed in [26], [27].

In this case, the resistor ladder is driven from both sides. Therefore, the propagation delay to reach the middle of the resistor ladder, where the signal is most delayed, in a first order approximation is given by

$$t_p \approx \frac{(N_R/2)^2}{2}\left(R + r_{out}\right)C \tag{2.128}$$

where r_{out} is the buffer output resistance.

By comparing eq. (2.128), (2.127) it highlights that the circuit in Fig. 2.85 can, theoretically, achieve a four-fold reduction of the propagation delay with respect to the conventional differential circuit.

Furthermore, this circuit suffers from an increasing *INL*, because the maximum differential *INL* is related to that of each single array and at least is proportional to its square length (N_R^2). This latter is confirmed by simulation results as shown in the following.

2.5.3 Proposed Differential Resistor Ladder

In this sub-section, a novel high-speed differential resistor ladder is proposed [33]. The schematic of the proposed differential resistor ladder is shown in Fig. 2.86 for the case N_R=256 (8-bits ADC).

In this circuit we observe that the input signal V_{in+} is applied to a first array composed by only two resistors. This first array generates three voltages V_{a+}, V_{b+} and V_{c+}. These three voltages drive, through three emitter followers, a second array, composed by N_R resistors. This second array is split by V_{a+}, V_{b+} and V_{c+} in two sub arrays. The upper sub array is biased with a voltage given by V_{a+}- V_{b+}=V_{ref}/4 (if eq. (2.126) is assumed). The lower sub array is biased with a voltage V_{b+}-V_{c+} which is also equal to V_{ref}/4.

The same reasoning can be applied to the two resistor arrays driven by V_{in-}, on the right side of Fig. 2.86.

If the currents I_{j+}, I_{j-} are neglected, by comparing the circuit in Fig. 2.86 with the conventional differential ladder shown in Fig. 2.82, it can be observed that the voltage drop on each sub array (of N_R/2 resistors) is exactly the same between the two circuits.

Since the arrays in the two circuits are biased with the same voltages, we can conclude that also the circuit of Fig. 2.86 gives the threshold voltages given by (2.125).

Moreover, it is worth noting that the dashed current sources shown in Fig. 2.86 are useful to reduce the dc output currents of the upper and lower emitter followers, reducing in this way the gain error of the circuit.

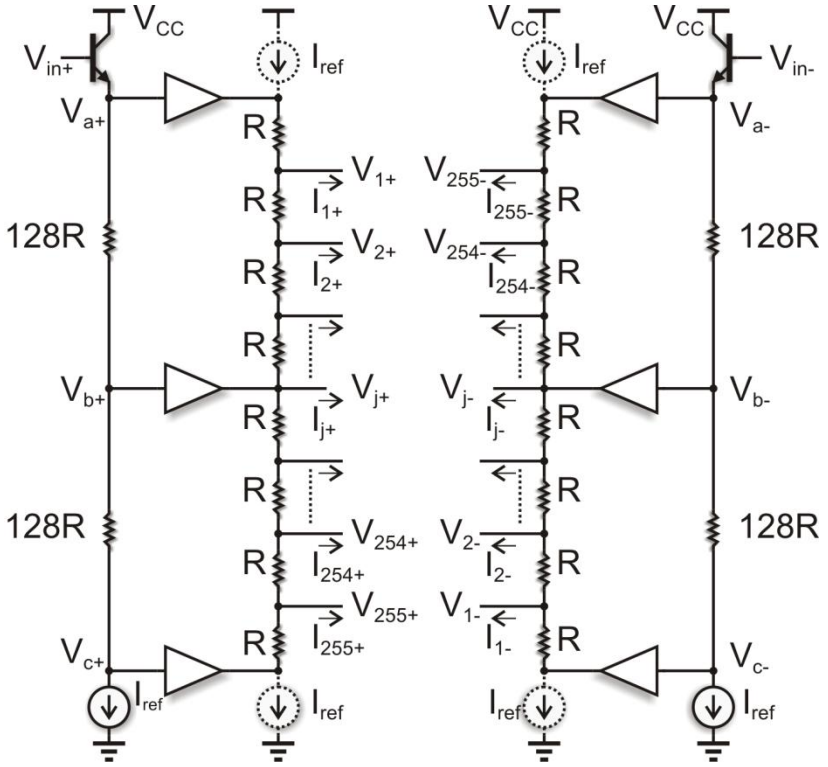

Fig. 2.86. Proposed differential ladder for N_R=256.

With reference to the linearity of the ladder, we can distinguish three contribution.

The contribution of the first arrays, which generates V_{a+}, V_{b+}, V_{c+}, V_{a-}, V_{b-} and V_{c-}, is almost negligible since these arrays are composed by only two resistors and, in addition, they are loaded with almost constant currents.

The second contribution is due to the load currents of the six buffers. The design experience shows that this contribution can be easily made negligible with a careful choice of the buffers biasing current. Additionally, the offset voltages of the buffers may also impact the ladder *INL*. This effect, however, tends to be cancelled by the CMRR (Common Mode Rejection Ratio) of the ladder load, and, therefore, becomes again ascribable to a load effect.

The final contribution, due to the four sub-arrays of $N_R/2$ resistors each, is the real linearity bottleneck. In fact, when the currents I_{j+}, I_{j-} are not equal (assuming the comparator topology used in this work,

Fig. 2.74), the *INL* of each sub-array is no longer symmetric, thus asymmetries arise which result in a non-linear behavior.

In conclusion the proposed circuit presents a non-linear behavior similar to the conventional differential topology of Fig. 2.82. The non-linearity of the proposed circuit, for N_R>32, is, in general, lower than the conventional differential topology since each sub array is composed by N_R/2 resistors (as opposed as the N_R resistors of conventional topology) and the contribution due to the buffer is nearly negligible. Thus, the maximum *INL* will be proportional to $(N_R/2)^2$.

The main advantage of the proposed circuit against the conventional topology, is the speed. In fact, the most relevant contribution to the signal propagation delay in the proposed topology of Fig. 2.86 is due to the four sub-arrays. In this case, the slowest signals are the four midpoints of each array.

Therefore, neglecting the delays of the first arrays, it follows

$$t_p \approx \frac{\left(N_R/4\right)^2}{2}\left(R+2r_{out}\right)C \;\Rightarrow\; t_p \propto \frac{\left(N_R/4\right)^2}{2}RC \qquad (2.129)$$

where r_{out} is the output resistance of the buffers driven by V_{b+} and V_{b-}. Eq. (2.129) corresponds to a sixteen-fold reduction of the propagation delay, with respect to the conventional topology (see eq. (2.127)), in the ideal case r_e=r_{out}=0. Furthermore, recalling eq. (2.128) the proposed topology results in a four-fold reduction of the propagation delay with respect to the high-speed ladder in [26],[27].

2.5.4 Resistor Ladders Performances

The proposed resistor ladder has been designed for a BiCMOS 0.25µm technology by using 50 *GHz* NPN HBT devices. For comparison also the conventional differential ladder and the high-speed ladder proposed in [26],[27] have been designed in the same technology.

In the following we will consider two N_R values: 64, 256. The ladder with N_R=64 uses R=4 Ω, while the ladder with N_R=256 uses R=1 Ω.

All arrays have been loaded with the comparator topology presented in section 2.4, which, as observed before, represents both the most critical and the most common case.

A suitable simulation set-up at the aim to observe the *INL* is defined as in Fig. 2.87.

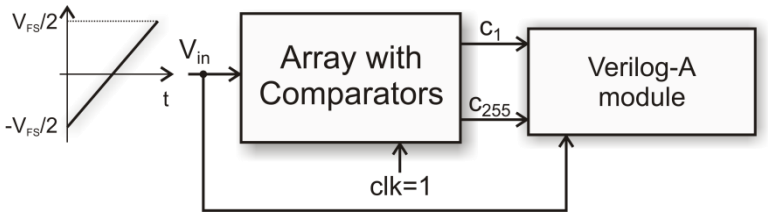

Fig. 2.87. Ladder *INL* simulation set-up.

A transient simulation has been performed by varying the input voltage V_{in} very slowly (10 *s*) from $-V_{FS}/2$ to $+V_{FS}/2$. The *VerilogA* module detects the zero-crossings of the differential outputs of the comparators. The input voltage corresponding to the output zero−crossing is stored in a data file, that is later processed in Matlab extracting *INL*, gain and offset error.

The Fig. 2.88 shows the obtained *INL* of the different ladders. It is interesting to observe the high-speed ladder [26],[27] shows an higher non-linearity with respect to conventional ladder both for N_R=64 and N_R=256. For N_R=64 the proposed ladder exhibits a maximum *INL* comparable to the conventional ladder. For N_R=256, where the contribution of buffer non-linearity becomes quite negligible, proposed circuit shows a sensible lower non-linearity with respect to conventional ladder. For sake of completeness the values of the maximum *INL* are reported in Table 2.XII.

Table 2.XII

Stated bits	**Ladder topology**	INL_{max}
6	conventional	0.011
	Kobayashi et al.	0.018
	proposed	0.009
8	conventional	0.217
	Kobayashi et al.	0.314
	proposed	0.137

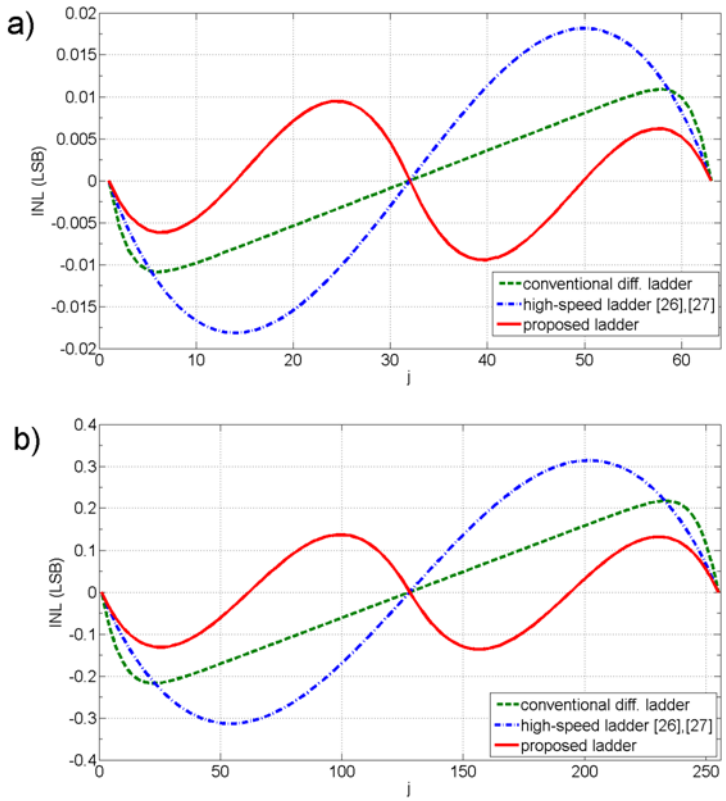

Fig. 2.88. Simulated ladders *INL*, **a)** N_R=64 (R=4 Ω); **b)** N_R=256 (R=1 Ω).

Fig. 2.89 compares a transient simulation of the proposed ladder with the simulations of the conventional and high-speed ladder of [26],[27], for N_R=256.

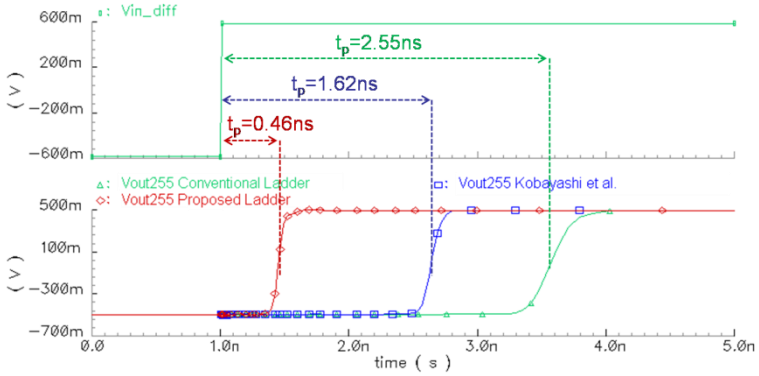

Fig. 2.89. Transient simulation of the three ladders (N_R=256, R=1 Ω).

This simulation considers a full swing switch of the ladder input voltage. In these conditions the proposed ladder is clearly faster with respect to the other circuits, with a propagation delay as low as 0.6 *ns*.

It is worth to highlight that the propagation delay may vary considerably as a function of considered ladder output or input voltage switch. A real measure of the ladder speed can only be obtained by inserting the ladder in the ADC and by measuring the total harmonic distortion (THD) of the converter as a function of sampling rate. This analysis is presented in the next section.

2.6 ADCs Performances

At this point, all the circuitry required to implement the 8-bits Flash ADC have been designed and appropriately tested. The final circuit consists of more than 2500 transistors. In order to have a real indication of the overall performances and, in particular of the effectiveness of the proposed ladder circuit, several ADCs have been designed using the Flash topology.

Furthermore, starting from the designed Flash ADC, at the aim of comparison, different ADCs have also been implemented using the Folding/Interpolating topology.

In the case of Flash converters, two circuits have been considered: a 6-bits converter (N_R=64) and a 8-bits converter (N_R=256). Both circuits employ the comparator described in section 2.4.

The Fig. 2.90 shows the *ENOB* extracted from the *THD* and the signal to noise and distortion ratio (*SNDR*) obtained by simulating the 8-bits Flash converter using the proposed ladder.

At low sampling frequencies the converter exhibits a THD of 9 bits, limited by the ladder *INL*. The resulting *SNDR* (which includes also quantization noise) is slightly lower than 8 bits. By increasing the sampling frequency, due to limited ladder speed, a dynamic non-linear behavior is introduced, which worsens the *THD*.

For $f_s \cong 630\ MHz$, the *SNDR* reduces to 7.5 bits (3 *dB* below the ideal value). From the Shannon theorem we can conclude that the effective resolution bandwidth (*ERB*) of this converter is 630/2 = 315 *MHz*.

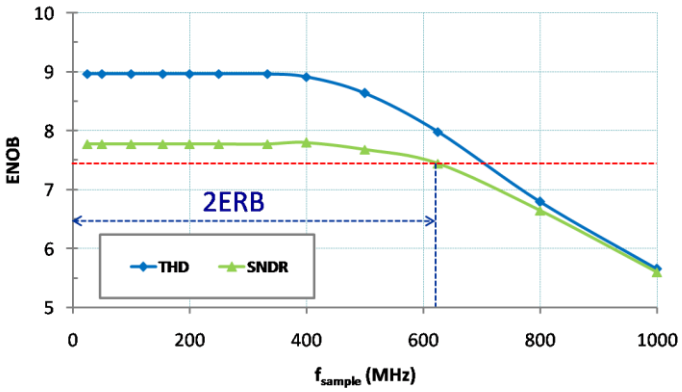

Fig. 2.90. Simulated *ENOB* extracted from the *THD* and the *SNDR* for the 8-bits Flash converter using proposed ladder.

The Table 2.XIII reports the ERB obtained by simulating Flash ADCs designed by using the proposed, the conventional and the high−speed [26], [27] ladder topologies.

Table 2.XIII

ADC topology	# bits	ladder topology	ERB (MHz)	ladder		ADC	
				P_D (mW)	FOM (pJ/conv.)	P_D (mW)	FOM (pJ/conv.)
Flash	6	conventional	370	37	1.10	354	10.6
		high-speed [10],[11]	735	79	1.19	397	6.0
		proposed	890	94	1.17	411	5.1
	8	conventional	65	37	1.57	1322	56.2
		high-speed [10],[11]	125	79	1.75	1364	30.1
		proposed	315	94	0.82	1379	12.1
Folding and Interp.	8	conventional	525	65	0.34	472	2.48
		proposed	905	216	0.66	623	1.90
	9	conventional	340	65	0.26	764	3.10
		proposed	645	216	0.46	915	1.96

For 8-bits converters the proposed solution results in about a 4.8 times higher *ERB*. A bandwidth larger than previous high-speed ladder is also highlighted in the case of 6-bits converters.

The simulated Folding/Interpolating converters employ the topology described in [26]-[28]. Two converters have been considered with a resolution of 8 bit and 9 bit, respectively. The 8-bits converter

uses a ladder with N_R=42, while the 9-bits converter employs a ladder with N_R=82.

The Table 2.XIII reports the obtained ERB. The proposed topology is effective also in increasing the effective bandwidth of Folding/Interpolating converters.

The Table 2.XIII includes also Power Dissipation data and Figure of Merit performance, computed according to the specification in (1.15).

By looking to the power dissipation data reported in Table 2.XIII it can be observed that proposed ladder requires a substantial higher power with respect to other ladders.

As an example, in Flash 8 bit case, the proposed ladder results in an about 2.5 times larger power with respect to conventional ladder. However, in Flash and in Folding & Interpolating converters, the power is dominated by the comparators and by the folders. As a consequence the higher power of proposed ladder results only in a marginal power dissipation increase if we look at the whole converter. As an example, in the 8-bits Flash converter, the power dissipation increases only of the 4.3% by using the proposed solution with respect to the conventional ladder.

Similar conclusions can be drawn by analyzing the Figure of Merit of the ladders and the whole ADCs.

Finally, the designed ADCs can be added to Fig. 1.19, reported below (Fig. 2.91).

The designed flash ADCs are plotted considering the maximum achievable sampling frequency (two times the *ERB*). The corresponding *ENOB*, extracted from *SNDR*, is also labeled.

As an example the designed 6-bits Flash ADC (green circle with *ENOB*=5.5) shows a resolution similar to the other flash ADCs in the same range of sampling frequency.

On the other hand, the designed 8-bits Flash ADC (green circle with *ENOB*=7.5) shows better resolution than the other flash ADCs. However, this advantage is paid in terms of reduced maximum sampling frequency.

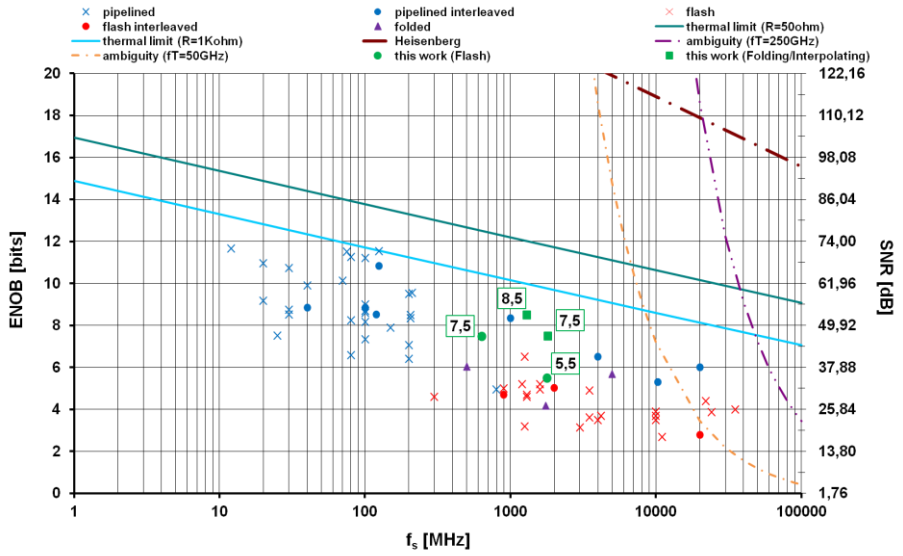

Fig. 2.91. ENOB versus sampling frequency, and limitations imposed by thermal noise (solid lines), comparator ambiguity (orange and purple dashed lines), and Heisenberg principle (brown dashed line).

The designed Folding/Interpolating ADCs (green square in Fig. 2.91) show better performances than the other Folding/Interpolating ADCs. However, it is worth highlighting that the layout implementation of the designed ADCs can worse their performances, although they currently show a good margin with respect to the other converters plotted in Fig. 2.91.

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International Symposium on International Symposium on Circuits And Systems, pp.1723-1726, June 2010.

Chapter 3

Step-Up DC-DC Converter

Dc-dc converters play a fundamental role in applications as traction, drive systems of electric vehicles, high performance drive, small-scale energy storage, renewable energy generation, novel electric distribution and smart grids systems.

The dc-dc converters, used in these applications, are required to step-up a low voltage level to much higher voltage level (usually more than two times the input voltage), both in normal and heavy operating conditions.

It can be also noted that in all these applications, the high-step-up dc-dc converters can be nonisolated but they should operate at high efficiency while taking high currents from low-voltage dc sources at their inputs. As well known, conventional boost converters, due to limitations on the maximum duty cycle, are not able to meet high step–up ratio.

Instead, the aforementioned applications require high-voltage step-up and high-efficiency power conversion. Under such conditions, it is a major challenge to operate the boost converters at high efficiency [1]. This is because, with the high-output voltage, the switch power device (i.e. power VD-MOS) has to block a large voltage and hence the on-state resistance will be very high. Furthermore, the low-level input voltages cause large input currents to flow through the switches.

The extreme duty-cycle operation drives short-pulsed currents with high amplitude to flow through the output diodes and the capacitors; which cause severe diode reverse recovery problem and increases in the conduction losses. The high on-resistance of the switches, the increased conduction losses, and the severe reverse-recovery problem will degrade the efficiency and limit the power level of the conventional boost converters [1], [2].

Moreover, the parasitic ringing, present in the practical circuits, induces additional voltage stresses and necessitates the use of switches with higher blocking voltage ratings, which will lead to more losses [3].

From the above discussion, it is immediately apparent that the choice of the most suitable topology is a continuous challenge, requiring to focus on various technical aspects that demand for the optimization of both the circuit and devices.

There are several suitable topologies to boost the input voltage to required voltage output; these topologies differ in terms of both step-up gain and performances.

As well known it might be very useful to employ coupled-inductor configurations for obtaining high efficiency and high voltage gain [3]-[8]. In fact, the turns ratio of the magnetically coupled inductors can be effectively used to reduce the duty ratio and the voltage stress of the switch [9], [10]. Therefore, for high-voltage step-up applications, the coupled inductor boost converter can be more efficient than the conventional boost converter.

3.1 Conventional and Coupled Inductors Converters

The conventional boost converter topology is preferred in medium-high power stepping up voltage applications due to the simple and reliable design. The considered boost converter topology shown in Fig. 3.1.a) includes a resistor R that accounts for inductor resistive losses, a power MOS switch, a fast-recovery power PiN diode, while the load is modeled with a dc current source I_{out}.

The input voltage in series with the inductor acts as a current source. The energy stored in the inductor builds up when the switch is closed. When the switch is opened, the inductor discharges current to the load with the input voltage source still connected. This results in an output voltage across the capacitor larger than the input voltage. The load consists of a dc current source in parallel with a filter capacitor. The capacitor voltage is larger than the input voltage. The capacitor must be large enough to keep a constant output voltage, and acts to reduce the ripple in the output voltage. Under steady-state, by considering the volt-second balance condition to the inductor L, the output voltage gain for step-up is

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{3.1}$$

where D is the duty cycle.

Increased voltage gain can be obtained with a coupled boost converter, whose scheme is shown in Fig. 3.1.b). In this case there are two resistors that account for the inductors copper losses: R_1 is referred to the primary inductor L_1, while R_2 to the secondary inductor L_2. Neglecting the power losses, the voltage gain for the circuit in Fig. 3.1.b) is

$$\frac{V_{out}}{V_{in}} = \frac{1+N_w D}{1-D} \tag{3.2}$$

where $N_w=N_{w2}/N_{w1}$ is the winding ratio of the magnetically coupled inductors, while N_{w1} and N_{w2} are the winding turns of the primary and secondary inductors. The coupling coefficient, k, is considered ideal (k=1).

By comparing eq. (3.1) and (3.2), it can be noted that the voltage step-up ratio of the coupled inductors configuration depends not only on the duty-cycle but also on the winding ratio.

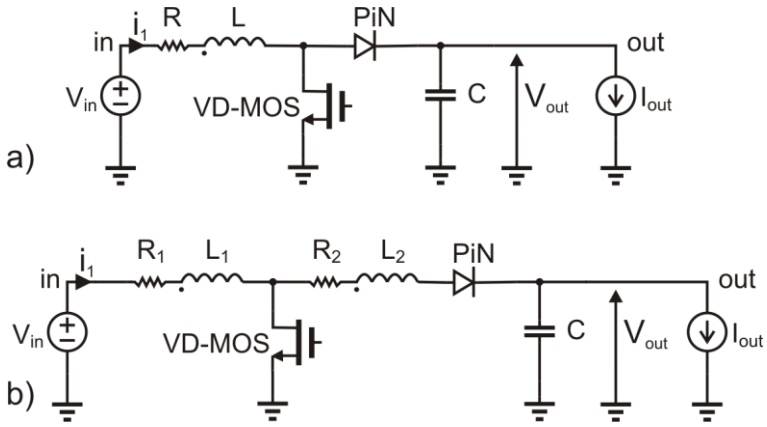

Fig. 3.1. Boost converter **a)** Conventional; **b)** Coupled-inductor.

3.2 Converter Comparison

Since most of the efficiency is due to device behavior, a great attention has been devoted to proper modeling of the power MOS and the PiN diode shown in Fig. 3.1. In the test circuit, the employed diode model is the one described in [11]-[13] and fitted to the parameters of a commercial fast recovery power PiN diode with a maximum forward current I_F=60 *A* and breakdown voltage V_R=400 *V* (IR 60EPU04PbF).

The power MOS model fits to the parameters of a commercial MOS (IXYS IXTQ52N30P) with a maximum drain-source voltage V_{DS}=300 *V* and current I_{DS}=52 *A*.

The input voltage is V_{in}=50 *V*. The desired output power is 300 *W* with dc load I_{out}=2 *A*, while the output voltage is V_{out}=150 *V*, corresponding to a step-up ratio of 3. Steady state duty cycle is obtained from (3.2).

Once given the output voltage ripple (ΔV_{out}=0.02V_{out}) and the steady state switching frequency f_{sw} (45 *kHz*) for the circuit of Fig. 3.1.a) the filter capacitance (C=10 μF) can be derived as follows

$$C = \frac{I_{out}}{\Delta V_{out}} \frac{D}{f_{sw}} \tag{3.3}$$

Furthermore, in a boost converter continuous conduction mode (CCM) is the preferred mode of operation for high-power applications when compared to the discontinuous conduction mode (DCM), because CCM has lower conduction loss and smaller current stress on the semiconductor devices [14], [15]. The CCM operation occurs when the current through the inductor in the converter circuit is continuous, with the inductor current always greater than zero.

At the aim of guarantee the *CCM* operation, the total inductance (L in Fig. 3.1.a) and L_1+L_2+2M with $M=k(L_1L_2)^{1/2}$ in Fig. 3.1.b) must verify the following constraint on its minimum value

$$L > \frac{\left(V_{out} - V_{in}\right)\left(1-D\right)^2}{2I_{out} f_{sw}} = L_{\min} \tag{3.4}$$

In order to fairly compare the converters of Fig. 3.1, it has been assumed that the same devices and the same components are used in both topologies. In particular, with reference to the inductors, it is

assumed that the same total windings are used in both Fig. 3.1.a) and Fig. 3.1.b).

As a consequence, if L_0 is the inductance of a single winding, the inductance L of Fig. 3.1.a) is

$$L = \left(N_{w1} + N_{w2}\right)^2 L_0 \tag{3.5}$$

and the following equation is obtained for

$$\begin{cases} L_1 = \dfrac{L}{\left(1+N_w\right)^2} \\ L_2 = \dfrac{N_w^2}{\left(1+N_w\right)^2} L = N_w^2 L_1 \end{cases} \tag{3.6}$$

The total inductance of the coupled inductors of Fig. 3.1.b) is equal to the inductance of Fig. 3.1.a).

Hence, the total inductors copper resistance R is the same but is split into two contributions as

$$\begin{cases} R_1 = \dfrac{R}{1+N_w} \\ R_2 = R\dfrac{N_w}{1+N_w} \end{cases} \tag{3.7}$$

The inductance value has been fixed at $L=5mH$ assuring the *CCM* operation for all the considered N_w values.

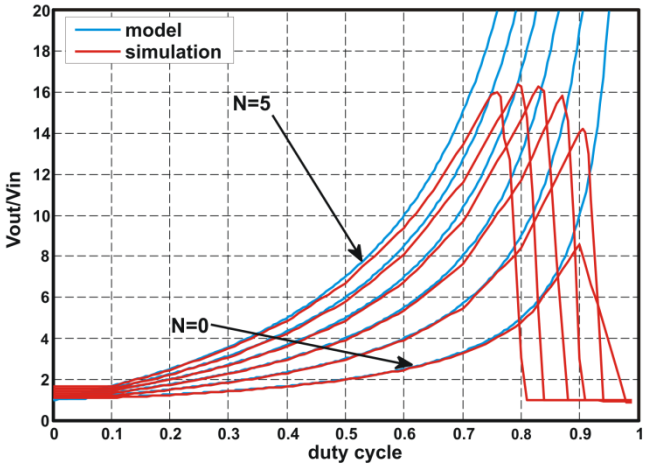

Fig. 3.2. Voltage gain versus duty-cycle and N_w values.

Fig. 3.2 reports voltage gain versus duty cycle for different winding ratio values (N_w=*[0,..,5]*). Increasing the winding ratio N_w and fixing the duty cycle, higher step up ratio is observed.

On the other hand, the duty-cycle of the conventional boost converter (N_w=0) increases with the increase of the voltage step-up ratio, while the coupled-inductors reduces the necessary duty-cycle for a given ste-up gain.

Fig. 3.2 also reports the gain obtained from the numerical *Spice/VerilogA* simulations for a fixed *MOS* switching duty cycle. The numerical simulation are in close agreement with the theoretical value of eq. (3.2) for duty cycle lower than 0.7. For high duty cycle values, converter losses start dominating and the gain drops.

It is evident from the above discussion that the turns ratio N_w is a key design parameter of a coupled inductors converter. Thus, it would be useful a power losses model to determine what is the optimal value of the winding ratio that minimizes losses, while maximizes the efficiency.

In the next section an efficiency analysis of the converter will be presented.

3.3 Power Losses Model

A power losses model for the boost converters of Fig. 3.1 has been developed that includes passive as well as the active circuit components [16].

Power loss contributions depend on the winding ratio N_w helping the designer to choose the N_w value that maximizes converter efficiency. The inductors copper losses are

$$P_{R_1} = \frac{1}{T}\int_T R_1 I_1^2 dt = \frac{1}{T}\left[\int_{T_{on}} R_1 I_1^2\left(T_{on}\right)dt + \int_{T_{off}} R_1 I_1^2\left(T_{off}\right)dt\right] = \\ = \frac{T_{on}}{T} R_1 \left(\frac{N_w+1}{1-D}\right)^2 I_{out}^2 + \frac{T_{off}}{T} R_1 \frac{I_{out}^2}{\left(1-D\right)^2} \tag{3.8}$$

where $T_{on}=DT$, $T_{off}=(1-D)T$ and $T= T_{on}+T_{off}$ is the switching time period, while L_1 current, I_1, during T_{on} and T_{off} is

$$I_1(T_{on})=\frac{1+N_w}{1-D}I_{out} \quad I_1(T_{off})=I_2=\frac{I_{out}}{1-D} \tag{3.9}$$

I_2 is the current in inductor L_2. Recalling eq. (3.2) and (3.7), eq. (3.8) can be rewritten as

$$P_{R_1}=\frac{RI_{out}^2}{1+N_w}\left[\begin{array}{l}\frac{(V_{out}-V_{in})V_{out}}{V_{in}^2}+\frac{(V_{out}-V_{in})}{V_{in}}N_w+\\ +\frac{1}{1+N_w}\left(\frac{V_{out}}{V_{in}}+N_w\right)\end{array}\right] \tag{3.10}$$

As for the loss contribution of the primary winding, the power dissipation on the resistor R_2 can be obtained as

$$P_{R_2}=RI_{out}^2\frac{N_w}{(1+N_w)^2}\left(\frac{V_{out}}{V_{in}}+N_w\right) \tag{3.11}$$

Fig. 3.3 shows the comparison between eq. (3.10), (3.11) and numerical simulation data. It can be noted a very good agreement between the model and numerical simulation data.

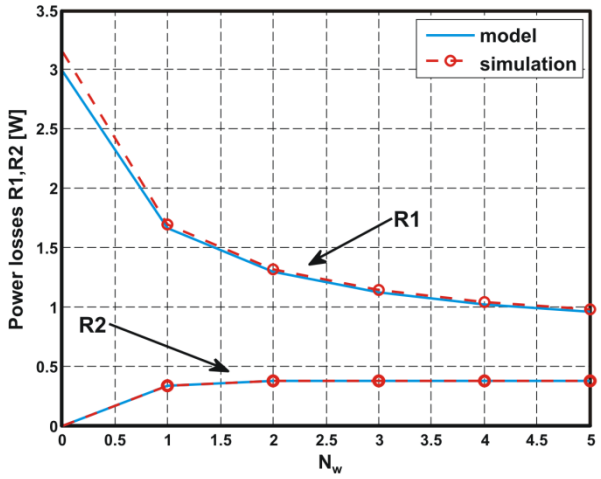

Fig. 3.3. Inductors copper losses versus winding ratio.

MOS power losses are divided into static *MOS* dissipation and switching losses. Static losses are

$$P_{MOS_{on}} = \frac{1}{T}\int_{T} R_{DS} I_{DS}^2 dt \tag{3.12}$$

where R_{DS} is the *MOS* on-resistance, I_{DS} is equal to I_1 (eq. (3.9)) during T_{on} and is zero during T_{off}. Hence, eq. (3.12) becomes

$$P_{MOS_{on}} = R_{DS} I_{out}^2 \frac{(V_{out} - V_{in})}{V_{in}} \left[\frac{V_{out}}{V_{in}} + N_w \right] \tag{3.13}$$

MOS switching losses can be expressed as [1]

$$P_{MOS_{sw}} = \frac{1}{2} V_{DS_{off}} I_{DS_{on}} \left(t_{c_{on}} + t_{c_{off}} \right) f_{sw} \tag{3.14}$$

where the off drain-source voltage V_{DSoff} can be expressed as

$$V_{DS_{off}} = V_{in} + \frac{(V_{out} - V_{in})}{1 + N_w} \tag{3.15}$$

while the conduction current is equal to I_1 during T_{on} (eq. (3.9))

$$I_{DS_{on}} = \frac{1 + N_w}{1 - D} I_{out} \tag{3.16}$$

and f_{sw} is the switching frequency. The *MOS* turn-on characteristic time t_{con} is the sum of rise and fall time of drain current and drain-source voltage, respectively (see Fig. 3.4).

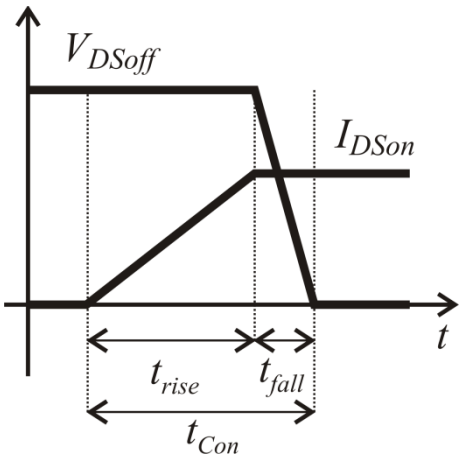

Fig. 3.4. *MOS* turn-on characteristic times.

Instead, t_{coff} is defined in a complementary way. Furthermore, according to the simulation results the worst-case for the total time $t_c = t_{con} + t_{coff} \cong 175$ *ns* has been chosen.

Finally, eq. (3.14) can be rewritten as follows

$$P_{MOS_{sw}} = \frac{t_c}{2}\frac{I_{out}^2}{C\Delta V_{out}}\left(V_{out} - V_{in}\right)\left[1 + \frac{V_{out} - V_{in}}{V_{in}\left(1 + N_w\right)}\right] \tag{3.17}$$

In Fig. 3.5 the *MOS* dissipation power behavior is depicted.

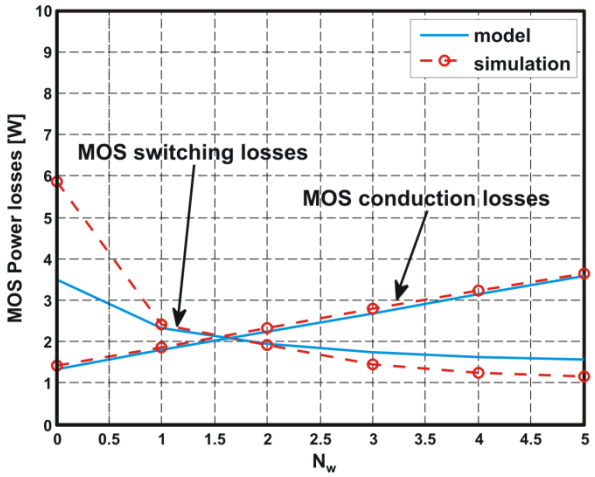

Fig. 3.5. *MOS* power losses versus winding ratio.

It is worth noting that the gate-charge contribution to the *MOS* power losses, according to simulation results, is negligible with respect to the other contributions, thus, in a first order approximation, it will be not included in the model.

The last contributions, concerning the diode conduction and switching power dissipation, are shown in Fig. 3.7. The conduction loss is

$$P_{diode_{on}} = \frac{1}{T}\int_T V_F I_F dt \tag{3.18}$$

where V_F is the forward voltage drop on the diode, and according to the simulation results is V_F=1 *V*, while I_F is the forward current (eq. (3.9)), hence it follows

$$P_{diode_{on}} = V_F I_{out} \tag{3.19}$$

Diode switching losses are [1]

$$P_{diode_{sw}} = \frac{1}{2} I_{rr} t_b V_R f_{sw} \tag{3.20}$$

I_{rr} is the reverse recovery peak current and can be evaluated according to the simulation results as

$$I_{rr} \simeq \alpha\left(I_F - \Delta I_{pk-pk}/2\right) \tag{3.21}$$

with $\alpha=1.8$, where $\Delta I_{pk\text{-}pk}$ is the forward current peak to peak ripple (see Fig. 3.6).

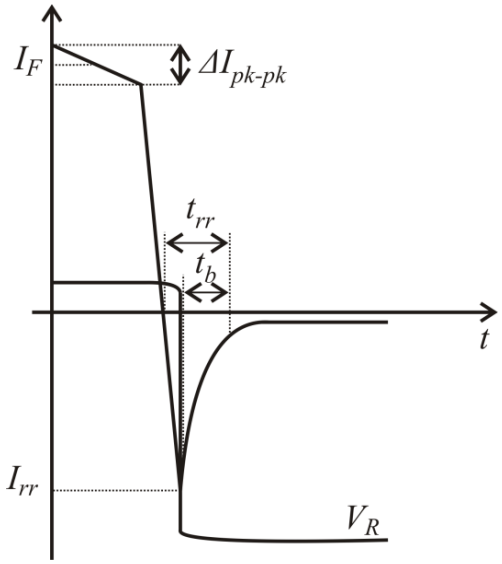

Fig. 3.6. *PiN* diode turn-off.

The reverse voltage drop is $V_R=N_wV_{in}+V_{out}$, while t_b is part of the total reverse recovery time and, in this case, about *35 ns*.

Substituting in eq. (3.20) gives

$$\begin{aligned} P_{diode_{sw}} = {} & \frac{\alpha}{2} t_b I_{out}^2 \frac{\left(V_{out}-V_{in}\right)}{V_{in} C \Delta V_{out}} \frac{\left(V_{out}+N_w V_{in}\right)}{\left(1+N_w\right)} + \\ & -\frac{\alpha}{2} t_b \frac{V_{in}\left(V_{out}-V_{in}\right)}{2L}\left(1+N_w\right) \end{aligned} \tag{3.22}$$

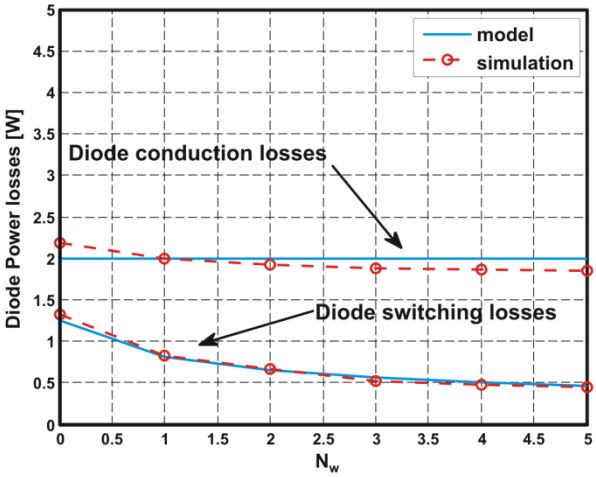

Fig. 3.7. Diode power losses versus winding ratio.

3.4 Simulation Results

The total power losses can be obtained as function of N_w, from eq. (3.10), (3.11), (3.13), (3.17), (3.19), (3.22), and is depicted with the resulting efficiency in Fig. 3.8.

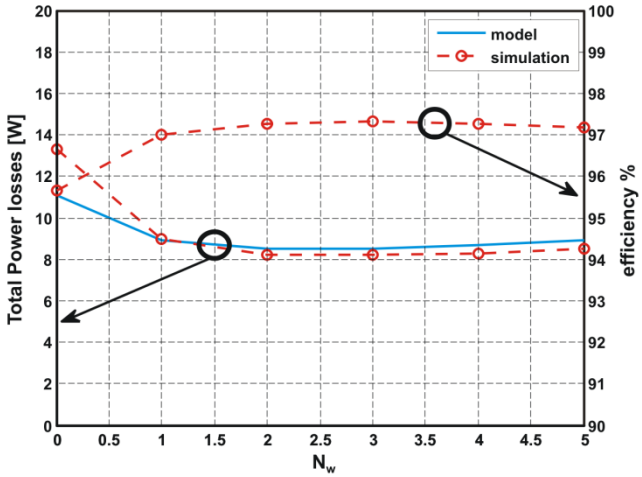

Fig. 3.8. Power losses and converter efficiency as function of N_w.

Considered *N* values range from 0 to 5. The case *N=0* corresponds to the conventional step-up converter of Fig. 3.1.a).

Numerical results are in good agreement with the proposed analytical model showing that the proposed approach is promising for the analytical optimization of converter design.

Converter efficiency shows a maximum value for *N≅2*. A significant improvement is obtained passing from *N=0* to *N=1*. The curve is quite flat for *N>1* and hence also *N=1* is a feasible design choice.

Further results regarding converter efficiency are shown in Fig. 3.9.

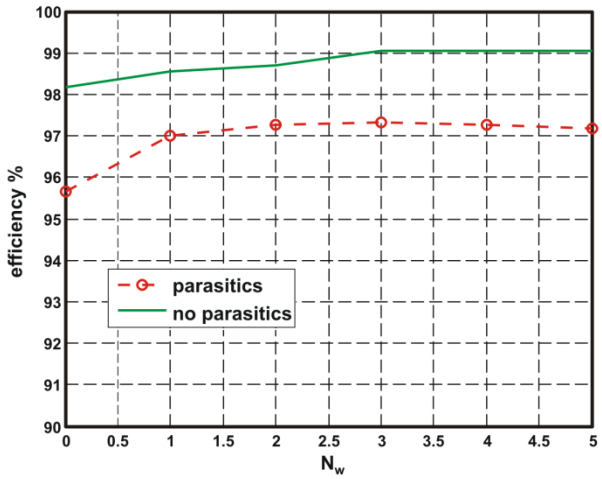

Fig. 3.9. Converter efficiency as function of the winding ratio. Green line: ideal switch and diode models; red line: accurate switch and diode models.

Two cases are considered. The first case (green line) includes inductor resistive losses but uses ideal switch and diode components. The second case (red line) includes the effect of accurate switch and diode models, as reported in section 3.2, showing that around 1% efficiency loss is dependent on device behavior demonstrating the need of accurate device models.

In conclusions, it can be noted that for a given voltage step-up ratio, the coupled-inductors circuit is more efficient than the conventional circuit. An analytical model of the power losses has been

developed, whose usefulness is clearly showed in deriving the optimal value of the winding ratio. However, also *Spice* numerical simulations have been performed for better understanding the incidence of parasitic phenomena which could compromise converter efficiency and reliability.

Next chapter will be devoted to developed a suitable control strategy improving the dynamic characteristics of the coupled-inductors converter.

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Chapter 4

Control Strategy

A control technique suitable for dc-dc converters must comply with their inherent non-linearity. In fact, control should ensure system stability in any operating condition and good static and dynamic performances. In other words, these characteristics should be guaranteed in spite of wide input voltage and load variations, while maintaining a good dynamic behavior [1].

The dc-dc converters are natural nonlinear and time variant systems, and do not lend themselves to the application of linear control theory. As a consequence, the classical control approaches could be not adequate to dc-dc converters. On the other hand, the sliding mode control technique for VSS (Variable Structure Systems) offers an alternative way to implement a control action which exploits the inherent variable structure nature of dc-dc converters. In fact, VSS are defined as systems where the circuit topology is intentionally changed, following certain rules, to improve the system behavior in terms of speed of response, stability, and robustness [2].

The sliding mode control offers these advantages with a relatively simple implementation. Some drawbacks derive from theoretical complexity, which can make selection of control parameters difficult, and necessity, in theory, of sensing of all state variables and generation of suitable references for each of them. In practice, converter control can be done effectively by sensing only one inductor current in addition to the output voltage [1].

From the above discussion is clear that it is appropriate to use sliding mode controllers for the control of dc-dc converters [3].

In this chapter, it is presented the various aspects concerning the sliding mode controller, which includes the choice of state space variables and sliding surface, the existence properties and the selection of the control parameters.

Moreover, a constrained optimization problem is formulated in order to derive from a single algorithm the characteristic parameters of

both coupled-inductor converter and sliding surface for guaranteeing the stability requirements, even in presence of large load variations.

At this purpose a control law, obtained in presence of small errors with respect to reference quantities, is proven to be feasible also for large disturbances, by employing a filtering action of the reference quantities. In other words, these last ones are varied, depending on the load change, according to a slower dynamics, so assuring the existence of the sliding mode. The slow sequence of operating conditions allows to justify the assumption of negligible state-space errors.

Furthermore, analog and digital controllers have been implemented in high-level modules by using a suitable hardware description language. In particular, the *VerilogA* and *VerilogAMS* for the analog and digital controller, respectively [4]. Instead, the dc-dc converter circuit has been designed at transistor-level by using also accurate *Spice* models for the power semiconductor devices as already described in section 3.1. The full system derives from a single design flow and includes power, analog, digital circuits that work together. The Cadence Design Environment has been adopted for the circuit verification through mixed-level simulations, in order to confirm the validity of the proposed converter analysis and design methodology.

4.1 Sliding Mode Control

The sliding mode approach proposed in [5] has been performed for the coupled inductor converter in Fig. 4.1. The first step for modeling the proposed topology of dc-dc converter is the choice of state space variables. As suggested in [3], the current of both inductor windings is discontinuous, thus unsuitable as state variable, while the magnetic flux in the coupled-inductor core is continuous.

Since the magnetic flux is not directly measurable, the current i_m, defined as follows, will be employed

$$i_m = \begin{cases} i_1 & t \in T_{on} \\ i_1\left(1+N_w\right) & t \in T_{off} \end{cases} \tag{4.1}$$

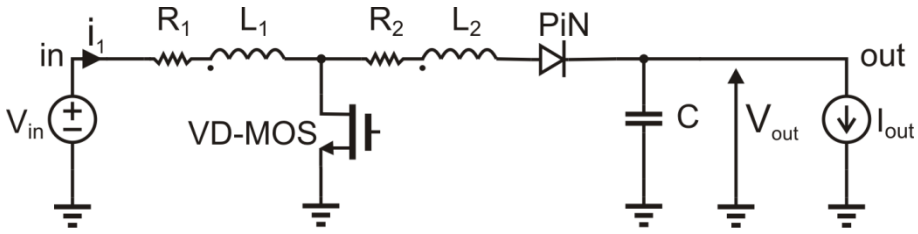

Fig. 4.1. Coupled-inductors step-up converter.

where, $T_{on}=DT$, $T_{off}=(1-D)T$ and $T= T_{on}+T_{off}$ is the switching time period, N_w is the turns ratio, and i_1 is the primary winding current. Additionally the output voltage v_{out} has been chosen as state variable.

By referring to (4.1) and Fig. 4.1, the following relationships can be stated

$$\begin{cases} \dfrac{di_m}{dt} = \dfrac{v_{in}-R_1 i_m}{L_1}u + \dfrac{(v_{in}-v_{out})}{L_1(1+N_w)}(1-u) - \dfrac{(R_1+R_2)}{L_1(1+N_w)^2} i_m (1-u) \\ \dfrac{dv_{out}}{dt} = \dfrac{i_m}{(1+N_w)C}(1-u) - \dfrac{i_{out}}{C} \end{cases} \tag{4.2}$$

where $u \in \{0, 1\}$. More specifically, $u=1$ when the *MOS* is ON; $u=0$ when the *MOS* is OFF. It must be note that these state-space equations include the coupled-inductors copper and core losses through the resistors R_1 and R_2 in (4.2).

By keeping in mind the approach proposed in [7], [8], if the vector **x** of state-variables error is defined as

$$\mathbf{x} = \left[x_1, x_2\right]^T = \left[i_m - I_m^{ref}, v_{out} - V_{out}^{ref}\right] \tag{4.3}$$

the following standard modeling can be deduced

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}u + \mathbf{A}\mathbf{z} + \mathbf{F} \tag{4.4}$$

where the vector of references is $\mathbf{z} = \left[I_m^{ref}, V_{out}^{ref}\right]^T$ and $I_m^{ref} = \dfrac{1+N}{1-D} I_{out}^{ref}$.

Matrix **A**, **B**, **F** are defined as

$$\mathbf{A} = \begin{pmatrix} -\dfrac{(R_1+R_2)}{L_1\cdot(1+N_w)^2} & -\dfrac{1}{L_1\cdot(1+N_w)} \\ \dfrac{1}{(1+N_w)\cdot C} & 0 \end{pmatrix}$$

$$\mathbf{B}=\begin{pmatrix} \dfrac{v_{in}}{L_1}-\dfrac{R_1}{L_1}\cdot i_m-\dfrac{\left(v_{in}-v_{out}\right)}{L_1\cdot\left(1+N_w\right)}+\dfrac{\left(R_1+R_2\right)}{L_1\cdot\left(1+N_w\right)^2}\cdot i_m \\ -\dfrac{i_m}{\left(1+N_w\right)\cdot C} \end{pmatrix}$$

$$\mathbf{F}=\begin{pmatrix} \dfrac{v_{in}}{L_1\cdot\left(1+N_w\right)} \\ -\dfrac{i_{out}}{C} \end{pmatrix}$$

The reference value of duty ratio is estimated as

$$D=\frac{1-\dfrac{v_{in}}{v_{out}}}{1+N_w\dfrac{v_{in}}{v_{out}}} \tag{4.5}$$

According to the variable structure system theory, a sliding surface has to be chosen, within the state variables space, where control functions are discontinuous.

The following sliding surface is chosen

$$S\left(\mathbf{x}\right)=\beta_1 x_1+\beta_2 x_2=\boldsymbol{\beta}^{\mathbf{T}}\mathbf{x} \tag{4.6}$$

where $\boldsymbol{\beta}^{\mathbf{T}}=[\beta_1, \beta_2]$ and the surface is a linear combination of the state-variables errors.

The existence condition of the sliding mode requires that all state trajectories near the surface are directed towards it, [2]. In mathematical terms the necessary and sufficient condition is expressed by

$$\begin{cases} \dot{S}\left(\mathbf{x}\right)<0 \quad if\ S\left(\mathbf{x}\right)>0 \\ \dot{S}\left(\mathbf{x}\right)>0 \quad if\ S\left(\mathbf{x}\right)<0 \end{cases} \tag{4.7}$$

In order to ensure that the system state remains near the sliding surface, a proper operation of the switch is required designing a discontinuous control law to force the system to move on the sliding mode surface in a finite time

$$u=\begin{cases} 0 \ \ if \ \ S(\mathbf{x})>0 \\ 1 \ \ if \ \ S(\mathbf{x})<0 \end{cases} \tag{4.8}$$

Recalling (4.4), (4.6), (4.8) the existence conditions (4.7) can be rewritten as follows

$$\begin{cases} \lambda_1(\mathbf{x}) = \boldsymbol{\beta}^{\mathbf{T}}\mathbf{A}\mathbf{x} + \boldsymbol{\beta}^{\mathbf{T}}\mathbf{G} < 0 & S(\mathbf{x}) > 0 \\ \lambda_2(\mathbf{x}) = \boldsymbol{\beta}^{\mathbf{T}}\mathbf{A}\mathbf{x} + \boldsymbol{\beta}^{\mathbf{T}}\mathbf{B} + \boldsymbol{\beta}^{\mathbf{T}}\mathbf{G} > 0 & S(\mathbf{x}) < 0 \end{cases} \tag{4.9}$$

where $\mathbf{G} = \mathbf{A}\mathbf{z} + \mathbf{F}$.

If the inequalities (4.9) are satisfied for a region that contains the sliding surface $S(x)=0$, then the trajectories starting from any point on this region will converge to the surface (hitting condition) and once they reach it, they will stay on it [9].

On the assumption that the error variables are conveniently smaller than the corresponding references, the following inequalities can be derived from (4.9) for guaranteeing the sliding mode existence

$$\begin{cases} \lambda_1(\mathbf{x}) = \boldsymbol{\beta}^{\mathbf{T}}\mathbf{G} < 0 & S(\mathbf{x}) > 0 \\ \lambda_2(\mathbf{x}) = \boldsymbol{\beta}^{\mathbf{T}}\mathbf{B} + \boldsymbol{\beta}^{\mathbf{T}}\mathbf{G} > 0 & S(\mathbf{x}) < 0 \end{cases} \tag{4.10}$$

The equations $\lambda_1(\mathbf{x})=0$, $\lambda_2(\mathbf{x})=0$ define two lines in the phase plane Fig. 4.2. If both the intersection of line $\lambda_1(\mathbf{x})=0$ with the x_2 axes and of $\lambda_2(\mathbf{x})=0$ with the x_1 axes are positive, then the existence region includes the origin (which represents the steady-state point) [2]. Thus, assuring that the state trajectory of the system under sliding mode operation will always reach a stable equilibrium point.

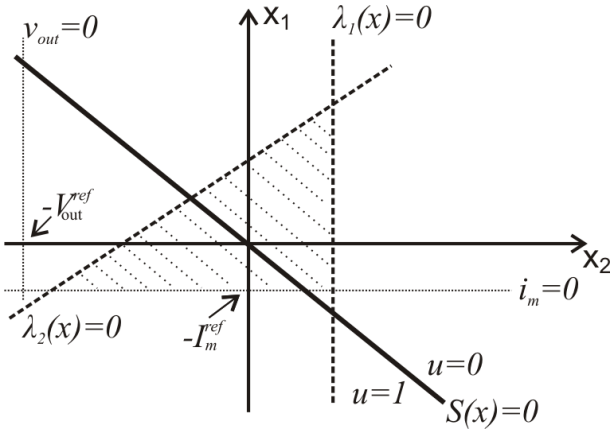

Fig. 4.2. State variable plane. The dashed area is the region in which sliding surface exists.

In the ideal case of sliding mode operating at infinite switching frequency, state trajectories are directed toward the sliding surface and

move exactly along it. Instead, in the actual case of finite switching frequency, it must be employed a circuit features a practical relay, thus a suitable hysteresis band has to be foreseen and, hence, the control law (see Fig. 4.3) becomes

$$u = \begin{cases} 0 \;\; if \;\; S(\mathbf{x}) > +\Delta \\ 1 \;\; if \;\; S(\mathbf{x}) < -\Delta \end{cases} \tag{4.11}$$

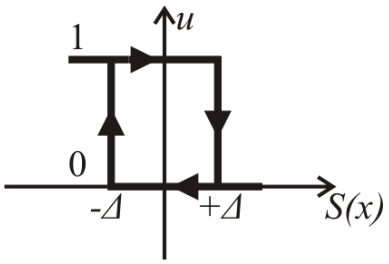

Fig. 4.3. Control law with hysteresis. When *u*=1 switch is ON. When *u*=0 switch is OFF.

where Δ is an arbitrarily small positive quantity, while 2Δ is the amount of hysteresis in the sliding surface.

The hysteresis band defines the boundary conditions $S=+\Delta$ and $S=-\Delta$. So, the hysteresis modulation does not allow to switch the control on the surface $S(x)=0$, but on the lines $S=+\Delta$ and $S=-\Delta$ resulting in oscillations of width 2Δ around sliding surface as shown in the following Fig. 4.4.

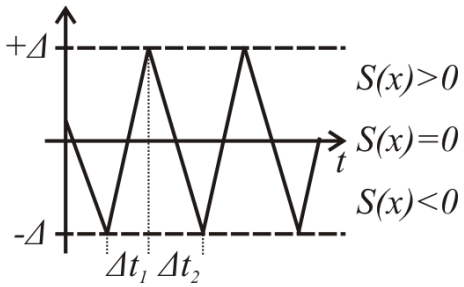

Fig. 4.4. Example of variation of the *S* function versus time.

The time intervals Δt_1 and Δt_2 represent the on and off state of the switch respectively. So we can write [7]

$$f_{sw} = \frac{1}{\Delta t_1 + \Delta t_2} \tag{4.12}$$

where

$$\Delta t_1 = \frac{2\Delta}{\boldsymbol{\beta}^{\mathrm{T}}\mathbf{B} + \boldsymbol{\beta}^{\mathrm{T}}\mathbf{G}}$$
$$\Delta t_2 = \frac{-2\Delta}{\boldsymbol{\beta}^{\mathrm{T}}\mathbf{G}} \tag{4.13}$$

while the duty cycle can be expressed as

$$D = \frac{\Delta t_1}{\Delta t_1 + \Delta t_2} \tag{4.14}$$

Since system behavior depends on both circuit and control parameters, it is worth to highlight the importance of a simultaneous design in order to comply with the working constraints of the switching converter.

4.2 Optimization Procedure for Parameters Extraction

Aim of this section is determining an optimization procedure able to derive the parameters of the coupled-inductor converter and the sliding mode controller.

Target of the design is the satisfaction of the design constraints (output voltage ripple and value, switching frequency) while guaranteeing the stability of the control even in presence of large load variations.

The assigned quantities, indicated in the following with the symbol $\boldsymbol{\theta}$, in the design problem are the hysteresis band, the output capacitance, the input voltage, the load current. So, $\boldsymbol{\theta}$ can be expressed as a vector

$$\boldsymbol{\theta} = \left[\Delta, C, v_{in}, i_{out}\right]^T \tag{4.15}$$

The copper and core losses of the coupled inductor have been considered in conservative way globally equal to 1% of the input power.

Table I provides the assigned input parameters.

Table 4.I

Parameters	Value
Δ	1
C	50 μF
$v_{in}=V_{in}$	50 V
$i_{out}=I_{out}$	2 A

The vector of variables is

$$\mathbf{y}=\left[y_1,y_2,y_3,y_4,y_5\right]^T=\left[\beta_1,\beta_2,N_w,L,D\right]^T \tag{4.16}$$

It is trivial to remark that these ones are each other dependent, both from the point of view of the physical mechanism and the control strategy.

The input power $P_{in}=f(y)$ is a function of the vector of variables and can be expressed as follows

$$P_{in}=\frac{1}{T}\int_T v_{in}i_1=V_{in}I_{out}\left(\frac{1+y_3y_5}{1-y_5}\right) \tag{4.17}$$

The goal function $\varphi(\mathbf{y})$, provides the overall power losses by using the analytical model reported in section 3.3. Target of the optimization is the minimization of $\varphi(\mathbf{y})$ that is here written as a function of the vector of variables of the optimization problem.

$$\begin{aligned}\varphi(\mathbf{y})=&\frac{R}{1+y_3}\frac{(1+y_3)^2y_5}{(1-y_5)^2}i_{out}+\frac{R}{1+y_3}\frac{i_{out}^2}{(1-y_5)}+\\&+R\frac{y_3}{1+y_3}\frac{i_{out}^2}{(1-y_5)}+R_{DS}\frac{(1+y_3)^2y_5i_{out}^2}{(1-y_5)^2}+\\&+\frac{1}{2}t_c\left[v_{in}+\frac{(v_{out}-v_{in})}{(1+y_3)}\right]\frac{i_{out}(1+y_3)}{(1-y_5)}f_{sw}+v_Fi_{out}\\&+\frac{1}{2}t_b\left[\begin{array}{l}\alpha\dfrac{i_{out}}{(1-y_5)}+\\-\dfrac{(v_{out}-v_{in})(1-y_5)}{2y_4f_{sw}}\end{array}\right](v_{out}+v_{in}y_3)f_{sw}\end{aligned} \tag{4.18}$$

where $R = 0.01V_{in}/I_{out}(1+y_3\,y_5)/(1- y_5)$.

Eq. (4.18) must be minimized while satisfying the equality constraint of (4.14) that as a function of the vector of variables becomes

$$y_5 = -\frac{y_1 A_{11} x_1 + y_1 A_{12} x_2 + y_2 A_{21} x_1 + y_1 G_{11} + y_2 G_{21}}{y_1 B_{11} + y_2 B_{21}} \tag{4.19}$$

where matrix ***A***, ***B***, ***G*** have been defined in section 4.

The inequality constraints are (4.9) and the ones for guaranteeing that the existence region includes the origin.

For sake of completeness they are rewritten as

$$\begin{aligned} \lambda_1(\mathbf{x}) &= (y_1 A_{11} x_1 + y_1 A_{12} x_2 + y_2 A_{21} x_1 + \\ &+ y_1 G_{11} + y_2 G_{21}) < 0 \\ \lambda_2(\mathbf{x}) &= (y_1 A_{11} x_1 + y_1 A_{12} x_2 + y_2 A_{21} x_1 + + y_1 B_{11} + y_2 B_{21} \\ &+ y_1 G_{11} + y_2 G_{21}) > 0 \end{aligned} \tag{4.20}$$

$$\begin{aligned} \lambda_1(0, x_2) &> 0 \\ \lambda_2(x_1, 0) &> 0 \end{aligned} \tag{4.21}$$

Furthermore it is necessary to satisfy the constraints on CCM converter operation. Recalling eq. (3.4), reported below for clarity

$$L > \frac{(V_{out} - V_{in})(1-D)^2}{2 I_{out} f_{sw}} = L_{\min} \tag{4.22}$$

and then rewritten as a function of the vector of variables

$$y_4 > \frac{(v_{out} - v_{in})(1 - y_5)^2}{2 i_{out} f_{sw}} \tag{4.23}$$

Moreover, considering the constraint to obtain the desired output voltage ripple (eq. (3.3)), it can be rewritten as

$$C > \frac{i_{out}}{\Delta V_{out}} \frac{y_5}{f_{sw}} \tag{4.24}$$

Then, it has been imposed the constraint on the minimum winding ratio and the maximum switching frequency expressed as follows

$$\begin{aligned} y_3 &\geq 1 \\ f_{sw} &\leq 50\, kHz \end{aligned} \tag{4.25}$$

Finally, the optimization procedure can be summarized in the compact form

$$\begin{cases} \min \varphi(\mathbf{y}, \boldsymbol{\theta}) \\ e(\mathbf{y}, \boldsymbol{\theta}) = 0 \\ h(\mathbf{y}, \boldsymbol{\theta}) \geq 0 \end{cases} \tag{4.26}$$

where the vector functions $e(\mathbf{y},\boldsymbol{\theta})$ and $h(\mathbf{y}, \boldsymbol{\theta})$ represent the equality and inequality constraints respectively.

The optimization procedure has been conducted using the sequential quadratic programming algorithm available in the *Matlab* optimization toolbox.

Table 4.II provides the variables vector values obtained by performing the proposed procedure on the assumption of negligible state-space errors. The latter means that we can consider (4.3) $\mathbf{x}\approx 0$ or rather

$$\begin{cases} i_m \simeq I_m^{ref} \\ v_{out} \simeq V_{out}^{ref} \end{cases} \tag{4.27}$$

Table 4.II

Parameters	Value
β_1	1.72
β_2	4.069
N	2.2
L	4 mH
D	0.387

As previously discussed, from Table 4.I and Table 4.II the total resistance that models copper and core losses can be derived as

$$R = 82.9\, m\Omega \tag{4.28}$$

4.3 Converter Performances

A *50 V* to *150 V* step-up coupled inductor converter with nominal output power rating of *300 W* has been designed considering the key circuit parameters listed in Table 4.I and Table 4.II and using the electronic device models presented in section 3.1.

A set of simulations has been conducted to validate the proposed design procedure. The scheme of the controller is presented in Fig. 4.5.

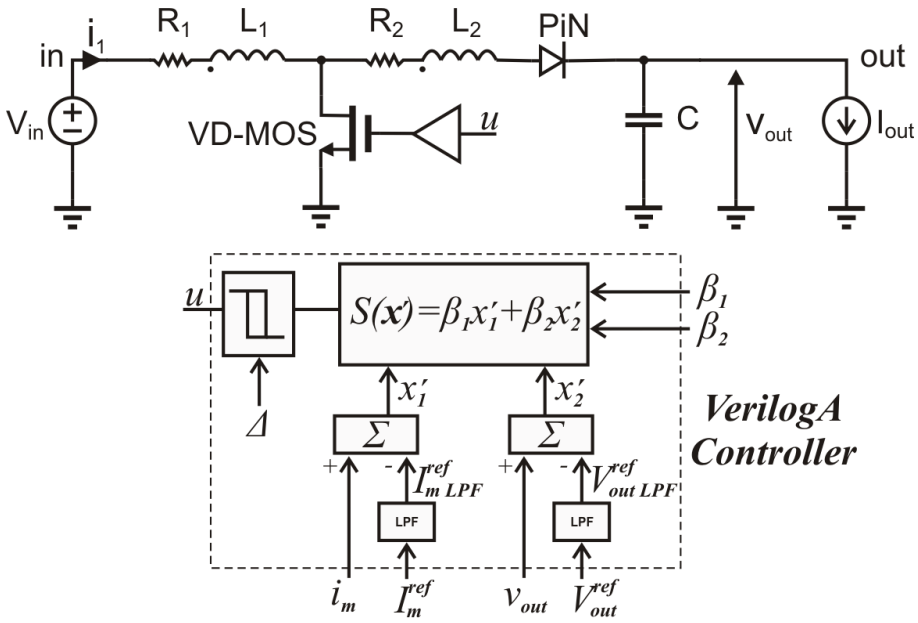

Fig. 4.5. The scheme of the analog controller.

The full system consists of the power stage designed at transistor-level, also including the accurate device models presented in section 3.1, and the analog controller implemented using *VerilogA* modules.

Now, it can be described the principle of operation. The status of the switch u (see Fig. 4.5) is controlled by the hysteresis block which maintains $S(\mathbf{x})$ near zero.

A filtering action of the reference quantities is useful to satisfy the assumption of state variables error smaller than references. These latter are varied according to a slower dynamics, so assuring the existence of the sliding mode from every starting point. In fact when the drive system is away from the set point, the system presents a large output error, while slow sequence of operating conditions allows to enforce the state variable to track the desired reference.

The numerical results for voltage and current tracking errors are depicted in Fig. 4.6 and Fig. 4.7 respectively. It is worth highlighting that in Fig. 4.6 and Fig. 4.7 are reported the state-variables tracking errors both in the cases of filtered references (red line) and no filtered references (dashed blue line). It can be noted that in the case of

filtered references the system, after a transient time, reaches a stable operating condition or rather the error goes to about zero.

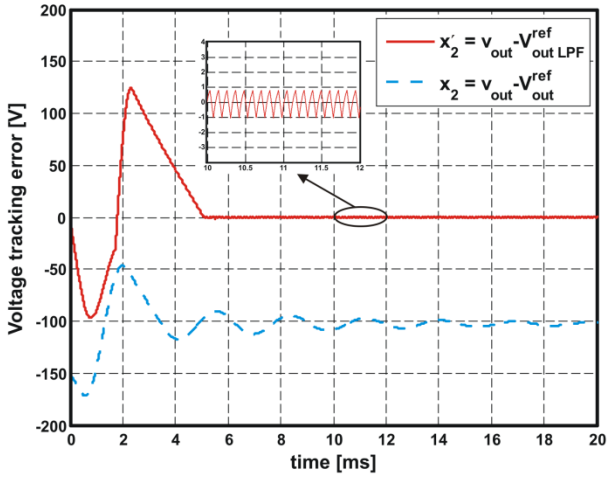

Fig. 4.6. Voltage tracking error. Red line: filtered references; dashed blue line: no filtered references.

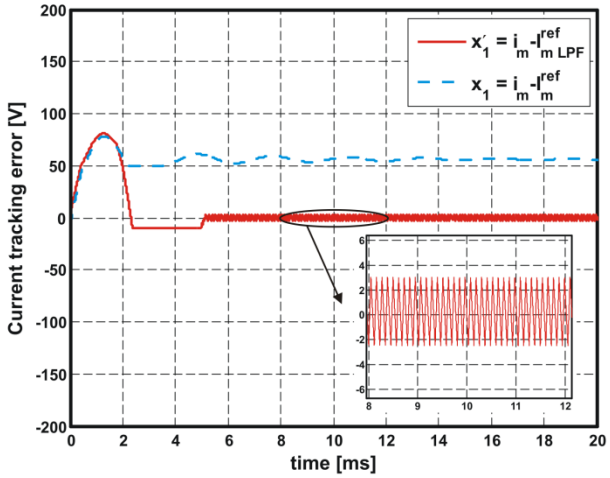

Fig. 4.7. Current tracking error. Red line: filtered references; dashed blue line: no filtered references.

On the other hand, when the reference quantities are not filtered the error is still large and doesn't converge to zero as desired.

Fig. 4.8 highlights the output voltage of the coupled inductor converter under sliding mode operation and full-load condition.

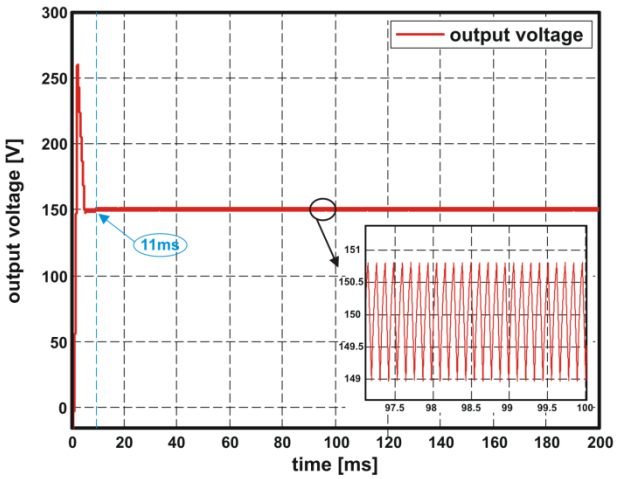

Fig. 4.8. Transient response on V_{out} using proposed sliding mode control.

The control shows a stable behavior allowing fast and safe settling of the output voltage. The steady-state operation is reached in less than *11 ms*.

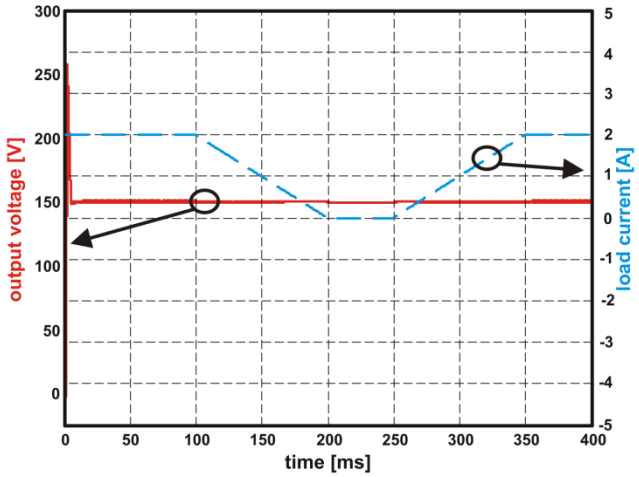

Fig. 4.9. Output voltage for load variation, under proposed sliding mode control.

The output voltage manifests oscillations around the desired steady-state value due to the hysteresis modulation, however in the range of the desired output voltage ripple as imposed by eq. (4.24). The estimated efficiency of the converter is *95.2%*.

The second set of simulations investigates the robustness of the sliding mode control against load variations (Fig. 4.9).

If a 100% load variation is assumed to occur in a time interval equal to *100 ms*, the controller shows a fast and consistent dynamical response demonstrating a suitable performance over a wide range of operating conditions.

Furthermore, digital controllers are becoming very attractive in dc-dc converters because of the inherently lower sensitivity to process and parameter variations, programmability, ability to implement sophisticated control schemes, and ease of integration with other digital systems [10]-[12].

Another very important advantage is the flexibility inherent in any digital controller, which allows the designer to modify the control strategy, or even to totally reprogram it, without the need for significant hardware modifications [13].

Thus, the controller has also been implemented in a digital way by using an analog-to-digital conversion of the state-variables. The ADC and the other parts of the digital control section have been implemented in *VerilogA*-*Verilog-AMS* modules, in order to explore the possibility of integrating an ADC in the control loop without performance loss with respect to the analog implementation.

Moreover, it is also useful verify the effectiveness of the proposed control technique and of the optimization procedure by using a digital controller.

The schematic diagram of the digital controller is reported in Fig. 4.10. In this case the control section includes a *VerilogA* model of an 8-bits ADC providing the digital representation of the state-variables.

The entire system has been designed considering the same circuit parameters and detailed device models of the system of Fig. 4.5.

The simulation has been effected using Cadence *Spectre/VerilogA–AMS* tool. Fig. 4.11 depicts the converter output voltage for both analog and digital control.

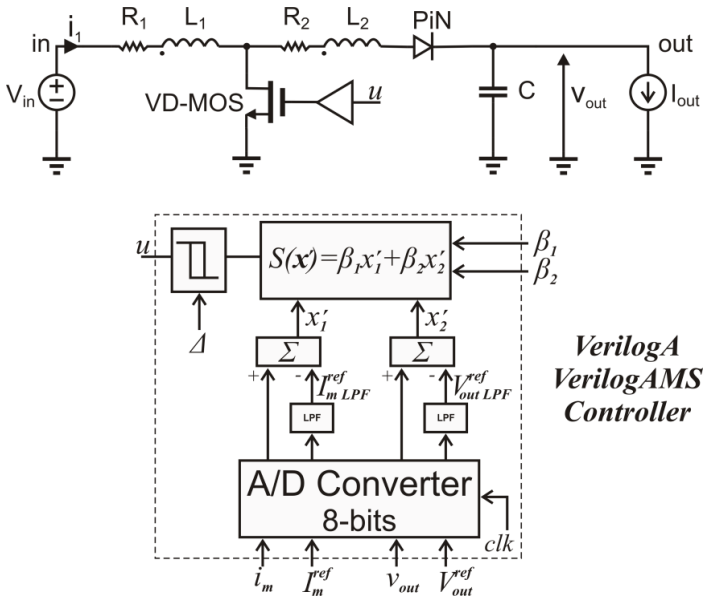

Fig. 4.10. The scheme of the digital controller.

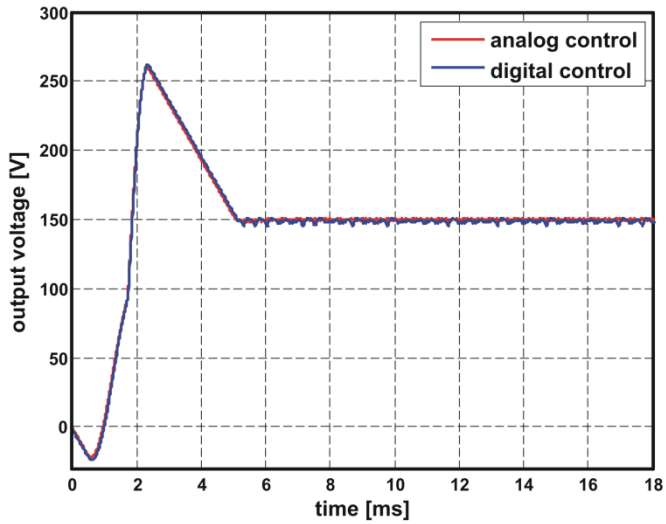

Fig. 4.11. Transient response on V_{out} using proposed sliding mode technique both for analog (red line) and digital (blue line) control.

It is worth highlighting the inherent quantization noise due to the analog-to-digital conversion process worsening the steady-state performance but also the good dynamic behavior practically similar to

the analog counterpart. This latter issue confirms the good performance of the digital controller and makes promising the use of IC ADCs.

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Conclusions

This thesis presented the design of a power/analog/digital system. It consisted of a power stage designed at transistor-level, also including accurate power device models, and a control section implemented by using HDL modules. Furthermore, the controller is implemented both in analog and digital way. This last complies with the growing requirements of more sophisticated control approaches, where the design of custom integrated digital controllers is presented like a viable solution for the next generation of high performance power supplies.

This dissertation made an effort to address these requirements by designing an high-performance ADC useful not only for the control application aforementioned but also for applications with huge requirements in terms of speed and signal bandwidth.

In fact, among the most important devices in mixed systems is certainly the ADC that is required providing high performance in terms of both speed (maximum sample rate) and resolution (effective number of bits). The ADC designed in this work is derived from the Flash architecture, chosen for its inherent ability to provide the desired output in one clock cycle.

Downstream of study, analysis and design of the main circuits comprising in the Flash topology (track and hold amplifier, comparators, resistor arrays) and their extensive simulation, the resistor ladder resulted the speed bottleneck of ADC. It was, therefore, proposed a novel high-speed differential resistor ladder.

This configuration allowed to obtain, in a first order approximation, a sixteen-fold reduction of the propagation delay, with respect to the conventional topology and a four-fold reduction of the propagation delay with respect to the high-speed ladder proposed by Kobayashi which represented the state-of-the-art for this circuit in bipolar technology.

Moreover, the proposed circuit presented a non-linear behavior better than the other topologies. Numerical simulation results also highlighted the effectiveness of the proposed solution in increasing the effective resolution bandwidth of the designed ADCs, with only a little increase of power dissipation. Thus, the designed ADC could be

a viable solution for the integrated digital control of the coupled inductors step-up dc-dc converter presented in this work.

The coupled-inductor configuration showed to be effective for obtaining high efficiency and high voltage gain. In fact, the turns ratio of the magnetically coupled inductors was effectively used to reduce the duty ratio and the voltage stress of the switch. Therefore, for high voltage step-up applications, the coupled inductor boost converter resulted more efficient than the conventional boost converter.

Furthermore, an analytical model of the converter power losses was proposed whose main advantages were prediction of efficiency and usefulness in deriving the optimal value of the winding ratio. The proposed model was in good agreement with the numerical simulation results showing that the proposed approach was promising for the analytical optimization of converter design. In fact, this model has been used as goal function in a constrained optimization problem, formulated in order to derive from a single algorithm the characteristic parameters of both coupled-inductor converter and controller. The control strategy proposed in this work was the sliding mode technique that showed its well-known properties of robustness against disturbances and uncertainties.

The analog controller has been implemented in *VerilogA* module, while, using the analog to digital conversion, the same control technique has also been implemented in a digital section by using *VeriloA-VerilogAMS* modules. A set of numerical simulations have confirmed the validity of the proposed technique, showing a stable control behavior allowing fast and safe settling of the output voltage. Hence, the overall system, including power, analog, digital circuits was verified through mixed-level simulations, in order to confirm the validity of the proposed analysis and design methodology.

The research presented in this work was an attempt to address the problems related to the design and verification of complex power/analog/digital mixed-systems and to reduce the distance between the tools and the design methodology of power electronics, analog and digital designers.

Appendix A

A.1 Distortion Analysis of the Emitter-Follower

An analysis of distortion introduced by the THA and its dependence on the bias current, amplitude and frequency of the input signal, and hold capacitance is a key step in the design of the circuit itself.

By referring to the emitter-follower shown in Fig. A.1, it can be written

$$I_E = \frac{I_S}{\alpha_F} \exp\left(\frac{V_{BE}}{V_T}\right) \tag{A.1}$$

From (A.1) it can be obtained

$$V_E = V_B - V_T \ln I_E - V_T \ln \frac{\alpha_F}{I_S} \tag{A.2}$$

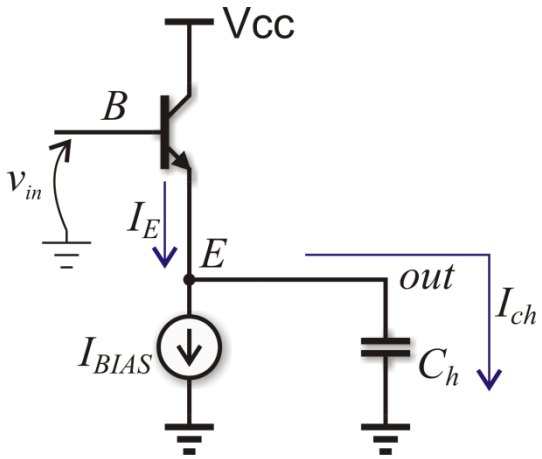

Fig. A.1. Emitter follower.

In dc bias condition, it can be obtained

$$I_{Ch} = 0 \Rightarrow I_E = I_{BIAS} \tag{A.3}$$

and eq. (A.2) can be written as

$$V_{E0} = V_{B0} - V_T \ln I_{BIAS} - V_T \ln\left(\frac{\alpha_F}{I_S}\right) \tag{A.4}$$

When a small signal v_{in} is applied (see Fig. A.1), it follows

$$V_E = V_{E0} + v_{out} \tag{A.5}$$

$$V_B = V_{B0} + v_{in} \tag{A.6}$$

Recalling eq. (A.2), (A.3), substitution of (A.5), (A.6) into (A.2) gives

$$V_{E0} + v_{out} = V_{B0} + v_{in} - V_T \ln\left(I_{BIAS} + I_{Ch}\right) - V_T \ln\left(\frac{\alpha_F}{I_S}\right) \tag{A.7}$$

By substituting (A.4) in (A.7), after some calculations we have

$$v_{out} = v_{in} - V_T\left[\ln\left(1 + \frac{I_{Ch}}{I_{BIAS}}\right)\right] \tag{A.8}$$

The current flowing through C_h, using the approximation $v_{in} \cong v_{out}$, is

$$I_{Ch} \simeq C_h \frac{dv_{in}}{dt} \tag{A.9}$$

Assuming a sinusoidal input voltage $v_{in}(t)=A\sin(2\pi f_{in}t)$, (A.9) becomes

$$I_{Ch} \simeq C_h 2\pi f A\cos\left(2\pi f_{in}t\right) \tag{A.10}$$

Considering $I_{Ch} << I_{BIAS}$ and keeping in mind the Taylor series

$$\ln(1+x) \simeq x - \frac{x^2}{2} + \frac{x^3}{3} + o\left(x^4\right) \text{ when } x \ll 1$$

and neglecting the terms higher than the third, it can be obtained

$$v_{out} = v_{in} - V_T\left[\frac{I_{Ch}}{I_{BIAS}} - \frac{1}{2}\left(\frac{I_{Ch}}{I_{BIAS}}\right)^2 + \frac{1}{3}\left(\frac{I_{Ch}}{I_{BIAS}}\right)^3\right] \tag{A.11}$$

Use of (A.10) in (A.11) gives

$$v_{out} = A\sin\left(2\pi f_{in}t\right) - V_T\left[\begin{array}{l} \dfrac{C_h 2\pi f_{in} A\cos\left(2\pi f_{in}t\right)}{I_{BIAS}} + \\ -\dfrac{\left(C_h 2\pi f_{in} A\cos\left(2\pi f_{in}t\right)\right)^2}{2I_{BIAS}^2} + \\ +\dfrac{\left(C_h 2\pi f_{in} A\cos\left(2\pi f_{in}t\right)\right)^3}{3I_{BIAS}^3} \end{array}\right] \tag{A.12}$$

After some calculations, it can be derived

$$\begin{aligned} v_{out} &= A\sin\left(2\pi f_{in}t\right)+\frac{1}{4}\left(\frac{AC_h 2\pi f_{in}}{I_{BIAS}}\right)^2 V_T + \\ &-\left[\left(\frac{AC_h 2\pi f_{in}}{I_{BIAS}}\right)+\frac{1}{4}\left(\frac{AC_h 2\pi f_{in}}{I_{BIAS}}\right)^3\right]V_T\cos\left(2\pi f_{in}t\right)+ \\ &+\frac{1}{4}\left(\frac{AC_h 2\pi f_{in}}{I_{BIAS}}\right)^2 V_T\cos\left(2\pi 2 f_{in}t\right)+ \\ &-\frac{1}{12}\left(\frac{AC_h 2\pi f}{I_{BIAS}}\right)^3 V_T\cos\left(2\pi 3 ft\right) \end{aligned} \tag{A.13}$$

Now, assuming $i_{C\,max}=2\pi f_{in}C_hA$, (A.13) becomes

$$\begin{aligned} v_{out} &= A\sin\left(2\pi f_{in}t\right)+\frac{1}{4}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^2 V_T + \\ &-\left[\left(\frac{i_{c\max}}{I_{BIAS}}\right)+\frac{1}{4}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^3\right]V_T\cos\left(2\pi f_{in}t\right)+ \\ &+\frac{1}{4}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^2 V_T\cos\left(2\pi 2 f_{in}t\right)+ \\ &-\frac{1}{12}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^3 V_T\cos\left(2\pi 3 f_{in}t\right) \end{aligned} \tag{A.14}$$

In (A.14) the term $\left[\left(\frac{i_{c\max}}{I_{BIAS}}\right)+\frac{1}{4}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^3\right]V_T \ll A$ and can be neglected, so obtaining

$$\begin{aligned} v_{out} &= A\sin\left(2\pi f_{in}t\right)+\frac{1}{4}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^2 V_T + \\ &+\frac{1}{4}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^2 V_T\cos\left(2\pi 2 f_{in}t\right)+ \\ &-\frac{1}{12}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^3 V_T\cos\left(2\pi 3 f_{in}t\right) \end{aligned} \tag{A.15}$$

Finally, the harmonic components are:

- fundamental frequency $\Rightarrow \quad H_1 = A$
- second order $\Rightarrow \quad H_2 = \frac{1}{4}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^2 V_T$
- third order $\Rightarrow \quad H_3 = \frac{1}{12}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^3 V_T$

Recalling the specification in sub-section 1.3.2, the *n-th* harmonic distortion HD_n can be obtained as

$$HD_2 = \frac{H_2}{H_1} = \frac{1}{4}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^2 \frac{V_T}{A}$$
$$HD_3 = \frac{H_3}{H_1} = \frac{1}{12}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^3 \frac{V_T}{A} \qquad \text{(A.16)}$$

It can be noted that the harmonic distortion is proportional to i_{Cmax}/I_{BIAS}. As a consequence an increase of the input signal frequency increases distortion, while reducing the hold capacitance decreases distortion.

Furthermore, an increase of the bias current I_{BIAS} decreases the distortion. It is worth noting that HD_2 is proportional to A, while HD_3 to A^2, if the input signal amplitude is small enough.

The total harmonic distortion is given by

$$THD = \sqrt{HD_2^2 + HD_3^2} \qquad \text{(A.17)}$$

neglecting the higher order components. Moreover, in this case HD_3 is negligible with respect to HD_2, thus obtaining

$$THD \simeq HD_2 \qquad \text{(A.18)}$$

A.2 Distortion Analysis of the Diode-Bridge

The distortion analysis of the diode-bridge can start from the analysis of a single diode as depicted in Fig. A.2. The diode current can be expressed as

$$I_D = I_S\, e^{V_D/V_T} \qquad \text{(A.19)}$$

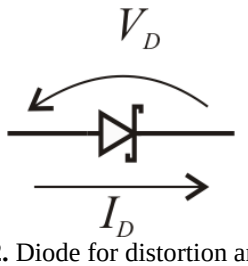

Fig. A.2. Diode for distortion analysis.

From the eq. (A.19) it follows

$$V_D = V_T \ln I_D - V_T \ln I_S \tag{A.20}$$

so it can be written

$$V_{D1} = V_T \ln I_{D1} - V_T \ln I_S \tag{A.21}$$

$$V_{D2} = V_T \ln I_{D2} - V_T \ln I_S \tag{A.22}$$

By subtracting (A.22) from (A.21), it gives

$$v_D = V_{D1} - V_{D2} = V_T \ln \frac{I_{D1}}{I_{D2}} \tag{A.23}$$

Considering the diode-bridge in dc bias condition, and in the hypothesis of symmetry, the current I_B is equally distributed in both sides of the bridge as shown in Fig. A.3.

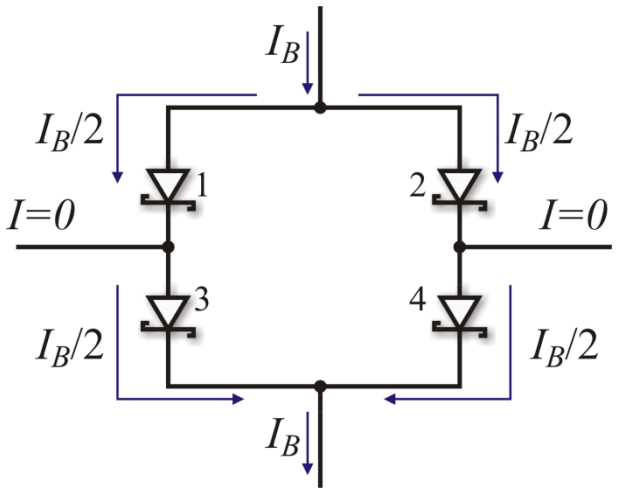

Fig. A.3. Diode-bridge in dc bias condition.

Now, considering the diode-bridge in conduction and in the hypothesis of symmetry, the current i_C is also present as shown in Fig. A.4.

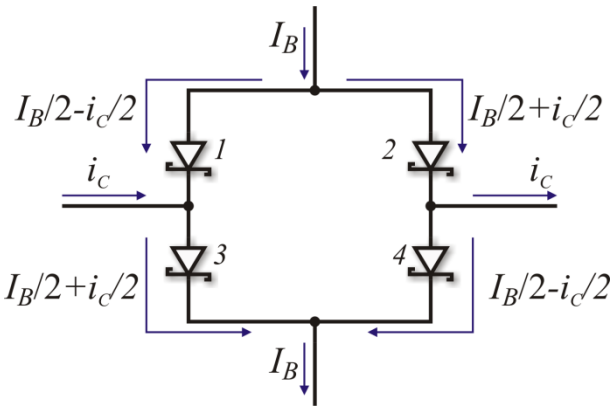

Fig. A.4. Diode bridge in conduction mode.

By taking into account the difference between the two different bridge conditions depicted in Fig. A.3 and Fig. A.4, it can be derived

$$v_{d1} = V_T \ln\left(\frac{I_B/2 - i_C/2}{I_B/2}\right)$$
$$v_{d2} = V_T \ln\left(\frac{I_B/2 + i_C/2}{I_B/2}\right) \quad \text{(A.24)}$$

The voltage drop across the bridge is

$$\Delta v_B = -v_{d1} + v_{d2} = V_T \ln\left(\frac{I_B + i_C}{I_B - i_C}\right) = V_T \ln\left(\frac{1 + i_C/I_B}{1 - i_C/I_B}\right) \quad \text{(A.25)}$$

By analyzing the circuit depicted in Fig. A.5, it can be written

$$v_{out} = v_{in} - \Delta v_B = v_{in} - V_T \ln\left(\frac{1 + i_C/I_B}{1 - i_C/I_B}\right) \quad \text{(A.26)}$$

Assuming that $i_C/I_B << 1$, and recalling the Taylor series stopped at the third order $ln((1+x)/(1-x)) \cong 2x+2/3x^3$ when $x<<1$, eq. (A.26) becomes

$$v_{out} \simeq v_{in} - V_T \ln\left(2\frac{i_C}{I_B} + \frac{2}{3}\left(\frac{i_C}{I_B}\right)^3\right) \quad \text{(A.27)}$$

while i_C is

$$i_C = C_h \frac{dv_{out}}{dt} \simeq C_h \frac{dv_{in}}{dt} \tag{A.28}$$

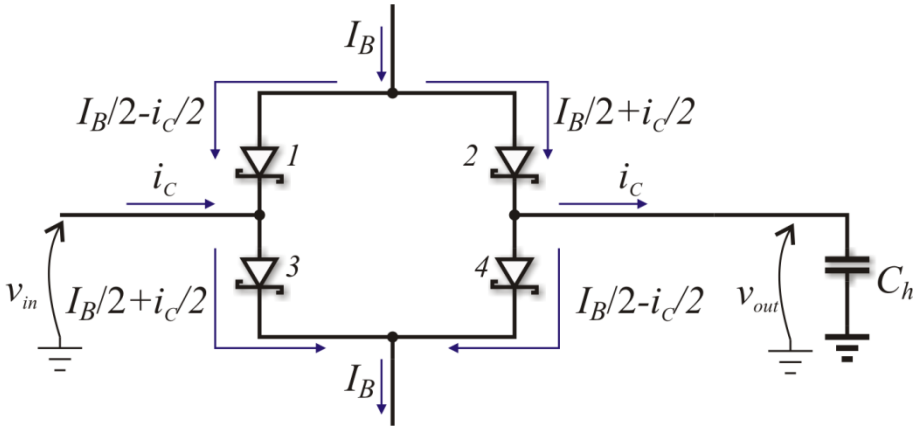

Fig. A.5. Diode bridge circuit for distortion analysis.

Assuming a sinusoidal input voltage $v_{in}(t)=A\sin(2\pi f_{in}t)$, (A.28) becomes

$$i_C = C_h A 2\pi f_{in} \cos\left(2\pi f_{in} t\right) \tag{A.29}$$

Substitution into eq. (A.27) gives

$$\begin{aligned} v_{out} &= A\sin\left(2\pi f_{in} t\right) + \\ &-V_T\left[2\frac{i_{C\max}}{I_B} + \frac{1}{2}\left(\frac{i_{C\max}}{I_B}\right)^3\right]\cos\left(2\pi f_{in} t\right) + \\ &-V_T \frac{1}{6}\left(\frac{i_{C\max}}{I_B}\right)^3 \cos\left(2\pi f_{in} t\right) \end{aligned} \tag{A.30}$$

where $i_{C\,max}=2\pi f_{in}C_hA$.

Finally, the harmonic components are:

- fundamental frequency $\Rightarrow \quad H_1 = A$
- third order $\Rightarrow \quad H_3 = \frac{1}{6}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^3 V_T$

and the harmonic distortion is

$$HD_3 = \frac{H_3}{H_1} = \frac{1}{6}\left(\frac{i_{c\max}}{I_B}\right)^3 \frac{V_T}{A} \tag{A.31}$$

It can be noted that in this case can be assumed the same considerations already stated in section A.1. Moreover, it is worth highlighting the presence of only the third harmonic component, thus the total harmonic distortion is

$$THD \simeq HD_3 \tag{A.32}$$

A.3 Distortion Analysis of Diode-Bridge with Emitter-Follower

Now, it can be derived the total harmonic distortion introduced by the emitter-follower followed by the diode-bridge as shown in Fig. A.6.

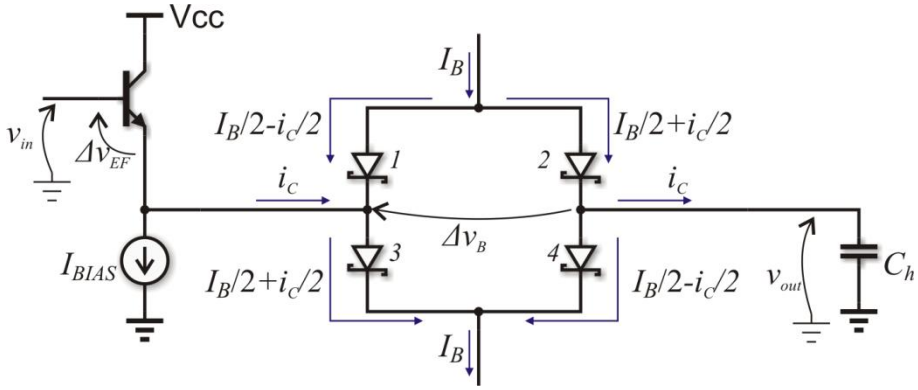

Fig. A.6. Distortion analysis of diode-bridge with emitter-follower.

The output voltage is

$$v_{out} = v_{in} - \Delta v_{EF} - \Delta v_B \tag{A.33}$$

The same current i_C flows through the emitter-follower and the diode-bridge, thus it can be written

$$\begin{cases} H_1 = A \\ H_2 = H_{2EF} + H_{2B} \\ H_3 = H_{3EF} + H_{3B} \end{cases} \tag{A.34}$$

and recalling (A.16), (A.31), the resulting harmonic distortion is

$$HD_2 = \frac{H_2}{H_1} = \frac{1}{4}\left(\frac{i_{c\max}}{I_{BIAS}}\right)^2 \frac{V_T}{A}$$
$$HD_3 = \frac{H_3}{H_1} = \frac{1}{12}\left(\frac{i_{c\max}}{I_B}\right)^3 \frac{V_T}{A}\left[1 + 2\left(\frac{I_{BIAS}}{I_B}\right)^3\right] \quad \text{(A.35)}$$

Eq. (A.35) shows that the second order component is due to the emitter-follower, while the third order component is equal to that of the emitter-follower (A.16) and a term due to the diode-bridge (A.31).