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DOTTORATO DI RICERCA IN
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ANALYSIS AND EXPERIMENTAL CHARACTERIZATION OF SAFE OPERATING AREA OF SIGE HETEROJUNCTION BIPOLAR TRANSISTOR

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Introduction

I.1. Safe Operating Area of silicon-germanium heterojunction bipolar transistors

During the past several years, silicon-germanium heterojunction bipolar transistor (SiGe HBT) technology has entered the global semiconductor electronics market and SiGe HBT technologies are being increasingly deployed for a wide variety of communications circuit applications. Progress in SiGe HBT device performance has proceeded at a truly fast pace. The introduction of SiGe BiCMOS technology allows integration of analog and digital parts, providing high integration densities and saving costs. Due to careful lateral scaling and vertical profile optimization, state-of-the-art SiGe HBTs currently demonstrate performance in excess of 350-GHz peak cut-off frequency f_T.

Nevertheless, reaching higher peak f_T and oscillation frequency f_{max} in SiGe HBTs needs higher current densities, and therefore, increased collector doping is required to suppress Kirk effect. This requirement yields to an increase of the impact ionization effect in collector-base junction and to the main trade-off of this technology, namely between breakdown voltage and cut-off frequency. For this reason designers must pay attention to the reduced upper voltage limits for the biasing of the device and carefully define the Safe Operation Area of the SiGe HBT transistors.

This thesis has been developed within the European project DOTFIVE [1], whose aim is the development of SiGe HBTs with a maximum oscillation frequency of 500 GHz. Several state-of.the-art SiGe:C bipolar transistors provided by STMicroelectronics and Infineon Technologies (partners of the project) have been used to investigate different phenomena impacting the Safe Operating Area.

I.2. Thesis contents

In Chapter 1, a brief introduction to state-of-the-art SiGe heterostructure bipolar transistors and its evolution is described. The

main junction breakdown phenomena are presented. Finally, an overview on trade-offs in the design of this kind of devices is provided.

In Chapter 2, a new 2D theoretical model for the bipolar transistor operation under reversal base current conditions is presented. In this operating condition the focusing of the current in the central area of the intrinsic base region limits the Safe Operating Area. A detailed study on the behavior of the bipolar transistor above the open-base breakdown voltage has defined a partial differential equation numerically solved by a finite element software package. The analysis has been extended to include the emitter resistance contribution and high injection effects. By means of this model, the cause of instabilities occurring in the common base output characteristics has been clarified.

In Chapter 3, the description of a complete characterization of state-of-the-art SiGe HBT devices is reported. The measurements have been totally realized in department laboratories.

In Chapter 4, a new technique for the base resistance extraction of bipolar transistor is presented. This method is the first in literature to capture the bias dependence of the base resistance of modern devices. The new extraction strategy has been applied to STM and Infineon SiGe HBT. The good accuracy of the extraction is demonstrated.

In Chapter 5, the design, realization and characterization of an *in-house* pulse generator required for isothermal characterization is described. Main features and specifications of the proposed system are highlighted. The pulser has been successfully adopted for the characterization of packaged power BJTs and MOS transistors, as well as of on-wafer SiGe:C HBTs.

Chapter 1

Silicon-germanium heterojunction bipolar transistors

The design of bipolar transistors requires trade-offs between a number of competing mechanisms. To achieve a reduced base transit time, and hence a high value of cut-off frequency, the basewidth needs to be very small. The mechanism that limits the extent that the basewidth can be reduced is punch-through of the base, which occurs when the emitter-base depletion region reaches the collector-base depletion region in the base. Thinner depletion regions can be achieved by increasing the base doping concentration, and hence one strategy for improving the performance of silicon bipolar transistors would be to increase the base doping concentration, so that narrower basewidths could be achieved without encountering punch-through. The problem with this strategy is that an increase of the base doping results in a degradation of the current gain gain. In addition, a higher base doping also results in higher base-emitter junction capacitance and base-emitter leakage, as well as to a lower base-emitter breakdown voltage, This trade-off between gain and base transit time is the main issue that limits the maximum achievable cut-off frequency of a silicon bipolar transistor. In practice, it is technologically difficult to obtain cut-off frequencies much higher than 50GHz in silicon bipolar transistors.

Silicon-Germanium has a lower bandgap than Si, and hence if a bipolar transistor could be created with SiGe in the base and Si in the emitter, much higher values of gain would be achieved. This bandgap engineering introduces a new degree of freedom in the design of bipolar transistors that makes it possible to increase the base doping and reduce the basewidth, while at the same time achieving a reasonable value of gain. In this way, much higher values of cut-off frequency can be achieved with silicon germanium heterojunction bipolar transistors (SiGe HBTs) than Si bipolar junction transistors (Si BJTs). SiGe HBTs have been produced with a cut-off frequency f_T as

high as 265 GHz and a maximum oscillation frequency f_{max} as high as 400 GHz [2].

1.1 Evolution of Silicon Bipolar technology

The bipolar transistor was invented by a team of researchers at the Bell Laboratories, USA, in 1948 [3]. The original transistor was a germanium point contact device, but in 1949 Shockley published a paper on pn junctions and junction transistors [4]. These two papers laid the foundations for the modern bipolar transistor, and made possible today's multi-million dollar microelectronics industry.
A large number of innovations and breakthroughs were required to convert the original concept into a practical technology for fabricating VLSI circuits. Among these, diffusion was an important first step, since it allowed thin bases and emitters to be fabricated by diffusing impurities from the vapour phase [5]. The use of epitaxy [6] to produce a thin single-crystal layer on top of a heavily doped buried layer was also a big step forward, and led to a substantial reduction in the collector series resistance. Faster switching speeds and improved high-frequency gain were the main consequences of this innovation.
The next stage in the evolution of bipolar technology was the development of the planar process [7], which allowed bipolar transistors and other components, such as resistors, to be fabricated simultaneously. This is clearly necessary if circuits are to be produced on a single silicon chip (i.e. integrated circuits).

In the 1970s and 1980s major innovations in silicon technology were introduced that led to considerable improvements in bipolar transistor performance. Ion implantation was used to improve the uniformity and reproducibility of the base [8] and emitter [9] regions, and also to produce devices with narrower basewidths [10]. Furthermore, the use of polysilicon emitters [11] and self-aligned processing techniques [12] revolutionized the design of silicon bipolar transistors and led to the development of the self-aligned double polysilicon bipolar transistor.

For many applications, there are many benefits to be obtained by combining bipolar and MOS transistors on a single chip [13]. The

main motivation in digital circuits for moving from CMOS to BiCMOS technology is that bipolar transistors can sink a larger current per unit device area than MOS transistors. They are therefore more effective in driving the large on-chip capacitances that are commonly encountered in digital VLSI systems [14]. BiCMOS processes also allow high-speed digital circuits to be combined on the same chip as high-performance analog circuits [15], thereby producing a technology capable of integrating a wide variety of mixed signal systems.

1.2 Evolution of Silicon-Germanium HBT technology

In the 1990s a further revolution in bipolar transistor design occurred with the emergence of SiGe Heterojunction Bipolar Transistors (HBTs). Previously, heterojunction bipolar transistors had only been available in compound semiconductor technologies, such as AlGaAs/GaAs [16], because effective heterojunction formation requires two semiconductors with similar lattice spacing, as is the situation for AlGaAs and GaAs. The lattice mismatch between Si and Ge is relatively large at 4.2%, and hence it is very difficult to form a heterojunction between Si and SiGe without the generation of misfit dislocations at the interface. However, materials research carried out in the 1980s showed that a good heterojunction could be obtained if the SiGe layer was thin and the Ge content relatively low (below 30%). In these circumstances, the SiGe layer grows under strain so that it fits perfectly onto the silicon lattice without the generation of misfit dislocations. The epitaxial growth of reproducible strained, or pseudomorphic, SiGe layers was the vital technology breakthrough that led to the emergence of the SiGe HBT [17]-[20].

The cut-off frequency f_T and the maximum frequency of oscillation f_{max} are widely used figures of merit (FoM) to characterize high-frequency bipolar technologies. SiGe HBTs have been produced with values of f_T and f_{max} of over 300 GHz, and with extremely low values of noise figure. Their main applications are in wireless

communication systems and optical fibre communication systems. SiGe HBTs are generally integrated with MOS transistors in a BiCMOS technology, so that the HBTs are used in the RF circuits and the MOS transistors in the digital CMOS circuits. BiCMOS technologies incorporating SiGe HBTs are therefore ideally suited for producing RF systems on a single chip.

Since the parameters of a bipolar transistor are correlated and a modification that improves one parameter may cause a deterioration of another one, in order to obtain a figure of merit that takes account for how well a trade-off between different parameters is performed, the product of their values is frequently considered [21]. However, for devices towards the terahertz range just the product of the collector-emitter breakdown voltage and the cut-off frequency f_T could be of interest. The trade of between the breakdown voltage and the cut-off frequency is also known as the Johnson limit [22].

1.3 Bandgap engineering

A SiGe HBT is produced by sandwiching a SiGe base between a Si collector and a Si emitter. To understand the physical behaviour of SiGe HBTs, the band diagrams of a SiGe HBT and a Si BJT are compared in Fig. 1.1. The band diagram of the SiGe HBT is indicated by the solid line and that for the Si BJT by the dashed line. In the valence band, the bandgap difference is seen as discontinuities at the emitter/base and collector/base heterojunctions, while in the conduction band it is seen as spikes. The majority of the bandgap difference between SiGe and Si occurs in the valence band, so the valence band discontinuity is much bigger than the conduction band spike. In Fig. 1.1, the size of the conduction band spike has been exaggerated for clarity, but for most practical purposes the conduction band spike is so small that it has little effect on the electrical behavior of SiGe HBTs.

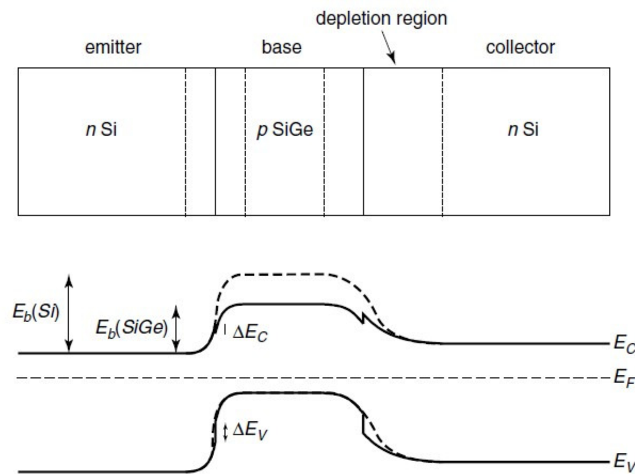

Fig. 1.1 Comparison of the band diagrams of a SiGe HBT (solid line) and a Si bipolar transistor (dashed line).

A comparison of the band diagrams in Fig. 1.1 shows that the barrier height to electron flow from emitter to base E_b (conduction band barrier) is much smaller in the SiGe HBT than the Si BJT. This means that the collector current at a given base/emitter voltage will be bigger in a SiGe HBT than in a Si BJT. The barrier height to hole flow from the base to the emitter (valence band barrier) is approximately the same in the SiGe HBT and the Si BJT, which means that the base currents of the two types of device will be approximately the same. The Gummel plots of a comparable SiGe HBT and Si BJT are shown in Fig. 1.2.

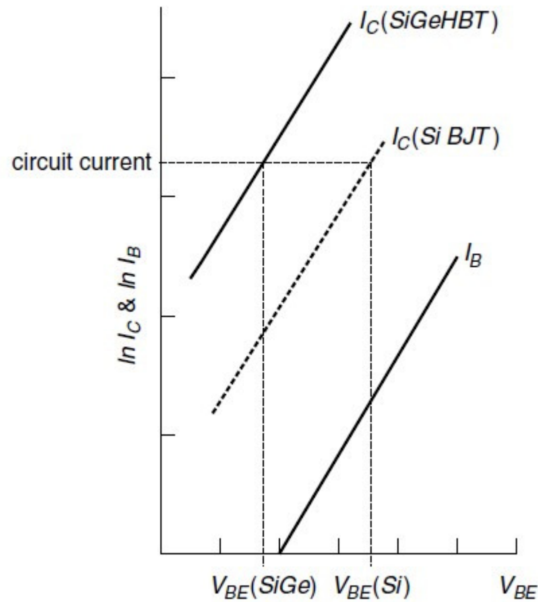

Fig. 1.2 Comparison of Gummel plots of a SiGe HBT and a Si bipolar transistor showing the lower V_{BE} for the SiGe HBT.

It can be seen that the gain of the HBT is much higher than that of the BJT and that this increased gain is due to an increased collector current. The increased collector current of a SiGe HBT can be thought of in another way. When HBTs are used in circuits, the circuits are usually designed to operate at a given current. If a SiGe HBT and Si BJT are compared at a given current, the HBT has a lower V_{BE}, as illustrated in Fig. 1.2. This lower V_{BE} in SiGe HBT circuits is very valuable, since it leads to lower power consumption.

1.4 Series resistances

In practical bipolar transistors, the silicon that is used to create the emitter, base and collector of the device has some series resistance. We would therefore expect series emitter resistance, base resistance and collector resistance to limit the current that the bipolar transistor can deliver. In a silicon bipolar transistor, the emitter is generally heavily doped, the base moderately doped and the collector lightly doped. We would therefore expect collector resistance to be very high, base resistance moderately high and emitter resistance small. Minimization of base resistance is vitally important, since it has a strong influence on the switching speed of bipolar circuits.
The influence of series resistance on the transistor currents can be understood from the circuit diagram in Fig. 1.3.

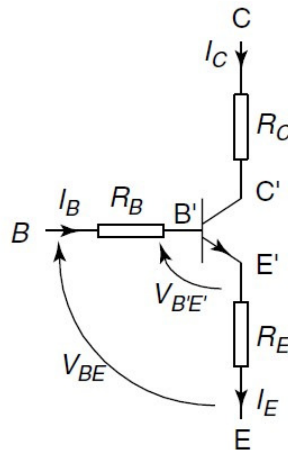

Fig. 1.3 Circuit diagram showing internal collector, base and emitter series resistances.

The external connections to the transistor are the terminals C, B and E, whereas the internal terminals of the ideal transistor that we have been discussing so far are the terminals C', B' and E'. Of course there is no way of gaining access to these internal terminals of the transistor in

practice. The relationship between the internal and external base/emitter voltages can be found using Kirchoff's voltage law:

$$
\begin{aligned}
V_{B'E'} &= V_{BE} - I_B R_B - I_E R_E = V_{BE} - I_B R_B - (\mathrm{I_C} + \mathrm{I_B}) R_E = \\
&= V_{BE} - I_B R_B - I_B R_E (1+\beta)
\end{aligned} \tag{1}
$$

The collector current is then given by:

$$
I_C = I_S \exp\left(\frac{qV_{B'E'}}{kT}\right) = I_S \exp\left(\frac{q\left(V_{BE} - I_B R_B - I_B R_E (1+\beta)\right)}{kT}\right) \tag{2}
$$

Eq. (2) shows that at low currents, the external and internal base-emitter voltages will be approximately the same, so the collector current will be given by the basic theory. However, at high currents, the voltage drop across the base and emitter resistance will cause the internal base-emitter voltage to be smaller than the external base-emitter voltage, with the result that the collector current will be smaller than predicted by the basic theory. The net result is that the collector characteristic will turn over at high currents, as illustrated in Fig. 1.4.

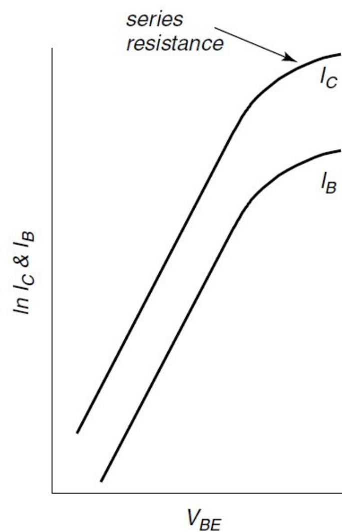

Fig. 1.4 Gummel plot showing the effect of series resistance at high current.

Similar behaviour is seen at high currents in the base characteristic. It should be noted that, although the emitter resistance is generally very small, it is multiplied by the gain of the bipolar transistor in Eq. (2). Minimization of emitter resistance, as well as base and collector resistance, is therefore important in the design of bipolar transistors.

1.5 Junction breakdown

There is a limit to the reverse voltage that can be applied to the collector of a bipolar transistor. At high reverse voltages, the junction breaks down and a high current flows between the emitter and collector. The voltage at which this occurs is known as the breakdown voltage. No transistor action is obtained above the breakdown voltage, and hence this imposes an upper limit on the supply voltage of the circuit in which the transistor is used.

Several physical mechanisms can give rise to excessive current at high collector voltages, the most important of which are punch-through, Zener breakdown and avalanche breakdown. The first two mechanisms can usually be avoided by careful transistor design, but avalanche breakdown imposes a fundamental limit on the operating voltage of bipolar transistors.

1.5.1 Punch-through

The application of a reverse bias to the collector yield to the extension of the collector-base depletion region into the base and hence modulates the basewidth. In the limit, the application of a reverse bias to the collector could causes the depletion region to extend across the whole width of the base and join up with the emitter-base depletion region. The emitter and collector are then connected together by a single depletion region. This is known as punch-through, and when it occurs a large current flows between emitter and collector. Its electrical effect is similar to junction breakdown, although, of course, the physical mechanism is completely different.

State-of-the-art silicon bipolar transistors typically have basewidths much less than 0.1μm, and consequently often operate close to the punch-through limit. Careful transistor and process design is therefore required in order to ensure that punch-through does not occur. From these considerations it is also clear that punch-through imposes a fundamental limit to the scaling of the basewidth of a bipolar transistor.

1.5.2 Zener breakdown

Zener breakdown is a tunnelling mechanism in which large numbers of carriers penetrate through the energy barrier imposed by the bandgap of the semiconductor. This is illustrated schematically in Fig. 1.5 for a reverse-biased *pn* junction.

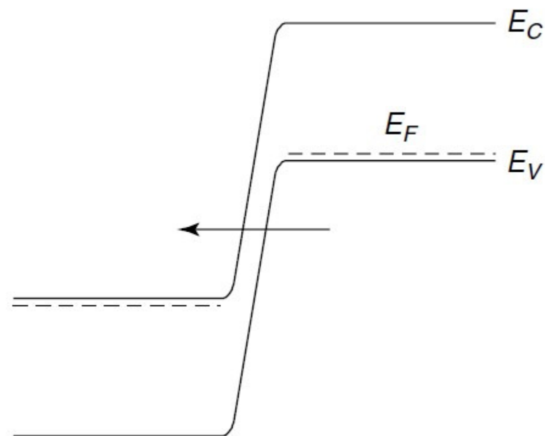

Fig. 1.5 Band diagram illustrating the mechanism of Zener breakdown.

For tunnelling to occur, the barrier presented to the tunnelling carriers must be very thin. This situation only arises at electric fields above approximately 10^6 V/cm. In general, such high electric fields only occur when both the *n* and *p* regions are very heavily doped. In practical transistors, tunnelling is therefore most likely to be seen in the reverse emitter-base diode characteristics [23], [24]. The tunnelling mechanism illustrated in Fig. 1.5 is referred to as band-to-band tunnelling, since carriers tunnel from one band directly to another.

1.5.3 Impact ionization

Impact ionization or avalanche multiplication is by far the most common breakdown mechanism in practical bipolar transistors. In a reverse-biased *pn* junction, electron–hole pairs are continually being generated by thermal agitation. At low reverse voltages this gives rise to a leakage generation current. At high reverse voltages, however, the

generated carriers gain sufficient kinetic energy between collisions with the silicon lattice for them to be able to shatter the silicon-silicon bond. This mechanism is referred to as impact ionization, and leads to the generation of an electron–hole pair. The original carrier and the electron and hole generated are then accelerated in opposite directions by the electric field, and in turn are able to produce further electron–hole pairs by impact ionization. This process, known as avalanche multiplication, rapidly leads to the generation of large numbers of carriers and hence to a large current.

For avalanche multiplication to occur, a critical electric field E_{crit} must be established across the reverse-biased junction. Since the depletion width depends upon the doping concentration it is clear that the breakdown voltage BV will also depend on the doping concentration. For a one-sided step junction the breakdown voltage is given by [25]:

$$BV = \frac{\varepsilon_0 \varepsilon_r (E_{crit})^2}{2qN_L} \tag{3}$$

where N_L is the doping concentration on the lightly doped side of the junction. If E_{crit} was a constant, Eq. (3) would indicate that the breakdown voltage was inversely proportional to the doping concentration.

In bipolar transistors, the breakdown voltage depends on the way that the bipolar transistor is connected in the circuit. In common base connection, the breakdown voltage obtained is the same as that predicted by Eq. (3), whereas in common emitter connection the breakdown voltage is considerably lower. In practice, the breakdown voltage in bipolar transistors is measured with the base open circuit, and hence in common base mode the breakdown voltage is referred to as BV_{CBO} (breakdown voltage in common base connection with the emitter open circuit). In the common emitter mode the breakdown voltage is referred to as BV_{CEO} (breakdown voltage in common emitter connection with the base open circuit).

The lower breakdown voltage in common emitter connection can be understood by considering the currents flowing in the transistor when it is connected in common emitter configuration. With reference to Fig. 1.6, if the current flowing across the emitter/base junction is I_F, a

fraction of this current is collected at the collector/base junction, given by αI_F, where α is the common base current gain, as described collector due to the leakage current of the collector/base junction I_{CBO}. In this case, we can write:

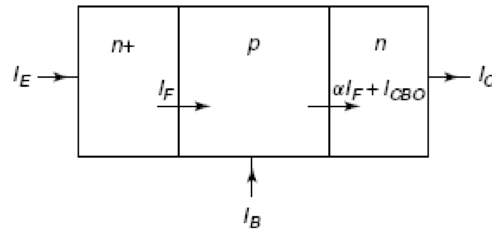

Fig. 1.6 Schematic view of current flowing across the emitter/base and collector/base junctions.

$$I_E = I_F$$
$$I_C = \alpha I_F + I_{CBO} \quad (4)$$

When the collector/base junction is breaking down, the current across the junction is multiplied by the electron–hole pairs created by avalanche breakdown. In this case, the current at the collector/base junction is multiplied by M which yields:

$$I_C = M\left(\alpha I_F + I_{CBO}\right) \quad (5)$$

being *M* is the collector current multiplication factor due to impact ionization.
If the base is open circuit, the emitter current must equal the collector current, so that Eq. (5) becomes:

$$I_C = -I_E = I_C = M\left(\alpha I_C + I_{CBO}\right) \quad (6)$$

From (6) we obtain:

$$I_{CEO} = \frac{MI_{CBO}}{1-\alpha M} \quad (7)$$

where I_{CEO} is the current flowing between emitter and collector when the base is open circuit. Eq. (7) shows that the collector/emitter current begins to increase very rapidly when αM approaches unity. In contrast, in the common base mode the collector/base leakage current only begins to increase when αM approaches infinity. This explains why the breakdown voltage in the common emitter mode BV_{CEO} is lower than that in the common base mode BV_{CBO}.

1.6 Figures of Merit

The cut-off frequency f_T and the maximum frequency of oscillation f_{max} are widely used figures of merit to characterize high-frequency bipolar technologies.
The cut-off frequency f_T represents the frequency at which the gain of a bipolar transistor drops to unity. Beyond this frequency the gain of the transistor is less than unity, so it is no longer useful as either an amplifying or a switching device. In practice, it becomes increasingly difficult to design circuits as the required circuit operating frequency approaches the cut-off frequency of the transistor. More precisely, the cut-off frequency of a bipolar transistor is defined as the frequency at which the extrapolated common emitter, small-signal current gain drops to unity under conditions of a short-circuit load.

Another important high-frequency parameter for a bipolar transistor is the maximum oscillation frequency f_{max}. This is defined as the frequency at which the power gain drops to unity. The expression of f_{max} as function of f_T is:

$$f_{\max} = \sqrt{\frac{f_T}{8\pi C_{JC} R_B}} \quad (8)$$

1.7 Device design trade-offs in a SiGe HBT

The SiGe base gives new degrees of freedom for the design of SiGe HBTs and allows much higher values of f_T to be achieved than in conventional silicon BJTs. A very high gain is not very useful for most circuit applications, so the approach taken is to trade-off the increased gain of a SiGe HBT for increased base doping. This allows the basewidth to be dramatically reduced without encountering problems of punchthrough. To maximize the value of f_T, the boron profile in the SiGe base should be made as thin as possible. To maximize the value of f_{max}, the base resistance and collector-base capacitance also have to be minimized. The extrinsic components of base resistance and collector-base capacitance can be minimized by using self-aligned fabrication techniques. However, there remains a trade-off between basewidth and intrinsic base resistance. To minimize the base resistance, and hence maximize the value of f_{max}, the doping in the base needs to be as high as possible. To simultaneously maximize the values of f_T and f_{max}, it is clear that the boron profile in the base should be as thin and highly doped as possible.

When combining a highly doped base with a highly doped emitter, it is necessary to consider emitter-base tunnelling leakage, which occurs when the doping concentrations on both sides of a *pn* junction are very high. In this situation the depletion region becomes sufficiently narrow for tunnelling to occur, which results in excess leakage current in reverse bias and non-ideal base characteristics in forward bias. Research has shown that tunnelling leakage occurs when the doping concentration on the low doped side of the junction is greater than about 5×10^{18} cm^{-3} [26]. One method of producing an HBT with a very heavily doped base is therefore to reduce the doping in the emitter to a level at or below 5×10^{18} cm^{-3} [27]. This low doped emitter allows a very heavily doped base to be produced without encountering any problems with emitter/base tunnelling leakage. The low doped emitter must be relatively thin to avoid unwanted stored charge and an increase in the emitter delay. A second approach is to tailor the base profile so that the base doping adjacent to the emitter-base depletion region is less than 5×10^{18} cm^{-3}, while that deeper in

the base is much higher. The aim here is to give a wide enough emitter-base depletion region to avoid tunnelling, while at the same time minimizing the overall basewidth.

Chapter 2

Theoretical analysis and modeling of bipolar transistor operation under reversal base current conditions

The Safe Operating Area (SOA) of bipolar transistor is dependent on the driving conditions at the input port [28]. It is well known that the widely cited open-base breakdown voltage BV_{CEO}, which limits the operation under forced-I_B conditions, does not fully describe the operating limits in practical cases, since the base is not commonly driven by a large impedance [29]. Thus, the device can be safely biased above BV_{CEO} when driven under forced-V_{BE} or forced-I_E conditions. However, the analysis of the operating limits under forced-V_{BE}/I_E conditions is made complex by the base current reversal which, combined to the ohmic drop across the base region, yields a current focusing in the center of the base [29]. This current crowding effect is thought to be responsible of anomalous current discontinuities observed in common base (CB) output characteristics [28]-[31], as can be seen in Fig. 2.1. In this section, a theoretical model for the current crowding effect occurring under base current reversal conditions is described. Using this model an analysis of the operating limits related to impact-ionization under forced-V_{BE} and forced-I_E conditions is realized, and an elucidation on the physical mechanisms causing the discontinuities observed in CB characteristics is reported. Simple equations are derived for defining SOA boundaries. In addition, a simple model for the base resistance which is suitable for being incorporated into compact models to properly describe device operation above BV_{CEO} is presented.

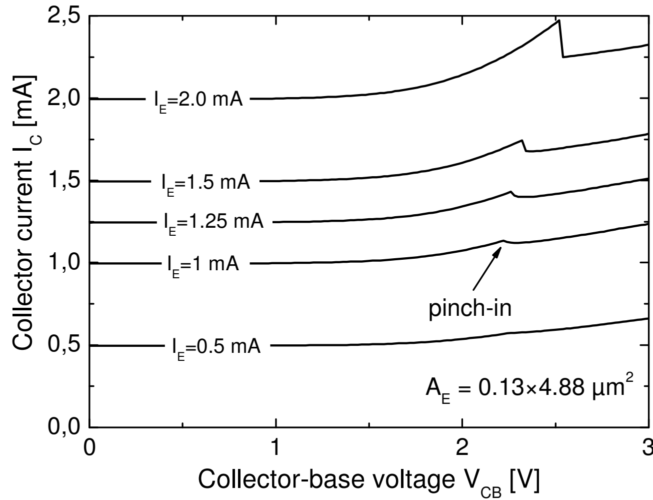

Fig. 2.1 Experimental common-base output characteristics obtained in our laboratories for an STM device.

2.1 2D theoretical model

In this analysis the intrinsic base region is considered (Fig. 2.2), where the ohmic drop caused by the two-dimensional hole flow in the (y,z) plane results in a nonuniform potential distribution [32], [33]. Note that for this problem we cannot use standard 2D device simulation codes which analyze the device in the (x,y) plane.

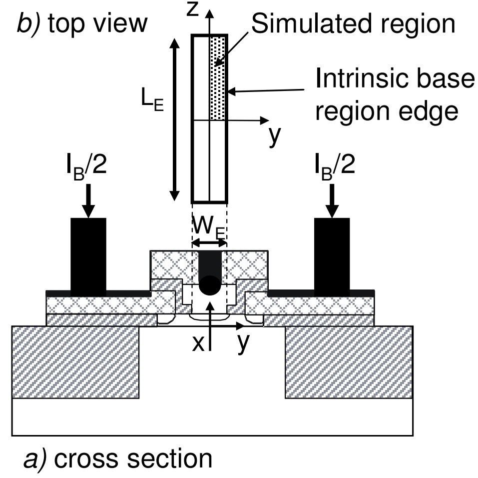

Fig. 2.2 a) Cross section of a double-base contact SiGe HBT; b) Top view of the intrinsic base region located underneath the emitter region.

The continuity equation in the neutral base reads

$$\frac{\partial J_{px}}{\partial x} + \frac{\partial J_{py}}{\partial y} + \frac{\partial J_{pz}}{\partial z} = -qU \tag{1}$$

where all symbols have their customary meaning. Denoting as x_{bc} (x_{be}) the boundary of the neutral base region with the base-collector (base-emitter) space charge region, integrating with respect to x we find

$$\int_{x_{bc}}^{x_{be}} \left(\frac{\partial J_{py}}{\partial y} + \frac{\partial J_{pz}}{\partial z} \right) dx + J_{px}(x_{be}) - J_{px}(x_{bc}) = -\int_{x_{bc}}^{x_{be}} qU dx = -J_R \tag{2}$$

where J_R represents the recombination current density in the neutral base and $J_{px}(x_{be})$ the hole current density injected into the emitter. Introducing the hole current per unit length

$$\mathbf{I}_p = (I_{py}, I_{pz}) = \left(\int_{x_{bc}}^{x_{be}} J_{py} dx, \int_{x_{bc}}^{x_{be}} J_{pz} dx \right) \tag{3}$$

equation (2) may be written in the form

$$\nabla \cdot \mathbf{I}_p = \frac{\partial I_{py}}{\partial y} + \frac{\partial I_{pz}}{\partial z} = -J_{px}(x_{be}, y, z) - J_R + J_{px}(x_{bc}, y, z) = \\ = -\frac{J_n(x,y)}{\beta} + (M-1) J_n(x,y) = J_n\left[(M-1) - \frac{1}{\beta}\right] \tag{4}$$

where ∇ represents the *del* (nabla) operator in the (y,z) plane, $J_n(y,z)$ is the electron current density in the neutral base (assumed positive), and β is the common-emitter current gain. Note that J_n/β represents the hole current density due to base recombination and hole injection into the emitter, while $-(M-1)J_n$ is the hole current density generated by impact ionization in the base-collector space charge region (flowing into the neutral base). In the case of negligible impact ionization (M=1) Eq. (4) reduces to the formulation of [32].
The electron current density is expressed as

$$J_n(y,z) = J_S \exp\frac{\varphi_{p,B}(y,z) - \varphi_{p,E}}{V_T} = J_S \exp\frac{V_{BE}(y,z)}{V_T} \tag{5}$$

where $\varphi_{p,E}$ and $\varphi_{p,B}$ are the hole quasi-Fermi potentials in the emitter and in the base, respectively. Since the emitter is equi-potential, we can set $\varphi_{p,E} = 0$. Thus, at the base edge we have $\varphi_{p,B} = V_{BE}$. In addition, we have

$$\mathbf{I}_p = (I_{py}, I_{pz}) = -\int_{x_{be}}^{x_{bc}} \sigma_p(x) \nabla\varphi_{p,B} dx \simeq \\ \simeq -\nabla\varphi_{p,B} \int_{x_{be}}^{x_{bc}} \sigma_p(x) dx = -\frac{1}{R_{sh}} \nabla\varphi_{p,B} \tag{6}$$

where the hole quasi-Fermi level is assumed to be nearly constant along the vertical (x) axis, and R_{sh} represents the intrinsic base sheet resistance.
Combining (4) and (6) the following PDE is obtained

$$\nabla^2\varphi_p = -R_{sh}\left[(M-1) - \frac{1}{\beta}\right] J_n = R_{sh} J_S \frac{M}{b} \exp\frac{\varphi_p}{V_T} \tag{7}$$

where:

$$\frac{1}{b} = \frac{\frac{1}{\beta} + 1 - M}{M} = \frac{\frac{1}{\alpha} - M}{M} = \frac{1 - \alpha M}{\alpha M} \tag{8}$$

In deriving (7) a position-independent sheet resistance is assumed. As a boundary condition for (7), at the edge of the intrinsic base region (see Fig. 2.2) the hole quasi-Fermi potential can be taken as constant, and equal to the applied base-emitter voltage : $\varphi_p|_{edge} = V_{BE}$. The hole quasi-Fermi potential φ_p is a positive quantity, decreasing from the intrinsic base edge ($\varphi_p|_{edge} = V_{BE}$) to the center ($\varphi_p < V_{BE}$), if $I_B>0$. Note that $I_{pz}<0$ and $I_{py}<0$ if the reference system is centred in the middle of the emitter finger (and b>0). In this case the hole flux is entering the emitter region, and the direction is thus opposite to that of the y- and z-axis.
For a double-base contact device (Fig. 2.2), due to symmetry, we can analyse a domain $0 \le y \le W_E / 2, 0 \le z \le L_E / 2$, given by one fourth of the intrinsic base region (see Fig. 2.2,a), where the symmetry conditions

$$\left.\frac{\partial \varphi_p}{\partial y}\right|_{z=0} = \left.\frac{\partial \varphi_p}{\partial z}\right|_{y=0} = 0 \tag{9}$$

are specified. For this reduced domain the currents I_b, I_c, I_e will be one fourth of the currents flowing in the real structure: $I_b=I_B/4$, $I_e=I_E/4$, $I_c=I_C/4$.

Integrating (4) over the reduced domain we obtain:

$$\begin{aligned} -I_b &= -\frac{I_B}{4} = \int_{boundary} \mathbf{I}_p \cdot d\mathbf{n} = \left[(M-1) - \frac{1}{\beta}\right] \int_0^{\frac{W_E}{2}} \int_0^{\frac{L_E}{2}} J_n dydz \\ &= \left[(M-1) - \frac{1}{\beta}\right] J_S \int_0^{\frac{W_E}{2}} \int_0^{\frac{L_E}{2}} e^{\frac{\varphi_p}{V_T}} dydz \end{aligned} \tag{10}$$

which clearly represents a balance equation for the hole current in the base. Note that the collector current is given by:

$$I_C = 4M\int_0^{W_E/2}\int_0^{L_E/2} J_n dy dz = \frac{M}{\frac{1}{\beta} - (M-1)} I_B = bI_B \tag{11}$$

Introducing the normalized potential u=(φ_p – V_{BE})/V_T we have:

$$\begin{aligned} \nabla^2 u &= \frac{R_{sh}}{V_T} \frac{MJ_S \exp\frac{V_{BE}}{V_T}}{b} \exp(u) \\ \mathbf{I}_p &= -\frac{\nabla \varphi_{p,B}}{R_{sh}} = -\frac{V_T}{R_{sh}} \nabla u \end{aligned} \tag{12}$$

The boundary condition φ_p =V_{BE} is replaced by $u|_{edge}$=0. If we define the normalized space variables η=y/L and ζ=z/L, where is a suitable normalization length, the above formulation is rewritten as:

$$\nabla^2 u = \frac{\partial^2 u}{\partial \eta^2} + \frac{\partial^2 u}{\partial \zeta^2} = \frac{R_{sh}}{V_T}\left[\frac{L^2 MJ_S \exp\frac{V_{BE}}{V_T}}{b}\right]\exp(u) = \theta \exp(u) \tag{13}$$

where the ∇ operator is referred to the (η, ζ) variables. The parameter θ is defined as:

$$\theta = \frac{R_{sh}A_E J_S \exp\frac{V_{BE}}{V_T}}{V_T}\frac{M}{b} = -\frac{R_{sh}A_E J_S \exp\frac{V_{BE}}{V_T}}{V_T \alpha}(\alpha M - 1) \tag{14}$$

where A_E=$W_E L_E$ is the emitter area. Assuming $L = \sqrt{W_E L_E}$ the normalized dimensions of the intrinsic base are: $w_E = W_E / L = \sqrt{W_E / L_E} = 1/\sqrt{a}$, $l_E = L_E / L = \sqrt{a}$, where a=L_E/W_E denotes the emitter window aspect ratio. Note that θ embeds geometry (W_E, L_E), electrical (R_{sh}, J_S, α), and bias (V_{BE}, M(V_{CB})) parameters.
The current density is expressed in terms of normalized potential as

$$\mathbf{I}_p = -\frac{V_T}{R_{sh}L}\nabla u \tag{15}$$

With our approach the boundary value problem given by (13) was solved by the finite element software package COMSOL [34].

2.2 Numerical simulations

The PDE defined in (13) was numerically solved in a specific domain drawn in COMSOL. The first step was the analysys of the intrinsic base region (see Fig. 2.2). The domain of interest and the boundary conditions are highlighted in Fig. 2.3.

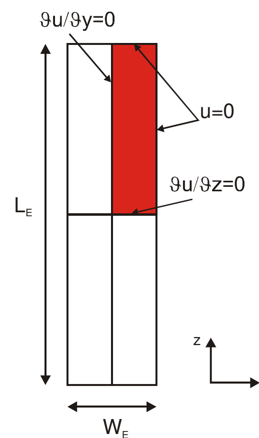

Fig. 2.3 Top view of the intrinsic base region and applied boundary conditions.

The numerical solution of the (13) is the normalized potential u(z,y). In Fig. 2.4 a biasing point where the impact ionization is not enough to invert the base current is shown.

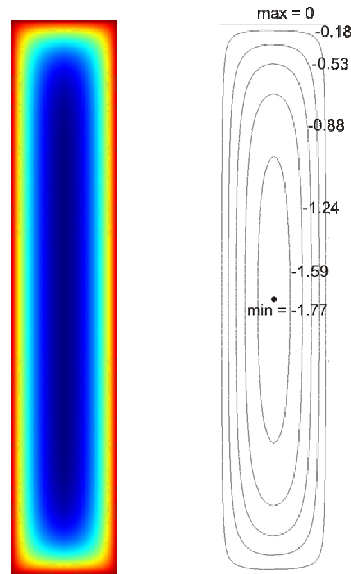

Fig. 2.4 Numerical results obtained for the normalized potential u(z,y) in the instrinsic base region for an I_B>0 case.

In this case $(M-1)J_n < J_n/\beta$ and the base current is again entering in the base terminal. The focusing of the current is at the peripheral area of the intrinsic base [see Eq. (10)].

For increasing V_{CB} (beyond BV_{CEO}) the injection of the carriers generated by impact ionization reverses the base current sign yielding a current crowding effect (pinch-in). Due to the distributed ohmic drop across the intrinsic base region, the electron current focuses in the device center as can be seen by the numerical results shown in Fig. 2.5.

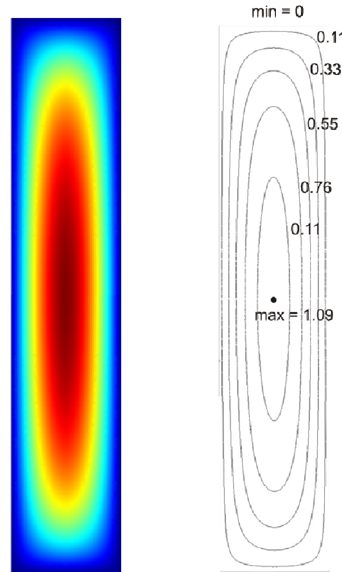

Fig. 2.5 Numerical results obtained for the normalized potential u(z,y) in the instrinsic base region for an I_B<0 case.

Note that the focusing of the current in the central area of the intrinsic base region increases the base resistance because the path of the carrier to reach the base terminal increases. For this reason the very important parameter R_B (it contributes to degrade the device performance) is not fixed but dependent on the biasing, i.e. $R_B=R_B(V_{CB})$.
As shown in Fig. 2.4-2.5 the results of our numerical approach is the normalized potenzial inside the domain of interest. In order to obtain the terminal currents a post-processing operation is required.

2.2.1 Calculation of the currents

The base current is calculated as:

$$I_B = 4\left[\frac{1}{\beta} - (M-1)\right] J_S \int_0^{W_E/2}\int_0^{L_E/2} \exp\frac{\varphi_p}{V_T}\, dydz = \\ = 4\frac{A_E M J_S \exp\frac{V_{BE}}{V_T}}{b}\int_0^{\frac{w_E}{2}}\int_0^{\frac{l_E}{2}} \mathrm{e}^u\, d\eta d\zeta = 4\frac{V_T\theta}{R_{sh}}\int_0^{\frac{1}{2\sqrt{a}}}\int_0^{\frac{\sqrt{a}}{2}} \mathrm{e}^u\, d\eta d\zeta \tag{6}$$

where the factor 4 accounts for the fact that, due to symmetry, the integral is calculated over one fourth of the base. As shown by (16), base current reversal ($I_B<0$) occurs for $M\alpha>1$ (i.e. $V_{CE}>BV_{CEO}$).
Defining a normalized base current as $i_B= I_B R_{sh}/V_T$, we obtain:

$$i_B = \frac{I_B R_{sh}}{V_T} = 4\theta\int_0^{\frac{w_E}{2}}\int_0^{\frac{l_E}{2}} \mathrm{e}^u\, d\eta d\zeta \tag{17}$$

which completes the formulation of the problem in normalized form. The input parameters to be specified are θ and $a=L_E/W_E$. The output parameters are the normalized potential u(η,ζ), and the normalized current i_B.
The collector current is given by:

$$I_C = 4MJ_S\int_0^{\frac{W_E}{2}}\int_0^{\frac{L_E}{2}} \exp\frac{\varphi_p}{V_T}\, dydz = 4MA_E J_S\, \mathrm{e}^{\frac{V_{BE}}{V_T}}\int_0^{\frac{w_E}{2}}\int_0^{\frac{l_E}{2}} \mathrm{e}^u\, d\eta d\zeta \tag{18}$$

or in normalized form:

$$i_C = \frac{I_C R_{sh}}{V_T} = \frac{R_{sh} M A_E J_S\, \mathrm{e}^{\frac{V_{BE}}{V_T}}}{V_T} 4\int_0^{\frac{w_E}{2}}\int_0^{\frac{l_E}{2}} \mathrm{e}^u\, d\eta d\zeta = \frac{R_{sh} M A_E J_S\, \mathrm{e}^{\frac{V_{BE}}{V_T}}}{V_T}\frac{i_B}{\theta} = \\ = \frac{R_{sh} M A_E J_S\, \mathrm{e}^{\frac{V_{BE}}{V_T}}}{V_T}\frac{bV_T}{R_{sh} M A_E J_S\, \mathrm{e}^{\frac{V_{BE}}{V_T}}} i_B = b i_B = \frac{\alpha M}{1-\alpha M} i_B \tag{19}$$

Finally, the normalized emitter current is expressed as:

$$
\begin{aligned}
i_E &= i_C + i_B = \frac{\alpha M}{1-\alpha M} i_B + i_B = \frac{1}{1-\alpha M} i_B = \\
&= 4 \frac{R_{sh} A_E J_S \, e^{\frac{V_{BE}}{V_T}}}{V_T \alpha} \int_0^{\frac{w_E}{2}} \int_0^{\frac{l_E}{2}} e^u \, d\eta d\zeta
\end{aligned} \tag{20}
$$

The collector current can be also expressed in terms of i_e as:

$$
i_C = 4 \frac{R_{sh} M A_E J_S \, e^{\frac{V_{BE}}{V_T}}}{V_T} \int_0^{\frac{w_E}{2}} \int_0^{\frac{l_E}{2}} e^u \, d\eta d\zeta = \alpha M i_E \tag{21}
$$

It is interesting to note that for small values of θ we have |u|<<1 and thus

$$
\begin{aligned}
i_B &= 4\theta \int_0^{\frac{w_E}{2}} \int_0^{\frac{l_E}{2}} e^u \, d\eta d\zeta \simeq 4\theta \frac{w_E}{2} \frac{l_E}{2} = \theta \Rightarrow \\
I_B &= \frac{V_T i_B}{R_{sh}} \simeq \frac{V_T \theta}{R_{sh}} = \frac{1-\alpha M}{\alpha} A_E J_S \exp \frac{V_{BE}}{V_T} \\
I_C &= \frac{V_T i_C}{R_{sh}} = \frac{V_T i_B}{R_{sh}} \frac{\alpha M}{1-\alpha M} \simeq M A_E J_S \exp \frac{V_{BE}}{V_T}
\end{aligned} \tag{22}
$$

Under forced-I_B conditions the governing equation reads

$$
\nabla^2 u = \theta \, e^u = i_B \frac{e^u}{4 \int_0^{\frac{w_E}{2}} \int_0^{\frac{l_E}{2}} e^u \, d\eta d\zeta} \tag{23}
$$

Under forced-I_E conditions the governing equation reads

$$
\nabla^2 u = i_B \frac{e^u}{4 \int_0^{\frac{w_E}{2}} \int_0^{\frac{l_E}{2}} e^u \, d\eta d\zeta} = -i_E \left(\alpha M - 1 \right) \frac{e^u}{4 \int_0^{\frac{w_E}{2}} \int_0^{\frac{l_E}{2}} e^u \, d\eta d\zeta} \tag{24}
$$

2.3 Analysis

For an assigned value of the normalized base current i_B, the normalized potential distribution $u(\eta,\zeta)$ is determined from the numerical solution of (23), while the parameter θ can be evaluated from (17). It is therefore possible to plot the normalized base current i_b as function of parameter θ (see Fig. 2.6). In this analysis negative values of the base current are considered. This implies that the parameter θ must be also negative. From (14) we see that θ is negative only if $\alpha M>1$, i.e. the collector voltage must be higher than the open base breakdown voltage BV_{CEO}. Since both θ and i_B are negative, the magnitude of both quantities is displayed in this figure. It can be noted that this plot can be regarded as a “universal” result, since it does not refer to a specific device or bias condition. Device and bias information are embedded in the normalized parameters i_B and θ. In particular, θ includes either the dependence on both the base-emitter voltage (see (14)) and the collector voltage (through the multiplication factor $M(V_{CB})$). Therefore, Fig. 2.6 can be used to describe the dependence of the base current on either V_{BE} (for a fixed collector voltage), or V_{CB} (for a fixed V_{BE}). In fact, the dependence of the base current on the collector voltage for a specific device can be straightforwardly derived from the results presented here if a $M(V_{CB})$ model is specified. The results shown here do not refer to any specific $M(V_{CB})$ model.

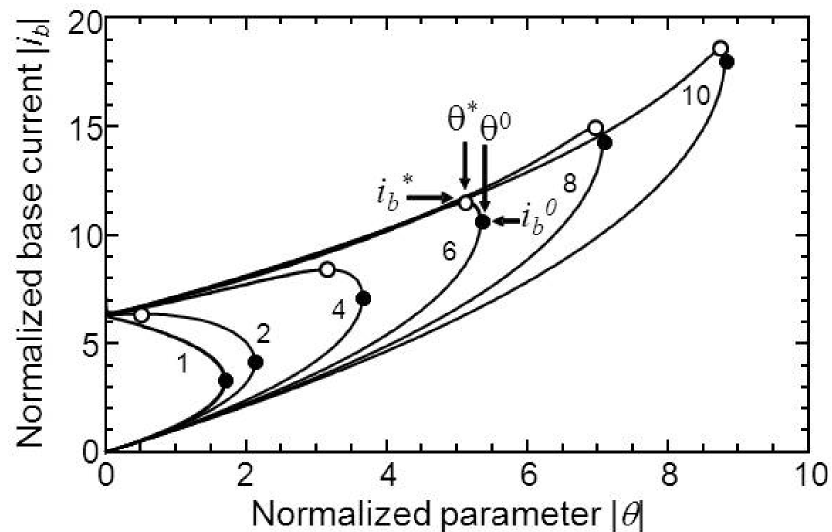

Fig. 2.6 Normalized base current $|i_b|$ as function of parameter $|\theta|$ for different values of the aspect ratio a=L_E/W_E.

Considering for instance the curve for a=6, it can be seen that the base current increases monotonically with increasing $|\theta|$ until a first critical current i_B^0 is reached. At this point a snapback behaviour is observed, that is, the i_B vs θ plot "turns back". Beyond the snapback point (θ^0,i_B^0), $|i_B|$ increases when decreasing $|\theta|$. Eventually, a second critical current i_B^* is reached, where $|i_B|$ reaches a maximum ($di_B/d\theta=0$). For values of $|\theta|$ lower than the critical value $|\theta^*|$, $|i_B|$ decreases with respect to the maximum value $|i_B^*|$. This region, however, is not of practical interest, as it will be shown below. The existence of the second critical point i_B^* is observed only for aspect ratios higher than about 1.8. Indeed, Fig. 2.6 shows that for a=1, after the snapback point (θ^0,i_B^0) is reached, the base current turns back and increases monotonically with decreasing $|\theta|$, without passing through a point of maximum.

The critical points (θ^0,i_B^0) and (θ^*,i_B^*) in the (θ,i_B) plane represent different limitations to the safe operating area of bipolar transistors. To clarify the significance of these critical points, let us examine the output characteristics under forced-V_{BE} conditions. Fig. 2.7 shows the

normalized collector current as a function of (αM-1) for different values of the base emitter voltage, and an aspect ratio a=6. Since the multiplication factor is dependent on the collector voltage, this plot is representative of the I_C-V_{CE} characteristics under forced-V_{BE} conditions. In Fig. 2.7 values of the multiplication factor αM>1 are considered, which correspond to values of the collector voltage V_{CE} above BV_{CEO}. This plot can be easily constructed from the i_b vs θ plot shown in Fig. 2.6 as follows. If we increase (αM-1) while keeping V_{BE} constant, it means that parameter |θ| is increased (see (14)). For a given value of θ, the normalized base current is obtained from the numerical formulation above (see (22) and Fig. 2.6 above). Once $i_B(\theta)$ is calculated, the collector current is obtained from (19) for the specified value of αM.

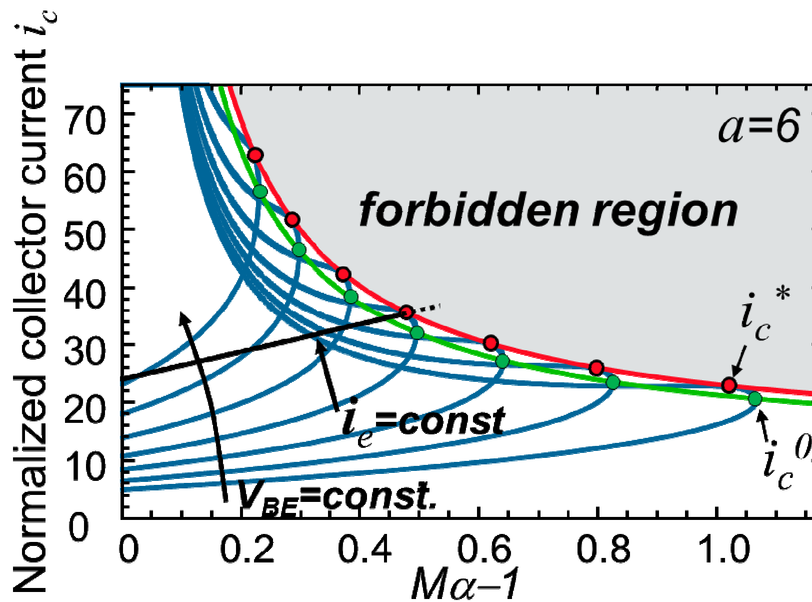

Fig. 2.7 Normalized collector current i_c vs. (αM-1) for different values of the base emitter voltage. An aspect ratio a=6 is assumed. Also shown are the critical i_c^0 locus (green line) and i_c^* locus (red line).

To generate the characteristics the following procedure is used:

1) Assume a fixed value for V_{BE}. This corresponds to a given value of

$$\theta_0 = \frac{R_{sh} A_E J_S \exp \frac{V_{BE}}{V_T}}{V_T \alpha} \tag{31}$$

2) For the numerical solution above, a vector of solutions (i_B,θ) is generated. For a given value of θ_0, we can vary θ by varying M. Therefore, for each value of (i_B, θ) we find the corresponding values of M and i_C from

$$\begin{aligned} \theta &= -\theta_0 (\alpha M - 1) \\ i_C &= \frac{\alpha M}{\alpha M - 1}(-i_B) = \frac{(\alpha M - 1) + 1}{\alpha M - 1}(-i_B) \end{aligned} \tag{32}$$

Let us examine the characteristic corresponding to the lowest value of V_{BE}. Starting from αM-1=0 (i.e. $V_{CE}=BV_{CEO}$) the collector current increases with increasing M, until a snapback point i_C^0 is reached (i.e. i_B^0 in the i_B vs. αM-1 plot). This critical point corresponds to the critical point (i_B^0, θ^0) where the snapback occurs in the (i_B, θ) plane (Fig. 2.6). The "snapback locus" obtained from the collection of all snapback points in the output plane (filled dots) represents the limit of the safe operating area limit under forced-V_{BE} conditions, and is represented by the green curve in Fig. 2.7. This critical locus can be easily traced by first determining the critical base current i_B^0. For *a*=6 we obtain i_B^0=-10.6 (see. Fig. 2.6). Recalling (19), the critical snapback locus can be traced in the output plane using

$$i_C^0 = -\frac{\alpha M}{\alpha M - 1} i_B^0 \tag{33}$$

Once the snapback point is reached , the multiplication factor (i.e. the collector voltage) must decrease, and the output characteristic passes through a critical current i_C^* indicated by an open dot in Fig. 2.7. This current corresponds to the current i_B^* in the (i_B, θ) plane (see Fig. 2.6). While the meaning of i_C^0 is clear from Fig. 2.7, the role of i_C^* is less straightforward. To understand the significance of the critical current i_C^*, we can trace the output characteristics for other values of V_{BE},

locate the critical current i_C^* for each characteristic (open dots), and join all critical points i_C^* (red line in Fig. 2.7). It can be recognized that the critical i_C^* locus represents a sort of "envelope" of the output characteristics, so that no stable operating point in seen to exist outside this critical locus. More specifically, denoting as M^* the multiplication factor corresponding to a critical current i_C^* (see Fig. 2.7), it is not possible to reach collector currents higher than i_C^* for $M=M^*$, regardless the value of V_{BE} . This "forbidden region" is indicated by the shadowed area in Fig. 2.7. Therefore, while the snapback i_C^0 locus represents the operation limit under forced V_{BE} conditions, the i_C^* locus represents the maximum operation boundary under any condition. In particular, it represents the SOA boundary under forced-I_E condition. This can be recognized by examining the output characteristic for a constant I_E shown in Fig. 2.7. As M increases, the collector current increases and the I_E=const. characteristic intersects different V_{BE}=const. characteristics, indicating that V_{BE} has to decrease in order to keep I_E=const. However, no possible operation is allowed beyond the critical i_C^* point, as there are no "available" base-emitter voltages. As a consequence, the dotted portion of the i_E=const. characteristic cannot be reached. Similarly to (33), the i_C^* locus can be traced in the output plane from

$$i_C^* = -\frac{\alpha M}{\alpha M - 1} i_B^* \tag{34}$$

where the critical current i_B^* depends only on the aspect ratio. This critical locus is represented by the red curve in Fig. 2.7. For the case considered in Fig. 2.7 (a=6), i_B^*=-11.5 (see Fig. 2.6).

The same conclusion can be drawn from the analysis of the i_B characteristic in Fig. 2.7. For a given emitter current, the base current is calculated from $i_B=-(\alpha M-1)i_E$. Therefore, $|i_B|$ must increase as αM is increased (see the straight line in Fig. 2.7). However, as the critical current i_B^* is reached, it not possible to further increase $|i_B|$.

2.3.1 Analytical model for the critical currents

From the above discussion it is clear that it is important to calculate the critical points for a given device. As apparent from Fig. 2.6, all critical parameters i_B^0, θ^0, i_B^*, θ^* increase monotonically with the aspect ratio *a*. In addition, numerical results indicate that, for a large aspect ratio (*a*>10), $i_B^0 \cong i_B^*$ and $\theta^0 \cong \theta^*$ become proportional to *a*. For this reason, it is convenient to plot the critical parameters divided by the aspect ratio *a*, as shown in Fig. 2.8.

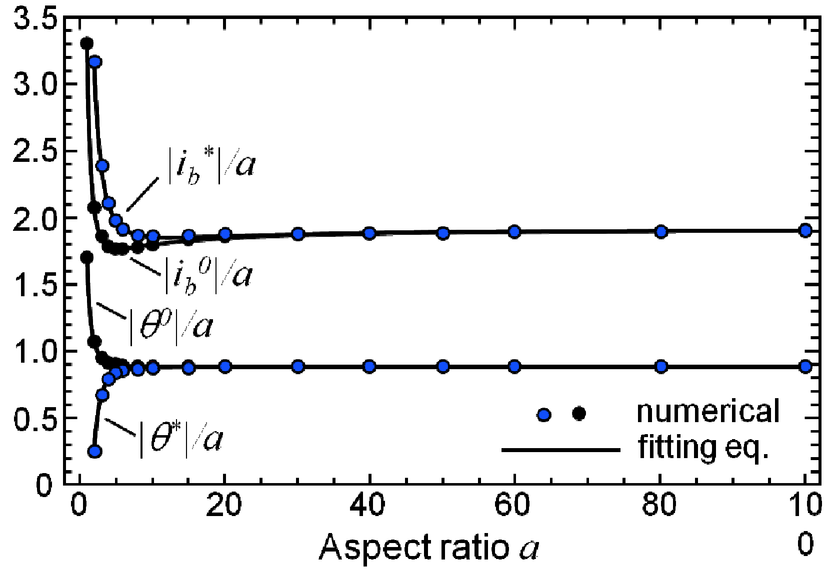

Fig. 2.8 Normalized critical parameters (divided by aspect ratio *a*) vs *a*. Dots: numerical results; solid lines: Eq. (35).

The symbols in Fig. 2.8 denote numerical results. These results can be fitted by

$$\begin{aligned} \theta^0(a) &= 4aF(a) \\ i_B^0(a) &= 4(aF(a)-2) \\ \theta^*(a) &= \theta^0(a)\,/\,F(a) \\ i_B^*(a) &= i_b^0(a)F(a) \end{aligned} \quad (35)$$

where F(a) denotes a fitting function, which has the form

$$F(a) = \frac{b_1 + \left[b_2 \left(a^{b_4} - b_3^{\,b_4} \right) + b_5 \right]}{b_1 \left[b_2 \left(a^{b_4} - b_3^{\,b_4} \right) + b_5 \right]} \tag{36}$$

The constants used to fit the various quantities in (35) are summarized in the Tab. 2.1.

	b_1	b_2	b_3	b_4	b_5
$\lvert\theta^0\rvert$	1.137	0.383	1	2.56	1.21
$\lvert i_b^{\,0}\rvert$	0.519	0.243	1	1.75	0.296
$\lvert\theta^*\rvert$	1	0.102	2	3.05	0.311
$\lvert i_b^*\rvert$	1	0.317	2	1.99	1.89
n	9	2.56	1	2.02	0

Tab. 2.1 Fitting parameters used in Eq. (35).

The results obtained using these fitting functions show an error less than 1%.

2.3.2 Analysis including the effect of a distributed emitter resistance

The analysis shown until now refers only to the intrinsic base region. An important influence on the onset of the pinch-in phenomena is due to the emitter resistance that represents a negative feedback effect. Indeed, if a focusing of the current in a particular area of the junction occurs, a large drop across the emitter resistance with a depolarization of the same section will take place. This contribution can be added to the model as follows.

Including a distributed emitter resistance, the electron current density is expressed as

$$J_n(x,y) = J_S \exp \frac{\varphi_p(x,y) - r_e J_E(x,y)}{V_T} \tag{37}$$

where r_e represents the specific emitter resistance [Ωcm^2]. The emitter current density is given by

$$J_E = J_n + \frac{J_n}{\beta} = \frac{J_n}{\alpha} \tag{38}$$

For a given applied V_{BE}, the electron current density is determined by solving the equation

$$J_n(x,y) = J_S \exp \frac{\varphi_p(x,y) - r_e J_n(x,y)/\alpha}{V_T} \tag{39}$$

which defines the dependence of J_n upon φ_p: $J_n = f(\varphi_p)$.
This result is substituted into the (non normalized) governing equation

$$\nabla^2 \varphi_p = -R_{sh}\left[(M-1) - \frac{1}{\beta}\right] J_n = -R_{sh}\frac{\alpha M - 1}{\alpha} J_n(\varphi_p) \tag{40}$$

which is solved with the boundary condition $\varphi_p|edge = V_{BE}$.
To solve (39) let

$$J_{n0} = J_S \exp \frac{\varphi_p}{V_T} \tag{41}$$

which represents the electron current density for a zero resistance. Then, (39) may be written in the form

$$\frac{J_n}{J_{n0}} = \exp\left(\frac{-r_e J_n}{\alpha V_T}\right) = \exp\left(\frac{-r_e J_{n0}}{\alpha V_T}\frac{J_n}{J_{n0}}\right) \tag{42}$$

or, introducing the normalized variables $y = J_n/J_{n0}$, $x = r_e J_{n0}/\alpha V_T$,

$$y = \exp(-xy) \tag{43}$$

which can be solved numerically for the unknown function y(x).
It is interesting to note that, letting w=xy, (43) may be written in the form

$$w \exp(w) = x \tag{44}$$

where w(x) is known as the Lambert function.
An approximate solution to the nonlinear equation (43) is given by the ratio of polynomials

$$y(x) = \frac{1 + a_1 x + a_2 x^2}{1 + b_1 x + b_2 x^2 + b_3 x^3} \tag{45}$$

Assuming a_1=0.732746, a_2=0.0339562, b_1=1.70016, b_2=0.408992, b_3=0.00831313, approximation (96) gives an error less than 0.3% in the range x∈ (0,50).
As a result, we may write

$$J_n = J_{n0} y\left(\frac{r_e J_{n0}}{\alpha V_T}\right) = J_S \, e^{\frac{\varphi_p}{V_T}} \, y\left(\frac{r_e J_S \, e^{\frac{\varphi_p}{V_T}}}{\alpha V_T}\right) \tag{46}$$

and Eq. (40) may be recast in normalized form as

$$\begin{aligned}
\nabla^2 u &= -\frac{R_{sh} L^2 J_S \, e^{\frac{\varphi_p}{V_T}}}{\alpha V_T} (\alpha M - 1) y\left(\frac{J_S r_e \, e^{\frac{\varphi_p}{V_T}}}{\alpha V_T}\right) = \\
&= -\frac{R_{sh} L^2 J_S \, e^{\frac{V_{BE}}{V_T}}}{\alpha V_T} (\alpha M - 1) e^u \, y\left(\frac{R_{sh} L^2 J_S \, e^{\frac{V_{BE}}{V_T}}}{\alpha V_T} \frac{r_e}{R_{sh} L^2} e^u\right) = \\
&= \left[-\frac{R_{sh} L^2 J_S \, e^{\frac{V_{BE}}{V_T}}}{\alpha V_T}\right] (\alpha M - 1) e^u \, y\left(\frac{R_{sh} L^2 J_S \, e^{\frac{V_{BE}}{V_T}}}{\alpha V_T} \frac{R_E}{R_{sh}} e^u\right) = \\
&= \theta_0 (\alpha M - 1) e^u \, y\left(-\theta_0 \frac{R_E}{R_{sh}} e^u\right)
\end{aligned} \tag{47}$$

where θ_0 is a negative quantity.

The base current is calculated as:

$$\begin{aligned} I_B &= 4\left[\frac{1}{\beta}-(M-1)\right]\int_0^{\frac{W_E}{2}}\int_0^{\frac{L_E}{2}} J_n dxdy = \\ &= 4\left[\frac{1}{\beta}-(M-1)\right]\int_0^{\frac{W_E}{2}}\int_0^{\frac{L_E}{2}} J_S\, e^{\frac{\varphi_p}{V_T}}\, y\left(\frac{r_e J_S\, e^{\frac{\varphi_p}{V_T}}}{\alpha V_T}\right) dxdy = \\ &= -\frac{4L^2 J_S\, e^{\frac{V_{BE}}{V_T}}}{\alpha}(\alpha M-1)\int_0^{\frac{w_E}{2}}\int_0^{\frac{l_E}{2}} e^u\, y\left(\frac{R_{sh}L^2 J_S\, e^{\frac{V_{BE}}{V_T}}}{\alpha V_T}\frac{R_E}{R_{sh}}e^u\right) d\xi d\eta = \\ &= 4\frac{V_T\theta_0}{R_{sh}}(\alpha M-1)\int_0^{\frac{w_E}{2}}\int_0^{\frac{l_E}{2}} e^u\, y\left(-\theta_0\frac{R_E}{R_{sh}}e^u\right) d\xi d\eta \end{aligned} \tag{48}$$

and the normalized base current is given by:

$$i_B = \frac{I_B R_{sh}}{V_T} = 4\theta_0(\alpha M-1)\int_0^{\frac{w_E}{2}}\int_0^{\frac{l_E}{2}} e^u\, y\left(-\theta_0\frac{R_E}{R_{sh}}e^u\right) d\xi d\eta \tag{49}$$

The collector current is given by:

$$I_C = 4M\int_0^{\frac{W_E}{2}}\int_0^{\frac{L_E}{2}} J_n dxdy = \frac{M}{\frac{1}{\alpha}-M} I_B = \frac{M}{\frac{1}{\beta}-(M-1)} I_B = bI_B \tag{50}$$

and the emitter current is obtained as:

$$\begin{aligned} I_E &= I_C + I_B = \frac{I_C}{\alpha M} = \frac{I_B}{1-\alpha M} \Rightarrow \\ i_E &= \frac{-i_B}{\alpha M-1} = -4\theta_0\int_0^{\frac{w_E}{2}}\int_0^{\frac{l_E}{2}} e^u\, y\left(-\theta_0\frac{R_E}{R_{sh}}e^u\right) d\xi d\eta \end{aligned} \tag{51}$$

$$
\begin{aligned}
i_B &= 4\theta_0(\alpha M-1)\int_0^{\lambda_x}\int_0^{\lambda_y} e^u\, y\left(-\theta_0 \frac{R_E}{R_{sh}} e^u\right) d\xi d\eta \\
i_B &= 4\theta_0(\alpha M-1)\frac{1}{4} e^{\frac{-R_{Bi} I_B + R_{Eeff} I_E}{V_T}} = \theta_0(\alpha M-1) e^{-\frac{R_{Bi} i_B + R_{Eeff} i_E}{R_{sh}}} \\
e^{\frac{R_{Bi} i_B + R_{Eeff} i_E}{R_{sh}}} &= \frac{1}{4\int_0^{\frac{w_E}{2}}\int_0^{\frac{l_E}{2}} e^u\, y\left(-\theta_0 \frac{R_E}{R_{sh}} e^u\right) d\xi d\eta} = \frac{\theta_0(\alpha M-1)}{i_B} = \frac{-\theta_0}{i_E}
\end{aligned}
\tag{52}
$$

The Eq (47) has been numerically solved in Comsol. Fig. 2.9 shows an Common-Base output characteristic under forced-I_E obtained in this way. Red line refers to the solution of (47) with $R_E=0$. Including the contribution of a $R_E \neq 0$ the maximum biasing point shifts to right, as can be seen by the blue curve, enlarging the Safe Operating Area and underlying the positive effect of the distributed emitter resistance on the pinchin phenomena.

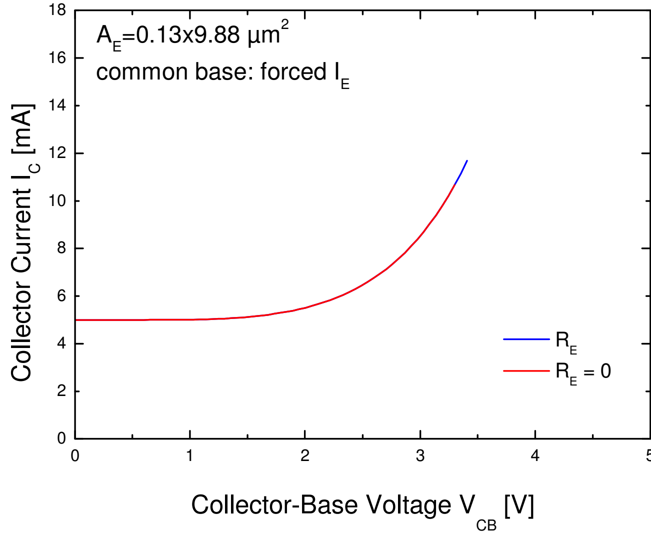

Fig. 2.9 Numerical results obtained for a common-base configuration under a forced-I_E biasing.

2.3.3 Analysis including the current dependence of the multiplication factor

The numerical solution of the model described above cannot explain the discontinuities commonly observed in the common base output characteristics due to the pinch-in effect (see Fig. 2.1). This behaviour is ascribed to the high-injection effects that reduces the electrical field and thus the multiplication factor (Kirk effect [35]).
We can generalize the previous analysis by including the dependence of the multiplication factor upon the current density. This dependence can be empirically modelled as:

$$\alpha M - 1 = (\alpha M_0 - 1)\exp\left(-\frac{J_n}{J_0}\right) \tag{53}$$

which yields:

$$\begin{aligned} \alpha M(y,z) - 1 &= (\alpha M_0 - 1)\, e^{-\frac{J_S}{J_0}\exp\frac{\varphi_p(y,z)}{V_T}} = \\ &= (\alpha M_0 - 1)\, e^{-\frac{J_S}{J_0}\exp\frac{V_{BE}}{V_T}\exp u} = (\alpha M_0 - 1)\, e^{-\theta_H \exp(u)} \end{aligned} \tag{54}$$

where:

$$\theta_H = \frac{J_S \exp\frac{V_{BE}}{V_T}}{J_0} = \frac{\theta_0}{J_0 A_E R_{sh} / (V_T \alpha)} = \frac{\theta_0}{I_0} \tag{55}$$

being:

$$\begin{aligned} \theta_0 &= \frac{R_{sh}}{V_T \alpha} A_E J_S \exp\frac{V_{BE}}{V_T} \\ I_0 &= \frac{R_{sh}}{V_T \alpha} A_E J_0 \end{aligned} \tag{56}$$

The normalized voltage u is obtained from the solution of the following PDE:

$$\nabla^2 u = \theta \exp(u) = -\theta_0 (\alpha M_0 - 1) e^{u - \frac{\theta_0}{I_0} \exp(u)} \tag{57}$$

where:

$$\theta = \frac{R_{sh} A_E J_S \exp \frac{V_{BE}}{V_T}}{V_T \alpha} (1 - \alpha M) = -\frac{R_{sh} A_E J_S \exp \frac{V_{BE}}{V_T}}{V_T \alpha} (\alpha M_0 - 1) e^{-\theta_H \exp(u)} =$$
$$= \theta_0 (\alpha M_0 - 1) e^{-\theta_H \exp(u)} = \theta_0 (\alpha M_0 - 1) e^{-\frac{\theta_0}{I_0} \exp(u)} \tag{58}$$

The input parameters to be specified are: θ_0, αM_0-1, and *a*.
The base current is calculated as:

$$i_B = \frac{R_{sh} I_B}{V_T} = 4 \frac{R_{sh} J_S}{\alpha V_T} \int_0^{W_E/2} \int_0^{L_E/2} (1 - \alpha M) \exp \frac{\varphi_p}{V_T} dydz =$$
$$= -4 \frac{R_{sh} A_E J_S e^{\frac{V_{BE}}{V_T}}}{\alpha V_T} (\alpha M_0 - 1) \int_0^{w_E/2} \int_0^{l_E/2} e^{-\theta_H \exp(u)} e^u \, d\eta d\zeta = \tag{59}$$
$$= 4\theta_0 (\alpha M_0 - 1) \int_0^{w_E/2} \int_0^{l_E/2} e^{u - \frac{\theta_0}{I_0} \exp(u)} \, d\eta d\zeta$$

The collector current is given by:

$$I_c = 4 J_S \int_0^{W_E/2} \int_0^{L_E/2} M e^{\frac{\varphi_p}{V_T}} dydz =$$
$$= 4 A_E J_S e^{\frac{V_{BE}}{V_T}} \int_0^{w_E/2} \int_0^{l_E/2} M e^u \, d\xi d\eta \tag{60}$$

or in normalized form:

$$i_C = 4\frac{R_{sh}A_E J_S\, e^{\frac{V_{BE}}{V_T}}}{V_T}\int_0^{w_E/2}\int_0^{l_E/2} M\, e^u\, d\eta d\zeta =$$

$$= -4\alpha\theta_0\int_0^{w_E/2}\int_0^{l_E/2} M\, e^u\, d\eta d\zeta = -4\alpha\theta_0\int_0^{w_E/2}\int_0^{l_E/2}\frac{(\alpha M-1)+1}{\alpha}e^u\, d\eta d\zeta =$$

$$= -4\alpha\theta_0\int_0^{w_E/2}\int_0^{l_E/2}\frac{(\alpha M_0-1)\,e^{-\frac{\theta_0}{I_0}\exp(u)}+1}{\alpha}e^u\, d\eta d\zeta \tag{61}$$

In order to obtain a common base output characteristics family, Eq. (57) has been solved in Comsol environment. Fig. 2.10 refers to Comsol results in the output plane (the output voltage V_{CB} is hidden in the multiplication factor $M=M(V_{CB})$).

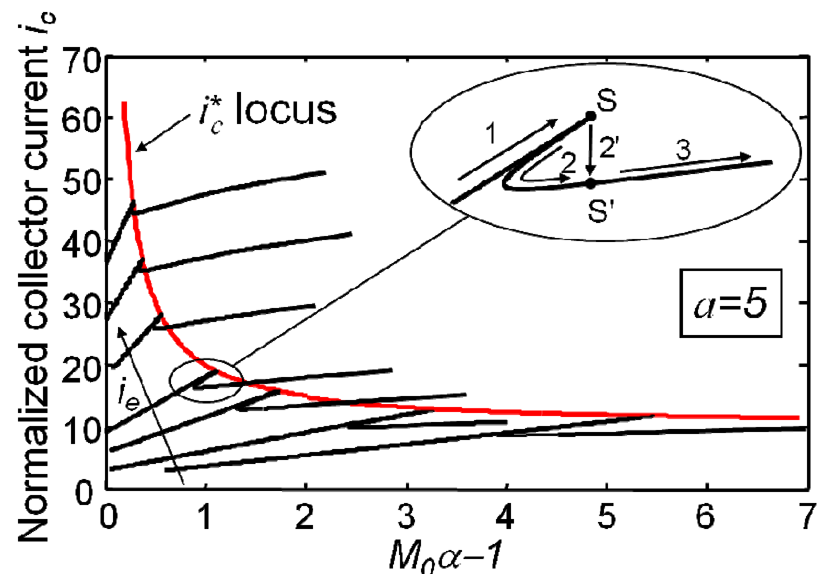

Fig. 2.10 Normalized collector current i_c vs. (αM_0-1) for different values of the emitter current i_e (*a*=5). Also shown is the critical i_c^* locus (red line) given by (34). The inset shows the behaviour near a critical point S for one characteristic.

As can be seen, below the critical i_c^* locus, the behaviour is nearly identical to that obtained without high-injection effects. However, as the critical current i_c^* is approached (point S in the inset), i_c shows a double snapback singularity (see the arrow labelled 2). This anomalous behaviour explains the I_C discontinuity observed experimentally. Indeed, the path 2 from S to S' cannot be seen in experimental common base characteristics because, as the multiplication factor is increased (by increasing V_{CB}), I_C would suddenly jump from S to S', (see the arrow 2'), and then proceed along branch 3 beyond the i_c^* locus.

Chapter 3

Experimental characterization of state-of-the-art SiGe:C HBTs

In order to experimentally define the Safe Operating Area of state-of-the-art SiGe:C HBTs, several bipolar transistors with various values of effective emitter width and length were fully characterized in our laboratories. The extraction steps defined in this section represents also the basics operations needed by the new technique for base resistance extraction proposed in Ch. 4. Finally, electrical stress was applied to devices in order to investigate the time-to-failure (TTF).

3.1 Devices and experimental setup

Devices under test, featuring f_T/f_{MAX}=260/350 GHz, were provided by STMicroelectronics and Infineon Technologies (hereinafter referred to as STM and IFX). Tab. 3.1 summarizes the characterized transistors with extracted values of thermal resistance R_{TH} (see Par. 3.2) and open emitter breakdown voltage BV_{CBO} (see Par. 3.7).

Device	**Company**	**A_E [µm^2]**	**R_{TH} [K/W]**	**BV_{CBO}[V]**
SBY2	STM	0.13×0.88	**10600**	5.5
SBZ2	STM	0.13×4.88	**3470**	5.5
SCA1	STM	0.13×9.88	**2000**	5.5
SCA2	STM	0.13×19.88	**1090**	5.5
SCB1	STM	0.38×0.88	**8210**	5.5
SCC2	STM	0.38×4.88	**2850**	5.5

SCE1	STM	0.38×9.88	**1690**	5.5
SCF2	STM	0.38×19.88	**960**	5.5
SCB2	STM	0.63×0.88	**7050**	5.5
SCD1	STM	0.63×4.88	**2500**	5.5
SCE2	STM	0.63×9.88	**1530**	5.5
SCG1	STM	0.63×19.88	**880**	5.5
SCC1	STM	0.88×0.88	**5790**	5.5
SCD2	STM	0.88×4.88	**2260**	5.5
SCF1	STM	0.88×9.88	**1430**	5.5
SCG2	STM	0.88×19.88	**850**	5.5
S007S33	INFINEON	0.20×0.57	**13790**	6.8
S010S33	INFINEON	0.20×0.87	**11690**	6.8
S028S33	INFINEON	0.20×2.67	**5960**	6.8
S058S33	INFINEON	0.20×5.67	**3400**	6.8
S100S33	INFINEON	0.20×9.87	**2200**	6.8
S028S55	INFINEON	0.42×2.67	**4820**	6.8
S028S120	INFINEON	1.07×2.67	**3840**	6.8
S028S220	INFINEON	2.07×2.67	**2910**	6.8

Tab. 3.1 STM and Infineon devices under test.

On-wafer measurements were performed by means of a PM5 Carl Suss probe station that can be alternatively equipped with RF probes and PH100 probeheads with Tungsten needles. Electrical signals are handled by Keithley 2400 source-meter units. The baseplate (i.e., thermo-chuck) temperature T_B can be set to a prescribed value by an ATT heating/cooling system. Fig. 3.1 shows the experimental setup used during characterization measurements.

Fig. 3.1 Experimental setup for device characterization.

3.2 Thermal resistance

The self-heating thermal resistances R_{TH} were evaluated by invoking a widely-used approach [36] involving 2 steps:
First, the electrothermal feedback coefficient ϕ of the base-emitter voltage V_{BE} was determined at various emitter currents by extracting the slope of the DC V_{BE}–T_B characteristics at power levels sufficiently low so as to reasonably assume $T_j \approx T_B$, where T_j is the (average) temperature of the base-emitter junction. Parameter ϕ was found to logarithmically depend on current according to the following relation:

$$\phi = \phi_0 - \frac{k}{q}\ln\left(\frac{I_E}{A_E \cdot J_S}\right) \approx \phi_0 - \frac{k}{q}\ln\left(\frac{I_C}{A_E \cdot J_S}\right) \qquad (1)$$

where ϕ_0 was evaluated to be equal to 3.47 mV/K regardless of the DUT.
The accuracy of (1) was validated by comparing the I_C–V_{BE} characteristics measured at various baseplate temperatures T_B (i.e., 300, 320, 340, and 360 K) with the following first-order model [36]:

$$I_C = A_E \cdot J_S \exp\left(\frac{V_{BE} + \phi_0 \cdot \Delta T_B}{\eta V_{T0} + \frac{k}{q} \cdot \Delta T_B} \right) \tag{2}$$

where A_E is the emitter area, J_S is the reverse saturation current, η is the ideality factor, and $\Delta T_B = T_B - T_0$, T_0 being equal to 300 K. J_S and η were found to fall in the ranges 3.4-3.8×10^{-16} A/μm^2 and 1.06-1.07 (1.06 for “large” devices and 1.07 for “small” ones), respectively.

The Fig. 3.2 illustrates the comparison between (2) and the experimental I_C–V_{BE} curves measured on devices SBZ2, at V_{CE}=1 V by setting T_B to 300, 320, 340, and 360 K. Since (2) does not include resistive and high-injection effects, the accuracy worsens at high current levels.

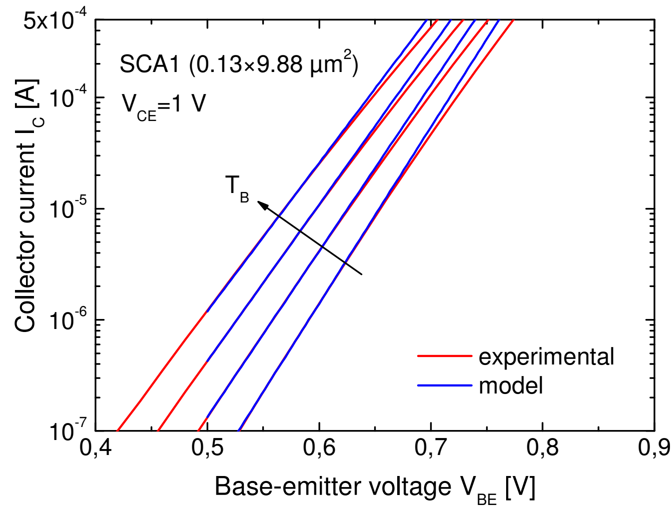

Fig. 3.2 Collector current I_C against base-emitter voltage V_{BE} for transistor SCA1 at V_{CE}=1 V and baseplate temperature T_B equal to 300, 320, 340, and 360 K: comparison between (red lines) experimental data and (blue) model (2) with optimized parameters ϕ_0 and η.

Second, the slope γ of DC V_{BE}–V_{CB} characteristics was measured under common-base conditions by keeping I_E constant. The emitter current is chosen so as to entail perceptible self-heating, while the collector voltage is maintained sufficiently low in order to avoid impact ionization. The self-heating thermal resistance R_{TH} of the DUTs is then calculated as

$$R_{TH} = -\frac{\gamma}{I_E \cdot \phi(I_E)} \tag{3}$$

In Fig. 3.3, the determination of the slope γ is shown for transistors SCA1.

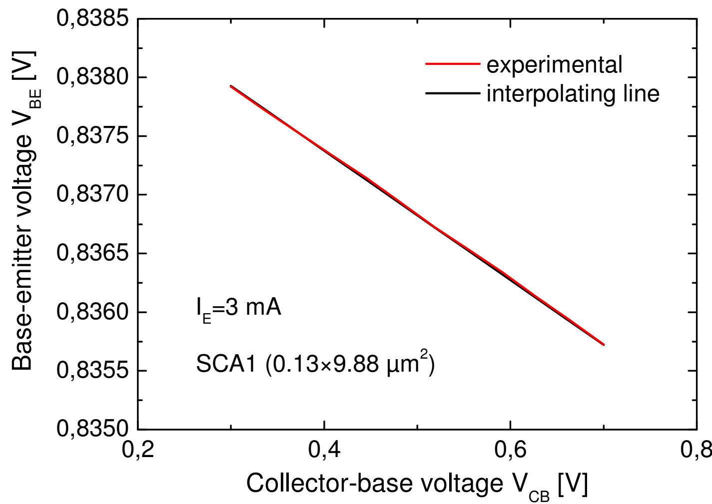

Fig. 3.3 Base-emitter voltage V_{BE} against collector-base voltage V_{CB} for transistor SCA1 at I_E=3 mA.

This procedure allowed determining the self-heating thermal resistances for all 16 B3T HBTs under investigation. An overview of the values is shown in Tab. 3.1.
The Fig. 3.4 shows the increase in R_{TH} as obtained by reducing the effective emitter length L_E for assigned emitter widths W_E. It can be inferred that the growth rate of the thermal resistances is higher for shorter devices.

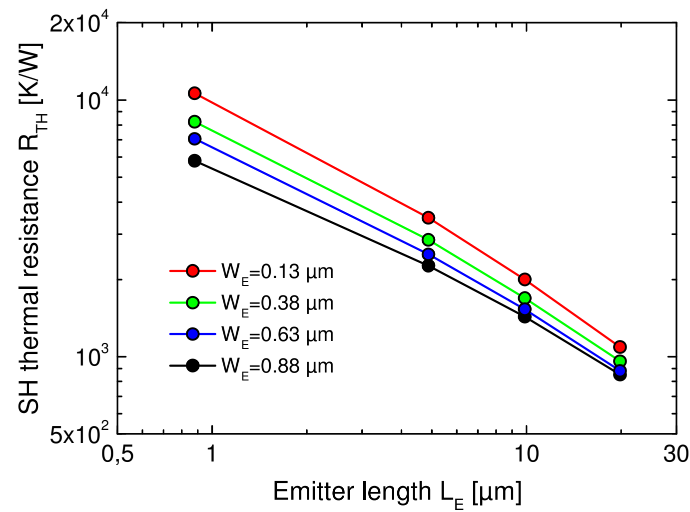

Fig. 3.4 Scaling of thermal resistance R_{TH} for assigned emitter widths W_E for characterized STM devices.

From the obtained trend it can be concluded that very large thermal resistances are expected for the next generation of advanced HF devices to be realized with <200 nm lithography.

3.3 Gummel plots

Fig. 3.5-3.6 report Gummel plots corresponding to STM and Infinenon devices. Measures were performed at V_{CE}=1 V by setting T_B to 300, 320, 340, and 360 K.

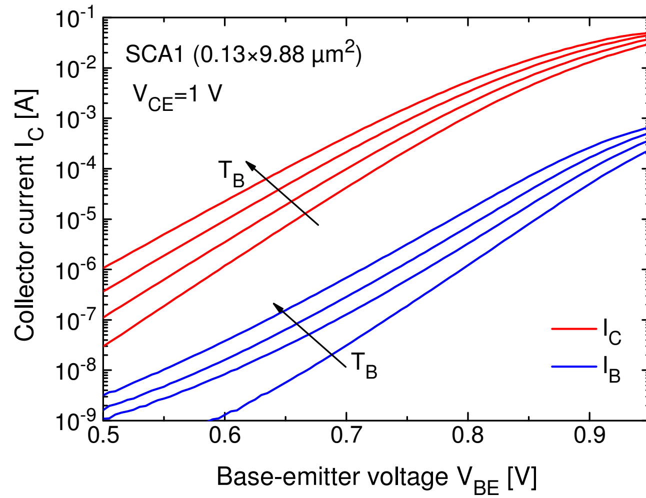

Fig. 3.5 Common emitter Gummel plot for STM transistor SCA1 at V_{CE}=1 V and baseplate temperature T_B equal to 300, 320, 340, and 360 K.

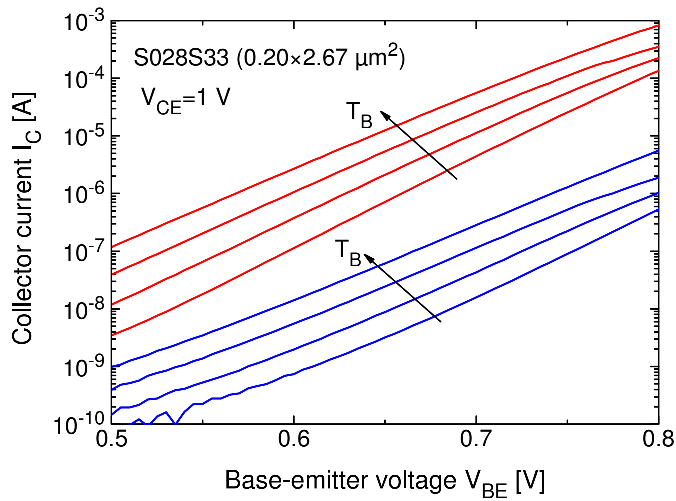

Fig. 3.6 Common emitter Gummel plot for IFX transistor S028S33 at V_{CE}=1 V and baseplate temperature T_B equal to 300, 320, 340, and 360 K.

A thermally-induced instability phenomenon can be detected at high V_{CE} in devices with self-heating thermal resistance R_{TH}. Fig. 3.7 reports the common-emitter Gummel plot corresponding to device SCB2 (R_{TH} = 7050 K/W). The baseplate temperature T_B is kept equal to 300 K. The curves were measured at V_{CE}=0.8 and 2.9 V; in the latter case, the instability is detected at V_{BE}=0.78 V.

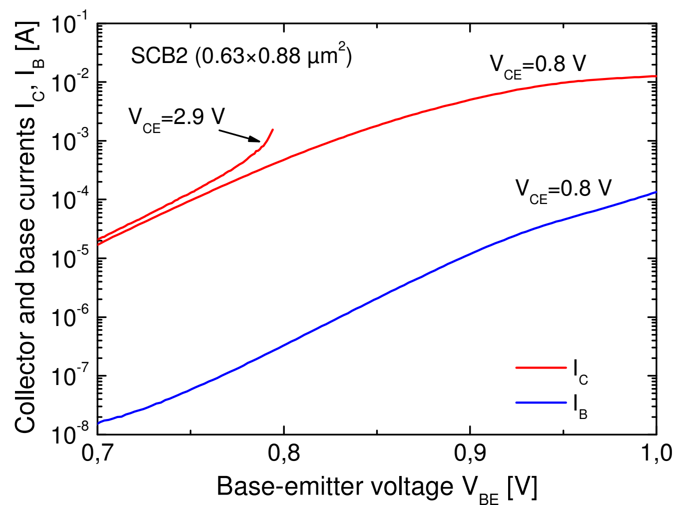

Fig. 3.7 Common-emitter Gummel plot related to the STM device SCB2.

3.4 Common emitter current gain

The Fig. 3.8 details the common-emitter current gain β_F of transistor SCB2 as a function of base-emitter voltage V_{BE} for V_{CE}=0.8 V and T_B=300 K. The gain at medium current levels was found to be about 1650 while reducing to nearly 100 at V_{BE}=1.0 V due to high-injection effects. In general, the gain peak was found to fall in the span 1400-1700 for the analyzed DUTs.

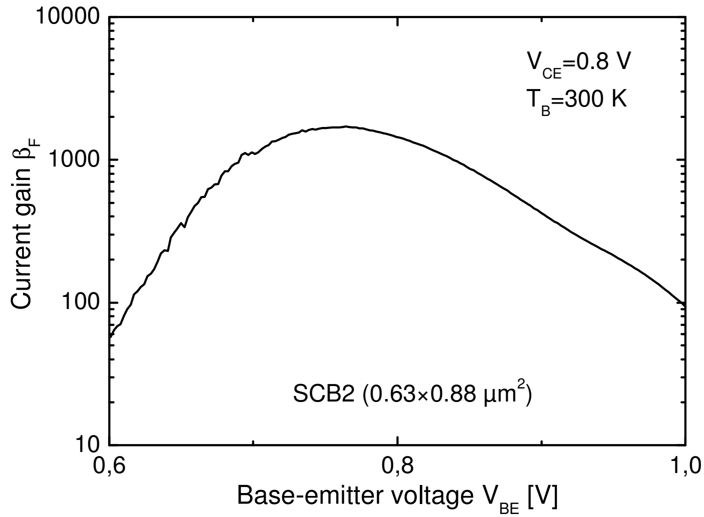

Fig. 3.8 Common-emitter current gain as a function of V_{BE} for the STM device SCB2.

3.5 Common emitter output characteristics

3.5.1 Forced-I_B characteristics

Fig. 3.9-3.10 depict the output common-emitter I_C-V_{CE} characteristics under forced-I_B biasing for ST and Infineon devices. The negative temperature coefficient at high I_B and the occurrence of impact ionization at high V_{CE} are evident.

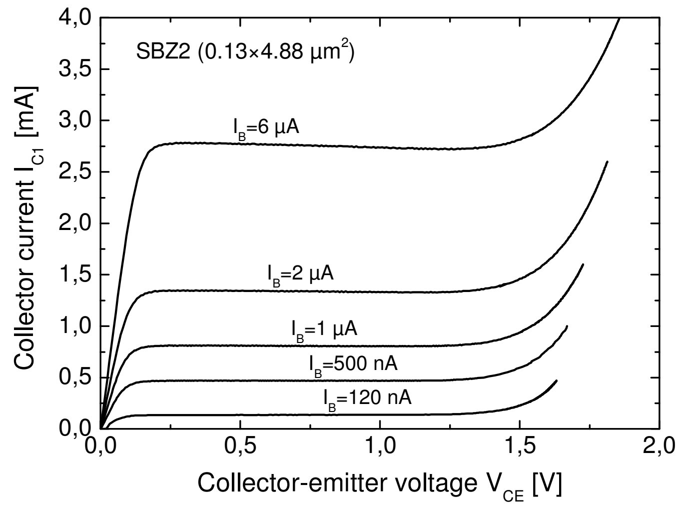

Fig. 3.9 Common-emitter output characteristics under forced-I_B biasing for STM device SBZ2.

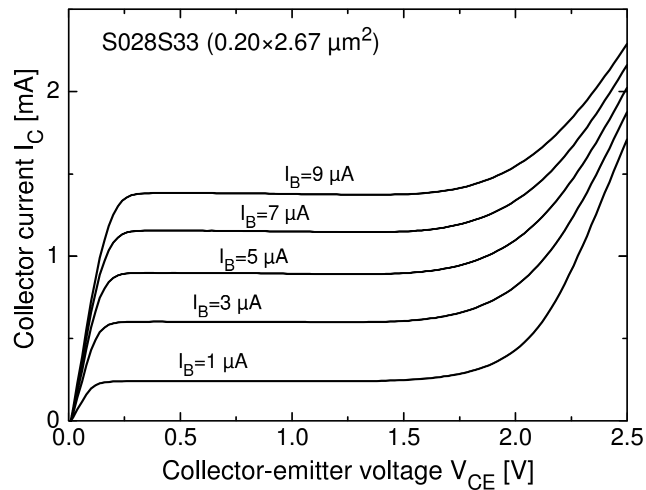

Fig. 3.10 Common-emitter output characteristics under forced-I_B biasing for IFX device S028S33.

The collector current shows a negative temperature coefficient. This trend is highlighted in the Fig. 3.11 at I_B=5 μA for T_B=300, 320, 340, and 360 K.

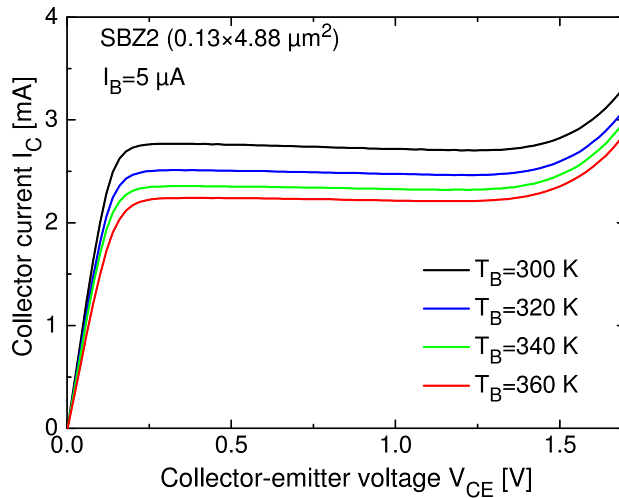

Fig. 3.11 Common-emitter output characteristics under forced-I_B biasing and baseplate temperature T_B equal to 300, 320, 340, and 360 K for STM device SBZ2.

3.5.2 Forced-V_{BE} characteristics: "the runaway"

The output common emitter I_C-V_{CE} characteristics at various V_{BE} highlighted some unexpected non-destructive "runaway" occurrences. This phenomenon is measured at V_{CE} values rather lower than the expected limit (the "insuperable" voltage limit should be in principle given by BV_{CBO} (≈5.4 V) + V_{BE}). Fig. 3.12 shows this instability for an STM device.

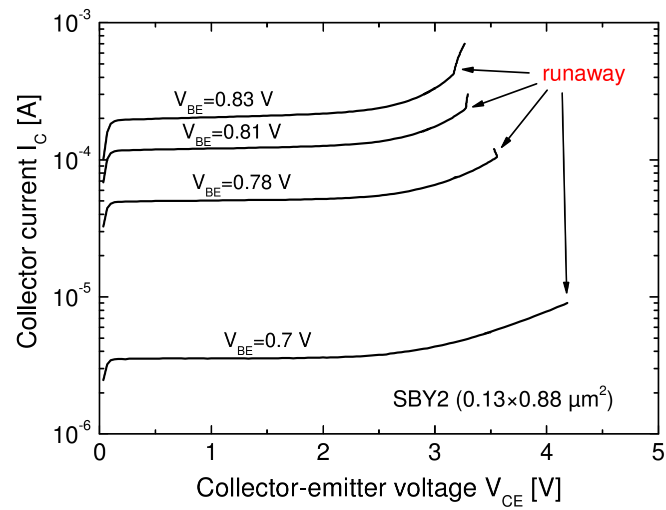

Fig. 3.12 Common-emitter output characteristics under forced-V_{BE} biasing for STM device SBY2.

In addition, it was found that biasing the HBTs with V_{CE} higher than that corresponding to these "runaway" points systematically destroys the DUTs. Moreover, the runaway is detected by either sweeping V_{CE} or forcing I_C and is fully reproducible as can be seen in the "magnification" shown in Fig. 3.13 for STM SCB2 device.

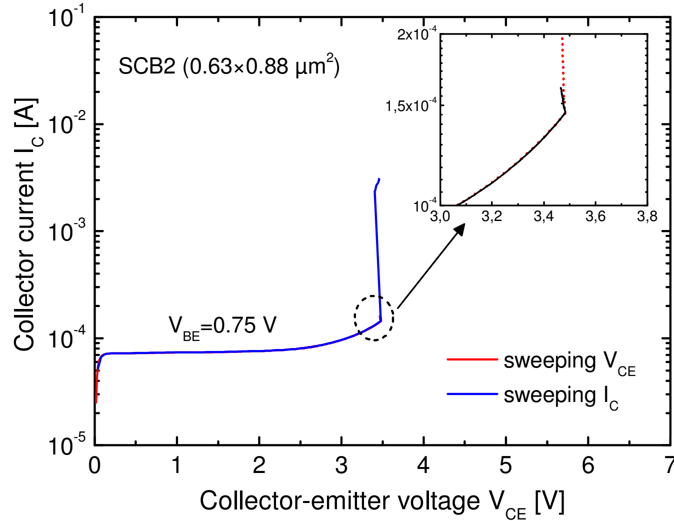

Fig. 3.13 Common-emitter output characteristics under forced-V_{BE} biasing for STM device SCB2. The runaway phenomena occurs both in a sweeping V_{CE} or sweeping I_C approach.

The occurrence of this unexpected behavior is well evident also in the common-emitter Gummel plane. Indeed, the SOA boundary due to the concurrent influence of electrothermal and avalanche effects in the (V_{CE}, I_C) plane coincides with that occurring in the (V_{BE}, I_C) plane. Fig. 3.14, compared with Fig. 3.13, shows that this correspondence was found to occur also for the “runaway” mechanisms.

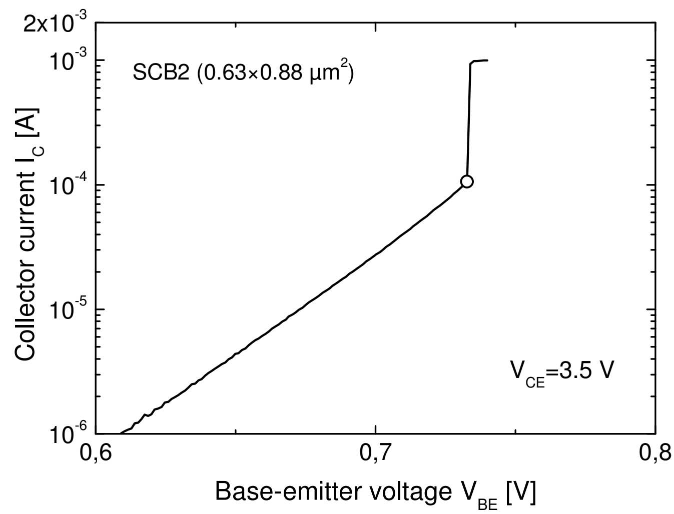

Fig. 3.14 Common-emitter Gummel plot under collector-emitter voltage V_{CE}=3.5V for STM device SCB2.

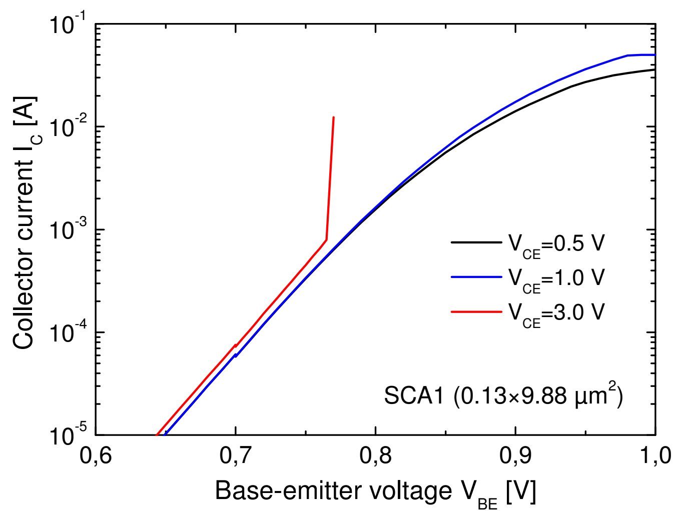

Fig. 3.15 Common-emitter Gummel plot under collector-emitter voltage V_{CE}=0.5V, 1.0V and 3.0V for STM device SCA1.

Runway detection for device SCA1 is reported in Fig. 3.15.
The “runaway” mechanism disappears when temperature increases. Fig. 3.16-3.19 show I_C–V_{CE} characteristics at constant V_{BE} for T_B=300, 320, 340, and 360 K for device SCA1.

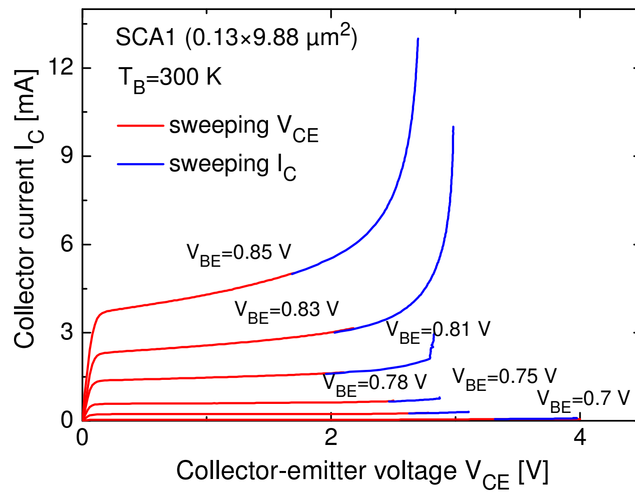

Fig. 3.16 Common-emitter output characteristics under forced-V_{BE} biasing and baseplate temperature T_B equal to 300K for STM device SCA1.

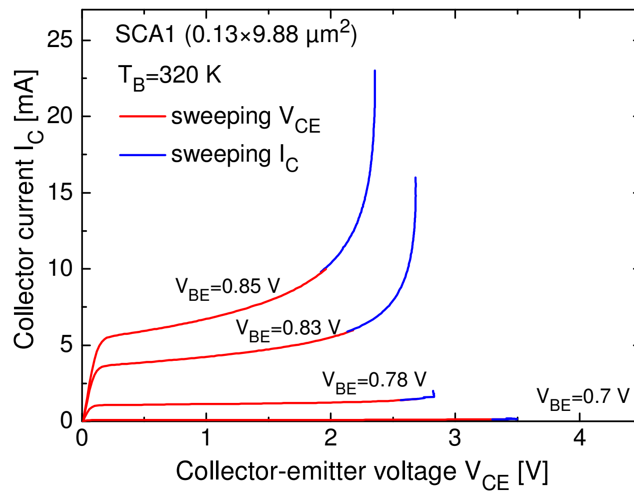

Fig. 3.17 Common-emitter output characteristics under forced-V_{BE} biasing and baseplate temperature T_B equal to 320K for STM device SCA1.

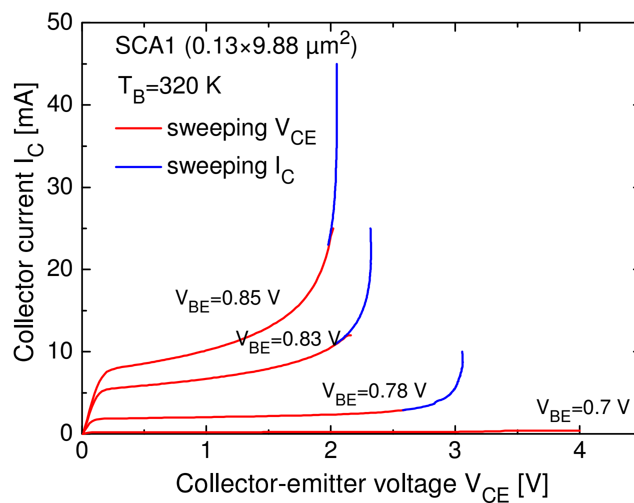

Fig. 3.18 Common-emitter output characteristics under forced-V_{BE} biasing and baseplate temperature T_B equal to 340K for STM device SCA1.

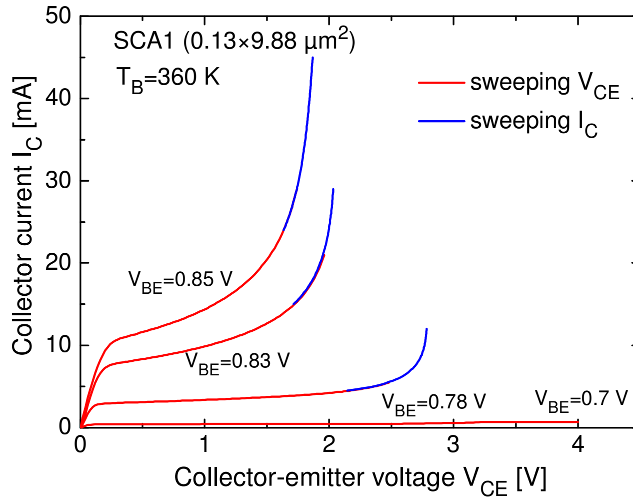

Fig. 3.19 Common-emitter output characteristics under forced-V_{BE} biasing and baseplate temperature T_B equal to 360K for STM device SCA1.

3.6 Common base output characteristics

Common Base I_C-V_{CB} characteristics, measured for ST and Infineon devices, evidence a pinch-in mechanism arising at low I_E values: for voltages beyond BV_{CEO} the avalanche multiplication factor increases and the base current I_B becomes negative; at a “critical” V_{CB}, the current hogs in the device center (pinch-in), thus giving rise to an avalanche-induced negative-differential-resistance behavior [37], [38]. The curves reported in Fig. 3.20-3.21 were attained by resorting to the PH100 probeheads with Tungsten needles to allow common-base measurements.

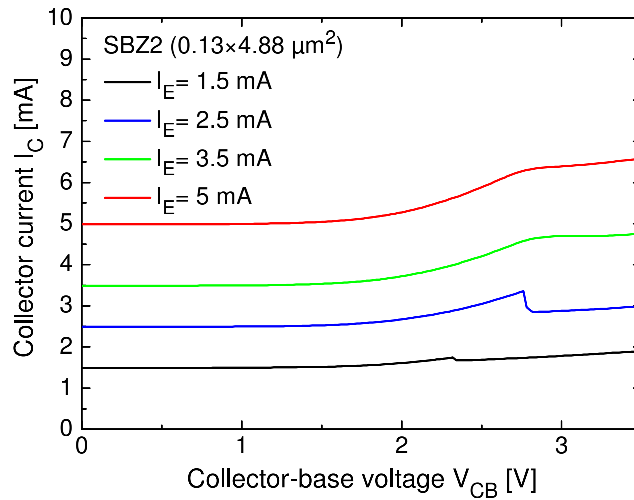

Fig. 3.20 Common-base output characteristics under forced-I_E biasing for STM device SBZ2.

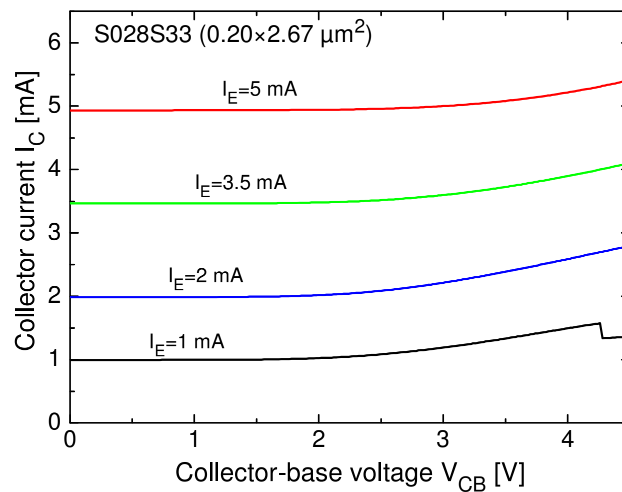

Fig. 3.21 Common-base output characteristics under forced-I_E biasing for STM device S028S33.

Fig. 3.22-3.23 depict the corresponding behavior of V_{BE} against V_{CB}.

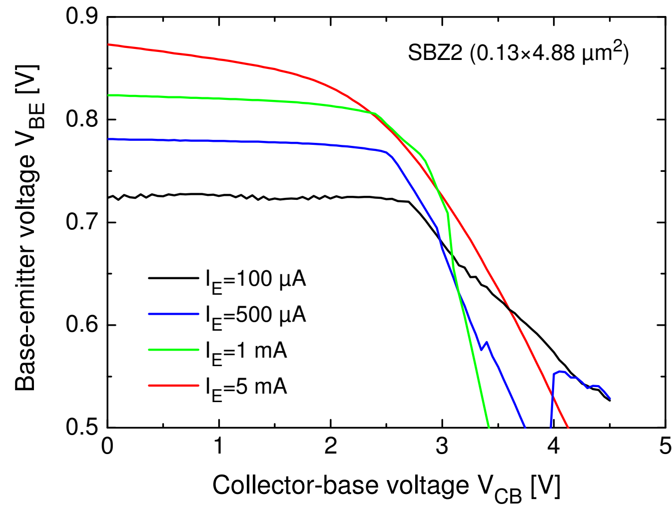

Fig. 3.22 Base-emitter voltage V_{BE} in a common-base configuration under forced-I_E biasing for STM device SBZ2.

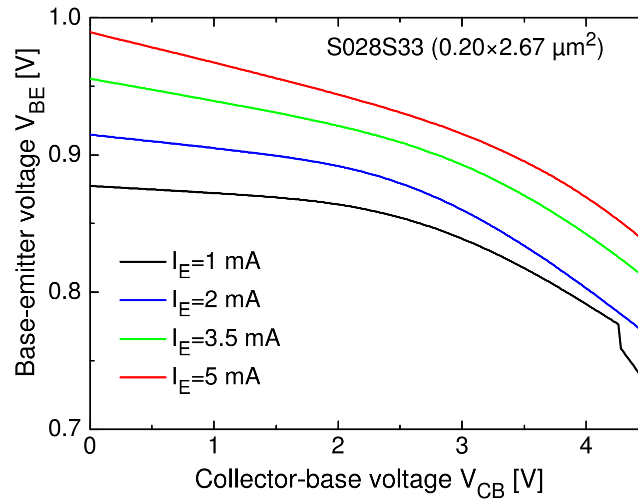

Fig. 3.23 Base-emitter voltage V_{BE} in a common-base configuration under forced-I_E biasing for STM device S028S33.

The Fig. 3.24-3.25 describe the corresponding behavior of I_B against V_{CB}. As can be seen, after the pinch-in occurrence, the absolute values of I_B first drop and then become somewhat insensitive to V_{CB}; this is in accordance with the previous literature on this topic.

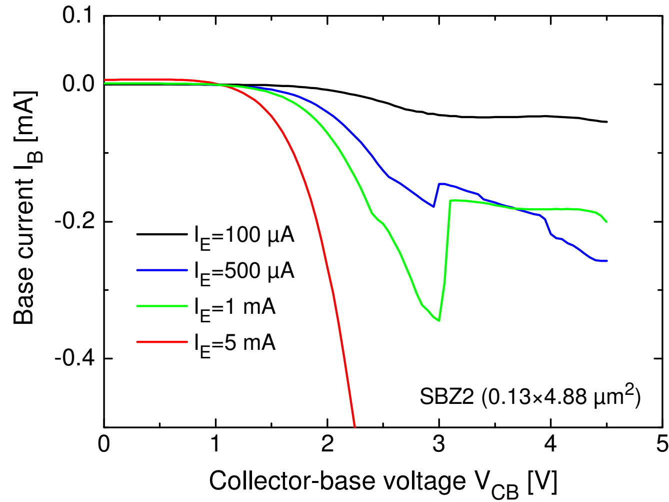

Fig. 3.24 Base curent I_B in a common-base configuration under forced-I_E biasing for STM device SBZ2.

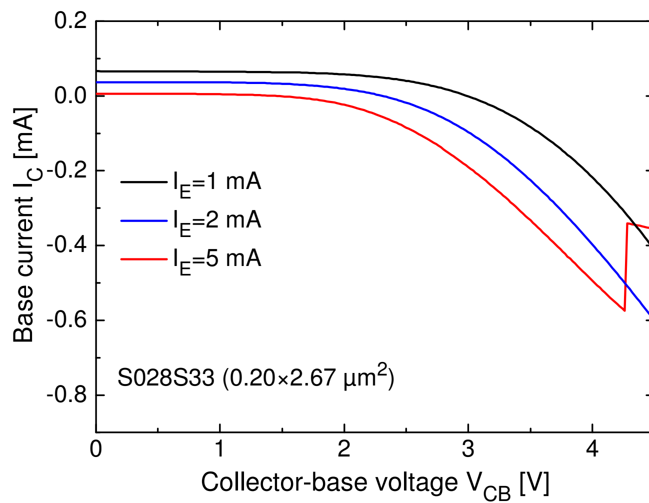

Fig. 3.25 Base curent I_B in a common-base configuration under forced-I_E biasing for STM device S028S33.

3.7 BV_{CBO} extraction

The open-emitter breakdown voltage BV_{CBO} was determined by measuring the reverse breakdown voltage of the base-collector diode while keeping the emitter terminal floating. Measurements on various devices, allowed evidencing that BV_{CBO} amounts to about 5.4-5.45 V for ST devices and 6.8 V for Infineon ones. The BV_{CBO} extraction for an Infineon device is shown in Fig. 3.26.

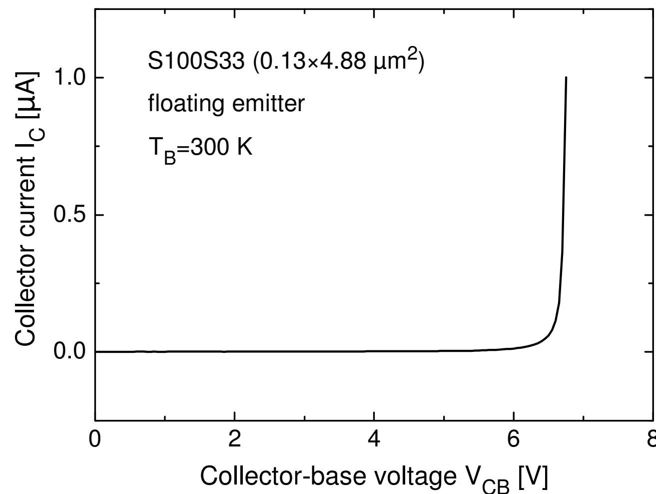

Fig. 3.26 Collector current I_C against collector-base voltage V_{CB} in a floating emitter configuration for IFX device S100S33.

3.8 Emitter resistance

The parasitic emitter series resistance R_E was extracted by employing the DC procedure proposed in [39], usually referred to as open-collector technique. The base current I_B is increased by keeping the

collector floating, and I_E, V_{CE} are measured. The experimental I_E–V_{CE} behavior is then described through the analytical relation:

$$V_{CE} = a_1 \cdot I_E + b_1 \cdot \ln\left(1 + \sqrt{\frac{I_E}{c_1}}\right) \quad (4)$$

where a_1, b_1, and c_1 are to be optimized through a routine relying on the least-squares method; in particular, R_E=a_1. The results obtained by this approach have been successfully compared with 2-D FEM simulations carried out with MEDICI in [39]. Tab. 3.2 reports the R_E values extracted for some of the DUTs, namely, SBY2, SBZ2, and SCA1 for the ST devices and S028S33, S058S33 and S100S33 for Infineon devices. As expected, the emitter downscaling entails an increase in R_E.

HBT	R_E [Ω]
SBY2	11.12
SBZ2	4.24
SCA1	3.05
S028S33	7.27
S058S33	3.85
S100S33	2.29

Tab. 3.2 Extracted emitter resistancefor different STM and Infineon devices.

Fig. 3.27-3.28 illustrate the experimental V_{CE}–I_E characteristics as measured on STM and Infineon devices by keeping the collector floating, along with the interpolating curves for the extraction of parameter a_1=R_E.

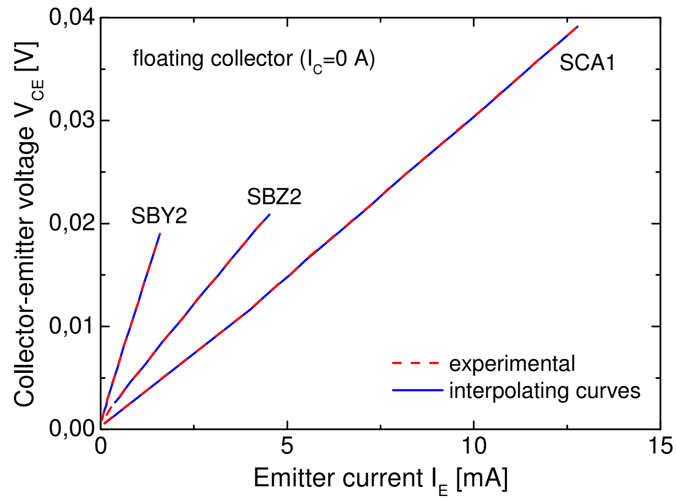

Fig. 3.27 Collector-emitter voltage V_{CE} against emitter current I_E in a floating collector configuration for different STM devices.

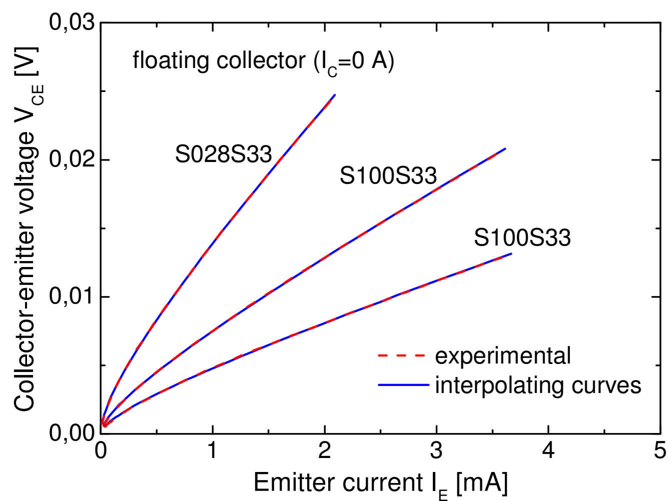

Fig. 3.28 Collector-emitter voltage V_{CE} against emitter current I_E in a floating collector configuration for different IFX devices.

3.9 Stress characterization

In order to reach peak frequency performance (f_T) beyond 500GHz for millimeter wave applications hetero-junction bipolar transistors are designed to operate at high current density above 12 mA/µm². Moreover, they are more likely to operate at the base-collector voltage limit, under avalanche condition in the base-collector junction region. These conditions are able to create serious damages which can limit the device life time. Device reliability emerges as a critical issue requiring in-depth investigations with stress measurements.
Devices under test were stressed in our laboratories with three classical degradation modes:

- Reverse bias stress
- Forward bias stress
- Mixed mode stress

3.9.1 Reverse bias stress

The current gain of bipolar transistors is degraded when the base–emitter junction is reversed biased. Hot carriers generated inside the base emitter junction space charge region creates Si/SiO_2 interface traps at the edges of the junction. These defects increase Generation Recombination base leakage current (predominant at low V_{BE}) but do not influence the collector current. Therefore the result is a decrease of the current gain. The process speed depends on the reverse bias stress condition and on the stress time [40]. I_B degradation follows the model proposed by [41]. Fig. 3.29 shows the result of the reverse bias stress (V_{BE} = -2.5V) applied to STM SCC2 device by means of Gummel plots measured after different values of stress time.

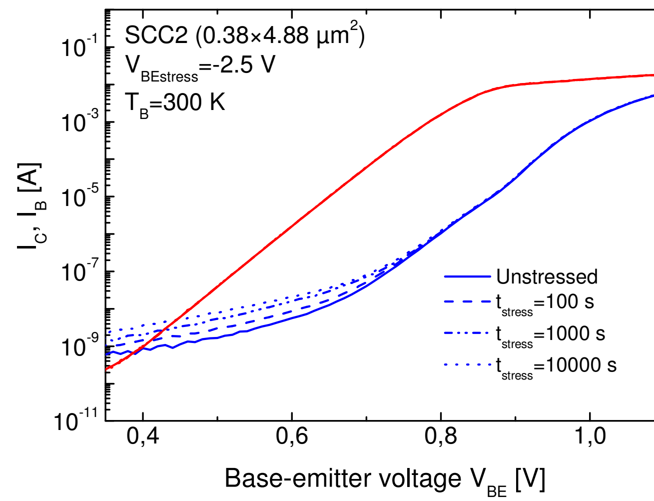

Fig. 3.29 Gummel plot evolution under reverse bias stress for STM device SCC2.

While collector current is unchanged after stress, it's clear the degradation of base current with reduction of current gain as shown in Fig. 3.30.

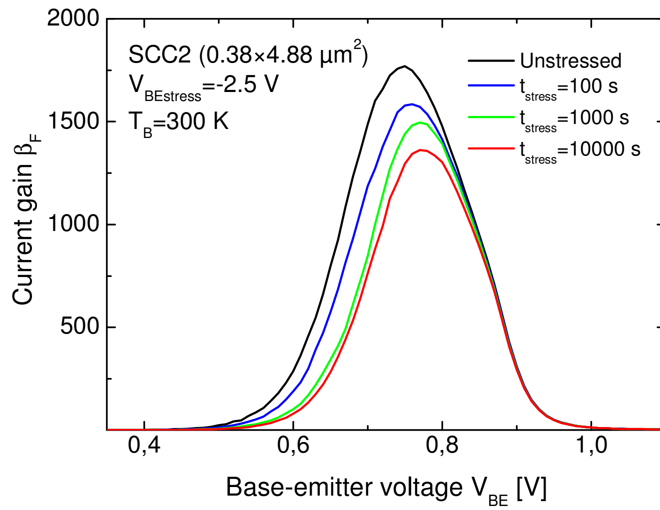

Fig. 3.30 Common emitter current gain evolution under reverse bias stress for STM device SCC2.

Similar behavior is highlighted by all devices stressed during this phase. As can be observed in Fig. 3.31 and Fig. 3.32, a stress time of 10 seconds is enough to reduce the current gain in a considerable way.

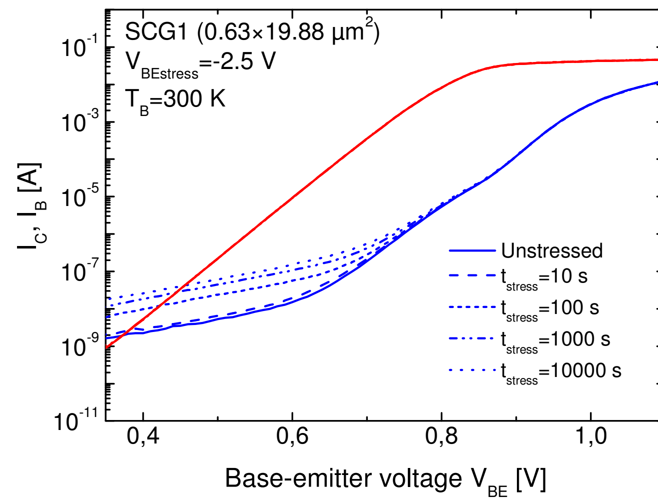

Fig. 3.31 Gummel plot evolution under reverse bias stress for STM device SCG1.

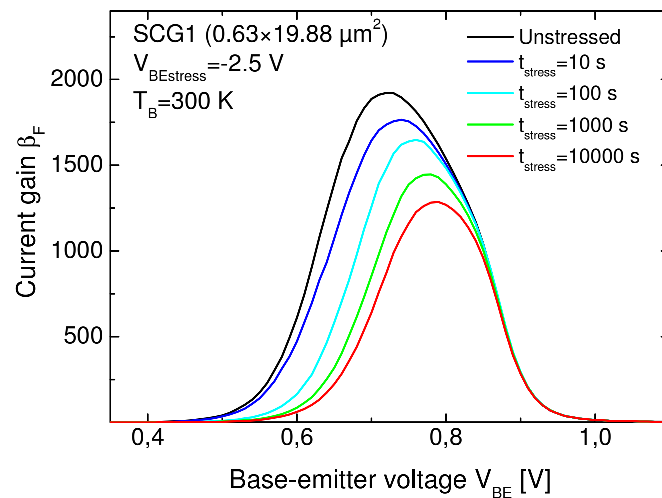

Fig. 3.32 Common emitter current gain evolution under reverse bias stress for STM device SCG1.

Temperature has a positive impact on defect repairing. Thermal annealing yields a reduction of the base current at low and middle V_{BE}. In [42] a storage of SiGe:C HBTs at 150°C during 24 hours is performed and excess base current was totally removed. However, literature asserts the stability (unchanged for days) of the base current after stress at room temperature. This fact is not true for STM devices analyzed. In fact, as can be seen in Fig. 3.33 e Fig 3.34, a decrease in base current at room temperature for all stressed devices was observed.

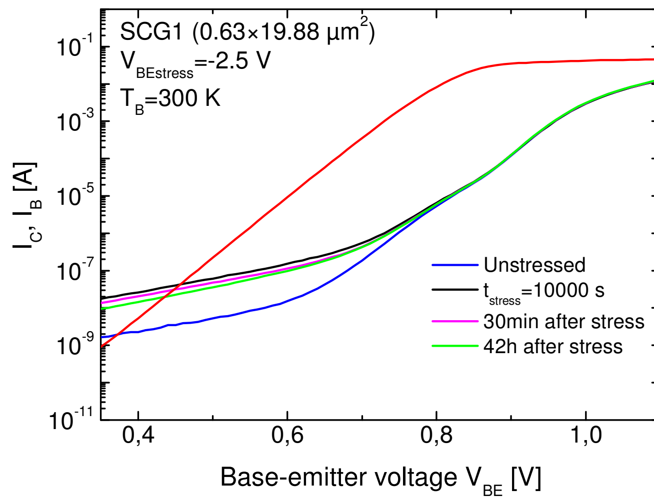

Fig. 3.33 Defect repairing at room temperature after reverse bias stress for STM device SCG1.

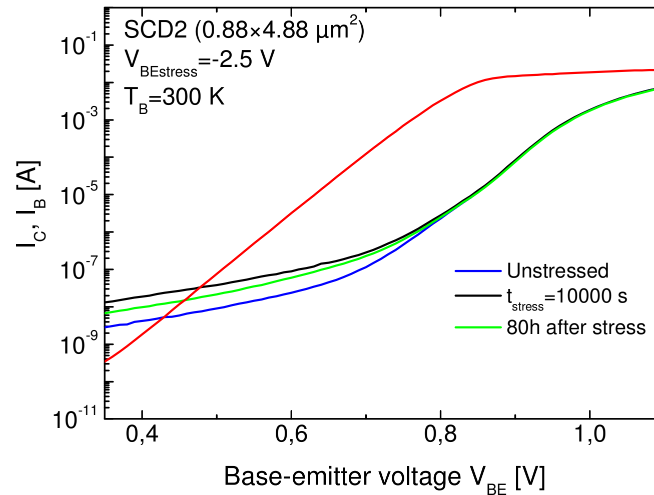

Fig. 3.34 Defect repairing at room temperature after reverse bias stress for STM device SCD2.

3.9.2 Forward bias stress

In circuit applications, HBTs fabricated within BiCMOS technology, are sometimes subject to reverse bias during the on/off transition time of MOS transistors. Nevertheless, the typical operation mode of bipolar transistor is the forward mode.

In forward bias stress mode, high emitter current stress was applied with fixed base-collector junction voltage for long stress time. The stress current rises until 5 x $J_C@f_{Tpeak}$ while holding the collector and base terminals at zero bias. STM devices show $J_C@f_{Tpeak}$=14 mA/µm^2 [43]. It's important to underline that this stress is able to improve the transistors degraded by means of reverse bias stress. High current densities produce local heating at emitter-base junction yielding a passivation of traps previously generated [42]. Applying this stress mode (56h after base emitter reverse stress) on STM devices, as can

be seen in Fig. 3.35, a defect repairing but there is an uncertainty caused by the “natural” defect improvement at room temperature.

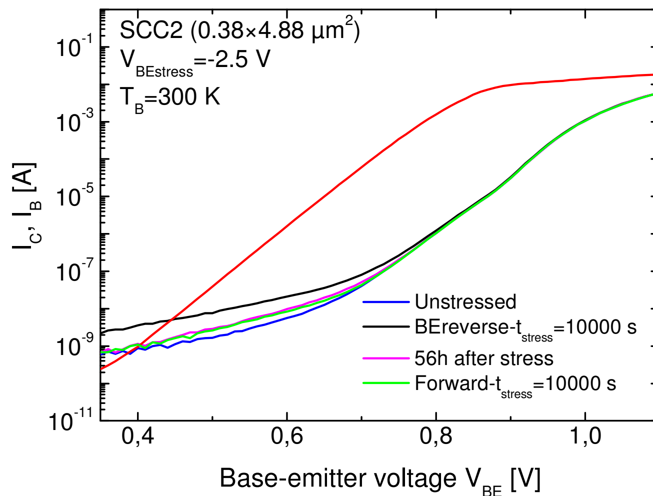

Fig. 3.35 Gummel plot evolution under forward bias stress for STM device SCC2.

3.9.3 Mixed-Mode stress

This stress mode occurs when high collector current and high collector-base voltage (mixed-mode) are applied simultaneously on the device [44]. These conditions are often used in RF and mixed-signal applications to achieve maximum circuit performance. This makes this stress mode an important reliability regime for advanced SiGe HBTs. Mixed-mode stress produces traps in the emitter-base space-charge region but also in the collector-base space-charge region. The presence of these defects produces an increase of I_B current at low and middle V_{BE}. The avalanche multiplication process (V_{CE} of stress

above BV_{CEO}) gives to some carriers enough energy to cross the base creating defects at Si/SiO_2 base emitter lateral spacer.
In [44] stress is applied by means of an extreme Gummel measurement. In this measurement, V_{BE} reaches a very high value (1.2-1.4 V) to guarantee an high I_C and V_{CB} steps from 0 to 3V. The effect of the stress is recorded by tracing regular Gummel plots between each extreme stress Gummel plot.
In [45] devices are stressed at constant I_E and high V_{CB} for different time duration. A time-to-fail model for Mixed-mode stress on SiGe HBTs is presented in [46].
The strategy presented in [44] was applied to SiGe:C HBTs under test. Fig. 3.36-3.39 show Gummel plots and current gain reduction after stress applied to 2 STM devices.

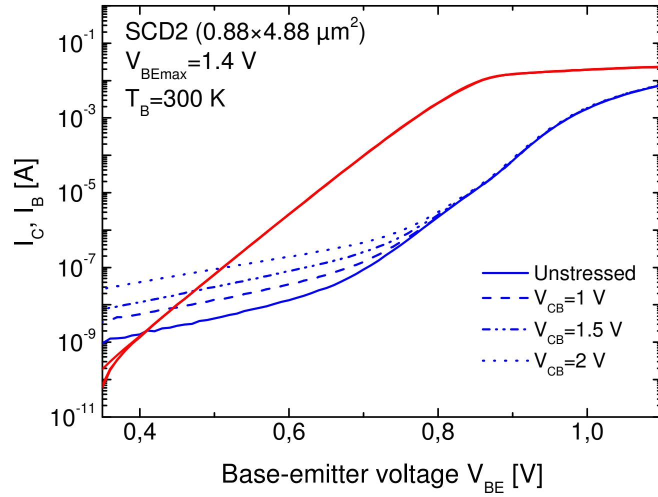

Fig. 3.36 Gummel plot evolution under mixed-mode stress for STM device SCD2.

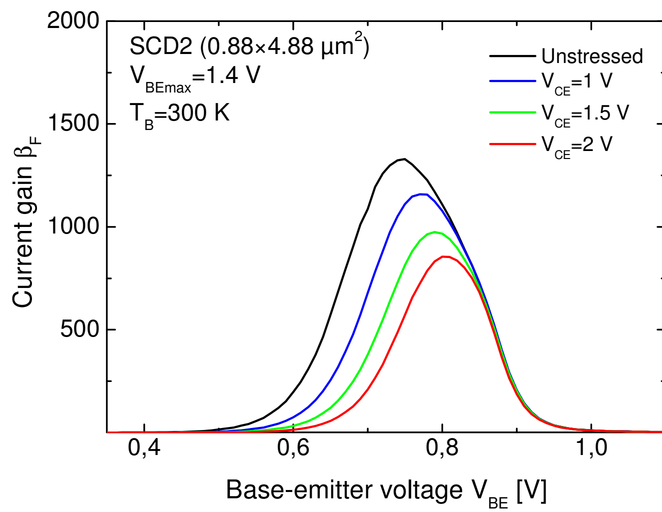

Fig. 3.37 Common emitter current gain evolution under mixed-mode stress for STM device SCD2.

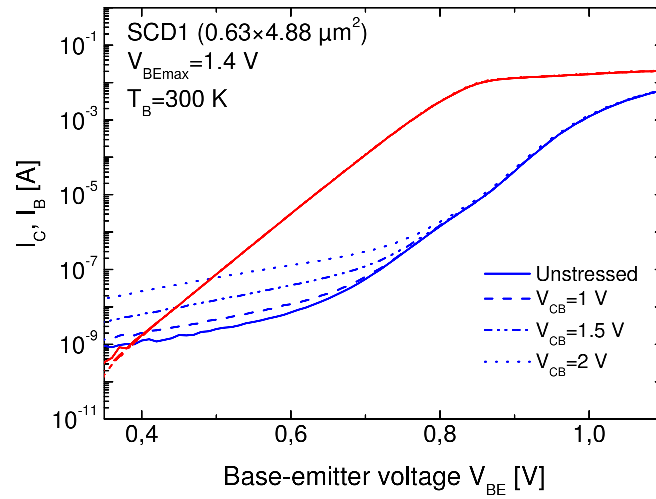

Fig. 3.38 Gummel plot evolution under mixed-mode stress for STM device SCD1.

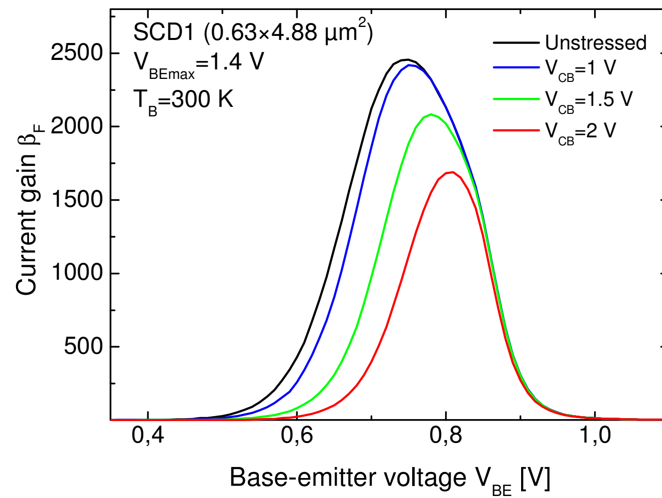

Fig. 3.39 Common emitter current gain evolution under mixed-mode stress for STM device SCD1.

The influence of W_E (for constant L_E) on ΔI_B (defined as I_B post-stress divided by I_B pre-stress) is shown in Fig. 3.40. The observed reduction of ΔI_B for larger devices can be due to the pinch-in effect because increases the distance between the avalanche current generation (in the center) and the base-emitter spacer [45].

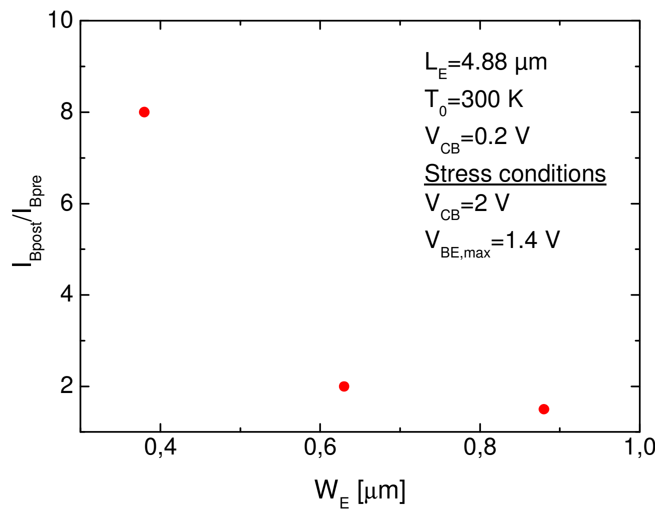

Fig. 3.40 I_B post-stress divided by I_B pre-stress for assigned emitter length L_E for characterized STM devices.

An important difference observed for HBT under test regards the defect repairing at room temperatures. The defects generated by mixed-mode stress are not repaired at room temperatures as is shown in Fig. 3.41 and Fig. 3.42 for 2 STM devices.

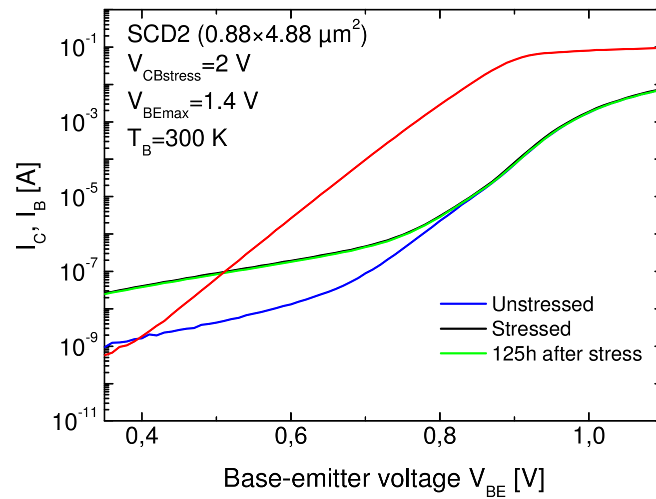

Fig. 3.41 Gummel plot evolution after mixed-mode stress for STM device SCD2.

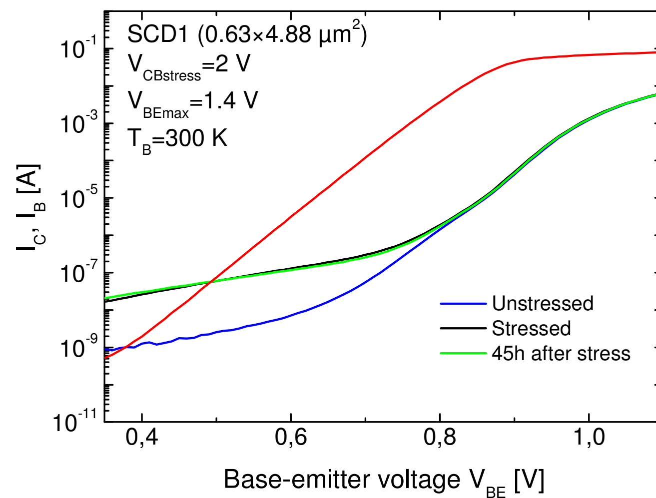

Fig. 3.42 Gummel plot evolution after mixed-mode stress for STM device SCD1.

Chapter 4

A new technique for base resistance extraction

It is commonly recognized that the parasitic base resistance R_B can degrade the performance of bipolar transistors in terms of noise, gain, and bandwidth. Unfortunately, the experimental extraction of this critical parameter is generally troublesome due to the concurrent occurrence of various physical mechanisms, as e.g., self-heating, current crowding, and base push-out. Several approaches have been proposed in the literature to tackle this issue. Ac techniques [47] are versatile and accurate, but rely on expensive instrumentation and significant measurement efforts. As a consequence, the less-demanding dc methods are usually preferred. Some of these require dedicated dual-base test structures [48]. Others rely on measurements performed directly on the device to characterize [49]-[55]. In particular, the classical method suggested in [50] suffers from various approximations that affect its reliability, while the sophisticated procedure presented in [51] requires the simultaneous extraction of several parameters. In [54], an elaborate dc technique accounting for self-heating and Early effect is proposed. All the techniques present in literature allow the extraction of a single value of the R_B (bias-independent). As described in Sec. 2, under common base (CB) conditions by keeping the emitter current I_E constant, R_B increases with collector voltage V_{CB} due to the current crowding induced by the growing reversed base current, eventually leading to the pinch-in of the current to a very small area [28], [37], [38]. An important contribution is given in [55], where Verzellesi et al. develop a simple method to extract the base resistance dependence upon biasing in the impact-ionization regime (i.e., above the open-base breakdown voltage BV_{CEO}) under CB conditions. However, this approach is based on a simplified transistor model that neglects self-heating (SH), impact-ionization (II), and high-injection (HI) effects, thereby leading to intolerable inaccuracy when applied to device categories where

these mechanisms play a major role, as in e.g., advanced HF SiGe HBTs [2] and silicon-on-glass BJTs [56].
Starting from Verzellesi method, all the relevant effects that influence the device behavior in forward active mode has been included in the transistor model. The additional physical parameters can be effortlessly extracted through the procedures shown in Sec. 3. In this section, the improved approach is described and applied to various state-of-the-art HF SiGe:C HBTs.

4.1 The Verzellesi's method

The method proposed by Verzellesi et al requires a simple common base dc measurement to be carried out by increasing V_{CB} at constant I_E (see Fig. 4.1).

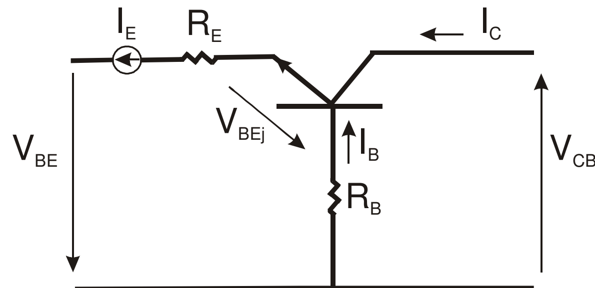

Fig. 4.1 Common-base configuration.

In this configuration, the base current is reduced until it reverses its sign, as can be seen in Fig. 4.2.

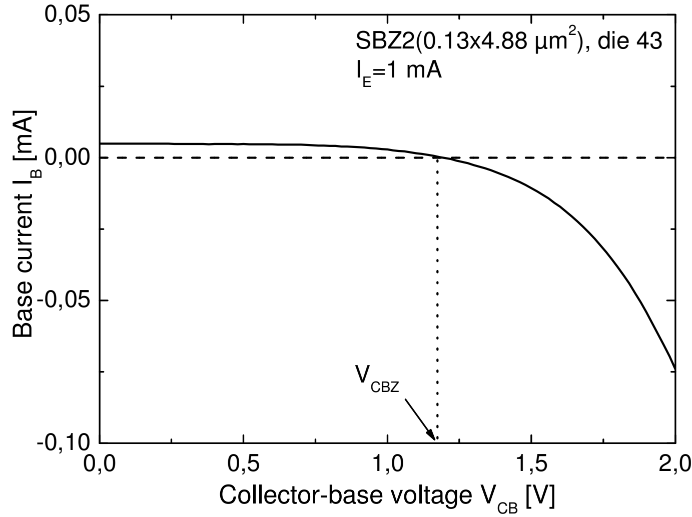

Fig. 4.2 Base curent I_B in a common-base configuration under forced-I_E biasing for STM device SBZ2.

The drop on R_B is zero in this reverse point (V_{CB}=V_{CBZ}). The corresponding base-emitter voltage, V_{BEZ}, is the sum of the drop on intrinsic base-emitter junction, V_{BEj}, and across the emitter resistance, R_E. In this point we have:

$$V_{BEz} = V_{BEj} + R_E \mid I_E \mid \tag{1}$$

When we increase V_{CB}, in order to keep a constant I_E, we have to reduce V_{BE}. This is caused by Early effect that increases the base-collector space charge region reducing the neutral base region.
As a result, at V_{CB}/=V_{CBz} (V_{BEj}/=V_{BEjz}):

$$V_{BE} = V_{BEj} + R_B I_B + R_E \mid I_E \mid \tag{2}$$

By substracting (1) from (2), we have:

$$R_B = \frac{V_{BE} - V_{BEZ}}{I_B} - \frac{V_{BEj} - V_{BEjZ}}{I_B} \quad (3)$$

Verzellesi et al ascribed the difference between V_{BEj} and V_{BEjZ} to the Early effect only (neglecting Early effect yields to an overestimation of the extracted R_B values). In this way (3) becomes:

$$R_B = \frac{V_{BE} - V_{BEZ} + V_{T0} \ln\left(\frac{1 + V_{CB} / V_A}{1 + V_{CBZ} / V_A}\right)}{I_B} \quad (4)$$

where V_A is the Early voltage, V_{T0} is the thermal voltage and all the other terms are available from the measurement.
The Verzellesi method was applied to state-of-the-art SiGe HBTs in order to verify the accuracy of the method but the its accuracy is inacceptable for this kind of devices (see Fig. 4.6-4.10).

4.2 The improved technique

The aforementioned method technique does not account for some mechanisms that play a relevant role in state-of-the-art SiGe HBTs as e.g., self-heating (SH) and impact ionization (II). Through simple formulations associated to a straightforward parameter extraction methodology the transistor model has been enriched by adding SH, II, and high-injection effects (HI). By including these effects, the collector current of a bipolar transistor operated in forward active mode can be expressed as:

$$I_C = M \cdot \left(1 + \frac{V_{CE}}{V_A}\right) \cdot \left(\frac{1}{HI}\right) \cdot A_E \cdot J_S \cdot \exp\left[\frac{V_{BEj} + \phi \cdot (\mathrm{T}_j - \mathrm{T}_B)}{\eta V_{T0}}\right] \quad (5)$$

The models and the extraction procedures are described in the following paragraphs.

4.2.1 Self-heating

The self-heating thermal resistances R_{TH} were evaluated as shown in Par. 3.2. The following first order model was used to take in account of self-heating phenomena:

$$I_C = A_E \cdot J_S \cdot \exp\left[\frac{V_{BE} + \phi_0 \cdot \Delta T_B}{\eta V_{T0} + \frac{k}{q} \cdot \Delta T_B}\right] \qquad (6)$$

where η is the ideality factor, and $\Delta T_B = T_B - T_0$, T_0 being equal to 300 K. J_S and η were found to fall in the ranges $3.4\text{-}3.8\times10^{-16}$ A/μm^2 and 1.06-1.07 (1.06 for “large” devices and 1.07 for “small” ones), respectively.

4.2.2 Impact ionization

The following recently-developed model [38] was adopted to describe the dependence of parameter ξ=M-1 (M being the avalanche multiplication factor) on collector-base voltage V_{CB}:

$$\xi = M - 1 = a \cdot \frac{V_{CB}/BV_{CBO}}{1 - V_{CB}/BV_{CBO}} \cdot \exp\left[-b \cdot \left(\frac{V_{CB}}{BV_{CBO}}\right)^c\right] \qquad (7)$$

The open-emitter breakdown voltage BV_{CBO} was determined by measuring the reverse breakdown voltage of the base-collector diode while keeping the emitter terminal floating. Fig. 4.3 shows the curve obtained for SBZ2 device.

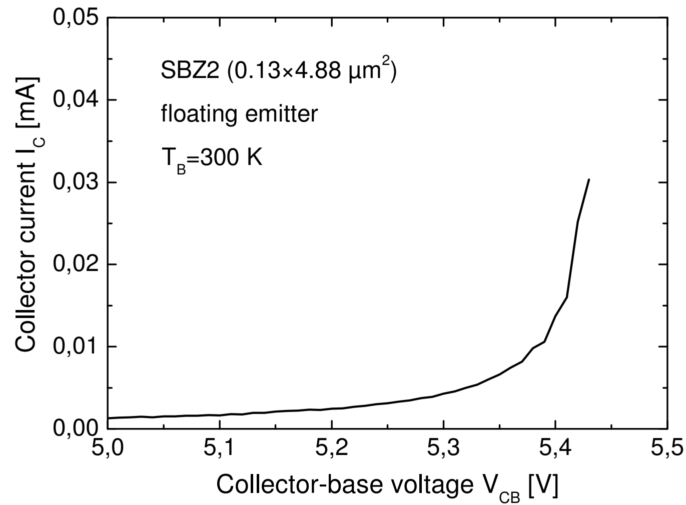

Fig. 4.3 Collector current I_C against collector-base voltage V_{CB} in a floating emitter configuration for STM device SBZ2.

The experimental ξ–V_{CB} curves were achieved from the common base output characteristics by exploiting the technique proposed in [57]. Afterward, the parameters *a*, *b*, and *c* were optimized through a custom routine so as to guarantee the best match between Eq. (7) and the portion of the experimental ξ–V_{CB} characteristics limited to the V_{CB} voltage corresponding to the pinch-in. Fig. 4.4 depicts the comparison between the ξ–V_{CB} curve corresponding to STM HBT SBZ2 for I_E=1 mA and Eq. (7).

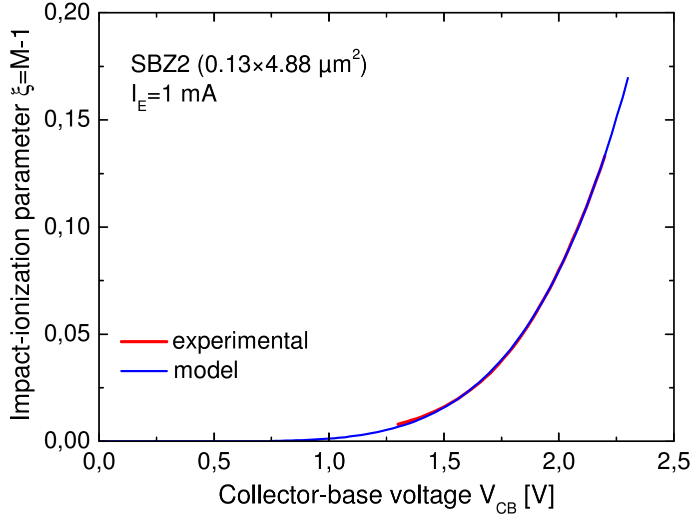

Fig. 4.4 Impact ionization parameter ξ against collector-base voltage V_{CB} STM device SBZ2.

4.2.3 High-injection effects

High-injection effects were modeled by dividing the expression of the current under medium current levels by the term

$$HI(I_C) = 1 + \left(\frac{I_C}{A_E \cdot J_{HI}} \right)^{n_{HI}} \tag{8}$$

where parameters J_{HI} and n_{HI} were optimized by comparing the experimental common-emitter current gain, as measured by increasing V_{BE} at a low V_{CE} value (so as to safely disregard SH and II effects) with

$$\beta_F = \frac{\beta_{F0}}{HI(I_C)} \tag{9}$$

β_{F0} being the gain at medium current levels.

4.2.4 The model

The Verzellesi method can now be enriched with aforementioned phenomena (see par. 3.2.1-3.2.3). By including into (5) the described formulations for ϕ, M, and HI, the bipolar transistor model becomes

$$I_C = M\left(V_{CB}\right)\cdot\left(1+V_{CE}/V_A\right)\cdot A_E\cdot J_S\cdot \\ \cdot\frac{1}{HI\left(I_C\right)}\cdot\exp\left[\frac{V_{BEj}+\phi_0\cdot\Delta T_j}{\eta V_{T0}+\left(k/q\right)\cdot\Delta T_j}\right] \tag{10}$$

where it is evidenced that M and HI depend upon V_{CB} and I_C, respectively.
From (9), voltages V_{BEj} and V_{BEjZ} to be employed in (3) become

$$V_{BEj} = -\phi_0\cdot\Delta T_j + \\ +\left(\eta V_{T0}+\frac{k}{q}\cdot\Delta T_j\right)\cdot\ln\left[\frac{I_C\cdot HI\left(I_C\right)}{A_E\cdot J_S\cdot M\left(V_{CB}\right)\cdot\left(1+V_{CE}/V_A\right)}\right] \tag{11}$$

$$V_{BEjZ} = -\phi_0\cdot\Delta T_{jZ} + \\ +\left(\eta V_{T0}+\frac{k}{q}\cdot\Delta T_{jZ}\right)\cdot\ln\left[\frac{I_E\cdot HI\left(I_E\right)}{A_E\cdot J_S\cdot M\left(V_{CBZ}\right)\cdot\left(1+BV_{CEO}/V_A\right)}\right] \tag{12}$$

where

$$\Delta T_j = R_{TH}\cdot\left(V_{CE}\cdot I_C+V_{BE}\cdot I_B\right) \tag{13}$$

$$\Delta T_{jZ} = R_{TH}\cdot BV_{CEO}\cdot I_E \tag{14}$$

The subscript Z denotes that the voltages, currents, and temperatures correspond to I_B=0 A.

In conclusion, after a preliminary stage to optimize parameters φ_0, η, BV_{CBO}, a, b, c, I_{HI}, and n_{HI}, one can employ the generalization of the approach developed in [55] obtained by substituting (11)-(14) into (3). The extraction requires a single CB output characteristic. Fig. 4.5 illustrates the experimental CB output characteristics of a ST device (SBZ2) obtained at various emitter current values; it is shown that in the impact-ionization regime current discontinuities arise, which are due to the occurrence of the pinch-in mechanism.

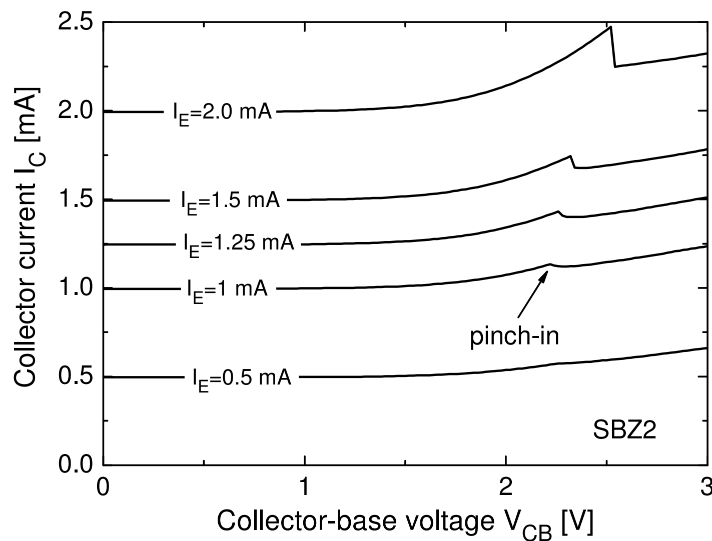

Fig. 4.5 Experimental common-base output characteristics for STM device SBZ2.

4.3 Measurements results

The new technique has been applied to several SiGe:C bipolar transistors provided by STMicroelectronics and Infineon Technologies with various values of effective emitter width and length. Fig. 4.6-4.8, which illustrates the R_B behavior against V_{CB}, show the results

measured for STM devices (SBZ2, SCA1, and SCE2), as evaluated by adopting the original expression (4) [55], and the improved versions obtained by including self-heating, impact ionization and high-injection effects, i.e., the model given by (3) and (11)-(14). Fig. 4.9 and Fig. 4.10 report the analogous results attained for the IFX HBTs S058S33 and S100S33.

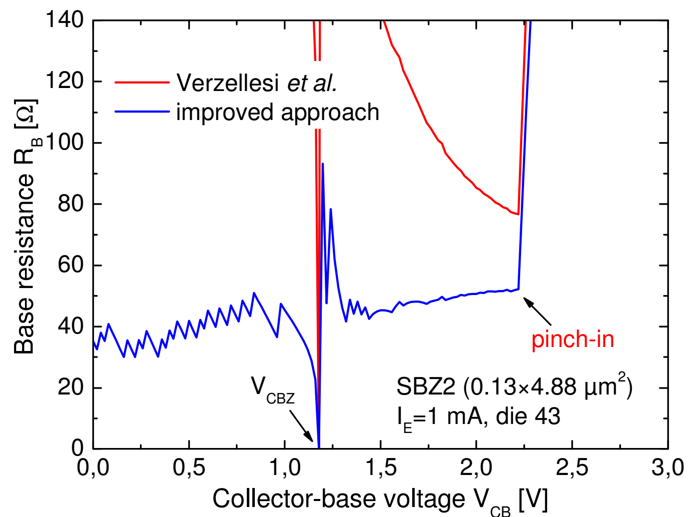

Fig. 4.6 Base resistance R_B as a function of collector-base voltage V_{CB} for STM devices SBZ2.

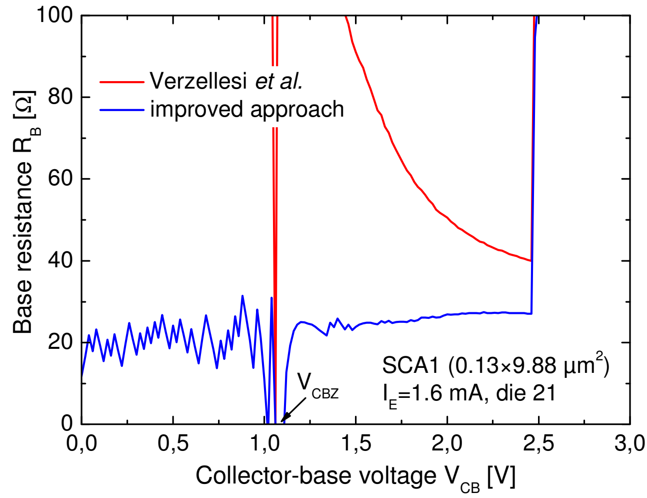

Fig. 4.7 Base resistance R_B as a function of collector-base voltage V_{CB} for STM devices SCA1.

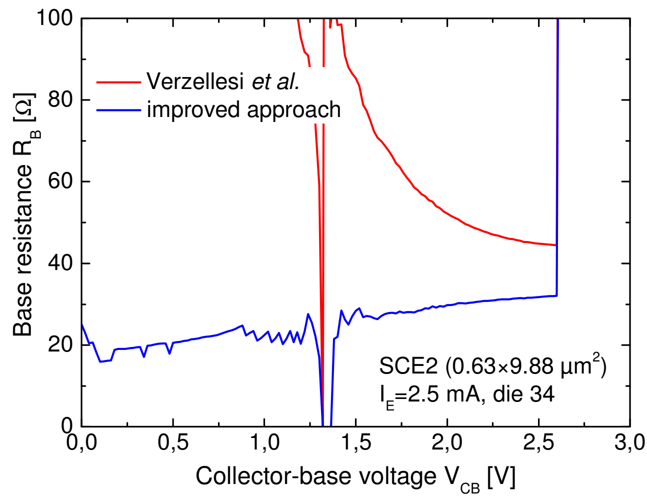

Fig. 4.8 Base resistance R_B as a function of collector-base voltage V_{CB} for STM devices SCE2.

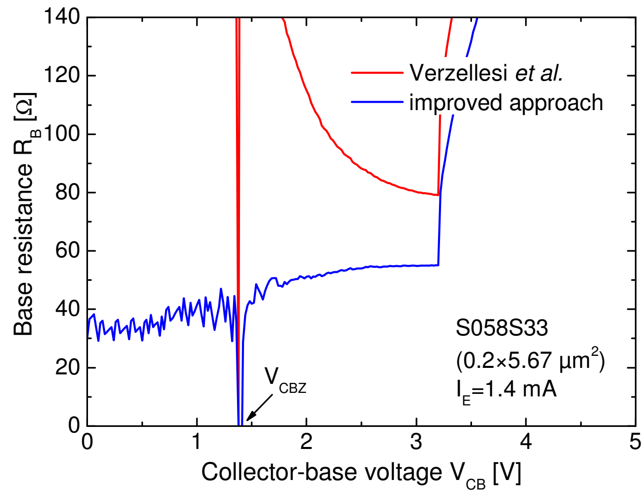

Fig. 4.9 Base resistance R_B as a function of collector-base voltage V_{CB} for IFX devices S058S33.

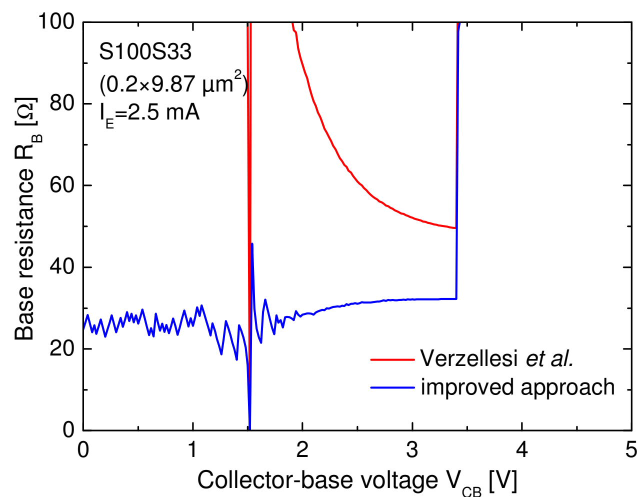

Fig. 4.10 Base resistance R_B as a function of collector-base voltage V_{CB} for IFX devices S100S33.

As can be seen in all R_B extractions (Fig. 4.6-4.10) R_B increases above BV_{CEO}. This is caused by the enhanced current focusing caused by the increment of (the negative) I_B. When the current flow is eventually restricted to a very small area in the device center (at high V_{CB}), i.e., the current hogging is pushed to the extreme (pinch-in), there is an abrupt growth in R_B. This explains the collector current reduction in the I_C–V_{CB} characteristics, as shown in Fig. 4.5.

The noise that characterizes the range of output voltage V_{CB} under V_{CBZ} for very small devices can be ascribed to the low values of the base currents. Nevertheless, in most cases, an increase in R_B with V_{CB} can be observed, which is due to the reduction in base-emitter debiasing (i.e., in the current crowding along the emitter periphery) since (the positive) I_B decreases.

It's interesting to note that R_B scale with $1/L_E$. Values of R_B as extracted for a V_{CB}=2V are summarized in Fig. 4.11.

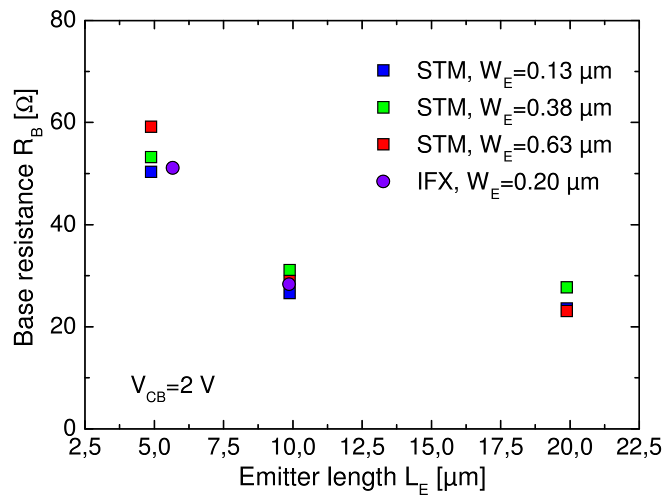

Fig. 4.11 Scaling of base resistance R_B for assigned emitter widths W_E for characterized STM and IFX devices.

4.4 Validation and comparisons

The accuracy evaluation of the proposed method is a not trivial task. Fig. 4.6-4.10 clearly evidenced that the original formulation derived by Verzellesi *et al.* is unreliable for advanced HBTs with thermal resistances of thousands of K/W and low BV_{CBO}. For V_{CB} < 2 V the adoption of (4) might lead to R_B values in the order of several hundreds of Ω, due to the approximation of negligible SH, II, and HI effects.
An other method has been used in order to compare the R_B extraction results. Vanhoucke *et al* [58] implemented a dc technique, based on common-base measurements, to extract the R_B. It's important to underline that this method is devised to extract single (i.e., biasing-independent) R_B values and, therefore, it should not allow a direct comparison with our formulation. Nevertheless, it is designed to extract
R_B values of the state-of-the-art HBTs and yield to extractions in an interesting range of values. The Vanhoucke method requires a forced emitter currents quite higher than those adopted by our method but the results always fall in the R_B range achieved for $V_{CB} > V_{CBZ}$ through our approach. In particular, a R_B=40.7 Ω is extracted for SBZ2 device and R_B=22 Ω for SCA1 (see Fig. 4.6 and Fig. 4.7, respectively).
Finally, the reliability of the method was validated by putting an intentional resistor R_{Bext}=100 Ω in series with the base terminal; the extracted R_B should be the sum between the external resistor R_{Bext} and device base resistance. This measure has been applied to 2 different devices. Fig. 4.12 and Fig. 4.13 show clearly that the internal contribute is shifted upward by exactly the expected amount.

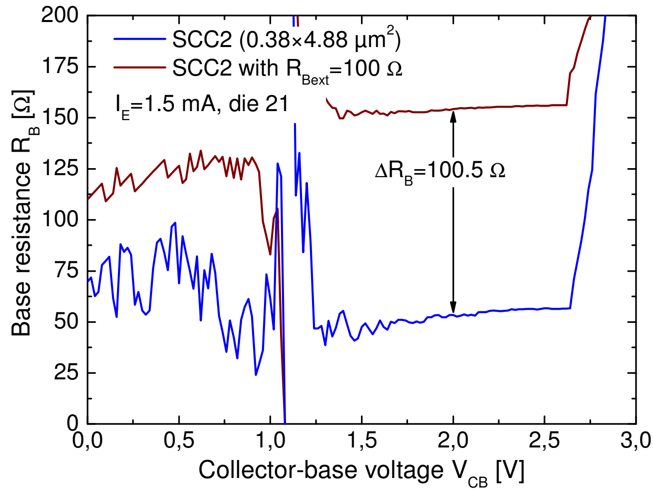

Fig. 4.12 Base resistance R_B with and without an extra resistance on the base as a function of collector-base voltage V_{CB} for STM device SCC2.

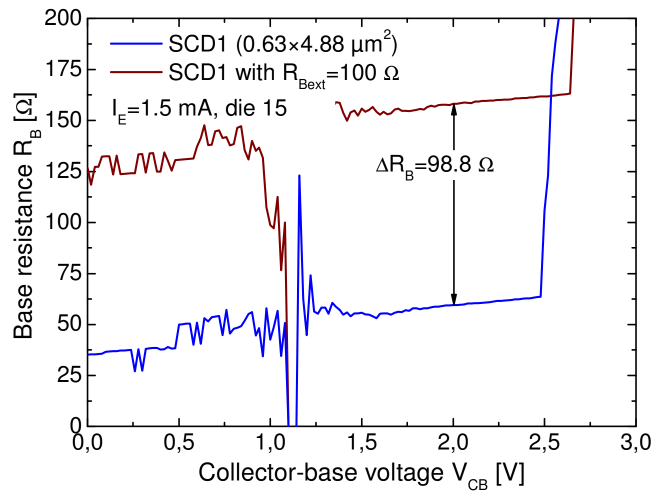

Fig. 4.13 Base resistance R_B with and without an extra resistance on the base as a function of collector-base voltage V_{CB} for STM device SCD1.

Chapter 5

A in-house pulse generator for isothermal I-V measurements

A reliable experimental characterization of semiconductor devices is commonly requested for several purposes, e.g., model parameters extraction, process diagnostics, and safe operating area definition. However, measurements are often performed under dc bias conditions, which may give rise to a significant self-heating and a consequent distortion of the I–V curves in comparison to the isothermal case. Besides, electrothermal effects – traditionally associated to high-power devices – are nowadays exacerbated also in state-of-the-art HF transistors, like SiGe HBTs and silicon-on-glass BJTs. This is ascribable to a twofold reason: (i) the self-heating thermal resistances of these devices have grown to several thousands of K/W due to the scaling process and to the low thermal conductivity of the materials surrounding the active device region [59], [60]; (ii) the operating point is shifted to higher current densities to improve frequency performance, thus increasing the power density consumption.
Advanced equipments suited to bias transistors with short pulse widths (even lower than 1 μs) are therefore needed to annihilate self-heating during the measurement process, thus ensuring isothermal conditions [61], [62]. Unfortunately, the cost of commercial curve tracers including this feature may exceed 100 k$. This has motivated a relevant effort to develop cheaper, yet reliable, systems [63]-[65]. In this scenario, an advanced in-house pulse system was designed and realized in order to characterize, by means of isothermal conditions, state-of-the-art SiGe HBTs of interest. This Chapter deals with the description of the different sections of the system and with its specifications. Furthermore, a set of measurements applied to various transistor typologies is shown.

5.1 The architecture

The in-house general-purpose pulse generator is composed by different sections. The block diagram is shown in Fig. 5.1.

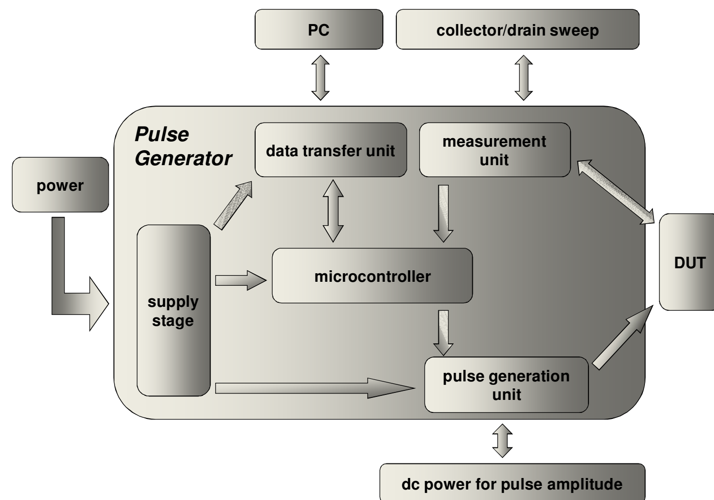

Fig. 5.1 Schematic block diagram of the proposed circuit.

The circuit is based on a microcontroller unit (MCU) and allows the setting (via firmware) of the period and duty-cycle of the voltage pulse train; in addition, it is equipped with a section based on an instrumentation amplifier for on-board measurements. The sections of the realized pulser are described in detail in the following paragraphs.

5.1.1 The Supply stage

The system requires different voltages for the dc-supply of the on-board integrated circuits. In particular:

- 3.3 V and 2.5 V for the MCU;

- 5 V for the Max232;
- 15 V for the half-bridge driver;
- ±15 V for the instrumentation amplifier of the measurement unit.

The supply stage is based on an external 12 V power supply with a maximum output current of 500 mA. LDO regulators are used to generate 2.5V, 3.3V e 5V. These components require the addition of input/output terminal bypass capacitors to improve ripple rejection. The ±15 V supply is devised to DC/DC low-power converter in package SIP5. They don't need of external components allowing a more simple connection on board. The components used to generate the requested voltages are listed in Tab. 5.1.

I.C.		Output voltage
LM7805	Fairchild Semiconductor	5 V
LM1117T-2.5	National Semiconductor	2.5 V
LMS1585ACS3.3	National Semiconductor	3.3 V
TMA1215S	Traco Power	+ 15 V
TMA1215D	Traco Power	±15V

Tab. 5.1 Integrated circuits used for the supply stage.

Fig. 5.2 shows a 3D visualization of the supply stage.

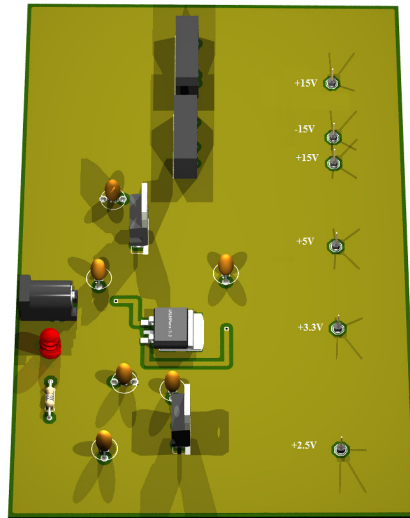

Fig. 5.2 3D visualization of the supply stage.

5.1.2 The Microcontroller unit

The control unit is based on the Microchip 28-pin MCU dsPIC33FJ16GS402, which represents the core of the system. It is a High-Performance 16-bit Digital Signal Controller that includes a high-speed PWM module, a high-speed 10-bit ADC, an UART serial peripheral, and a 2-Kbytes data SRAM. The developed firmware of the MCU coordinates the measurement flow by means of the following steps:

- generation of the PWM signal to send to the half-bridge driver as highlighted in Fig 5.3 (this signal has the same width T_{ON} and period T as the desired pulse);
- acquisition – via the 10-bit ADC – of a prescribed number of samples (programmed by firmware), which are stored in the internal SRAM (see Section 5.1.4);

- data transfer through the UART peripheral (see Section 5.1.5).

The driver chosen to bias the pulse generation unit is the IR2183 of the International Rectifier. The IR2183 is high voltage, high speed power MOSFET driver with dependent high and low side referenced output channels. This component provides a floating channel useful to drive an N-channel power MOSFET in the high side configuration which operates up to 600 volts. This feature is widely exploited for the pulse generation.

5.1.3 The pulse generation unit

The pulse generation is done by a power MOS with high breakdown voltage and low on-resistance so as to satisfy the desired pulse specifications; in particular, the STP22NF03L transistor was selected and mounted on the prototype. The drain of this device is connected to an external voltage supply, while the gate-source voltage V_{GS} is provided by the half-bridge driver as shown in Fig. 5.3.

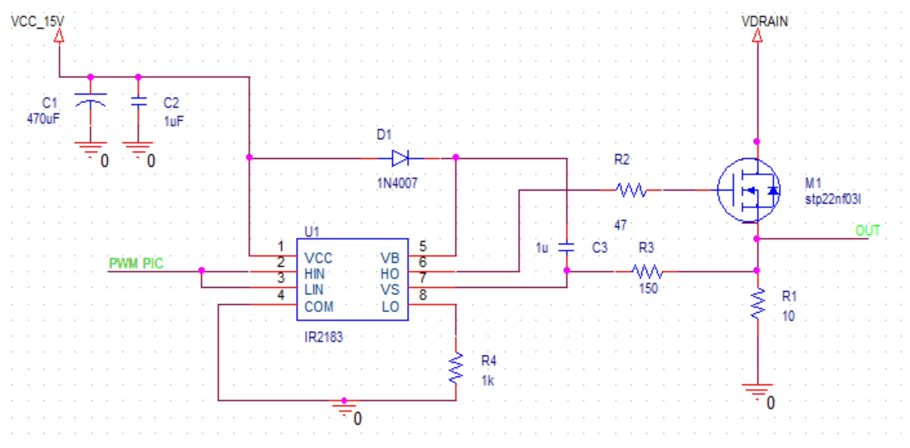

Fig. 5.3 Pulse generation unit schematic.

As a result, the MOS is switched on and off accordingly to the period and duty-cycle of the PWM signal. In particular, the positive V_{GS} value is high enough to push the transistor into deep linear mode, thereby ensuring a low voltage drop between drain and source. This gives rise to a train of pulses on the source terminal, with amplitude slightly lower than the supplied drain voltage (due to the V_{DS} drop), and period and duty-cycle programmed via firmware. However, in order to know the correct amplitude of the pulse train (V_{drain} - V_{DS}), the amplitude can be measured on-board by the 10-bit ADC of the MCU.

5.1.4 The measurement unit

The proposed system, besides generating a pulse train with assigned features, is also equipped with an ad-hoc unit – based on the instrumentation amplifier INA110KP – which can be enabled for on-board measurements. The operating principle of this block can be described as follows. A known resistance R_C is connected between an external voltage supply and the collector/drain of the DUT, whose base/gate is biased with the pulse train as shown in Fig. 5.4 (V1 signal represents the generated pulse train).

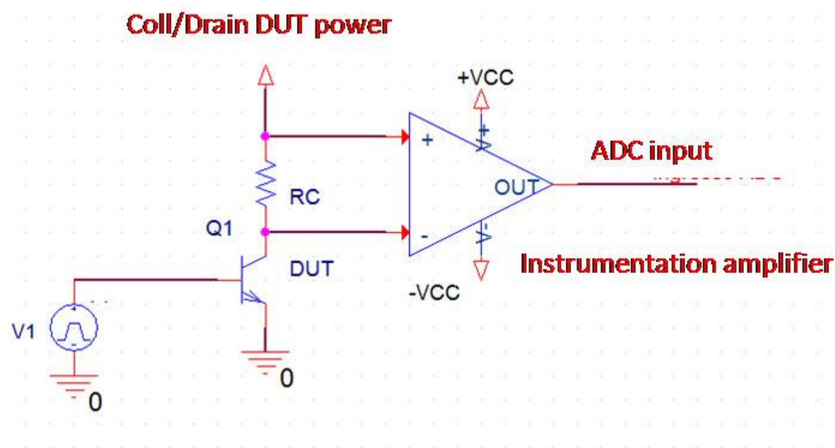

Fig. 5.4 Measurement unit schematic.

The input pins of the INA100KP are connected in parallel to R_C to sense and amplify the voltage drop due to the collector/drain current as the device is turned on by the pulses; the output pin is connected to a channel of the 10-bit ADC of the MCU (a 3.3 V Zener diode is used to protect the analog part of the ADC channel). Moreover, another ADC channel is devised to measure the supply voltage. In conclusion, both the voltage and current corresponding to each point of an I–V characteristic are determined and subsequently stored in the internal SRAM.

The measurement unit is conceived to sense the current within a wide range of values (from 10 nA to 1 A), which is accomplished as follows. A group of 10 different resistors are available, which have a terminal tied to the external voltage supply and the other floating; R_C is selected among them consistently with the current span to be investigated by connecting the floating terminal to the collector/drain of the DUT through a jumper. In principle, the resistance R_C can be also given by a selected combination of paralleled resistors belonging to the aforementioned group.

The trigger for the ADC acquisition is represented by the rising edge of the PWM generated by the MCU with a delay programmed via firmware. This allows safely performing the measurement during the pulse width T_{ON}.

Lastly, it must be remarked that the measurement unit can be kept fully deactivated as the system is exploited only to generate the pulse train while the data acquisition is demanded to external instruments (off-board mode). However, in this case the synchronization between pulse train and data acquisition becomes quite cumbersome.

5.1.5 The data transfer unit

At the end of the programmed number of acquisitions, a firmware routine coordinates the data transfer via the UART peripheral. The Max232 integrated circuit is employed to adapt the voltage levels to the RS-232 protocol.

5.2 Specifications

The entire pulse generator was completely designed and assembled in house. The PCB prototype of the system is shown in Fig. 5.5.

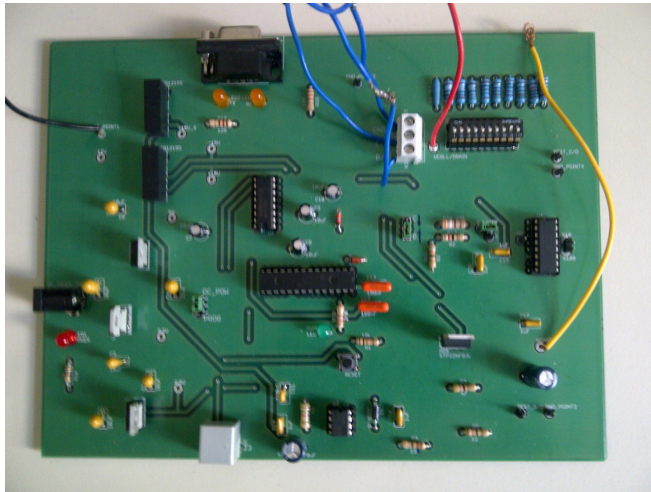

Fig. 5.5 Picture of the realized prototype.

The selection of all the components of the system was made upon accounting for the characterization of the devices of interest for the research group. In particular, state-of-the-art HBT devices with a very high junction-to-ambient thermal resistance required a minimum pulse width lower than 1 us.
The main pulser specifications are reported in Tab. 5.2.

Specification	Value
Maximum pulse amplitude	15 V
Current range	10^{-8} A ÷ 1 A
Minimum pulse width	400 ns
Minimum duty cycle	0.074%
Maximum duty cycle	100%
Start-up time	10 μs
Maximum number of samples	480
Maximum number of sample averages	120

Tab. 5.2 Specifications of the proposed pulser.

The minimum pulse width is 400 ns as highlighted in Fig. 5.6.

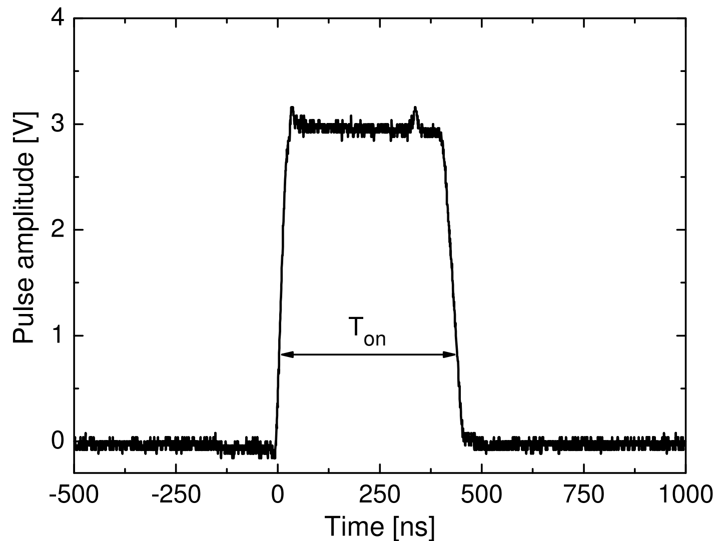

Fig. 5.6 Generated pulse with amplitude of 3 V and width T_{ON} of 400 ns.

The realized experimental system is capable of state-of-the-art performances allowing the characterization of most of the modern circuits and devices and, in spite of the much lower cost, it can be considered as a trustworthy alternative to advanced commercial curve tracers.

5.3 Measurements results

The proposed pulse generator was used to experimentally characterize various device categories, i.e., in-package power Si BJTs and MOS transistors, as well as on-wafer SiGe HBTs for RF applications. A comparison with the corresponding dc data – measured through an HP4142B parameter analyzer – was also carried out in order to emphasize the reduction in self-heating effects achieved with the pulsed bias.

First, the constant-V_{BE} I_C–V_{CE} characteristics of the commercial packaged 2N3415 NPN power BJT (featuring BV_{CEO}=25 V, I_{Cmax}=500 mA, and junction-to-ambient thermal resistance

R_{TH}=200°C/W) were measured by applying the pulse train to the base terminal and sweeping the collector voltage by means of an external dc voltage source. In particular, the pulsed characteristics were obtained by varying the width T_{ON} of the applied pulse for a period T=100 μs (i.e., by varying the duty-cycle). Fig. 5.7 plainly illustrates that a reduction in T_{ON} allows increasingly counteracting the self-heating impact on the curve slope induced by the well-known positive temperature coefficient (TC) of the collector current [66]. In particular, it is found that T_{ON}<10 μs (i.e., duty-cycle <10%) is enough to achieve isothermal conditions. For the sake of clarity, the common-emitter configuration adopted for this analysis is also depicted in the figure inset.

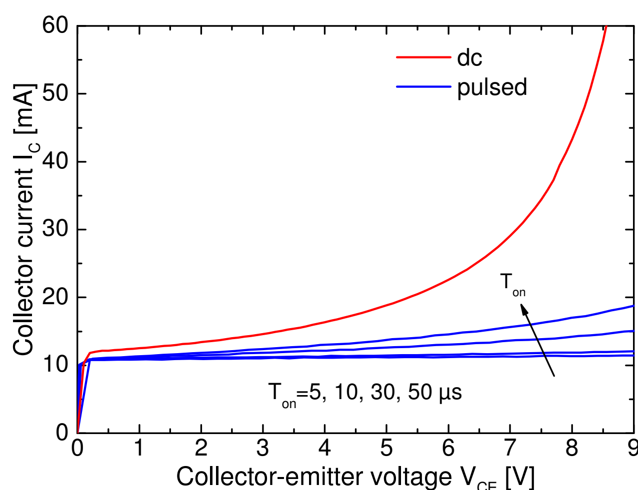

Fig. 5.7 Experimental I_C–V_{CE} characteristics of a 2N3415 BJT measured at V_{BE}=0.7 V under pulsed conditions for different pulse widths (blue lines), along with the corresponding dc curve (red).

A curve family obtained by varying V_{BE} is shown in Fig. 5.8; all the isothermal characteristics were measured by applying a pulse train with T_{ON}=5 μs and T=100 μs to the base.

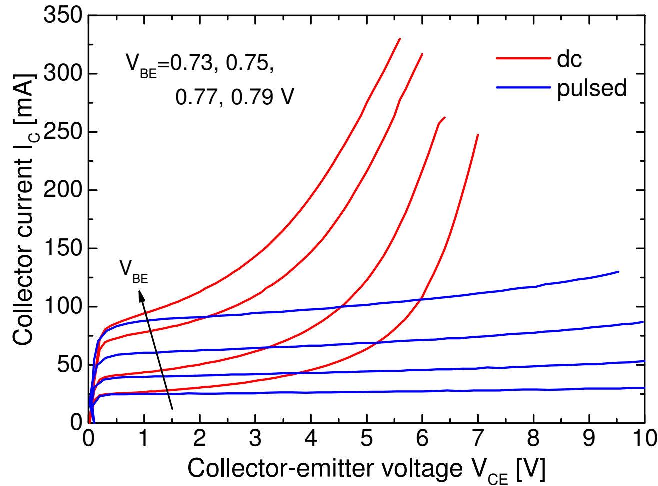

Fig. 5.8 Experimental dc (red lines) and pulsed (blue) output characteristics of a 2N3415 BJT for various V_{BE} values. The pulsed curves were obtained with T_{ON}=5 µs and T=100 µs.

Fig. 5.8 shows how the proposed pulse system is able to capture isothermal condition in spite of dc-tracer.

The proposed system allows on-board measurements also for on-wafer transistors. As an illustrative case-study, state-of-the-art SiGe:C HBTs featuring f_T/f_{max}=260/350 GHz [2] were experimentally analyzed. Fig. 5.9 reports both the dc and pulsed I_C–V_{CE} characteristics of a device with high R_{TH} (≈5000 K/W). Again, the pulsed curves were obtained by considering a pulse train with T_{ON}=5 µs and T=100 µs, for which self-heating is nearly eliminated; it should be noted that in this case the current increase observed at high V_{CE} values is induced by weak avalanche effects (BV_{CBO} was measured to be about 5 V).

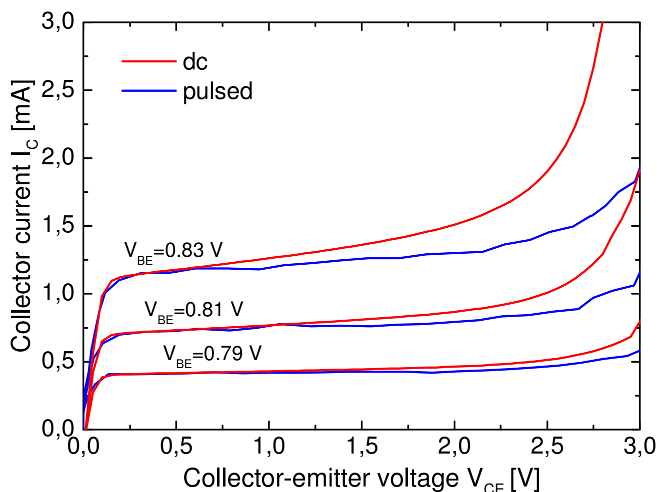

Fig. 5.9 Experimental dc (red lines) and pulsed (blue) I_C–V_{CE} characteristics of a SiGe:C HBT for various V_{BE} values. The pulsed curves were obtained with T_{ON}=5 µs and T=100 µs.

Fig. 5.10 reports the I_D–V_{DS} characteristics measured for the commercial packaged BS170 NMOS transistor (characterized by V_{TH}=2.1 V, BV_{DS}=60 V, I_{Dmax}=500 mA, R_{TH}=150°C/W) at different gate-source voltages V_{GS}. A pulse train with T_{ON}=10 µs and T=100 µs was found to be suited to guarantee isothermal conditions. A close inspection of the curves plainly confirms that the TC of the drain current I_D reverses its sign by increasing V_{GS}, which can be explained as follows. The thermal behavior of a MOS transistor is related to the temperature dependence of threshold voltage V_{TH} and channel mobility µn. Both these key parameters decrease with increasing temperature. However, the influence on the drain current is different: the reduction in V_{TH} leads to a positive TC, whereas the µn lowering entails a negative TC. At low V_{GS} (low I_D) the first effect prevails, while the second dominates at high V_{GS} (high I_D) [67], [68]. The proposed system allows also concluding that the device is weakly subject to the (merely electrical) channel modulation effect, as can be evinced by the low slope of the isothermal characteristics.

The proposed system was also employed as a mere pulse generator for the off-board monitoring of the transient thermal impedance evolution of on-wafer multi-finger GaN HEMTs [69].

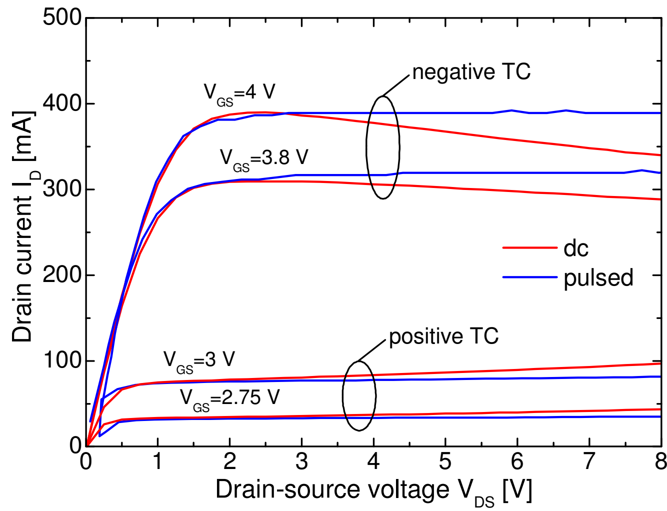

Fig. 5.10 Experimental dc (red lines) and pulsed (blue) I_D–V_{DS} characteristics of a BS170 NMOS for various V_{GS} values. The pulsed curves were obtained with T_{ON}=10 µs and T=100 µs.

Conclusions and outlook

The main focus of this thesis was the definition of the Safe Operating Area for state-of-the-art of advanced SiGe heterostructure devices.
The pinch-in, that is one of the causes of reduction of SOA, has been studied and the onset of the phenomenon has been highlighted by means of on-wafer measurements. A two-dimensional theoretical analysis of bipolar transistor operation under pinch-in regime has been presented. This model describes the current crowding effect occurring when the device is biased above the open-base breakdown voltage BVCEO. The defined boundary value problem was numerically solved by the finite element software package COMSOL. The emitter resistance contribution and high-injection effects have been also included in the model. In addition, for the first time, the physical origin of instability phenomena occurring under common-base operating conditions has been clarified.
In order to define the limit of SOA for state-of-the-art of advanced SiGe HBT, a wide characterization of STM and Infineon devices has been performed in our laboratories.
A very critical parameter to extract for this kind of devices is the base resistance. Focusing of the current above the open-base breakdown voltage yields to an increase of this parameter that becomes bias-dependent. All published works do not include this dependence except one method that is inapplicable to modern SiGe HBT. An improved dc method to experimentally extract the biasing-dependent base resistance in SiGe HBT devices has been proposed. The proposed method is suitable for any bipolar transistor category. The reliability of the new procedure has been successfully demonstrated by means of on-wafer measurements.
DC measurements influence the temperature of the device. This dependence can be avoided by biasing the device in a pulsed way. A novel general-purpose pulse generator has been designed, realized and characterized. The system is provided with a section devised for on-board measurements, which allows a reliable synchronism between pulse train and data acquisition. The versatility of the pulser has been demonstrated by obtaining isothermal I–V characteristics for different

types of transistors, including on-wafer SiGe:C HBTs with very high thermal resistances.

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