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DOTTORATO DI RICERCA IN
INGEGNERIA ELETTRONICA E DELLE TELECOMUNICAZIONI

AGILE ALL-DIGITAL CLOCK GENERATORS WITH SPREAD-SPECTRUM CAPABILITIES IN 28nm TECHNOLOGY

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Introduction

Electromagnetic interference (EMI) is an energy disturbance that affects the performance of electrical/electronic circuit due to radiated electromagnetic fields or conducted power source. In high speed digital system, nowadays, the EMI reduction has become an essential part of design considerations. In fact, the high-speed clocks employed in digital chips radiate electromagnetic noise over a wide frequency band, which may interfere the performance of the equipment that generates it or other electronic equipments in proximity to it. The EMI also increases noise and leads to bad jitter performance of the integrated circuit (IC).

Regulatory agencies, such as FCC in the United States and the CISPR have established the EMI measurement standards, which prescribe the maximum allowable emission levels and prescribe also precise measurement procedures in order to evaluate compliance with regulations.

Many method for reducing the EMI level have been developed in the last twenty years. The shielding is a traditional method for preventing EMI emissions. This method consists in covering, fully or partially, the emission locations with grounded conductive shields. Unfortunately, for many system, the shielding technique is the least desirable method for reducing EMI emissions.

The line filter is another well-known method that allows to reduce the EMI level. In this case the EMI level can be mitigated with the help of a low pass filters in order to eliminate the high-order harmonics. In particular, this method reduces the rise and the fall times of the signal in order to reduce the radiated EMI. However, in the high speed system the filtering reduce critical the setup and hold margins, increases the amount of signal overshoot. This result in a worsening of

the jitter performance. Moreover the line filter method is not systemic and only produces a limited, local effect.
The spread spectrum clocking (SSC) is an established, effective and efficient technique to reduce the radiated EMI. This method allows to reduce the level of EMI of digital circuit by intentionally sweeping the frequency of the clock signal (frequency modulated) within a certain frequency range in order to evenly spread the energy of each clock harmonic over a given bandwidth, reducing in this way the peak power level of radiated electromagnetic interference.
In this work, a novel all-digital Spread Spectrum Clock Generator (SSCG) prototype is presented in all its aspects: design, simulation and post-fabrication measurements. The architecture and the first post-layout simulation results of a second new all-digital SSCG is presented in the second part of this thesis.

The thesis is structured as follows:

- The Chapter 1 deals with the SSC techniques for digital circuits. In particular, the performances achievable with continuous frequency modulated signals and with discontinuous frequency modulated signals in spread spectrum applications are presented. The SSC is commonly implemented with ΔΣ phase locked-loop (PLL). The most recent approaches implement SSCG by using all-digital PLL or frequency locked-loops (FLL) or ad hoc all-digital techniques. A brief description of such approaches is discussed in the second part of this chapter.

- The design of an all-digital Spread Spectrum Clock Generator (SSCG) prototype is presented in Chapter 2. This circuit is based on an all-digital architecture which do not require any loop to implement frequency synthesis and spreading. The developed SSCG is realized by using a design flow completely based on standard cells simplifying design and porting in new technologies, and is able to perform both discontinuous frequency modulation or complex modulation profiles.
  In the first part of this chapter the whole SSCG architecture is explained in detail. Afterwards, the circuit sizing details are given and the major components of deterministic jitter are

discussed. Finally, the on-chip measurement results are reported and are compared with the state of the art.

- The implementation of a second novel all-digital SSCG with injection locking digitally controlled oscillator (DCO) is presented in Chapter 3. The circuit allows the clock multiplication and is able to perform the injection locking technique in order to reduce the jitter of the circuit.
  At first, a detailed description of the whole SSCG architecture is discussed. Afterwards, the circuit implementation details are given and the major sources of deterministic jitter are also discussed. Finally, the first post-layout simulation results are presented.

Chapter 1

Spread Spectrum Clocking techniques

Spread-spectrum clocking (SSC) [1], also known as “clock dithering” or “clock frequency modulation” is a well known approach to reduce the electromagnetic interference level (EMI) produced by digital chips. This method generates a clock signal with a frequency that is intentionally swept (frequency modulated) within a given frequency range with a predetermined modulation waveform (modulation profile). In particular, SSC allows us to spread the energy of each clock harmonic over a certain bandwidth in order to mitigate. the peak power level at each harmonic.

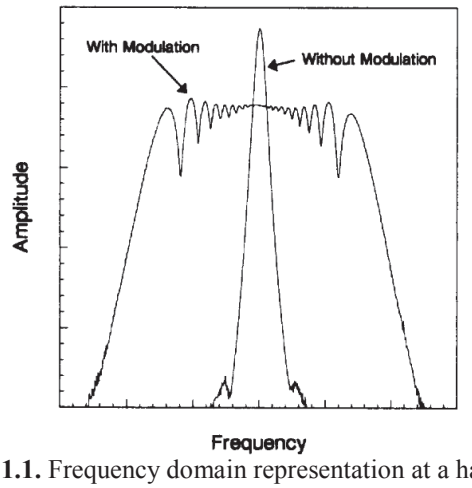

Figure 1.1. Frequency domain representation at a harmonic of a trapezoidal clock signal with and without SSC [1].

This is demonstrated in figure 1.1, where a harmonic of a clock signal with and without spreading is shown. SSC is nowadays used in a

number of applications, like high-speed serial links [2],[3], high-performance digital circuit [4]-[8] and switching power converters [9]-[12].
The peak power level reduction, also known as modulation gain, generally depends on the frequency deviation (modulation depth), modulation frequency (f_m) and on modulation profile (modulation waveform). The procedures to evaluate the peak power level of frequency-modulated waveforms are prescribed by the EMI measurements standards [13]-[16]. Please note that these procedures require the analysis of the signal with a spectrum analyzer in a swept-frequency mode with a prescribed resolution bandwidth (RBW) and peak-type detector.
The spectrum of frequency-modulated signal is studied in [1] by using the Fourier series. However, it is generally difficult to obtain an analytic form of a frequency modulated clock signal by using the Fourier transform. Moreover, the Fourier analysis does not take into account the combined effect of the spectrum analyzer RBW and the peak-type detector. This results in a remarkable difference between the experimental data and the spectrum mathematically obtained through Fourier transform. However, this property is lost when the effect of the detector and spectrum analyzer RBW are considered.
An empirically derived optimal modulation waveform, when the spectrum analyzer RBW and the peak-type detector are considered, is presented in [17].
An analytical and efficient method for determining the spectrum of modulated signal by considering the effect of the spectrum analyzer RBW and the detector is presented in [18] and [19]. In particular, in these papers, it is theoretically demonstrated for the first time that the optimal modulation frequency is close to the spectrum analyzer RBW, when the peak-type detector is taken into account. Moreover, in [18] and [19] is shown that the optimal modulating waveform can be obtained as a solution to a simple differential equation. However, following this approach the optimal waveform depends on the spectrum analyzer filter shape. Therefore, if different instruments with slightly different filter shape are used then a slightly different results can be observed. Furthermore, the basic formulae for analyzing a frequency modulated clock signal and its spectrum derived in [18] and [19] assumes the continuity of the modulating waveform and provides only a coarse approximation in the case of waveforms with discontinuous frequency modulation.

In [20] the analysis of [18] and [19] is extended to the discontinuous frequency modulation. Therefore, in this paper, for the first time the peak-level reduction of the spectrum achievable with discontinuous frequency modulated signal, in spread spectrum clocking applications, is investigated. In particular, in [20] is shown that the discontinuous frequency waveforms can achieve higher modulation gains in comparision to continuous frequency signals. In addition, the spectrum of a discontinuous frequency modulated signals, measured by a spectrum analyzer with a given RBW, is obtained in closed form. The optimal discontinuous frequency modulated waveform is, in this paper, also obtained, under some assumptions, as the solution of a first-order differential equation.
The analysis presented in [20] is very important since the recent all-digital SSC generators [5],[7] allow the synthesis of the clock signals with a discontinuous frequency behaviour.
This Chapter is organized as follows. The section 1.1 recalls the results of [18],[19] and [20] and shows the simulation results in which the discontinuous frequency modulation allows an improvement of the modulation gain with respect the continuous frequency modulations. Afterwards, a brief introduction to the state-of-the-art of the SSC generators is presented in the section 1.2.

1.1 Spectrum of Frequency Modulated Signal

1.1.1 Continuous Frequency Modulation

Let a function *u(t)* represent the waveform of a clock signal with a constant fundamental frequency f_0. This signal can be written by using the Fourier series as:

$$u(t) = \sum_{k=-\infty}^{+\infty} \frac{I_{0k}}{2} \cdot \exp[j2\pi k f_0 t] \tag{1.1}$$

The waveform of the frequency-spread clock signal $u_s(t)$ is obtained by replacing the variable t with the variable t' as follows:

$$u_s(t) = u(t') \tag{1.2}$$

where:

$$t' = t + \frac{\delta}{f_m}\int_{-\infty}^{f_m t} V(\tau)d\tau \tag{1.3}$$

and $V(\tau)$ is a periodic function of unity period with values [-1,+1]. By using the equations (1.2) and (1.3) the signal $u_s(t)$ can be written as:

$$\begin{aligned} u_s(t) &= \sum_{k=-\infty}^{+\infty} \frac{I_{0k}}{2} \cdot \exp\left[j2\pi k f_0 \left(t + \frac{\delta}{f_m}\int_{-\infty}^{f_m t} V(\tau)d\tau \right) \right] \\ &= \sum_{k=-\infty}^{+\infty} \frac{I_k(t)}{2} = \frac{I_{00}}{2} + \sum_{k=1}^{+\infty} \mathrm{Re}\left[I_k(t) \right] \end{aligned} \tag{1.4}$$

Therefore, the instantaneous frequency $f(t)$ of this waveform is given by:

$$\begin{aligned} f(t) &= \frac{1}{2\pi}\frac{d}{dt}\left[2\pi f_0 \left(t + \frac{\delta}{f_m}\int_{-\infty}^{f_m t} V(\tau)d\tau \right) \right] \\ &= f_0(1 + \delta V(f_m t)) \end{aligned} \tag{1.5}$$

By looking the equation (1.5) note that δ and f_m correspond, respectively, to the relative frequency deviation ($\delta = \Delta f / f_0$) and to the modulation frequency of the frequency-spreaded clock waveform.
In this section the possible frequency overlapping effect of the modulated spectrums of neighbour harmonics is neglected, assumption that is correct when $k \cdot \Delta f << f_0$. Therefore, only the spectrum of a single modulated harmonic $I_k(t)$ is analyzed.
The modulation gain (Gain) is defined as follows:

$$Gain \equiv \frac{I_{0k}}{\max\left[S(f_c) \right]} \tag{1.6}$$

where I_{0k} and max$[S(f_c)]$ are, respectively, the amplitude of the un-modulated harmonic and the peak value of the spectrum $S(f_c)$ of a frequency modulated harmonic $I_k(t)$.
The spectrum $S(f_c)$ is the spectrum measured by a swept-frequency spectrum analyzer in a peak-hold mode (see figure 1.2), in according to the EMI measurements standards [13]-[16].

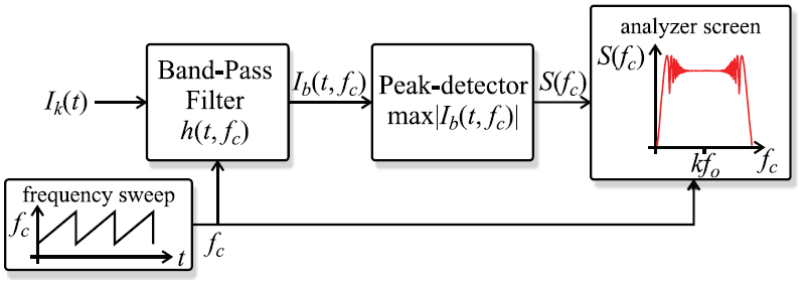

Figure 1.2. Model of a swept-frequency spectrum analyzer in a peak-hold mode.

Figure 1.2 shows the model of a swept-frequency spectrum analyzer in a peak-hold mode. It is realized by using a band-pass filter with impulse response $h(t,f_c)$ centered around the frequency f_c, followed by a peak detector. The filter impulse response $h(t,f_c)$ can be written as:

$$h(t, f_c) = h_0(t) \cdot \exp\left[j2\pi f_c t \right] \tag{1.7}$$

where $h_0(t)$ is a low-pass impulse response with a 3dB bandwidth RBW. The parameter RBW correspond to the so-called RBW of the spectrum analyzer. The output signal of the filter can be written as:

$$I_b(t, f_c) = \int_{-\infty}^{+\infty} I_k(t-\tau) \cdot h(\tau, f_c) d\tau \tag{1.8}$$

The peak-detector evaluates the maximum absolute value of $I_b(t,f_c)$, named $S(f_c)$. The spectral component $S(f_c)$ is plotted by the spectrum analyzer at frequency f_c. In [18], the criterion bandwidth is defined as:

$$B_{sw} \equiv \left(4k\Delta f \cdot f_m \right)^{1/2} \tag{1.9}$$

In [18] and [19], it is demonstrated that if RBW>>B_{sw} then no reduction of the peak spectral components can be obtained. However, in our applications of interest that is the frequency-spreading applications, the condition RBW<<B_{sw} can be considered valid. In [18] and [19] this hypothesis results in an approximate expression of the output of the band pass filter in figure 1.2:

$$I_b(t,f_c) \cong \sum_n \left(-jkf'(t_n)\right)^{-1/2} h\left(t-t_n,f_c\right) I_k\left(t_n\right) \qquad (1.10)$$

where t_n denotes the time at which the instantaneous harmonic frequency $k{\cdot}f(t)$ coincides with the filter center frequency f_c, that is $k{\cdot}f(t)=f_c$.

Let us consider an example of a clock signal that is frequency modulated with a simple triangular waveform. In particular, the output of the band-pass filter of figure 1.2 is schematically shown in figure 1.3 for two different center frequencies f_{c1} and f_{c2}. As you can see, the frequency f_{c1} is near to the harmonic center frequency $k{\cdot}f_0$. In this case, the impulse response $h((t-t_n,f_{c1})$ does not interfere with the successive impulse response $h((t-t_{n+1},f_{c1})$. This implies that the maximum value of $I_b((t,f_c)$ becomes independent of f_c and depends only on the maximum value of $h((t,f_c)$ and on the first derivative of instantaneous frequency $f(t)$.

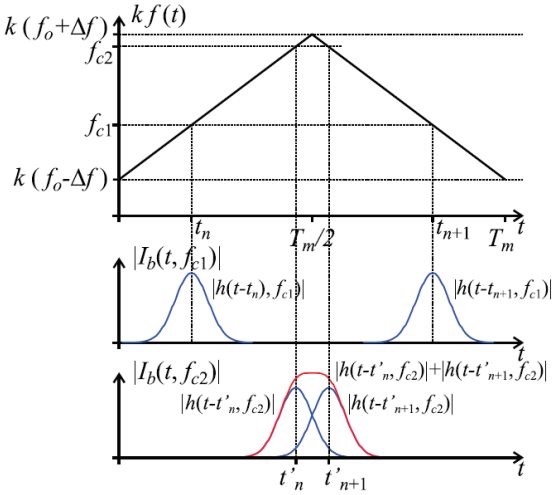

Figure 1.3. Schematic illustration of the output of the bandpass filter $I_b(t,f_c)$ considering a triangular modulation for two different filter center frequencies.

In [20] it is shown the simulated spectrum of the first harmonic (k=1) of a clock signal with a triangular modulation with Δf=5MHz, f_m=40KHz and RBW=100kHz (see figure 1.4). This figure shows that the spectrum is almost flat for f_c close to f_0 and the modulation gain in the middle is about 15.5 dB.
Instead, when a frequency f_{c2} is chosen close to the upper instantaneous harmonic frequency (k(f_0+Δf)) then the two successive pulses $h((t-t'_n,f_{c2})$ and $h((t-t'_{n+1},f_{c2})$ interfere with each other. This interference can be either constructive or destructive, depending on the particular value of f_{c2}. As you can see in figure 1.4, this implies an oscillating behaviour of the spectrum. In particular, when the two pulses interfere constructively, the maximum value at the output of the filter is increased and the modulation gain on the obtained spectrum reduces (e.g. in figure 1.4 it reduces to about 10.4 dB).

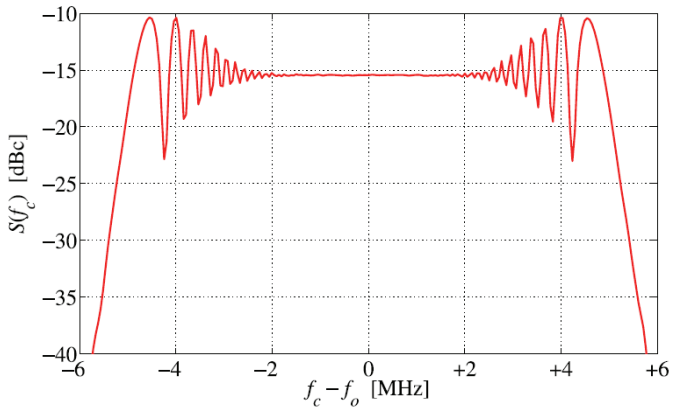

Figure 1.4. Spectrum $S(f_c)$ of the first harmonic (k=1) of a clock signal with a triangular modulation (Δf=5MHz, f_m=40KHz and RBW=100KHz) [20].

In [20] is also shown why, by intuition, the discontinuous modulation frequency can provide higher modulation gains with respect to the continuous modulation frequency signal. To clarify this point, the figure 1.5 shows a schematic illustration of the output of the band-pass filter considering, unlike the figure 1.3, a sawtooth modulating waveform that is a discontinuous waveform (around t=kT_m). As you can see in figure, the time distance between two successive pulses is independent of the particular filter center frequency f_c.
The figure 1.6 shows the simulated spectrum of a clock signal with a sawtooth modulation and the same value of $f'(t)$ with respect to the case of figure 1.3.

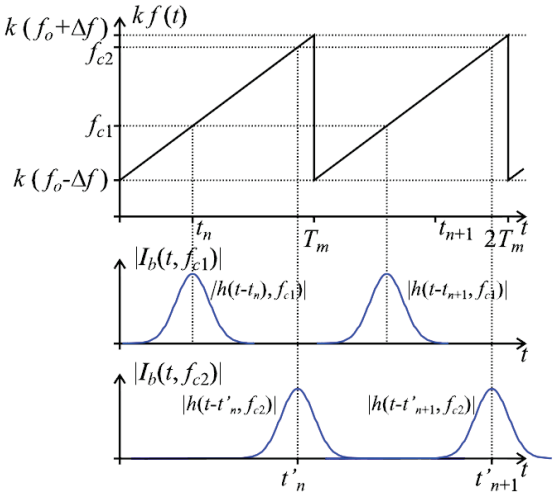

Figure 1.5. Schematic illustration of the output of the bandpass filter $I_b(t,f_c)$ considering a sawtooth modulation for two different filter center frequencies.

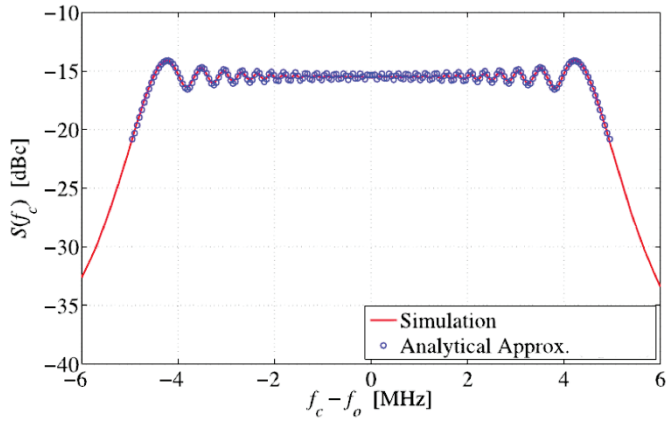

Figure 1.6. Spectrum $S(f_c)$ of the first harmonic (k=1) of a clock signal with sawtooth modulation (Δf=5MHz, f_m=80KHz and RBW=100KHz) [20].

The modulation gain is increases to about 14.1dB with respect to the modulation gain obtained by using a triangular modulation (10.4dB). However, this modulation gain value for the sawtooth modulation differs from the value predicted by using the equation (1.10). In fact, a non oscillating spectrum behaviour with a modulation gain close to 15.5dB is expected by using the equation (1.10). Therefore, the modulation gain predicted (≈15.5dB) by the (1.10) is higher than the simulated modulation gain (≈14.1dB) because an oscillating behaviour

of the spectrum. This oscillation depends on the discontinuity of the instantaneous modulating frequency. This discontinuity is not taken into account in (1.10).
The next section recalls the analytical approximation of the spectrum of discontinuous frequency modulated derived in [20].

1.1.2 Discontinuous Frequency Modulation

In the previous section, it was shown that the frequency discontinuity allows to avoid the constructive interference at the output of the band-pass filter. However, an oscillating behaviour of the spectrum caused by the discontinuity points has been observed too. This results in a worsening of the modulation gain. Therefore, in order to minimize the discontinuous frequency points, in [20] the signal of interest is the one described by (1.4) where *V(t)* is a continuous and monotonic function for $t \in [0,1]$:

$$\begin{cases} V(0) = -1 \\ V(1) = +1 \end{cases} \tag{1.11}$$

Thanks to the constraints of (1.11) the only discontinuous frequency points are the points $n \cdot T_m$. Therefore, the output of the band-pass filter (figure 1.2) can be written as:

$$I_b(t, f_c) = \sum_{n=-\infty}^{+\infty} \int_{nT_m}^{(n+1)T_m} I_k(\tau) \cdot h(t-\tau, f_c) d\tau \tag{1.12}$$

so thanks to the (1.11) the signal $I_b((t,f_c)$ is equal to a summation of integrals with continuous integrands.
In [20] the method of stationary phase [21]-[24] is used in order to compute each integral in (1.12). This method requires two conditions, the first one is the criterion bandwidth (see eq. (1.9)) while the second one can be written as:

$$k\Delta f \gg f_m \tag{1.13}$$

This condition is always verified in spread-spectrum applications. Assuming that the modulation function *V(t)* is monotonic and considering the previous two conditions, each integral in (1.12) can be approximated as:

$$\int_{nT_m}^{(n+1)T_m} I_k(\tau)\cdot h(t-\tau,f_c)d\tau$$
$$\simeq \frac{1}{\left(kf'(t_0)\right)^{1/2}} I_k(t_n)h(t-t_n,f_c)e^{j\pi/4}\cdot\Gamma(\delta t\sqrt{\pi kf'(t_0)}) \qquad (1.14)$$

where the function Γ(t) is:

$$\Gamma(t)\simeq 1/2\cdot\left(1+C\left[\sqrt{2/\pi}\cdot t\right]+S\left[\sqrt{2/\pi}\cdot t\right]\right) \qquad (1.15)$$

C(t) and *S(t)* are the well-known Fresnel integrals.
In (1.14) δt is equal to:

$$\delta t=\min[t_0,T_m-t_0] \qquad (1.16)$$

By substituting (1.14) in (1.12):

$$I_b(t,f_c)\simeq\sum_{m=-\infty}^{+\infty}\frac{1}{\left(kf'(t_0)\right)^{1/2}} I_k(t_n)h(t-t_n,f_c)e^{j\pi/4}$$
$$\cdot\Gamma(\delta t\sqrt{\pi kf'(t_0)}) \qquad (1.17)$$

where the function Γ accounts for the effect of the discontinuous frequency points. The peak detector computes the spectral component $S(f_c)$ that is the maximum value of the filter output $\max[I_b(t,f_c)]$. The spectral component $S(f_c)$ is computed when the pulses do not overlap each other. Since the pulses $h(t-t_n,f_c)$ are spaced by T_m and the duration of each pulse is about 1/RBW, the pulses not overlap when f_m<<RBW. Therefore, the spectral component can be written as:

$$S(f_c)\simeq I_{0k}\frac{1}{\left(kf'(t_0)\right)^{1/2}}\max[h_0(t)]\cdot\Gamma\left(\delta t\sqrt{\pi kf'(t_0)}\right) \qquad (1.18)$$

The good agreement between the analytical approximation of (1.18) and the simulation results is shown in figure 1.6.
In addition, in [20] the optimal discontinuous frequency modulation waveform is obtained numerically as the solution of a nonlinear, first order, boundary value problem with a Dirichlet boundary condition. Figure 1.7 shows the modulation gain obtained for different modulation techniques by varying f_m. In particular, the modulation gain is evaluated for Δf = 5MHz, RBW = 100 kHz and f_m is varied between 10 and 500 kHz.

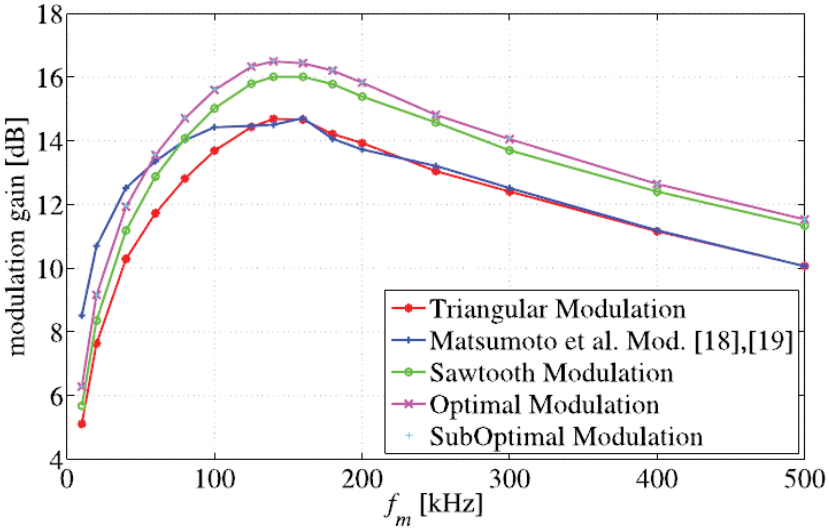

Figure 1.7. Modulation Gain for different modulations and modulation frequencies (Δf=5MHz, RBW=100kHz).

As you can see, the modulation gain increases with the modulation frequency as long as the f_m is lower than 100 kHz, in accordance with (1.18). When f_m is higher than 100 kHz then the condition f_m<<RBW begins to no longer verified. This implies that the equation (1.18) becomes progressively less accurate. For f_m>>RBW the spectrum analyzer filter does not have any effect on the spectrum. In this case, the Fourier analysis can be used to compute the spectrum of the frequency modulated clock signal and the modulation gain decreases with the f_m. Moreover, the figure 1.7 shows that for low f_m values the highest modulation gain is achieved by the continuous frequency optimal modulation [18],[19]. Instead, for high f_m values the highest modulation gain is obtained by the optimal discontinuous modulation derived in [20]. In fact, by increasing the modulation frequency, the

continuous modulation performances become severely limited by the pulses superposition effect.

The simulation result of figure 1.7 also shows that, for fixed frequency deviation Δf and RBW, the employment of discontinuous optimal frequency modulation allow to obtain the maximum modulation gain value, 16.5dB. This best modulation gain is 0.5dB and 2dB higher than the highest modulation gains achievable by using sawtooth modulation frequency and continuous optimal modulation frequency.

1.2 Spread Spectrum Clock Generator

Modern system-on-chip integrates several modules (e.g. CPU, graphics, memories, USB interfaces, I/O interfaces,....) working at different frequencies that can be dynamically varied to implement localized dynamic and frequency scaling. In particular, some modules require spread spectrum clocking to reduce the EMI level, while others modules (e.g. USB interfaces) need un-modulated clock signal with reduced jitter. The clock generators should fulfil all those requirements (frequency synthesis and spreading capabilities, low jitter).
The spread spectrum clock generators (SSCGs) are commonly implemented by using phase-locked loop (PLL) [25]-[28], frequency-locked loop (FLL) [8] or ad-hoc all digital techniques [4],[5],[7],[29]. Unfortunately, the wake-up time in a PLL/FLL architectures is limited by the loop locking-time. Moreover, PLL/FLL bandwidth limitation makes it difficult to implement triangular or Hershey-kiss modulation profiles and do not allow to produce discontinuous modulation (e.g. sawtooth) that result in additional EMI improvements. All-digital techniques, on the other hand, suffer from very large deterministic jitter.

1.2.1 PLLs/FLLs architectures

The PLL-based SSCGs architectures are reported in [25]-[28]. The all-digital digital clock generator core presented in [25] is shown in figure 1.8.

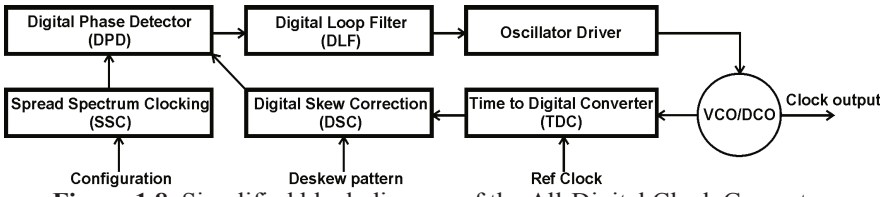

Figure 1.8. Simplified block diagram of the All-Digital Clock Generator Core proposed in [25]

A time-digital converter (TDC) is used as a phase detector in order to provide a digital word to the digital skew correction (DSC) logic. The

digital phase detector (DPD) allows to evaluate the phase error between the reference and the oscillator output by using the TDC output. The spread spectrum clocking is implemented within a PLL loop. In particular, the SSC is performed as a frequency modulation at the output of the oscillator. Figure 1.9 shows the block diagram of the SSC. As you can see, in the SSC block an arbitrary spreading operation is performed by adding the frequency command word to a digital modulation sequence.

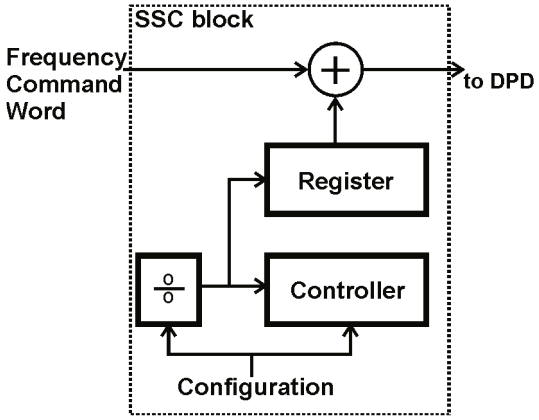

Figure 1.9 SSC block diagram [25].

The architecture proposed in [26] uses a fractional injection-locked oscillator. The injection locking is a well-know technique that allows to reduce the output jitter of clock generators.

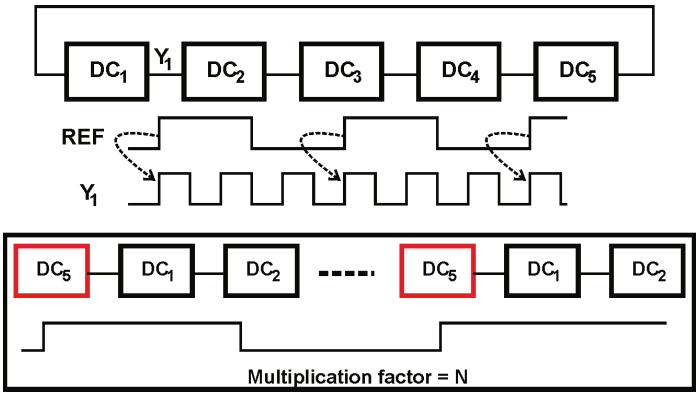

Figure 1.10. Conventional injection locking method.

The figure 1.10 shows the conventional injection locking technique. In this method the reference signal is shorted to the output of the delay

cell (DC), named reference-injected DC, in order to realign the output edge of the delay cell every reference period. The accumulated jitter from the VCO is, therefore, suppressed since the output edge of the delay cell has been realigned in the correct position. The drawback of this solution is that the output frequency can be changed only by integer multiplies of the reference frequency.
The solution of [26] allows to overcome this drawback. The figure 1.11 shows the fractional injection locking technique proposed in [26]. In this architecture, a ring oscillator with a multiphase output is used in order to allow the injection to an output that is a fractional multiple of the reference frequency. Therefore, the reference-injected delay cell is selected in according to the fractional value of the frequency control word. In figure 1.11, as an example, the injection-delay cell changes from DC_5 to DC_1 in order to obtain a fractional multiplication factor equal to N+1/5.

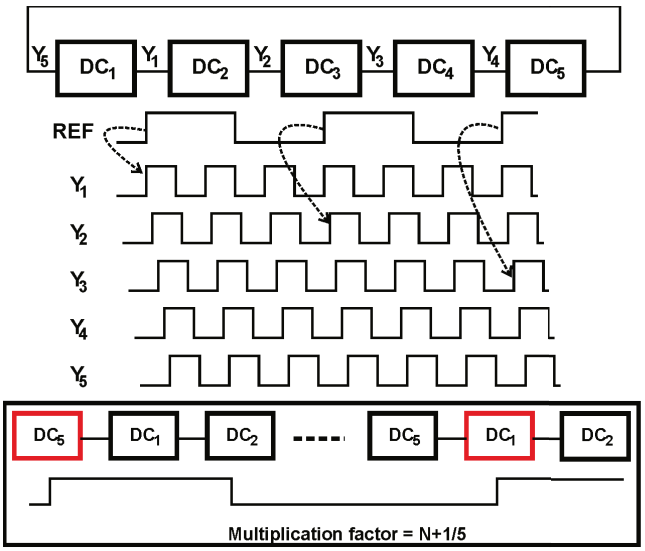

Figure 1.11. Fractional injection locking method of [26].

In [27] the spread spectrum clocking is performed by using a digital PLL with a high-frequency random modulation (RM). Figure 1.12 shows the architecture of [27]. A 3-phase clock is generated by using a digitally controlled oscillator (DCO). The frequency of the DCO is controlled by a digital code. The phase error (N_e) is evaluated by subtracting the output of the phase quantizer and the accumulated frequency control word. A digital loop filter (DLF) receives the phase

error and provides the DCO control signal. A pseudo-random binary sequence (PRBS) generator is used to generate the random sequence which is added to the DLF output.

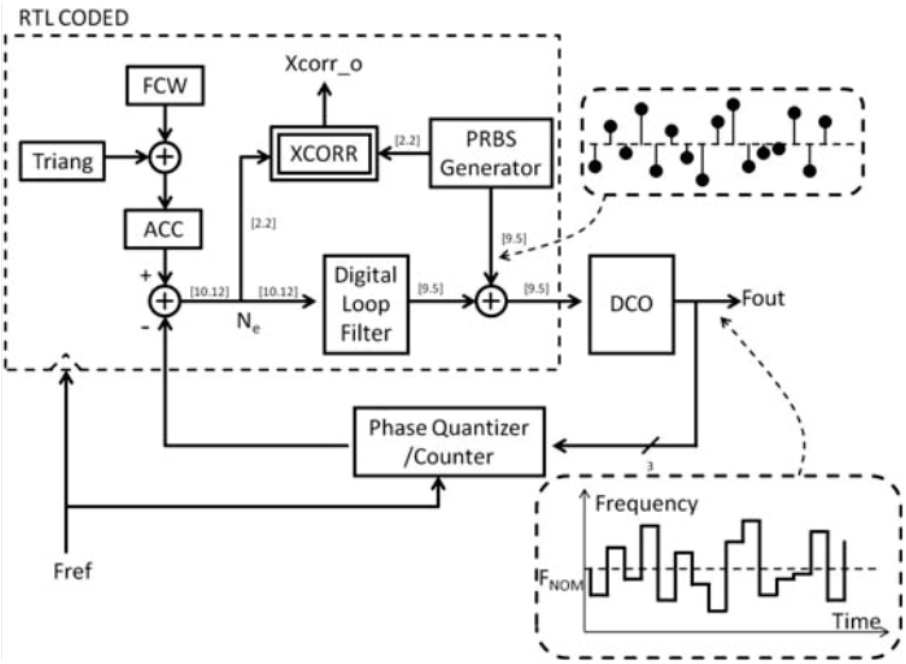

Figure 1.12. Random modulation digital PLL architecture proposed in [27].

In [28] a triangular-modulated SSCG with phase-rotating technique is proposed. This architecture allows to obtain an improved jitter performance and a lower design complexity with respect the ΔΣ-based technique.

The SSCG architecture presented in [8] is realized by using a frequency-locked loop (FLL) with a memoryless Newton-Raphson modulation profile. In this work, the profile generator performs the Newton-Raphson mathematical algorithm in order to generate the optimized nonlinear profile without the need for memory. This result in a reduction of area and power consumption.

1.2.2 Ad-hoc all-digital technique

The SSCGs implemented with ad-hoc all-digital techniques are presented in [4],[5],[7],[29]. The SSCG architecture proposed in [29] allows to perform both clock spreading and synthesis. An output frequency of 400MHz is obtained by parallelizing six generators. However, this circuit requires a careful design to avoid metastability and a complicate testing due to the use of many clock domains.
In [5] an all-digital SSCG is implemented by using a digital controlled delay line with a digital circuit to control it. The figure 1.13 shows a simple block diagram of this SSCG architecture. Note that the digital delay line is employed to modulate an input clock signal. In particular, the control digital circuit allows to increase or decrease the delay on a clock in order to obtain a modulated output signal.
This circuit can do up and down spread by modulating the reference frequency with a triangular waveform. However, in this circuit the frequency synthesis capability (output frequency multiplication or division) is not allowed and the maximum clock frequency is limited to 27MHz.

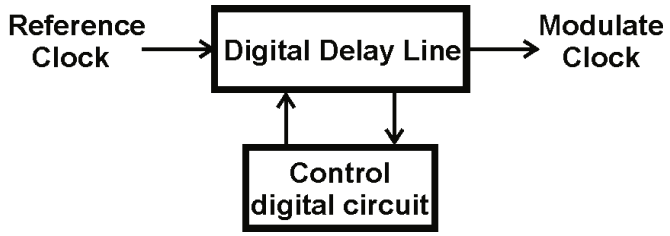

Figure 1.13. SSCG top-level diagram of [5].

The figure 1.14 shows the SSCG architecture proposed in [4]. As you can see, a delay cell array (DCA) is used in order to control the position of clock transitions with a triangular modulation profile. In particular, the delay of each individual delay cell is tailored to achieve the required period modulation. This architecture does not allow performing the frequency synthesis and operates at 100MHz. Moreover, the process, voltage and temperature (PVT) variations of the delay lines are not compensated. This result in a variation of the output waveform modulation depth with PVT.

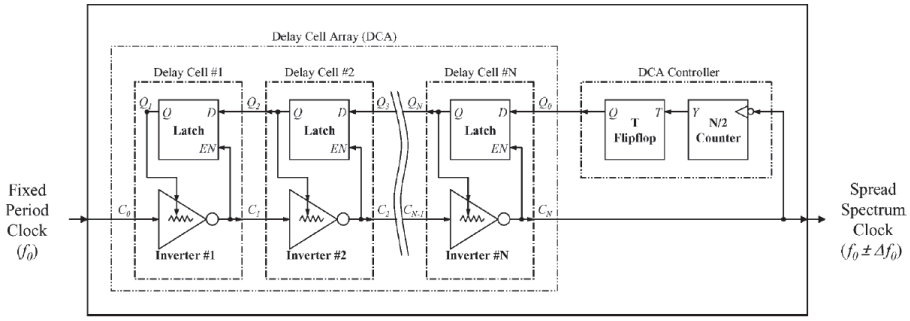

Figure 1.14. SSCG with Delay Cell Array of [4].

The all-digital SSCG presented in [7] is based on a fully synchronous architecture. The circuit is able to perform frequency synthesis and is able to generate a clock frequency larger than 1GHz with an arbitrary modulation profile and a modulation frequency up to 5MHz. The top level diagram of the all-digital SSCG of [7] is shown in figure 1.15. As you can see, the circuit is realized by using a digital processor and a delay line block which including three digitally controlled delay lines. The delay lines Δ_{RE} and Δ_{FE} are used to generate the modulated output waveform. The third delay line Δ_{MEAS}, closed in a ring oscillator topology, is employed for the on-line measurement of the delay line resolution in order to compensate the PVT variations.

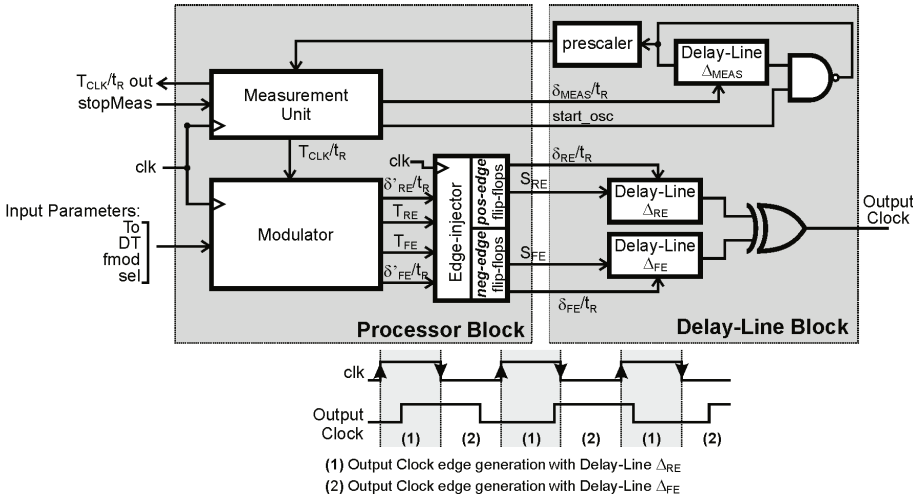

Figure 1.14. All-digital SSCG architecture of [7].

The modulator provides the control signal of the delay lines to achieve the required period modulation. However, this architecture suffers from a very large deterministic jitter.

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Chapter 2

All-Digital SSC Generator in 28nm CMOS Supporting Discontinuous Modulation Profile

The developed circuit presented in this chapter exploits an all-digital architecture which do not require any loop to implement frequency synthesis and spreading. This allows to solve all limitations of PLL/FLL in term of capability to implement frequency discontinuous modulation profiles, with high accuracy and large modulation frequency and instant recovery time. In addition, the developed circuit can be designed by using a design flow completely based on standard-cells, reducing in this way the design time and simplifying the porting in new technologies.

This chapter is organized as follows. Firstly a detailed description of the developed architecture is discussed. The circuit implementation details are given in the sections 2.1, 2.2 and 2.3. Section 2.4 describes the circuit sizing and the major sources of deterministic jitter are also discussed. Finally, the section 2.5 reports the on-chip experimental measurement results.

The top-level diagram of the developed all-digital Spread Spectrum Clock Generator (SSCG) is shown in Fig. 2.1. The system has an input clock signal (*clk*) having a constant period $T_{clk}=1/f_{clk}$ and 50% duty cycle and generates a frequency modulated output clock signal. The output clock signal is produced by using the four digitally-controlled delay-lines (DCDL), named $\Delta 0_{RE}$, $\Delta 1_{RE}$, $\Delta 0_{FE}$, $\Delta 1_{FE}$ and two delay interpolators, digitally controlled by a *Modulator*. The DCDL couple $\Delta 0_{RE}$, $\Delta 1_{RE}$ is driven on the rising-edge of *clk* and

is in charge of generating output clock edges in a timing window of length $T_{clk}/2$ starting from the input clock rising-edge. Similarly the DCDL couple $\Delta 0_{FE}$, $\Delta 1_{FE}$ is in charge of generating output clock edges in a timing window starting from the falling edge of the input clock signal. Each delay-line is used for one half clock period, the remaining half clock period is used as timing margin for the settling time of the delay-lines control signals (*delay-control R* and *delay-control F*). Each DCDL has a delay resolution equal to t_R (about 28 ps in our implementation).

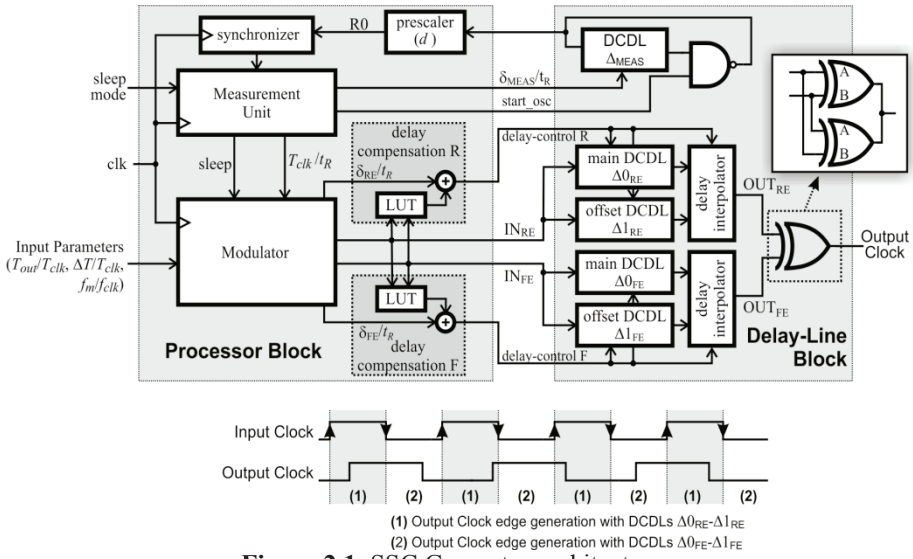

Figure 2.1. SSC Generator architecture.

Offset-DCDLs ($\Delta 1_{RE}$ and $\Delta 1_{FE}$) have the capability to provide delay-values offset by $t_R/2$ with respect to standard DCDL ($\Delta 0_{RE}$ and $\Delta 0_{FE}$). As a consequence each delay interpolator receives two signals delayed by $t_R/2$ and is able to interpolate the delay of these two signals with a 1/16 step. The overall resolution in output clock edge positioning (encoded by δ_{RE}/t_R and δ_{FE}/t_R signals) of the SSCG is therefore $t_R/32$ (about 0.9 ps in our implementation, typical corner). The XOR gate merges the two waveforms produced by the DCDLs and interpolators and generates the output clock signal.

By choosing the number of delay elements of each delay-line so that an input clock semi-period is covered, the *Modulator* is able to position output clock edges anywhere in the time axis, with a delay resolution equal to $t_R/32$ (see section 2.1). This topology has the

capability to position two output clock edges within one clock period. Therefore, the maximum output clock frequency, named f_{out} is:

$$f_{out_{MAX}} = f_{CLK} \tag{2.1}$$

Note that the digital inputs T_{out}, ΔT and f_m represent the nominal output period, the modulation depth and the modulation frequency, respectively.

Such a tight resolution allows to generate output clock signals with reduced jitter by compensating the delay asymmetries (rise/fall asymmetries of DCDL, delay asymmetries of the XOR gates which provide the output clock signal) between the different paths between the input clock and the output clock signal.

In this work we have verified a very simple compensation approach, in which delay asymmetries are evaluated in simulation and implemented in two simple compensation Lookup-Tables (*delay compensation R* and *delay compensation F* in figure 2.1). It is worth to note that each LUT requires only two input bits, and encodes delay asymmetries normalized to t_R. This makes the asymmetry compensation weakly dependant on process, voltage and temperature (PVT) operating conditions. Our simulations, on different corners and operating conditions, showed that this approach is very effective in reducing the output jitter of the circuit. As we will see in the section 2.5, this is also confirmed by jitter measurements of the test chip.

A fifth delay line (named Δ_{MEAS}), closed in a ring-oscillator topology, and a *Measurement Unit* are included to compensate PVT variations. The ring-oscillator period is $T_{OSC} \cong 2(\delta_{MEAS}+\delta_{nand})$, where δ_{nand} is the delay of the NAND gate used to start/stop the oscillator. A simple counter is employed in the measurement unit, to measure the ratio T_{OSC}/T_{clk}. The ratio t_R/T_{clk} is obtained by performing two successive measurements of T_{OSC} (T_{OSC1}, T_{OSC2}), for two different values (N_1, N_2) of the control signal δ_{MEAS}/t_R: $t_R=(T_{OSC2}-T_{OSC}1)/(2(N_2-N_1))$ where, N_2-N_1 is a power of 2, to simplify hardware implementation (see section 2.3).

The Δ_{MEAS} DCDL can be smaller than the other two DCDL. In our implementation $\Delta 0_{RE}$, $\Delta 1_{RE}$, $\Delta 0_{FE}$ and $\Delta 1_{FE}$ DCDLs use 88 elements, while Δ_{MEAS} requires only 40 elements. The value of t_R is continuously measured and feeds the modulator block (see figure 2.1), to track PVT variations. In Fig. 2.1, the signal R0 at prescaler output is asynchronous with respect to the input clock, and hence a

synchronizer is required. This is the only synchronization point between different clock domains in our architecture.
Implemented SSCG supports two different sleep modes. In weak sleep mode all sub-modules are shut-down , with the exception of the ring-oscillator and the counter, that constantly tracks voltage and temperature variations. In these conditions the SSCG presents a power dissipation of only 390μW and is able to wake-up in a very low recovery time (few nanoseconds), which depends only on the pipelining latency of the circuit. In full sleep mode, all sub-modules are turned-off and the recovery time depends on the measurement time of the measurement unit (5.5μs in our implementation). It is worth to note that weak sleep mode functionality is not possible in a PLL/FLL where tracking the voltage and temperature variations requires the operation of the whole loop.
The developed all-digital SSCG has been implemented by using only standard cells. As you can see in the next sections, all the output jitter sources are confined within the *Delay Line* block, therefore a full custom layout has been realized for the *Delay Line* block in order to mitigate the asymmetries components. Instead, an automatic place & route design is used to design the *Processor* block.

2.1 Modulator

The *Modulator* determines the shape of the modulation, the modulation depth and the modulation frequency by computing the position of the edges of the output clock signal. Fig. 2.2 shows the architecture of the *Modulator*. This blocks is composed by two subsystems: a Direct Digital Frequency Synthesizer (*DDFS*) and a *Modulation Profile* block. Both subsystem are synchronized by the input clock signal (*clk*).

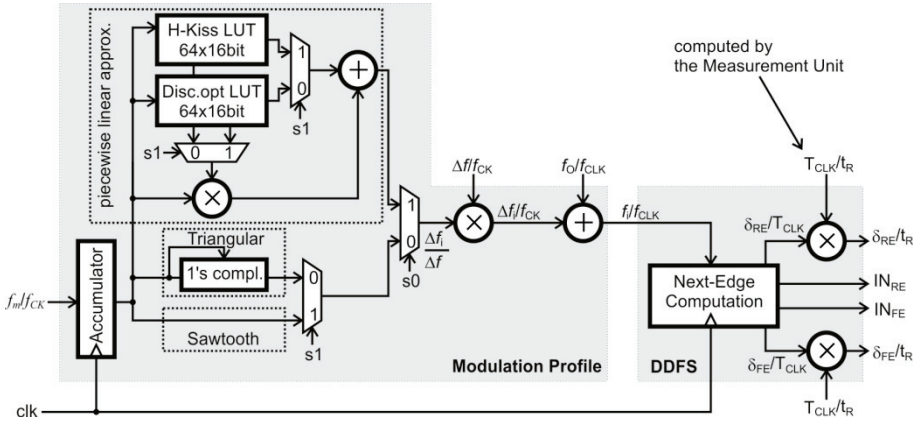

Figure 2.2. Architecture of the Modulation profile and Digital Frequency Synthesizer.

The DDFS receives as input the instantaneous frequency f_i of the output clock, normalized to the input clock frequency (f_{CLK}) and computes, in each clock cycle, the DCDL inputs (IN_{RE}, IN_{FE}) and delay control signals (δ_{RE}/T_{CLK}, δ_{FE}/T_{CLK}). As shown in Fig. 2.2 this is obtained with the help of a finite state machine (*Next-Edge Computation* block).

The signal IN_{RE} is high when an output clock edge has to be generated between the next rising and the falling edges of the input clock signal. In this case, the signal δ_{RE}/t_R encodes the delay (normalized the delay line resolution t_R) between the input clock rising edge and the output clock edge. Similarly, the signal IN_{FE} is high when an output clock edge has to be generated between the next falling and the rising edges of the input clock signal. In this case, the signal δ_{RE}/t_R encodes the

delay (normalized the delay line resolution t_R) between the input clock falling edge and the output clock edge. Note that the output clock can have a frequency as high as f_{clk}, therefore it is possible that in the same clock cycle both IN_{RE} and IN_{FE} are high. The DCDL control signals are scaled to the DCDL resolution t_R by using two multipliers and the value T_{CLK}/t_R is given by the Measurement Unit.
The *Modulation Profile* block computes the instantaneous frequency f_i by adding the desired output frequency (f_o) to the instantaneous frequency deviation Δf_i imposed by the frequency modulation profile.
The assumed definition of modulation parameters (Δf and f_m) is shown in figure 2.3 (considering as an example a linear modulation profile). Note that the modulations are realized in down-spreading.

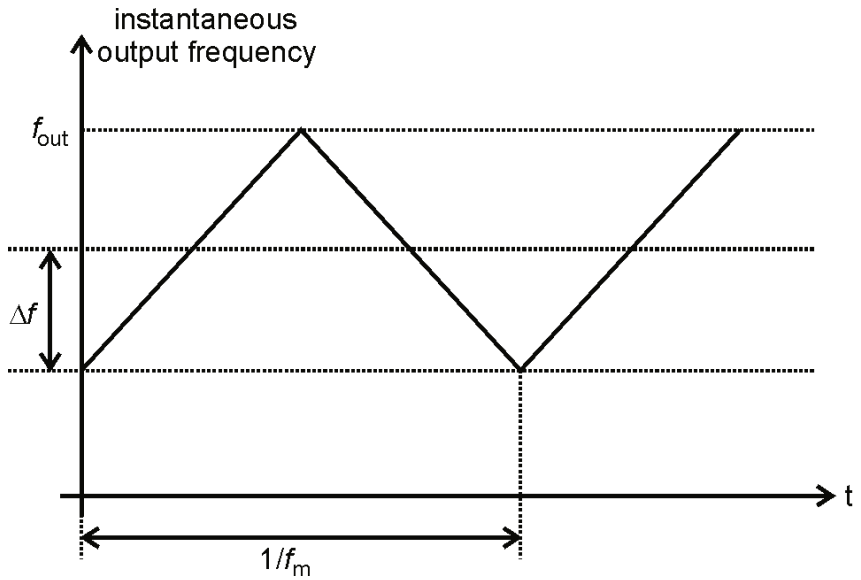

Figure 2.3. Modulation parameter (e.g. triangular modulation shape).

As you can see in the figure 2.2 an accumulator counts the elapsed time normalized to the modulation period $T_m=1/f_m$. This signal feeds the blocks which compute four different modulation profiles. Triangular and Sawtooth profiles are realized by using respectively a 1's complementer and the output of the accumulator directly. The Hershey-Kiss and the optimal discontinuous frequency modulation [1] are implemented by using a piecewise linear approximation using 64 uniform segments. These blocks output the instantaneous period deviation (Δf_i) normalized to Δf. The desired modulation can be selected by using the signal *s0* and *s1* bits. Finally a multiplier and an

adder allows to compute the instantaneous frequency f_i. Please note that, with respect the previous all-digital SSCG [2], the our *Modulator* allows to realize the optimal discontinuous frequency modulation. Note that the discontinuous frequency modulation allows to obtain an improvement of the modulation gain of 1.5—2dB with respect to continuous frequency modulations (see section 1.1).
The Table 2.1 reports the exact meaning of the *Modulator* inputs. Please note that there is no need to compute modulation parameters ($\Delta f_i/T_{CLK}$, f_i/f_{CLK}) at gigahertz frequency. The modulation profile block, therefore, is divided by four to reduce the power dissipation. The resolution of T_{OUT} is, in the worst case (f_{CLK}=300MHz), equal to 0.41ps. In the worst case (T_{OUT}/T_{CLK}=1024) the maximum relative modulation depth $\Delta T/T_{OUT}$ is 3.1%. Please note that a larger modulation depth can be obtained for $T_{OUT}<1024T_{CLK}$. In the worst case (T_{OUT}/T_{CLK}=1) the resolution depth is 0.20%. Finally, in the worst case (f_{CLK}=300MHz) the maximum modulation frequency is 18.75MHz, while the modulation frequency resolution is 0.07KHz.

Signal	MSB	LSB	maximum	minimum	resolution
$\frac{T_{OUT}/2}{T_{CLK}}$	2^{8}	2^{-14}	$T_{OUT} \leq 1024T_{CLK}$	$T_{OUT} \geq T_{CLK}$	$2^{-13} \cdot T_{CLK}$
$\frac{\Delta T}{T_{CLK}}$	2^{4}	2^{-9}	$\frac{\Delta T}{T_{OUT}} \leq 3200\frac{T_{CLK}}{T_{OUT}}\%$	$\frac{\Delta T}{T_{OUT}} \geq 0\%$	$0.20 \cdot \frac{T_{CLK}}{T_{OUT}}\%$
$\frac{f_m}{f_{CLK}}$	2^{-3}	2^{-20}	$f_m \leq 62.50 \cdot 10^{-3} f_{CLK}$	$f_m \geq 0$	$9.53 \cdot 10^{-7} f_{CLK}$

Table 2.1. Meaning and range of *Modulator* input signals

2.2 Delay Line Block

A key element of an all digital Spread Spectrum Clock Generator is the design of the digitally controlled delay line (DCDL), since INL of these components translates in output clock jitter. As introduced in the section 2.1, four DCDLs and two interpolators are used in order to generate the output clock signal.
In literature different architectural solutions have been developed to implement the DCDL. In many papers the DCDL is realized by using a delay cells chain and a multiplexer to select the desired cell output [3]-[8]. The drawback of these solutions consists in the trade-off between the frequency range and the minimum delay (t_{min}) of the DCDL due to increase of the multiplexer delay with the increase of the number o cells. Please note that t_{min} is a critical design parameter in many application. In fact, for example, in ADDLL/ADPLL t_{min} determines the maximum output frequency of the circuit. This critical aspect is true also for the all-digital SSCG of [2], where a correct DCDL synchronization is obtained only by imposing that t_{min} is lower than one half input clock period. Note that the solution presented in [3] allows to obtain a reduced t_{min} by using a tree-based multiplexer topology. However, this implies an irregular structure which results in increased non-linearity layout effects.
In [9]-[12] the DCDL consists in series of equal delay elements (DE). Each DE is constructed by using only NAND gates, obtaining a very good linearity and resolution equal to $2t_{NAND}$ (t_{NAND} being the delay of a NAND gate). The minimum delay of DCDL (t_{min}) is very low and becomes independent of the number of cells. Moreover the highly regular topology allow a simple layout organization which provides very low non linearity layout effects. However this topology presents a glitching which does not allow its employ to use in a SSCG architecture.
The DCDL topology employed in [13] uses again a structure of cascaded delay-elements. However, differently from [9]-[12], each element is constructed by using tree-state inverter (TINV), obtaining a resolution $t_R=2t_{TINV}$. In addition, in [13] the two parallel DCDL topology, shown in Fig. 2.4, is proposed. This topology consists in using two DCDL in parallel connection, where the delay of one DCDL is offset by $t_R/2=t_{TINV}$. This structure, named coarse stage,

presents an "equivalent" resolution equal to $t_R/2=t_{TINV}$ that, in general, results lower than the resolution of [9]-[12]. In fact, the pull-up network of a TINV requires two series devices whereas a NAND gate uses a single device in the pull-up. Therefore, we can expect that $t_{NAND}<t_{TINV}<2t_{NAND}$.

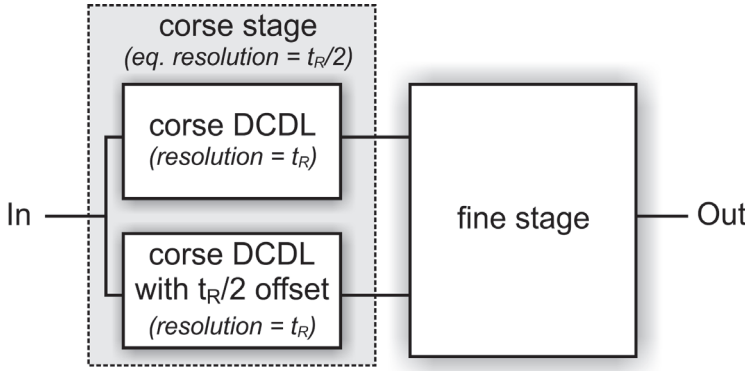

Figure 2.4. Two parallel DCDL topology proposed in [13] to halve the resolution of the coarse stage.

In [2] the DCDL is also realized by using a cascade of equal delay elements. In particular, each delay element is constructed by using an inverter and an inverting multiplexer. Note that the different delays of the inverter and the multiplexer results in a t_{min} mismatch between odd and even control codes. This mismatch results in an increased integral non linearity (INL). Moreover, the multiplexer have a large delay, which provides a resolution higher than the resolution of both NAND-based and TINV-based DCDLs. The DCDL presented in [14] is also based on a NAND-based delay elements chain. This topology avoids the glitching problem of previous NAND-based solutions [9]-[12] and maintains the same resolution ($2t_{NAND}$) and minimum delay. The *Delay Line Block* of the developed SSCG use the glitch free NAND-based DCDL proposed in [14]. Note that in our implementation, as you can see in the next section, the parallel coarse stage approach of [13] is extended to the NAND-based DCDL of [14]; this results in a resolution equal to t_{NAND} which results lower than the previous DCDL topology. Moreover, as you can see in section 2.2.2, this work introduces a novel fine stage that allows to provide a lower resolution. Note that the total absolute jitter depends on delay resolution and asymmetries, therefore the improving delay-line resolution with reducing of asymmetries have a strong impact on the overall jitter.

2.2.1 NAND-based Digitally Controlled Delay Lines (DCDL)

The NAND-based DCDL presented in [14] is shown in Fig. 2.5. This DCDL is composed by a cascade of equal delay elements (DE), each realized by using four NAND gates (where "A" denotes the fast input) and 2 dummy NAND gates (highlighted in gray) added for load balancing. This architecture guarantees the monotonicity if the delay chain and also very good linearity, if the DCDL layout is properly arranged. Two sets of control bits (S_i and T_i) are used for controlling the delay of the DCDL. The S_i bits encode the control-code c by using a thermometric code: $S_i = 0$ for $i < c$ and $S_i = 1$ for $i \geq c$. Instead, the bits T_i encode again c by using a one-cold code: $T_{c+1} = 0$, $T_i = 1$ for $i \neq c+1$. In the Fig. 2.5, as an example, the state of the control bits are shown considering In=1 and c=1. According to the chosen control-bits encoding, each DE can be in one of three possible state: turn state (S_i=1, T_i=1), pass state (S_i=0, T_i=1) and post-turn state (S_i=1, T_i=0). In Fig. 2.5 the NAND highlighted in gray allow to obtain the same load (two NAND gates) for all the NAND gates which, therefore, in a first order approximation, present the same delay. In this way we can write the delay δ, from *In* to *Out*, as follows:

$$\delta = 2t_{NAND} + 2t_{NAND} \cdot c \tag{2.2}$$

where $t_{NAND}=(t_{NAND\ LH} + t_{NAND\ HL})/2$ while $t_{NAND\ LH}$ e $t_{NAND\ HL}$ represent the delay of each NAND gate for a low-to-high and high-to-low output commutation, respectively.

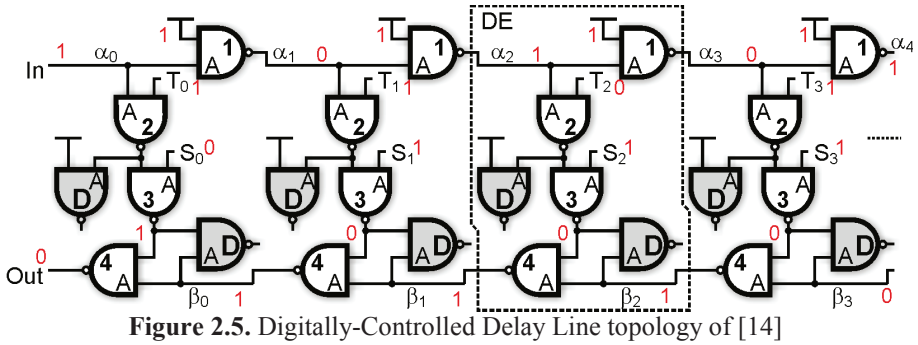

Figure 2.5. Digitally-Controlled Delay Line topology of [14]

The equation (2.2) suggests that $t_R = 2t_{NAND}$ and $t_{min} = 2t_{NAND}$. Please note that there is a relationship between the logic-states of successive DEs. As an example a DE in post-turn state is always followed by a DE in turn-state.

i-th DE state	valid i+1-th DE state	Notes
Pass	*Pass*	*Post-Turn* after *Pass* is not possible
	Turn	
Turn	*Turn*	*Pass* after *Turn* is not possible
	Post-Turn	
Post-Turn	*Turn*	After *Post-Turn* only *Turn* is allowed

Table 2.2. All possible states of a couple of DEs

The Table 2.2 shows all the possible logic-states of i+1-th DE given the logic state of i-th DE. Glitching is a common problem into the DCDL design, in fact, for example, when the DCDLs are employed to process clock signals the glitch-free operation is required. The NAND-based DCDL is glitch free when the switching of every couple of successive DE is glitch-free in all possible conditions. In particular, a timing constraint on control bits is required to avoid the glitching events for the DCDL of [14]. Therefore, a properly driving circuit is used to compute a correct time temporization of control-bits S_i and T_i. The Figure 2.6 shows the driving circuit presented in [14] which, assuming the employ of the encoding mentioned before, have no-glitch in presence of delay control code switching. Please note that this driving circuit uses two flip-flop for determining the control bits of each DE. So, in general, if we have N delay element then 2N flip flop are required for driving the DCDL.
In order to reduce the number of those flip-flops, an improved driving circuit is realized. The developed driving circuit is able to generate the control-bits of the NAND-based DCDL avoiding the glitch events and using one flip-flop for each DE.
For this purpose a new encoding for the control bits is implemented (see Table 2.3). This encoding allows to evaluate each S_i signal by looking two successive Ti signals (T_i and T_{i-1}).

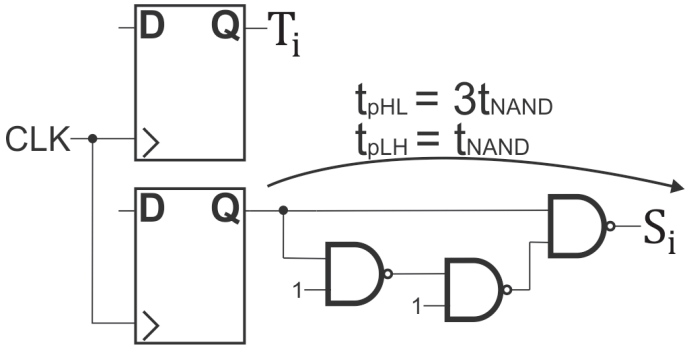

Figure 2.6. Driving Circuit of [14]

More precisely, the S_i can be obtained by using an OR logic function between the signals T_i and S_i.

S_i	T_i	DE state
0	0	*Pass*
1	1	*Turn*
1	0	*Post-Turn*

Table 2.3. New encoding for logic states of DE

The Fig. 2.7a shows the novel driving technique that allows to halve the flip-flop number of the driving circuitry with respect to the driving circuit of Fig. 2.6. Instead, the Fig. 2.7b shows an alternative driving circuit obtained by using complemented flip-flop inputs ($n\tau_i$ signals), one NAND gate and an inverter to compute S_i and T_i signals. Unfortunately, with the driving circuit of both Fig. 2.7a and Fig. 2.7b a glitch can occurs at the output of the DCDL.

As an example, the Fig. 2.8 shows a possible glitch case in the NAND-based DCDL when the delay control code is increased. In fact, referring to the i-th DE both inputs of the NAND "4" switch, in particular the "A" input of this gate switches from 1 to γ, and this switching is driven by the high-to-low (HL) switching of S_{i+1}. The other input ("B" input) of the NAND gate switches from γ to 1, because of the HL switching of S_i. A glitch ($\bar{\gamma} \to 0 \to \bar{\gamma}$) can occurs at the output of this gate if the "B" input switches much before the "A" input.

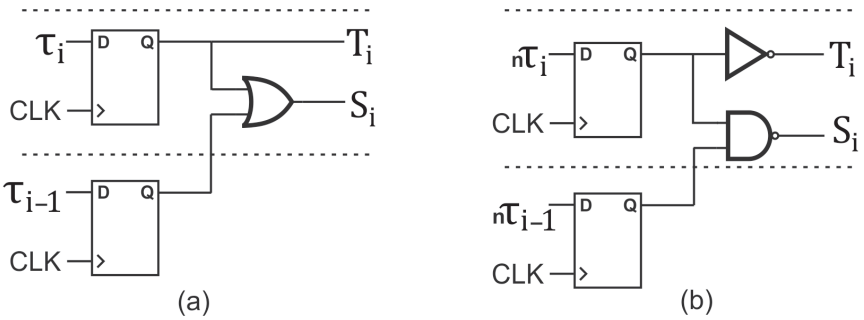

Figure 2.7. New driving circuit topology.

We will assume that no glitch is produced when the difference between the arrival time of "A" input and the arrival time of "B" input is lower than the propagation delay of the gate (t_{NAND}). Referring to the Fig. 2.8, the arrival time of "A" input and "B" input are indicated as t_A and t_B respectively.

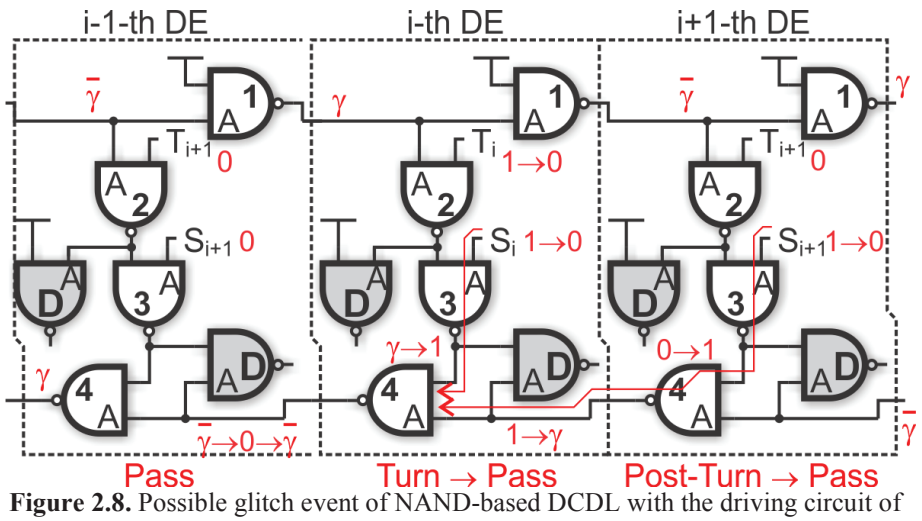

Figure 2.8. Possible glitch event of NAND-based DCDL with the driving circuit of Fig 2.7.

In particular $t_A = t_{Si+1HL} + 2t_{NAND}$ where t_{Si+1HL} represent the arrival time of HL switching of S_{i+1} signal and $t_B = t_{SiHL} + t_{NAND}$ where t_{SiHL} represent the arrival time of HL switching of S_i signal. If the driving circuit shown in the Fig. 2.7b is used then the arrival time t_{SiHL} and the arrival time t_{Si+1HL} are both equal to t_{NAND}; in this way the time difference $t_B - t_A = -t_{NAND}$, that is the "A" input switches after the "B" input, so the glitch occurs at the output of the NAND "4".

The Fig. 2.9 shows a glitch-free design of the driving circuit where a certain number of gates are used in order to guarantee the timing constraints on control bits S_i and T_i for avoiding the glitch. In fact, referring to the Fig. 2.9, the arrival time $t_{SiHL}=3\cdot t_{NAND}$ and the arrival time $t_{Si+1HL}=t_{NAND}$, therefore $t_B - t_A = t_{NAND}$, that is the "B" input switches much after the "A" input. In this way the glitching at the output of the NAND "4" is avoided and the timing glitch margin is equal to $2\cdot t_{NAND}$.

The analysis of all the possible glitch cases is out of the scope of this thesis, however we have verified that the glitch events are avoided in all possible cases. To sum up the circuit of Fig. 2.9, composed by a cascade of control elements (CE), exploits the redundancy of the encoding of S_i, T_i bits ($S_i=T_i+T_{i-1}$) which allows to employ a single flip-flop for each CE.

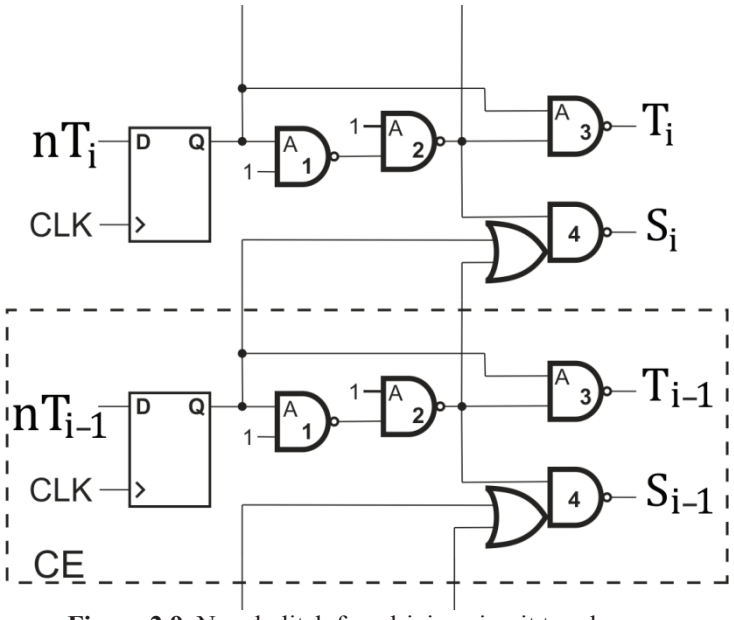

Figure 2.9. Novel glitch free driving circuit topology.

In comparison to the solution of [14], which requires two flip-flops for CE, this results both in a sensible reduction of area occupation and power dissipation.

As mentioned in the previous section, in order to improve the resolution of the DCDL presented in [14], we have been extended the parallel topology proposed in [13] to a NAND-based structures. This topology consists in using two DCDL in parallel connection, where

the delay of one DCDL is offset by $t_R/2$. This approach allows to obtain an "equivalent" resolution equal to $t_R/2=t_{NAND}$.

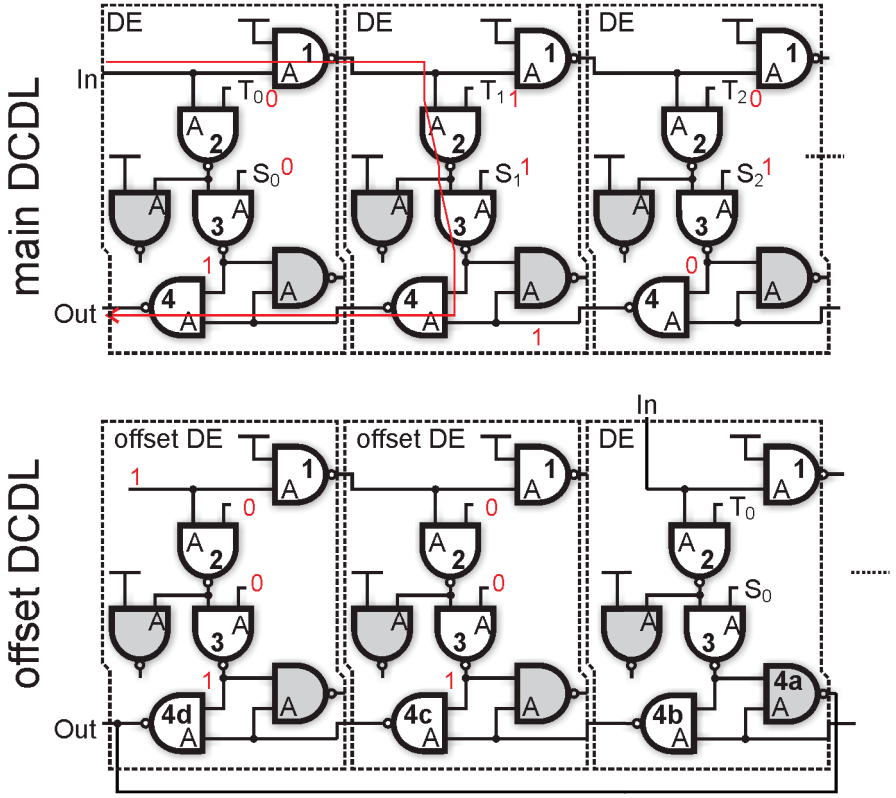

Figure 2.10. Digitally-Controlled Delay-Line (DCDL) topologies.

Therefore, as you can see in Fig. 2.10, an offset NAND-based DCDL is realized. In the offset-DCDL, the first DE is modified and two offset DEs are added at the beginning of the line. The effect of these DEs is replacing the NAND 4 of the first DE of the main DCDL, with the parallel of NAND 4a and the cascade of NANDs 4b,4c,4d. This structure results in an overall delay of $2t_{NAND}$ (half-way between $3t_{NAND}$ and t_{NAND}) which corresponds to add $t_R/2$ to the signal propagation path, in comparison to the main DCDL. The DE layout has been placed and routed manually, by carefully controlling parasitic.

As discussed in section 2.1, note that each delay-line has able to position the output clock edge within a window with a duration of one half clock input clock period ($T_{CLK}/2$). This requires the following constraint:

$$(N-1)\cdot t_R \geq T_{CLK}/2 \tag{2.3}$$

where N is the number of elements of the delay lines $\Delta 0_{RE}$, $\Delta 1_{RE}$, $\Delta 0_{FE}$, $\Delta 1_{FE}$. Since the minimum input clock frequency is 300MHz and the minimum t_R is 21.8ps, the minimum number of elements of the delay lines is N_{MIN}=77. In the realized circuit, in order to optimize the symmetry of the layout of the delay lines N is chosen equal to 88. This allows the circuit to work down to a frequency of 264MHz.

2.2.2 MUX-based Digital Delay Interpolator

As we have highlighted at the beginning of this chapter, the design of highly linear interpolators and the design of the DCDLs is a key point to realize a SSCG with reduced output jitter. In the developed IC a novel digital delay interpolator is employed, which, differently from previously proposed solution (e.g. [13]), can be realized by using only standard cells. The employed circuit topology, with an interpolation factor N equal to 16, is shown in Fig. 2.11.
The circuit is composed by sixteen parallel two to-one MUX cells, available from the standard-cells library, and is driving by a thermometric code through the control bits F_0,....,F_{15}. Let us name *x* the delay control code. If we assume for each multiplexer a simple delay model with intrinsic delay t_i and rise time t_r, the voltage at the output node can be written as:

$$V_{OUT} = \frac{V_{DD}}{t_R}\left(t - t_i - \Delta\frac{x}{N}\right) \tag{2.4}$$

where *N* is the number of multiplexers and Δ is the delay between the two input signals.
The propagation delay t_d of the interpolator can be therefore written as:

$$t_D = t_i + \frac{t_R}{2} + \Delta\frac{x}{N} \tag{2.5}$$

This simple equation shows that the interpolator allows to linearly control the delay with a delay-range corresponding to the delay Δ of the two input signals. Clearly this simple model neglects a number of non-ideal effects, like asymmetry in multiplexer propagation delay between the two multiplexer inputs (D0 and D1), dependence of the MUX delay on the logic value of the control bit state, that translate in a non-linear behaviour.

One solution to mitigate these effects is flipping each other the multiplexers, as shown in the figure 2.11. This allows to have, independently from the control code *x*, always almost *N*/2 multiplexer control bits at state 0 and *N*/2 multiplexer control bits at state 1. In these conditions the multiplexers asymmetries tends to compensate each other.

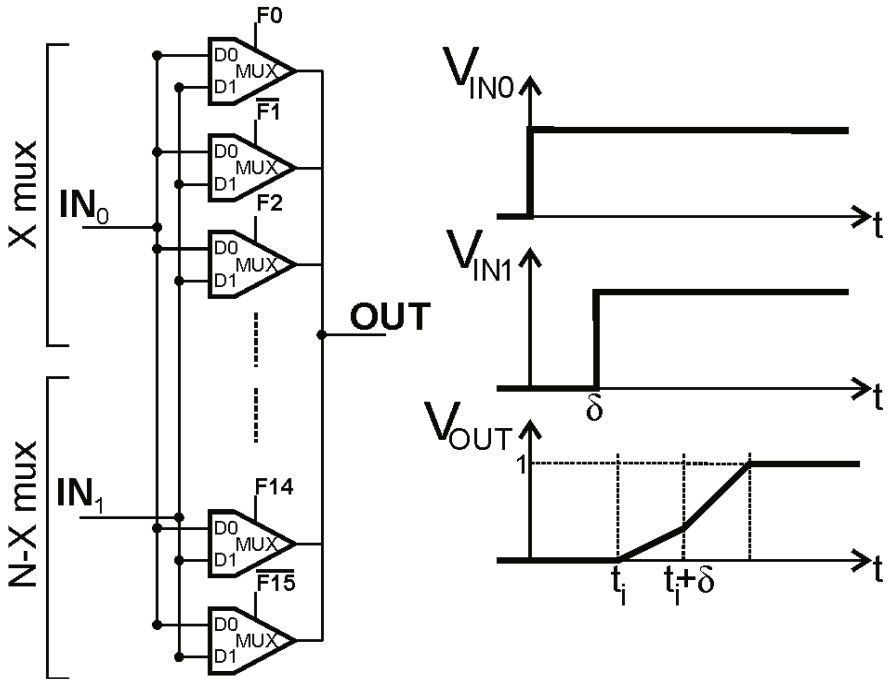

Figure 2.11. Architecture of the MUX-based digital delay interpolator used in the developed SSCG.

In our implementation the delay interpolator receives two signals delayed by $t_R/2$ from the DCDLs. In particular, an architecture with sixteen multiplexer has been used in order to interpolate the delay of these two signals with a 1/16 step. In this way the overall resolution in output clock positioning of the SSCG is equal to $t_R/32$.

2.2.3 Delay Line Block timing

As explained previously, the delay lines $\Delta 0_{RE}$ and $\Delta 1_{RE}$ covers a timing window which starts from the rising edge of the input clock. On the other hand, the delay lines $\Delta 0_{FE}$ and $\Delta 1_{FE}$ covers a timing window which starts from the falling edge of the input clock. Therefore, in the architecture of figure 2.1, the input signals of the delay lines $\Delta 0_{RE}$ and $\Delta 1_{RE}$ are the output of positive-edge flip-flops. The input signals of the delay lines $\Delta 0_{FE}$ and $\Delta 1_{FE}$ are the outputs of negative flip-flops. Note that no dual-edge flip-flop is necessary within the circuit. This simplifies the design of the clock tree.

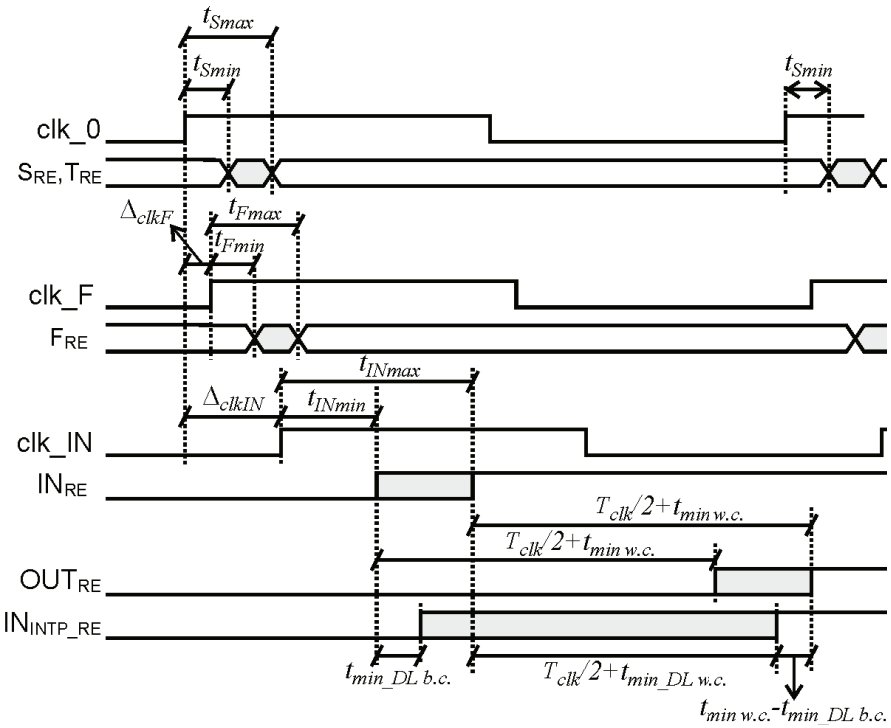

Figure 2.12. Delay Line block detailed timing.

Figure 2.12 shows a detailed timing of the delay lines $\Delta 0_{RE}$ and $\Delta 1_{RE}$ and the delay interpolator. Note that the timing of the delay lines $\Delta 0_{FE}$ and $\Delta 1_{FE}$ is similar, the only difference is that the delay lines $\Delta 0_{FE}$ and $\Delta 1_{FE}$ are timed on the falling edge of the clock signal. Therefore,

without loss of generality we can consider only the delay lines $\Delta 0_{RE}$ and $\Delta 1_{RE}$ and delay interpolator for the timing analysis.
In figure 2.12 the following definitions are assumed:

– *clk_0*: clock signal of the control block of the delay lines $\Delta 0_{RE}$ and $\Delta 1_{RE}$.
– S_{RE}, T_{RE}: control signals of the delay element of the delay lines $\Delta 0_{RE}$ and $\Delta 1_{RE}$.
– *clk_F*: clock signal of the delay interpolator.
– *F*: control signals of the delay interpolator.
– *clk_IN*: clock signal of the flip-flop.
– IN_{RE}: output signal of the flip flop that is the input of the delay lines $\Delta 0_{RE}$ and $\Delta 1_{RE}$.
– OUT_{RE}: output signal of the delay interpolator.
– IN_{INTP_RE}: input signal of the delay interpolator.
– Δ_{clkIN}: timing margin of the *clk_IN* signal with respect the *clk_0* signal.
– Δ_{clkF}: timing margin on the *clk_F* signal with respect the *clk_0* singal.
– t_{Smax}: maximum propagation delay through the control block of the delay lines.
– t_{Smin}: minimum propagation delay through the control block of the delay lines.
– t_{Fmax}: maximum propagation delay of the interpolator control signals.
– t_{Fmin}: minimum propagation delay of the interpolator control signals.
– t_{INmax}: maximum propagation delay of the flip-flop.
– t_{INmin}: minimum propagation delay of the flip-flop.
– $t_{minw.c.}$: minimum propagation delay of the delay lines and delay interpolator in the worst case.
– $t_{min\_DLw.c.}$: minimum propagation delay of the delay lines in the worst case.
– $t_{min\_DLb.c.}$: minimum propagation delay of the delay lines in the best case.

Note that the clock signals are synchronized by the clock tree of the top-level of the SSCG.
Let us evaluate the setup/hold time constraints on the control signals of the delay lines $\Delta 0_{RE}$ and $\Delta 1_{RE}$ (*S* and *T* signals) and the setup/hold

time constraint on the control bits of the delay interpolator (*F* signals). The setup time constraint on the control signals S_{RE} and T_{RE} can be written as:

$$\Delta_{clkIN} + t_{IN\min} > t_{S\max} \tag{2.6}$$

Therefore:

$$\Delta_{clkIN} > t_{S\max} - t_{IN\min} \tag{2.7}$$

The hold time constraint can be written as:

$$\Delta_{clkIN} + t_{IN\max} + t_{\min\_DLw.c.} + T_{clk}/2 < T_{CLK} + t_{S\min} \tag{2.8}$$

Therefore:

$$\Delta_{clkIN} < T_{clk}/2 - t_{IN\max} - t_{\min\_DLw.c.} + t_{S\min} \tag{2.9}$$

By using the equations (2.7) and (2.9) the clock period constraint on the S,T signals can be obtained as:

$$T_{clk}/2 > t_{IN\max} - t_{IN\min} + t_{\min\_DLw.c.} + t_{S\max} - t_{S\min} \tag{2.10}$$

Similarly, the setup time constraint on the control signals of the delay interpolator can be written as:

$$\Delta_{clkIN} + t_{IN\min} + t_{\min\_DLb.c.} > \Delta_{clkF} + t_{F\max} \tag{2.11}$$

Therefore:

$$\Delta_{clkF} < \Delta_{clkIN} + t_{IN\min} + t_{\min\_DLb.c.} - t_{F\max} \tag{2.12}$$

Instead the hold time constraint is given by:

$$\Delta_{clkIN} + t_{IN\max} + T_{clk}/2 + t_{\min w.c.} < T_{CLK} + t_{F\min} + \Delta_{clkF} \tag{2.13}$$

Therefore:

$$\Delta_{clkF} > \Delta_{clkIN} + t_{IN\max} + t_{\min w.c.} - t_{F\min} - T_{clk} / 2 \qquad (2.14)$$

By using the equations (2.12) and (2.14) the clock period constraint on the F_{RE} signals can be obtained as:

$$T_{clk} / 2 > t_{IN\max} - t_{IN\min} + t_{F\max} - t_{F\min} + t_{\min w.c.} - t_{\min\_DLb.c.} \qquad (2.15)$$

An extensive set of simulations have been performed in order to evaluate the delay of the propagation signals t_{Fmax}, t_{Fmin}, t_{Smax}, t_{Smin}, t_{INmax}, t_{INmin}, $t_{minw.c}$, $t_{min\_DLw.c}$ and $t_{min\_DLb.c}$. In this way, it is possible to evaluate the constraints on Δ_{clkIN}, Δ_{clkF} and T_{clk} by using the equations (2.7), (2.12), (2.10) and (2.15). The Tab. 2.4 summarizes the timing constraints of the delay line block.

Parameter	Value	conditions
Δ_{clkIN}	>35ps >20ps	eq. (2.7), slow corner eq. (2.7), fast corner
Δ_{clkF}	<211ps <46ps	eq. (2.12), slow corner eq. (2.12), fast corner
f_{CLKmax}	2.15GHz 3.92GHz	eq. (2.15), slow corner eq. (2.15), fast corner
f_{CLKmax}	1.50GHz 2.69GHz	eq. (2.10), slow corner eq. (2.10), fast corner

Table 2.4. Timing constraints of the Delay Line Block.

2.3 Measurement Unit

As introduced in the section 2.1, the SSCG is needed to take into account the process, voltage and temperature (PVT) variations which modifies the delay-line resolution t_R. In order to compensate the variations of t_R with the PVT operating condition of the circuit, the *Measurement Unit* continuously measures the ratio T_{CLK}/t_R and provides the value of this parameter to the *Modulator* block.
As shown in Fig. 2.1, the measurement circuit is composed by a *Measurement Unit* which drives a replica delay-line (Δ_{MEAS}), closed in a ring oscillator topology. Let us to explain the measurement operation.
The period of the ring oscillator output (T_R) is given by:

$$T_R = 2 \cdot \left(t_{NAND} + t_{MIN} + \frac{\delta_{MEAS}}{t_R} \cdot t_R \right) \tag{2.16}$$

where t_{NAND} is the delay of the NAND gate and t_{MIN} is the minimum delay through Δ_{MEAS}.
The value of t_R can be extracted in the following way. Firstly the delay line Δ_{MEAS} is driven with δ_{MEAS}/t_R input equal to N_1. The resulting period of the ring oscillator T_{R1} is divided by the prescaler with a division ratio equal to 4 and the frequency divider with a division ratio equal to d'. In the following, let us name d=4·d'. The output of the frequency divider is used as the enable signal of a up/down counter clocked by input clock. At the end of one cycle, the counter content M_1 will be a measure of the half period of the prescaler output:

$$\left(M_1 \pm 1\right) \cdot T_{CLK} = \left(\frac{d \cdot T_{R1}}{2} \right) = d \cdot \left(t_{NAND} + t_{MIN} + N_1 \cdot t_R \right) \tag{2.17}$$

Similarly, a second measurement is performed with δ_{MEAS}/t_R input equal to N_2. Therefore the counter content M_2 will be given by:

$$\left(M_2 \pm 1\right) \cdot T_{CLK} = d \cdot \left(t_{NAND} + t_{MIN} + N_2 \cdot t_R \right) \tag{2.18}$$

By subtracting the two equations (2.17) and (2.18) the two unknowns t_{NAND} and t_{MIN} are deleted from the measurement:

$$M_1 - M_2 = d \cdot \left(N_1 - N_2 \right) \frac{t_R}{T_{CLK}} \pm 2 \tag{2.19}$$

Therefore:

$$\frac{t_R}{T_{CLK}} = \frac{M_1 - M_2}{d \cdot \left(N_1 - N_2 \right)} \pm \frac{2}{d \cdot \left(N_1 - N_2 \right)} \tag{2.20}$$

The *Measurement Unit* evaluates the ratio T_{CLK}/t_R by using an arithmetic unit:

$$\frac{T_{CLK}}{t_R} \simeq \frac{d \cdot \left(N_1 - N_2 \right)}{M_1 - M_2} \tag{2.21}$$

Therefore the maximum measurement error of t_R/T_{CLK} is:

$$\varepsilon_{t_R/T_{CLK}} = \frac{2}{d \cdot \left(N_1 - N_2 \right)} \tag{2.22}$$

By expanding in Taylor series and truncating at the first order it is possible to evaluate the error on T_{CLK}/t_R measurement:

$$\varepsilon_{T_{CLK}/t_R} = \left(\frac{T_{CLK}}{t_R} \right)^2 \cdot \varepsilon_{t_R/T_{CLK}} \tag{2.23}$$

The total measurement time is equal to:

$$T_{meas} = d \cdot \left(N_1 + N_2 \right) \cdot t_R + 2d \cdot \left(t_{MIN} + t_{NAND} \right) \tag{2.24}$$

Please note that by reducing N_2 we improve the measurement error and the measurement time but we increase also the frequency of the ring oscillator. Therefore, the N_2 value is selected as low as possible, by taking account the prescaler maximum operating frequency. In our implementation, t_R=21.8ps in the fast corner (see the next section) and we have chosen N_2=6, obtaining a maximum ring oscillator frequency equal to 3.28GHz, that is the maximum clock frequency for which the prescaler has to be designed. Clearly, the maximum clock frequency of the frequency divider will be given by 3.28GHz/4=821MHz. Moreover, in the slow corner (t_R=51.2ps) so the maximum ring oscillator frequency is 1.39GHz and the maximum clock frequency of frequency divider is 1.39GHz/4=349MHz. We have also chosen $N_1=N_2+32$ and $d=2^{16}$. In this way we have an error:

$$\varepsilon_{T_{CLK}/t_R} = \left(\frac{T_{CLK}}{t_R}\right)^2 \cdot 2^{-20} \tag{2.25}$$

Parameter	Value	conditions and annotation
N_1	38	
N_2	6	
d	65536	
$\varepsilon_{T_{CLK}/t_R}$	0.02238 0.00090 0.00404 0.00016	f_{CLK}= 300MHz, t_R=21.8ps (worst case) f_{CLK}=1500MHz, t_R=21.8ps f_{CLK}= 300MHz, t_R=51.2ps f_{CLK}=1500MHz, t_R=51.2ps (best case)
T_{meas}	161.1μs	t_R=51.2ps (worst case)
f_{clock} prescaler	3.28GHz 1.39GHz	max value in the fast corner (t_R=21.8ps) max value in the slow corner(t_R=51.2ps)
f_{clock} divider	821MHz 349MHz	max value in the fast corner (t_R=21.8ps) max value in the slow corner(t_R=51.2ps)

Table 2.5. Measurement Unit parameters and performances.

By considering the minimum clock frequency (300MHz) and the minimum delay-line resolution (21.8ps) we can evaluate the error in the worst case conditions:

$$\varepsilon_{T_{CLK}/t_R} \leq 0.02238 \tag{2.26}$$

Moreover, with the chosen parameters, by considering the worst speed corner (t_R=51.2ps), the total measurement time is:

$$T_{meas} = 161.1\mu s \tag{2.27}$$

The Table 2.5 reports the measurement circuit parameters and performances.

2.4 Circuit analysis and sizing

2.4.1 Measurement Circuit Sizing and Limitations

The range of t_R values which the measurement circuit is able to handle is determined by the length of the registers storing *M*1 and *M*2 and the number of bits used for the signal T_{CLK}/t_R in Fig. 2.1.
In this section the limits imposed by the length of M1 and M2 are discussed. The internal architecture of the *Measurement Unit* uses a single up/down counter to measure directly the quantity M1-M2. Initially the Delay-line Δ_{MEAS} is driven with δ_{MEAS}/t_R = N1, the up/down counter is cleared and is set for up-counting. Afterward, the Delay-line Δ_{MEAS} is driven with δ_{MEAS}/t_R = N2 and down-counting is selected. Without resetting the counter between the first and the second measure, the final value of the counter will be directly equal to M1-M2. The only condition to impose for the correct circuit operation is that M1-M2 is lower than the maximum value representable within the counter. This condition imposes a constraint on the maximum measurable t_R. Therefore we can write:

$$t_{RMAX} = \frac{2^{L_{M12}} - 1}{d \cdot (N_1 - N_2)} \cdot T_{CLK} \tag{2.28}$$

where L_{M12} is the number of bits of the counter which calculates M_1-M_2. In our case we chosen L_{M12}=19, consequently:

$$t_{RMAX} = 0.02499 \cdot T_{CLK} \tag{2.29}$$

In the worst case (f_{CLK} = 1500MHz), the maximum value allowed for t_R is 167ps.
Let us now consider the signal T_{CLK}/t_R (see Fig. 2.1). In our implementation this signal is composed by 14 bits, with a MSB of weight 2^7 and an LSB of weight 2^{-6}. The LSB weight results in a quantization error of T_{CLK}/t_R given by:

$$\varepsilon 1_{T_{CLK}/t_R} = 2^{-7} \tag{2.30}$$

Parameter	Value	conditions and annotation
L_{M12}	19	number of bits M_1-M_2register
MSB of T_{CLK}/t_R	2^7	
LSB of T_{CLK}/t_R	2^{-6}	
$\varepsilon 1_{T_{CLK}/t_R}$	2^{-7}	quantization error of T_{CLK}/t_R
t_{RMAX}	167ps	f_{CLK}=1500MHz (worst case)
t_{RMIN}	13ps	f_{CLK}= 300MHz (worst case)

Table 2.6. Parameter and limitations of the measurement circuit.

This is an additional source of error on the signal T_{CLK}/T_R of Fig. 2.1, which adds to the error $\varepsilon_{TCLK/tR}$ described in the section 2.2. The MSB weight of T_{CLK}/t_R imposes a limitation on the minimum t_R value which can be measured. The minimum possible t_R value can be written as:

$$t_{RMIN} = \frac{T_{CLK}}{2^8 - 2^{-6}} \tag{2.31}$$

In the worst case (f_{CLK} = 300MHz), t_{RMIN} is equal to 13ps. The Tab. 2.6 summarizes the parameters and limitations of the measurement circuit.

2.4.2 Jitter Analysis and Circuit Sizing

Let us analyze the jitter sources in our SSCG architecture. There are two main jitter sources: the jitter sources introduces by the *Modulator* block and the jitter sources due to the delay asymmetries of the *Delay-Line Block*. In this section a theoretical jitter analysis for both blocks is discussed.

The figure 2.2 show the architecture of the *Modulator*. Note that when the modulation is turned-off, $\Delta f/f_{CLK}$ is equal to 0 and, consequently also Δf_i=0. Therefore, in these conditions, no error is introduced by the *Modulation Profile* block in Fig. 2.2. Fig. 2.13 show the portion of *Modulator* relevant for the jitter analysis.

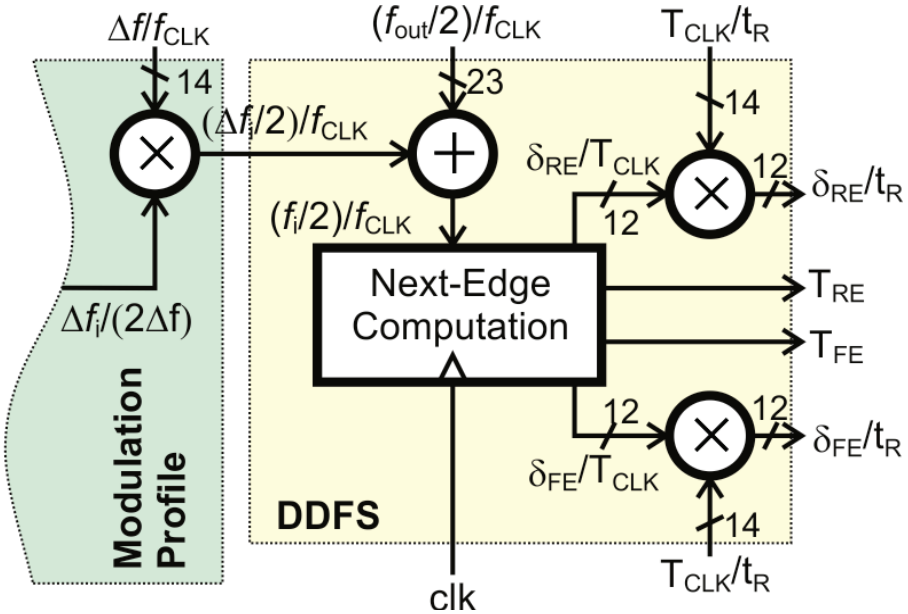

Figure 2.13. Portion of the *Modulator* relevant for the jitter analysis (without modulation).

The DDPS generates the input signals for the four delay-lines $\Delta 0_{RE}$, $\Delta 1_{RE}$, $\Delta 0_{FE}$, $\Delta 1_{FE}$ and for the delay interpolators. As shown in Fig. 2.13, this is obtained with the help of a *Next-Edge Computation* block that is a finite state machine (FSM). The output of the *Next-Edge Computation* block (δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK}) drive the delay lines and

interpolators through a scaling block. In this way it is possible to compute the position of output clock edges related to input clock period.

Note that the MSB of δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK} has a weight of 2^{-2} that is the maximum value of δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK} is 1/2. In fact, each clock edge can be positioned in a timing window of one half clock cycle. Let us name 2^{-u} the weight of the LSB of δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK}. In the implementation of Fig. 2.13, the signals δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK} are on 12 bit, therefore u=13. Moreover, the signals δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK} are scaled to the resolution t_R by using two multipliers and the value T_{CLK}/t_R is given by the *Measurement Unit*.

Let us analyze the jitter components of this portion of Modulator. The first jitter component is due to the quantization of δ_{RE}/t_R and δ_{FE}/t_R. This error correspond to the error due to the resolution of the Delay-line, and, consequently is independent from the particular architecture and sizing chosen for the *Modulator*. This first jitter component, named $Jabs_{t_R}$, can be easily write:

$$Jabs_{t_R} = 0.5 \cdot \frac{t_R}{I} \tag{2.32}$$

where I is the interpolation factor equal to 32. The second jitter component is due to the errors of the signal T_{CLK}/t_R. As discussed in the previous sections, this signal is affected by a measurement error ($\varepsilon_{TCLK/tR}$) and a quantization error ($\varepsilon 1_{TCLK/tR}$). Note that the maximum value of δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK} is 1/2, therefore the source of jitter due to the errors of T_{CLK}/t_R, named $Jabs_{TCLK/tR}$, can be write:

$$Jabs_{T_{CLK}/t_R} = \frac{1}{2} \cdot \left(\varepsilon_{T_{CLK}/t_R} + \varepsilon 1_{T_{CLK}/t_R} \right) \cdot \frac{t_R}{I} \cdot I \tag{2.33}$$

According to (2.33) we have:

$$Jabs_{T_{CLK}/t_R} \leq 0.483 \cdot \frac{t_R}{I} \tag{2.34}$$

The last source of jitter is due to the quantization of δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK}. By looking the Fig. 2.7, this source of jitter can be easily written as:

$$Jabs_{delayTclk} = \frac{1}{2} \cdot 2^{-u} \cdot \frac{T_{CLK}}{t_R \cdot I} \cdot t_R \cdot I \tag{2.35}$$

By considering the minimum clock frequency (300MHz), the minimum delay-line resolution (21.8ps) we can evaluate this source of jitter in the worst case conditions. Moreover in our implementation u is equal to 13, therefore:

$$Jabs_{delayTclk} \leq 0.299 \cdot \frac{t_R}{I} \tag{2.36}$$

By summing up the three jitter components, the following upper bound for the jitter is obtained:

$$Jabs_{SSCG} \leq 1.282 \cdot \frac{t_R}{I} \tag{2.37}$$

It is worthwhile to highlight that that the (2.37) represent an upper bound for the output jitter, since it assumes the independence of the three jitter sources. Therefore the actual jitter can be substantially lower.

Let us now analyze the jitter components in the *Delay-Line* block. For this purpose the delay lines and interpolators of the *Delay-Line* block have been simulated for all possible control words. The simulations have been done considering a transistor level netlist of the *Delay-Line* block extracted from the layout with the inclusion of parasitic. Note that the layout of *Delay Line Block* have been realized in order to equalizes the parasitic, minimizing the differential non-linearity (DNL) of the DCDLs. The Table 2.7 reports the post-layout simulation performance of the *Delay-Line block* for slow, typical and fast corners. The technology is STMicroelectronics 28nm CMOS. The integral non linearity (INL) values reported in Table 2.7 take into account a several jitter sources: the asymmetries of the t_{min} parameters of the delay lines and interpolators, the linearity error of the delay-lines and the asymmetries of the delays of the XOR gates. It can be observed that the jitter introduced by the *Delay-Line* block is comparable with the jitter introduced by the *Modulator*.

Corner	tmin(ps) LH	tmin(ps) HL	tr(ps)	INL (ps) LH	INL (ps) HL
typ, T=25°, Vdd=1.0V	93.8	88.2	0.98	4.83	4.87
slow, T=-40°, Vdd=0.9V	157.6	161.8	1.65	10.04	10.53
fast, T=125°, Vdd=1.1V	60.9	57.6	0.63	2.30	2.68

Table 2.7. Delay Line block performances obtained by transistor-level simulations.

Finally, a mixed-transistor level simulations have been performed to validate the circuit. Note that in the mixed-transistor level simulation the *Delay-Line* block is described at the transistor level (the netlist includes the parasitic extracted from the layout) and the *Processor* block is described by using a gate level netlist. The simulation results are reported in Table 2.8.

typical process	Jabs max(ps) comp	Jabs max(ps) no comp
Delay Line block resolut.	0.5	0.5
Measurement error	0.2	0.2
INL and asymmetries	3.9	5.4
Total	4.6	6.1

Table 2.8. SSCG absolute jitter obtained by mixed-transistor level simulations.

2.5 On-chip measurement

The circuit has been fabricated in STMicroelectronics 28nm CMOS technology and is included in a 420 pin test chip. The IC Micrograph and the SSCG layout are shown in Fig. 2.14. DCDL placement has been carried out manually; the regular structure in figure 2.10 corresponds to a regular layout. The remaining parts of the circuit have been implemented by place&route tools. The total silicon area is 0.031 mm^2.

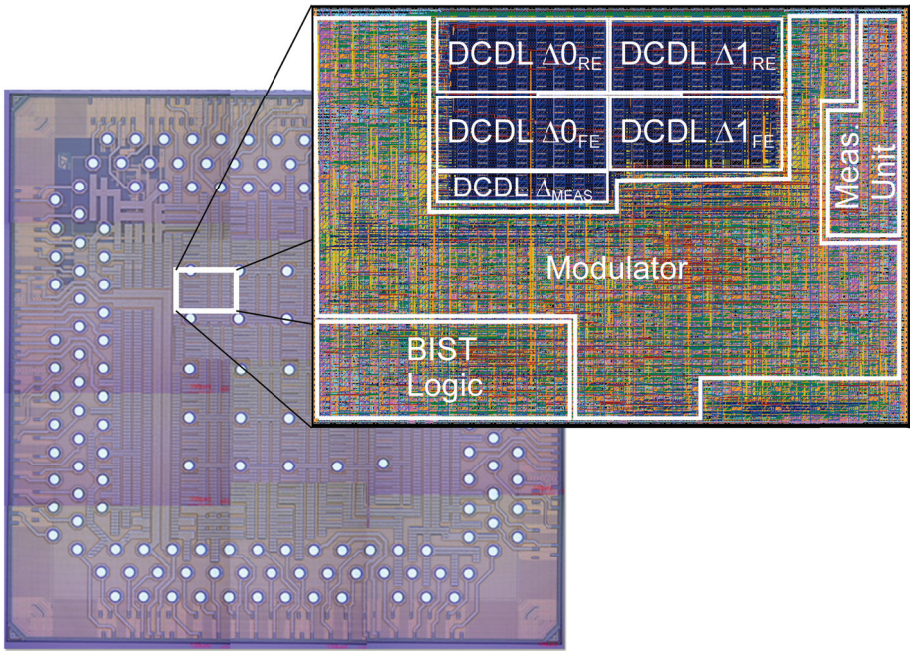

Figure 2.14. SSCG Layout and Micrograph.

The largest block is the modulator. Note that a BIST logic block has been added in order to easy circuit experimental verification. The maximum clock frequency is 1.5GHz, limited by the digital modulator. In the experimental verification a fast corner chip has been verified.

2.5.1 Verification of the Measurement Unit

The verification of the Measurement Unit is the first test performed on the SSCG, since a malfunction of the Measurement Unit compromises the overall circuit functionality. In the realized IC, the signal T_{CLK}/t_R, shown in Fig. 2.1, is available at the output of the chip allowing the constant monitoring of the measured DCDL resolution. The Fig. 2.15 show the measurement unit performances. In particular the figure on the left shows the t_R values obtained by varying the supply voltage, for different input clock frequencies. The right figure displays the measurement spread (Δt_R) given by the maximum difference between the t_R values measured at each supply voltage. As it can be observed t_R measurement are quite accurate with Δt_R lower than 90fs. This gives a strong evidence of the correct operation and performances of the measurement unit.

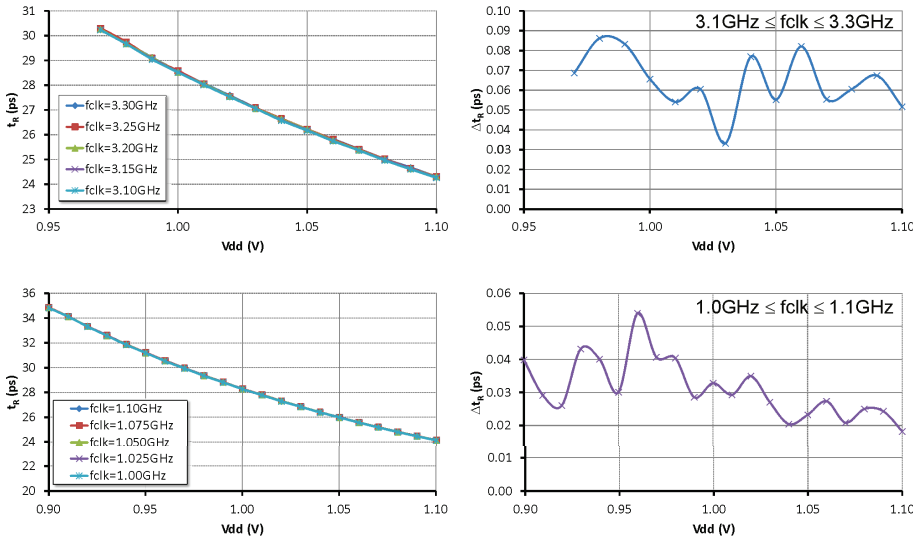

Figure 2.15. Experimental t_R values Δt_R obtained for different supply voltage and clock frequency.

2.5.2 Verification without modulation

The Fig. 2.16 shows the measured jitter of the output clock in the case f_{CLK} = 1.5GHz, f_{OUT} = 490MHz, Vdd=1.0V, obtained measuring the

fast chip when the modulation is turned off. As it can be observed the jitter, measured by using Tektronix TDSJIT software, reduces from 4.09ps$_{rms}$ to 3.16ps$_{rms}$ by activating the delay asymmetry compensation blocks.

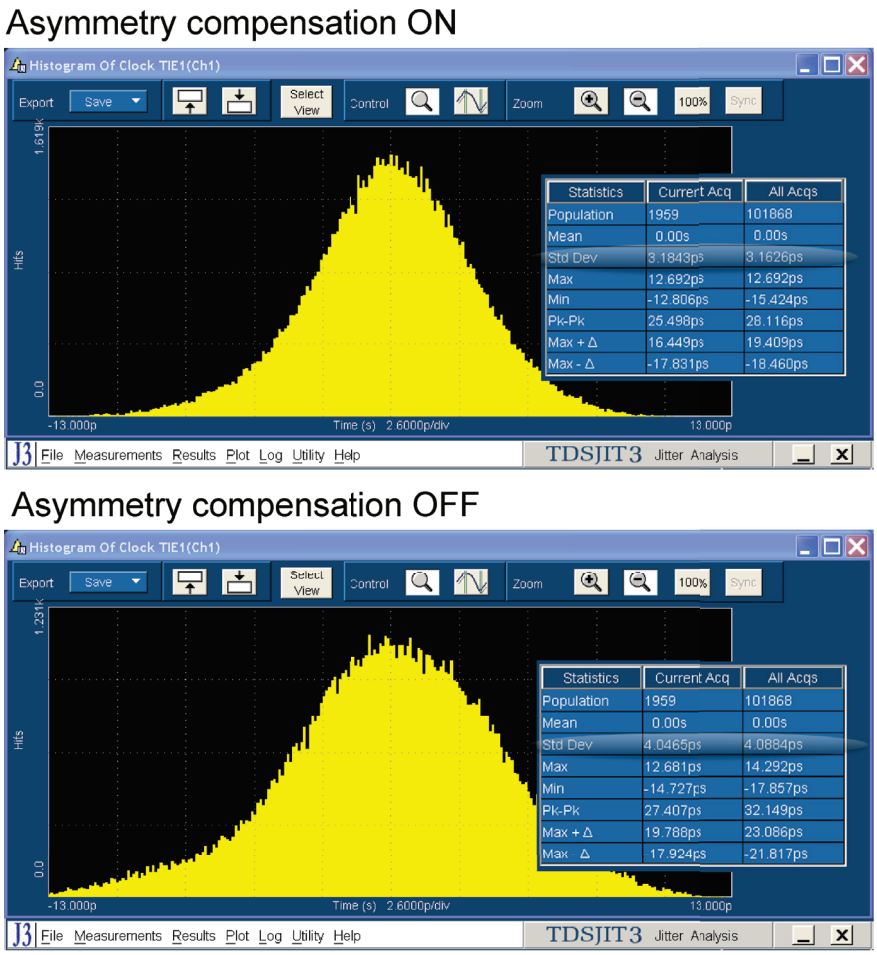

Figure 2.16. Measured Jitter with and without asymmetry compensation (spread spectrum OFF).

It is worth to highlight that in the developed circuit, differently from a PLL, the input jitter adds to the jitter introduced by the circuit. In this operating conditions an input clock jitter of 1.64ps$_{rms}$ (which corresponds to the datasheet performance of employed input clock generator: Agilent 81134A). This allow to estimate the jitter due to SSCG as 2.71ps$_{rms}$. The Tab. 2.9 summarizes the experimental jitter values obtained by using TDSJIT software in different conditions.

f_{OUT}	Jitter (ps)			
	rms		pk-pk	
	comp	no comp	comp	no comp
67 MHz	3.02	4.48	24.80	31.44
112 MHz	3.17	4.06	27.81	29.62
266 MHz	3.26	4.23	28.79	32.39
400 MHz	1.84	3.16	15.31	20.13
490 MHz	3.16	4.09	28.12	32.15
670 MHz	3.28	4.19	29.04	32.94
750 MHz	1.64	2.40	15.82	20.30
875 MHz	3.47	4.32	28.54	36.02
1000 MHz	2.01	2.84	17.27	19.10
1125 MHz	2.79	3.83	23.17	27.57
1250 MHz	2.67	3.78	22.26	31.88
1360 MHz	2.79	3.82	23.44	30.32
1500 MHz	1.96	2.86	14.98	18.31

Table 2.9. Experimental output clock jitter obtained by TDSJIT software with f_{CLK}=1.5GHz and Vdd=1.0V

In the Table 2.9 the performances of the SSCG are reported considering fast chip for f_{CLK}=1.5GHz and Vdd=1.0V. The fast chip have been verified for different output clock frequencies. The data reported in the table confirm the correct circuit operations in all conditions. Please note that for a $f_{OUT}=f_{CLK}$ and $f_{OUT}=f_{CLK}/2$ a very low output jitter is measured. In these conditions, in fact, the input clock is produced by selecting always the same tap of the same delay-line. Therefore, the output jitter corresponds only to the jitter of the input clock signal added to the jitter introduced by the clock tree of the SSCG.

2.5.3 Verification with modulation

The fast SSCG chip has been extensively verified when the modulation is turned on. In this section the most significant measurements are reported. The Fig. 2.17 shows the experimental instantaneous output frequency of the SSCG obtained with f_{CLK}=1.5 GHz, f_m=100kHz, f_{OUT}=1GHz and $\Delta f/f_{OUT}$=10%. Two different modulation profiles have been considered: Hershey-kiss and Sawtooth. The figure shows that the circuit operate correctly by imposing the desired modulation profile in down-spread from the imposed output frequency (1 GHz). This measurements highlights the capability of the SSCG to follow both discontinuous frequency modulations (e.g. sawtooth) or complex modulation profile (Hershey-kiss).

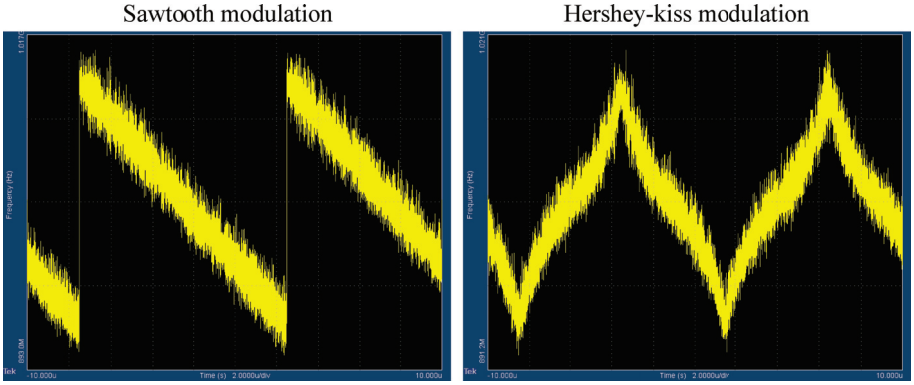

Figure 2.17. Experimental Modulation Profiles by TDSJIT software (f_{CLK}=1.5GHz, f_m=100KHz, f_{OUT}=1GHz, $\Delta f/f_{OUT}$=10% and Vdd=1.0V).

The effectiveness in reducing the EMI spectrum is investigated in figure 2.17 and in figure 2.18. The figure 2.18 shows the experimental peak power level of the output spectrum measured by Agilent PSA E4445A spectrum-analyzer in Peak-mode when the SSCG is configured in order to employ the Hershey-kiss modulation (fig. 2.18a), triangular modulation (fig. 2.18b), sawtooth modulation (fig. 2.18c) and optimal discontinuous modulation (fig. 2.18d) with f_{OUT}=1GHz, f_m=100kHz, RBW=100kHz and 10% modulation depth. The results of figure 2.18 show that the discontinuous frequency modulation can result in an sensible improvement with respect to continuous frequency clock signals.

The Fig. 2.19 reports the amount of reduction of the peak power level reduction of the output clock spectrum at 1GHz with 10% modulation depth, for different modulation profiles and modulation frequencies f_m. The output spectrum is measured by using Agilent PSA E4445A spectrum-analyzer in Peak-mode with a resolution bandwidth (RBW) of 100kHz.

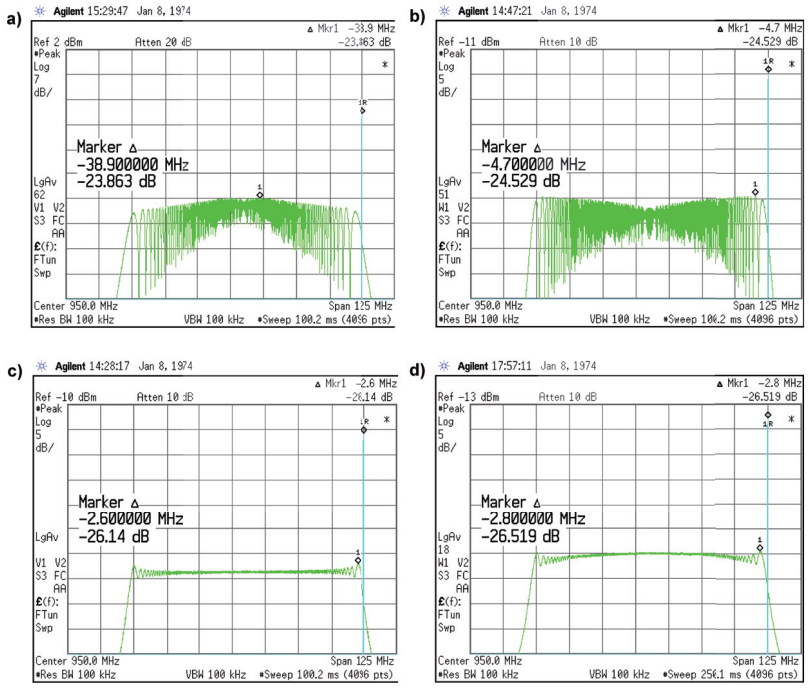

Figure 2.18. Experimental Modulation Gain for different modulation profiles: a)H-kiss modulation b)Triangular modulation c)Sawtooth modulation d)Discontinuous Optimal modulation (f_{OUT}=1GHz, $\Delta f/f_{OUT}$=10%, RBW=100kHz, f_m=100kHz).

To the best of our knowledge, the measurement results of figure 2.19 represent the first experimental verification of the advantages of frequency-discontinuous modulations. The figure, in fact, shows that the highest modulation gain (27dB) is achieved by using the optimized discontinuous modulation profile, which is slightly more effective than sawtooth; compared to the triangular and Hershey-kiss waveforms the improvement in modulation gain is larger than 2 dB. This behaviour is in accordance with the theoretical analysis done in [1] (see section 1.1). The measured spectrum obtained with the

optimal discontinuous modulation for f_m=140kHz is also reported in figure 2.19

As a final test, the capability of the SSCG to realize an instantaneous switching, between two frequencies without clock glitches, is verified. This is experimentally verified by the results of Fig. 2.20 where it is shown the measured instantaneous output frequency when the SSCG is driven in order to switch from f_{out}=750MHz to f_{out}=500MHz. (Hershey-kiss modulation, $\Delta f/f_{OUT}$=10%, f_m=100kHz).

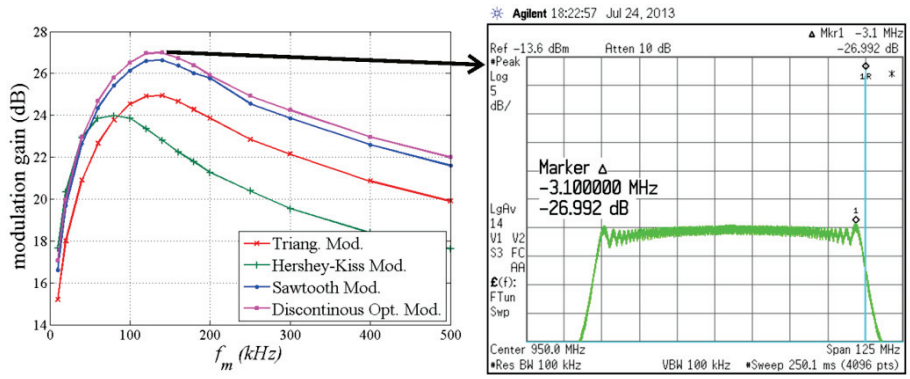

Figure 2.19. Experimental Modulation Gain for different modulation profiles and modulation frequencies (f_{OUT}=1GHz, $\Delta f/f_{OUT}$=10%, RBW=100kHz).

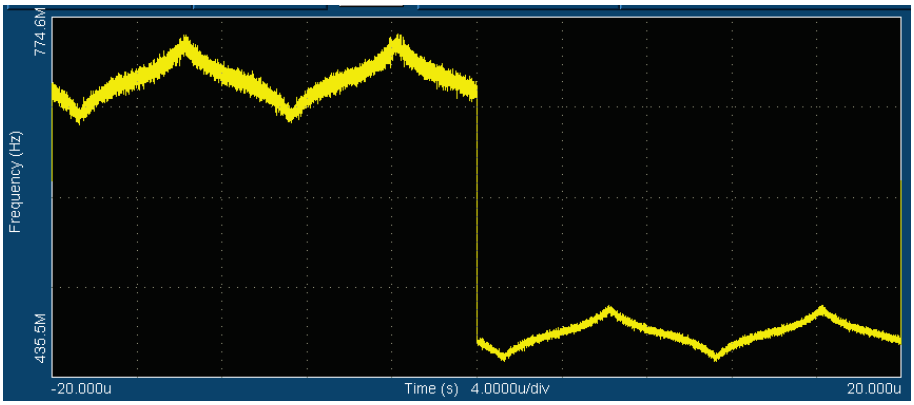

Figure 2.20. Instantaneous output frequency switching from 750MHz to 500MHz (f_{CLK}=1.5GHz, f_m=100KHz, and $\Delta f/f_{OUT}$=10% and Vdd=1.0V).

2.5.4 Comparison with the state of the art

The performances of the IC, considering the fast corner and a supply voltage of 1.0V, are summarized in Table 2.10 and are compared with the previous art. The developed circuit supports discontinuous frequency modulation with an f_m that can be as large as 20 MHz, and, considering measures with RBW=100kHz, presents the highest modulation gain, despite of the employ of a Δf value lower than the previous implementations, which allows achieving very modulation gains for RBW=1MHz (see [1]). The jitter of developed circuit, with few exceptions is comparable with the best PLL implementations. Power and area also compare favourably with respect to published results. Unique features of proposed SSCG are the weak and standby mode and the very low recovery time from full standby.

	Architecture	discontinuous modulation	Modulation Gain (RBW=100kHz)	max f_m	jitter	max f_{out}	tech	Area (mm^2)	Power (mW)	Weak Standby Recovery time	Full Standby Recovery time
This work	All-Digital	yes	27dB @10% of 1GHz	20 MHz	3.16 ps_{rms}	3.3 GHz	28nm	0.031	24.1	8 clock cycles	5.5 μs
Li *et al.*, ISSCC 2012	ADPLL	no	n.a.	25 kHz	10 ps_{rms}	3.6 GHz	22nm	0.030	18.4	n.a.	12 μs
Park *et al.*, ISSCC 2012	ADPLL with inj.-lock DCO	no	n.a.	n.a.	8.05 ps_{rms}	580 MHz	65nm	0.158	10.5	n.a.	n.a.
Da Dalt *et al.*, ISSCC 2013	ADPLL	no	n.a.	n.a.	~100 ps	500 MHz	65nm	0.230	9.9	n.a.	n.a.
Cheng *et al.*, JSSC 2011	ADPLL with true-frac. div.	no	16.1dB @0.5% of 6GHz	32.95 kHz	0.71 ps_{rms}	6 GHz	90nm	0.248	27.7	n.a.	n.a.
Hwang *et al.*, JSSC 2012	FLL with Newton-Raph mod.	no	24.2dB @3.5% of 3.5GHz	95 kHz	2.44 ps_{rms}	3.5 GHz	130nm	0.076	23.7	n.a.	n.a.
De Caro *et al.*, JSSC 2010	All-Digital	no	20.5dB @6% of 750MHz	5 MHz	12.8 ps_{rms}	1.27 GHz	65nm	0.044	44.0	n.a.	n.a.

Table 2.10. Circuit performances and comparison with the state of the art.

2.6 References

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Chapter 3

SSC Generator with injection locking Digitally Controlled Oscillator (DCO)

In this chapter a novel all-digital SSCG with injection locking digitally controlled oscillator (DCO) is presented. The first developed SSCG (Chapter 2) has been redesigned in order to allow the generation of an output clock signal with a frequency higher than the frequency of the input clock signal. In fact, the most important drawback of the previous developed SSCG architecture consists in the maximum output clock frequency limitation that is the output clock can have a frequency as high as the clock frequency of the circuit.
Several modifications and additions have been done in order to include new functionalities and characteristics. The functionalities of this novel circuit are the following:

- Maximum output clock frequency greater than 1.5GHz.
- Multiplication capability (maximum multiplication factor equal to 8).
- Same specification of previous SSCG (e.g. minimum output frequency 300MHz, minimum output frequency 1.5MHz, minimum modulation frequency=18MHz).

The present Chapter is organized as follows. The SSCG architecture is described in the section 3.1. The circuit implementation details are given in section 3.2 where the major sources of deterministic jitter are discussed. The section 3.3 describes the output signal jitter and

presents the post-layout simulation results. Moreover, in this section the future developments of the SSCG implementation are delineated.

3.1 Circuit architecture

The circuit architecture of the SSCG with injection locking is shown in Figure 3.1.

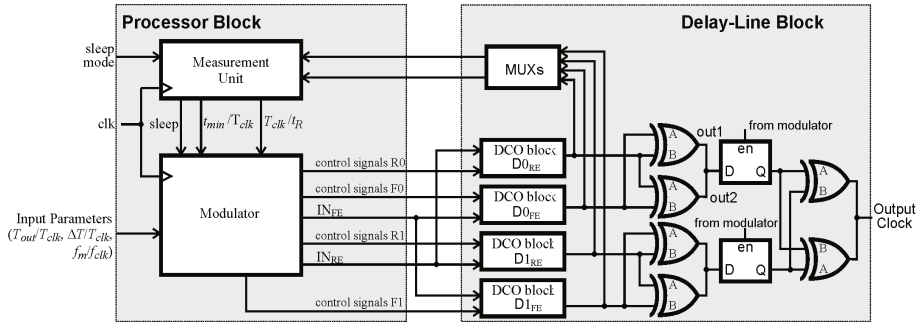

Figure 3.1. SSC Generator architecture.

The system has an input clock signal (*clk*) having a constant period T_{clk} and generates a frequency modulated output clock waveform. This novel architecture allows to perform the clock multiplication in order to obtain an output clock frequency much higher than the input clock frequency. To this purpose a novel *Delay-Line* block is designed by using a DCO-based architecture. In particular, the output clock signal is produced by using a four DCO blocks ($D0_{RE}$, $D0_{FE}$, $D1_{RE}$ and $D1_{FE}$) digitally controlled by the *Modulator*.

All the DCO blocks are employed for both the generation of the output signal and the on-line measurements of the DCO block parameters to compensate PVT variations. In particular, two DCO blocks (e.g. $D0_{RE}$ and $D0_{FE}$) are in charge of generating the output clock edges (*clock generation mode*) while the others DCO blocks (e.g. $D1_{RE}$ and $D1_{FE}$) are in charge for the on-line measurements of the DCO block parameters (*measurement mode*). However, when an on-line measurement is completed, the DCO blocks couple (e.g. $D1_{RE}$ and $D1_{FE}$) switch from *clock generation mode* to *measurement mode*, while the others DCO blocks (e.g. $D0_{RE}$ and $D0_{FE}$) switch from *measurement mode* to *clock generation mode*. Therefore, it is possible to measure the parameter of the DCO blocks which then will in charge of generating the output clock edges. In this way the PVT

compensation is more accurately with respect the architecture of the previous SSCG where a replica delay line was used to compensate the PVT variations (see section 2.1).
The DCO blocks $D0_{RE}$ and $D1_{RE}$ are driven on the rising-edge on the input clock and are in charge of generating up to a maximum of four output clock edges in a timing window of length $T_{CLK}/2$ starting from the input clock rising-edge. Similarly the DCO blocks $D0_{FE}$ and $D1_{FE}$ are in charge of generating up to a maximum of four output clock edges in a timing window starting from the falling edge of the input clock signal. Figure 3.2 shows, as an example, the case in which the DCO blocks $D0_{RE}$ and $D0_{FE}$ are in charge of generating the output clock edges. As you can see, each DCO-block is used for one half clock period, the remaining half clock period is used as timing margin for settling time of DCO block control signals.

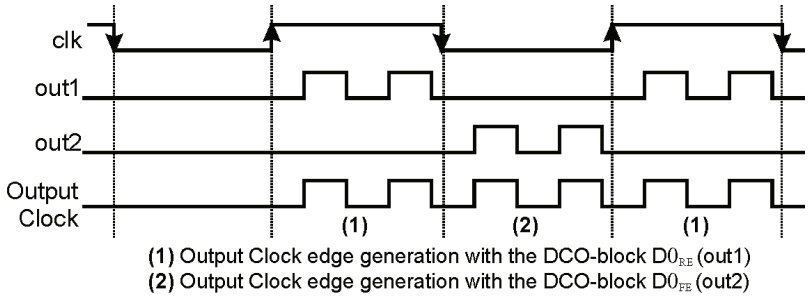

Figure 3.2. Output clock generation.

This topology has the capability to position up to a maximum of eight clock edges within one input clock period. Therefore, the maximum output clock frequency ($f_{out\text{-}MAX}$) is therefore:

$$f_{out-MAX} = 8 \cdot f_{CLK} \tag{3.1}$$

Note that the DCO blocks are employed in order to allow the multiplication of clock frequency that is an output clock signal with a frequency higher than the frequency of the input clock signal. Moreover, as described in the following section, these blocks also allow to implement the injection locking technique in order to mitigate the overall jitter of the circuit.

3.1.1 DCO-block

The employed DCO-block architecture is shown in Fig. 3.3.

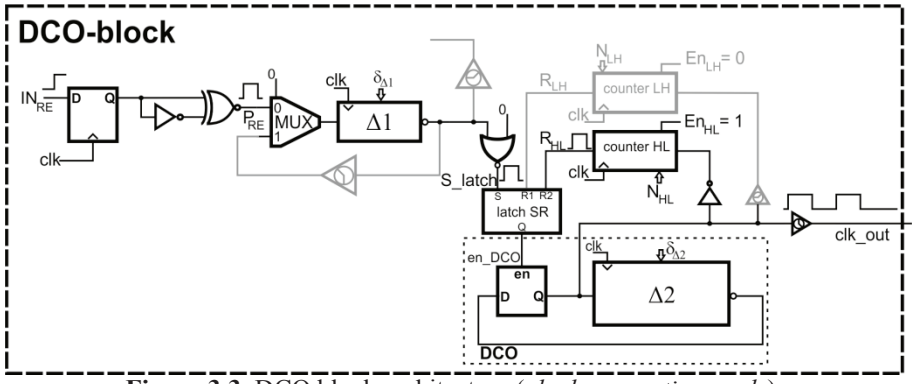

Figure 3.3. DCO block architecture (*clock generation mode*).

This architecture has been implemented by using a design flow based on standard cells. All the inputs are synchronized to the SSCG clock (*clk*) and includes only positive-edge flip-flops.
As you can see in figure 3.3, two delay-line units (Δ1 and Δ2) are employed. Each delay-line unit is realized by using two NAND-based DCDLs where the delay of one DCDL is offset by half resolution and a MUX-based digital delay interpolator, as seen in the previous Chapter (see section 2.1).
The delay line unit Δ2 is used in a ring oscillator topology in order to implement the clock multiplication, while the delay line unit Δ1 is employed to compute the correct position of the output clock edges generated by the DCO.
Let us analyze the operating principle of the DCO block when it is in charge of generating a certain number of output clock edges (*clock generation mode*). As an example, the DCO block of Fig. 3.3 is driven on the rising edge on the input clock. The flip-flop input IN_{RE} has a low to high transition or a high to low transition when at least an output clock edge has to be generated between the next rising and the falling edges of the input clock signal. As you can see in figure 3.3, a pulse generator has been implemented by using an inverter and a XNOR gate. This pulse generator receives as input the flip-flop output and computes the pulse signal P_{RE}. This pulse signal is properly delayed by using the delay line unit Δ1 to compute the set input signal

of the set-reset latch (*S_latch*). In this way, the output of set-reset latch (*en_DCO*) has a low to high transition, therefore the DCO is enabled to generate the output clock edges.
Two edge counters have been implemented in order to stop the clock edges generation. In particular, a rising edges counter (*counter LH*) and a falling edges counter (*counter HL*) have been realized. In fact, since the initial state of the output of the DCO is know and also the number of clock edges that needs to be generate is known, it is possible to choose which kind of counter should be activated for stopping the clock generation.
To clarify this point, in figure 3.3, as an example, four output clock edges are generated and the initial state of the DCO output is considered low. In this case, only the falling edge counter is enabled and only the two falling edges are counted. At the end of the count, the signal R_{HL} becomes high in order to reset the set-reset latch. Therefore, the signal *en_DCO* has a high to low transition and the generation of clock edges is stopped.

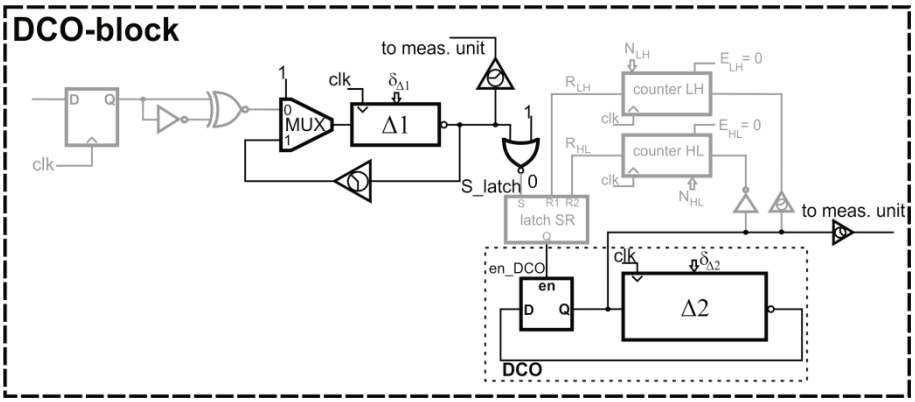

Figure 3.4. DCO block architecture (*measurement mode*).

Note that the architecture of figure 3.3 allows to implement the injection locking technique. The injection locking (see section 1.2.1) is an effective method to reduce the overall jitter produced by the DCO in each clock cycle. In our implementation, the injection locking method is implemented by using the delay line unit Δ1. In particular, the delay of the delay line unit Δ1 is properly choose in order to realign the first generated output clock edge every input clock semi-period. In this way it is possible minimize the jitter accumulated by the DCO in the semi-period.

The DCO block architecture in *measurement mode* configuration is shown in Fig. 3.4. As you can see, in this configuration the two delay line units are separately closed in a ring-oscillator topology for the on-line measurements of the delay line unit resolution t_R and the minimum delay t_{min} in order to compensate the process voltage and temperature variations.
At first the *Measurement Unit* is in charge of evaluating the ratio T_{CLK}/t_R of the delay line unit Δ1, by measuring the ring oscillator output. Afterwards, the *Measurement Unit* is in charge of evaluating the ratio T_{CLK}/t_R and the ratio T_{CLK}/T_{min} of the delay line unit Δ2 (see section 3.1.4).

3.1.2 Edge counter architecture

The edge counter architecture is shown in Fig. 3.5.

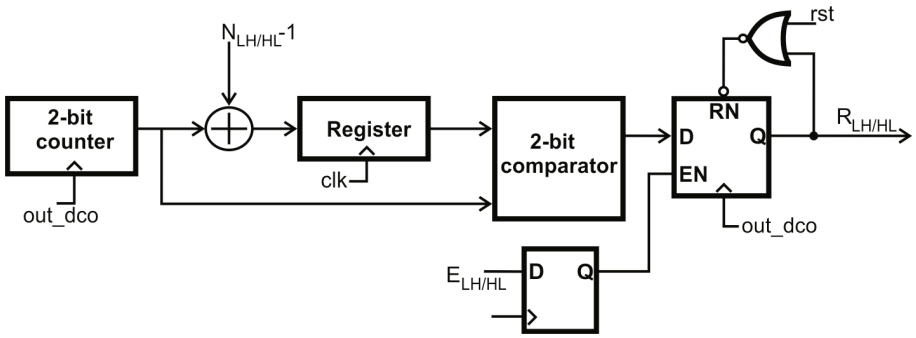

Figure 3.5. Edge counter architecture.

The edge counter receive as input the number of output clock edges that needs to be generated (named $N_{LH/HL}$), the output clock of the DCO (named *out_dco*), the enable signal (named $E_{LH/HL}$) and produce the reset signal (named $R_{LH/HL}$) of the latch SR in order to disable the DCO oscillation.
The *Register* is update with the SSCG clock (*clk*) on the basis of the required number of output clock edges that needs to be generated. Therefore when the *clk* signal has a low to high transition (or a high to low transition for the DCO blocks driven on the falling edge of the input clock signal) the register contain the sum of $N_{LH/HL}$ and the 2-bit counter value. The 2-bit counter and the flip flop are synchronized by the output of the DCO. In this way, the output of the 2-bit comparator

is high when the number of the generated output clock edges is equal to $N_{LH/HL}$-1. Moreover, when the last output clock edge is generated the output of the flip-flop $R_{LH/HL}$ has a low to high transition in order to reset the latch SR. Therefore the DCO oscillation is stopped.
The figure 3.6 show, as an example, a simulation of the DCO-block in *clock generation mode*. In particular a generation of four output clock edges is considered. In this case the falling edge counter is enabled in order to count two falling edges (N_{HL}=2). When the two falling edges are counted the output counter signal R_{HL} has a transition low to high, therefore the set-reset latch is disabled (*en_DCO* becomes low). However, the latch SR needs to be disabled before of the following (the fifth) edge of *clk_out*. This results in a constraint to the maximum output clock frequency.
As shown in the figure 3.6, the post-layout simulation confirm this scenario and the maximum output frequency is equal to 2 GHz (slow corner).

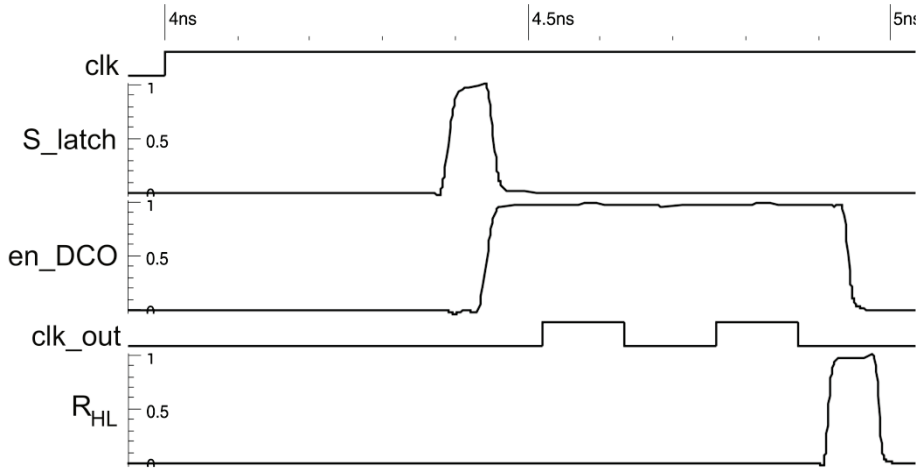

Figure 3.6. Edge counter frequency limitation.

3.1.3 Modulator

The architecture of the *Modulator* block is shown in Figure 3.7.

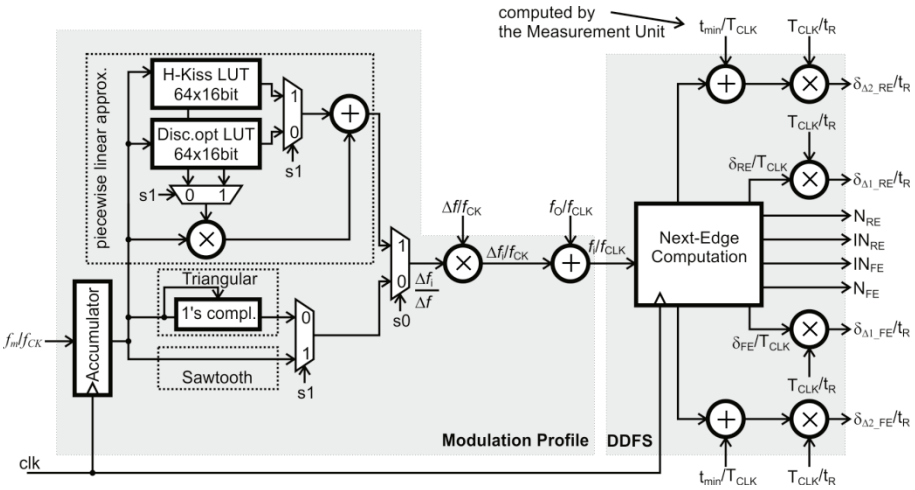

Figure 3.7. Architecture of the Modulation profile and Digital Frequency Synthesizer.

This architecture uses a Direct Digital Frequency Synthesizer (DDFS), which receives the instantaneous frequency f_i of the output clock signal and computes the DCO block inputs IN_{RE} and IN_{FE}, the number of falling/rising output clock edges that needs to be generated (N_{RE}, N_{FE}) and the control signals of the delay lines units Δ1, Δ2, named $\delta_{\Delta1\_RE}/t_R$, $\delta_{\Delta2\_RE}/t_R$, $\delta_{\Delta1\_FE}/t_R$, $\delta_{\Delta2\_FE}/t_R$, for the DCO-blocks that are charge of generating the output clock edges ($D0_{RE}$, $D0_{FE}$ or $D1_{RE}$, $D1_{FE}$). The control signals of the delay lines Δ1 ($\delta_{\Delta1\_RE}/t_R$, $\delta_{\Delta1\_FE}/t_R$) are scaled to the delay line resolution t_R by using two multipliers and the measurement signal (T_{CLK}/t_R) computed by the *Measurement Unit*. Instead, the control signals of the delay lines Δ2 ($\delta_{\Delta2\_RE}/t_R$, $\delta_{\Delta2\_FE}/t_R$) are scaled to the delay line resolution t_R and to the minimum delay of the DCO (t_{min}) by using two multipliers, two adders and the measurement signals (T_{CLK}/t_R, t_{min}/T_{CLK}) computed by the *Measurement Unit*. In fact, the control signals of the delay line Δ2 determine the oscillation frequency of the DCO. In particular, note that when the output clock frequency is higher than the input clock frequency then the DCO generates a certain number of output clock

edges in one input clock semi-period. The period of these output clock edges is:

$$T_{OUT} = 2 \cdot \left(t_{\min} + \frac{\delta_{\Delta 2}}{t_R} \cdot t_R \right) \tag{3.2}$$

where t_{min} is the minimum delay of the DCO equal to the sum of the minimum delay of the delay line and the delay of the enable latch of the DCO (see Fig. 3.3). As you can see, the output clock frequency depends on delay line resolution and on the t_{min}. Therefore it is necessary to measure also the minimum delay for the delay line unit $\Delta 2$ in order to compute the correct output clock frequency (see section 3.1.4).

The instantaneous frequency f_i is computed by the *Modulation Profile*, by adding the desired output frequency (f_o) to the instantaneous frequency deviation Δf_i imposed by the frequency modulation profile. Four profiles are implemented in the circuit. Triangular and saw tooth profiles are realized by suing respectively 1's complementer and the output of the accumulator directly. More complex modulation laws (Hershey-Kiss and the optimal frequency modulation) are implemented by using a piecewise linear approximation where the interval $[0,1/f_m]$ is divided in 64 uniform segments.

The Table 3.1 reports the exact meaning of the *Modulator* inputs. Note that the *Modulation Profile* block is divided by four to reduce the power dissipation. In the worst case ($f_{CLK}/f_{OUT} = 1024$) the maximum relative modulation depth $\Delta f/f_{OUT}$ is 3.1%. Please note that a larger modulation depth can be obtained for $f_{OUT} < 1024 f_{CLK}$. In the worst case ($f_{OUT}/f_{CLK} = 8$) the resolution depth is 1.60%. Finally, in the worst case (f_{CLK} = 300MHz) the maximum modulation frequency is 18.75MHz, while the modulation frequency resolution is 0.07KHz.

Signal	MSB	LSB	maximum	minimum	resolution
$\frac{f_{OUT}}{f_{CLK}}$	2^3	2^{-10}	$f_{OUT} \leq 8 f_{CLK}$	$f_{OUT} \geq f_{CLK}/1024$	$2^{-9} \cdot f_{CLK}$
$\frac{\Delta f}{f_{CLK}}$	2^4	2^{-9}	$\frac{\Delta f}{f_{OUT}} \leq 3200 \frac{f_{OUT}}{f_{CLK}}\%$	$\frac{\Delta f}{f_{OUT}} \geq 0\%$	$0.20 \cdot \frac{f_{OUT}}{f_{CLK}}\%$
$\frac{f_m}{f_{CLK}}$	2^{-3}	2^{-20}	$f_m \leq 62.50 \cdot 10^{-3} f_{CLK}$	$f_m \geq 0$	$9.53 \cdot 10^{-7} f_{CLK}$

Table 3.1. Meaning and range of *Modulator* input signals.

3.1.4 Measurement Unit

This circuit is needed to take into account the PVT variations which modifies the resolution t_R of the delay lines and the minimum delay t_{min} of the DCO. To compensate the variations of t_R and of t_{min} with the PVT operating condition of the circuit, the *Measurement Unit* continuously measures the ratio T_{CLK}/t_R and the ratio T_{CLK}/t_{min} and provides this information to the *Modulator* block (see Figure 3.1). Let us to explain the measurement operation. As shown in Figure 3.4, when the DCO-block is in measurement mode then the delay line unit $\Delta 1$ is closed in a ring oscillator topology. The output period (T_R) of this ring oscillator is given by:

$$T_R = 2 \cdot \left(t_{\min} + \frac{\delta_{\Delta 1}}{t_R} \cdot t_R \right) \tag{3.3}$$

where t_{min} is the minimum delay through $\Delta 1$ plus the delay of the multiplexer t_{MUX} (see Fig. 3.4). The value of t_R can be extracted in the following way. Firstly the delay line unit $\Delta 1$ is driven with $\delta_{\Delta 1}/t_R$ input equal to N_1. The resulting period of the ring oscillator T_{R1} is divided by the prescaler with a division ratio equal to 4 and the frequency divider with a division ratio equal to d'. In the following, let us name $d=4 \cdot d'$. The output of the frequency divider is used as the enable signal of a up/down counter clocked by input clock. At the end of one cycle, the counter content M_1 will be a measure of the half period of the prescaler output:

$$\left(M_1 \pm 1\right) \cdot T_{CLK} = \left(\frac{d \cdot T_{R1}}{2} \right) = d \cdot \left(t_{\min} + N_1 \cdot t_R \right) \tag{3.4}$$

Similarly, a second measurement is performed with $\delta_{\Delta 1}/t_R$ input equal to N_2. Therefore the counter content M_2 will be given by:

$$\left(M_2 \pm 1\right) \cdot T_{CLK} = d \cdot \left(t_{\min} + N_2 \cdot t_R \right) \tag{3.5}$$

By subtracting the previous two equations the unknown t_{min} are deleted from the measurement:

$$M_1 - M_2 = d \cdot \left(N_1 - N_2\right) \frac{t_R}{T_{CLK}} \pm 2 \tag{3.6}$$

Therefore:

$$\frac{t_R}{T_{CLK}} = \frac{M_1 - M_2}{d \cdot \left(N_1 - N_2\right)} \pm \frac{2}{d \cdot \left(N_1 - N_2\right)} \tag{3.7}$$

The *Measurement Unit* evaluates the ratio T_{CLK}/t_R by using an arithmetic unit:

$$\frac{T_{CLK}}{t_R} \simeq \frac{d \cdot \left(N_1 - N_2\right)}{M_1 - M_2} \tag{3.8}$$

Therefore the maximum measurement error of t_R/T_{CLK} is:

$$\varepsilon_{t_R/T_{CLK}} = \frac{2}{d \cdot \left(N_1 - N_2\right)} \tag{3.9}$$

By expanding in Taylor series and truncating at the first order it is possible to evaluate the error on T_{CLK}/t_R measurement:

$$\varepsilon_{T_{CLK}/t_R} = \left(\frac{T_{CLK}}{t_R}\right)^2 \cdot \varepsilon_{t_R/T_{CLK}} \tag{3.10}$$

The total measurement time is equal to:

$$T_{meas} = d \cdot \left(N_1 + N_2\right) \cdot t_R + 2d \cdot t_{\min} \tag{3.11}$$

Please note that by reducing N_2 we improve the measurement error and the measurement time but we increase also the frequency of the ring oscillator. Therefore, the N_2 value is selected as low as possible, by taking account the prescaler maximum operating frequency. In our implementation, t_R=0.68ps in the fast corner and we have chosen N_2=192, obtaining a maximum ring oscillator frequency equal to 3.28GHz (assuming t_{MUX}=0), that is the maximum clock frequency for

which the prescaler has to be designed. Clearly, the maximum clock frequency of the frequency divider will be given by 3.28GHz/4=821MHz. Moreover, in the slow corner (t_R=1.6ps) so the maximum ring oscillator frequency is 1.39GHz and the maximum clock frequency of frequency divider is 1.39GHz/4=349MHz. We have also chosen $N_1=N_2+1024$ and $d=2^{16}$. In this way we have an error:

$$\varepsilon_{T_{CLK}/t_R} = \left(\frac{T_{CLK}}{t_R}\right)^2 \cdot 2^{-25} \tag{3.12}$$

By considering the minimum clock frequency (300MHz) and the minimum delay-line resolution (0.68ps) we can evaluate the error in the worst case conditions:

$$\varepsilon_{T_{CLK}/t_R} \leq 0.71613 \tag{3.13}$$

Moreover, with the chosen parameters, by considering the worst speed corner (t_R=1.6ps), the total measurement time is (assuming t_{MUX}=0):

$$T_{meas} = 154.4\mu s \tag{3.14}$$

Parameter	Value	conditions and annotation
N_1	1216	
N_2	192	
d	65536	
$\varepsilon_{T_{CLK}/t_R}$	0.71613 0.02865 0.12935 0.00517	f_{CLK}= 300MHz, t_R=0.68ps (worst case) f_{CLK}=1500MHz, t_R=0.68ps f_{CLK}= 300MHz, t_R=1.60ps f_{CLK}=1500MHz, t_R=1.60ps (best case)
T_{meas}	154.4μs	t_R=1.60ps (worst case)
f_{clock} prescaler	3.28GHz 1.39GHz	max value in the fast corner (t_R=0.68ps) max value in the slow corner(t_R=1.60ps)
f_{clock} divider	821MHz 349MHz	max value in the fast corner (t_R=0.68ps) max value in the slow corner(t_R=1.60ps)

Table 3.2. Measurement Unit parameters and performances.

Similarly, at the end of this measurement, the *Measurement Unit* measures the resolution t_R of the delay line unit $\Delta 2$. Therefore the same error measurement and the same measurement time are obtained. However, as explained in the previous section, it is necessary to measure also the minimum delay of the DCO. Therefore, the *Measurement Unit* is able to measure the ratio t_{CLK}/t_{min}. By summing up (3.4) and (3.5) we can obtain:

$$M_1 + M_2 = d \cdot \left(N_1 + N_2\right) \frac{t_R}{T_{CLK}} + 2 \cdot d \, \frac{t_{\min}}{T_{CLK}} \pm 2 \tag{3.15}$$

Therefore:

$$\frac{t_{\min}}{T_{CLK}} = \frac{M_1 + M_2}{2 \cdot d} - \frac{N_1 + N_2}{2} \cdot \frac{t_R}{T_{CLK}} \pm \frac{2}{2 \cdot d} \tag{3.16}$$

The arithmetic unit of the *Measurement Unit* evaluates the ratio T_{CLK}/t_{min} as:

$$\frac{T_{CLK}}{t_{\min}} \simeq \frac{M_1 + M_2}{2 \cdot d} \tag{3.17}$$

The maximum measurement error of t_{min}/T_{CLK} is therefore equal to:

$$\varepsilon_{t_{\min}/T_{CLK}} = \frac{N_1 + N_2}{2} \cdot \varepsilon_{t_R/T_{CLK}} + \frac{2}{2 \cdot d} \tag{3.18}$$

The Tab. 2.4 reports the measurement circuit parameters and performances.

3.2 Circuit analysis and sizing

3.2.1 Measurement Circuit Sizing and Limitations

The range of t_R values which the measurement circuit is able to handle is determined by the length of the registers storing *M*1 and *M*2 and the number of bits used for the signal T_{CLK}/t_R in Fig. 3.6.
In this section the limits imposed by the length of M1 and M2 are discussed. The internal architecture of the *Measurement Unit* uses a single up/down counter to measure directly the quantity M1-M2. Initially the delay-line unit ($\Delta 1$ or $\Delta 2$) is driven with $\delta/t_R = N_1$, the up/down counter is cleared and is set for up-counting. Afterward, the Delay-line Δ_{MEAS} is driven with $\delta/t_R = N_2$ and down-counting is selected. Without resetting the counter between the first and the second measure, the final value of the counter will be directly equal to M1-M2. The only condition to impose for the correct circuit operation is that M1-M2 is lower than the maximum value representable within the counter. This condition imposes a constraint on the maximum measurable t_R. Therefore we can write:

$$t_{RMAX} = \frac{2^{L_{M12}} - 1}{d \cdot (N_1 - N_2)} \cdot T_{CLK} \tag{3.19}$$

where L_{M12} is the number of bits of the counter which calculates M_1-M_2. In our case we chosen L_{M12}=23, consequently:

$$t_{RMAX} = 0.125 \cdot T_{CLK} \tag{3.20}$$

In the worst case (f_{CLK} = 1500MHz), the maximum value allowed for t_R is 83ps.
Let us now consider the signal T_{CLK}/t_R (see Fig. 3.6). In our implementation this signal is composed by 14 bits, with a MSB of weight 2^{12} and an LSB of weight 2^{-1}. The LSB weight results in a quantization error of T_{CLK}/t_R given by:

$$\varepsilon 1_{T_{CLK}/t_R} = 2^{-2} \tag{3.21}$$

This is an additional source of error on the signal T_{CLK}/T_R of Fig. 3.6, which adds to the error $\varepsilon_{TCLK/tR}$ described in the section 3.1.4. The MSB weight of T_{CLK}/t_R imposes a limitation on the minimum t_R value which can be measured. The minimum possible t_R value can be written as:

$$t_{RMIN} = \frac{T_{CLK}}{2^{13} - 2^{-1}} \tag{3.22}$$

In the worst case (f_{CLK} = 300MHz), t_{RMIN} is equal to 0.41ps. The Tab. 2.5 summarizes the parameters and limitations of the measurement circuit.

Parameter	Value	conditions and annotation
L_{M12}	23	number of bits M_1-M_2 register
MSB of T_{CLK}/t_R	2^{12}	
LSB of T_{CLK}/t_R	2^{-1}	
$\varepsilon 1_{T_{CLK}/t_R}$	2^{-2}	quantization error of T_{CLK}/t_R
t_{RMAX}	83ps	f_{CLK}=1500MHz (worst case)
t_{RMIN}	0.41ps	f_{CLK}= 300MHz (worst case)

Table 3.3. Parameter and limitations of the measurement circuit.

3.2.2 Jitter analysis and circuit sizing

In this section a theoretical jitter analysis for *Modulator* block is discussed.
The figure 3.7 show the architecture of the *Modulator*. Note that when the modulation is turned-off, $\Delta f/f_{CLK}$ is equal to 0 and, consequently also Δf_i=0. Therefore, in these conditions, no error is introduced by the *Modulation Profile* block. The figure 3.8 show the portion of *Modulator* relevant for the jitter analysis.

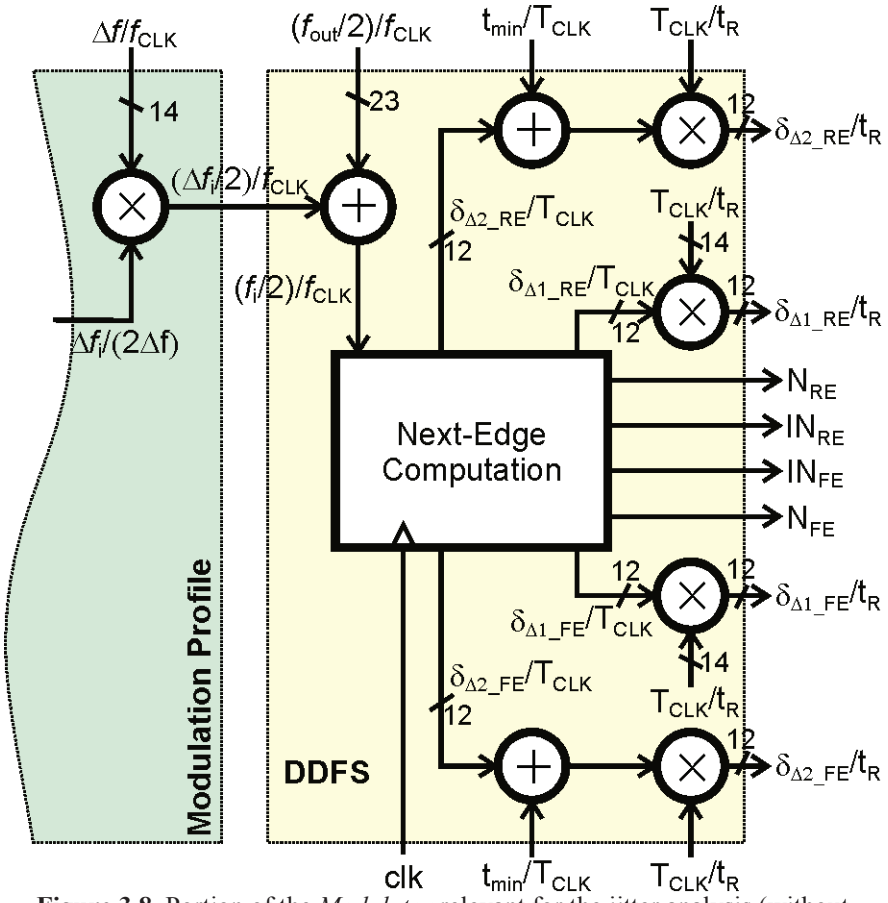

Figure 3.8. Portion of the *Modulator* relevant for the jitter analysis (without modulation).

The DDFS generates the input signals for the DCO-blocks. As shown in Fig. 3.8, this is obtained with the help of a *Next-Edge Computation*

block that is a finite state machine (FSM). The output of the *Next-Edge Computation* block ($\delta_{\Delta1\_RE}/T_{CLK}$, $\delta_{\Delta1\_FE}/T_{CLK}$, $\delta_{\Delta2\_RE}/T_{CLK}$ and $\delta_{\Delta2\_FE}/T_{CLK}$) drive the delay lines and interpolators of the delay line units of the DCO block through a scaling block.
Note that the MSB of δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK} has a weight of 2^{-2} that is the maximum value of δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK} is 1/2. In fact, each clock edge can be positioned in a timing window of one half clock cycle. Let us name 2^{-u} the weight of the LSB of δ_{RE}/T_{CLK} and δ_{FE}/T_{CLK}. In the implementation of Fig. 3.8, these signals are on 12 bit, therefore u=13.
Let us analyze the jitter components of this portion of *Modulator*. The first jitter component is due to the quantization of $\delta_{\Delta1\_RE}/t_R$, $\delta_{\Delta2\_RE}/t_R$, $\delta_{\Delta1\_FE}/t_R$, $\delta_{\Delta2\_FE}/t_R$. This error corresponds to the error due to the resolution of the delay-line, and, consequently is independent from the particular architecture and sizing chosen for the *Modulator*. This first jitter component, named $Jabs_{t_R}$, can be easily write:

$$Jabs_{t_R} = 0.5 \cdot t_R \tag{3.23}$$

The second jitter component is due to the errors of the signal T_{CLK}/t_R. As discussed in the previous sections, this signal is affected by a measurement error ($\varepsilon T_{CLK}/t_R$) and a quantization error ($\varepsilon 1 T_{CLK}/t_R$). Note that the maximum value of $\delta_{\Delta1\_RE}/T_{CLK}$, $\delta_{\Delta1\_FE}/T_{CLK}$, $\delta_{\Delta2\_RE}/T_{CLK}$ and $\delta_{\Delta2\_FE}/T_{CLK}$ is 1/2, therefore the source of jitter due to the errors of T_{CLK}/t_R, named $Jabs_{T_{CLK}/t_R}$, can be write:

$$Jabs_{T_{CLK}/t_R} = \frac{1}{2} \cdot \left(\varepsilon_{T_{CLK}/t_R} + \varepsilon 1_{T_{CLK}/t_R} \right) \cdot t_R \tag{3.24}$$

According to (3.24) we have:

$$Jabs_{T_{CLK}/t_R} \leq 0.483 \cdot t_R \tag{3.25}$$

The last source of jitter is due to the quantization of $\delta_{\Delta1\_RE}/T_{CLK}$, $\delta_{\Delta1\_FE}/T_{CLK}$, $\delta_{\Delta2\_RE}/T_{CLK}$ and $\delta_{\Delta2\_FE}/T_{CLK}$. By looking the Fig. 3.8, this source of jitter can be easily written as:

$$Jabs_{delayTclk} = \frac{1}{2} \cdot 2^{-u} \cdot \frac{T_{CLK}}{t_R} \cdot t_R \tag{3.26}$$

By considering the minimum clock frequency (300MHz), the minimum delay-line resolution (0.68ps) we can evaluate this source of jitter in the worst case conditions. Moreover in our implementation u is equal to 13, therefore:

$$Jabs_{delayTclk} \leq 0.299 \cdot t_R \tag{3.27}$$

By summing up the three jitter components, the following upper bound for the jitter is obtained:

$$Jabs_{SSCG} \leq 1.379 \cdot \frac{t_R}{I} \tag{3.28}$$

It is worthwhile to highlight that that the (3.28) represent an upper bound for the output jitter, since it assumes the independence of the three jitter sources. Therefore the actual jitter can be substantially lower.

3.3 Post-layout simulation and future works

The layout of the DCO-block is shown in Figure 3.9.

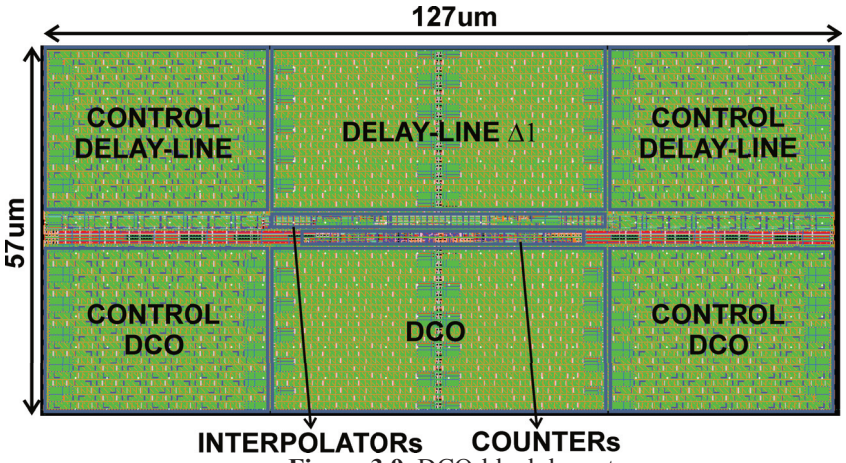

Figure 3.9. DCO-block layout.

Several simulations have been performed in order to realize a jitter analysis of the DCO-block. This analysis is fundamental for different reasons. In fact, this analysis gives an indication of the achievable jitter before completing the RTL design and it sets a specification to

Figure 3.10. : Jitter analysis results in the worst case (typical corner).

verify the SSCG performances. Moreover, the jitter analysis is the way to obtain the asymmetry components that configures the asymmetry compensation block within the RTL. A mixed-signal exhaustive simulations of the DCO-block are employed and a Matlab scripts are developed for the data analysis. The Fig. 3.10 shows the jitter analysis results in the worst case, obtained by varying the control signals of the delay lines of the DCO-block for different number of output clock edges generated. As you can see in figure 3.10, the jitter increase with the increasing of the number of the generated output clock edges.

The layout of the *Delay-Line* block is shown in figure 3.11.

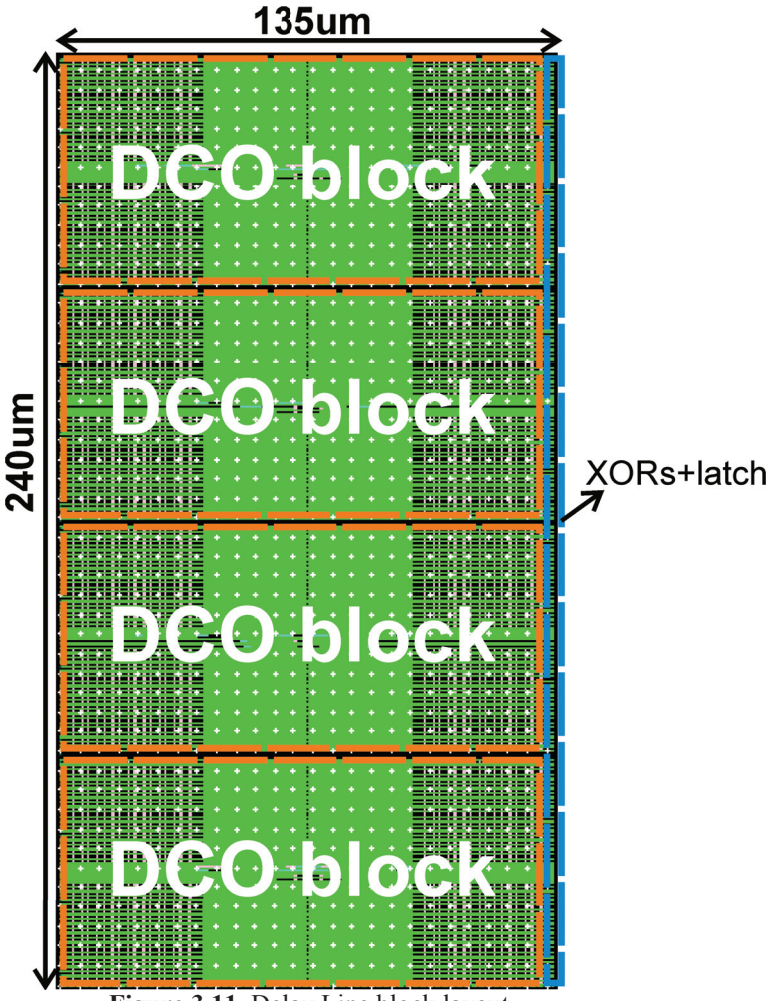

Figure 3.11. Delay Line block layout.

Starting from the analyses and the simulation results presented in this chapter, a several points can be considered as a fundamental to complete the design flow of the SSCG:

- Jitter analysis simulations of the entire SSCG.
- Asymmetries components evaluation in order to configure the asymmetry compensation blocks within the RTL.
- Final RTL including all the features.
- Place and Route of the SSCG.
- Development of a novel test-chip.
- Test-chip measurements.

Conclusions

In the first part of this thesis a prototype of an all-digital Spread-Spectrum Clocking Generator (SSCG) supporting the discontinuous frequency modulation has been presented in all its aspects: design, simulation and fabrication measurements. The developed architecture is based on an all-digital architecture which do not require any loop to implement frequency synthesis and spreading. In addition, the developed circuit can be designed by using a design flow completely based on standard cells, which simplifies the design and porting in new technologies. The circuit is included in a 420 pin test chip implemented in ST 28nm CMOS flip-chip technology. The experimental measurements show the capability of developed SSCG to implement both discontinuous frequency modulations (e.g. sawtooth) or complex modulation profiles (e.g Hershey-kiss). Moreover, these measurement results represent the first experimental verification of the advantages of frequency discontinuous modulations. Another advantage of developed IC is the much larger maximum modulation frequency with respect to previous implementation, which allows achieving very good modulation gains for RBW=1MHz.
The final specifications of the first developed SSCG can be summarized as follows:

	min	max
• circuit clock frequency (f_{CLK})	300MHz	1500MHz
• circuit output frequency (f_{OUT})	-	f_{CLK}
• modulation frequency (f_m)	10kHz	20MHz
• coarse/fine delay-line resolution (t_R)	0.68ps	1.6ps
• modulation depth ($\Delta f/ f_{OUT}$)	0.5%	10%

In the second part of this thesis the first developed SSCG has been redesigned in order to allow the generation of an output clock signal

with a frequency higher than the frequency of the input clock signal. To this purpose a new delay line block has been designed in order to implement the clock frequency multiplication. Furthermore, the injection locking technique is implemented by using a novel DCO-base architecture in order to improve the jitter performance of the circuit. The circuit is realized by using only standard cells and is able to generate an output clock frequency larger of 2GHz with a maximum multiplication factor equal to 8. However, the design flow of this circuit is not yet complete. In fact, a set of simulations to evaluate the jitter performance of the entire SSCG must be performed. This jitter analysis will be used to evaluate the asymmetries components of the circuit in order to configure the compensation blocks within the RTL. Afterwards a final RTL will be realized including all the future. Finally, a place and route of the SSCG may be implemented.

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