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OTFTs for electronic systems: devices fabrication, characterisation, analysis and reliability

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To my father, for the pride I always searched in his eyes.
To my mother, for her endless love that gives me strength.

When the winds of change blow,
some people build walls and others build windmills

-Chinese proverb

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Introduction

Since 1947, the discovery of the transistor effect, until now, electronics has seen many changes due to technological developments that have made possible to achieve the smaller devices with even better performance where the silicon element is well-established and consolidated in that field.

Currently it is trying to realize the new, smaller devices and possibly with higher performance than current ones. An idea, a hope, that represents the research in the field of development of organic conductors based on compounds of carbon. If it is to be placed as a premise that, in the present state of their development, the carbon can not be considered as a substitute for silicon; however the route was traced, to researchers the task of marking a new stage in the march of human history.

The carbon can be, however, defined as a special element for several reasons: first, it has a relatively small size, this reduces clutter in the molecules that contain carbon; has a moderate electronegativity, this entails the possibility of forming covalent bonds ideally with all type of the materials, including other carbon atoms and, belonging to the IV group, it can form four bonds, increasing its chemical versatility and favoring the formation of long polymer chains, it is also possible to hybridize the carbon in various forms, allowing a variety bond configurations that include single bonds, double and triple, as well as a series of resonant forms. Precisely by virtue of these characteristics, the organic chemistry can produce a series of blocks substantially similar wide range of carbon-based materials with optical properties, mechanical and electrical configurable depending on the specific requirements.

After the mid '70s, insights of the work of chemists AJ Heeger , Alan G. MacDiarmid and Hideki Shirakawa, first to reveal the conductive polymer, Nobel Prize for Chemistry in 2000, opened permanently a new era: organic electronics. In respect of the latter, both scientific and commercial interest has grown tremendously in the last ten years.

Important steps in this direction were moved after the construction in 1987 of the first device by the emission of light produced with organic material (OLED), the work of Tang

and Van Slyke[1]. But since the '70s the carbon was studied and research, albeit in an embryonic state, took its first steps in an attempt to create, by the organic material, the semiconductor industry. The initial setback of the research that had focused on the use of polymers, which had proved of poor semiconductors, followed by a new hope related to the use of small molecules. These have an essential advantage: the type of bond between the molecules inside them favors a more ordered morphology, making them more suitable for the conduction of energy. In the face of such advantage, it can not be underestimated various technical difficulties that these materials have, among them, the most pressing is their solubility is not easy, which makes it inappropriate deposition techniques in the liquid phase where the polymer is easily soluble.

Flexibility and availability of materials, convenience, and versatility in their brief, simple deposition techniques and applications on a large area. These are just some of the aspects that have made the organic materials subject to a growing interest in the field of research and investment by many companies. Technological research is a constantly evolving industry, costs and competitiveness on the market impose increasingly stringent specifications: in a twister of new ideas and attractive bets in a society where almost everything is disposable, future prospects are pursued and devoured by the day, the distant horizons become imminent and transform themselves into stimuli for unsuspecting targets. It is, in this context that is increasingly being encouraged and tested the electronics of unconventional materials.

Where the silicon has its limitations, the organic solids are put into play and make their way towards applications even more attractive. The recognition of the benefits of alternative materials and techniques necessary for their daring unfolding are the new frontiers of electronics that innovative research can no longer be removed.

The electronics has made its advantageous characteristics of organic materials, using them for three broad classes of devices, such classes are divided according to their functions: organic thin film transistors (OTFTs), organic light emitting diodes (OLEDs), organic solar cells.

[1] Tang, C. W., and S. A. VanSlyke. "Organic electroluminescent diodes." *Applied Physics Letters* 51.12 (1987): 913-915.

These devices, whose total thickness is between 50 - 200 nm, is made with a stacked structure of thin layers, such a structure in its simplest form consists of anode/organic material/ cathode.

The possible applications of carbon are, today, full expressed: many products currently on the market use applications of organic semiconductors: the latest generation of televisions, mobile phones and MP3 players, which have the OLED display. Probably the commercial products that have employed the first charge transport in organic materials have been laser printers, in which the organic material is loaded and then selectively illuminated by a laser beam which defines the printing areas. Meanwhile, the traditional electronic technology already makes extensive use of polymeric materials sensitive to UV rays, used as photoresist in lithographic processes that require micrometer resolution .

However, the organic materials are characterized by a high value of the bandgap (> 1.5 ev) that causes a low density of thermally generated charge at room temperature and therefore needs, for an effective operation, the injection of free carriers from the external electrodes, in addition, due to the presence of a density of traps is not negligible organic semiconductors exhibit a low electrical mobility. This has led to an increase in the effort for the development of increasingly thinner films.

The progress in the vast field requires a symbiotic union between various disciplines, each indispensable and not subordinated to the other, the chemical helps to define the synthesis of materials and provides training for them and their molecular structure; physics, on the other hand , provides the basic principles for the comprehension of the electronic structure of atoms and molecules, providing even the basic principles of acts to the description of the properties of different materials, synthetic or natural .

This information, combined together, constitute the starting point to find the most suitable techniques to exploit them. In other words placed the focus on the properties possessed by the various materials , in order to find the best location , the best possible use and optimize the process techniques to understand the connection with the performance of the devices.

To extend and improve the market penetration of the organic electronics, the stability of the organic devices is one of the key factors to settle. In this respect, for the strong importance that this theme present, we decided to study the stability of the behavior of the

OTFTs when exposed to different types of stress. In particular, this thesis is dedicated to analyze how the OTFTs behave when they are fabricated varying some process parameters, investigating the relationships between these parameters and some characteristics of the devices under the stress, and identifying the causes of the observed instabilities.

This thesis is divided into two parts: the first, essentially theoretical, makes a brief digression on the literature on the subject, citing a few basic steps, and returns the state of the art of organic technology, and then dwell on that applied to thin-film transistors and their reliability, and the second contains all the experimental work carried out at the ENEA Research Centre in Portici, at the University Federico II of Naples and in collaboration with the electrical characterization laboratory of the University of Algarve in Portugal.

Chapter I describes the molecular structure and the physics of charge transport in organic solids that give rise to semiconductor behavior.

Chapter II introduces the organic TFT. The main function of a field effect transistor is to modulate the current flowing in a conducting channel between the electrodes of the drain and source, through the application of a variable voltage to a third electrode, the gate. Its main application is to switch to pixels in flat panel displays. In the case of a p-type semiconductor, the charges majority are the holes. If there is no voltage at the gate free charges are homogeneously distributed within the whole of the semiconductor layer , but because of their low density, the conductance and hence the current are very low . Negatively biasing the gate an excess of holes is attracted to the surface and will concentrate in this region by a thin conductive layer , leading to a significant increase of the current. The organic TFT do not have particularly high performance. The highest values of mobility in organic solids were obtained in high purity crystals, which have mobility more than $1cm^2/Vs$, better than amorphous silicon, but in the best case have been appreciated mobility equal to $10cm^2/Vs$. The mobility is, however, to be particularly low in organic amorphous , where values are observed around 10^{-5}-$10^{-1}cm^2/Vs$.

Chapter III presents the state of the art concerning the reliability of the OTFT because although they are generally thought of as the macroscopic devices, their behavior is strongly dictated by microscopic phenomena dictated by the molecular interaction. In fact,

the parameters that can affect the stability of the electrical performance can be multiple, and basically can be summed up in two categories:

- Intrinsic parameters of the material , as the molecular structure and the growth mechanism of the film, in which the interface phenomena that have more weight are at the intermolecular level .
- Extrinsic parameters (environmental, light, electrical operation, temperature, etc.) whose presence plays an important role in the stability of the parameters of the devices.

Chapter IV focuses on the choice of materials and manufacturing techniques employed for the realization of the devices. The materials and layers made were carefully evaluated and studied since they, together with the conditions of the process, greatly affect the performances and stability of the devices. The semiconductor selected for the active layer of the transistor is the tips- pentacene, 6,13- bis (tri- isopropylsilylethynyl) pentacene. This organic material is a chemically modified form of pentacene, and has a functional group on the central carbon atom. Functionalizing pentacene molecules have previously been suggested as a means to improve the electronic performance of pentacene, TIPS pentacene is one of the soluble pentacene derivatives with the highest mobility, and it is believed to have better molecular orbital overlap and shows significant potential for improve both mobility and solution processability.

For high performance, gate dielectric materials are also important as the properties of the organic semiconductor layer are largely determined by the gate dielectric. Poly (4-vinylphenol) (PVP) has attract ours attention as a gate dielectric material. It is to be considered specially suitable for tips- pentacene, because it exhibits high insulation with a low leakage current density, it is possible to cross link it and provides a good surface energy for tips- pentacene molecular ordering.

At last, to highlight the strong correlation between process technology and stability of the device we have chosen to dwell experimental studies of four different process parameters for the OTFT realized, which include:

- Two different processing conditions for the dielectric;
- Two different solvents for the semiconductor in which is dissolved.

Chapter V presents the stability analysis performed on devices realized, by comparing the essential parameters useful to discriminate technology resulting more stable on the analyzed aspects, which include:

- **The study of the operational stability of the organic thin film transistor under electrical stress**. The stability has been studied through the analysis of the variation of the threshold voltage over time, after applying to the devices a constant electrical stress on the gate contact.
- **The study of the humidity dependent properties of OTFTs**, to understand the mechanisms involved with the presence of humidity that affect the charge transport in OTFTs.
- **The study of the effect of light pulses on the traps responsible for the operational stability of OTFTs.**

These analyses are designed to obtain information on the instability phenomena and use such information as a useful tool for understanding the dynamics of charge entrapment.
A final short chapter is dedicated to the conclusions.

Chapter 1

General Properties of Organic Semiconductors

The first studies of electronic properties on organic crystals date back to the early 20th century [1,2]. It was, with the discovery of electroluminescence, in the 1960s, [3,4], that the investigations increased and the basic models for the explanation of the charge carrier transport were established [5,6]. The first application of organic semiconductor started only in the 1970s , when the conjugated polymers were successfully synthesized and their doping was controlled [7]. In 1982, the metal-oxide-semiconductor structure was demonstrated, using polyacetylene as semiconductor and polysiloxane as dielectric [8]. Even if the device did not exhibit a great performance, it was recognized as a promising technology.

The milestone of organic electronics technology was the demonstration in 1986 of the first organic field-effect transistor (OFET), or alternatively named organic thin-film transistor (OTFT) [9]. At the same time, the development of the organic heterojunction solar cell [10] and of the organic light emitting diode [11] were reported. Later on, soluble forms of organic semiconductors were developed, opening the possibilities to printable circuits [12,13].

The development and the application of the organic molecules in their various forms (small molecules, polymer chains) are, now, the object of the study of a new discipline, called Organic Electronics, that uses organic molecules instead of the classical inorganic semiconductors normally used for the production of electronic and opto-electronic devices such as transistors, light emitting diode (LED), lighting products, components for optical telecommunications and radio communications, etc..

The main advantages of the use of organic semiconductors are: compatibility with plastic, low processing temperature (60°C ÷ 120°C) compared to traditional semiconductor growth temperatures, environmental compatibility of the preparation techniques (to compare with the complexity and the high risk to the environment and to humans of the techniques required for some

types of inorganic semiconductors), low cost of the deposition processes (such as spin-coating, ink-jet printing, evaporation), and possibility to realize flexible devices on large areas.
Several aspects of the device reliability need to be solved (i.e. environmental stability, lifetime, etc.), before a complete industrialization of this alternative technology becomes a reality,. Device reliability lies on a good understanding of their electrical properties. Nowadays, the charge carrier transport in organic semiconductors and the charge injection phenomenon in the organic/metal and organic/dielectric interfaces are not well understood. For example, the charge injection controls the physics of the device, so a strong comprehension of this interaction is fundamental to reach a good control of the devices characteristics.
In this chapter, it will be analyzed the general properties of the organic molecules, that make it possible to obtain crystals and semiconductor films.

1.1 Materials

Popularly known as "plastics", polymers are large molecules constructed from smaller structural units (repeating units), covalently bonded together in any conceivable pattern [14]. By modifying the repeating units building blocks and the bonding scheme, the mechanical and thermal properties of the polymers can be controlled. Polymers can be made 'rubbery' or brittle, soft or hard, soluble or non-soluble, and practically of any colour by blending with suitable chromophores. The special properties of the polymers allow for a variety of convenient processes, such as injection moulding, spin coating and 'spray' painting. This is in striking contrast to the processing of metals and, even more so, of inorganic semiconductors like silicon. So, polymers can be found in almost all products in our present day society: clothes, furniture, home appliances, cars, airplanes, electronics, packaging, etc..
The idea of utilizing the electrical conductive polymers was not proposed until the 1960's, but since then polymers have been used as active components in a variety of electronic applications. In 1977, it was discovered that an alternating bond conjugated polymer, trans-polyacetylene, could be doped and thereby transformed into a good electrical conductor [15].

This discovery led to the Nobel Prize in Chemistry 2000, being awarded to Profs. A.J. Heeger, A.G. MacDiarmid and H. Shirakawa. Early on, most of the research effort was concentrated to the conducting properties of the doped alternating-bond conjugated polymers, and alternating-bond conjugated polymers were often referred to as "conducting polymers".

Since then, organic conjugated polymers and oligomers have been the subject of numerous studies concerning their semiconducting properties.. As a matter of fact, small molecules (e.g. perylene and C60), oligomers (e.g. tetracene and pentacene), as well as polymers (e.g. polythiophenes) can be used. Figure 1.1 shows the chemical structure of these common organic materials [16] used as active layers in thin film transistors (TFTs) technology All these materials are characterised by an extended system of delocalised π orbitals, along which the charge defects, called polarons and bipolarons, can move. The thin films of these materials, obtained from their deposition, are usually van der Waals type solids, that have the mechanical flexibility typical of many plastic materials.

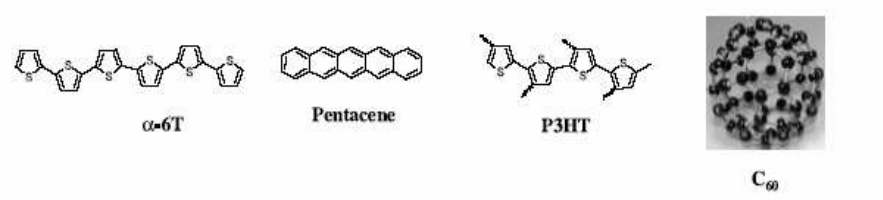

Fig.1.1. Chemical structure of some common organic materials used as active layers in transistors: sexithiophene, pentacene, poly(3-hexylthiophene), fullerene C60.

One of the most fascinating aspects of the active materials employed in OTFTs is the fact that they can be deposited using very low-cost procedures, such as casting or spin coating. This is the case of soluble polymers such as regioregular polythiophenes. Because they are carried out at room temperature these deposition procedures are also thermally compatible with plastic substrates,.

Practical application remains one of the most relavantproblem : organic semiconductor-based transistors are so far only efficient at carrying electronic current via positive charge carriers (holes). To realize a complete electronic circuit based on organic polymers, analogous to conventional silicon chips, devices must also be able to carry negative charge (electrons).

The past decade has seen many efforts to develop the so-called 'n-channel' organic transistors, in which electrons, rather than holes, are the charge carriers [17,18]. Ultimately, the so called 'ambipolar' materials have been studied, i.e. that can be used to create both n-channel and p-channel field-effect transistors (FETs) [19,20]. Until now, materials for making organic and polymer transistors have generally been grouped into two categories, either n-channel or p-channel: traditional organic OTFT materials, such as pentacene and polythiophenes, for instance, are known as p-channel materials. Anyway, experimental results suggest that the difficulty in observing efficient transport of electrons in an organic TFT is an extrinsic effect, caused by factors other than the organic semiconductor material itself. For example, a traditional p-channel OTFT based on pentacene can be converted into an n-channel device by inserting calcium at the interface between pentacene and the thin insulating layer used in transistors [21]. Chua et al. [22] made a convincing case that the trapping of electrons at the insulator–semiconductor interface is indeed the culprit, and they relate this trapping to electronegative hydroxyl (OH) groups in the insulator material. When they use materials that are free of hydroxyl groups, uninhibited electron transport is indeed observed. Chua et al. conclude that if the trapping of electrons by electronegative groups in the insulating layer could be avoided, then n-channel behaviour would be seen in a broad range of organic semiconductors.

Despite the considerable progress made in recent years, achieving high carrier mobilities with organic semiconductors remains inherently difficult, with good mobility values in the range 1÷3 cm^2/Vs [23,24]. Efforts to increase the mobility have been focused on the development of better semiconductor materials, on the understanding of their morphology and of the mechanism of charge transport. Nevertheless, it has been noticed that the interaction between the insulator and the semiconducting materials plays an important role in the carrier transport, because the morphology of the thin interfacial region is likely to be different from the bulk, and the interface has been found to affect the ordering of the molecules [25].

Most of the studies on OTFTs are still made using SiO_2 as the gate dielectric. However, in order to fully benefit the principal advantages of OTFTs, namely low cost, mechanical flexibility and large area electronics, it is highly desirable the use of polymeric gate dielectric materials instead of SiO_2 . The performances of the organic field-effect devices

depends on the use of high-performance dielectrics that form active interfaces with low defects densities [26,27]. High capacitance is certainly desirable, as it allows the reduction of the threshold voltage and of the operating voltage. Threshold voltages may be due to built-in charge, but may also be the indication of interface states (undesirable chemical groups/sites on the insulator itself or foreign impurities) that result directly in carrier trapping. Finally, the polarity of the dielectric interface may also play a role, as it can affect the local morphology or the distribution of the electronic states in the organic semiconductor [28].

In comparison to inorganic heterointerfaces, many aspects of the physics of charge transport along solution-processed heterointerfaces are still poorly understood. For a solution-processed active interface, in which the gate dielectric material is deposited from solution onto a solution-processable semiconducting material or vice versa, it is critical to avoid dissolution or swelling effects during the deposition of the upper layer, which can lead to interfacial mixing and increased interface roughness. This can be avoided by cross-linking the lower layer. This restricts the choice of materials and requires special care to avoid introducing unwanted impurities and trapping groups. An inherent problem in the fabrication of these polymer TFTs is that a polymer semiconductor layer on an insulating layer can get damaged when the second layer is spin-coated onto the existing, underlying layer for the fabrication of the transistor. The chemical purity and composition of the gate dielectric can have dramatic effects on interfacial charge transport. For instance, as previously stated, using appropriate gate dielectrics that are free of electron-trapping groups, such as silanol, hydroxyl, , or carbonyl groups, it can be obtained n-channel OTFT conduction. In contact with trapping-free dielectrics, such as benzocyclobutene (BCB), electron and hole mobilities were found to be of comparable magnitude in a broad range of polymers. Poly-vinylalcohol (PVA), poly-methylmethacrylate (PMMA), poly-vinylphenol (PVP), are some of the most promising materials used as solution-processable gate dielectrics (see Fig. 1.2).

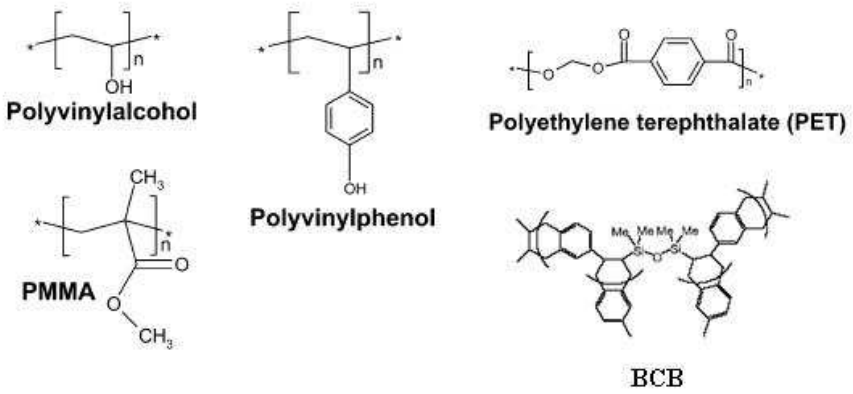

Fig.1.2. Chemical structure of some of the organic materials used as transistors gate dielectric layers.

Another important issue in device fabrication concerns the availability of suitable materials for contacts that, so far, have been mainly fabricated with metals. Metals show several problems: first, they are not mechanically flexible though deposited in very thin layers and this could compromise the overall robustness of the devices; in second place, employing of very simple and low cost techniques for device assembly cannot be applied to metals. Therefore, in an industrial perspective, it would be desirable to employ a unique, easy technique to obtain each layer of the device [29,30]. One of the possibilities is the use of printing contacts with conductive polymers is, but it has several limits, as the spatial resolution of the printed pattern, and the compatibility between the employed "ink" and the printing hardware. Soft lithography [31,32] represents a step forward to obtain low dimensions structures through a reliable, easy, low cost, and reproducible method. It has been successfully applied to organic materials and devices, with very interesting results, and opens a possibility to fabricate flexible and efficient devices with very low dimensions.

A soft lithographic technique can be used to obtain all-organic field effect devices in a very simple and efficient way, realizing contacts with a conducting polymer. Among the numerous electrically conductive polymers that have been studied and developed over the past decades, poly (3,4-ethylene dioxythiophene) doped with polystyrene sulfonic acid (PEDOT:PSS, Fig. 1.3) has appeared to be one of the most successful materials [33,34]. It possesses several advantageous properties: it is water soluble and combines a low oxidation potential and a moderate bandgap with good stability in the oxidized state.

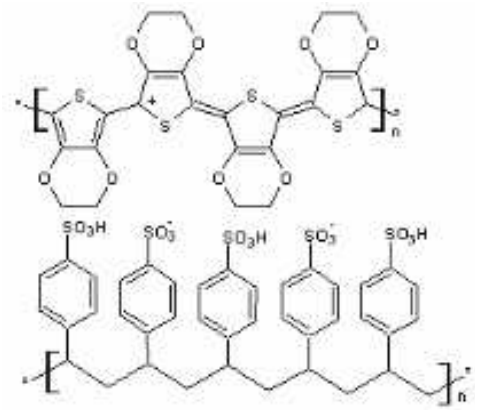

Fig.1.3: Chemical structure of PEDOT:PSS.

1.2 Organic semiconductor

Carbon, in the ground state, has four electrons in the outer electronic level. The orbitals of these electrons may mix, under creation of four chemical bonds, to form four equivalent degenerated orbitals, referred to as sp3 hybrid orbitals in a tetrahedral orientation around the carbon atom. If only three chemical bonds are formed, they have three coplanar sp2 hybridized orbitals which are at an angle of 120° with each other.

These bonds are called σ-bonds, and are associated with a highly localized electron density in the plane of the molecule. The one remaining free electron per carbon atom resides in the pz orbital, perpendicular to the plane of the sp2 hybridization.

The pz orbitals of neighbouring atoms overlap, to form so-called π-bonds [35,36]. A schematic representation of this hybridization is given for the simplest conjugated polymer, polyacetylene (Fig.1.4). Molecules with σ and π-bonds are schematically represented by single and double alternating chemical bonds between the carbon atoms, and are called conjugated molecules. The π-bonds establish a delocalized electron density above and below the plane of the molecule. These delocalized π-electrons are largely responsible for the opto-electronic behaviour of conjugated polymers.

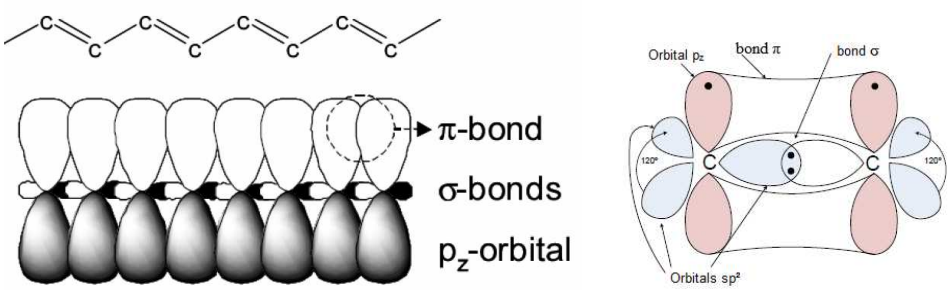

Fig.1.4. Schematic representation of the electronic bonds between carbon atoms in polyacetylene.

The electronic structure of these compounds is based on highly conjugated π electrons.

The π-bond and electronic transitions can be explained by the model based on 'Molecular Orbital (MO) [37]. According to this model, also called the LCAO (Linear Combinations of Atomic Orbitals), the wave functions of the molecule (Ψ_{mol}) can be obtained by a linear combination of wave functions of the atoms (Ψ_i) that constitute it, such as:

$$\Psi_{mol} = a_1\Psi_1 + a_2\Psi_2 + ... + a_n\Psi_n$$

The energy eigenvalues depend on the value assumed by the overlap integral, which depends on the degree of overlap of the atomics wave functions involved, and by the resonance integral, which represents the part of the energy due to the influence of all atomic nuclei on the electrons:

$$\varepsilon = \frac{\int \Psi^o \hat{H} \Psi d\tau}{\int \Psi^o \Psi d\tau}$$

where ε is the energy eigenvalue, the numerator integral is the resonance integral, the denominator is the overlap integral, Ψ^o is the complex conjugate of the wave function Ψ, and H is the Hamiltonian operator.

The electrical properties of the molecule depend, above all, on the type of atomic wave functions combined.

From the orbital theory, molecular orbitals are always equal in number to the atomic orbitals made available by the atoms combined. From the linear combination of two atomic orbitals of the s-type (spherical), or two p-type orbitals oriented along the line joining the two atoms (eg. type px), molecular orbitals are obtained, following the sum or the difference of the two related atomic wave functions. These orbitals have the property to have cylindrical symmetry respect to the axis of the bonded atoms. In the case the

molecular orbital results from the sum of two atomic wave functions, the electrons are concentrated between the nuclei of the two atoms and, therefore, there is an increase of the electron density in the region of the overlap. This orbital takes the name of molecular orbital binder and it has lower energy compared to the energy of the atomic orbitals from which it comes.

The other combination, obtained by subtraction of two wave functions, on the other hand, creates the so-called anti-bonding molecular orbital (from the apex marked *). The electron density between the two cores is reduced, while it increases in the outer regions. In the molecular orbitals, both binders and antibonding, the electrons are confined, however, between the atoms involved in the bond that is of covalent type, therefore very strong. From this strong localization, the organic molecules with these orbitals are electrically insulating.

In the case in which two overlapping atomic orbitals are perpendicular to the line joining the two atoms (pz), the resulting orbitals are characterized by a symmetry to the nodal plane (the planar surface in which the probability to find the electron is zero) and they are said π orbitals. In this case, the electrons are delocalized over several adjacent atoms. Because of this delocalization, the energies of these molecular orbitals have lower values than those of the σ-type orbitals. Furthermore, this delocalization of the electrons makes it simple to displace them using an electric field, and then these organic molecules (at least along the direction of the link) are conductive.

So, as for the inorganic semiconductors we speak of valence band and conduction band to describe the energy levels that electrons must acquire to become a free carrier, for organic semiconductors we use the acronyms HOMO (Highest Occupied Molecular Orbital) and LUMO (Lowest Unoccupied Molecular Orbital) (Fig.1.5): the highest occupied molecular orbital (or HOMO) is the energy level at the top of a continuous band of occupied states, whereas the lowest unoccupied molecular orbital (or LUMO) is the first available energy level in the unoccupied band.

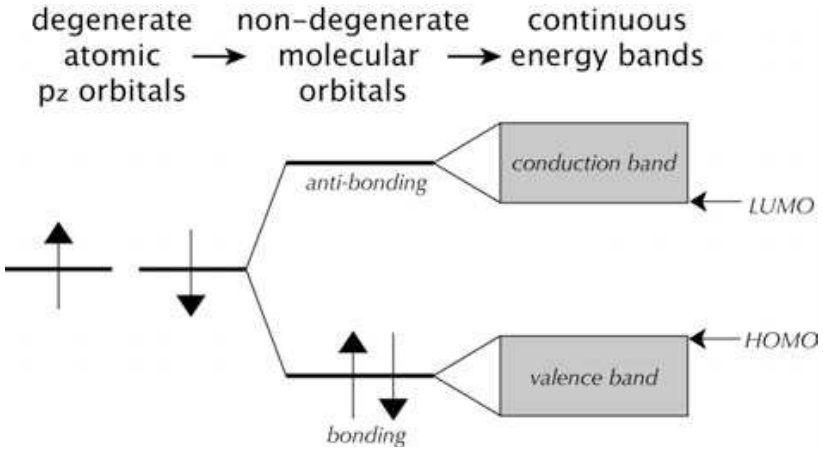

Fig.1.5. Energy diagram, valence (HOMO) and conduction (LUMO) bands.

There are large differences between the three-dimensional crystal lattice of most inorganic semiconductors and the amorphous structure of conjugated polymers. Inorganic semiconductor crystalline lattices, such as silicon and germanium, are characterized by long range order and strongly coupled atoms, in which silicon atoms are tightly held together by strong covalent bonds, with energies on the order of 70 kcal/mole for Si-Si bonds. For silicon and germanium, this results in the formation of long-range delocalized energy bands separated by a forbidden energy gap [38]. Charge carriers added to the semiconductor can move in these energy bands with a relatively large mean free path. These materials are very sensitive to chemical impurities, which modify the number of the charges in the energy bands: artificial addition of chemical impurities, and the effect of this, is called doping of a semiconductor. They are also marked by the presence of dangling bonds at their surface, leading to the high sensitivity of their electrical properties to surface states. The limiting factor for this band transport is scattering of the carriers by thermal lattice vibrations, i.e. phonons [37,38]. This is depicted schematically in Fig.1.6. As the number of lattice vibrations decreases with decreasing temperature, the mobility of the charge carriers increases with decreasing temperature.

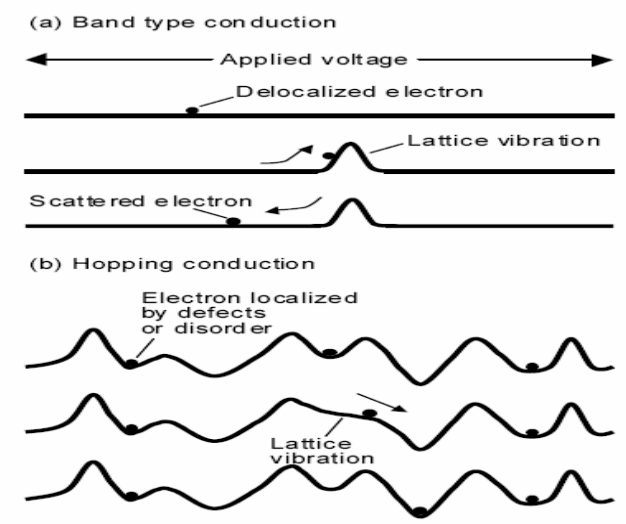

Fig.1.6. Charge transport mechanisms in solids: (a) band transport in a perfect crystal; (b) hopping transport.

1.3 Charge transport mechanisms

Semiconductors are divided into two types: intrinsic and extrinsic ones [39].

An intrinsic semiconductor is an insulator at very low temperature, but the band gap is small enough that the conduction band can partly be populated at room temperature. E.g. undoped silicon belongs to this class (Fig.1.7).

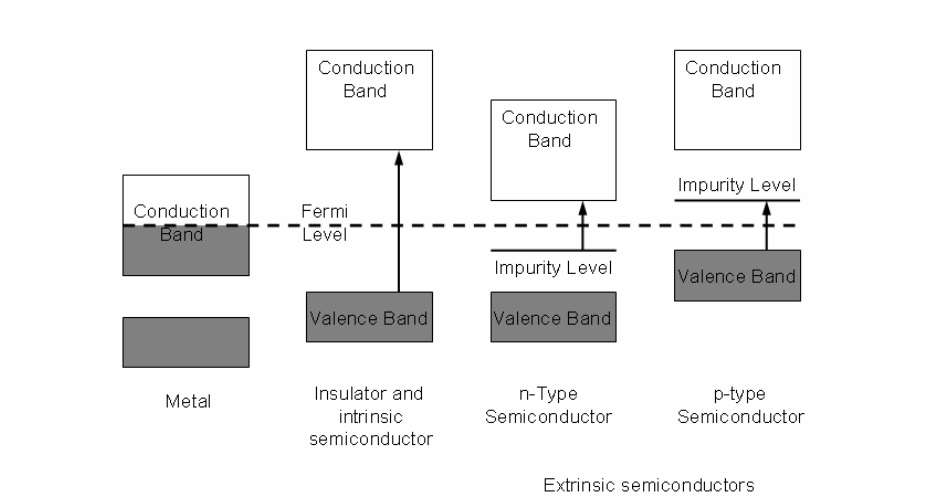

Fig.1.7.. Energy diagrams of a metal, an insulator or intrinsic semiconductor and two types of extrinsic semiconductors [39].

Doping of intrinsic inorganic semiconductors induces localized energy levels close to the conduction (n-type) or valence (p-type) band edge (Fig.1.7, extrinsic semiconductors). By this technique, the energy for the introduction of an electron or a hole in the material is tremendously lowered, and the compound becomes more suitable for the fabrication of the devices. But, only few inorganic materials can be produced with sufficient purity to this purpose, while most organic semiconductors are contaminated with relatively high amounts of both kinds (p- and n-type) of impurities. Due to these intrinsic impurities in organic semiconductors, doping in the range of some parts per million (ppm) (usually done in silicon) has no significant effect, whereas higher doping, in the range of some percent, will turn an organic semiconductor into a conductor and make the compound useless for electronic devices. Hence, organic semiconductors are more similar to insulators than inorganic semiconductors, and different models for the charge transport in the solid state are described in literature [39,40].

1.4 Charge Carrier Transport in Organic Materials

The charge transport mechanism in molecular organic solids differs significantly from that of inorganic semiconductors, because in organic materials normally ionic molecular states, i.e. radical cations and anions, are involved [41]. In molecular solids, electrons or holes have to move from one molecule to another and these ionic states are stabilized by polarization energies in the crystal. Due to these exciton binding energies, the optical gap is significantly smaller than the single molecule gap to create an uncorrelated electron-hole pair (Fig.1.8, E_g and E_{opt}). Furthermore, the active layer in most OFETs is not single crystalline and the energy levels of valence and conduction bands of polycrystalline or amorphous layers are less discrete, due to varying polarization energies of different molecular environments (Fig.1.9). The contribution of different defects or trapping states on the hopping transport was described by Bässler et al. with a Gaussian distribution [43]. The spatial and energetic disorder in the semiconducting layer is proportional to the bandwidth of the Gaussian density of states.

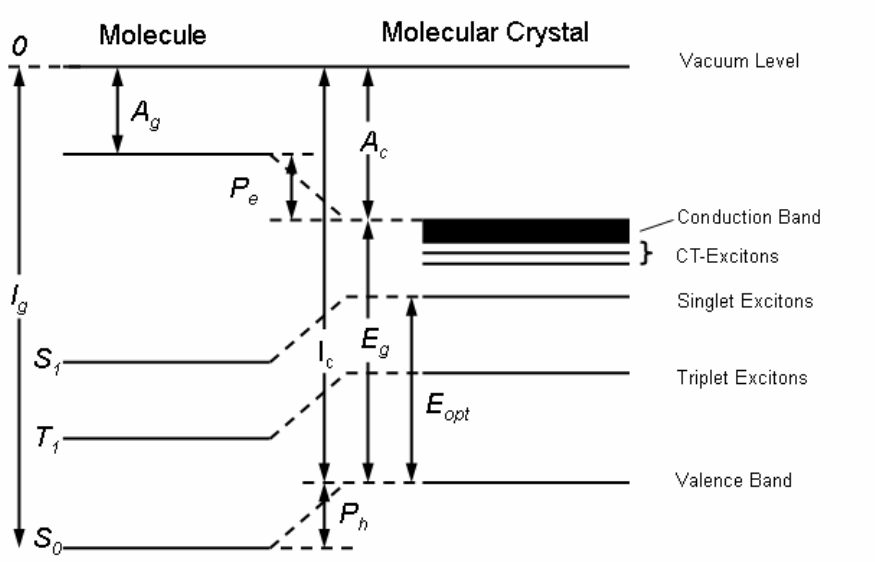

Fig.1.8. Energy levels of isolated molecule and molecular crystal. S_0, S_1, and T_1 = singlet and triplet states, I_g and A_g = ionization potential and electron affinity in gas phase, I_c and A_c = the respective quantities in crystal, P_e and P_h = polarization energies, E_g = single particle gap, E_{opt} = optical gap [40].

Otherwise, the band transport model, as it can be used to describe carrier transport in silicon-based devices, can only be applied for highly ordered organic single crystals at low temperatures. Compared to inorganic materials, the bandwidth of organic crystals is still very small and the measured charge carrier mobilities range from 1 to ~35 cm^2/Vs, which is comparable to the mobility in amorphous silicon [44-47]. As regards high purity crystals, different measurement techniques showed increasing mobilities with decreasing temperatures, suggesting band transport instead of hopping. This inverse temperature dependence of the charge carrier mobility μ can be expressed by equation

$\mu \propto T^{-n}$ *(con n = 1…3)* (1)

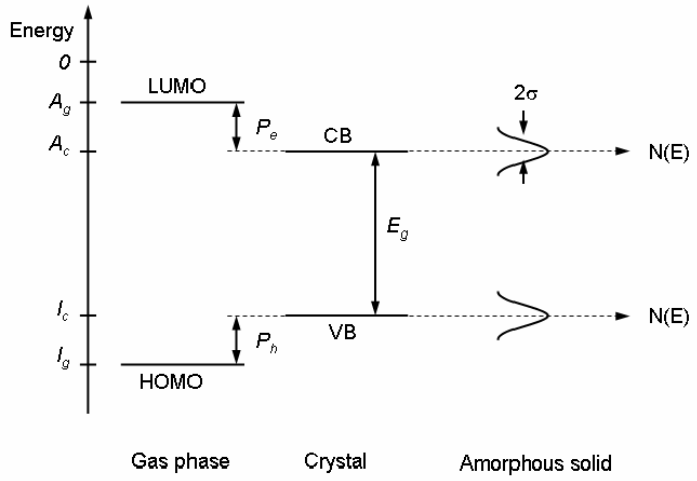

Fig.1.9. Energy levels of isolated molecule, molecular crystal, and amorphous solid. I_g and A_g = ionization potential and electron affinity in gas phase, I_c and A_c = the respective quantities in crystal, P_e and P_h = polarization energies, E_g = single particle gap [40].

Contrary to organic crystals, disordered organic materials do not form energy bands, due to low molecular interactions among the molecules based on Van der Waals forces. Some models have been developed to explain theoretically the temperature and electric-field dependencies of charge carrier drift mobility.

The **Poole-Frenkel model** (equation 2) demonstrates empirically the dependency of charge carrier mobility from the temperature and electric-field [45,46]. Many experimental results for organic disordered systems are in good accordance to this model.

$$\mu = \mu_0 \exp\left(\frac{E_0 - \beta_{PF}\sqrt{F}}{kT_{eff}}\right), T_{eff} = T^{-1} - T_0^{-1} \qquad (2)$$

E_0 = activation energy in the absence of electric field, β_{PF} = the Poole-Frenkel coefficient, F = electric field, k = Boltzmann constant, T_0 = temperature at which the extrapolated data of Arrhenius plots for various electric fields intersect with one another, μ_0 = mobility at T_0.

According to the **small-polaron theory**, the charge carrier hopping is supported by phonons [45,48]. This means that charge carrier transport occurs by hopping of small polarons among localized states, and the mobility of a small polaron in the limit of zero electric field can be calculated according to equation 3. The dependence of activation energy for charge transport in doped polymer systems on the spacing between the molecules has been explained with terms of this model.

$$\mu = (e\rho^2 / kT)P(\omega/2\pi)\exp\left[-\left(\frac{E_p}{2} - J\right)/kT\right] \qquad (3)$$

μ = mobility, e = elementary charge, ω = phonon frequency, J = overlap integral, E_P = polaron binding energy, ρ = spacing between molecules, P = probability of a charge carrier hopping in the case of energy coincidence (adiabatic regime: $P = 1$, nonadiabatic regime: $P < 1$), k = Boltzmann´s constant, T = temperature.

The **disorder formalism** includes the energetic and positional disorder of the system [45,43,48]. It can be assumed that the transport takes place by hopping through multiple localized states, which are influenced by the fluctuations of hopping site energy and

intermolecular wave function overlap. The hopping site energy and intermolecular distance are in accordance with the Gaussian distributions. The mobility is given by the equation 4.

$$\mu = \mu_0 \exp\left[-\left(\frac{2\sigma}{3kT}\right)^2\right] \exp\left\{C\left[\left(\frac{\sigma}{kT}\right)^2 - \sum^2\right]\sqrt{F}\right\} \quad (4)$$

σ and Σ = parameters that characterize the energetic and position disorders, μ_0 = hypothetical mobility in the disorder-free system, F = electric field, C = empirical constant, k = Boltzmann´s constant, T = temperature.

Finally, the **multiple trapping and release model** assumes that highly concentrated localized levels act as traps for a defined delocalized band. By interacting with these levels, the charge carriers are trapped and then released thermally. For this model, some interactions are postulated. Carriers arriving at a defect are trapped with a very high probability near to 1 and the release of the carriers is thermally controlled. The drift mobility μ_D is related to the mobility μ_0 in the delocalized band by an expression of equation 5 [42,49]. This model is widely used to explain charge transport in amorphous silicon.

$$\mu_D = \mu_0 \alpha \exp\left(-\frac{E_t}{kT}\right) \quad (5)$$

μ_D = drift mobility, μ_0 = mobility in the delocalized band, α = ratio of the effective density of state at the delocalized band edge to the concentration of traps, E_t = distance between the trap level and the delocalized band edge, k = Boltzmann´s constant, T = temperature.

Besides charge carrier mobility, the charge carrier density is also essential for the operation mode of the OTFTs. The charge carrier density can be calculated with the equation 6 [40].

$$n_i = N_0 \cdot \exp(-E_g / 2kT) \quad (6)$$

n_i = charge carrier density, E_g = energy gap, N_0 = effective density of states, k = Boltzmann´s constant.

With values of E_g = 2.5 eV and N_0 = 10^{21} cm^{-3} for an exemplary organic semiconductor, carrier densities of only n_i = 1 cm^{-3} can be found. Although the real density should be higher due to inevitable impurities, the corresponding value for silicon (E_g = 1.12 eV and N_0 = 10^{19} cm^{-3}) is about n_i = 10^{10} cm^{-3}. Therefore, it can be anticipated that particular impurities are responsible for charge carrier mobility in organic materials, and it is always

not sure whether the obtained values are genuinely for the organic material or owing to some unintended dopants.

In conclusion, the viability of organic electronics does not lie in the displacement of existing applications niches currently filled by conventional semiconductors, but rather lies in capturing the low cost and enormous variability inherent in organic systems that are otherwise not accessible. Success in achieving very low-cost electronics hinges almost entirely on the ability to deposit and fabricate organic electronic devices using methods that represent a revolutionary departure from those commonly used by the current high-performance electronics industry. However, much work must be done before such an ambitious goal can be realized. Although many innovative technologies have been developed relating to the fabrication of thin-film organic devices with high performance and long operational lifetime, very few of these technologies have left the laboratory. As the most sophisticated and versatile methods currently being developed in the laboratory make their way into the manufacturing environment, we can expect that organic electronic circuits, whose functions are only now being envisioned, will one day revolutionize the technological world in which we live.

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Chapter 2
Organic Thin Film Transistor

Organic semiconductors (OSs) have been studied since the late 1940's [1]. Main advantages of OSs based devices are low manufacturing cost due to low temperature processing, suitable mechanical properties that allow fabrication of flexible devices, and possibility of large area device fabrication. However, despite a large number of experimental and theoretical studies, electronic and optoelectronic organic devices have started to be marketed only in recent time.

A huge breakthrough was made in the mid-1980's, with the presentation of a low voltage efficient organic light emitting diode (OLED) [2]. Further progress has been made during the 1990's, when the pentacene-based organic thin film transistors (OTFTs) reached charge carrier mobility of the order of 1 cm²/Vs [1], which is comparable with the charge carrier mobility in amorphous silicon [5]. Recently, some prototypes of organic solar cells (OPV, organic photovoltaics) and OLED TV sets have been presented on the market (Fig.2.1).

Fig.2.1. (top left) LG OLED 55" TV set; (top right) OSRAM "Orbeos" OLED lamps; (bottom left) PHILIPS "Lumiblade" OLED lamps; (bottom right) Heliatek OPV prototype.

For the OTFTs, since their demonstration in the mid 1980s [4], their performances have been continuously improved. In particular, a tremendous improvement in the charge carrier mobility μ of the OSs was observed during the last years, which is attributed to the synthesis of new organic materials, to the optimisation of deposition methods and parameters, and to the optimisation of electrical contacts [1,3]. Fig.2.2 shows the trends of mobility values for the most important groups of OSs that are under research from the mid-80's.

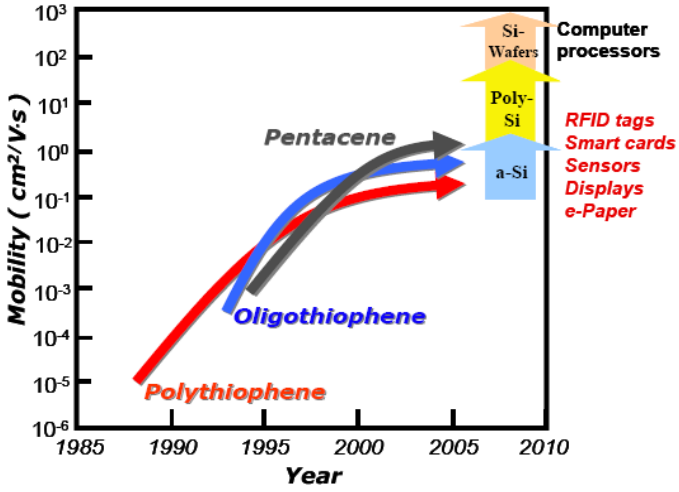

Fig.2.2. Evolution of OTFTs hole mobility for the most common p-type organic semiconductors. Representative ranges of electron mobility for silicon transistors are shown as a reference [1].

Very recently, OTFTs carrier mobilities in some high-performances devices are well beyond 1 cm²/Vs [69]. More importantly, noteworthy progress has been made in the application of OTFTs from laboratory to commercial products [6,7].

In this chapter, a review on the progress in OTFTs is given. First, the basic concept of OTFTs and mechanism of charge injection into organic semiconductor are introduced. Then, the most used organic semiconductors for OTFTs are reviewed.

2.1 Charge injection into organic semiconductor

Together with the charge transport along an organic semiconductor film, another important subject to describe the properties of OTFTs is the physical behaviour of the metal/organic semiconductor interfaces. These ones too are very important and can

strongly influence both the type and the amount of charge carriers injected into a semiconductor.

In principle, all organic semiconductors should allow both types of charge carriers transport. Therefore, achieving n-type or p-type conduction should only depend on the metal employed for the electrodes, that should be able to efficiently inject one type of charge carriers into the semiconductor layer. Indeed, charge injection strongly depends on the energy level matching between the Fermi level of the metal electrode and the organic semiconductor energy levels, namely, lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO). One of the fundamental aspects of the metal/semiconductor interface is the Fermi level alignment, described by the Mott-Schottky model [63,64]. When a neutral metal and a neutral semiconductor are brought in contact, the Mott-Schottky model predicts that their bulk Fermi levels align, causing the band bending in the semiconductor (Fig.2.3).

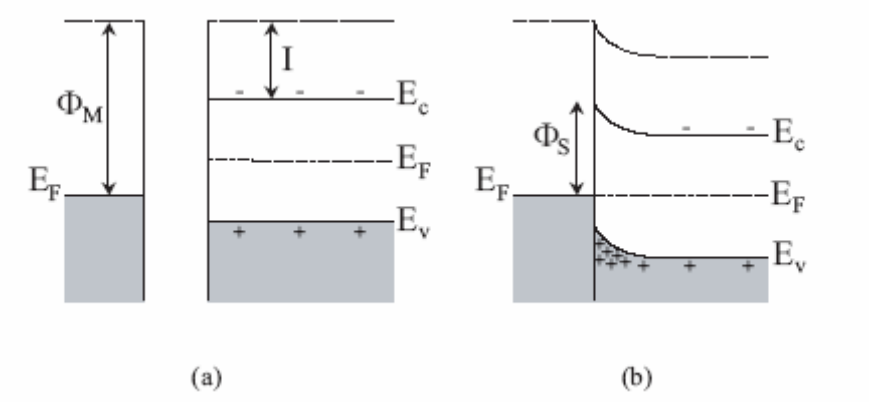

Fig.2.3. Energy-band diagrams under thermal equilibrium for (a) a metal (left) and an intrinsic semiconductor (right) that are not in contact; (b) a metal/semiconductor contact, with a band bending region in the semiconductor, close to the interface with the metal. E_c and E_v indicate respectively the edge of the conduction band and the edge of the valence band; E_F indicates the position of the Fermi level.

Due to the band bending, a non-ohmic Schottky barrier can be formed at the interface between metal and semiconductor. As a consequence, charge transport can be limited by injection through the Schottky barrier and is characterized by thermal excitation of charge carriers over the barrier, resulting in a temperature dependence. Mott-Schottky model is generally used as a guideline for choosing the contact metal to not limit the performances of a device because of non-ohmic contacts.

The height of the injection barrier will be given by the difference between the metal Fermi level and the HOMO or LUMO level of the organic semiconductor, for holes and electrons respectively. According to this, gold is generally used for the realization of p-type organic transistors, because its relatively high work function (5.1 eV) forms a low hole injection barrier with the most common organic semiconductors. On the other hand, low work function metals (for example, calcium shows 2.9 eV) are generally used as electron injectors.

There are several aspects that can modify the Mott-Schottky-type of band bending. One of these is the formation of surface dipoles at the interface between the metal and the organic semiconductor. The large interface dipole was explained by the change of the surface dipole of the metal upon adsorption of the molecule. A metal surface is characterized by an electron density tailing from the free surface into vacuum. Adsorbed molecules tend to push back these electrons, thus reducing the surface dipole and decreasing the work function of the metal, that can induce a vacuum level shift which can change the barrier height [65,66] as explained by Kahn et al. [67] (Fig.2.4).

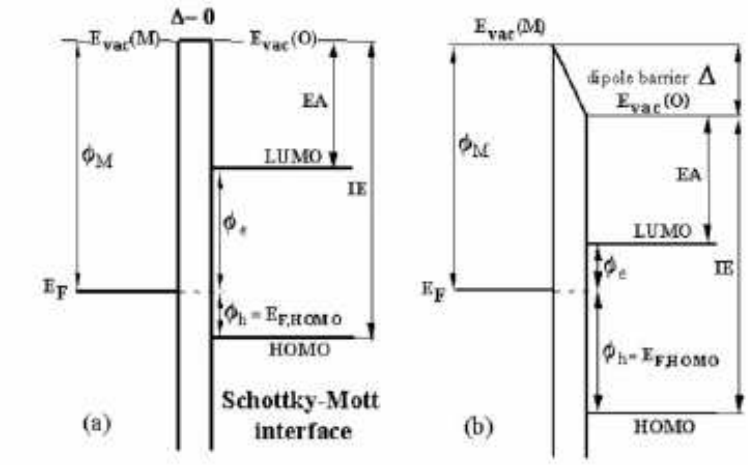

Fig.2.4. Energy bands of a metal-organic semiconductor interface (a) without and (b) with a dipole barrier (Δ).

Φ_e and Φ_h are the electron and hole barriers, respectively, and E_{vac}(O) and E_{vac}(M) are the organic and metal vacuum levels, respectively [67].

Another aspect that can have a strong influence in charge injection is the presence of traps at the metal/organic interface, which are mostly produced during contact fabrication [68]. The deposition of the metal contact over the already deposited organic film can cause local

damages in the crystalline structure of the material, due to the diffusion of the deposited specie into the active layer. On the other hand, the deposition of the organic material on top of pre-patterned metal electrodes can lead to an accumulation of structural defects at the triple interface between the metal contact, substrate and organic semiconductor. In fact, in this case, the organic material is not grown on a bare flat surface and the presence of pre-patterned structures (as the electrodes) can induce discontinuities in the morphology of the deposited organic film that act as trapping sites for charge carriers injected into the semiconductor.

2.2 Basic Concept of OTFTs

Field-effect transistor (FET) is an electronic device that relies on the electric field to control a current through the "conductive channel" made of a semiconducting material. When the active layer is fabricated from OSs, the device is referred to as an organic field-effect transistor (OFET). The most common configuration of an OFET is the organic thin film transistor (OTFT). OTFTs are usually applied for two goals: first, investigation of the OS properties (e.g. field-effect mobility, light-induced modifications, degradation effects after prolonged operation, etc.); second, OTFTs can be used as switching or sensing devices in organic electronic applications.

2.2.1 OTFT device geometries

The most commonly used geometries in OTFTs are the top-contact, bottom- gate (TB) (Fig.2.5 (a)) and the bottom-contact, bottom-gate (BB) (Fig.2.5(b)) geometries [8]. In TB transistor geometry, an OS layer is deposited prior to fabrication of source-drain contacts, that are usually fabricated by evaporation of the desired material (usually metal) through a shadow mask (shadow-mask technique) [9]. In BB transistor geometry, an insulator separates the gate contact from an OS layer and the source-drain electrical contacts, which are fabricated prior to the deposition of the OS layer (issue of a contact fabrication will be discussed in the chapter 6).

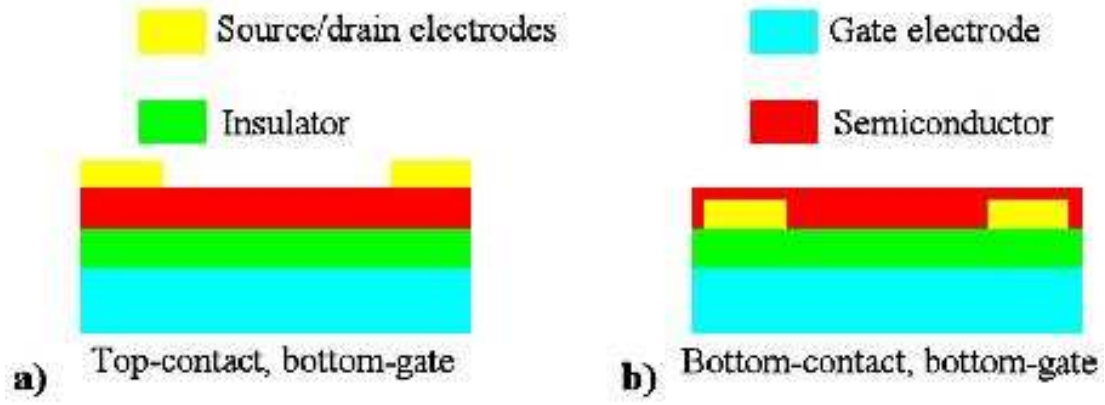

Fig.2.5. Schematic representations of (a) top-contact, bottom-gate OTFT geometry (TB), (b) and bottom-contact, bottom-gate OTFT geometry (BB). Different colours show different components of OTFTs.

The main advantages of the BB transistor geometry are the possible smaller separation between source and drain contacts (so-called channel length) and the fabrication of the source-drain contacts prior to the OS deposition. Therefore, despite of the inferior electrical characteristic compared to the TB transistor geometry [10,11], BB transistor geometry is frequently used in experimental works. Since the source-drain electrical contacts are fabricated prior to deposition of OS, the electrical characterisation can take place during the deposition of OS, and so the evolution of charge transport during the growth of OS layers can be observed [12,13].

2.2.2 Operation principle of OTFTs

OTFTs are primarily operated in the accumulation mode [14]. In the following discussion, the operation of a p-type OTFT is implied.

Voltage is applied to the gate (V_g) and to the drain electrodes (V_d), while the source electrode is grounded (V_s = 0 V). The potential difference between the gate and the source electrodes is referred to as the gate voltage (V_g), and the potential difference between the drain and source electrodes is referred to as source-drain voltage (V_{sd}) (Fig.2.6(a)). The source is the electrode that injects the charges into the body (or channel) of the transistor and is more positive than the gate electrode. However, in some cases, due to unintentional doping, surface treatment, etc., the accumulation of positive charge at the insulator/semiconductor can be observed even for positive gate voltages.

In Fig.2.6(b-d), basics operating regimes of OTFTs are presented [15,16]. The result of negative V_g is the accumulation of holes (positive charges) at the insulator/semiconductor interface. The charge density is proportional to the magnitude of the V_g and to the capacitance of the insulator (C_i). Not all of the accumulated charge is mobile and, therefore, does not contribute to the current through the transistor: some of the charge is trapped due to the presence of electrically active structural defects and chemical impurities. These traps must be filled before the current through the transistor can flow. In other words, a Vg value more negative than a certain offset voltage, called threshold voltage (V_{th}), must be applied to the gate electrode to fill the traps and observe a current in the OTFT. The presence of the traps reduces the applied V_g to the effective gate voltage (V_g - V_{th}).

Fig.2.6(b) shows the situation, when V_d = 0 V bias is applied to the drain contact and the negative Vg voltage is applied to the gate contact ($V_s = V_d = 0$ V; $V_g < 0$ V). In this case, the (positive) charge carrier concentration in the transistor is uniform across the transistor channel. When a small negative V_d bias is applied to the drain contact, a linear gradient of charge is formed along the channel ($V_d < 0$ V; $V_d > (V_g - V_{th})$) (Fig.2.6(b)), resulting in a current flow through the transistor, which value is proportional to the source-drain voltage (V_{sd}).

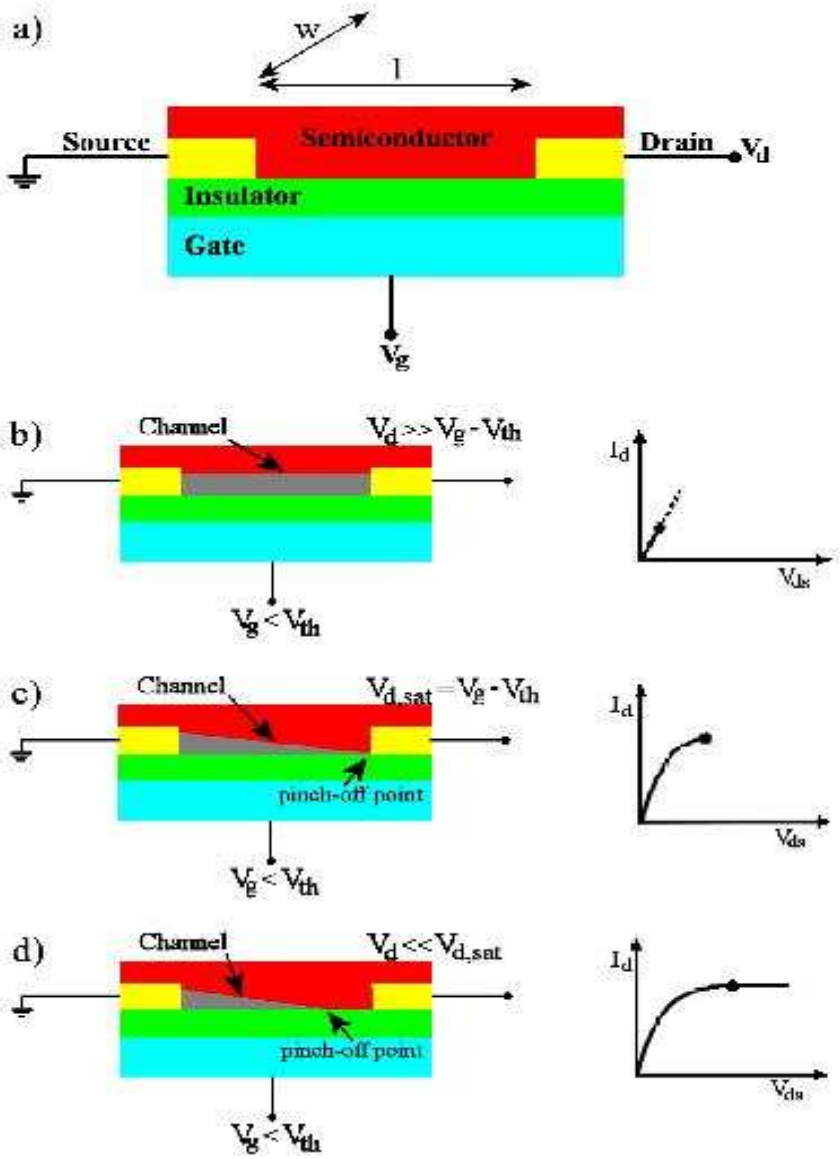

Fig.2.6. Schematic representation of an OTFT operating in different regimes: (a) shows the voltages applied to a transistor: source voltage (Vs), drain voltage (Vd) and gate voltage (Vg); channel length (l) is the distance between the source and drain contacts; channel width (W) is the length of source and drain contacts; (b) shows the situation, when Vd = 0 V and negative Vg is applied to the gate contact; (c) shows the end of the "linear regime" of OTFT operation; (d) shows the "saturation regime" of OTFT operation.

The mode of transistor operation under these conditions is referred to as the "linear regime" of transistor operation. This regime persists approximately up to the point $V_d >> (V_g - V_{th})$ at which the depletion region next to the drain contact starts forming (pinch-off point) (Fig.2.6(c)). The depletion region forms because the electrical potential inside the transistor channel near the drain contact is above the threshold voltage, therefore only the space-charge limited current can flow across the saturation region. Further decrease of V_d does not increase the current through the transistor, but only expands the depletion region

towards the source contact (Fig.2.6(d)). The mode of transistor operation under $V_d < (V_g - V_{th})$ condition is referred to as "saturation regime".

2.2.3 Analytical model of OTFTs

The description of the dependence of the drain current on gate voltage both in the linear and in the saturation regime begins with the derivation of two equations . These equations can be used to extract the "trap-free" mobility μ_0 and a threshold voltage V_t from the measured transfer characteristics. V is the electrical potential in the semiconductor and $V(x = 0) = V_0$ is the electrical potential at the insulator-semiconductor interface. Since the dielectric strength D at the insulator-semiconductor interface must be continuous, it results:

$$D_x = \varepsilon_0 \varepsilon_i F_x(x=0) = \varepsilon_0 \varepsilon_i \frac{V_g - V_0}{l} = C_i(V_g - V_0) = -\varepsilon_0 \varepsilon_s \left(\frac{dV}{dx}\right)_{x=0} \quad (2.1)$$

where F is the electric field and $C_i = \varepsilon_0 \varepsilon_i / l$ is the capacitance of the gate dielectric per unit area (ε_i is the dielectric constant of the gate insulator, ε_s is the dielectric constant of the semiconductor). On the other hand, Gauss's law yields:

$$\left(\frac{dV}{dx}\right)_{x=0} - \left(\frac{dV}{dx}\right)_{x=d} = \left(\frac{dV}{dx}\right)_{x=0} = \frac{1}{\varepsilon_0 \varepsilon_s} Q_{total} \quad (2.2)$$

as long as the electric field on the backside of the semiconductor (x = d) vanishes and the channel length L is much longer than the thickness of the gate insulator l (L >> l). Q_{total} is the total charge per unit area (trapped and free). Combining Eq. 2.1 and Eq. 2.2, it is possible finds that:

$Q_{total} = -Ci(Vg-V0)$ (2.3)

Note that $V_0 = V_0(y)$ in Eq. 2.3 depends on the distance from the source if a drain voltage is applied. The threshold voltage V_t is defined as the gate voltage above which essentially all of the incrementally added gate-induced charge is free. The threshold voltage depends on the density of charge carrier traps in the device and on the value of the flatband voltage V_{FB}. The flatband voltage is the gate voltage which needs to be applied in order to enforce flat bands at the insulator-semiconductor interface. A non-zero flatband voltage can result

from a difference of the Fermi levels in the semiconductor and in the gate. It should not be underestimated that, the flatband voltage is influenced by charge that is permanently trapped at the interface or within the gate dielectric. Replacing the gate voltage Vg in Eq. 2.3 by the effective gate voltage V_g-V_t an expression for the free charge per gate unit area is obtained:

$Q_{free} = -C_i(V_g-V_t -V_0)$ (2.4)

Eq. 2.4 will be inserted into an equation that is derived in the following. The drain current Id is given by:

$$I_d = \int j_d(x,y)dxdz = W\int_0^d j_d(x,y)dx = \\ = W\int_0^d \mu_0 e p_{free}(x,y)F_y(y)dx, \tag{2.5}$$

where μ_0 and p_{free} are the mobility and density of free holes. Fy is the component of the electric field in the direction of the current flow. It is possible write:

$$I_D = -W\frac{dV_0(y)}{dy}\mu_0 \underbrace{\int_0^d e p_{free}(x,y)dx}_{Q_{free}(y)} = \\ = -W\frac{dV_0(y)}{dy}\mu_0 Q_{free}(y). \tag{2.6}$$

Combining Eq. 2.6 with Eq. 2.4, we have the differential equation:

$$\frac{dV_0}{dy} = \frac{I_d}{W\mu_0}\left[\frac{1}{C_i(V_g - V_t - V_0)}\right]. \tag{2.7}$$

Variable separation (variables V0 and y) and integration gives:

$$\int_0^{V_d} C_i(V_g - V_t - V_0)dV_0 = \frac{I_d}{W\mu_0}\int_0^L dy \tag{2.8}$$

and eventually results in:

$$I_d = \frac{W}{L}\mu_0 C_i\left(V_g - V_t - \frac{V_d}{2}\right)V_d \tag{2.9}$$

as long as $|Vd| \leq |Vg - Vt|$. The term which is quadratic in V_d is often neglected and so, in the linear regime, resuts:

$$I_d = \frac{W}{L}\mu_0 C_i (V_g - V_t) V_d \qquad |V_d| \ll |V_g - V_t|. \tag{2.10}$$

In the linear regime, Eq. 2.10 predicts a linear dependence of the drain current on the effective gate voltage Id α (V_g - V_t). This behaviour was already mentioned above and is represented in Fig.2.6(b). A linear regression of the measured transfer characteristic would yield the trap-free mobility μ_0 and the threshold voltage V_t.

At V_g - V_t = V_d, the depletion zone at the drain electrode is about to form and the drain current saturates. By introducing V_g - V_t = V_d in Eq. 2.9, it results:

$$I_d = \frac{W}{L}\frac{\mu_0 C_i}{2}(V_g - V_t)^2 \qquad |V_d| \geq |V_g - V_t|. \tag{2.11}$$

Eq. 2.9 was derived by assuming $|V_d| \leq |V_g - V_t|$. Due to the saturation of the drain current, Eq. 2.11 is valid not only for $|V_d| = |V_g - V_t|$, but also for $|V_d| > |V_g - V_t|$. According to Eq. 2.11, the drain current in the saturation regime quadratically depends on gate voltage, i.e. Id α $(V_g - V_t)^2$.

From these equations, a field effect transistor operates as a voltage-controlled current source. Mobile charge carriers are induced in the semiconductor close to the interface with the dielectric, under a gate-source voltage applied across the gate dielectric. The current flows through the semiconductor when a drain-source voltage is also applied. In other word, the on/off states of channel current can be controlled by the gate-source voltage. These on and off states form the logic states of "1" and "0", respectively.

2.2.4 Parameters of OTFTs

The performances of OTFTs can be characterized by several key parameters including, on/off current ratio, field-effect mobility, subthreshold slope threshold voltage and so on. Reliable and reproducible extractions of the parameters from the transfer curve or the output curve of a transistor are prerequisites for a comparison between the performances of devices [5]. Here, the basic requirements for proper parameter extraction are defined. The main parameters of OTFTs are as follows.

Field-effect mobility (μ). This is the most important parameter for OTFTs, because the switching speed, on/off ratio, and other key parameters are correlated to the field-effect mobility. The real application of an OTFT is strongly dependent on the realization of high mobility in channel. So, materials with high carrier mobility are always a goal for many researchers in designing new organic semiconductors.

The linear field-effect mobility (μ_{lin}) of each transistor is calculated by plotting the drain current versus the gate voltage in the linear regime and fitting the linear transfer curve by the equation (2.10). On the other hand, the saturation field-effect mobility (μ_{sat}) of each transistor is calculated by plotting the square root of the drain current versus the gate voltage and fitting the curve by the equation (2.11).

The carriers mobility depends on the transversal electric field (gate-source), because of physical phenomena mostly related to the charge transport nature in the semiconductor and usually follows the relationship:

$$\mu = \mu_0 (V_{GS} - V_{TH})^{\alpha} \tag{2.12}$$

that is in accordance with both Multiple Trapping and Release and Variable Range Hopping transport models presented above.

On/off current ratio. It is also called on/off ratio. On/off ratio is the secondarily important parameter for OTFTs. This parameter indicates the ability of a device to shut down, that is to block the current flow, and it is particularly relevant in applications such as active matrix displays and logic circuits. On/off ratio of a-Si:H TFTs is about 10^6. Anyway, those of low voltage OTFTs can reach 10^7 [17], which can satisfy the requirement of many applications. The on/off ratio is extracted from a plot of I_{DS} on a logarithmic scale as a function of V_G. The on/off ratio is taken as the ratio of the maximum current divided by the minimum current.

Threshold voltage. The threshold voltage (V_T) is defined as the minimum gate voltage that can induce current flow between the source and drain electrodes. The theoretical dependence of V_T on parameters of the thin film transistor is quite complex. Here, a simple relation is given by equation 2.13 [18]:

$$V_T = \left| \frac{Q_s}{C_i} \right| \tag{2.13}$$

where Q_s is the effective total charge per unit area at the insulator/semiconductor at the zero gate voltage. The charge consists of different main contributions: mobile and fixed charges in the insulating layer and the semiconductor/dielectric interface charge. As a rule, V_T reaches higher value with the increase of the trap-state density at the interface of the semiconductor and dielectric. In many applications, stability and uniformity of V_T for large numbers of transistors are much more significant than the magnitude of V_T. Unstable V_T will result in turn-off failure of OTFTs. So, the variation of V_T of the OTFTs should be controlled in a small range. V_T can be extracted by fitting the linear or saturation curves according to the equation 2.10 and 2.11.

Subthreshold slope. Below the threshold voltage, there is a subthreshold region in which the drain current depends exponentially on the gate-source voltage. In the subthreshold region, the drain current is induced by the carriers that have sufficient thermal energy to overcome gate-voltage-controlled energy barrier. The subthreshold slope S, also called subthreshold swing, can be described quantitatively by equation 2.14 [8]:

$$S = \frac{\partial V_{GS}}{\partial(\log_{10} I_{DS})} \tag{2.14}$$

Conceptually, subthreshold voltage slope can be used to estimated the density of the trapped charge carriers at the interface by equation 2.15 [19]:

$$N_{trap}^{\max} \approx \left[\frac{qS\log(e)}{k_B T} - 1 \right] \frac{C_i}{q} \tag{2.15}$$

where q is electronic charge, $N_{trap}^{\max}$ is the upper limit of the trapped charges, and k_B is Boltzman's constant. Obviously lower trapped charge density will result in lower subthreshold slope.

The operating voltage. As known, the minimum working voltage that is applied at the device when an OTFT can realize the functions in circuits. The key challenge of OTFT's application is related to the unacceptably large power when the conventional gate

insulators are utilized [20]. High operating voltage not only results in high energy consumption but also is incompatible with portable applications that require the devices operated at a few volts [21].

Device stability. It is fondamental requirement for practical applications of OTFTs. V_T stability is a important figure of merit as well as the field-effect mobility because it is related to the operational and lifetime [5]. The stability of OTFTs mainly is about two main aspects [22]. One is the air stability, that is a well-known problem for organic semiconductor materials. The other limit is a characteristic of threshold voltage shift (ΔV_T) after gate-bias stress that results from the operation of *the* OTFTs..

IThe electronic trap states in the semiconductor or at the interface between the semiconductor and the dielectric or in the dielectric layer can cause instabilities of the threshold voltage of OTFTs [23].

2.2.5 Threshold voltage in OTFTs

From the concept of threshold voltage in the previous paragraph and this concept appears in the OTFT equations, a digression on this topic is needed.

In fact, this concept is rather different from the one in the MOSFET devices. In such devices, when the gate is biased to positive (negative) for an n-type (p-type) channel, an inversion layer is induced at the insulator/semiconductor interface, so as to form a conducting channel between source and drain. This leads to two consequences: first, the source and drain regions, along with the conducting channel between them, are isolated from the substrate by a depletion layer. Second, the conducting channel only forms after the gate voltage is beyond the so-called *threshold voltage*, that is, the onset voltage for the inversion regime. In first approximation, the threshold voltage can be defined as the gate bias where the Fermi level at the insulator/semiconductor interface crosses the middle of the gap [24]. The inversion regime is very specific to crystalline silicon. On the contrary, OTFTs operate in the accumulation regime, where the gate voltage is polarized positively (negatively) versus the n-type (p-type) substrate. The source and drain consist of simple ohmic contacts on a thin semiconductor film. In such a geometry, there is no depletion layer to isolate the conducting channel from the substrate, and a very low conductivity is

therefore required. Another consequence of the absence of a depletion layer is that, in principle, when no traps are present the threshold voltage should be zero, because, in the absence of localized states, originating from donors, acceptors or defects, all induced charge is necessarily mobile. Later, we will show how traps can cause a non-zero threshold voltage. Here, we continue by analyzing the sub-threshold current of trap-free devices. In MOSFETs, the sub-threshold current is exponentially depending on the gate-bias as well as the drain–source bias [25].

2.3 Specific Materials

The most common organic materials employed for electronics applications can be classified into two families: i) aromatic compounds; ii) heterocyclic compounds.

The aromatic compounds family is characterized by the benzene ring, reported in Fig.2.7(a). The benzene ring (C_6H_6) consists of six carbon atoms bonded in a flat or planar hexagon ring. Each carbon atom in the hexagonal cycle has four electrons to share. One goes to the hydrogen atom, and the others to the two neighboring carbons, with an alternation of a single and a double bond. Aromatic compounds are basically formed by a concatenation of several benzene rings, that lead to obtain a rodlike conjugated molecule.

The heterocyclic compounds is characterized by the thiophene ring. Thiophene (C_4H_4S) is a heterocyclic compound consisting of four carbon atoms and one sulfur atom in a five-membered ring (Fig.2.7(b)). Also in this case, carbon atoms are bonded to a hydrogen atom with a single bond and to the neighbour atoms of the ring by one single and one double bond.

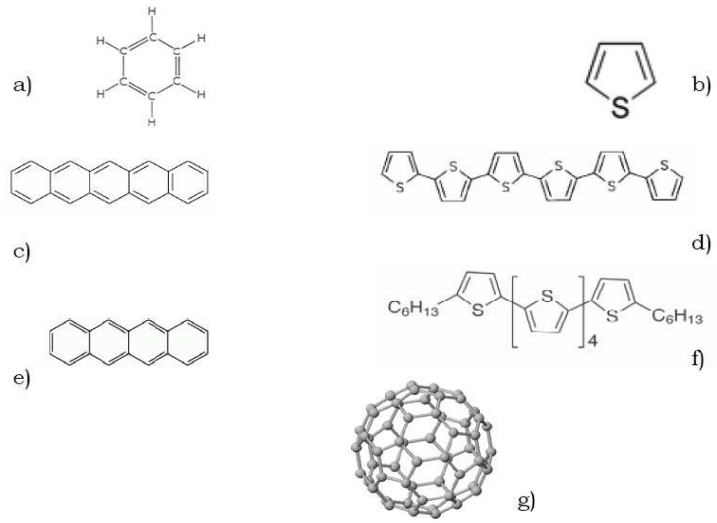

Fig.2.7. Chemical structure of (a) benzene ring, (b) thiophene ring, (c) pentacene, (d) a-sexithiophene(e) tetracene, (f) a,ω-dihexylsexuthiophene and (g) fullerene C60.

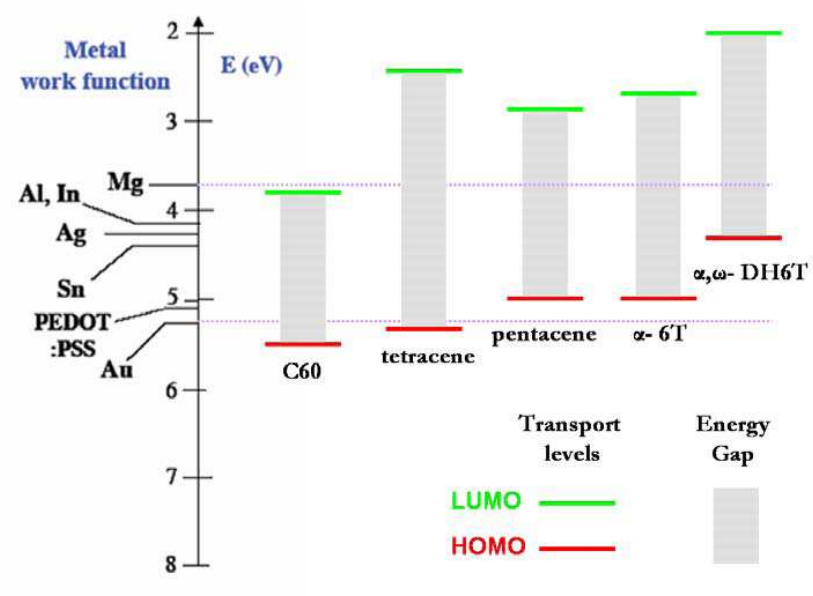

Fig.2.8. Band structure showing LUMO and HOMO energy levels of some organic semiconductors.

2.4 The Progress Of OTFT

The high-performance organic semiconductors can be classified into two types: conjugated polymers and small molecules. The choice of the material to be used in an OTFT depends on the desired type of conduction (p or n) [26]. In Fig.2.9, we can see that the mobility of organic semiconductors have reached values close to, and sometimes greater than, 1

cm^2/Vs in both types of carriers in transistors based on both small molecules and polymers.

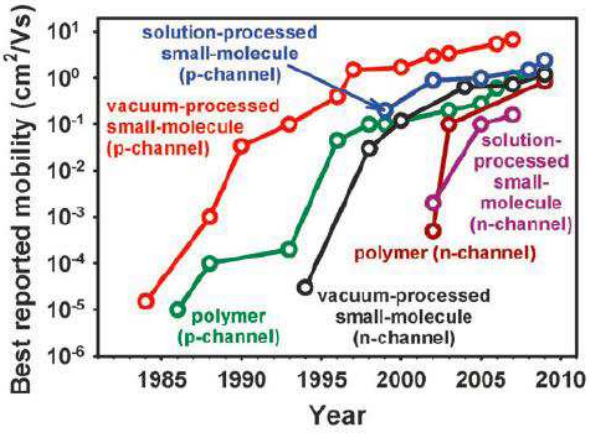

Fig.2.9. Development of the field effect mobility (measured in the ambient air) of p-channel and n-channel transistors based on small-molecule or polymeric semiconductors [8].

Due to the relatively low mobility in the organic semiconductor, the organic field effect transistors can not compete with the performances of the field effect transistors based on inorganic single crystal semiconductor, such as silicon and germanium, that have a mobility μ about three orders of magnitude higher. Consequently, the OTFT are not suitable for use in applications that require high-speed switching, because it is strictly linked to the mobility of the carriers. However, the characteristics and the performances of the OFET found so far suggest that a new market is opening for the organic devices.

The majority of small molecule semiconductors have a field effect mobility higher than that usually found in the polymeric semiconductors, thanks to their higher crystallinity degree. These small molecules are mainly deposited by thermal evaporation in vacuum systems.

A brief history of the progresses of the OTFTs is presented below.

The use of an organic material as the semiconductor in TFT was reported by Ebisawa et al. [27] in 1983, but already in 1980 the research on TFT based on organic semiconductors had focused mainly on small organic molecules, such as A-sexithienyl sexithiophene, tetracene, pentacene, etc.. The use of the pentacene as the active material in the OTFTs has been studied for the first time by Horowitz et al [28] in 1992, obtaining mobility of 2×10^{-3} cm^2/Vs. Brown et al. [29] reported that the field effect mobility for a pentacene TFT can be increased through the use of a precursor of pentacene deposited by spin coating and

subsequently heated to 140°C. They were able to obtain mobility in the order of 10^{-3} cm^2/Vs.

In 1996, Dimitrakopoulos et al [30] realized TFT through deposition of pentacene by molecular beam deposition technique, reaching a mobility even higher than those previously observed of 0.038 cm^2/Vs. In 1997, Sirringhaus et al. [31] realized OTFT based on Bis(dithienothiophene), reaching a ratio Ion / Ioff of 10^8 and a value of mobility of 0.02-0.05 cm^2/Vs in their devices.

In 2000, Hagen Klauk et al. [32] got field effect mobility 0.6 cm^2/Vs and ratio Ion / Ioff greater than 10^5 in pentacene OTFT, using contacts deposited through ion beam technique.

In 2002, Carmen Bartic et al. [33] reported OTFT based on poly(3-hexylthiophene) with Ta_2O_5 as gate dielectric (k = 21) operating at voltages lower than 3 V.

In 2003, Lee et al. [34] presented pentacene OTFT with mobility 0.14 $cm^2/V\ s$ with Al_2O_3 as gate dielectric, and in 2004 Puigdollers et al. [35] realized OTFT with field effect mobility of 0.01 cm^2/Vs. The first behavior of ambipolar pentacene TFT was observed by Wang Wei et al. [36] in 2005: the field effect mobility of the holes was about 0.17 cm^2/Vs, while the reported field-effect mobility of electrons was about 0.02 cm^2/Vs.

In recent years, many materials, processes and configurations have been tested, with the aim to improve the performances of the OTFTs. Among them, the most successful OTFTs are those made with semiconductor pentacene or rubrene.

The choice of the gate dielectric is crucial in the implementation of the OTFT. In fact, the size of the grains of the semiconductor film is strongly influenced by the surface roughness of the gate dielectric [37,38], which has direct effect on the field effect mobility. The gate dielectric most widely used in the pentacene OTFTs is the thermally grown silicon dioxide, but the operating voltages of these OTFTs are typically of the order of 20 V. For portable applications, in particular for radio frequency identification devices (RFID), it is necessary to reduce the operating voltage below 5 V in order to obtain a limited consumption of energy.

High values of the dielectric constants of insulators allow to reduce the operating voltage [39], but the surfaces of the materials with high dielectric constant are often rough, then the grains of the semiconductor film deposited on these materials are relatively small, with consequent lowering of the field effect mobility. Therefore, many laboratories have turned

their attention in the search for ways to reduce the operating voltage of the OTFT without reducing mobility through the use of specific insulating layers (HfLaO) [40].

Mc Dowell et al. [41] in 2006, increased the performance of the OFET using new self-assembled monolayers (SAM) as the dielectric. In 2008. M.F. Chang, G.F. Lee et al. [42] prepared OTFTs with pentacene films using HfLaO as dielectric and reporting operating voltage of less than 2 V, mobility of 0.71 cm^2/Vs and ratio I_{ON} / I_{OFF} of the order of 10^5.

Another crucial point that affects the performances of an OTFT is the choice of the electrical contacts. Pentacene is a p-type semiconductor and then gold (Au) is the most commonly used material for the electrodes. However, the use of expensive gold electrodes for devices based on pentacene not agrees with the idea of the low cost of production, which is one of the main advantages of the OTFTs. Therefore, researchers are currently looking for new materials to make the OTFTs really cheap. For example, Chih-Wei Chu et al. achieves high performances by inserting a layer of metal oxide (MoO_3) between the electrodes and the pentacene, and D.K. Hwang et al. [43] reported relatively low operating voltages (< 5 V) for pentacene OTFTs having NiO electrodes and mobility of 0.32 cm^2/Vs. Also electrodes made of the bilayers WO_3/Al or V_2O_5/Al can replace the expensive Au electrodes in OTFTs based on pentacene. In fact, the field-effect mobility with electrodes made of the double layer WO_3/Al is 0.253 cm^2/Vs and the On / Off ratio is equal to $4.1x10^4$. Similar values are found also in the devices with the double electrode layer V_2O_5/Al, with field effect mobility of 0.226 cm^2/Vs and On / Off ratio of $1.8x10^4$ [44].

Another small molecule that allows for outstanding performance in the OTFT is Rubrene, which currently holds the record for the highest value of field-effect mobility of organic semiconductors (15-40 cm^2/Vs) obtained in single-crystal transistors.

Exceptionally high values of mobility for pentacene (5.5 cm^2/Vs) was found in a study carried out by Sangyun Lee, Koo et Bonwon which synthesize intentionally dielectric polymer (PVP) with different percentages of concentration of hydroxyl groups, to study the effect of hydroxyl groups on the electrical properties of the organic transistors based on pentacene. The apparent hysteresis effects, which are usually observed in OTFT devices, confirmed to be strongly linked to the hydroxyl bonds existing within the polymeric dielectrics. These effects are therefore reduced by replacing them with cinnamoyl groups. Although the hydroxyl groups deteriorate the characteristics of

capacitance-voltage (CV) and result in an increase of the gate current, mobility becomes exceptionally high (5.5 cm^2/Vs). This high value of mobility can be achieved by increasing the number of hydroxyl groups, but it is not correlated with an improvement of the crystallinity degree of the pentacene, instead it depends on the characteristics of the interface between semiconductor and dielectric [45] (Fig.2.10).

Ratio of hydroxyl groups (cinnamoyl group) (%)	Dielectric constant	Mobility ($cm^2 V^{-1} s^{-1}$)	On/Off current ratio
100 (0)	4.04	5.5	$\sim 10^5$
50 (50)	3.47	0.06	$\sim 10^6$
35 (65)	3.44	0.045	$\sim 10^6$
20 (80)	3.34	0.03	$\sim 10^6$

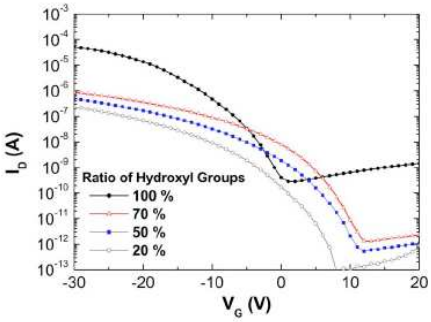

Fig.2.10. Trans characteristics and parameters related to OTFTs having dielectric with different percentages of concentration of the hydroxyl groups [45].

Due to their poor environmental stability and the lack of possibility to use techniques for deposition from solution, research directed to the synthesis of new materials that retain the properties and the performances of these ones, but with the aid of pendant groups in the molecules they become soluble in certain solvents. The search for these new materials has begun in 2003 by Sheraw et al., who has created five different functionalized pentacene derivatives to facilitate molecular interactions and thus increase the overlap between the π orbitals, resulting in a field-effect mobility of 0.4 cm^2/Vs and On / Off ratio of 10^6 in devices manufactured utilizing Triisopropylsilyl pentacene (TIPS pentacene) [46].

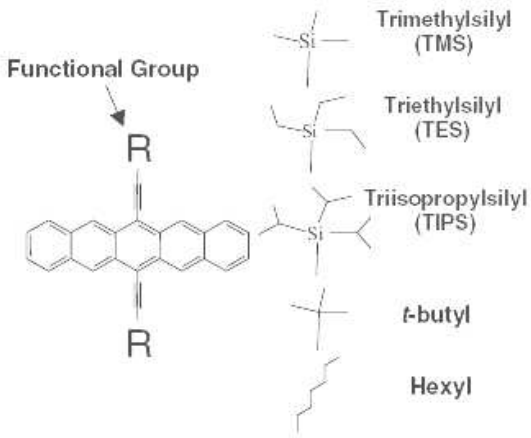

Fig.2.11. Molecular structure of the pentacene molecule functionalized with different pendant groups.

In 2004, Kuo-Chung Chen et al. reached 1 cm^2/Vs mobility using triethylsilylethynyl thienyl pentacene (TES thienyl pentacene) in OTFTs exhibiting an On / Off ratio of about 10^7 [47]. The following year, Park, Sung Kyu et al. [48] made OTFTs using (triisopropylsilylethynyl) pentacene (TIPS - pentacene), with mobility 1.5 cm^2/Vs, which was the highest mobility reported at the time for OTFTs made through processes from solution. The TIPS-pentacene thin films have a very limited thermal budget and also show remarkable molecular order. In this work it is shown that OTFTs fabricated through processes from solution show similar characteristics to devices deposited by evaporation in vacuum systems. Some other works have identified the close correlation between the properties of the solvent of the semiconductor, which is strongly linked to the crystallinity degree of the films of TIPS- pentacene, and the OTFTs performances using this molecule [49,50] (Fig.2.12).

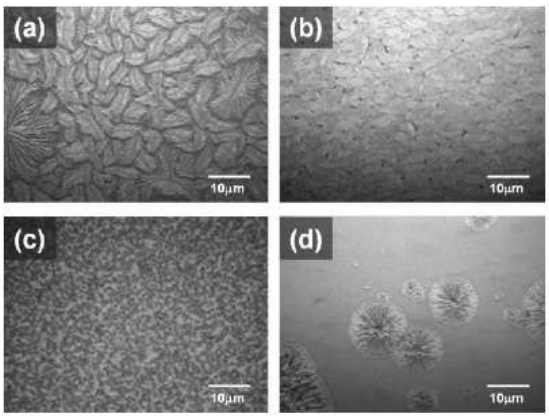

Fig.2.12. Optical images of TIPS-pentacene films deposited by spin coating on HMDS-treated PVP, using different solvents at the same 1% concentration: (a) chlorobenzene, (b) xylene, (c) chloroform, (d) toluene [49].

Many works, then, followed, in order to improve devices performances, by optimization of the deposition process and study of interface through surface treatments and annealing [51,52,53,54].

Although the performances of the OTFTs have increased dramatically over the past decade, it still remains difficult to realize large area arrays of transistors with good and consistent performances. Approaches based on the use of soluble organic semiconductors have become attractive both in terms of ease of deposition and in the possibility to patternate the semiconductors directly on substrates such as plastic. Despite the small

molecules still show advantages, in terms of the mobility of the charge carriers higher than that obtained with the use of the polymers, the realization of highly crystalline and uniform thin films on large area substrates is often much more difficult than in the case of polymers. This can be related to the intrinsic anisotropy of the charge transport in polycrystalline films of small molecules, in addition to the effects of the pronounced grain boundary [55,56].

An interesting approach to cope with these challenges is to combine the properties of high mobility of small molecules with the advantageous processability of the polymers, beinging to the manufacture of blend based OTFTs [57]. It was recently shown that the simple mixing of a small molecule and a polymeric matrix material allows to control the rate and the degree of crystallization of the small molecule during the formation of the film. This has been successfully demonstrated with mixtures of different organic p-type semiconductors, such as 6,13- bis (triisopropylsilylethynyl) pentacene (TIPS - pentacene) and 2,8 - difluoro - 5 ,11 -bis (triethylsilylethynyl) anthradithiophene (diF - TESADT) [58,59,60], in combination with different types of polymer binders. The OTFTs fabricated from such mixtures of semiconductors showed mobility of more than 5 cm^2/Vs [61]. In addition, a study done by Lada et al. in 2011 shows the solvent effects in the crystallization of the semiconductor. This study is based on devices with top-contact bottom-gate configuration, where the CYTOP is used as the gate dielectric and a blend of TIPS-pentacene (small molecule) and polystyrene (polymer) as the semiconductor. This semiconductor is dissolved in two solvents: the main solvent used (mesitylene) is a high boiling solvent and is particularly suitable for the solution of the small molecule, and the second solvent (anisole) exhibits a high solubility of the polymer and therefore is a good solvent for the polymer. This work shows that this approach can improve the crystallinity of the semiconductor, and therefore have a positive effect on mobility. It is shown that the solubility properties of the components can be used to identify the solvent that can allow the best arrangement of small molecules in the blended semiconductor [62].

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Chapter 3
Stability of Organic Thin Film Transistor

Organic electronics (also known as "printed electronics" or "plastic electronics") has begun to make inroads in research labs at the end of the eighties. Over the past few years, it has seen a huge development at the international level. Some applications are already present on the market (like the AMOLED displays in mobile phones), and others (e-paper , solar cells, RFID) are already at an advanced stage of experimentation.

The active element of the organic devices is no longer an inorganic semiconductor, such as the silicon or the gallium arsenide, but one from several organic semiconductors such as the conjugated polymers or the so-called small molecules. The organic optoelectronic devices and systems are commercially attractive because, thanks to the materials used to fabricate them, they possess a powerful combination of properties, including mechanical flexibility and easy processing on large areas, which can be done at a reduced cost, both from liquid solution (inks or pastes) or through simple evaporation processes. Moreover, typical methods of the printing industry can be used, such as screen printing or inkjet printing, to manufacture the organic optoelectronic components.

However, for a large market penetration of this new technology, it is necessary to impose, evaluate and improve the characteristics of the basic components: the performances of the OTFT are still far from the needs of the applications to which they are intended to be applied, as to efficiency and stability (it must be clearly said that organic transistors are not thought to compete with the traditional MOSFETs).

In this chapter, the current understanding of the reliability of organic field-effect transistors is reported, with a particular focus on the degradation of device characteristics under some sources of instability. The various factors that have been found to influence the operational stability of different material systems are discussed, including dependence on stress voltage, gate dielectric, environmental conditions, light exposure. An important question about devices instability concerns the role of the extrinsic factors, such as oxidation or presence of moisture, and that of the intrinsic

factors, such as the inherent structural and electronic disorder that is present in thin organic semiconductor films. The effects of the microscopic defects, that could play a role in charge trapping in organic semiconductors, are presented too.

3.1 Introduction

The increasing industrial interest which invests the OTFTs is motivated by the development of process technologies that make such devices feasible using low-cost processes (solution-processing technologies and vacuum deposition) giving high productivity volumes.

Moreover, the introduction of new materials and new superficial treatments can provide improved features, both in the charge transport and in the switching speed. Therefore, it has led to believe that the use of OTFTs could be increasingly pervasive to interface conventional integrated circuits, supplied by inorganic electronics, to organic electro-optical devices, with the possibility to integrate them on flexible substrates and on large areas.

However, the achievement of the objective to fabricate complex logic circuits using the OTFTs, to get real working applications, must overcome one of the biggest problems of the Organic Electronics (OE): the stability of the devices, i.e. obtaining long-term performances. It is known [1] that chemical and physical interactions between the organic materials of these devices and the surrounding environment greatly reduces the benefits that OE can provide in time.

In the general context of the OE, the stress can be defined as the cause of an unwanted variation (drift) of the electrical performances of an electronic device, when it is subjected to the typical uses of the application where it is inserted. It is indeed important to note that the electrical operation itself of an OTFT, as well as the system the transistor is integrated in or it interacts with [2] are clearly all causes of drifts in his behavior, both dynamic and static (drift of static behavior is said Bias Stress Effect - BSE). The stability analysis of the static behavior of an OTFT includes both electrical bias (bias) of the gate and drain in the saturation regime and in the sub - threshold regime.

An example of the static analysis for a simple circuit to pilot an OLED allows us to guess the impact that the performance drift of the driving transistor can have on the overall performances of the system (in this case a display). In Figure 3.1 it is shown the static working point of an OTFT that supplies current, through the drain, to an OLED. If the OLED current in its working point is 60 nA, the OTFT is working in the saturation zone with gate voltage V_G = -16 V. If, due to the applied bias over time, the threshold voltage of 2 V of the OTFT grows, the OLED would be powered by a current of about 37 nA, bringing the system to work out of the specification. It is obvious that during the life of the display, such a characteristic can change, so it is necessary to know in advance these drifts for both the driving elements and for the OLED.

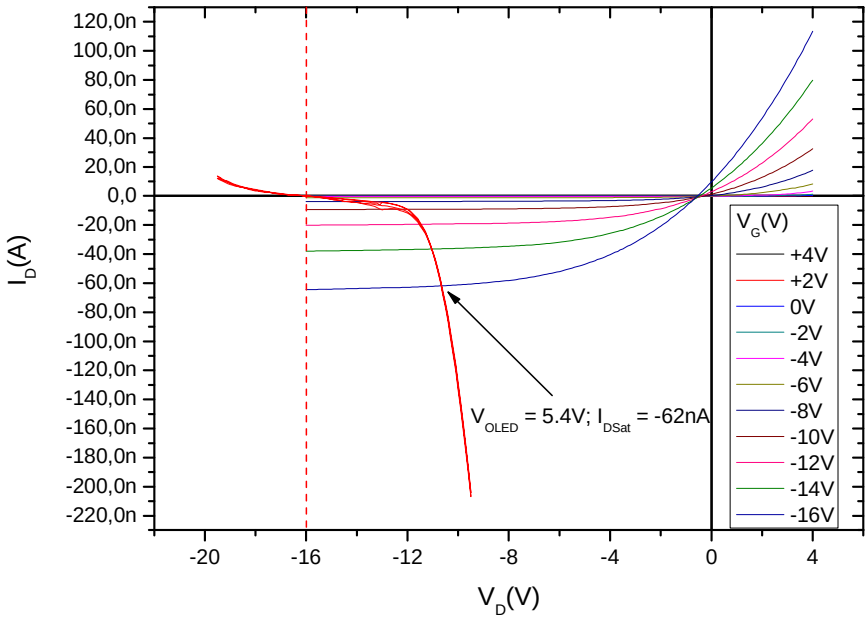


Fig.3.1. The working point of a pentacene OTFT with PMMA as dielectric (thickness 225 nm) and with W / L = 2.85, used to drive an OLED (ITO/NPD/ALQ3/LiF/Al) with an active area of 0.01 mm² in an organic display.

From the quantification of the effects of BSE, it is therefore essential to understand what are the causes of stress and what repercussions they have in the context where the OTFT operates, in order to predict, and as far as possible, minimize the degradation in time of the active element and the decrease of the saturation current of the OTFT.

3.2 *Identification of parameters affected by stress*

The most common parameters associated to the functional specifications of an OTFT are, from the static point of view, related to the drain current, when this output acts as the driving stage of other devices (here, the symbols refer to the ideal model of the transistor, in the first approximation used in the literature in the study of OFET [3]):

- **Threshold voltage**: V_T [V]
- **Field effect Mobility**: μ_{FET} [$cm^2/V\ s$]
- **On / off ratio**: I_{on} / I_{off}

To quantify the effects of BSE, the shift of the threshold voltage and the variation of the charge carriers mobility are estimated. It is known from the literature that both the exposure to environmental contaminants (such as oxygen and moisture) and the electrical stress due to the gate bias are able to shift the threshold voltage of an OTFT, and also process parameters (e.g. surface treatments) acting on the interfaces are able to influence the stability of a device [1].

The threshold voltage, intimately linked to the charge trapping at the channel / dielectric interface [4], is often used in the literature as an estimation of the degree of stability / instability of an OTFT [4,5]. In some cases, the drifts of the gate voltage are reversible [6,7], introducing a form of instability with hysteresis in the operation of the logic circuits made of OTFTs.

Much effort in recent years has been devoted to develop new materials that combine high field-effect mobility with good environmental stability. While some of the original high-mobility organic semiconductors, such as pentacene and poly-3-hexylthiophene (P3HT), suffer from chemical instabilities when exposed to atmospheric species and light, some of the recently developed materials exhibit much improved environmental stability and device shelf life.

3.3 *Non ideality of OTFT*

A study of the physical parameters that govern the behavior under stress of an OTFT, must take into account that, due to the hopping of the carriers in the channel [9], there exists a dependence of the electron field effect mobility μ_{FET} from the Gate voltage. In order to obtain the characteristic parameters of an OTFT, generally using the model of monocrystalline MOS (in triode region for a transistor of type "p", approximated by Eq. 3.1), there are, however, more sophisticated models that take into account the non-ideality of the amorphous semiconductor film [11] In fact, if you remove the mobility of the ideal model (equation 3.1):

$$I_{DS} = \mu_{pFET} \frac{W}{L}\left[C_{ins}\left((V_G - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right)\right] \quad (3.1)$$

a relationship is obtained that ideally should not depend on the gate field (eq. 3.2):

$$\mu_{pFET}(V_{GS}) = \frac{2L}{WC_{ins}}\left(\frac{\partial\sqrt{I_{DSsat}}}{\partial V_{GS}}\right)^2 \quad (3.2)$$

However, in practice, there is an effect of entrapment of charges in the channel region of an OTFT which manifests itself at low vertical fields. If, in fact, the procedure for the extraction of μ_{FET} given by Eq. 3.2 is applied to the trans-characteristic of one of the transistors used in the experimental part, we obtain that, for V_{GS} small enough to consider the device in saturation, mobility depends on the gate voltage through a power law (Fig.3.2).

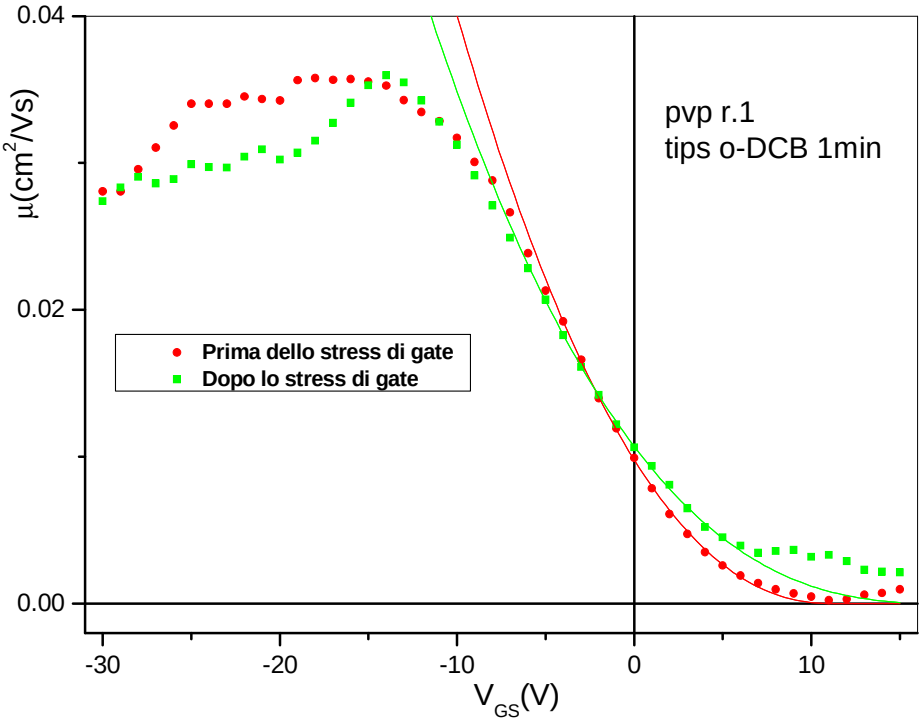


Fig.3.2. Comparison between (red) the mobility of a not stressed OTFT with (green) that of a device stressed solely by the gate bias (V_G =-30 V). Continuous lines show the simulations using the mobility model cited by Estrada, et al. [8].

The model used for the fits in Figure 3.2 (solid lines) is the one used in the literature [5,8] and summarized by the equation:

$$\mu_{FET} = \mu_0(T) \cdot (V_{GS} - V_T)^{\gamma} \qquad (3.3)$$

where μ_0 is the so called intrinsic mobility and depends on the material, V_T is the threshold voltage and γ is an exponent dependent on the temperature and on the trap states that are triggered through the field effect.

Many analyses allow to evaluate more effectively the characteristic parameters of the OTFTs by decoupling the intrinsic transport phenomena from those ones induced by traps [8].

3.4 *Trap state in organic semiconductors*

Models developed for the crystalline inorganic devices are not always valid for systems of organic semiconductors, and in particular it is to be noted the absence of a uniquely definable mobility and a distinguished threshold voltage. This can arise from a gradual profile of the density of the states (DOS) at the HOMO and the LUMO of the materials, so the carriers are relatively localized and jump from molecule to molecule. When the Fermi level of the semiconductor moves towards one of the bands, under the application of a voltage, it causes the accumulation of the charges near that band edge, so more and more states are filled and the new injected carriers can be mobile.

In a disordered organic semiconductor, where the concept of well-defined conduction and valence-band edges is not applicable, there is a certain arbitrariness about what constitutes a trap state. As a result of the energetic disorder, the DOS of both the HOMO and LUMO levels in the bulk is generally represented as a Gaussian with a standard deviation σ. For this broadened density of states, a transport energy can be defined, which denotes statistically the energy to which a carrier in a deep state in the DOS is most probably excited in order to move to a neighbouring site. A state below this transport energy is called a trap state, while states above it are effectively transport states. Trap states might be due to either the inherent site-to-site fluctuations in molecular conformation and intermolecular packing that gives rise to the Gaussian DOS, or they might arise from specific extrinsic chemical impurities, fixed charges, or structural defects left over from the synthesis or incorporated into the film during its processing, operation, or storage [54].

Localized levels acting as traps are called acceptor states if located close to the LUMO and donor states if located close to the HOMO. Acceptor levels close to the HOMO and donors close to the LUMO act as dopants. An acceptor-like trap is in a neutral state when the Fermi level is below a characteristic energy E(0/-) and becomes negatively charged when the Fermi level is above this energy. In accumulation, when the Fermi level is moved close to the HOMO the charge state of the defect, is neutral. However, in depletion, an acceptor-like state is negatively charged, and manifests itself as a shift of the transistor onset voltage to more positive voltages [53]. Equivalently, a donor-like state favours a neutral charge state when the Fermi level is above a characteristic energy E(+/0), and becomes positively charged when the Fermi level is moved below this energy level. A donor-like trap can

capture mobile holes formed under hole-accumulation conditions, and trap them in a positive charge state. Such trapped holes still contribute to the overall charge that is induced by the gate voltage, but are no longer mobile, and result in a shift of the threshold voltage to more negative voltages.

The localized electronic states within the bandgap of the semiconductor or the dielectric damages inside the device behave not only reducing the effective mobility of the mobile carriers but also increasing the threshold voltage [13].

When discussing threshold-voltage shifts in organic FETs, it is important to distinguish between trapping and recovery processes that involve shallow and deep trap states and occur on different timescales. In the case of a short, continuous stress applied typically for less than 100 s, the device recovers very rapidly (within a few seconds) and almost fully to its original state, that is, most charges are trapped in shallow trap states from which they can escape rapidly. For longer bias stress times, there is still a partial rapid recovery, together with a longer-lived component of the threshold voltage shift, which is due to charges trapped in deep states. Also this long-lived component eventually recovers, but on a much longer time scale, of several hours or days in the dark. When the stress is removed, the device recovers close to its original state within a few days. It is believed that the stabilization of V_T after a few hours of stress is a result of a balance between continued charge trapping and recovery/charge detrapping on a time scale of hours/days [55].

The trapped charges created by bias stress have been observed directly using Scanning Kelvin Probe Microscopy (SKPM). Burgi et al. [20] observed a positive electrostatic potential in the channel after biasing the device in the ON state for an extended period of time and then switching it OFF. This is due to trapped charges remaining in the film after switching off the device. The release of the trapped charge over several hours could also be tracked with SKPM, and it was found that exposure to above band-gap light accelerates the detrapping process significantly. These effects may be present even in a highly pure crystal, probably originated from the tendency of the material to react with oxygen and water present in the atmosphere [14,15].

Kalb et al. [15] showed that molecular single-crystal FETs of rubrene and pentacene with a low-k gate dielectric (Cytop™, a fluoropolymer, which eliminates any moisture from the active interface) do not exhibit any measurable threshold-voltage shift during positive and

negative gate-bias stress at V_G = -70 V for up to 2 hours in an inert helium atmosphere ($|\Delta V_T|$ < 0.2 V). This experiment provides a proof-of-principle demonstration that in a well-ordered organic single crystal in the absence of moisture and oxygen, very high levels of stability can be achieved. The stability of thin films is significantly worse, however. In the same work, it is reported that polycrystalline pentacene TFTs fabricated in the same device structure and tested under the same conditions showed a significantly larger negative gate voltage shift of $|\Delta V_T|$ = 5.2 V when applying V_G = -70 V for 2 hours. This could possibly be taken as an evidence that structural defects present in the thin films play an important role in charge trapping, but a thin film will also generally have higher levels of residual extrinsic impurities. In addition, many thin film technologies suffer from variations in the threshold induced by stress polarization and temperature. For example, in p-type organic semiconductors it is often observable a shift in the negative threshold voltage after a prolonged operation of the device in accumulation, generally attributed to trapping of the charges in the semiconductor and / or at the active interface [16,17].

For quantitative assessment of threshold-voltage shifts, a number of models have been developed and used extensively to describe the threshold-voltage instabilities in a-Si TFTs [18]. Also in this material, the cause of threshold-voltage shifts under prolonged operation in ON condition is that some of the mobile charge carriers in the channel become trapped in pre-existing or stress-generated deep localized states in the semiconductor, in the gate dielectric, or at the active interface. Once trapped, they no longer contribute to the current, and a higher gate voltage to apply is needed to achieve the same mobile-carrier concentration and current.

In studies of the bias-stress effect it has become customary to describe the threshold-voltage shift $\Delta V_{th}(t)$ using a stretched-exponential function (Eq. 3.4) [21,22]:

$$\Delta V_{th}(t) = V_0 \left(1 - \exp[-(t/\tau)^{\beta}]\right) \quad (3.4)$$

This fitting practice is analogous to the analysis used to describe threshold-voltage shifts in amorphous silicon-based field-effect transistors. In analyzing threshold-voltage shifts in OFETs, β and τ are treated as fitting parameters, V_0 is close to the applied gate bias voltage, τ is referred to as relaxation time, and it is essentially a measure of the time scale

of the threshold-voltage shift in OFETs. β is an exponent and indicate the non-exponential behaviour of the threshold-voltage shift. This fitting procedure is useful when comparing the stability of different OFETs.

3.5 Stability of OTFT

Some of the first data on bias stress stability and threshold-voltage shifts in organic FETs were reported by the group at Philips. In pentacene FETs and using poly-thienylenevinylene (PTV) and SiO_2 gate dielectrics, the threshold voltage was found to shift in the direction of the applied gate-bias stress. The degradation was found to be reversible, allowing to operate the devices for extended periods of time. The magnitude of the threshold voltage shift was similar for SiO_2 and SiN_x gate dielectrics, suggesting that trapping occurs in defect states located in the semiconductor [19].

The instability of the OTFTs due to a bias stress was observed to be related not only to the interface with the dielectric in the channel, but also to the interface between the contacts metal and the organic semiconductor. The decay of the bias current during the stress results from the combination of the variation of the contact resistance and the shift of the threshold voltage in the channel. These results suggest that the time dependence of the charge trapping in deep states, both in the region of the contact and in the channel region, is responsible for the effects of bias stress in organic thin film transistors [16].

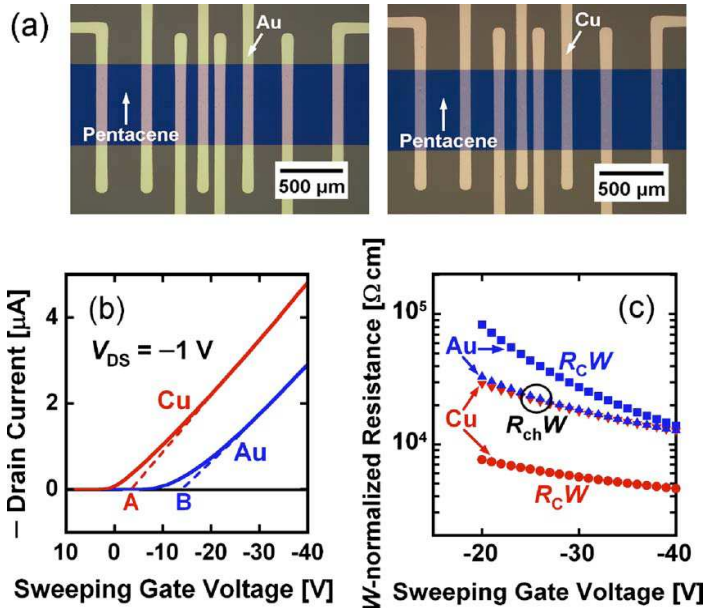


Fig.3.3. Effects of the bias stress on two devices having different source and drain contact [16].

In general, the instability from stress polarization refers to long-term changes in the properties of the transistors, that tend to lose the saturation regime until they becomes unusable, while the phenomenon that generates reversible short term changes it is called hysteresis; this one leads to cycles in the measured characteristics dependent on the direction in which the bias voltage is moved. Hysteresis is an undesirable memory effect, in which the DC characteristics of a transistor, measured in a certain instant of time, depend on the voltages applied to the device in the past. Physical causes of the instability and of the hysteresis are, however, similar [23,24].

Kim et al. [25] investigated the role of residual solvent in films of 6,13-bis(triisopropylsilylethynyl) (TIPS) pentacene and of triethylsilylethynyl antradithiophene (TES-ADT), and showed that films deposited from toluene exhibit significantly lower hysteresis as well as better threshold-voltage stability than films cast from chlorobenzene. The more polar chlorobenzene solvent is thought to contain more moisture and ionic impurities (such as HCl), resulting in a positive threshold voltage shift upon negative gate bias stressing.

In the literature, it is reported also an increase of the levels of the OTFTs current after stress by static polarization. This effect is attributed to the polarization of the polar molecules of dielectric materials having pendant hydroxyl groups (for example, PVP), subjected to the electrical stress. This polarization remains even after the removal of the

stress voltage, thus causing a residual field in the channel, which accumulates additional free charges during usual operations of the devices, and so resulting in an increase of the current in the channel. Through this mechanism, it is also possible to explain the increase of the off current due to electrical stress for these devices [26-30].

The organic TFT are also sensitive to light: absorbed photons generate free charges in the channel region, which are transported to the electrodes under the applied drain voltage, resulting in a current increase under lighting [31].

The positive trapped charges in the channel lead to an increased curvature of the potential profiles, particularly in the vicinity of the drain electrode, because the drain region is most sensitive to the charge trapping because of a lower carrier concentration. Near the drain, a higher electric field along the channel is needed to compensate the loss of mobile carriers due to trapping. The light-induced recovery behaviour was investigated in detail by Salleo et al [32]. If an exciton during its short (nanosecond) lifetime collides with a trapped hole, there is a finite probability that the electron recombines with the trapped hole, leaving behind a mobile hole, that can escape from the channel. The light-induced recovery process follows the absorption spectrum of the organic semiconductor, so providing a strong indication that the relevant traps are located within the semiconductor, and does not involve charge injection into the gate dielectric.

3.6 Role of extrinsic factors for devices stability

One of the important questions about the stability of the OTFTs is whether bias stress effects are primarily caused by extrinsic factors, such as oxidation, presence of moisture, chemical impurities, or instead the intrinsic structural and energetic disorder of the organic semiconductors and/or specific structural defects are responsible for the charge trapping. Closely related to this is also the choice of gate dielectric, which can generally influence the device stability in a number of different ways (e.g., the polarity of the gate dielectric has effect on the sensitivity of the devices to moisture and ion migration).

Zilker et al. [33] found that in a photoresist-based polymer dielectric, exposure to humidity results in an increased ion migration in the gate dielectric, which causes a shift of the threshold voltage in the opposite direction respect to the polarity of the gate bias.

Gate dielectrics made of polar polymers, such as PVP, are particularly prone to this effect [34], while low-k, apolar polymeric dielectrics do not usually exhibit this behaviour. This is closely related to the phenomenon of hysteresis observed in many OFET structures. There is clear evidence in many systems that hysteresis is due to the moisture uptake in the polar polymeric dielectric. Noh et al. [35] showed that hysteresis observed in a pentacene FET with a PVP gate dielectric disappears upon annealing the device at 120°C in vacuum and reappears upon subsequent exposure to moisture, suggesting that the moisture primarily induces a polarization of the bulk of the dielectric instead to cause a specific modification of the interface electronic structure. Hong et al. [36] showed that even in the case of an apolar polymeric dielectric, such as polystyrene, prolonged atmospheric exposure results in an increased gate leakage and OFF current, a negative shift of the turn on voltage, and an increased hysteresis.

Not protected and encapsulated organic devices suffer degradation due to water vapor or oxygen absorption. The air influences the parameters of the transistor such as the mobility, the on / off ratio and the threshold voltage [37].

The oxygen atoms can bind to aromatic rings of the semiconductor, forming new molecules and introducing therefore states that make available acceptors of the negative charges at the grain boundaries of the material and at the surface of the dielectric, resulting in a shift of the threshold voltage. Similarly, the oxidation creates scattering centers responsible for the reduction of the operating current [38,39].

It is known that the association of a molecule with a low ionization potential (as an electron donor) with a molecule with high electron affinity (electron acceptor) can lead to the formation of a pair or a donor - acceptor charge transfer complex. In a study conducted by [39] Hu, Yan et al.,, the current in saturation and the mobility of OTFTs increase with the decrease in the percentage of oxygen in the mixture of nitrogen and oxygen to which the device is subjected, and decrease with the increase of the oxygen component. The reason is that O_2 can easily bind with pentacene and allow the transfer of charge.

Due to the covalent bonds, the ions H^+ and OH^- form crystal defects and act as traps for charge carriers, going to polarize the interface between the gate dielectric and the semiconductor, and causing once again the variation of the threshold voltage [40].

Kumaki et. al. [40] have reported a study on the positive displacement of the threshold voltage caused by the presence of molecules of H_2O and O_2 in p-type and n-type OTFT. The positive displacement of V_T is attributed to the deprotonation of SiOH on the surface of the insulator, that is induced by an adsorption of H_2O and O_2. The presence of H_2O induces a shift of V_T more marked than that induced by the presence of O_2. Therefore, it is possible that the electrochemical reaction at the interface is related to deprotonation of SiOH with O_2.

Gomes et al. [41] observed anomalies in the temperature dependence of the FET current at a temperature around 200 K, for several different organic semiconductors, suggesting a common origin. They attributed this to a phase transition of water incorporated in the organic semiconductor, from a supercooled liquid state above 200 K to a solid state below 200 K (Fig.3.4). They also investigated the stress behaviour as a function of temperature, and found that below 200 K stress effects are much reduced, suggesting that liquid water might be responsible for the charge trapping behaviour at room temperature.

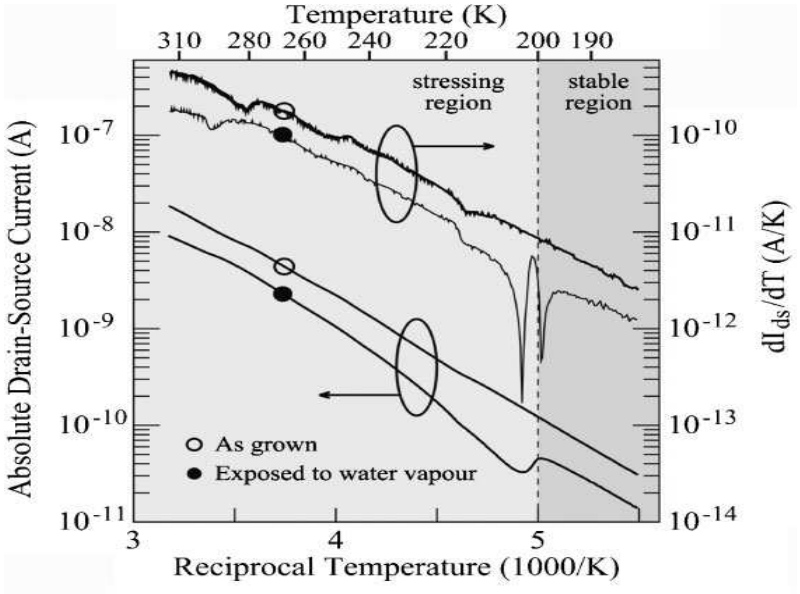


Fig.3.4. Temperature dependence of the drain-source current in the linear region Vsd = -1 V and Vg = -8 V of PTAA bottom-gate, bottom-contact OFET on HMDS treated SiO2. The lines with open circles show the behaviour of the as-grown device. The lines with filled circles show the behaviour after exposure to water. To highlight the water-induced anomaly at 200 K, the derivatives of the curves are shown in the top part of the figure [41].

Li et al. [42] showed that the transistor current and field-effect mobility, in several small molecules organic semiconductors, with increasing humidity degrade more in short

channel devices than in long ones. From these results, it is clear that ingress of moisture into the organic semiconductor or presence of moisture at the interface with the gate dielectric is an important factor that degrades the bias-stress stability of many organic semiconductors. The effect is likely due to local polarization effects associated with the large dipole moment of the H_2O molecule, as opposed to a chemical reaction of the water with the organic molecules.

It is important, therefore, for the stability of the OTFTs and their operation in the air, to consider the influence of H_2O and O_2 not only on the organic semiconductor, but also the presence of these pollutants at the surface of the gate insulator.

3.7 Role of the gate dielectric

The gate dielectric has an important influence on the hysteresis behaviour and on reliability of organic FETs. Strong hysteresis effects are commonly observed with polar gate dielectrics, such as PVP [43] or PVA, which are hygroscopic and prone to contain a significant concentration of ions. The hysteresis effects can be reduced by careful crosslinking [44,45], or by inserting an inorganic barrier layer in contact with the gate electrode [43,46,47].

Specific functional groups on the surface of the gate dielectric can trap charges in the organic semiconductor. There is clear evidence that charge trapping in the gate dielectric or on its surface is not directly relevant, but the charge-trapping sites are located within the organic semiconductor itself. Salleo et al. [48] compared threshold voltage shifts in F8T2 devices with different gate dielectrics, and found that when the threshold-voltage shift, induced by negative gate-bias stress, is corrected for the differences in the induced charge concentrations due to different dielectric constants, it was found to be relatively insensitive to the choice of the gate dielectric.

However, even in systems where electronic states on the surface of the dielectric are not directly involved in charge trapping, the dielectric still has an important influence on hysteresis and long-term stability. The polarity of the gate dielectric determines the electronic structure at the active interface.

Richards et al. [49] recently developed a quantitative model for the disorder broadening due to this charge–dipole interaction at the interface, and showed that the density of states of the organic semiconductor layer in direct contact with the gate dielectric at the interface is broadened significantly, compared to that a few angstroms away from the interface, and contains a significantly higher density of deep trap states (Fig.3.5). These are believed to be responsible for the increased hysteresis and lower threshold voltage stability reported for higher-k gate dielectrics [50].

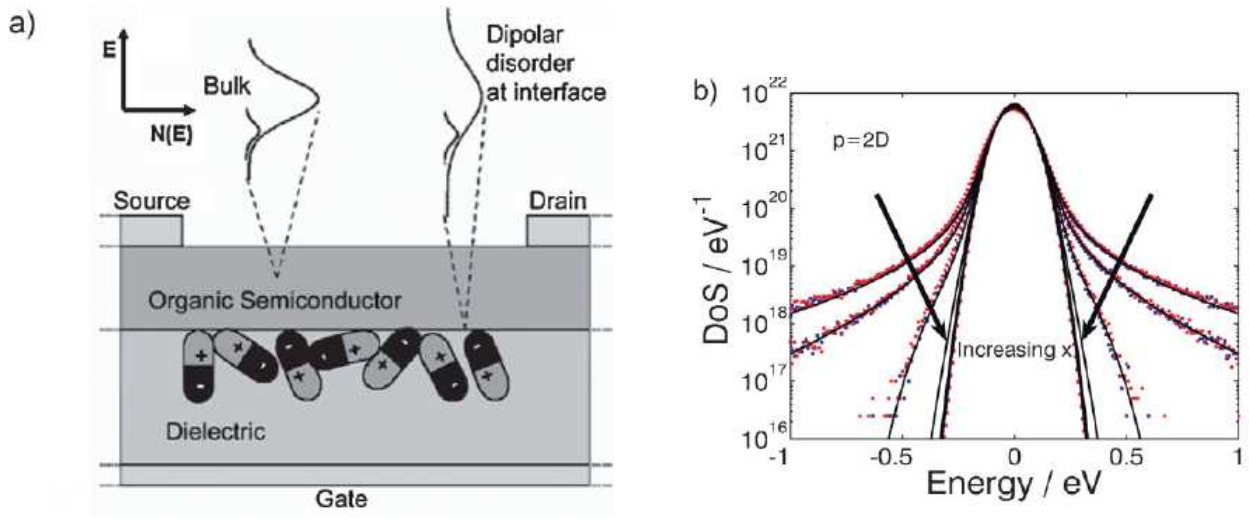
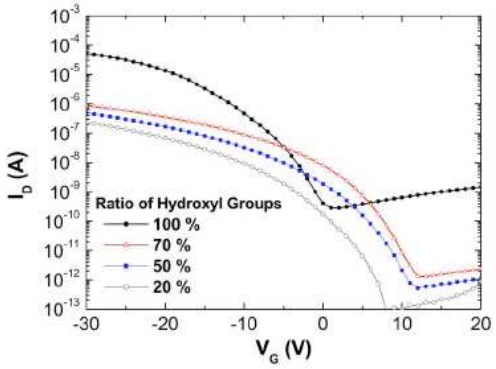


Fig.3.5. a) Schematic diagram of the effect of disordered polar groups on the energetic disorder at the active interface. b) Calculated DOS broadening due to static dipolar disorder in a dielectric with dipole moment of 2 Debye (D) with increasing distance into the semiconductor. Each line corresponds to a different distances x of the location in the organic semiconductor from the dielectric interface, varying from x = 0 Å (broad DOS right at interface) up to x = 5 Å (bulk-like DOS). The dashed line indicates the unbroadened Gaussian DOS in the bulk with a characteristic width of 60 meV. The dots come from numerical simulations including either just the nearest dipole (n = 1, blue squares) or the nearest ten dipoles (n = 10, red circles) [49].

Sangyun Lee, Koo and Bonwon [51] intentionally synthesize dielectric polymer (PVP) having different percentages of concentration of hydroxyl groups, to study the effect of hydroxyl groups on the electrical properties of the organic transistors based on pentacene. Obvious hysteresis effects, usually observed in OTFT devices, confirmed to be strongly linked to the hydroxyl bonds existing within the polymeric dielectrics. These effects are therefore reduced by replacing them with cinnamoyl groups.

Although the hydroxyl groups deteriorate the characteristics of the capacitance-voltage (C-V) and result in an increase of the gate current, mobility becomes exceptionally high (5.5 cm^2/Vs). This high value of mobility can be achieved by increasing the number of hydroxyl groups, but it is not correlated with an improvement of the crystallinity degree of pentacene, instead it depends on the characteristics of the interface between semiconductor and dielectric (Fig.3.6) [51].



Ratio of hydroxyl groups (cinnamoyl group) (%)	Dielectric constant	Mobility ($cm^2 V^{-1} s^{-1}$)	On/Off current ratio
100 (0)	4.04	5.5	$\sim 10^5$
50 (50)	3.47	0.06	$\sim 10^6$
35 (65)	3.44	0.045	$\sim 10^6$
20 (80)	3.34	0.03	$\sim 10^6$

…

Fig.3.6. Trans-characteristics and parameters related to OTFTs having dielectrics with different percentages of the concentration of hydroxyl groups [51].

Anyway, some dielectrics have a good stability; in fact, Umeda et al. [52] investigated bottom-gate top contact pentacene TFTs with a Cytop™ gate dielectric, and demonstrated that these devices have good threshold voltage stability against negative gate-bias stress in air ($|\Delta VT|$ = 1.1 V, after 10^4 s at $V_G = V_{DS}$ = -20 V). This was also claimed to be better than the stability of a-Si TFTs.

However, better scientific understanding is still necessary in order to further improve the reliability of organic FETs and to address applications, such as active matrix addressing of organic LED displays, where higher levels of operational stability exceeding those achievable with a-Si TFTs are required. The study of the defect electronic structure of organic semiconductors will remain an interesting and important subject in the coming years.

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Chapter 4
Fabrication of OTFTs

The organic semiconductors are not able to compete with inorganic semiconductors regarding electrical properties, but one of the major goals of OE is to produce organic devices and systems at very low costs for applications where these limitations are not an issue. According to this idea, very fast and simple deposition techniques have been developed for the mass production.

The manufactures of OTFTs (organic thin film transistor) using polymers or small molecules are slightly different, but have the same steps: purification of organic materials, deposition of dielectric material on a conductor (TFT gate), electrodes deposition (source and drain) and semiconductors deposition. The order in which steps are performed depends on the chosen structure for the OTFT.

Thanks to the good mechanical properties and to the simplicity of the deposition process of organic semiconductors, the OTFTs can be fabricated on any substrate which is sufficiently flat.

During the PhD activity, different types of transistors have been prepared, changing some technological parameters, to understand the influence of these parameters on the stability of the devices. The transistors have been manufactured in a clean room class 100, on borosilicate glass substrates where the structures of the contacts and of the islands of semiconductor have been defined.

Four OTFT configurations have been analysed, which include:

- ✓ *two different concentrations of dielectric polymer and crosslink agent,*
- ✓ *two different solvents in which the semiconductor is dissolved, and the films cured at 60°C for one minute to evaporate the solvents.*

The OTFT are in bottom-contact bottom-gate configuration.

The gate has been made of ITO (indium tin oxide), patterned by photolithography technique and chemical etching; the source and drain electrodes have been made of gold, deposited by thermal evaporation in vacuum through a shadow mask.

Soluble organic materials have been used for the dielectric and for the semiconductor.

In particular, PVP (poly-4-vinylphenol) was used as the dielectric polymer, cross-linked (with two different recipes) to make it more stable, and deposited on the substrate through the spin coating technique.

The semiconductor material used has been the TIPS-pentacene (6,13-bis (triisopropyl-silylethynyl)-pentacene), deposited by drop casting using two different solvents: chlorobenzene and orthodichlorobenzene.

In this chapter, an overview of the techniques used to fabricate semiconductor thin films, dielectric thin films and the contact electrodes of OTFTs, is reported. Then, the semiconductor and the dielectric materials, used for the OTFTs of this thesis, together with the physical characterisations of these materials are also presented.

4.1 Architecture of the devices

The chosen structure for the OTFTs has been the Bottom-Gate Bottom-Contacts (BGBC) one (Fig.4.1). BGBC is particularly convenient from the technological point of view, because, wanting to fabricate a circuit, even complex, the conductive interconnections between the devices can be fabricated before the deposition of the semiconductor, without any risk to affect the active area of the devices. Moreover, exposing the surfaces of the insulator and of the contacts to subsequent processes, this structure can be used to prepare a "standard" OTFT optimizable by surface treatment, and in which the deposition of the layer of the semiconductive material can be made by solution (e.g. drop-casting, zone casting or printing techniques) or by evaporation, depending on the material chosen.

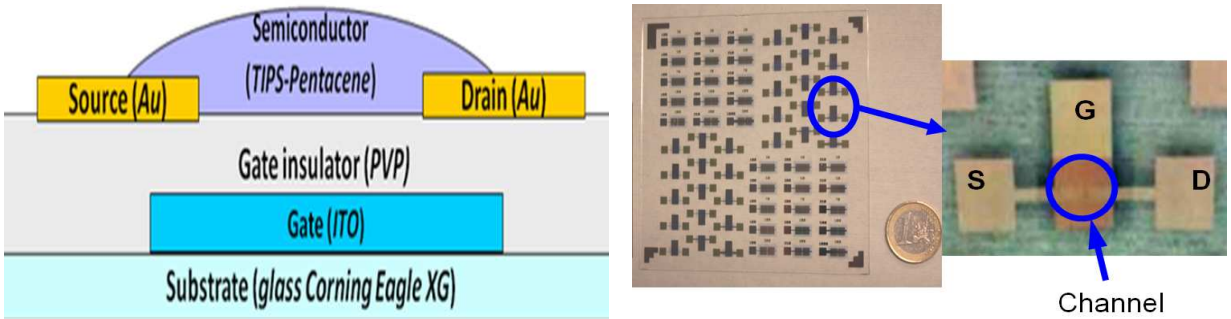

Fig.4.1. (left) Schematic cross-section of the Bottom-Gate Bottom-Contacts (BGBC) structure of the devices tested in this thesis; (right) photograph of a sample of the fabricated devices.

The BGBC structure has been chosen because of the simplifications of the fabrication process that it offers, as theoretical and experimental studies give evidence that devices made in Top-Contacts (TC) configuration, in the absence of process optimization, outperform their Bottom-Contacts counterparts [1,2]: simulations of the channel current show that in the case of TC configurations the presence of the charge induced by the field below the electrodes modulates the contact resistance [3], making this configuration more advantageous from the point of view of the performances.

4.2 Fabrication process of the devices

The realization of the devices used in the present study is briefly described by the following steps, also indicating the variants under study:

1 . Substrate: ***Glass***

2 . Gate: commercial ***ITO (Indium Tin Oxide)*** patterned by photolithography and chemical etching

3 . Dielectric: ***PVP (poly -4- vinylphenol)***, deposited by spin-coating using the following recipes:

a. Recipe 1: PVP (15 wt %) + 3 % poly (melamine - co -formaldehyde) methylated) CLA (cross-linking agent) in PGMEA (propylene glycol monomethyl ether acetate)

b. Recipe 2: PVP (10 wt %) + 5 % CLA in PGMEA

4 . Cross-linking of ***PVP***

a. Recipe 1 - **PVP1**, *curing at 150°C for 10 minutes and 200°C for 20 minutes*

b. Recipe 2 - **PVP2** *curing at 100°C for 1 minute and 200°C for 5 minutes*

5 . Source and Drain: ***Gold***, evaporated in vacuum and patterned by shadow mask

6 . Semiconductor: ***TIPS-pentacene (6,13- bis (triisopropyl - silylethynyl))***, deposited by drop casting and dissolved in:

a. ***Chlorobenzene (CB)*** - Boiling point 138°C

b. ***ortoDiCloroBenzene (o-DCB)*** - Boiling point 198°C

7 . Solvent evaporation from TIPS films: annealing at 60°C for one minute.

Below are detailed the different processes for the deposition of the dielectric, semiconductor and electrodes.

4.3 Fabrication techniques

The following sections are dedicated to the description of the technologies employed for the fabrication of the OTFTs studied in this thesis. In particular, the organic materials depositions and the patterning of the metal electrodes will be described.

4.3.1 Sputtering

The technique used for the deposition of the ITO on glass substrate has been *sputtering*. Sputtering is based on the momentum exchange of accelerated ions incident on a target made of material to deposit [4]. At very low kinetic energies (< 5 eV), the interaction is confined to the outermost surface layer of the target material. Ions, such as Ar and Xe, are used for bombardment as these can be accelerated to any desired kinetic energy with applied electric fields. Ions can be supplied in a number of different ways, for example by a glow discharge (diode, triode and magnetron) or an ion beam. Non-magnetron sources, especially ion beam sources and RF planar diodes, are widely used.

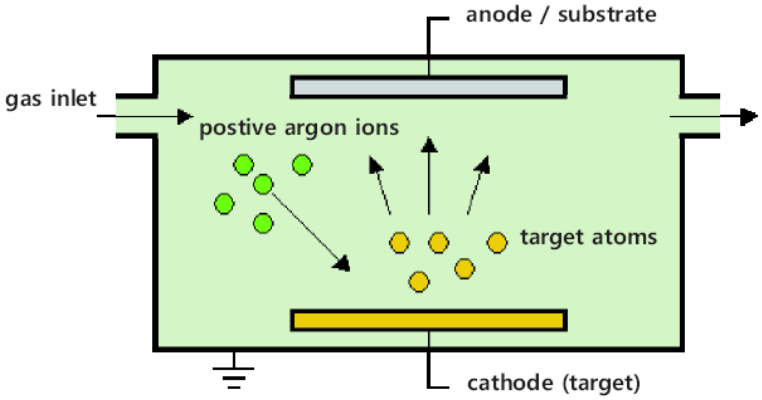

Fig.4.2. DC planar diode system for sputtering deposition of thin film.

Figure 4.2 shows a schematic diagram of a simple DC planar diode sputtering system. It consists of two electrodes, the cathode and anode, placed inside a vacuum chamber and connected to an external high-voltage power supply. The material to be sputtered, the

target, is the cathode. The chamber is pumped down by a vacuum pumping system to pressures well below the desired operation pressure. At this base pressure, gas (Ar or Xe) is admitted back into the chamber at the desired pressure. A high electric field is applied between the electrodes, causing the ionisation of the gas and forming a plasma. Positive gas ions are then accelerated by the electric field so that they hit the cathode with considerable energy and cause sputter some particles of the target material. Some secondary electrons are also produced at the cathode and these accelerate towards the anode and help to maintain the plasma. To use insulating materials as either targets or as substrates in the sputtering system, a DC potential cannot be used, because of the accumulation of electric charges on the biased insulating surface; RF power must be applied to the electrodes. The sputtering technique has been used also with some organic polymers, such as polytetrafluoroethylene (PTFE), which are difficult to evaporate [5].

4.3.2 Photolithography

Following the deposition of the ITO, the substrate was subjected to a *photolithography* process, to define the structures of the gate electrode.

Photolithography is a very common technique widely used in Semiconductor industry for the patterning of the materials of the devices. The goal of this technique is to transfer a certain pattern or drawing on a substrate. For this purpose two elements are required: i) a mask, which reproduces the image to transfer on the substrate and must be opaque to ultraviolet (UV) light; ii) a photosensitive material, called photoresist, which is exposed to ultraviolet light during the process by interposing the mask between an UV source and the surface of the photoresist. There are two types of resists, namely, positive and negative photoresist. Positive resist is 'softened' by exposure to the UV light and the exposed areas are subsequently removed in the development process, the resist image will be identical to the opaque image on the mask. Negative resist is 'hardened' by exposure to UV light and therefore it is the unexposed areas that are removed by the development process, so the resist image will be an inverted (negative) image of the mask. Photoresists are sensitive to a wide range of wavelengths of light, typically 200 - 500 nm. This range of wavelengths includes the visible blue and violet wavelengths contained in normal white light, so, for

this reason, photolithography process is usually performed in a special filtered ambient light, to remove all of the wavelengths to which the resist is sensitive.

Photoresist films are deposited onto the sample surface generally by spin coating. Before the exposure process, heating of the sample (soft baking) is usually required, in order to dry the deposited photoresist. Then, during the exposure phase, the photoresist layer is exposed to UV light through an opaque mask. In this way it is possible to transfer the mask pattern on the resist film. After exposure, the resist is developed in order to remove the unwanted resist, thus leaving only the defined pattern on the substrate. Usually, a post baking step is made, to increase resist adhesion to the substrate and to increase its resistance to etch process. Taking advantage of the presence of the patterned resist film, it is then possible to etch away the beneath layers from areas they are not needed. Once the etching process is performed, the photoresist can be removed using an organic solvent, generally acetone, or oxygen plasma, and the basic structure for the realization of the final device is assembled.

4.3.3 Spin coating

The PVP dielectric was deposited on the entire substrate with the *spin coating* technique.

To deposit thin films of polymers or of some small molecules, it is necessary that they are previously dissolved in a solvent to form a solution. The spin-coating process starts depositing a small amount of organic material in liquid form on the substrate, then rotating the sample at a speed of 500 to 10000 rpm, to spread the fluid by centrifugal force, to push a part of it off the edges of the substrate and form a solid thin layer thanks to the flow and the evaporation of the solvent from the fluid. The desired thickness is controlled by the rotational speed (the higher the angular speed of spinning, the thinner the film) and by the initial concentration of the solution deposited on the substrate.

The thickness of the film produced, d, is governed by the equation:

$d = k\,\omega^{\alpha}$

Here, ω is the angular velocity and k and α are empirical constants for given solvent, polymer and substrate.

Thickness, morphology and surface topography of the films produced using this method have been found to be very reproducible. Anyway, there are two major disadvantages with spin coating: there is a significant amount of waste produced, as most of the solution is lost through radial spreading, and then spin coating is in no way scalable to very large substrates or commercial production. Because spin coating is normally done on a small scale, the waste is not an issue, although for industrial purposes spin coating is not a viable option.

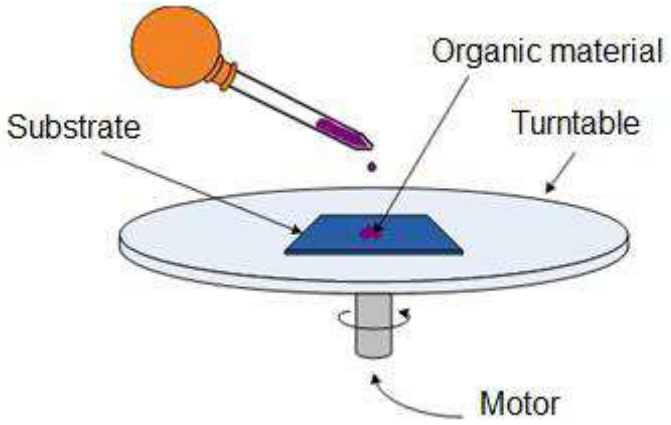

Fig.4.3.Spin coating technique.

4.3.4 Thermal Evaporation

After the cross-link of the dielectric, the gold contacts were deposited by *thermal evaporation* through a shadow mask.

Solid materials vaporise when heated to a sufficiently high temperature. Thin film deposition then occurs, as molecules are removed from a solid or liquid (generation of the depositing species) and then travel over some distance in a vacuum chamber (transport of species from source to substrate) and sublimates on the substrate (film growth on the substrate). According to the Langmuir expression, the rate of evaporation Γ (in kg m^{-2} s^{-1}) from a surface is given by

$$\Gamma = P\left(\frac{M}{2\pi RT}\right)^{\frac{1}{2}}$$

where P is the vapour pressure (in N m^{-2}) of the material at temperature T (in K), M is the molecular weight and R is the gas constant [5]. Also in a vacuum chamber, the molecules

travel at high velocities but make frequent collisions with residual gas molecules such as N_2, O_2, H_2O and CO_2. From kinetic theory, the mean free path of gas atoms (λ) is given by

$$\lambda = \frac{k_B T}{P \pi d^2 \sqrt{2}}$$

where d is the diameter of the molecules and k_B is Boltzmann's constant [5]. The use of low pressures is necessary because it leads to straight line paths between the source and the substrate. In the pressure range of 10^{-5} - 10^{-8} torr, the mean free path is very large (10^2 to 10^5 cm) as compared to the source-to-substrate distance.

Relevant characteristics of thin film growth are: the substrate temperature, the evaporation rate, and the chemical and physical natures of the substrate surface. Residual gas molecules in the chamber also have an effect: the most probable scenario is that some of residual gas molecules to be trapped in the film or that chemical reactions occur between residual gas molecules and evaporated molecules . A schematic diagram of a thermal evaporation system is shown in Figure 4.4. Typically, it consists of a bell jar, a vacuum pumping system, a 'boat' where the material to deposit can be thermally heated to the sublimation temperature by Joule effects or sometimes with an electron gun, and a substrateis accommodated at a certain distance from the source. A quartz crystal microbalance is generally used to measure the thickness of the film during the deposition, by monitoring the change of its oscillating frequency as the evaporating species condenses on it.

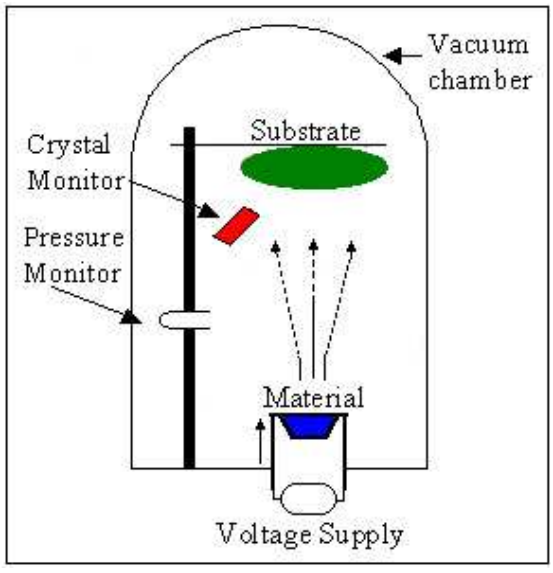

Fig.4.4. Thermal evaporation system for thin film deposition.

4.3.5 *Drop Casting*

Finally, the TIPS-pentacene semiconductor was deposited by *drop casting* technique.

Drop casting is the simplest way to produce a thin film. In this coating method, a horizontal surface is required and the polymer solution is dropped or poured on it and the solvent is evaporated spontaneously. In Figure 4.5 the technique is illustrated, and in Figure 4.6 a SEM image of an example of the obtained films of TIPS-pentacene is shown.

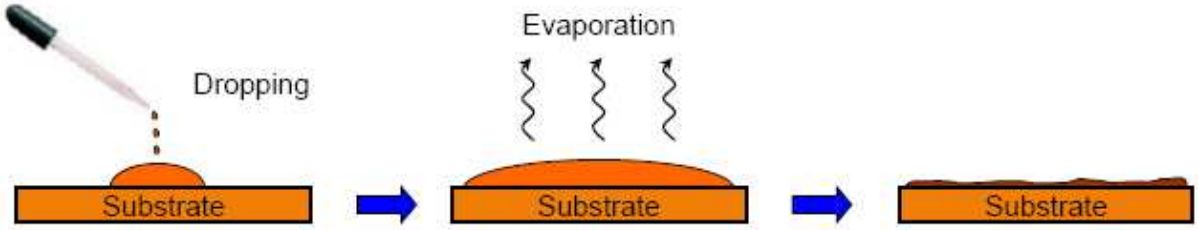

Fig.4.5. Drop casting technique.

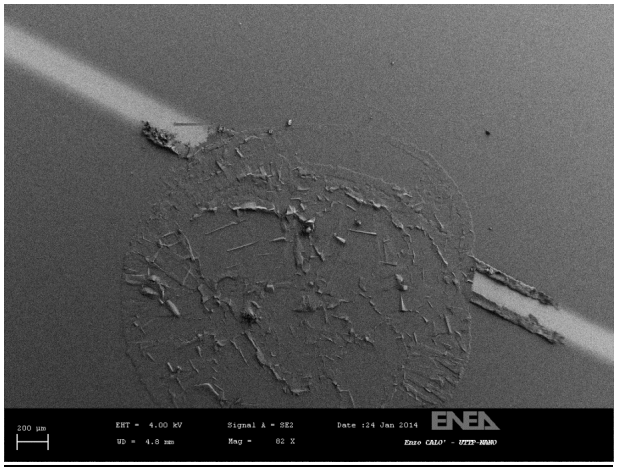

Fig.4.6.:SEM image of the TIPS-pentacene, deposited via drop casting, in the channel of an OTFT tested in this thesis.

The advantages of this technique are the simplicity and the possibility of no waste material; but this method provides no major control with respect to the film thickness, that is proportional to solution concentration. Moreover. there is a limitation in large area coverage.

4.4 Organic Materials and layer characterization

4.4.1 TIPS-pentacene

Pentacene is the organic semiconductor which exhibits the highest performances in terms of stability and of measured mobilities (up to 1 cm^2/Vs for polycrystalline pentacene films [6] and up to 30 cm^2/Vs for pentacene single crystals [7]). It is an organic molecule with chemical formula $C_{22}H_{14}$ and with a planar structure composed of five linearly fused benzene rings, depicted in Figure 4.7. It appears, at ambient conditions, as a purple powder and it is typically deposited by thermal evaporation, since it shows insolubility in most organic solvents. This unprocessability in liquid phase represents a huge limitation in terms of its deposition using low cost printing techniques. Even, pentacene has a crystalline order, often referred to as herringbone packing (Figure 4.9(a)) with only minimal π-stacking, which results in a poor dispersion of the electronic bands in the solid, implying that pentacene transport properties may be limited by its crystal packing [8].

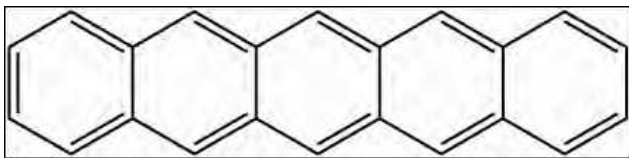

Fig.4.7. Chemical structure of pentacene.

In order to overcome the insolubility issue, several pentacene derivatives have been developed by addiction of different functional groups to the basic molecule. Through these functionalizations, also tuning of the electronic properties of the new material, such as charge injection barriers, HOMO-LUMO gaps, charge transfer rates, and molecular ordering of pentacene, can be accomplished. Among these pentacene derivatives, triisopropylsilylethynyl-substituted (TIPS) pentacene is very popular and applied for thin-film transistors [9]. Its complete name, 6,13-bis(triisopropylsilylethynyl) pentacene suggests its chemical structure, depicted in Figure 4.8: the carbon atoms of the triisopropylsilylethynyl chains are bonded with the carbon atoms in position 6 and 13 of the pentacene molecule.

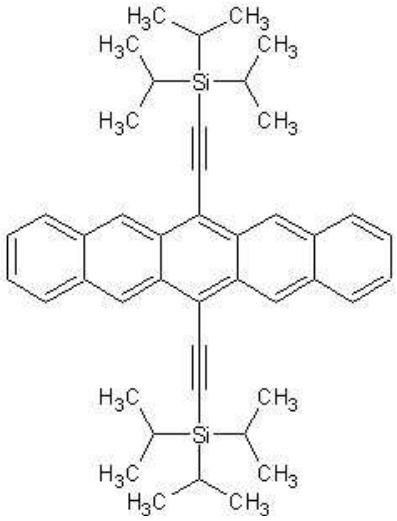

Fig.4.8. Chemical structure of TIPS pentacene.

It has sufficient solubility in common organic solvents (e.g. toluene, chlorobenzene, tetrahydrofuran and chloroform [10]) and, in addition, the bulky functionalized groups in TIPS-pentacene efficiently maximize π-orbital overlap [8]. In fact, the bulky group substitution on the central aromatic ring disrupts aromatic edge-to-face interactions, preventing the herringbone packing motif, typical of the unsubstituted pentacene crystals: the triple bond between the carbon atoms (see Figure 4.8) allows adjacent molecules to interact in a face-to-face π-stacking orientation, since the substituents are hold away from the aromatic surface. This inter-molecular interaction improves π-orbital coupling and potentially increases the carrier mobility [8][11]. In Figure 4.9, the molecular packing arrangements are shown, reporting also the average distances between the π-faces in (a) the solid state pentacene and (b) TIPS-pentacene.

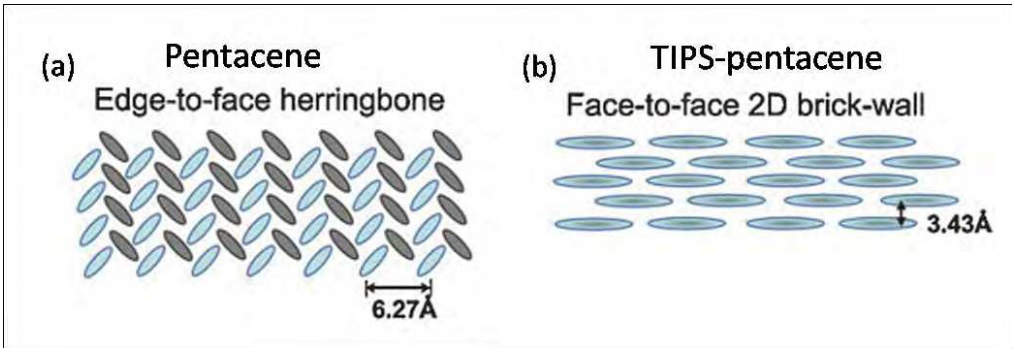

Fig.4.9. Molecular packing arrangements with average distances between the π–faces in the solid state for (a) pentacene and (b) TIPS-pentacene [14].

Thanks to its solubility in a wide range of organic solvents, TIPS-pentacene is commonly deposited by spin coating [11], drop casting [10][12] and inkjet printing [13], in order to form the active layer in OTFTs. The electrical characteristics of such devices were found to be highly dependent on processing conditions, i.e. the solvent used, the post processing treatment and the deposition method, since they determine the morphology of the deposited semiconductor film [11][14].

The highest electrical performances have been found in transistors with single crystal TIPS-pentacene, because they are free of grain boundaries and molecular disorder, which limit the charge transport through the material. Usually, to use a high boiling point solvent and the drop casting technique allows slower solvent evaporation leading to highly ordered films: mobilities up to 1.8 cm^2/Vs in drop casted TIPS-pentacene OTFTs are reported in literature [11].

4.4.2 PVP - Poly(4-vinylphenol)

Poly(4-vinylphenol) is a weak acid polymer. Due to the variety of its applications and simple fabrication process, many research groups have investigated its properties [15,16,17]. Applications of this polymer include the use as gate dielectric insulator in the microelectronic field, and responsive surface coating [18].

The interest for the PVP in this thesis work lies in the fabrication of thin films for potential application as dielectric layers applied via spin-coating process. However, when the dielectric is a polymer, a cross-linker agent should be applied to support the impact of solvents and bases from further subsequent process steps. The cross-linking reaction

should not leave any mobile ions in the film and the cross-linker agent used in the photoresist should be avoided [15]. Moreover, the cross-linked polymer should have a very smooth surface, high electrical field strength, preferably a high dielectric constant, high purity, and be hydrophobic while still allowing sufficient adhesion to adjacent layers. The cross-linked PVP is normally prepared from solution using propylene glycol methyl ether acetate (PGMEA) as solvent, and poly(melamine-co-formaldehyde)-methylated as a cross-linker agent [15,19,20]. Figure 4.10 presents the chemical structures of these polymers, (a) is the pure PVP, (b) is the cross-linker agent and (c) is the cross-linked PVP.

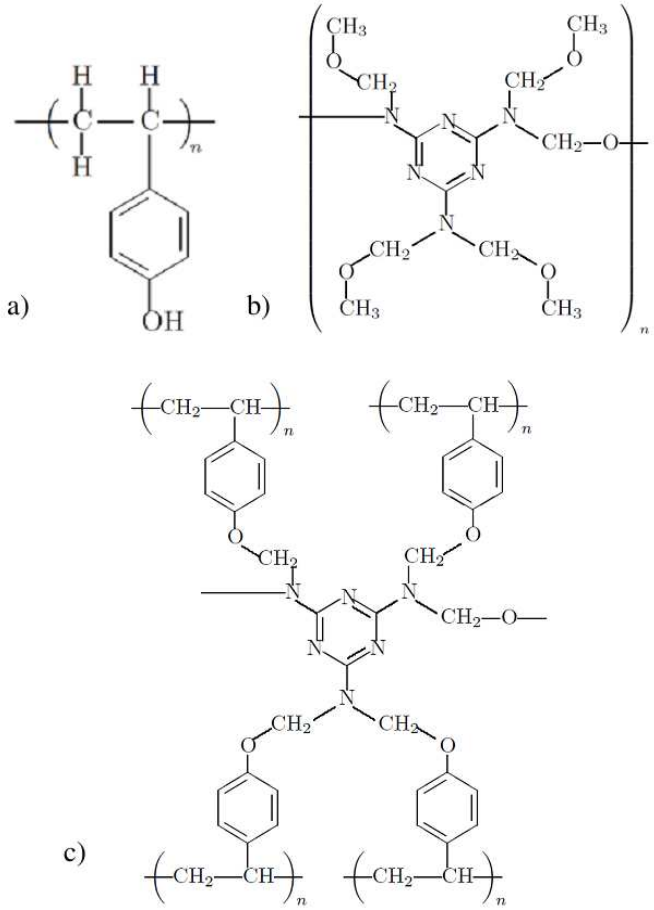

Fig.4.10. Chemical structures of polymeric dielectrics used in this work: (a) pure PVP; (b) cross linker agent; (c) cross-linked PVP.

Lim et al. [21] and Faber et al. [22] report the use of PVP as the polymeric gate dielectrics, and especially they observe the effect of the hydroxyl groups (OH^-) which may lead to a shift in the threshold voltage depending on the direction of the gate-source voltage sweep, corresponding to a hysteretic behaviour in the transfer characteristics. The relative permittivity and the insulator thickness were obtained from Wolff et al. and their values

are ε_r = 5.9 and t_k = 0.18 μm respectively, under the conditions used in the transistor's integration.

4.4.3 Morphological characterization of the organic layer

The most important problems that strongly influence electrical performances of the organic transistors are charge carriers accumulation and transport across the channel, and charge carriers injection into the channel. The first problem is generally correlated to the morphological and structural properties of the deposited organic films.

Organic films are generally characterized by very poor degree of crystallinity, and charge transport is dramatically limited by charge carrier scattering at the grain boundaries. For this issue, it is useful to investigate the topographical properties of the film, showing how it is assembled in a large scale, and the way the molecules are packed and oriented on a very small scale. Charge carrier injection into the channel is correlated to the interfacing between metal electrodes and the organic semiconductor. For these reasons, this section is focussed on the characterizations of the layers used during this thesis to fabricate the OTFTs, in order to correlate structural and morphological properties of the materials to the device performances.

In order to evaluate the effect of the solvent on the morphology and on the crystal structure of a film of TIPS-pentacene, the semiconductor was first dissolved in two different solvents having different boiling points: *chlorobenzene* (CB) and *orthodichlorobenzene* (o-DCB) (respectively 138°C and 198°C), and then deposited by drop casting on a PVP layer (Table 4.1).

	Solvent	***Boiling Point***	***Polarity (dielectric constant)***
Non-polar solvent →	*orthodichlorobenzene o-DCB*	198°C	2.7
	chlorobenzene CB	138°C	5.7

Table 4.1. Characteristics of the solvents used for the TIPS-pentacene.

In order to have information on the crystal growth of the semiconductor on the dielectric, the morphology of the surface of the TIPS-pentacene was observed with a scanning electron microscope (SEM). All SEM images shown in the figure 4.11 are at the same scale.

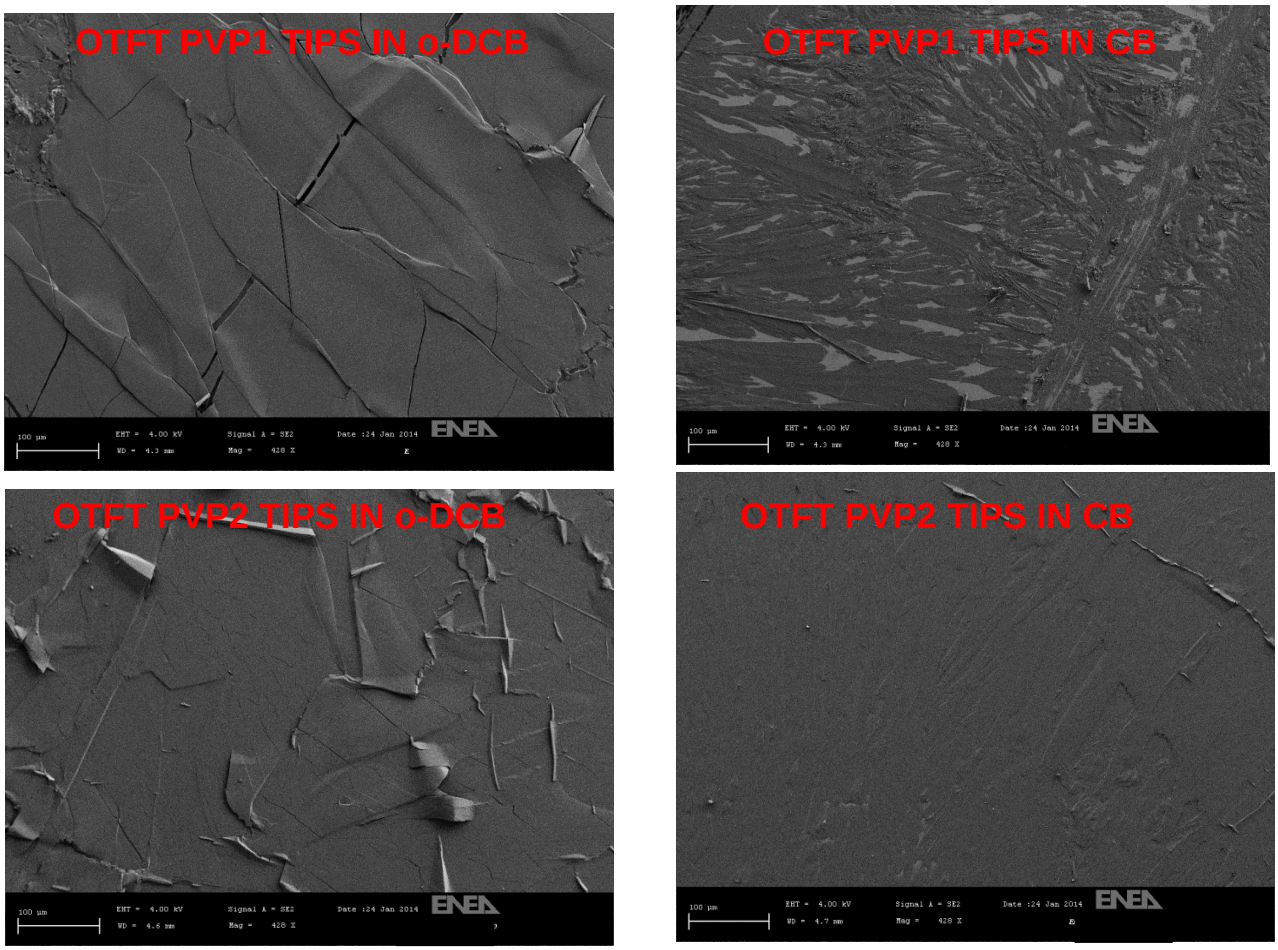

Fig.4.11. SEM images of TIPS-pentacene films prepared for the 4 types of OTFTs used in this thesis.

It is clear that the morphology of the films of TIPS-pentacene is significantly modified by varying the solvent and the underlying dielectric.

From figure 4.11, it is clearly observed that o-DCB gives a semiconductor with larger grains. This phenomenon is due to the slower evaporation rate of the o-DCB solvent, which has a boiling temperature higher than the CB, so giving enough time to the TIPS-pentacene molecules to arrange during drying.

Since the TIPS-pentacene contains 5 benzene rings (segments of conjugated π electrons), it is expected that the "aromaticity" of the solvent has significant effects on the morphology

of the polymer film. In addition to aromaticity, the boiling point of the solvent can affect the morphology and the crystallites of the material.
It is reported that the semiconducting polymers obtained from solvents having high boiling points show a better crystallites compared to films obtained from solution using a solvent with a lower boiling point [24,25].

Laterally grown large crystallites showing remarkable molecular order was seen in drop cast TIPS-pentacene films. In addition, they are consistent with film formation speed. In other words, the solutions from higher boiling point solvents typically produce larger crystals, stronger molecular order and higher mobilities [24,25]. Moreover, the films which form in a solvent ambient show larger crystals and higher mobilities.
The large lateral grains observed in TIPS-pentacene films are a consequence of crystal re-growth from the liquid-phase of the drop casted TIPS-pentacene solution. The re-growth may start from discontinuous small solid seeds, which solidified rapidly in the meniscus region. Therefore, as the solvent begins to evaporate, growth from these seeds proceeds as a function of the distance between them. It is then possible that a significant lateral growth takes place before impingement of the rapidly solidified grains. The limit to maximum lateral growth distance is therefore achieved by the continuous evaporation of the solvent via conduction to the ambient. This mechanism qualitatively explains the observation of a larger grains lateral growth with lower film formation speeds. Solvents with lower evaporation rates provide more time for lateral growth to take place and larger crystals to form.
In the drop cast films deposited for this work, it has been observed that films from chlorobenzene result in lower mobilities than from a o-DCB solution. This was an expected result, from the just recalled literature about the film formation speed, which is related to the boiling point of the solvent affecting the domain size. Typically, it is observed that films with larger domain sizes indicated higher mobility and molecular order. However, charge transport properties such as mobility are not always consistent with the domain size. Moreover, lower mobilities of films from chlorobenzene solutions may derive from the higher dipole momentum of this solvent, which can introduce a higher probability to form defects or traps inside the films, and the degree of defectivity or

the traps amount can be related to the device performances. Therefore, there can be a certain point of mobility saturation region with increasing film formation speed.

These hypotheses were confirmed by XRD analysis shown in Figure 4.12

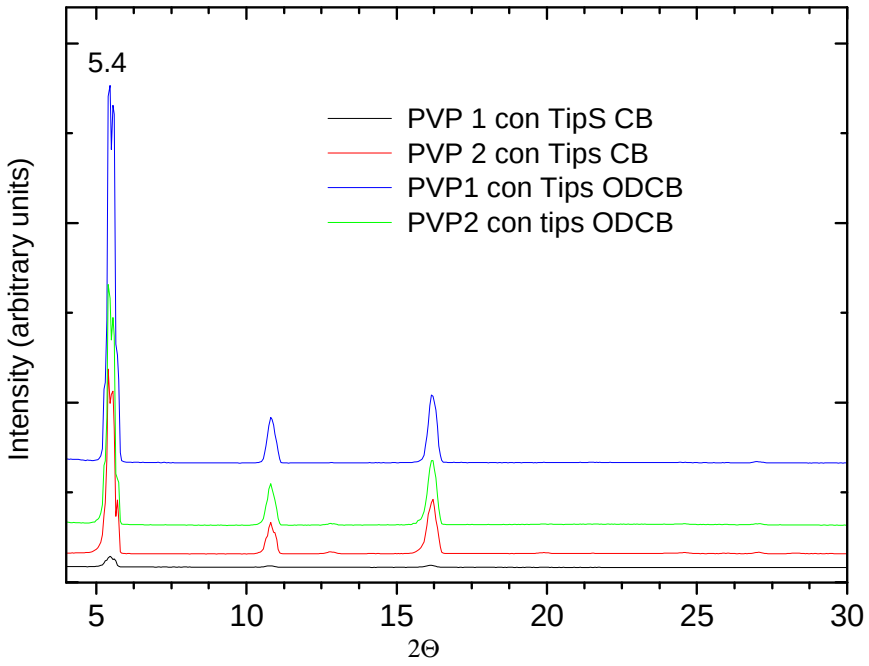

Figure 4.12: X-ray crystallography on the layers tested

The XRD result shows good molecolar ordering for a deposited solution thin film and the same diffraction peaks as bulk crystal TIPS-pentacene. Single crystal TIPS-pentacene has a triclinic structure with unit cell parameters a=7.5650 Å, b=7.7500 Å, c=16.835 Å, a= 89.15°, β= 78.42°, and γ= 83.63 ° [28]. From these parameters, strong, sharp peaks observed at 5.4° indicate a well-organized molecular structure.

As shown in Fig4.12 when comparing films of approximately the same thickness, we found that film TIPS-pentacene prepared with o-DCB is more crystalline.

The surface energy and the morphological roughness of the deposited PVP films have been examined too. SEM images show a good uniformity of the two types of the PVP films (figure 4.13).

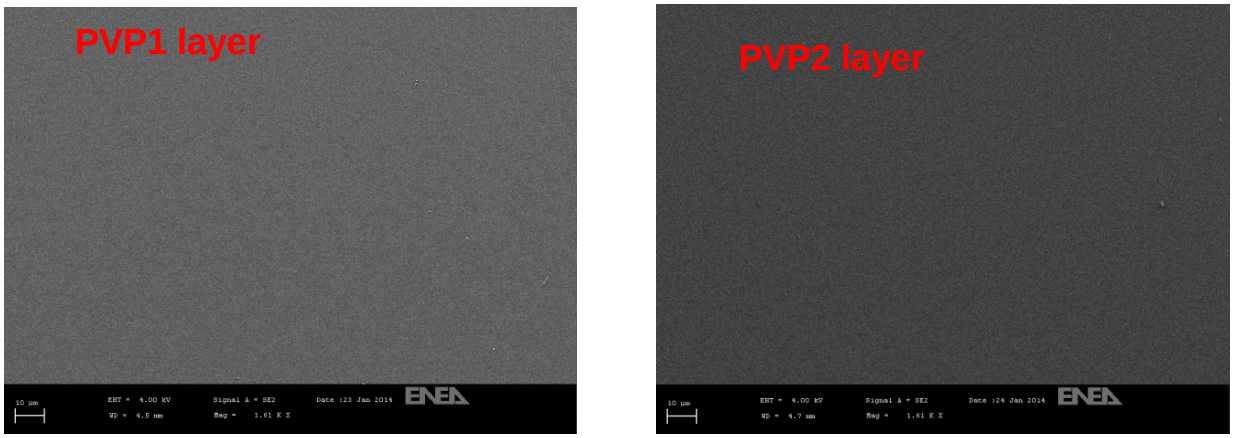

Fig.4.13. SEM images of the two types of the PVP films.

Surface energy has been evaluated through contact angle measurements. When a liquid droplet strikes a substrate, the edge of the drop can be characterised as hydrophilic (wetting) or hydrophobic (dewetting) by the value of the angle θ_0 formed between the tangent at the profile of the droplet and the surface where it has been deposited, angle measured at the point of contact of the droplet with the surface (Figure 4.14) [26]. For example, clean and untreated glass reveals hydrophilic properties, because of unterminated OH groups on the glass surface, which are ready to attach to water molecules through hydrogen bonding.

Contact angle measurements have been done to investigate the surface energies of the two types of the dielectric layers used in this thesis. From Figure 4.14, it has been found that the contact angle on the PVP1 layer is slightly smaller than that on the PVP2 layer.

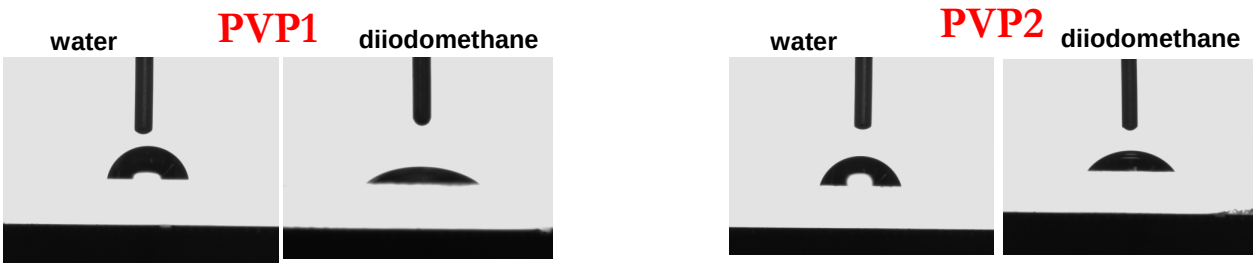

Fig.4.14.Contact angle images of the two types of the PVP films.

The surface free energy (γ_P) of each layer can be calculated using the following equation [27]. The obtained values result comparable between the two recipes (Table 4.2).

$$\gamma_p = \frac{\gamma_W}{4} \times (1 + \cos\theta_0)^2$$

where θ_0 is the contact angle at equilibrium and γ_W is the water surface free energy (73 mJ/m^2). The values of γ_P for PVP1 and PVP2 layers were determined, indicating that the surface of the PVP1 layer is relatively more hydrophilic and polar in comparison to that of the PVP2 layer.

	Surface Energy (mN/m)	**Dispersive Component**	**Polar component**
PVP1	**39.94**	**33.33**	**6.61**
PVP2	**39.51**	**35.52**	**3.99**

Table 4.2. Contact angle parameters for the deposited insulators.

From the FTIR (Fourier Transform Infrared Spectroscopy) spectrum, it can be observed that in both the dielectric layers the same amount of hydroxyl groups is present (figure 4.15). Therefore, the higher polarity in PVP1 is probably due to the massive presence of other electronegative groups.

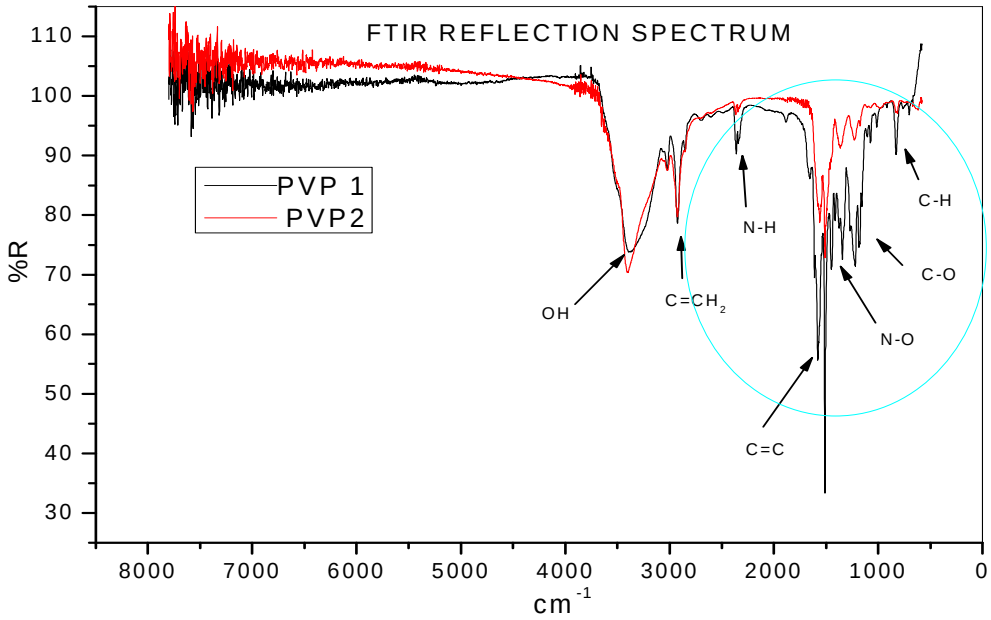

Fig.4.14. Fourier Transform Infrared Spectroscopy (FTIR) spectrum of the two dielectrics films..

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Chapter 5
Stability analysis on OTFTs

In the last years a lot of improvements have been seen in small molecules and solution processed OTFTs, these organic devices still present the important shortcoming of their performances degradation due to several stresses. Wide research efforts have been focused on synthesizing organic materials witch have: environmental and/or operational stability; high mobility and large ION / IOFF ratios, and to improve the OTFTs performances by device engineering and optimizing processing conditions.

In addition to characterize the OTFT mobility and current modulation, the stability of devices must be understood and monitored. Electronic applications and circuits require stability in threshold voltage and subthreshold slope. Environmental considerations such as moisture, illumination and oxygen in the atmosphere are some of the causes of the modification of the electrical performances.

It has been reported [11,12] that ambient H_2O and other polar molecules degrade pentacene TFTs performances, and their interactions form traps at the grain boundaries in the semiconductors, which causes the increasing of the TFT off-current, the lowering of the TFT on-current, and the threshold voltage shift. These kinds of effects may be invert in vacuum. Operational stress has only been investigated as far as showing that continued applied voltage leads to a decrease in the device on-current, that may be recovered by applying a reverse bias [13,14].

Many researches have been concentrated to investigate solutions to these problems. For example, in the OLED displays backplanes, usually a pair of transistor design is used as the switching device. The shift of threshold voltage during devices operation can be compensated with more complicated circuit designs. Another solution to attack this instability is to encapsulate the organic materials to avoid the direct exposure to air or illumination [15].

In this chapter, we report the analysis of the operational stability of the electrical characteristics for TIPS-pentacene based thin-film transistors, prepared using two different solvent for the semiconductor and with poly(4-vinylphenol) (cross linked in two different recipes) as gate insulator, under humidity, light and bias stresses.

5.1 *Devices architecture*

The devices architecture was fixed as Bottom-Gate Bottom-Contacts (BGBC). OTFTs have been prepared on glass substrates, with patterned Indium Tin Oxide (ITO) as gate contact. The gate insulator has been made by cross-linked PVP (poly-4-vinylphenol) (thickness = 1 µm) prepared in two distinct recipes with two different concentrations of crosslinking agent (CLA) deposited by spin-coating from solution (solvent propylene glycol monomethyl ether acetate (PGMEA), curing agent poly (melamine-co-formaldehyde) methylated:

- *PVP 1: PVP (15 wt%)+ 3% CLA in PGMEA*

curing at 150°C for 10 minutes and at 200°C for 20 minutes.

- *PVP 2: PVP (10 wt%)+ 5% CLA in PGMEA*

curing at 100°C for 1 minute and at 200°C for 5 minutes.

The source and drain contacts have been made of Gold (60 nm), deposited by evaporation in vacuum (base pressure 10^{-7} mbar) through a shadow mask. Organic semiconductor 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS-pentacene) has been deposited by drop casting, from two different solutions, with 2% wt respectively in chlorobenzene (CB) or in orthodichlorobenzene (o-DCB), and dried at 60°C for 60 s on a hot plate. No encapsulation has been applied.

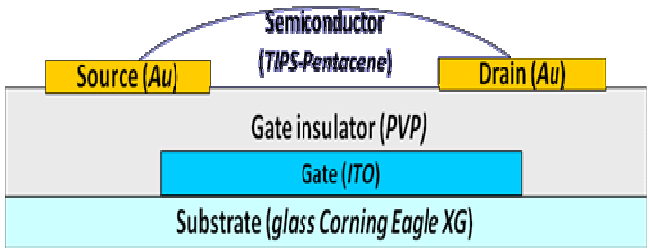


Fig.5.1. OTFT cross section scheme for the applied architecture Bottom-Gate Bottom-Contacts.

5.2 Analysis of the effects of electrical stress on OTFT

In a field-effect transistor, a charge carrier channel is created by applying a gate-source voltage above a certain threshold value. But, it has been observed that the threshold voltage changes over time. This phenomenon is known as bias stress effect. The bias stress effect is attributed to the trapping of carriers from the gate bias-induced conduction channel into localized (i.e., less mobile) electronic states. These trap states may be located within the semiconductor, at the semiconductor/dielectric interface, or in the gate dielectric. The longer the gate bias is applied, the more carriers are trapped, and hence the larger is the shift of the threshold voltage. The trapped charge carriers still contribute to the charge balance in the transistor, but not to the drain current, and this manifests itself as a shift in threshold voltage. As a result, the number of mobile charges and hence the drain current at a given gate-source voltage decrease over time.

In this section, we report the investigation of the bias stress effect on four types of organic field-effect transistors, using TIPS pentacene, dissolved in two different solvents, as semiconductor and poly(4-vinylphenol), cross linked in two different recipes, as gate dielectric.

Electrical instabilities are due to threshold voltage shifts under the applied gate bias, while mobility is stable in vacuum, exhibiting no variation after 24 h stress even under high gate bias stress (V_{GS} = −20 V). The threshold-voltage shifts vs. time can be modeled according to a stretched exponential behavior.

The stability of the organic transistors is influenced by the properties of the organic film and by the environmental condition during the bias stress. We attribute the origin of the charge trapping to residual water related trap sites.

5.2.1 Introduction

Electronics based on organic and polymer materials has gained considerable attention in recent years. The interest in organic electronics can be attributed to the emerging demands in novel display media (active and passive) on low cost and/or flexible substrates. The progress has been caused by distinct improvements of material and device properties [1–2] Organic TFTs are of potential interest for application like backpanels of displays or organic radio frequency identification tags (organic RFID tags). However, the realization of active matrix addressed displays or RFID tags require the fabrication of highly stable TFTs [3,4]. In particular the threshold voltage has to be stable to allow the realization of complex

organic circuitry. Small variations of the threshold voltage might have a significant influence on the operation of displays or organic RFID tags. The change of the threshold voltage is usually caused by bias stress effects.

Device degradation commonly manifests itself as a shift of the threshold voltage, an increase in the sub-threshold slope, a reduction of the field-effect mobility, an increase of the OFF current, and/or increased hysteresis between subsequent measurements of the transfer characteristics with increasing and decreasing gate voltage. In many systems, the dominant degradation observed is a shift of the threshold voltage upon prolonged gate bias stress in the ON and/or OFF state. In most systems, this is caused by trapping of charge carriers in localized states in the organic semiconductor, in the gate dielectric, or at the interface between the two layers. In many cases, the microscopic, molecular-level nature of these defects whether they are related to intrinsic structural defects or extrinsic chemical impurities or a combination thereof is not well understood.

The instabilities of the threshold voltage and of the mobility for TIPS-pentacene thin film transistors using a poly(4-vinylphenol) (PVP) gate dielectric have been investigated under constant bias stress.

The behavior of the threshold voltage in four different OTFTs has been evaluated. The devices have the same structure and materials already discussed in the chapter 4 (figure 5.1):

In order to obtain insight into the stress behavior of these devices, two series of measurements have been performed.

In the first experiment, voltages V_{GS} = −20 V and V_{DS} = 0 V have been applied to the OTFTs as the constant bias stress for 600 s. The stress has been carried out in vacuum as well as in air (room temperature), in order to elucidate the intrinsic properties from the air effects.

In the second experiment, measurements have been carried out in dark conditions in vacuum, and the stress effect has been measured as a function of time.

We observed the trends of the threshold voltages over time for the 4 types of transistors. The devices were subject to gate bias stress in vacuum (V_G = -20 V) for more than 24 hours,

during which the gate voltage stress was periodically stopped and the trans characteristics measured and threshold voltages evaluated.

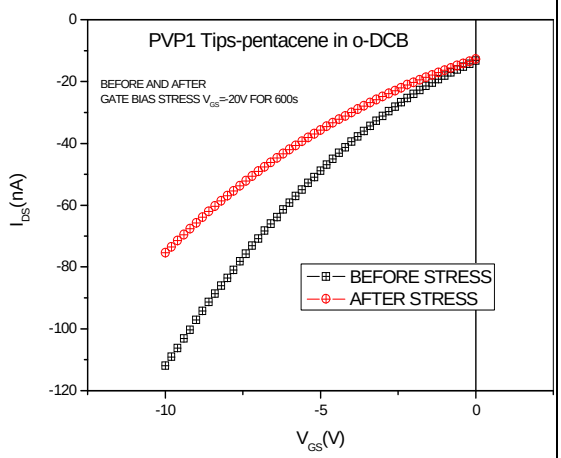
We observe a negative shift of the threshold voltage after the stress in vacuum, and a positive shift after the stress in air. We attribute these shifts to charges trapped in deep electronic states in TIPS-pentacene near the gate interface.

5.2.2 Experimental and discussions

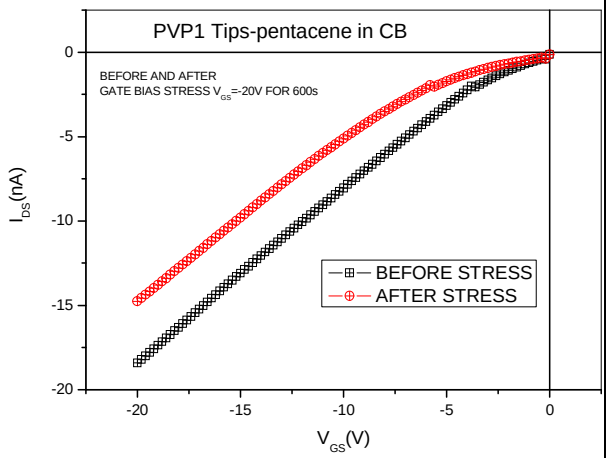
- ***First experiment***

The electrical stress has been performed keeping the devices in static polarization (V_{GS} = -20 V, V_{DS} = 0 V) for 600 seconds. This measurement has been made on all the devices in air and in vacuum condition. In Figure 5.2 the trans characteristics of the four types of devices, before and after the electrical stress, measured in vacuum or in air, are shown.

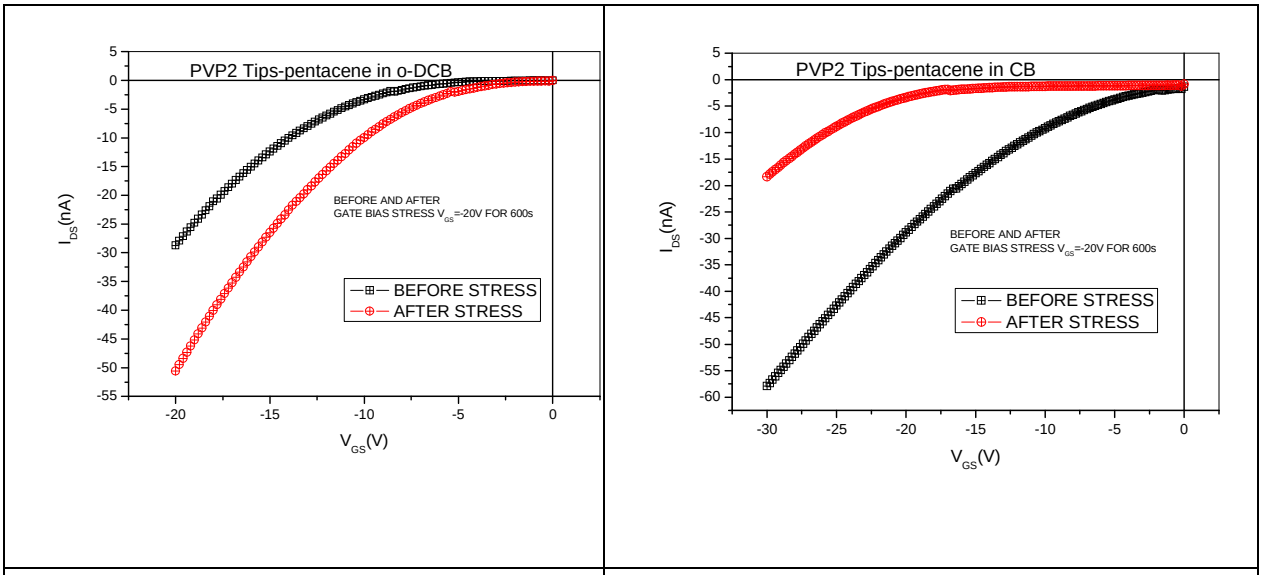
(A) IN VACUUM



PVP1, TIPS-pentacene in o-DCB



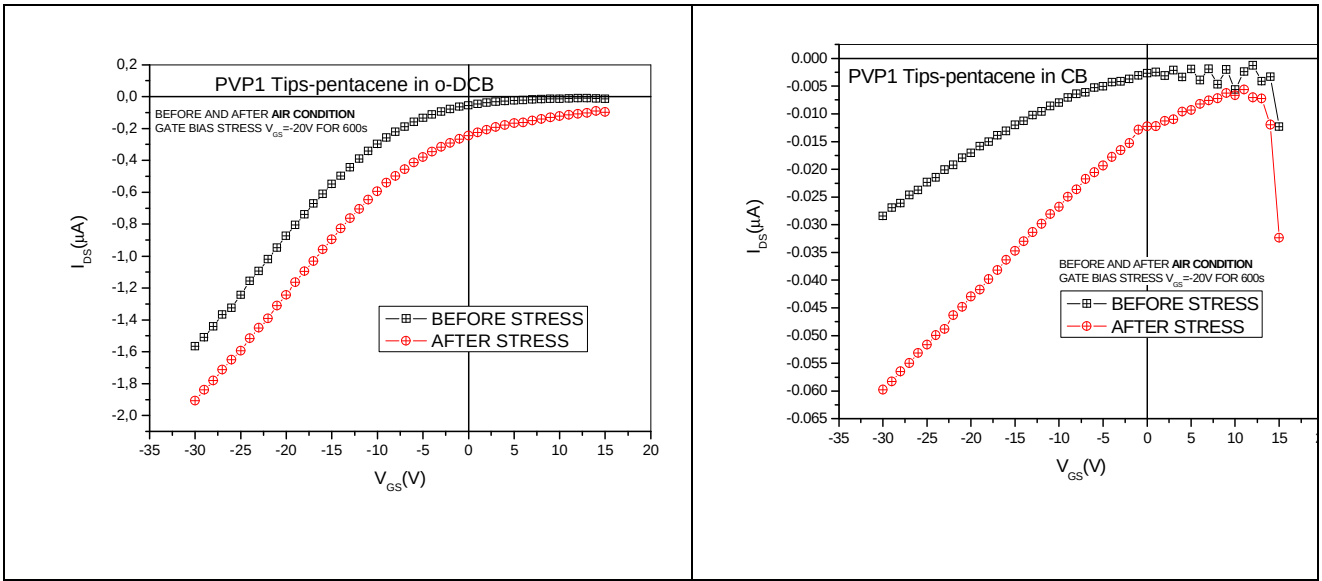
PVP1, TIPS-pentacene in CB



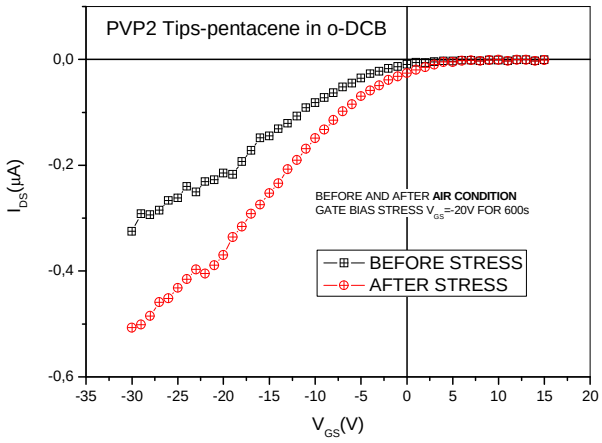
PVP2, TIPS-pentacene in o-DCB	PVP2, TIPS-pentacene in CB

Fig.5.2(A). Comparison of the trans characteristics of the four types of OTFTs before and after the gate stress in vacuum (V_{GS} = -20 V for 600s).

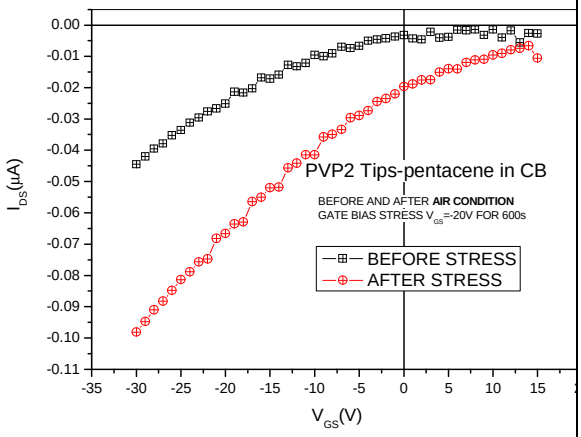
(B) IN AIR



PVP1, TIPS-pentacene in o-DCB	*PVP1, TIPS-pentacene in CB*



PVP2, TIPS-pentacene in o-DCB



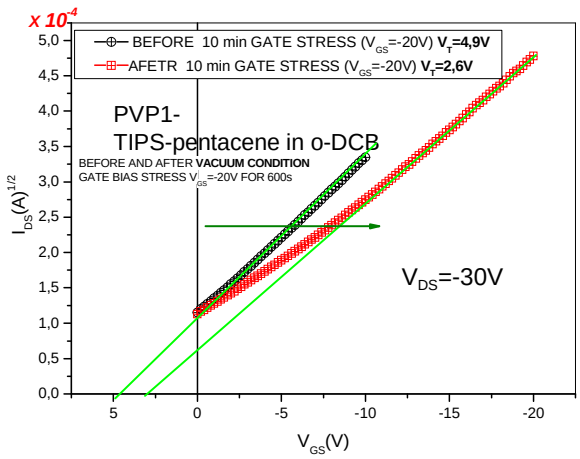
PVP2, TIPS-pentacene in CB

Fig.5.2(B). Comparison of the trans characteristics of the four types of OTFTs before and after the gate stress in air (V_{GS} = -20 V for 600s).

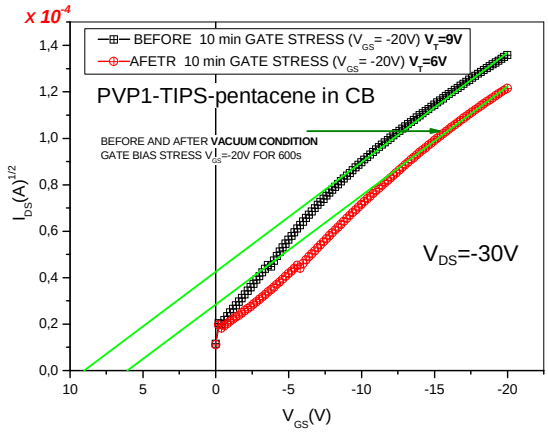
As shown in Figure 5.2, the trans characteristics curves vary with different behavior depending on the environment and on the nature of the solvent used to deposit the semiconductor. The slope of the curves, when the devices are expose to air, changes, implying a variation of the mobility. This variation in air seems to be attributed to water vapor, which produces hydroxyl radicals in the grain boundaries of the TIPS-pentacene [4]. This is supported by finding that the mobility is stable both in vacuum and in air when OTFTs are protected from air via encapsulation, as noted in [5]. In the devices fabricated in this thesis, in vacuum, the mobility was very stable and exhibited no large variations even after 24 h stress (this will be shown in the second experiment).

The variations of the threshold voltages after the electrical stress are shown in Figure 5.3.

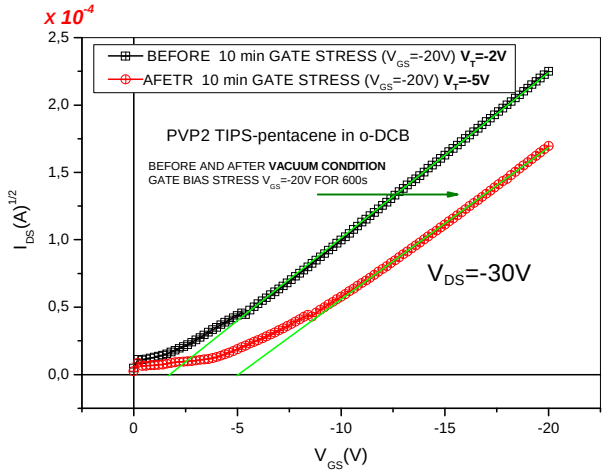
(A) IN VACUUM



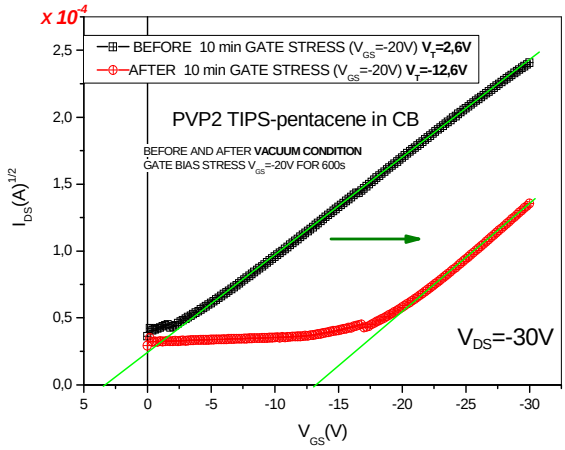
PVP1, TIPS-pentacene in o-DCB



PVP1, TIPS-pentacene in CB



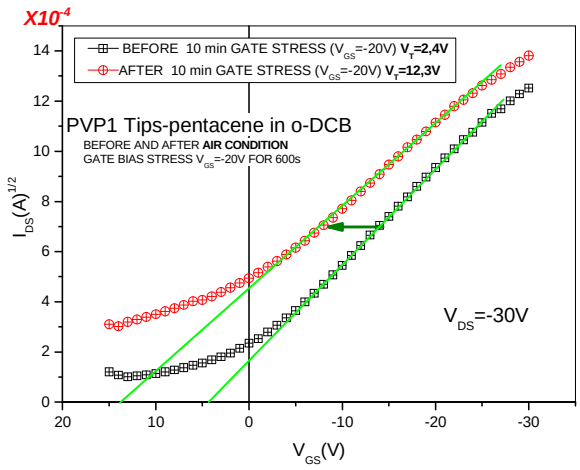
PVP2, TIPS-pentacene in o-DCB



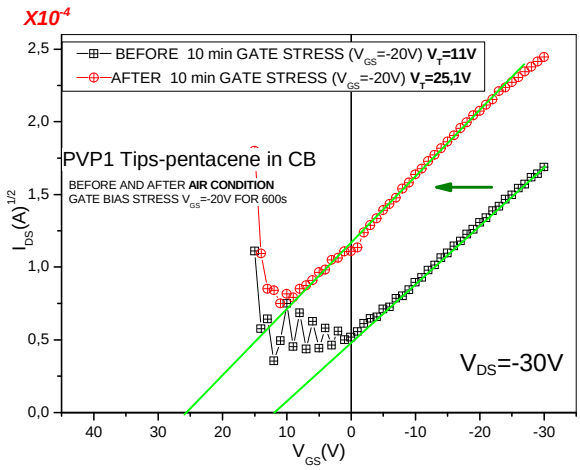
PVP2, TIPS-pentacene in CB

Fig.5.3(A). Comparison of the square root of the trans characteristics and evaluation of the threshold voltages of the four types of OTFTs before and after the gate stress in vacuum.

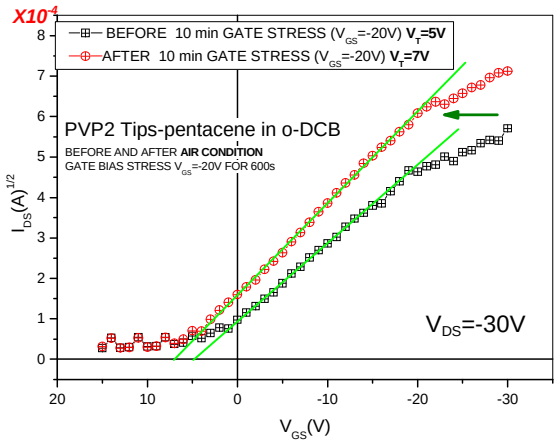
(B)IN AIR



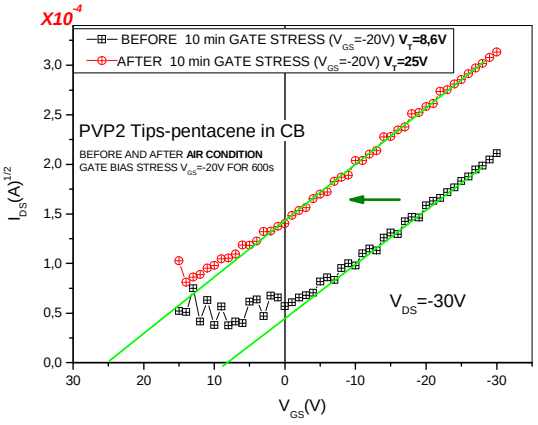
PVP1, TIPS-pentacene in o-DCB



PVP1, TIPS-pentacene in CB



PVP2, TIPS-pentacene in o-DCB



PVP2, TIPS-pentacene in CB

Fig.5.3(B). Comparison of the square root of the trans characteristics and evaluation of the threshold voltages of the four types of OTFTs before and after the gate stress in air.

A

In AIR	*PVP2 o-DCB*	*PVP2 o-DCB*	*PVP2 CB*	*PVP2 CB*	*PVP1 o-DCB*	*PVP1 o-DCB*	*PVP1 CB*	*PVP1 CB*
/	*μ (cm^2/Vs)*	*V_T (V)*	*μ (cm^2/Vs)*	*V_T (V)*	*μ (cm^2/Vs)*	*V_T (V)*	*μ (cm^2/Vs)*	*V_T (V)*
BEFORE STRESS	4,78E-02	4,63	3,60E-03	9,06	3,82E-01	4,39	3,60E-03	9,06
AFTER STRESS	7,13E-02	6,14	3,83E-03	26,53	2,90E-01	13,29	3,83E-03	26,53

B

In VACUUM	*PVP2 o-DCB*	*PVP2 o-DCB*	*PVP2 CB*	*PVP2 CB*	*PVP1 o-DCB*	*PVP1 o-DCB*	*PVP1 CB*	*PVP1 CB*
/	*μ (cm^2/Vs)*	*V_T (V)*	*μ (cm^2/Vs)*	*V_T (V)*	*μ (cm^2/Vs)*	*V_T (V)*	*μ (cm^2/Vs)*	*V_T (V)*
BEFORE STRESS	4,82E-03	-1,915	8,20E-03	8.52	5,39E-02	4,744	1,60E-02	6,049
AFTER STRESS	4,16E-03	-5,376	1,00E-02	-13,3	4,39E-02	3,3	1,80E-02	2,112

Table 5.1.The characteristic parameters of the four devices before and after gate stress (A) in air and (B) in vacuum.

The OTFTs exhibited a negative shift of threshold voltage in vacuum and a positive shift in air. In Figure 5.3 the threshold voltages of OTFTs are presented before and after bias stress.

The positive shift of the threshold voltage in air can be explained by the polar nature of hydroxyl group induced by water vapors absorbed into the PVP and aligned by the applied electric field, thus exposing the negative charges to channel direction. This attracts holes into the channel, resulting in the positive shift of V_T.

Numerical simulations of the electrical transistor characteristic indicate that the shift of the onset of the drain current is caused by acceptor-like states deep in the bandgap [6,7,8,9].

The acceptor-like states are supposed to be created by oxygen or OH^- molecules that are incorporated in the organic film [10,11].

In air, after 600 s negative bias stress, the positive threshold shifts observed, mean that V_T moves in the direction opposite to that of the applied gate bias. Assuming that the effect of the electrical stress is the same, both in vacuum and in air, in this latter case occurs the overlap of an additional cause of instability which identify water absorption of the material, the effect of which leads to an increase of the current channel and to a positive shift of the threshold voltage. The stability of organic transistors is influenced by the structural properties of the organic film It is possible to note that, both in air and in vacuum, the devices in CB most suffer the effects of the stress, giving one more marked shift of the threshold voltage. TIPS-pentacene films with increased structural order are less susceptible to bias stress and environmental influences, thus in the devices with tips in CB a higher amorphous phase is reflected in a greater tendency to populate traps due to external stimuli (see Chapter 4, section 4.4.3).

A possible explanation for the observed positive threshold shift upon negative gate bias stress can be found in a paper by Young and Gill [12] on polycrystalline Si TFTs formed with oxides insulator. These porous oxides (which contain a significant amount of water) bear more resemblance to an organic insulator than the thermally grown SiO_2 layers used in previous studies on organic hybrids. Young and Gill observed positive threshold shifts arising from negative ions which were moving in the gate field [12]. As the negative ions drift towards the interface to the semiconductor, positive countercharges (holes) accumulate on the semiconductor side of the interface to the insulator. This manifests itself electrically in a positive shift of the threshold voltage. Because the ionic effect vanished after annealing the device to 250°C, Young and Gill concluded that water absorption in the insulator may be its origin.

To eliminate possible water effects, stress measurements were carried out in vacuum. Under these conditions, no positive shift was observed, as is depicted in Fig. 2(c). ΔV_T is purely negative and manifests the charge trapping.

These observations demonstrate that water is a necessary prerequisite for positive threshold instabilities.

An important question, however, remains. It is not clear whether the water provides the mobile ions itself (H^+ and OH^-), or a water network is formed in the insulator, or water generates high-mobility paths for already present ionic impurities [13]. These ions may arise from residual ions in the insulator or from doping ions migrating from the electrodes.

It was considered that the ambient water might be absorbed physically and chemically into the pentacene films. Namely, the physically absorbed water, which exists between tips pentacene grains, is increased with exposure time and degrades the OTFT performance with increasing the absorbed contents [14,15]. This behavior may be used as humidity sensors [14]. On the other hand, the chemically absorbed water interacts with tips pentacene to form TIPS-pentacene/(H_2O)n clusters. Due to weakly bound charge transfer (p-doping) in the clusters, I_D^{Sat} can be enhanced. However, some clusters in the vacuum are unstable and dissociated. As a result, the I_D^{Sat} is decreased when pumped down to vacuum. Latter phenomenon is also observed in the devices tested, showing the possible formation of clusters H_2O and tips pentacene mentioned above.

- ***Second experiment***

Stability of the transistor operation is essential for the realization of organic integrated circuits. In particular variations of the threshold voltage have a distinct influence on the operation of OLED displays or organic radio frequency identification tags (RFID). Major sources of instabilities are bias stress effects, which leads to a change of the threshold voltage over time. Such effects are well known for inorganic and organic TFTs prepared at low temperatures.

The threshold voltage shift for amorphous and polycrystalline silicon TFTs has been extensively investigated [16,17]. The effect can arise from slow trapping in the dielectric and/or surface states at the semiconductor/dielectric interface, or defect creation in the semiconductor.

Bias stress effects are closely related to the electronic structure of the organic films. The electronic structure is again related to impurities in the film, which are affected by environmental conditions. Therefore, It has been shown that environmental conditions have a strong effect on the stability of organic thin film transistors. To avoid the influence

of environmental conditions on the device behavior the bias stress experiments were carried out under vacuum conditions

This work provides a quantitative study of the gate-bias stress instability on four type of OTFTs.

Stress was measured as a function of time, the applied gate was -20 V, between source and drain has been applied 0 V and the transfer curves were measured in the saturation region.

The gate-bias induced stress does not affect significantly the μ_{FE}, which is readily confirmed by the observation that the transfer curves shift in a parallel way.

In figure 5.4 is shown square root of the trans characteristic in saturation region over time relative to a device with PVP2 as dielectric and tips pentacene dissolved in o-DCB this picture is used as an example of the trend of measurements over time, made on all devices.

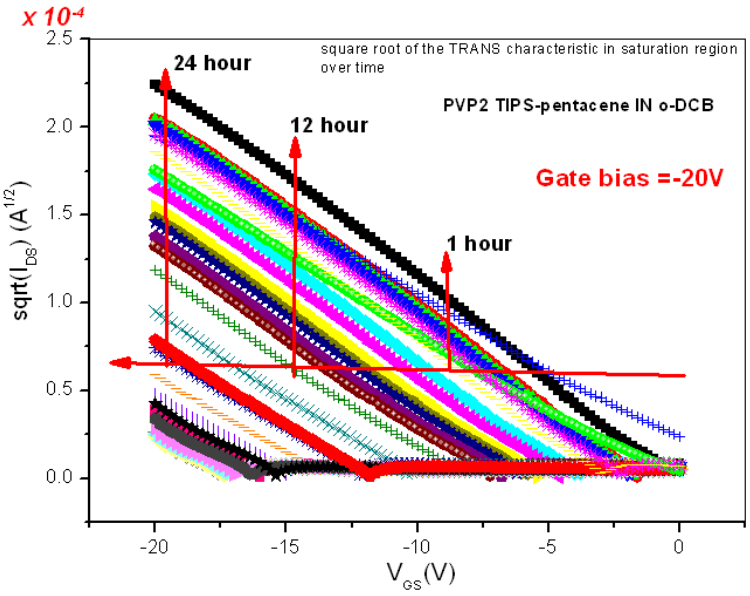


Figure 5.4:Square root of the trans characteristic in saturation region over time.

For quantitative assessment of threshold-voltage shifts, a number of models have been developed and used extensively for describing the threshold-voltage instabilities in a-Si TFTs [18]. The cause of threshold-voltage shifts under prolonged operation in ON condition is of course that some of the mobile charge carriers in the channel become trapped in pre-existing or stress-generated deep localized states in the semiconductor, in the gate dielectric, or at the active interface. Once trapped, they no longer contribute to the

current such that a high applied gate voltage is needed to achieve the same mobile-carrier concentration and current. In a-Si TFTs, charge trapping is due to creation of dangling-bond defects under electron accumulation conditions, and the rate for defect creation is limited by the diffusion of hydrogen, which is involved in the process to stabilize the broken Si-Si bond [19]. Hydrogen diffusion is dispersive ina-Si, and the diffusion coefficient D in a system with an exponential distribution of trap energies (with a characteristic energy k_BT_0) is time-dependent, and can be shown to have a power-law time dependence, $D(t)= D_{00}(\omega t)^{\beta-1}$, where D_{00} is the microscopic diffusion coefficient, ω is the attempt frequency for diffusion, and the exponent $\beta = T/T_0$. This leads to a rate equation for the creation of defect states of the form:

$$\frac{d\Delta N_t}{dt} = -AD(t)\Delta N_t(t) = -AD_{00}(\omega t)^{\beta-1}\Delta N_t(t) \qquad (1)$$

where ΔNt(t) is the difference between the actual concentration of defects at time t and the equilibrium concentration for a particular electron concentration. A is a constant. The solution to this differential equation is given by a stretched exponential function.

$$\Delta N_t(t) = \Delta N_t(0)\exp\left(-\frac{t}{\tau}\right)^{\beta}$$

with

$$\tau = \omega^{-1}\exp\left(\frac{E_\tau}{k_B T}\right) \qquad E_\tau = k_B T_0 \ln\left(\frac{\omega\beta}{AD_{00}}\right)$$

τ represents the characteristic trapping time of carriers where the thermal activation energy is given by $Ea = E_\tau \beta$ (in which β is the stretched-exponential exponent and E_τ is the average effective energy barrier that electrons in the TFT channel need to overcome before they can enter the insulator), and ω^{-1} is the thermal prefactor for emission over the barrier.

The threshold-voltage shift is proportional to the concentration of defects from
$\Delta N_t = C_{ox}\,\Delta V_T / e$, where C_{ox} is the capacitance per unit area of the dielectric layer, and then

$$\Delta V_T(t) = (V_T(t=\infty) - V_T(t=0))\left(1 - \exp\left(-\frac{t}{\tau}\right)^{\beta}\right) \quad (2)$$

The rate at which the charges are trapped depends on the free carrier concentration Nt.
Of course, in an organic semiconductor, the rate of charge trapping in deep states is not likely to be limited by the same process of hydrogen diffusion. We have reproduced the argument for a-Si here to illustrate the generality of the stretched exponential behavior.
The result of this distribution of time constants is a faster-than-exponential response early in the process (for times up to the time constant τ) and a slower than exponential response later in the process (for times beyond the time constant τ), i.e. a stretched exponential function [20].
There are two apparent causes of a negative shift in the threshold voltage: charge trapping at localized-states inside the gate insulator [19–21] and charge trapping in deep electronic states of the semiconductor near an interface [22].
Therefore, the negative shift of the threshold voltage can be rationalized as follows. Holes are accumulated in channels as a result of prolonged application of the negative stress gate voltage. These holes are then trapped in deep electronic states [23] generated by defect TIPS-pentacene molecules located within the semiconductor near the dielectric interface and/or the trap states at grain boundaries near interface [24,25,26] as shown in Fig. 5.5. The trapped holes screen the gate field, which in turn cause the negative shift of the threshold voltage. The trapping rate is gradually reduced with time because the vacant states are decreased as the trapped holes are increased with time

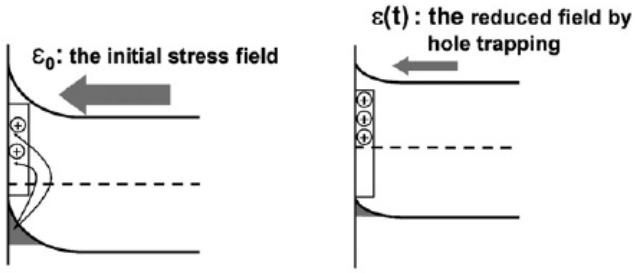


Figure 5.5*:The schematic model of threshold voltage shift; the holes in channel are trapped in deep electronic states as the stress time elapses, and then the gate field is reduced by the trapped charges, resulting in threshold voltage shift to negative direction.*

In the figure 5.6 it is shown the trend of the threshold voltage over time in semilogarithmic scale for the four types of the devices analyzed.

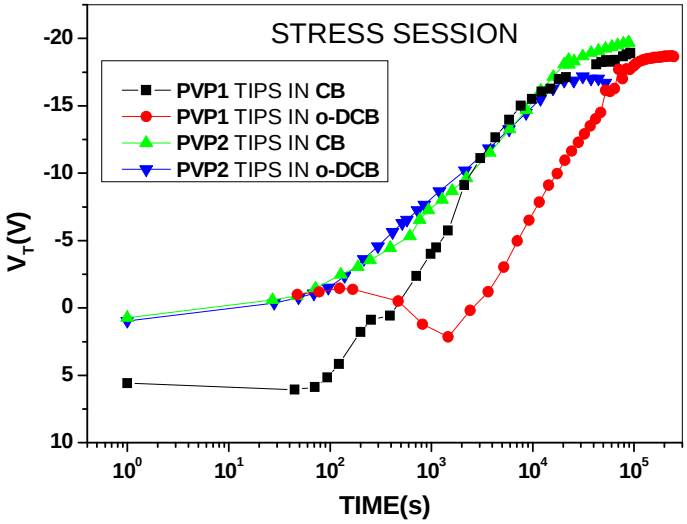
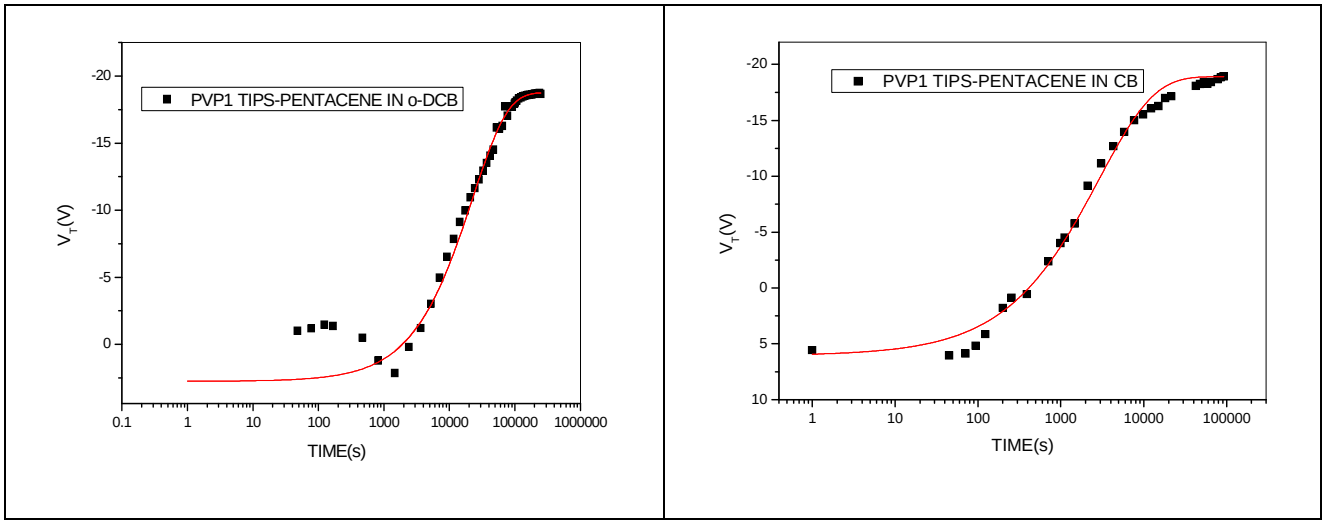


***Figure 5.6**:V_T as function of time on a logarithmic scale.*

In figure 5.7 the continuous curves are the fits with stretched-exponential time dependence. In Table 5.2 the values of the fit parameters are reported.



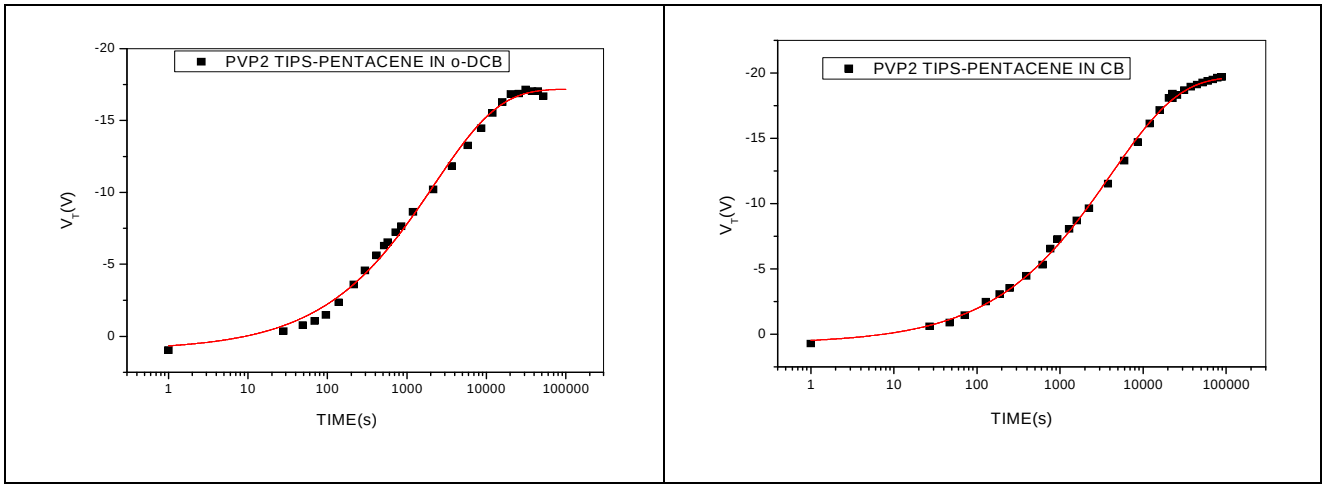


Figure 5.7. *V_{th} as function of time on a logarithmic scale and the stretched-exponential fit of each measurement.*

device	β	τ *(s)*
PVP1 TIPS pentacene in CB	0,66 ± 0,02	(2,90 ± 0,09) x10^{+3}
PVP1 TIPS pentacene in o-DCB	0,81 ± 0,05	(2,30 ± 0,9) x10^{+4}
PVP2 TIPS pentacene in CB	0,53 ± 0,04	(2,20 ± 0,08) x10^{+3}
PVP2 TIPS pentacene in o-DCB	0,53 ± 0,01	(4,08 ± 0,09) x10^{+3}

Table 5.2. Values of the stretched-exponential parameters for the fits infigure 5.7.

Also in this type of analysis it is observed that the devices with TIPS-pentacene dissolved in o-DCB are more stable compared to devices with TIPS-pentacene dissolved in CB. It is observed that the trapping time of the devices in o-DCB is longer than the other, thus indicating that these devices are more stable and thus also confirming the results reported in the first experiment.

5.2.3 Conclusion

The stability of the devices is a very important requirement for the application of organic thin film transistors. In particular the stability of the threshold voltage is of major importance for the realization of organic integrated circuits. In general the change of the threshold voltage due to bias stress is caused by charge trapping or recharging of defect states in the dielectric, trapping and slow release of carriers in existing deep states in the

semiconductor (bulk or interface), or a reversible structural change in the semiconductor that creates new traps.

The influence of environmental conditions on the device operation and the stability of four type of tips pentacene thin film transistors (OTFTs) were investigated. electrical instabilities are due to threshold voltage shift under applied gate bias. The threshold voltage was shifted to the negative or positive direction of gate voltage depending on stress environment. the OTFTs produces a positive shift in air and negative shift in vacuum. The positive shift was attributed to water or hydroxyl group absorbed in the organic materials.

The extended bias in vacuum shows a threshold voltage shift whit time according to a stretched exponential. The measured stress effects, depend on the structural properties of the organic transistors. It was found that the devices having larger grains (devices with tips-petacene dissolved in o-DCB) show less instability to external stimuli with smaller variations of the threshold voltage and longer trapping times.

5.3 Analysis of the effects of environmental stress on OTFTs

In this paragraph we report the effects of ambient moisture on the electrical characteristics of the prepared OTFTs. The measurements were carried out keeping the devices in absence of oxygen (a constant flow of pure nitrogen).

An increase of mobility is observed at increasing percentage of the moisture. The mobility recoveres if the devices are held at low percentages of moisture for relatively long time.

Furthermore, the threshold voltage shifts toward the positive direction after exposure to 30% and 60% moisture. These characteristic degradations under the influence of the moisture can be explained by charge-trapping of absorbed H_2O molecules at the TIPS-pentacene/PVP interface and in dielectric layer.

5.3.1 Introduction

In recent years organic semiconductors (OSs) attracted much attention in the field of organic electronics. The main attributes of organic semiconductors are low temperature processing, mechanical flexibility and applicability for large area devices fabrication [27,

28, 29]. However, when exposed to ambient air, the electrical and in some cases morphological stability of the organic devices is affected [30, 31, 32]. While in some cases degradation of device performance in ambient air is problematic, since the life-spent of devices is affected, sensitivity to air and light gases could be exploited for fabrication of sensors based on organic semiconductors. In either case, understanding influence of air gases, to the performance of that kind of devices, is the key issue.
Furthermore, also the gate insulators play an important role in the operational stability of OTFTs. On this account, the electrical and environmental stability issues in OTFTs are required to be interpreted by the nature of gate insulating materials.

5.3.2 Experimental

This work reports the experimental results for the humidity dependent properties of organic field effect transistors made with the structure presented in figure 5.1.
In order to investigate the effects of ambient moisture on the electrical stability of devices, transistor characteristics were measured varying the relative humidity (RH). The OTFTs current (I_{ds}) versus voltage characteristics were measured using a Keithley 2636A source meter.
All measurements has been carried out in an environmental test chamber, able to control the relative humidity. A constant flow of pure nitrogen was maintained during all the measurements, to keep the content of oxygen as low as possible in the chamber. Devices have never left the test chamber during all the measurements.
For the first step of the measurements, each device was held for 15 min in 10% of moisture. Measurements were carried out evaluating mobility and threshold voltage of device placed for 15 min at 10%, 30% and then at 60% of humidity environment.
After the measurement to 30% and 60% the device was always brought back at RH = 10% and kept in this condition for 15 min, at the end of which it was characterized.

5.3.3 *Results*

When all type of TIPS-pentacene based OTFTs are exposed to air, the same mechanism involving the presence of oxygen and humidity are influencing the charge transport in OTFTs . According to [33], absorbed oxygen, enhances the conductance in active layer by introducing holes near the valence band [33]. In addition, Vollmer *et al:* [34] showed that the semiconductor /electrode hole injection barrier is affected and is lowered for 0.25 eV upon exposition to oxygen, which should substantially decrease the contact resistance at the source/metal interface, and therefore improve the charge carrier injection from the source contact to the semiconductor layer. In order to avoid such effects, the ours measurements were carried out in inert atmosphere.

The effect of the increase of moisture is reflected in a modification of level of current and then in a variation of threshold voltage. This process becomes quite reversible if the device is held for enough time in the condition of low humidity (figure 5.8).

In Figure 5.8 the trends of mobility and threshold voltage are summarized for the four types of devices as function of the time of permanence in the state of the environment.

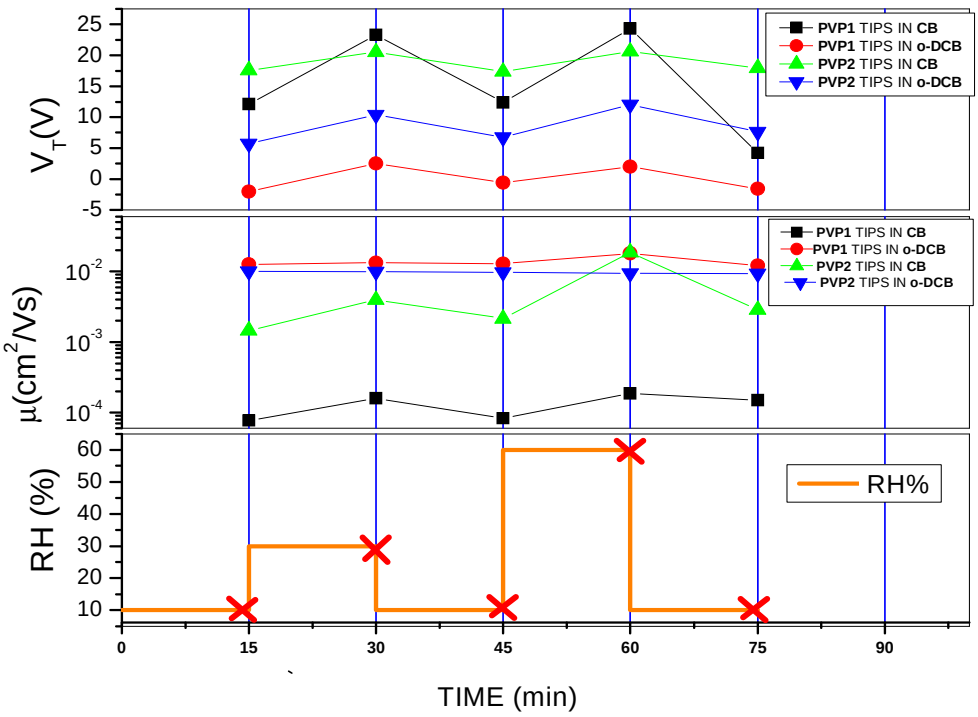


Figure 5.8:Trends of mobility and threshold voltage for the four types of device as functions of the time of permanence in the state of the environment.

Red "X" in the plot of RH marks the time of each measurement.

The threshold voltage depends on the amount of trapped charges in the channel, from this type of measures it can be observed that all the devices show shift in threshold voltage when exposed to moisture. The devices having the semiconductor dissolved in orthodichlorobenzene, show the highest mobility and lower threshold voltages. OTFTs with the TIPS in o-DCB demonstrate to have less traps, and therefore require lower gate voltages to switch to the on state.

Furthermore, the higher mobility and the stability of values over time of the devices with tips pentacene dissolved in o-DCB, is expected from estimated grain dimension (see Chapter 4, section 4.4.3).

Films derived from tips pentacene in CB have a higher amount of grain boundaries, this allows water to more easily reach the semiconductor/dielectric interface causing increased polarizability of the dielectric, this causes, in turn, an apparent increase of the mobility (μ_{FET}) at high values of RH% not attributable to the charge transport, but an increased value of gate dielectric specific capacity as in [36].

The dielectric PVP2, makes the behavior of the devices with humidity, approx independent of solvent used for semiconductor, the difference is observed, mainly on the magnitude of the threshold voltage that the device having the tips pentacene in dissolved o-DCB is lower.

It can be noticed that the device with PVP1 and tips pentacene dissolved in CB is the most sensitive to changes in humidity environment.

The tendency of the threshold voltage shift towards the positive values after exposure to ambient air was recently reported by Kumaki et al: [35]. They associate observed shift in V_T towards positive values to the accumulation of the holes inside the channel, which was observed even for $V_G > 0$ V.

The presence of accumulated holes was attributed to the influence of trap sites formed at the insulator/semiconductor interface and at the grain boundaries. The traps were generated by the chemical reactions between the water molecules and the dielectric surface. The positive shift of the threshold voltage in air can be explained by the polar

nature of water vapors. Water vapours were absorbed into the PVP gate and aligned by the applied electric field exposing the negative charges to channel direction. This then attracts holes into the channel, resulting in the positive shift. A similar result has been reported in conjunction with solution-processed pentacene TFTs using an organic gate such as a photoresist [37.]. Meanwhile, a positive shift has not been reported to date for an SiO2 gate. Thus, the positive shift of the threshold voltage is believed to be associated with the organic gates, which display relatively high absorption of water vapours.

5.3.4 Conclusion

We investigated the influence of four type of tips pentacene-based OTFTs exposure to controlled RH% without oxygen.

Our measurements demonstrate that exposure of OTFTs to humidity for extended periods of time, results in a mechanism that is responsible for observed variation in mobility and threshold voltage. The observed effects are closely related to the amount of grain boundaries of the film of semiconductor, in turn dependent on the conditions process used for the realization of the device. We observed a deterioration of the threshold voltage in correspondence of an increase of% RH, while the mobility increases only in the case of devices having Tips pentacene dissolved in CB which has lower crystallinity. It is noted, also, that the effects of instability due to the presence of moisture, are quite reversible. In fact, the measures show that once soon as the conditions of low humidity (10% RH), the characteristics regain, roughly, the parameters obtained in the first measurements made at low humidity. This type of effect is common to all four types of TFT analyzed, the main differences are marked in devices with tips pentacene dissolved in orthodiclorobenzene which show greater stability to environmental changes (in addition to better performance).

5.4 Analysis of the effects of light and bias stress on OTFTs

In this section, we present the behaviors observed in Organic Thin-Film Transistors fabricated using different solvents for the semiconductor (6,13-bis(triisopropyl-silylethynyl) pentacene) and different recipes for cross-linking dielectric (Poly(vinylpyrrolidinone)) when subjected to electrical bias stress and illumination. The measurements indicate the presence of two distinct trapping

phenomena. Appreciable hole trapping can be achieved using negative bias stresses for a limited time (10 min). Exposure of the devices to the light neutralizes defects under positive gate biases, having as a result a shift of the threshold voltages towards positive values. The devices made using two different recipes for cross-linking PVP used as dielectric, and the semiconductor with the different solvents show distinctive stabilities under the stresses, with different extents for the variations of the threshold voltages and an evident difference in the time dynamics of these variations.

5.4.1 Introduction

Solution processed Organic Thin Film Transistors (OTFTs) are recognized to be a key device for efficient and cheap Flexible Organic Large Area Electronics (FOLAE) circuits and systems. Affordable applications of these devices demand very good stability. Unfortunately, many issues are still affecting OTFTs, such as the sensitivity to external environment factors (temperature, humidity, light) [38,39], and result in poor stability and shorter lifetime if compared to silicon TFTs.

The properties of the organic materials strongly depend on their morphology. This one largely derives from the processing conditions and influences the behaviour of the interfaces between the materials, which are very relevant in the device's performances and stability [40].

In this work, the effects of the electrical stress and of the light on the performances of OTFTs, fabricated using different solvents for the semiconductor and different recipes for cross-linking dielectric with a fixed architecture, have been studied, in order to investigate the influence of a technological parameter on the stability of the OTFTs.

5.4.2 Experimental

For a much more accurate investigation on the role of light and bias, we performed a 4-phases experimental procedure, as shown in Fig. 5.9. At the end of each phase, the transfer characteristic of the devices has been measured and the shift of the threshold voltage evaluated. In particular, we applied to the OTFTs a 600 s gate stress, with source and drain grounded (stress phase). The gate voltage during the stress phase was -20 V (negative

stress). The stress phase was performed in dark conditions in low vacuum and at room temperature. After the stress, the device has been subjected to a first recovery phase, by applying a positive gate bias (+20 V) during a short (2 s) pulse of light. Then, a second longer recovery phase is carried out, applying the same bias and the same light for ~15 s. Finally, a relax phase has been performed in dark, by applying no gate bias and keeping drain at -1 V for long time.

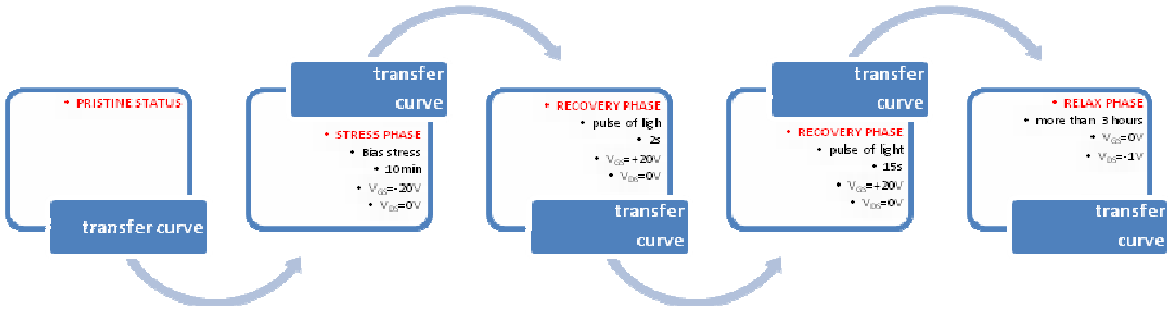
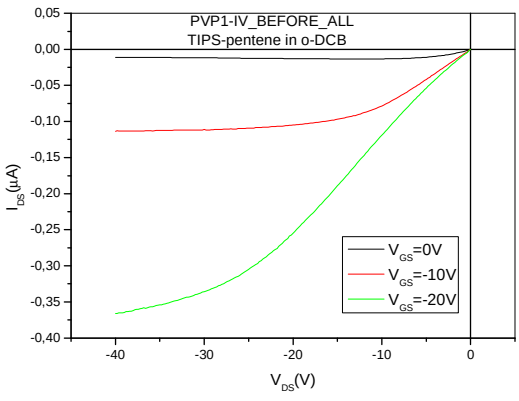


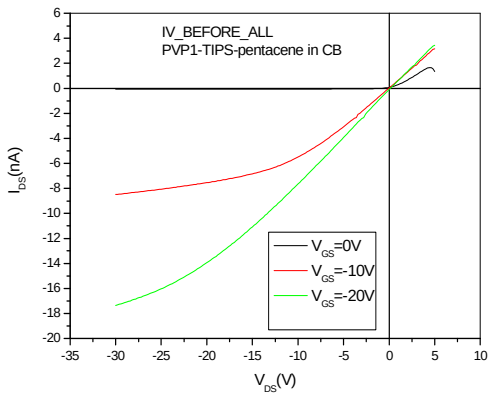
Figure 5.9: Experimental procedure applied for the characterization of the OTFTs.

Figure 2a) shows typical output characteristics for the four types of TIPS-pentacene OTFTs at room temperature, and figure 2b) shows the transfer characteristics in the saturation regime (V_{DS} = −30 V) measured in vacuum and in dark condition.

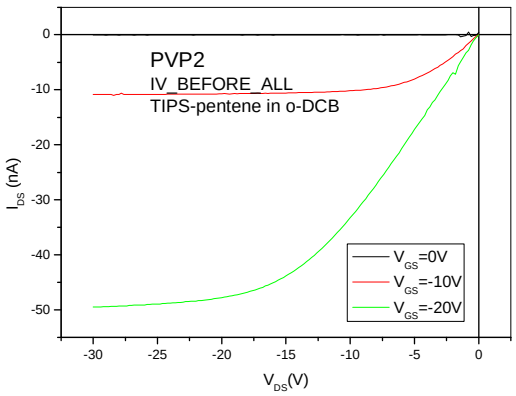
Output characteristics (a)

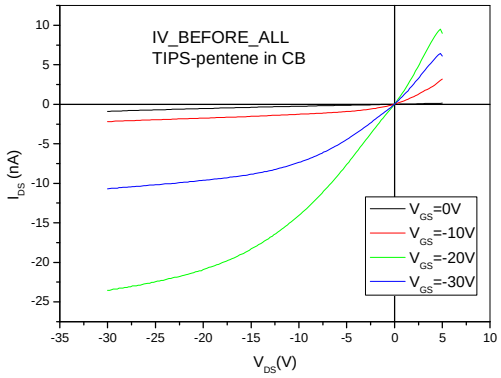


PVP1, TIPS-pentacene in o-DCB



PVP1, TIPS-pentacene in CB

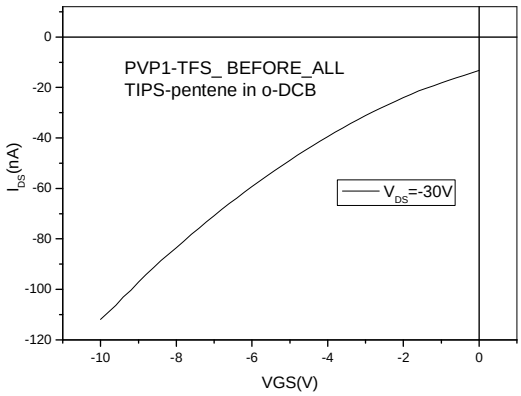


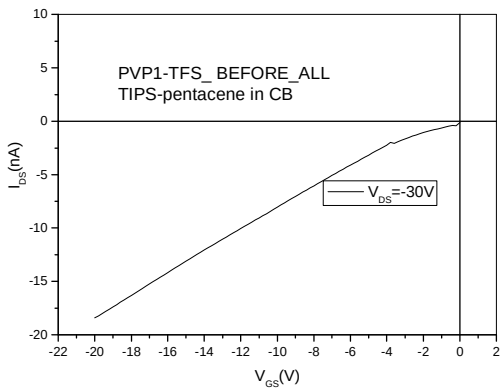


PVP, TIPS-pentacene in o-DCB	***PVP1, TIPS-pentacene in CB***

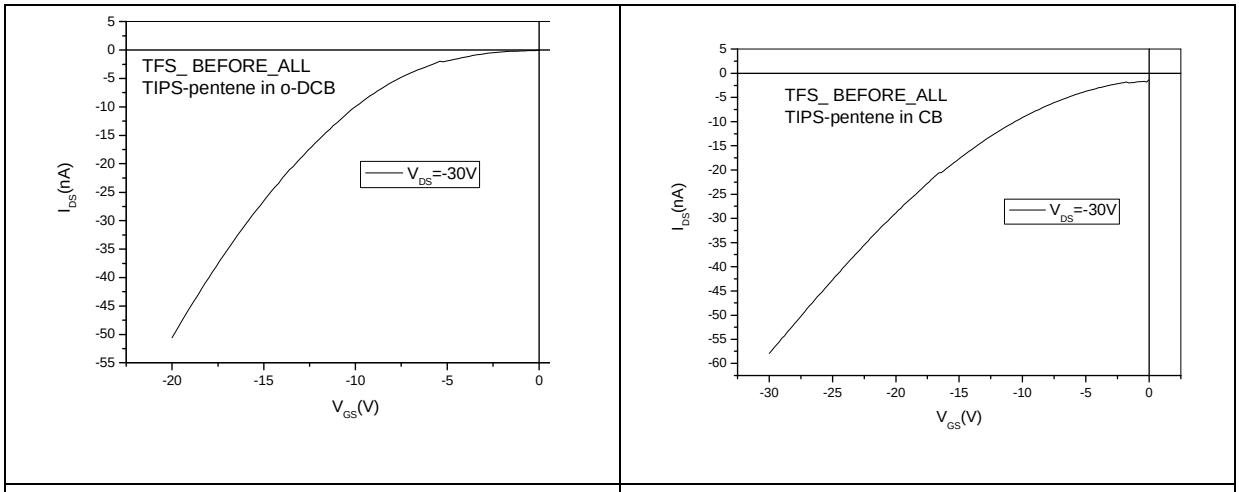
Fig. 5.10 a): Output characteristics of OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right). Devices made with PVP recipe 1 are shown above and those made with the recipe 2 are shown in the bottom of the figure.

Trans characteristics (b)





PVP1, TIPS-pentacene in o-DCB	***PVP1, TIPS-pentacene in CB***



PVP2, TIPS-pentacene in o-DCB	***PVP2, TIPS-pentacene in CB***

Fig. 5.10 b): Transfer characteristics in saturation regime of OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right). Devices made with PVP1 are shown above, and those made with the PVP2 are shown at the bottom of the figure.

The estimated threshold voltages of OTFT with TIPS-pentacene in o-DCB was V_T = +4.7 V, whilst the estimated threshold voltages of OTFT with TIPS-pentacene in CB was V_T = +6.04 V in devices made with PVP dielectric recipe 1, while, in devices made with PVP dielectric recipe 2, the estimated threshold voltages of OTFT with TIPS-pentacene in o-DCB was V_T = -1.95 V, whilst the estimated threshold voltages of OTFT with TIPS-pentacene in CB was V_T = +3.3 V.

5.4.3 Results And Discussion

- ***STRESS PHASE***

Figures 4 shows the transfer characteristics of the four types of transistors before and after the 10 min gate stress (V_{GS} = -20 V. As a result of this bias stress, the threshold voltage has shifted to negative direction.

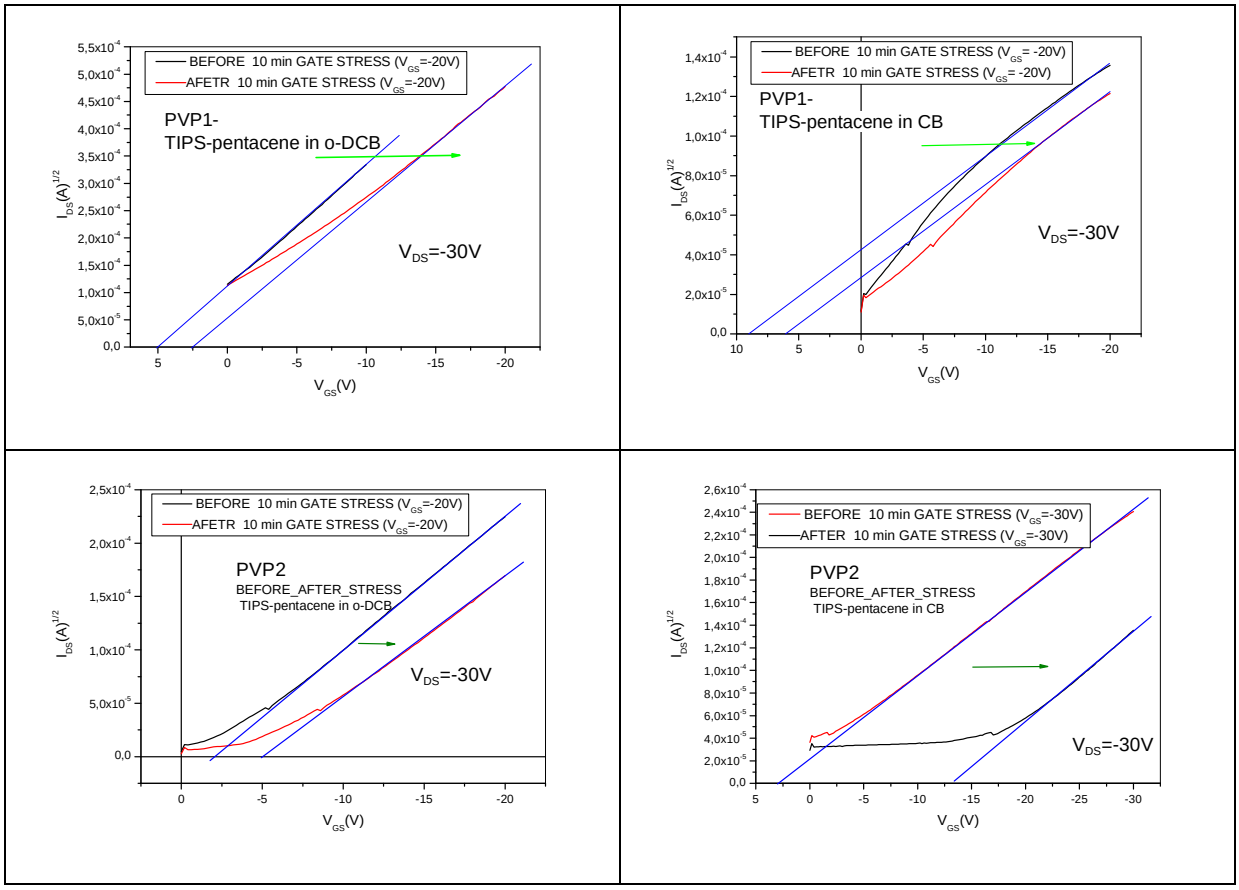


Fig. 5.11: Square root of I_{DS}-V_{GS} of OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right) before and after the bias stress phase. Devices made with PVP recipe 1 are shown above and those made with the recipe 2 are shown in the bottom of the figure.

The shift of the threshold voltage is related to the amount of trapped charge.

The effect of gate stress is more evident in the device having TIPS-pentacene in CB than in the one in o-DCB where the shift of the threshold voltage is less marked. This effect is particularly evident in devices made of dielectric PVP recipe 2

The results of figure 5.11 indicate that moderately high biases induce charge trapping. If negative gate bias is employed, mobile charges are trapped. In the literature, some authors reported charge trapping in organic TFT, both polymer and small-molecule based [41,42]. In principle, charge can be trapped at (i) the bulk of the insulator, (ii) at the semiconductor/insulator interface, and (iii) in the bulk of the semiconductor layer. Some authors also reported about trapping in the organic semiconductor [43,44,45], or bias-induced charged defects [45], which, in turn, move in the organic semiconductor, inducing long-lived threshold voltage variations with the mechanism explained in paragraph 5.2.2.

- ***RECOVERY PHASE #1 (2 s of light exposure)***

We have investigated the optical properties of these transistors and observed a reversible light-induced threshold voltage shift. Under illumination, we observed a reversible light-induced threshold voltage shift towards the positive direction while the field-effect mobility and on/off ratio remain almost unchanged.

After the bias gate stress, the devices have been subjected to a first recovery session during which the gate voltage was set at +20 V, the drain kept at 0 V, and the channel regions illuminated for 2 seconds using a LED a 536 nm. As can be seen from Figure 5.12, the current of the channel, increases in correspondence of lighting.

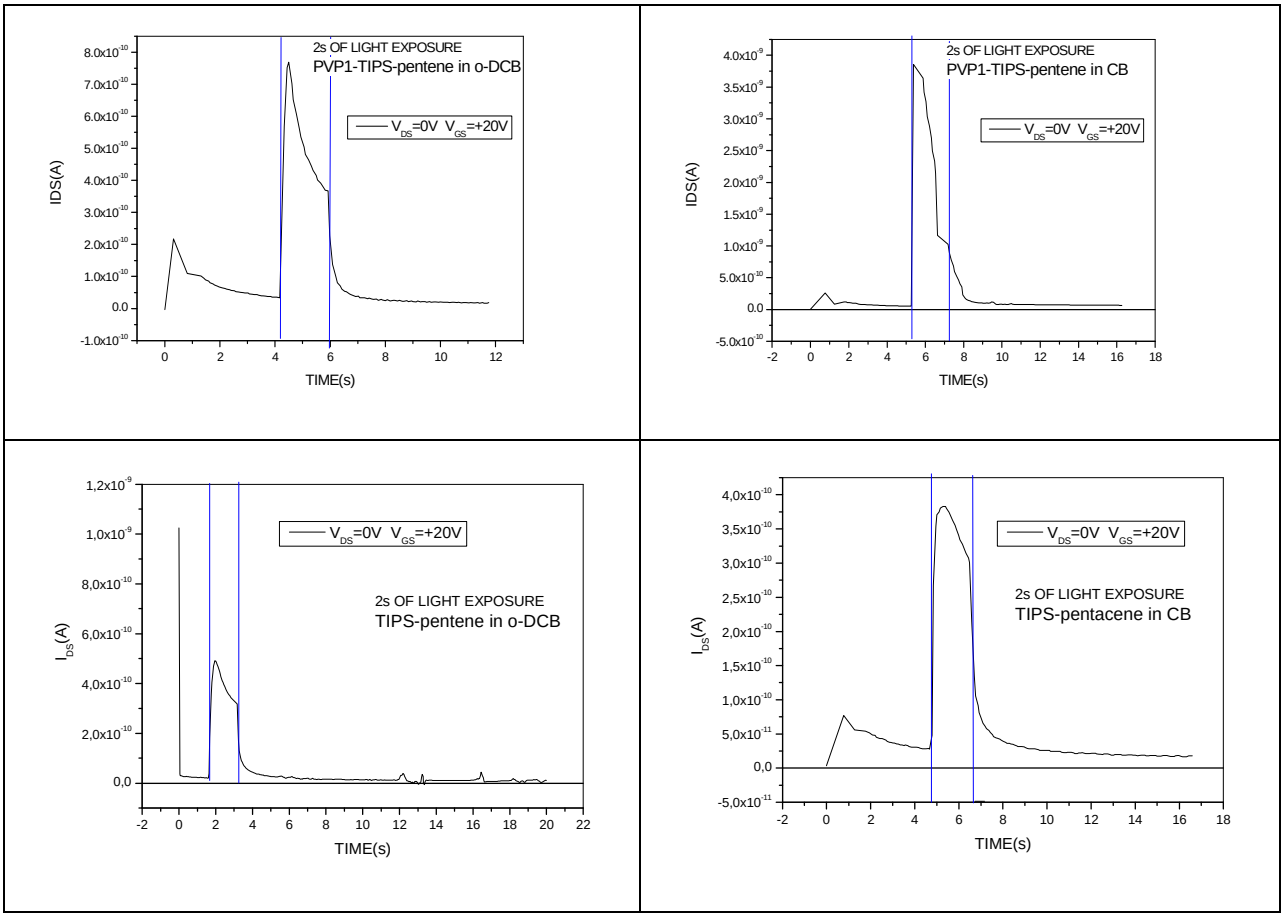


Fig. 5.12: Recovery session #1 for OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right). Devices made with PVP recipe 1 are shown above and those made with the recipe 2 are shown in the bottom of the figure

Figure 5.13 shows the variation of the transfer curves and the plots of $|I_{DS}|^{1/2}$ vs V_G at V_D=−30 V under broadband illumination

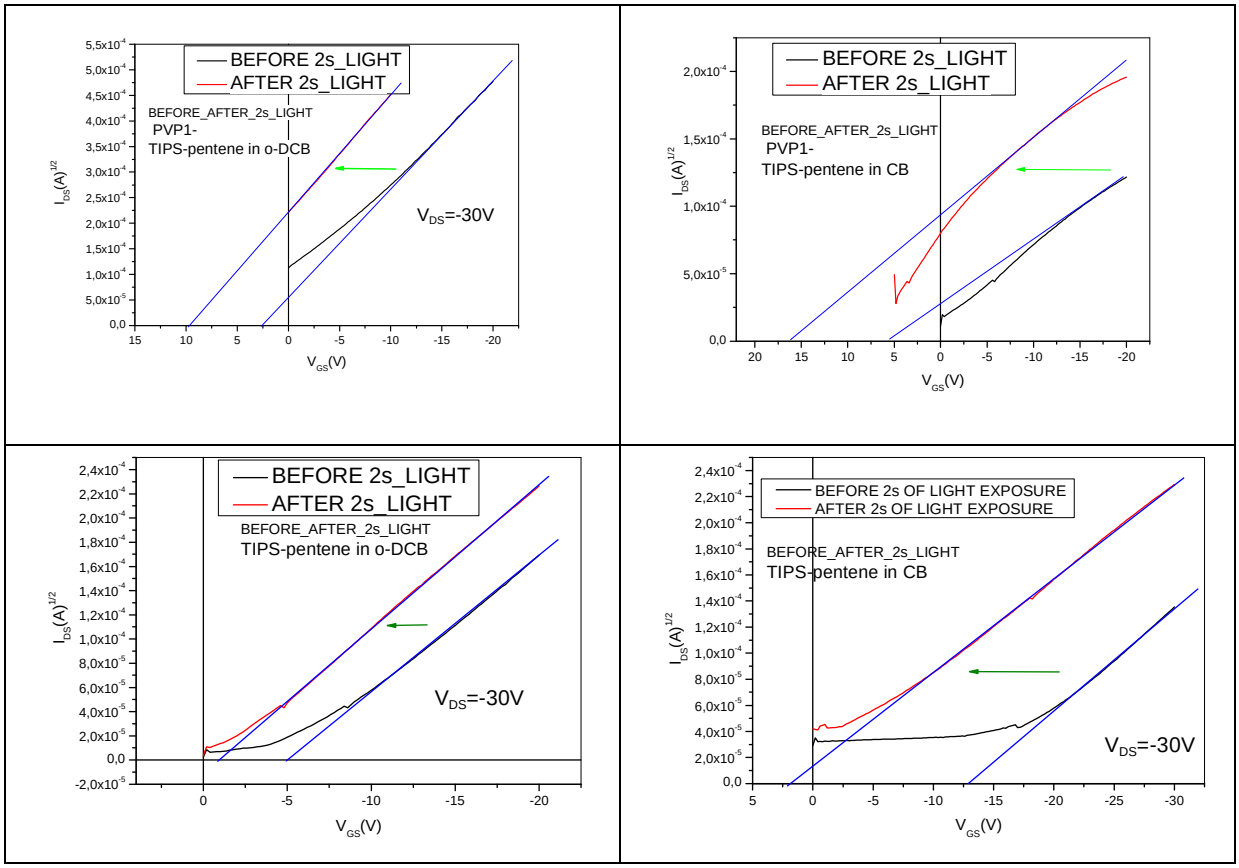


Fig. 5.13: Square root of I_{DS}-V_{GS} for OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right) before and after the recovery phase #1 (2 s of positive gate bias and light exposure). Devices made with PVP recipe 1 are shown above and those made with the recipe 2 are shown in the bottom of the figure

It can be seen from the figure that the V_T shifted towards the positive direction,. The drain current under illumination I_D^{light} was increased at low V_{GS}.

- ***RECOVERY PHASE #2 (~15seconds of light exposure)***

When a high enough positive bias is applied, electrons are trapped. Photons with high enough energy increase the effects of positive bias, because of the excess of photogenerated electrons. In fact, it is well known [46] that photons with energy larger than the energy gap can photogenerate electron-hole pairs, which may either be trapped or may neutralize the trapped holes.

Light accelerates positive charge neutralization if a positive bias is applied. In fact, under the action of the positive bias, the photogenerated electrons drift toward the interface between the semiconductor and the gate insulator, neutralizing the trapped holes [42]. When the positive bias is applied, the TFT is driven toward a strong depletion, and then

the excess photo-generated holes are swept away by the field. The Photo-generated electrons recombine with the trapped charges and neutralize them.

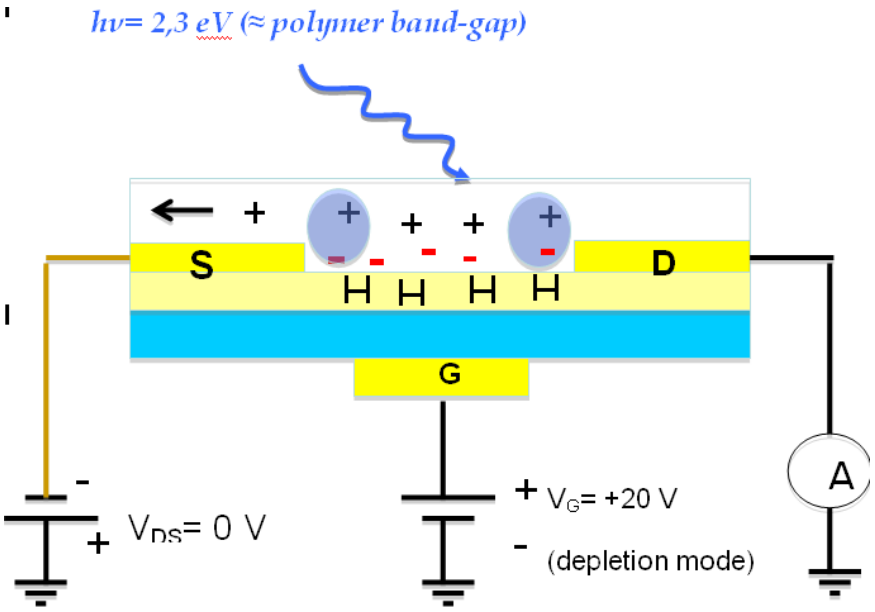
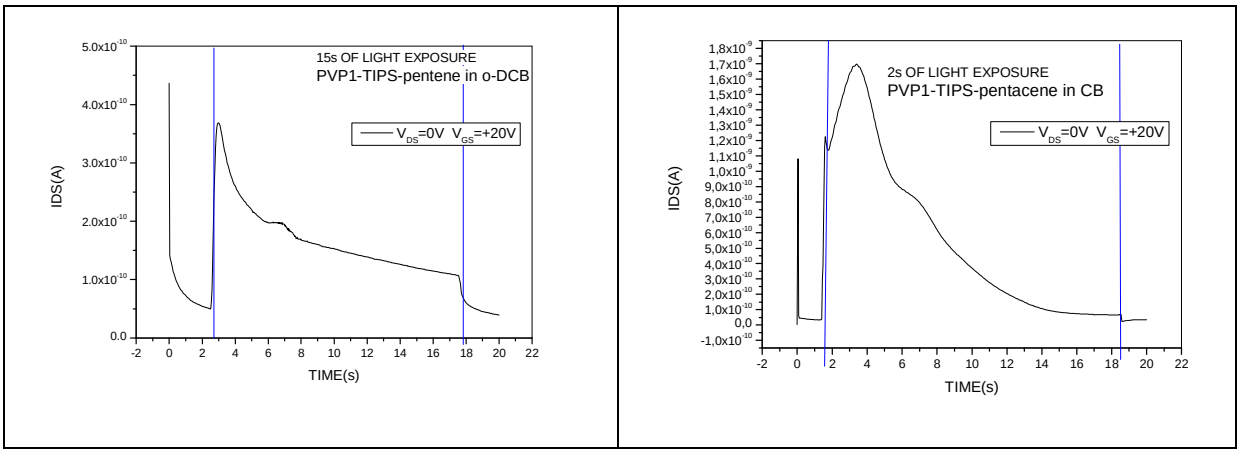


Figure 5.14 :light effect scheme



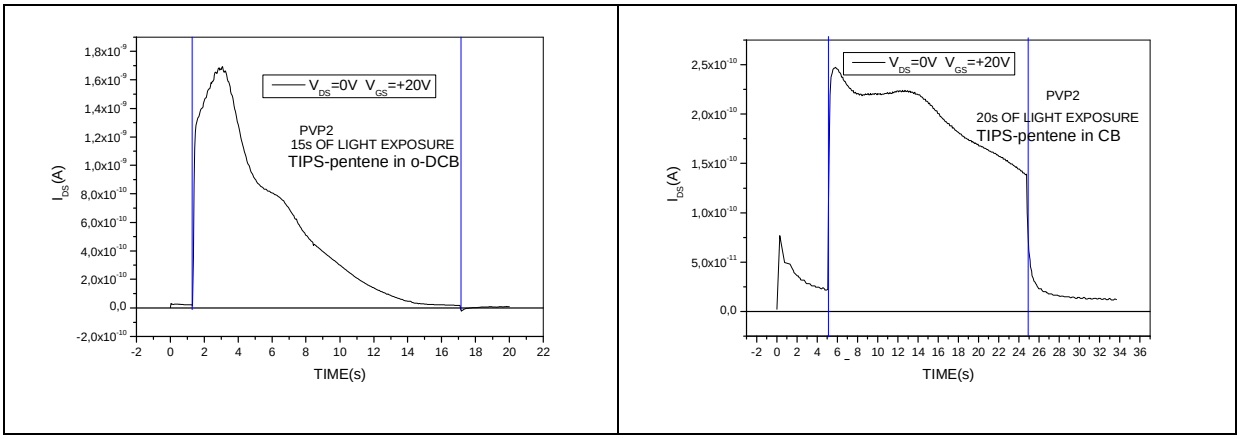


Fig. 5.15: Recovery phase #2 for OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right). Devices made with PVP recipe 1 are shown above and those made with the recipe 2 are shown in the bottom of the figure

If too much light has been flashed, it can start to trap electrons and this then moves the threshold voltage to more positive values, as shown in figure 5.16.

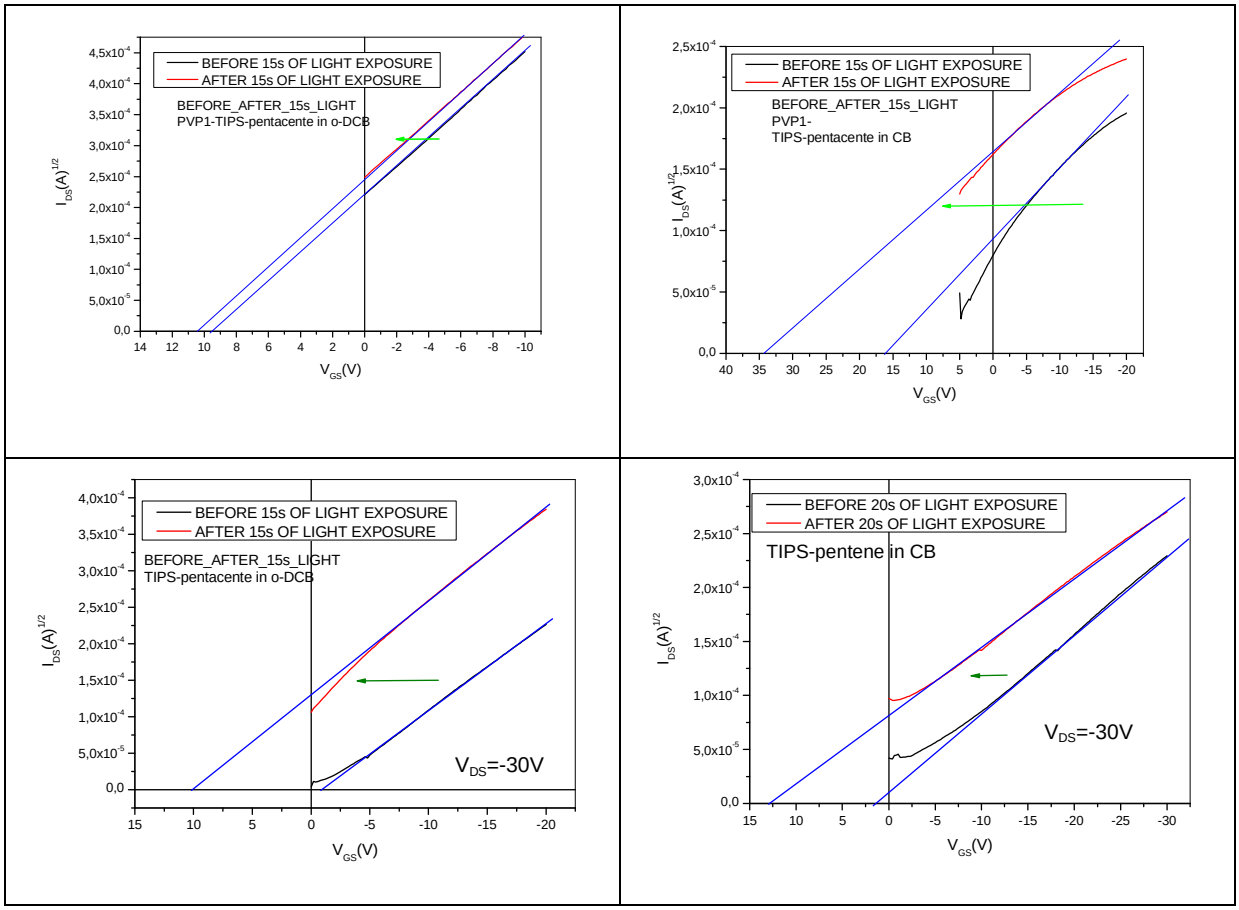


Fig. 5.16: Square root of I_{DS}-V_{GS} for OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right) before and after the recovery phase (~15 seconds of light exposure). Devices made with PVP recipe 1 are shown above and those made with the recipe 2 are shown in the bottom of the figure.

- ***RELAX PHASE***

After the second recovery, the devices experienced a relax phase in dark, by applying no gate bias and V_{DS} = -1 V for a long time (some days) at room temperature.

When the device was put in the dark again after illumination, V_T began to shift towards the negative direction. After many hours in the dark, the electrical characteristics had almost returned to their original states, as shown in Fig. 5.18. In other words, the light-induced carriers were gradually neutralized and the overall carrier density in the channel was restored to its original state after the transistor was kept in the dark for enough time.

Figure 9 shows the relaxation of I_D at V_G =0 V, V_D=−1 V after the illumination. The trends of the relax kinetics in figure 5.17 can be described through exponential decays.

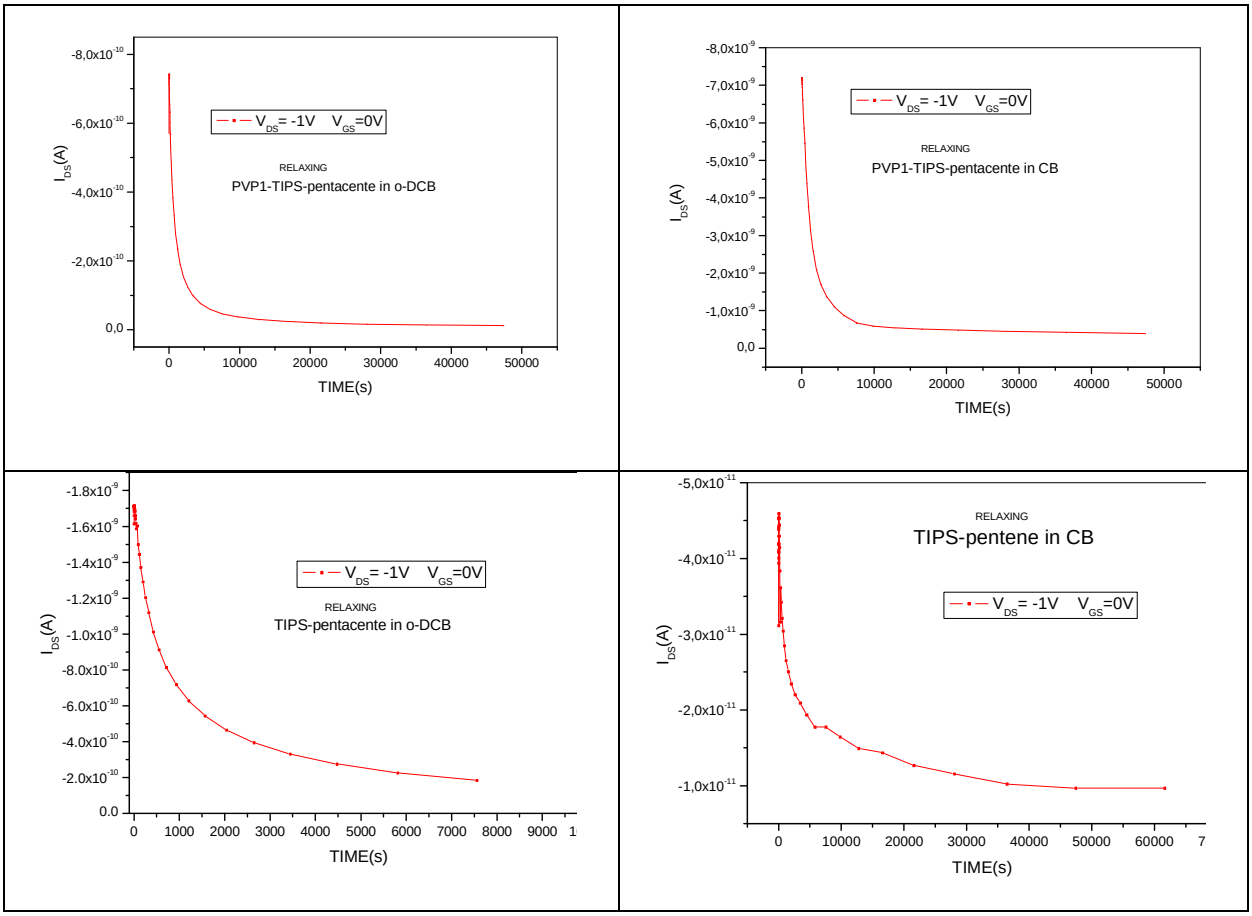


Fig. 5.17: Relaxing session of OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right) Devices made with PVP recipe 1 are shown above and those made with the recipe 2 are shown in the bottom of the figure.

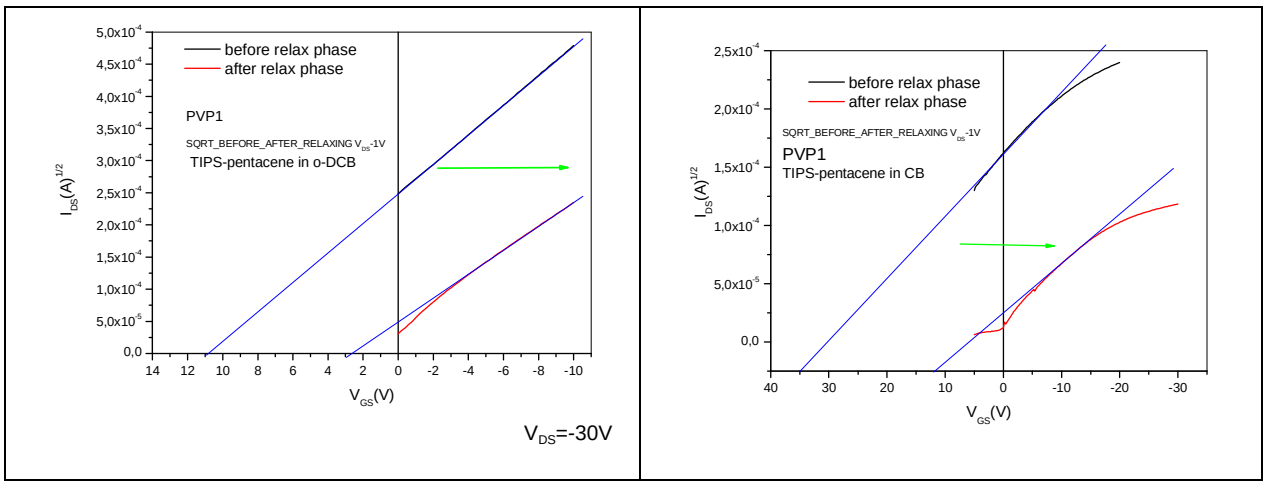
Approximately, the time where half of the drain current decreased was used as the recombination time for the holes in the channel (τ). From Fig. 5.17, τ was determined to be about:

DEVICES	**τ (s)**	**error**
PVP1 CB	1364	1,7%
PVP1 ODCB	870	0,7%
PVP2 CB	1953	1,3%
PVP2 ODCB	688	0,6%

Table 5.3:time where half of the drain current decreased was used as the recombination time for the holes in the channel (τ) for all type of devices.

The long recombination time might indicate the deep electron traps in the PVP film or at the TIPS-pentacene/PVP interface. We can observe that the device having longest recombination time result the device having tips pentacene dissolved in CB.

As a result of the relaxing phase, the threshold voltages of all the devices shifted from positive values to values near 0 V. Figure 5.18 shows the transfer characteristics in saturation before and after the relaxing phase, and the variations of the threshold voltages.



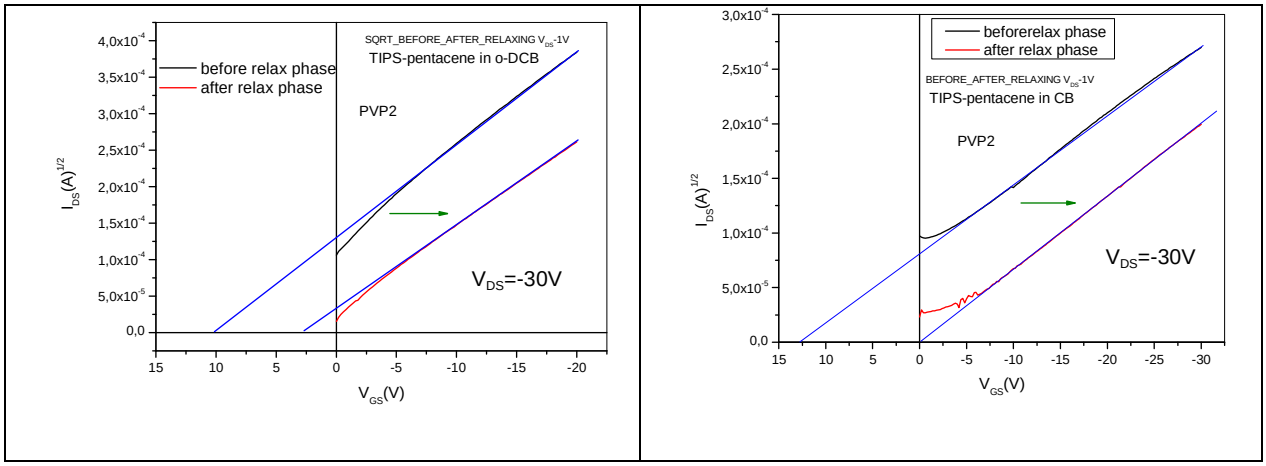
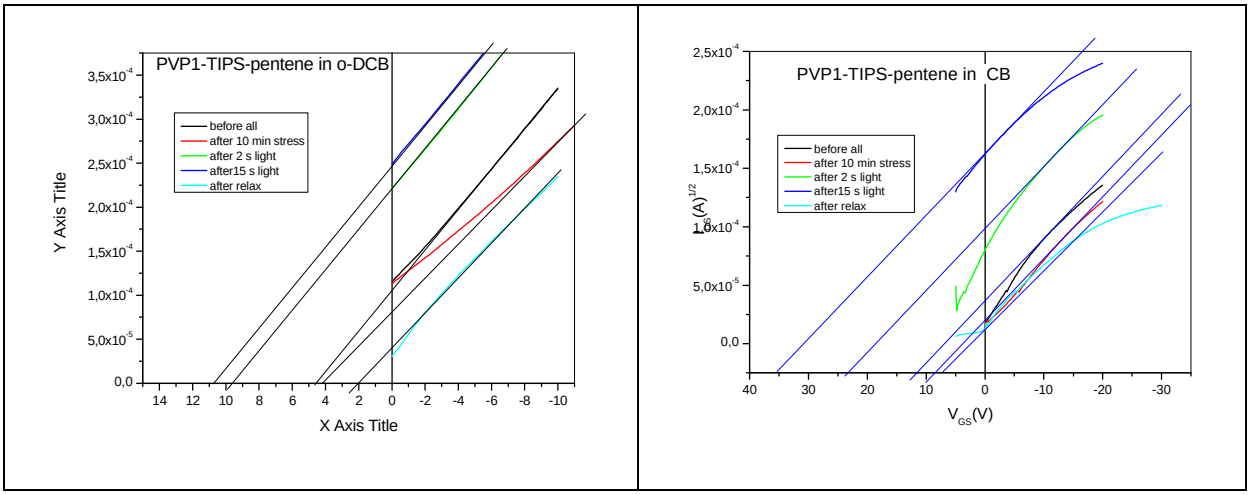


Fig. 5.18: Square root of I_{DS}-V_{GS} of OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right) before and after the relaxing phase . Devices made with PVP recipe 1 are shown above and those made with the recipe 2 are shown in the bottom of the figure

It is possible that, when photogenerated excitons in the TIPS-pentacene film are dissociated into holes and electrons, some of the electrons are trapped in the PVP film or at the TIPS-pentacene/PVP interface. As a result, the holes become free carriers and the overall carrier density in the channel is increased. After the light was switched off, the trapped electrons were slowly released and recombined with the holes in the channel, resulting in the decrease of the drain current.

The general trends of the threshold voltages of the four types of transistors during the five phases are shown in figure 5.19.



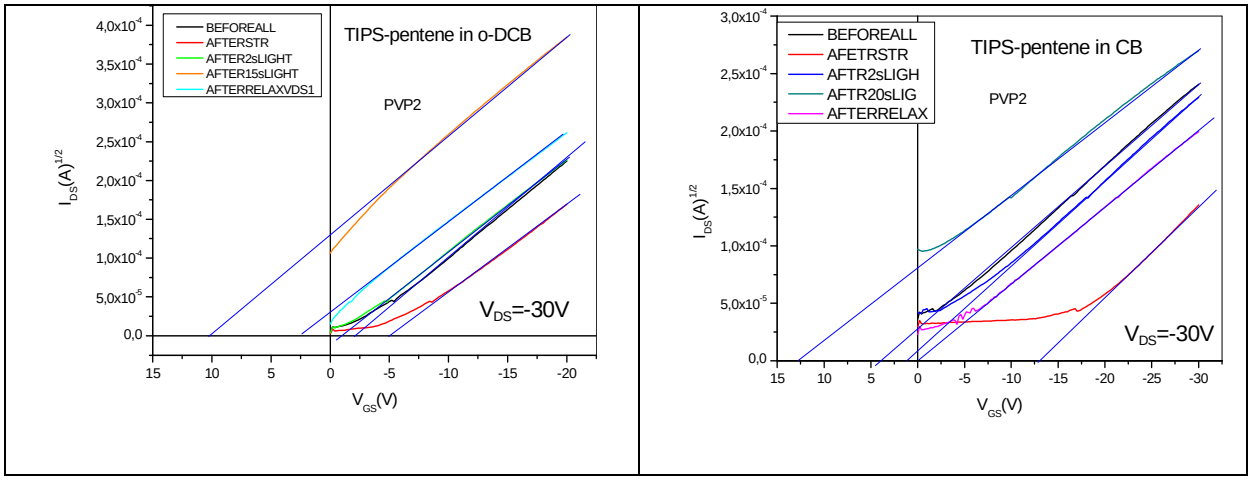


Fig. 5.19: Square root of I_{DS}-V_{GS} of OTFTs with TIPS-pentacene in o-DCB (left) and in CB (right) before all, after stress, after 2 s of light recovery, after ~15s of light recovery and after relaxing phase. Devices made with PVP recipe 1 are shown above and those made with the recipe 2 are shown in the bottom of the figure

The characteristic parameters, calculated through the use of the MOSFET theory, of the four devices during different phases of measurement, are summarized in the following table.

	PVP2 ODCB	***PVP2 ODCB***	***PVP2 CB***	***PVP2 CB***	***PVP1 ODCB***	***PVP1 ODCB***	***PVP1 CB***	***PVP1 CB***
	μ (cm²/Vs)	***V_T(V)***	***μ (cm²/Vs)***	***V_T(V)***	***μ (cm²/Vs)***	***V_T(V)***	***μ (cm²/Vs)***	***V_T(V)***
BEFORE ALL	4,82E-03	-1,915	8,20E-03	8,52	5,39E-02	4,744	1,60E-02	6,049
AFTER STRES	4,16E-03	-5,376	1,00E-02	-13,3	4,39E-02	3,3	1,80E-02	2,112
AFTER-2SLIGHT-	4,19E-03	-0,486	8,50E-03	3,50	5,74E-02	9,333	1,63E-02	16,998
AFTER-15sLIGHT-	4,58E-03	11,699	5,80E-03	14,24	5,60E-02	10,724	7,59E-03	45,255
AFTER-RELAX-	4,01E-03	3,035	6,90E-03	0,0895	3,65E-02	2,616	1,02E-02	5,149

Table 5.4:The characteristic parameters, calculated through the use of the MOSFET theory, of the four devices during different phases of measurement

5.4.4 *Discussion Of The Data*

Surface density of long-lived traps

We have investigated the optical properties of four type of transistors and observed a reversible light-induced threshold voltage shift. Under illumination, the threshold voltage shifts towards the positive direction while the field-effect mobility and on/off ratio remain almost unchanged. In the dark, however, the threshold voltage can slowly be restored to its original state.

Surface density of long-lived traps ΔN can be estimated using $\Delta N = C_{ox} \Delta V_T / e$, where C_{ox} is the capacitance per unit area of the PVP layer, ΔV_T is the shift of the threshold voltage, and e is the elementary charge.[51.]

After each stage has been the evaluated ΔV_T (calculated through the use of the ideal theory) and calculated the ΔN.

The results obtained are summarized in figure 5.20.

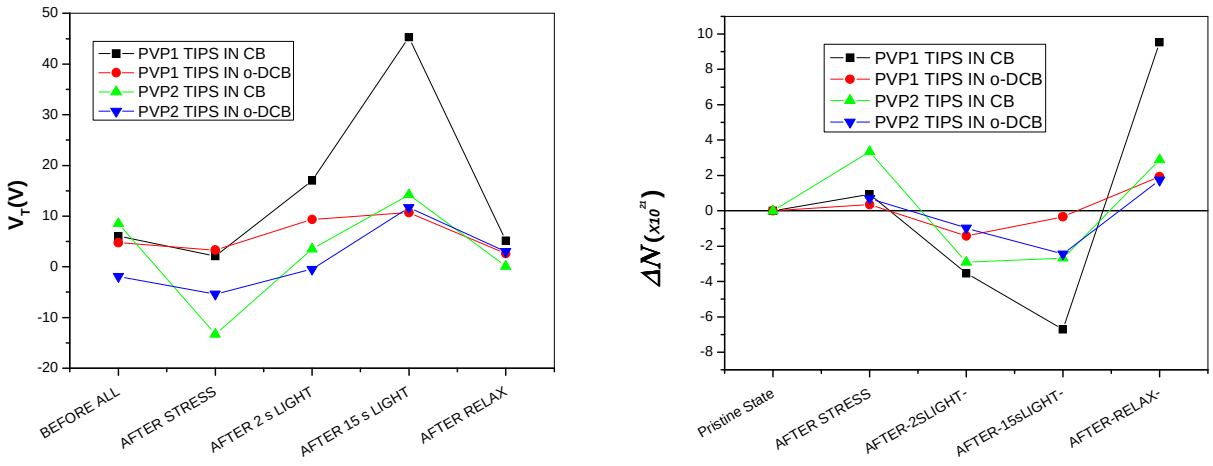


figure 5.20: (left) Trends of the threshold voltage during the phases of measurement; (right) trend of surface density of long-lived traps during the phases of measurement

In the figure 5.20 (*left*), the trends of the threshold voltage during the phases of measurement are shown. The shift of the transistor characteristic (threshold voltage shift) ΔV_T it has been used to estimate the surface density of long-lived traps showed in figure 5.20 (*right*) .

Even in this case it is observed that the devices in o-DCB have less solicitation during the various stages of measurement which result in fewer amount of trapped charges.

The device in PVP1 and TIPS-pentacene in CB demonstrates, even in this case, more sensitive than the others.

Shallow Traps Analysis

The model showed in chapter 2 paragraph 2.2.3 is very simple as it involves only two parameters (field-effect mobility (μ) and V_T) and three constants (L, W, and C_{ox}). That equations fits many device's characteristics relatively well and it allows for an easy extraction of its parameters μ and V_T from the slope and the intercept of $\sqrt{I_D}$ vs. V_{GS} in saturation, which are thus widely used to compare device performance.

The mobility extracted using the above method is usually V_{GS} dependent for strongly disordered systems such as a-Si:H and organic semiconductors [50].

It is used to model a-Si:H TFTs using only the presence of exponential tail states and well defined mobility edges [47,48].

An intrinsic mobility in the transport band(s) (beyond the mobility edge) is assumed to be constant. Exponential distributions of localized trap states tailing the bands are further assumed. The free and trapped charge density can be approximated, as long as the Fermi level is more than a few thermal voltages away from the mobility edge. In the case of hole transport this gives

$$q_{trapped} = eN_t e^{\frac{\psi_0 - \psi}{eV_t}}$$
$$q_{free} = eN_v e^{\frac{\psi_0 - \psi}{k_B T_t}} \qquad (1)$$

where Ψ is the Fermi energy level relative to the mobility edge, Ψ_0 its value at charge neutrality, V_t the characteristic slope of the tail states and N_V and N_t the effective density

of states for the valence band and the tail states. Using $q_{free} << q_{trapped}$ and thus $q \sim q_{trapped}$ one arrives at:

$$\mu_{eff} = \frac{q_{free}}{q_{trapped}} \mu_{band} \propto (V_G - V_T - V(x))^{\frac{eV_t}{k_B T}-1} \quad (2)$$

and after integration along the channel it can be finds the V_{GS} dependence(viewed in chapter 2 paragraph---) of the effective mobility in the Shockley Model to be:

$$\mu_{eff} \propto (V_{GS} - V_T)^{2\left(\frac{eV_t}{k_B T}-1\right)} \quad (3)$$

and of the saturated drain current:

$$I_{D,sat} \propto (V_{GS} - V_T)^{2\frac{eV_t}{k_B T}} \quad (4)$$

which is useful for the extraction of the tail state parameter V_t since it can strongly reduce contact effects by applying a strong bias along the channel beyond the saturation condition. Similarly the bias dependence in the linear region is approximated by:

$$I_{D,lin} \propto (V_{GS} - V_T)^{2\frac{eV_t}{k_B T}-1} V_{DS} \quad (5)$$

If the behavior of the active material is dominated by traps is then possible to extract V_t from transfer curves in above-threshold regime.

Taking into consideration the flow-chart of measurement in figure 3, can be counted four different solicitations:

1. Gate stress for 600s
2. Recovery of 2s: the reverse bias of the gate associated with light pulse 2 s
3. Recovery of ~15s: the reverse bias of the gate associated with light pulse ~15 s
4. Relax "long" without stress through gate-drain flushing

We modeled the deviation from the standard characteristics by the formalism from Estrada et al. described in [49]:

$\mu_{FET} = \mu_0(T)(Vg-V_T)^{\gamma}$

were, therefore, from equation 3, $\gamma=2(((eV_t)/k_bT)-1)$ and is parameter indicates the deviation from conventional theory and μ_0 is the intrinsic mobility.

From this equation was derived the threshold voltage V_T used to evaluate the thermal voltage (V_t) described above.

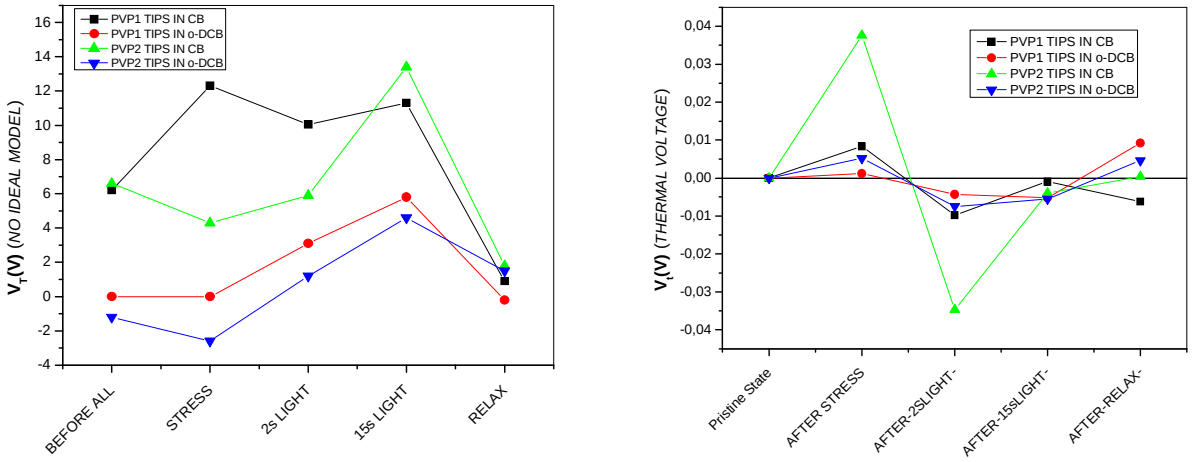


Figure 5.21: to the left threshold voltage for the different devices and in different phases of measurement, obtained through the model of Estrada et al. [49].to the right variation of the thermal voltage for the various devices between the different phases of measurement, obtained through the model described in [47,48].

The analysis of the parameters through the use of the model of Estrada et al [49] highlights the difference in behavior of samples having tips pentacene dissolved in o-DCB compared to devices with tips pentacene dissolved in CB, in which evidence be a higher threshold voltage variation (figure 5.21 *left*).

In particular devices with tips pentacene in o-DCB have threshold voltages more close to zero and with less tendency to positive values, typical of electronic entrapment .

This behavior is also reflected in the trends of the thermal voltage (see figure 5.21 *right*) in which stress bias and light pulses change more deeply the density of states above the band edge. Also, the transient behavior, occurred in the devices having dielectric PVP2, showed a trend less influenced by the solvent used for the semiconductor , thus giving a more controlled and repeatable chemical interaction.

Furthermore it is possible to observe that :

Both the stress of gate (# 1) that the relaxation (# 4) cause a negative delta of the threshold voltage $V_{threshold}$(except in the case of device in PVP1 and Tips in CB) . In fact, if we take into account the threshold voltages , both in the case that in the case # 1 # 4, for

the OTFT , V_G - $V_{threshold}$ < 0 is applied, in particular , in the case # 1 this happens because V_G = -20 while in the case # 4 the condition of over threshold is realized because the OFET has a positive threshold (emptying). Probably the flowing of p current leads fixed charges at the interface thus moving the threshold values towards negative directions during the stress phase, while introduces free charges during the relaxation .

Recovery conditions # 2 and # 3 not limited to compensate the shift of the threshold voltage induced by the stress of the step # 1 but it goes beyond . Probably because that exposure to light is able to change not only the charge of the traps that exist but also their quality (distribution) . In the other worlds the lighting condition is look like a stress solicitation. Light exposure can neutralize the traps, causing a temporary recovering of the threshold voltage, it may also fill traps and modify the sign of the threshold voltage.

5.4.5 Conclusions

In this work, we showed the effects of the gate bias stress and of the light on organic thin-film transistors fabricated with two different solvent for the semiconductor TIPS-pentacene and different receipts for cross linked PVP as dielectric.

Relatively high negative biases induce a noticeable charge trapping, which manifests itself as a shift of the transfer characteristics towards negative voltages. Such shift can be even larger than 10 V if a -30 V bias is applied for 600 seconds.

Light enhances both the electron trapping and the hole neutralization kinetics, with a positive bias applied after the negative gate stress. A subsequent long phase of relaxation allows a return to values close to those of the initial transfer curves.

A reversible light-induced threshold voltage shift with large responsivity and slow recovery in dark was observed in the transistor. The reversible light-induced threshold voltage shift is explained in terms of the electron trapping and detrapping mechanism in the TIPS-pentacene/PVP interface.

We attribute the different electrical instabilities to the different boiling points of the two adopted solvents, which reflects into a different cristallinity of the active materials. We conclude that the solvent plays an important role in the stability of the devices as well as for morphology and energy distribution of the states in disordered organic systems .

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Conclusions

This thesis has been dedicated to study, fabricate and characterize innovative organic thin film transistors (OTFTs: Organic Thin-Film Transistors), using organic semiconductors and insulators.

It is well known from literature that solution-processed organic materials for electronic devices can be deposited and processed employing very cheap and simple methods, like spin-coating, printing, drop casting [1,2,3].

The properties of organic materials strongly depend on their morphology, which depends on the method of deposition. Morphology also influences the behaviour of the interfaces between the materials and so can be very important for the performances of the device, in particular for OTFTs.

Device instability and limited lifetime have been the hurdles to commercialization of organic electronics. Through electrical characterizations and microscopy techniques, much progress has been made in understanding the stress mechanisms that limit the stability of the organic field-effect transistors. The kinetics and mechanisms of charge trapping in organic semiconductors are examined to explain the instability behaviours. The external processing factors, such as light and environmental conditions that affect the severity of instability, are also investigated to enable controllable and reproducible device fabrication.

So, starting from the analysis of the effects of different sources of instability on the performances of the organic TFTs, it has been tried to deduce some connection to the devices' fabrication.

Therefore, the study has been mainly concentrated on the properties of the devices and on the analysis of the effects of three distinct sources of stress, using one device architecture and different technological configurations.

Starting from literature analysis [4,5,6,7,8,9], OTFTs have been realized in configuration bottom-gate bottom-contacts on glass substrate, using crosslinked PVP as a gate dielectric and TIPS-pentacene as organic semiconductor. Different types of transistors have been realized, changing some process parameters to understand their influence on the stability of the devices.

Four OTFT configurations have been applied, changing only one parameter in each different device. It has been focused on:

- two different concentrations of the crosslinking agent in the dielectric (called as PVP1 and PVP2),
- two different solvents for the semiconductor (chlorobenzene, CB, and ortodichlorobenzene, o-DCB).

The layers obtained were morphologically studied: these analyzes showed a strong difference in the crystalline phase between the tips pentacene dissolved in CB and one in o-DCB. In particular it has been highlighted a greater crystalline phase in devices having tips pentacene dissolved in o-DCB that gives a semiconductor with larger grains .

This phenomenon is due to the slower evaporation rate of the o-DCB solvent, which has a boiling temperature higher than the CB. Furthermore there was a different polarity between the surfaces of two recipes of dielectric. Wherefore influence the capacity to absorb water.

With the purpose to have information about the stability, several studies have been performed on the OTFTs, measuring them after various types of stress.

In order to obtain insight into the stress behaviour, it has been performed two series of measurements.

• In the first experiment, voltages of V_{GS} = −20 V and V_{DS} = 0 V were applied for 600 s to the OTFTs as the constant bias stress. The stress was carried out in vacuum as well as in air (room temperature), in order to elucidate the intrinsic properties from air effects.

In that experiment, it has been observe a negative shift of the threshold voltages after the stress in vacuum, and a positive shift after the stress in air. It has been attributed this shift to charges trapped in deep electronic states in TIPS-pentacene near the dielectric interface. The positive shift was attributed to water or O_2 species, present in air, absorbed in the organic materials. Such air species dope the surface and create a top surface path for the current. The currents increase and change the threshold voltage The more evident variations are observed in the devices with TIPS-pentacene dissolved in CB both in air an vacuum.

• In the second experiment, measurements were carried out in dark conditions, in vacuum, and stress effect was measured as a function of time.

It has been measured the trend of the threshold voltages over time for the 4 types of transistors. The gate bias stress (V_G = -20 V) has been applied to the devices in vacuum for more than 24 hours. The effects of the stress on the threshold voltages were measured in function of time for each device, and were fit with stretched-exponential time dependence:
From the analysis of the fit characteristic parameters, it was possible to compare the trapping time in different transistors. It is observed that the different devices show different times of stress (and thus charges trapping). In particular, it was found that the devices having larger grains (devices with tips-petacene dissolved in o-DCB) show less instability to external stimuli with smaller variations of the threshold voltage and longer trapping times.
In order to investigate the effects of ambient moisture on the electrical stability of devices, typical transistor characteristics were measured varying the relative humidity (RH), keeping the devices in inert atmosphere (a constant flow of pure nitrogen).
The presence of humidity influences in the same way the charge transport in all these types of TIPS-pentacene based OTFTs., resulting in a mechanism that is responsible for observed variation in mobility and threshold voltage. The observed effects are closely related to the amount of grain boundaries of the film of semiconductor, in turn dependent on the conditions process used for the realization of the device. It has been observed a deterioration of the threshold voltage in correspondence of an increase of% RH, while the mobility increases only in the case of devices having Tips pentacene dissolved in CB which has lower crystallinity. It has been also possible noted that this effect is rather reversible, if the device was held for enough time at of low humidity.
It has been studied the effect of light pulses on the traps which are responsible for the operational stability of the OTFTs.
Exposition of the channel region of these OTFTs to the light causes a shift of the threshold voltage of the devices, so revealing a change in the number of the traps in the semiconductor.
For a much more accurate investigation on the role of light and bias on these TIPS-pentacene OTFTs, it has been performed a 4-phases experimental procedure, subjecting the devices to electrical bias stress and illumination. At the end of each phase, the transfer

characteristic of the devices has been measured and the shift of the threshold voltage evaluated .

The measurements indicate the presence of two distinct trapping phenomena. Appreciable hole trapping can be achieved using negative bias stresses for a limited time (600 s). Exposure of the devices to the light neutralizes defects under positive gate biases, giving as a result a shift of the threshold voltages towards positive values. From traps analysis, also in this type of experiment it has been demonstrated that the devices with tips pentacene dissolved in o-DCB have less solicitation during the various stages of measurement which result in fewer amount of trapped charges.

In conclusion four types of OTFTs have been fabricated and characterized, to evaluate the effects of environmental, luminous and electrical stresses on devices prepared using different recipes for the organic materials. The responses of the devices to these stimuli have shown different behaviours depending on the different processes applied for their fabrication. This work emphasized the importance of process conditions on the stability of the devices, but the utilization of a particular type of structure of the device depends on the application to which it is intended

We attribute the different electrical instabilities to the different boiling temperatures of the two adopted solvents for the semiconductor, and to the dissimilar electronegative group amount of the surface of PVP1 and PVP2, probably due to the different concentrations of the crosslinking agent and to the curing in the two recipes of the dielectric. These factors give origin to a different water adsorption, and so to different electrical responses to the stress.

In particular it has been observed that the devices processed by o-DCB solution have:

- higher mobilities, due to higher OSC's grain size and lower threshold voltages,
- longer time traps, if compared to CB ones,
- light trapping-detrapping experiments confirm that o-DCB made OTFTs have a minor number of total traps.

Devices made by PVP1 are more influenced by the combination with OSC's solvents. Bias stress characteristic times extraction demonstrates that best overall stability performances of the combination of PVP1 and TIPS-pentacene dissolved in o-DCB.

Naturally, these aspects may have important technological implications, regarding wider issues related to the time of life of the organic circuits and the integration issues, which deserve a strong interest and could be studied in a follow-up of the activities reported in this thesis.

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Appendage

Scientific Production

[1] *P. Maddalena,* ***R. Rega****, A. Grimaldi, M. G. Maglione, P. Tassini, P. Morvillo, C. Minarini* "**Analisi del degrado di materiali e di celle fotovoltaiche organiche indotto da stress termico"** TechNote archives ENEA.(2013)

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Under submission:

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