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Modeling and Experimental Investigation of Silicon Carbide MPS/JBS Diodes and Emerging Power Device Architectures

by

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*Hic cursus, quamvis arduus ac difficilis, ad finem
pervenit; sed hic finis nihil aliud est nisi initium
novi itineris.*

MODELING AND EXPERIMENTAL INVESTIGATION OF SILICON CARBIDE MPS/JBS DIODES AND EMERGING POWER DEVICE ARCHITECTURES

Ph.D. Thesis presented
for the fulfillment of the Degree of Doctor of Philosophy
in Information Technology and Electrical Engineering
by

VINCENZO TERRACCIANO

December 2025

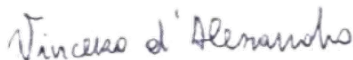


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Candidate's declaration

I hereby declare that this thesis submitted to obtain the academic degree of Philosophiæ Doctor (Ph.D.) in Information Technology and Electrical Engineering is my own unaided work, that I have not used other than the sources indicated, and that all direct and indirect sources are acknowledged as references.

Parts of this dissertation have been published in international journals and/or conference articles (see list of the author's publications at the end of the thesis).

Napoli, December 10, 2025

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Vincenzo Terracciano

Abstract

The thesis is organized into two complementary research directions, devoted to the modelling and characterization of silicon carbide (SiC) power devices. The first concerns the development and validation of a lumped-parameter electrothermal model, SPICE-compatible and geometrically scalable, for silicon carbide Merged PiN Schottky (MPS) diodes. The proposed circuit model accurately describes the forward conduction behaviour, including the dependence on temperature and geometry, self-heating effects, and the *snapback* phenomenon, as confirmed by TCAD simulations. Within the same research line, an experimental campaign has been carried out, followed by a failure analysis, on 1.2 kV SiC Junction Barrier Schottky (JBS) diodes, aimed at optimizing wire bonding at *die* level in order to increase the maximum current capability under *surge current* conditions.

The second research direction introduces an innovative concept of 1.2 kV SiC *Gate-All-Around* (GAA) MOSFET, investigated through static, dynamic, and electrothermal mixed-mode TCAD simulations. The proposed cylindrically symmetric structure enables a uniform distribution of the electric field without the need for a dedicated termination region, thereby improving the trade-off between specific on-resistance and breakdown voltage. However, the 360° silicon dioxide insulation limits heat dissipation, making short-circuit events particularly critical. As a possible solution, the last part of the thesis investigates the integration, within the gate oxide, of a ferroelectric layer capable of limiting the current and the resulting self-heating during short-circuit transients.

Keywords: silicon carbide, MPS, JBS, SPICE, electrothermal, self-heating, *snapback*, wire bonding, *surge current*, GAA MOSFET, TCAD simulations, short-circuit, reliability, ferroelectric.

Sintesi in lingua italiana

La tesi è articolata in due filoni di ricerca complementari, dedicati alla modellazione e alla caratterizzazione di dispositivi di potenza in carburo di silicio (SiC). Il primo riguarda lo sviluppo e la validazione di un modello elettrotermico a parametri concentrati, compatibile con SPICE e geometricamente scalabile, per diodi Merged PiN Schottky (MPS) in SiC. Il modello circuitale descrive con buona accuratezza la conduzione in polarizzazione diretta, includendo la dipendenza da temperatura e geometria, l'auto-riscaldamento e il fenomeno di *snapback*, come verificato mediante simulazioni TCAD. Nell'ambito dello stesso filone di ricerca è stata condotta una campagna sperimentale, con successiva analisi dei fallimenti, su diodi SiC Junction Barrier Schottky (JBS) da 1.2 kV, finalizzata all'ottimizzazione del bonding a filo a livello *die* per incrementare la massima corrente sostenibile in condizioni di *sovracorrente*.

Il secondo filone introduce un concetto innovativo di MOSFET SiC *Gate-All-Around* (GAA) da 1.2 kV, studiato tramite simulazioni TCAD statiche, dinamiche ed elettrotermiche in modalità mista. La struttura proposta, a simmetria cilindrica, permette di ottenere una distribuzione uniforme del campo elettrico senza ricorrere a una regione di terminazione, migliorando il compromesso tra resistenza specifica di conduzione e tensione di blocco. Tuttavia, l'isolamento a 360° di diossido di silicio limita lo smaltimento termico, rendendo critici gli eventi di corto circuito. Come possibile soluzione, nell'ultima parte della tesi si studia l'integrazione, nell'ossido di gate, di uno strato di materiale ferroelettrico in grado di limitare la corrente e il conseguente auto-riscaldamento durante i transitori di corto circuito.

Parole chiave: carburo di silicio, MPS, JBS, SPICE, elettrotermico, auto-riscaldamento, *snapback*, *sovracorrente*, bonding a filo, MOSFET GAA, simulazioni TCAD, corto circuito, affidabilità, ferroelettrico.

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List of Acronyms

The following acronyms are used throughout the thesis.

TCAD	Technology Computer-Aided Design
MPS	Merged PiN Schottky
JBS	Junction Barrier Schottky
SGAA	SiC Gate All Around

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List of Symbols

The following symbols are used within the thesis

ε_0 Vacuum permittivity [F/m]

h Planck constant [J · s]

k Boltzmann constant [J/K]

m_0 Electron rest mass [kg]

q Elementary charge [C]

Chapter 1

Introduction

Modern society is increasingly dependent on electrical systems for comfort, transportation, and healthcare. This growing dependence has driven significant advancements in power generation, distribution, and management technologies—developments that are closely tied to improvements in the performance of power semiconductor devices, which regulate and control the flow of electricity. Following the replacement of vacuum tubes with solid-state devices in the 1950s, the industry relied heavily on silicon bipolar devices such as bipolar power transistors and thyristors. Although these components quickly achieved higher ratings to meet a broadening range of applications, they suffered from inherent limitations: the need for complex control and protection circuits often resulted in bulky and costly system designs. The introduction of MOS technology for digital electronics in the 1970s paved the way for a new class of devices for power-switching applications—silicon power MOSFETs. These devices became widely adopted in high-frequency applications with relatively low operating voltages (typically below 100 V). In the 1980s, the integration of MOS and bipolar device physics led to the emergence of hybrid devices, among which the insulated-gate bipolar transistor (IGBT) proved the most impactful. Providing high power density, simple drive requirements, and robustness, the IGBT rapidly became the preferred choice for medium- and high-power applications, with the notable exception of high-voltage direct current (HVDC) transmission systems. Even in these high-power domains, traditional thyristors are increasingly being challenged by MOS-

gated structures.

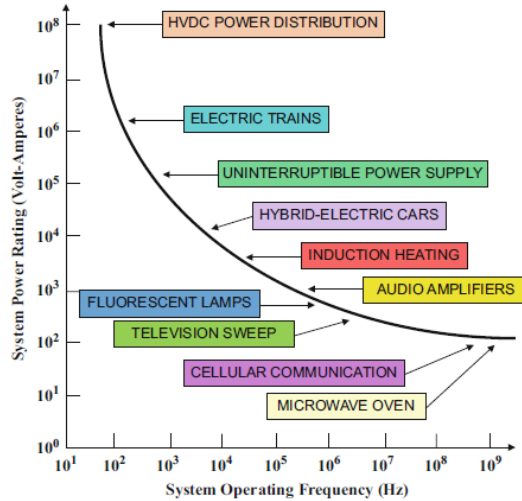


Figure 1.1. Applications for power devices.

Power devices are employed across a wide range of operating power levels and frequencies. As illustrated in Fig. 1.1, high-power systems—such as HVDC distribution networks and locomotive traction drives—operate at relatively low frequencies, often in the megawatt range. As operating frequency increases, the achievable power rating decreases: for example, typical microwave devices handle around 100 W. Currently, all of these application areas are served primarily by silicon-based technologies, with thyristors dominating low-frequency, high-power applications; IGBTs covering medium-frequency, medium-power needs; and power MOSFETs suited for high-frequency, low-power scenarios. An alternative method of classifying power device applications is by their current and voltage handling capabilities, as shown in Fig. 1.2. At the high-power extreme, thyristors can handle voltages exceeding 6000 V and currents over 2000 A, enabling control of more than 10 MW in a single monolithic device—making them ideal for HVDC transmission and traction drive systems. In the 300–3000 V range, where substantial current handling is also required, IGBTs remain the optimal choice. For applications with current requirements below 1 A,

it is often feasible to integrate multiple devices on a single chip, enhancing functionality in systems such as telecommunications and display drivers. When current demands exceed only a few amperes, discrete power MOSFETs combined with appropriate control ICs offer a more cost-effective solution for applications such as automotive electronics and switch-mode power supplies. Despite these advancements, no single device architecture can currently meet the full spectrum of application requirements. This technological gap continues to drive research and innovation in the design, materials, and architectures of next-generation power devices [2].

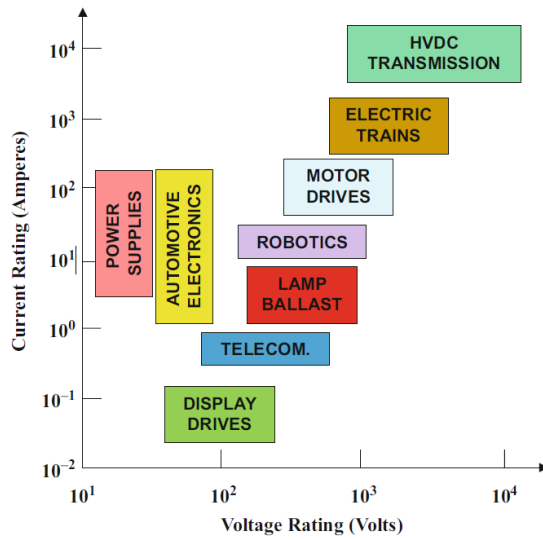


Figure 1.2. System ratings for power devices.

1.0.1 Ideal and Typical Power Device Characteristics

Although silicon power devices have been used in industry for more than five decades, their characteristics deviate significantly from those of an ideal device.

An ideal power rectifier should exhibit the I - V characteristics shown in Fig. 1.3. In forward conduction mode (first quadrant of the figure), it would be able to conduct any amount of current with zero on-state voltage drop. In reverse blocking mode (third quadrant of the figure), it would be capable of sustaining any reverse voltage with zero leakage current. Furthermore, an ideal rectifier would switch between the on-state and the off-state instantaneously, with zero switching time.

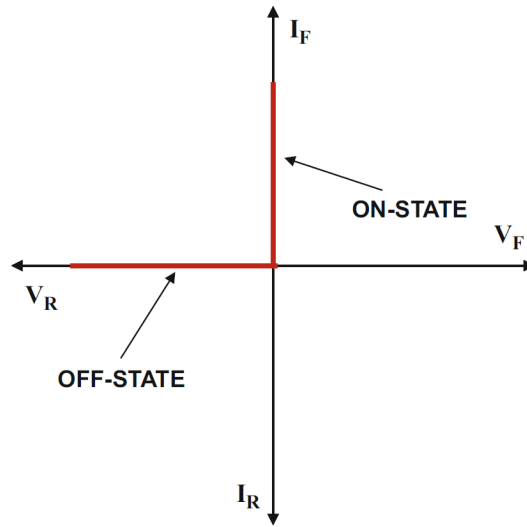


Figure 1.3. Characteristics of an ideal rectifier.

In practice, however, silicon power rectifiers display the non-ideal I - V characteristics illustrated in Fig. 1.4. In the on-state, they exhibit a finite voltage drop (V_{ON}), which results in conduction losses. In the off-state, they allow a finite leakage current (I_{OFF}) while blocking voltage, leading to additional power losses. Moreover, the doping concentration and thickness of the drift region must be carefully engineered to achieve a target breakdown voltage (BV). Increasing the breakdown voltage generally raises

power dissipation, as the on-state voltage drop also increases with voltage rating.

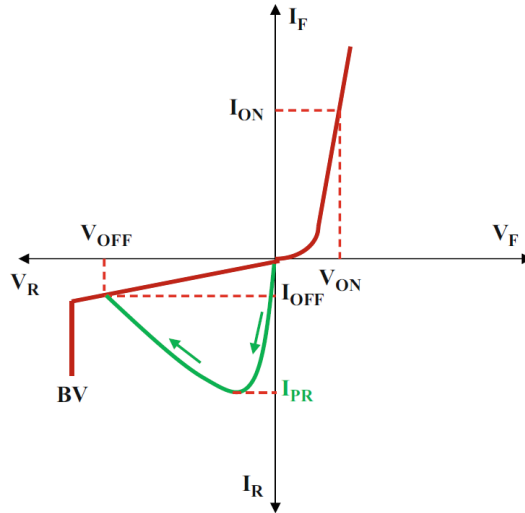


Figure 1.4. Characteristics of a typical rectifier.

The I - V characteristics of an ideal power switch are shown in Fig. 1.5. As with the rectifier, the ideal transistor would conduct current in the on-state with zero voltage drop and block voltage in the off-state with zero leakage current. In addition, it could operate at high current and voltage in the active region, where the forward current is controlled by the applied gate bias. In this ideal case, the spacing between the output characteristics in the active region would be uniform, indicating a gain independent of both current and voltage.

In contrast, the I - V characteristics of a practical power switch, illustrated in Fig. 1.6, deviate from this ideal behavior. A real transistor has a finite on-state resistance and a finite off-state leakage current (not shown in the figure, as it is much smaller than the on-state current). Its breakdown voltage is also limited, as indicated by BV in the figure. However, it can still operate at high currents and voltages in the active region. For a bipolar transistor, the current is controlled by the base current, whereas for a MOSFET or IGBT it is controlled by the gate voltage. The latter approach is generally preferred, as gate-voltage control allows integration of

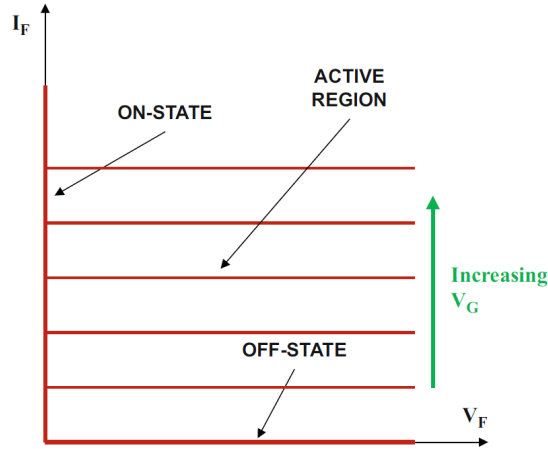


Figure 1.5. Characteristics of an ideal transistor.

the drive circuit, reducing overall cost. Unlike the ideal case, however, the spacing of the output characteristics in the active region is non-uniform. In devices operating in the current saturation mode with channel pinch-off, the behavior follows a square-law relationship.

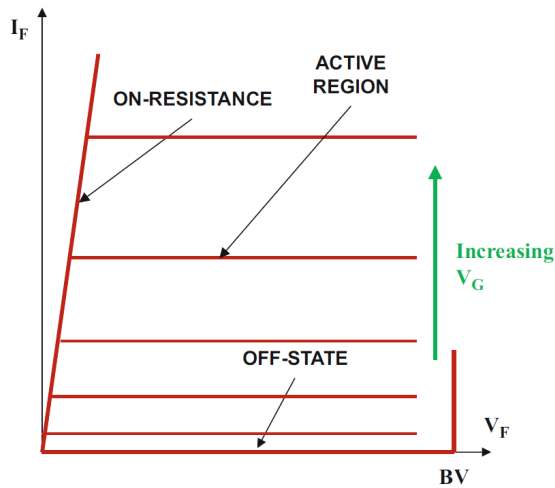


Figure 1.6. Characteristics of a typical transistor.

1.0.2 Efficiency and Switching Aspects of Unipolar and Bipolar Conduction

Bipolar power devices operate through the injection of minority carriers during on-state current conduction. When switching from the on-state to the off-state, these carriers must be removed. This occurs either through charge extraction by the gate drive current or through electron-hole recombination. However, both mechanisms introduce significant power losses that reduce overall power management efficiency. For this reason, unipolar current conduction is generally preferred in power devices. The most common unipolar power diode structure is the Schottky rectifier, which achieves current rectification through a metal–semiconductor barrier. In high-voltage Schottky rectifiers, a drift region is also incorporated, as illustrated in Fig. 1.7, to support the reverse blocking voltage. However, the electrical resistance of the drift region R_S increases rapidly with a higher blocking voltage capability, as will be discussed later in this chapter. Commercial silicon Schottky rectifiers are available with blocking voltages up to approximately 100 V. Beyond this limit, their on-state voltage drop becomes prohibitively high for practical applications. For higher breakdown voltage requirements, silicon P-i-N rectifiers are typically employed, as they provide a lower on-state voltage drop despite their slower switching speed. As will be shown in the following chapters, silicon carbide (SiC) Schottky rectifiers offer a significant advantage: their drift region resistance is much lower than that of their silicon counterparts, enabling the design of very high-voltage devices with reduced on-state voltage drop.

1.0.3 Ideal Drift Region

All unipolar power devices described above include a drift region, specifically designed to sustain the blocking voltage. The characteristics of this region, namely, its doping concentration and thickness, can be analyzed by considering an idealized abrupt junction profile, with a highly doped region on one side and a uniformly low-doped region on the other. In this analysis, junction curvature effects are neglected by assuming a parallel-plane configuration. The resistance of the ideal drift region can thus be directly related to the fundamental properties of the semiconductor. The solution of Poisson's equation yields a triangular electric field distribution within a

Schottky Contact Metal

ANODE



CATHODE

Ohmic Contact Metal

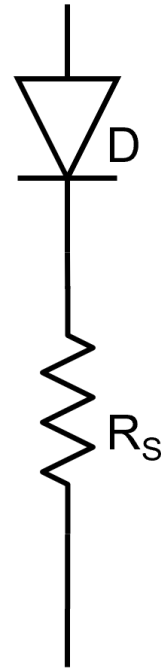


Figure 1.7. Schematic of power schottky rectifier structure and its equivalent circuit.

uniformly doped drift region, where the slope of the field profile is determined by the doping concentration. The maximum voltage that the drift region can sustain is reached when the maximum electric field (E_M) equals the critical electric field (E_C) for the breakdown of the semiconductor material. The critical electric field and the doping concentration together define the maximum depletion width (W_D). The specific resistance (i.e., resistance per unit area) of the ideal drift region is then expressed as:

$$R_{ON} = \frac{W_D}{q\mu_n N_D} \quad (1.1)$$

Since this resistance was initially considered to be the lowest value achievable with silicon devices, it has historically been referred to as the ideal specific on-resistance of the drift region. The depletion width under breakdown conditions is given by:

$$W_D = \frac{2BV}{E_C} \quad (1.2)$$

where BV is the desired breakdown voltage. The doping concentration in the drift region required to obtain this breakdown voltage is given by:

$$N_D = \frac{\varepsilon_s E_C^2}{2qBV} \quad (1.3)$$

Combining these relationships, the specific resistance of the ideal drift region is obtained:

$$R_{ON-IDEAL} = \frac{4BV^2}{\varepsilon_s \mu_n E_C^3} \quad (1.4)$$

The denominator of this last equation is commonly referred to as Baliga's figure of merit for power devices. This figure provides a measure of how the intrinsic properties of a semiconductor material influence the resistance of the drift region.

The resistance of the drift region depends on the carrier mobility considered here for electrons, since their mobility is generally higher than that of holes. This dependence favors semiconductors such as gallium arsenide (GaAs). However, the much stronger cubic dependence of the on-resistance on the critical electric field for breakdown favors wide-band gap semicon-

ductors such as silicon carbide (SiC) [1]. The critical electric field itself is determined by the impact ionization coefficients of holes and electrons, as will be discussed in the next chapter.

Figure 1.8 illustrates how the specific on-resistance of the drift region varies with both the carrier mobility and the critical electric field, for a breakdown voltage of 1000 V. In the figure, the characteristic values for silicon (Si), gallium arsenide (GaAs), and silicon carbide (SiC) are marked.

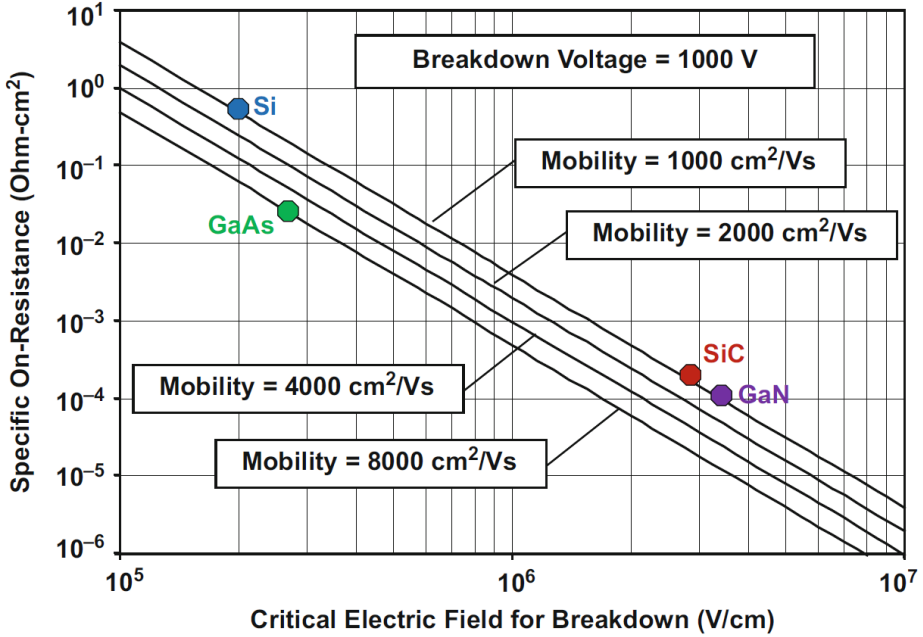


Figure 1.8. Specific on-resistance vs critical electric field.

The improvement in drift region resistance observed in GaAs compared to silicon is mainly due to its much higher electron mobility. In contrast, the superior performance of SiC is primarily a result of its significantly higher critical breakdown field. Based on these considerations, GaAs enabled the development of high-voltage Schottky rectifiers in the 1980s. Even greater performance improvements, however, are clearly predicted for SiC devices—an area that forms the central subject of this work. Interest in the development of power devices from wide-bandgap semicon-

ductors, including gallium nitride (GaN), continues to grow.

1.1 Introduction Summary and Thesis Objectives

In this introductory chapter, we outlined the application domain of power semiconductor devices and examined the key design and process parameters affecting both static and dynamic performance. We introduced Baliga's Figure of Merit, which highlights how the intrinsic properties of a semiconductor material influence the resistance of the drift region.

A second fundamental approach to enhancing these trade-offs lies in the development of novel device architectures. This approach is closely linked to the ability not only to refine but also to invent and standardize new technological processes that enable increasingly high-performance designs.

The two main research topics addressed in this dissertation stem directly from these two approaches and can be summarized as follows:

1. The development of a lumped-parameter compact model for the description of the forward behavior of silicon carbide (SiC) Merged PiN Schottky (MPS) diodes. This model, for the first time, accounts for the snapback effect and proposes a physically based interpretation of this phenomenon within a circuit-level framework.
2. The study and analysis of a novel concept of a cylindrical SiC power MOSFET with a gate-all-around (GAA) structure.

Before addressing the circuit-level modeling of MPS diodes in the following chapters, Chapter 2 summarizes the most important physical and electrical properties of silicon carbide. Chapters 3 and 4 then review the fundamental structures of PiN and Schottky diodes, respectively. Finally, Chapter 5 presents the Junction Barrier Schottky (JBS) and Merged PiN Schottky (MPS) structures, together with the lumped-parameter model mentioned above.

In the last chapter (Chapter 6), the basic concepts related to the design of SiC power MOSFETs are briefly introduced, followed by an overview of the state of the art of existing MOSFET technologies. The chapter concludes with the results of the study carried out on the cylindrical gate-all-around SiC power MOSFET concept.

Chapter 2

SiC: Material Properties

Silicon carbide (SiC) is a wide-bandgap semiconductor, commercially available as monocrystalline wafers with diameters between 50 and 150 mm. Among its various polytypes, the 3C, 6H, and 4H structures are most relevant for electronic applications, exhibiting bandgaps ranging from 2.9 to 3.2 eV. The wide bandgap results in a lower intrinsic carrier concentration at room temperature compared to silicon. Combined with its higher thermal conductivity (4.9 vs. 1.5 W/cm·K), greater dielectric strength, and higher electron saturation velocity, SiC is particularly well suited for high-temperature, high-voltage, and high-power applications, offering substantial efficiency improvements over silicon-based devices. The first commercial SiC devices were Schottky diodes (2001), valued for their negligible reverse recovery and reliable operation above 150 °C. Their low switching losses quickly established them as key components in advanced power conversion circuits. The first controllable devices, SiC JFETs, appeared around 2008–2011, though technological challenges—particularly related to gate oxide quality—delayed the introduction of SiC MOSFETs. JFETs, being normally-on devices, were considered unsuitable for power applications, leading to cascode solutions with Si MOSFETs. Attempts with SiC BJTs were also limited by strong dependence on material quality. In 2011, Cree released the first commercial 1200 V SiC MOSFETs, marking a turning point. Since then, the SiC device market has grown rapidly, exceeding €200M by 2015 with projected annual growth rates of 20%. SiC MOSFETs are expected to dominate the market thanks to their combination of high

breakdown voltage capability, low on-resistance (scaling inversely with the cube of the critical electric field), robustness, and high-temperature operation. These features not only improve efficiency but also reduce cooling requirements and increase device lifetime [1].

2.1 Fundamental Properties

This section summarizes the fundamental properties of silicon carbide and compares them with those of silicon. The analysis focuses on the 4H polytype, whose characteristics are superior to those of the 6H and 3C polytypes. The material properties most relevant for power devices include the energy bandgap, impact ionization coefficients, dielectric constant, thermal conductivity, electron affinity, and carrier mobility. From these parameters, both the intrinsic carrier concentration and the built-in potential can be derived; their values are also calculated here and compared with the corresponding values for silicon (Table 2.1).

Table 2.1. Si Vs SiC

Properties	Silicon	4H-SiC
Energy Bandgap (eV)	1.1	3.2
Relative Dielectric Constant	11.7	9.7
Thermal Conductivity (W/cmK)	1.5	3.7
Electron Affinity (eV)	4.05	3.7
Density of States Conduction Band (cm^{-3})	2.80×10^{19}	1.23×10^{19}
Density of States Valance Band (cm^{-3})	1.04×10^{19}	4.58×10^{18}

2.1.1 Energy Bandgap

The energy bandgap of silicon carbide (SiC) is much larger than that of silicon, which allows SiC to be classified as a wide-bandgap semiconductor. For 4H-SiC, the bandgap is $E_G = 3.26$ eV—about three times larger than that of silicon—while for 6H-SiC it is slightly smaller, at 3.0 eV. A wider bandgap reduces carrier generation in the depletion regions of devices, thereby lowering the leakage current in P–N junctions designed to sustain high voltages. It also enables the formation of metal–semiconductor

contacts with higher Schottky barrier heights, further reducing leakage currents in Schottky rectifiers and MESFETs.

The intrinsic carrier concentration is determined by the thermal generation of electron–hole pairs across the bandgap. It can be calculated using the mass-action law, which holds under thermodynamic equilibrium (i.e., steady-state conditions in the absence of electrical or optical excitation):

$$n_i = \sqrt{N_C N_V} e^{-E_G/2kT} \quad (2.1)$$

where E_G is the bandgap energy, N_C and N_V are the effective density of states in the conduction and valence bands, respectively, k is Boltzmann’s constant (1.38×10^{-23} J/K), and T is the absolute temperature.

For silicon, the intrinsic carrier concentration is:

$$n_i \approx 1.4 \times 10^{10} \text{ cm}^{-3} \quad \text{at } 300 \text{ K} \quad (2.2)$$

whereas for 4H-SiC it is:

$$n_i \approx 6.7 \times 10^{-8} \text{ cm}^{-3} \quad \text{at } 300 \text{ K} \quad (2.3)$$

This vast difference demonstrates that bulk generation currents play a negligible role in determining leakage current in SiC devices, although surface generation currents may still be significant due to interface states within the bandgap.

The intrinsic carrier concentration can also be expressed as a function of temperature. Figures 2.1 and 2.2 illustrate this dependence: Figure 2.1 uses the conventional inverse temperature scale, while Figure 2.2 provides a direct temperature scale for easier interpretation. As shown, the intrinsic carrier concentration in silicon increases rapidly with temperature, reaching a typical doping level of $1 \times 10^{15} \text{ cm}^{-3}$ at just 540 K (267°C). In contrast, for 4H-SiC the concentration remains extremely low—even at 700 K (427°C) it is only $3.9 \times 10^7 \text{ cm}^{-3}$.

As is well known, the built-in voltage of a P–N junction is given by:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A^+ N_D^-}{n_i^2} \right) \quad (2.4)$$

where N_A^+ and N_D^- are the ionized acceptor and donor concentrations

on either side of the junction. In silicon, these concentrations are effectively equal to the doping levels, since dopant ionization energies are small. In silicon carbide, however, this assumption no longer holds because dopants exhibit much higher ionization energies. This effect, known as *incomplete ionization*, will be discussed later in this chapter. So in summary, the wide bandgap of silicon carbide, which also results in a lower intrinsic carrier concentration, leads to significantly reduced leakage currents, but on the other hand, the wide bandgap also increases the built-in voltage (as can be easily seen from equation 8), causing a higher forward voltage drop across the P–N junction. For this reason, as will be discussed in the following chapters, device architectures such as Schottky, Junction Barrier Schottky (JBS), and Merged PiN Schottky (MPS) structures are often preferred in silicon carbide technology [1].

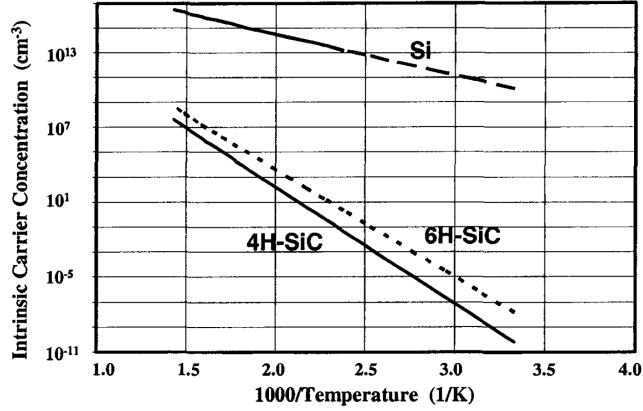


Figure 2.1. Intrinsic carrier concentration Vs 1000/Temperature.

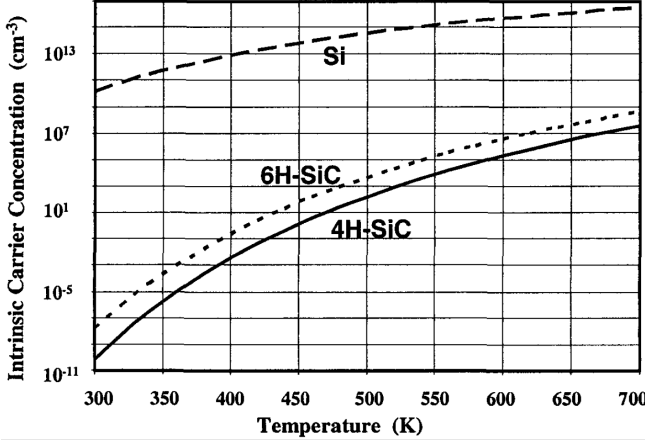


Figure 2.2. Intrinsic carrier concentration Vs Temperature.

2.1.2 Impact ionization coefficients

The primary advantage of wide bandgap semiconductors in power device applications lies in their ability to sustain much higher breakdown voltages. This enhanced capability is directly linked to the significantly lower impact ionization coefficients of these materials compared to silicon, for a given electric field [1]. The dependence of the impact ionization rate on the electric field is generally described by Chynoweth's Law:

$$\alpha = a \times e^{-b/E} \quad (2.5)$$

where E is the electric field component along the direction of current flow, while a and b are material- and temperature-dependent constants. For silicon, the ionization rate of electrons is much higher than that of holes. In contrast, experimental results on silicon carbide have revealed the opposite trend, with holes exhibiting higher ionization rates than electrons. In the case of silicon, the measured coefficients as a function of electric field and temperature can be modeled with values of $a = 7 \times 10^5 \text{ cm}^{-1}$ and $b = 1.23 \times 10^6 \text{ V/cm}$ at room temperature. For 4H-SiC, the impact ionization coefficients have been more recently determined using electron-beam excitation techniques. This approach enabled accurate extraction of ionization rates in defect-free regions by identifying and excluding defec-

tive areas through EBIC (Electron Beam Induced Current) imaging. This distinction was essential, since measurements taken at defect sites showed substantially higher ionization rates. For defect-free 4H-SiC, the extracted parameters for hole ionization were:

$$a(4H - SiC) = 6.46 \times 10^6 - 1.07 \times 10^4 T \quad (2.6)$$

$$b(4H - SiC) = 1.75 \times 10^7 \quad (2.7)$$

$$a(6H - SiC) = 4.6 \times 10^6 - 7.4 \times 10^3 T \quad (2.8)$$

$$b(6H - SiC) = 1.5 \times 10^7 \quad (2.9)$$

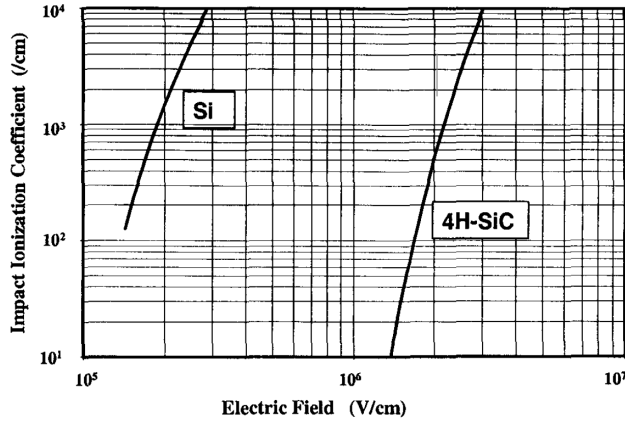


Figure 2.3. Impact Ionization Coefficients in 4H-SiC and Silicon.

A direct comparison of 4H-SiC and silicon (see Fig. 2.3) highlights that significant carrier generation by impact ionization begins only at much higher electric fields in 4H-SiC. Consequently, breakdown in 4H-SiC devices occurs at fields on the order of $2 - 3 \times 10^6 \text{ V/cm}$, nearly an order of magnitude greater than in silicon. This translates into a much higher critical electric field E_C for breakdown in 4H-SiC, which in turn yields a substantial increase in Baliga's Figure of Merit (BFOM) [1]. The implica-

tions of this higher critical electric field are explored in greater detail in the following chapter.

2.1.3 Carriers Mobility

In this subsection, we highlight the differences in carrier mobility between silicon carbide (SiC) and silicon. A simplified treatment of carrier mobility is first provided, followed by a focus on the main distinctions between these two semiconductor materials.

Carrier mobility is a parameter that quantifies the ability of a charge carrier to move through the crystal lattice under the influence of an electric field:

$$\vec{v}_d = \boldsymbol{\mu} \cdot \vec{E} \quad (2.10)$$

where $\vec{v}_d$ is the drift velocity vector, $\vec{E}$ is the electric field vector, and $\boldsymbol{\mu}$ is the mobility tensor.

In the particular case where the electric field and drift velocity are aligned—or more specifically, in isotropic semiconductor materials—the tensor reduces to a scalar quantity, and mobility can be expressed as:

$$\mu = \frac{v_d}{E} \quad (2.11)$$

Under typical operating conditions of semiconductor devices, the most important scattering mechanisms affecting mobility are:

- Phonon scattering
- Ionized impurity scattering

For devices such as surface-channel MOSFETs, where current conduction occurs near the semiconductor–insulator interface, a third mechanism becomes relevant:

- Interface scattering

All these contributions can be considered simultaneously using *Matthiessen's rule*:

$$\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{\text{ph}}} + \frac{1}{\mu_{\text{imp}}} + \frac{1}{\mu_{\text{int}}} + \dots \quad (2.12)$$

where μ_{ph} is the phonon-limited mobility, μ_{imp} the mobility limited by ionized impurities, and μ_{int} the interface-limited mobility [4].

As in silicon, in silicon carbide the electron mobility is significantly higher than the hole mobility. It is therefore advantageous to design unipolar devices using N-type drift regions rather than P-type drift regions.

The electron mobility at room temperature is plotted in Fig. 2.4 as a function of doping concentration for both silicon and silicon carbide. In both materials, mobility decreases with increasing doping due to enhanced Coulombic scattering from ionized impurities.

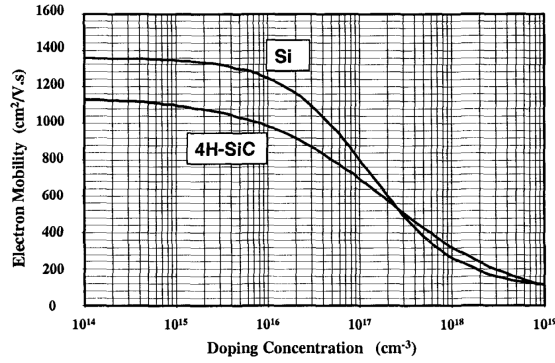


Figure 2.4. mobility Vs doping concentration [1].

With regard to temperature dependence, in the range from 300 K to 500 K, mobility decreases in both silicon and silicon carbide. This occurs because the phonon-scattering contribution (which has a negative temperature coefficient) dominates over the ionized impurity scattering contribution (which has a positive temperature coefficient). This behavior is clearly illustrated in Fig. 2.5.

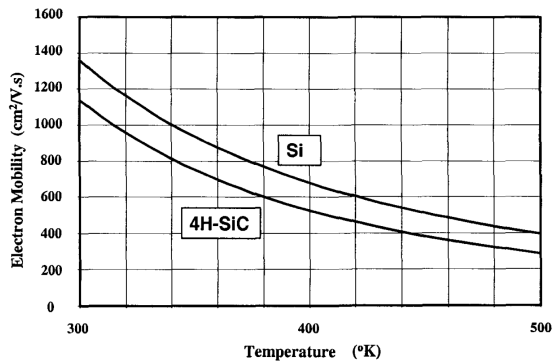


Figure 2.5. Mobility Vs Temperature [1].

2.1.4 Donor and Acceptor Ionization Energy Levels

The ionization of dopant atoms at a given temperature can be either complete or incomplete, depending on whether all dopant atoms have successfully donated (N-type) or accepted (P-type) electrons. In silicon, dopants are almost fully ionized at room temperature because their ionization energies are relatively small compared to the conduction-band edge (for donors) or the valence-band edge (for acceptors). However, below approximately 120 K, silicon is no longer completely ionized. This temperature range is known as the freeze-out regime.

In contrast, silicon carbide (SiC) exhibits incomplete ionization even at room temperature, due to the significantly higher ionization energies of its dopants. As a result, only a fraction of the dopant atoms contribute free carriers to the semiconductor. In particular, dopants with deep ionization levels—located more than about five times the thermal energy away from the conduction or valence band edges—remain “frozen” within the bandgap and are not thermally activated. These deep-level impurities can act as recombination centers where electrons and holes annihilate each other. The most common donor atoms in SiC are nitrogen and phosphorus. Nitrogen typically substitutes carbon atoms, while phosphorus replaces silicon atoms. The most common acceptors are aluminum and boron, both of which substitute silicon atoms. The exact energy level of a given dopant in SiC depends on the polytype. Moreover, because nearly all SiC polytypes contain both cubic and hexagonal lattice sites, the same dopant species

usually produces multiple ionization levels—one for each inequivalent site. The only exceptions are 3C-SiC and 2H-SiC, which are purely cubic and hexagonal, respectively. For bipolar devices, the incomplete ionization of dopants in SiC strongly affects the temperature dependence of their electrical characteristics. Therefore, in the design and simulation of SiC-based devices, an appropriate incomplete ionization model must be used, taking into account both dopant concentration and polytype.

2.1.5 Recombination Lifetimes

In silicon, high-voltage devices exploit minority-carrier injection into the drift region to lower resistivity through conductivity modulation. However, recombination of carriers—often mediated by deep levels—affects switching speed and can also generate leakage current under reverse bias. In contrast, for silicon carbide, power switching applications are limited to unipolar devices, partly because reported carrier lifetimes are short ($10^{-9} - 10^{-7}$ s), with corresponding diffusion lengths of only $1 - 2 \mu\text{m}$, likely influenced by surface recombination. Although bipolar devices such as 4H-SiC PiN rectifiers can achieve higher bulk lifetimes, their large on-state voltage drop and slow switching render them less practical than unipolar structures.

PiN rectifier

Power rectifiers are essential components in power electronic circuits, as they control the direction of current flow. In silicon Schottky barrier rectifiers, the on-state voltage drop becomes prohibitively large when the device is designed to sustain reverse blocking voltages greater than 200 V. However, many applications—such as motor drives—require rectifiers with blocking voltages in the range of 300 to 5000 V. For these conditions, silicon PiN rectifiers have been traditionally employed.

In a PiN rectifier, the reverse blocking voltage is sustained across the depletion region of a P–N junction, with most of the voltage supported by the N-type drift layer. To achieve high blocking capability, this drift region must be thick and lightly doped, while the P-type region is optimized to facilitate forward conduction. In silicon devices, high-level injection of minority carriers into the drift region plays a key role, as it drastically reduces the resistivity of the thick, low-doped layer. This conductivity modulation allows substantial forward current flow despite the weak doping. Additionally, punch-through designs can further reduce the drift region thickness, lowering the on-state voltage drop.

In contrast, silicon carbide (SiC) rectifiers rely on very different design principles. Owing to the much higher critical electric field of SiC, the drift region can be made thinner and more heavily doped while still achieving very high breakdown voltages. As a result, 4H-SiC Schottky rectifiers with reverse blocking capabilities of up to 3000 V can be realized with relatively low on-state voltage drops. Thanks to their inherently fast switching speed,

SiC Schottky rectifiers are expected to increasingly replace silicon PiN rectifiers in applications requiring blocking voltages up to 3000 V.

Commercial progress has already been made: SiC junction barrier Schottky (JBS) rectifiers with blocking voltages of 600–1200 V are now available and widely used as flyback rectifiers in inverters in combination with silicon IGBTs. Nonetheless, a complete replacement of silicon PiN rectifiers will depend on further reductions in the manufacturing cost of SiC technology. Until then, silicon PiN rectifiers will continue to play an important role, especially in applications where cost competitiveness remains a priority

3.1 Basic Principles Of PiN Rectifier

As the name suggests, PiN diodes consist of three regions: a heavily doped p-type region, a lightly doped n-type region (often referred to as the *epi-layer* or drift region), and a heavily doped n^+ cathode region that ensures a good ohmic contact between the semiconductor and the metal (Fig. 3.1 c). The central region is often referred to as “intrinsic,” although more accurately its doping concentration is several orders of magnitude lower than that of the outer regions.

Compared to unipolar devices, PiN diodes exhibit a lower on-state resistance (R_{ON}). This characteristic is primarily due to the phenomenon of *conductivity modulation*, which occurs when a large number of minority carriers are injected into the low-doped drift region. Although this reduces the effective resistance R_{ON} , the drift region still contributes significantly to the total voltage drop across the device, which can be expressed as:

$$V_{PIN} = V_{AE} + V_{EC} + I \cdot R_{ON} \quad (3.1)$$

where V_{PIN} is the total voltage drop across the device, V_{AE} is the voltage drop across the anode–epi junction, and V_{EC} is the drop across the epi–cathode junction.

Thus, the structure of a PiN diode can be summarized as:

- a heavily doped P^+ region at the anode,
- a lightly doped N^- drift region (epi-layer),

- a heavily doped N^+ cathode region.

Unlike signal diodes, PiN diodes are designed to withstand high reverse blocking voltages. Considering a one-sided abrupt junction (such as the anode–epi junction), under reverse bias the width of the space-charge region (W) is given by:

$$W \simeq W_{\text{epi}} \simeq \sqrt{\frac{2\varepsilon_s(V_{\text{BI}} + V_R)}{qN^-}} \quad (3.2)$$

where W_{epi} is the extension of the depletion region into the epi-layer (under reverse bias $W \approx W_{\text{epi}}$), ε_s is the semiconductor dielectric constant, N^- is the doping concentration of the drift region, q is the electron charge, V_{BI} is the built-in potential, and V_R is the applied reverse voltage.

At breakdown voltage BV (with $BV \gg V_{\text{BI}}$), this simplifies to:

$$W \simeq \sqrt{\frac{2\varepsilon_s BV}{qN^-}} \quad (3.3)$$

The corresponding critical electric field is:

$$|E_C| = W_{\text{epi}} \frac{qN^-}{\varepsilon_s} \simeq \sqrt{\frac{2qBVN^-}{\varepsilon_s}} \quad (3.4)$$

From which the breakdown voltage can be expressed as:

$$BV \simeq \frac{E_C^2 \varepsilon_s}{2qN^-} \quad (3.5)$$

From this expression, it is straightforward to infer that increasing the breakdown voltage can be effectively achieved by decreasing the doping concentration in the N^- epi-layer. Assuming the same applied voltage across the diode, the absolute value of the area under the electric field $E(x)$ in the space-charge region (SCR) must remain constant as N^- decreases. Consequently, the SCR will extend further into the epi-layer and shrink within the heavily doped anode region (as illustrated in Fig. 3.1 b) and expressed by the equations 23-24). As a result, the absolute peak value of the electric field E_{max} will decrease (see Eq. 24). Ultimately, it becomes clear that, with a lower N^- , a higher breakdown voltage BV is required

in order to reach the critical electric field value

$$W_{\text{epi}} \simeq \sqrt{\frac{2\varepsilon_s(V_{\text{BI}} + V_R)}{qN^-}} \quad (3.6)$$

$$W_{\text{anode}} \simeq \sqrt{\frac{2\varepsilon_s(V_{\text{BI}} + V_R)}{q}} \cdot \sqrt{\frac{N^-}{(P^+)^2}} \quad (3.7)$$

with the corresponding maximum electric field:

$$|E_{\text{max}}| = \frac{qP^+W_{\text{anode}}}{\varepsilon_s} \quad (3.8)$$

If the drift doping N^- is sufficiently low, the space-charge region may extend beyond the epi-layer, leading to full depletion. In this case, the electric field is effectively confined between the anode–epi and epi–cathode junctions. A second design strategy to improve breakdown performance is therefore to increase the thickness of the epi-layer, which reduces the peak electric field and requires a higher applied reverse voltage to reach $|E_C|$ (Fig. 3.1 a). Ultimately, in the design of the drift region, both the thickness and the doping concentration must be carefully optimized to balance the trade-off between forward voltage drop and breakdown voltage.

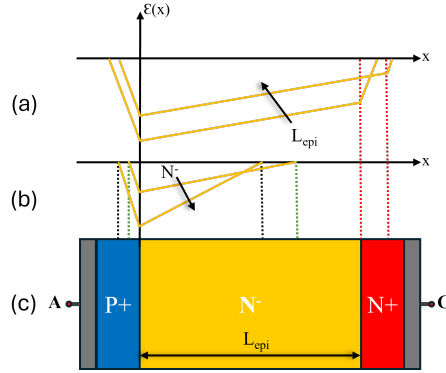


Figure 3.1. (a) Electric field under punch-through conditions by varying epi-thickness, (b) electric field by varying epi-doping concentration, (c) schematic 2-D structure of PiN rectifiers.

3.2 Recombination Rate and Carrier Lifetime

Shockley, Read, and Hall derived the expression of the recombination rate U_{SRH} under the assumption of exciting an indirect bandgap N -type semiconductor with incident optical radiation fulfilling the absorption condition. It is worth noting that, in deriving this expression, the well-known Fermi-Dirac distribution was not employed (since the system is not at thermodynamic equilibrium). Instead, an alternative expression for the occupancy probability F was obtained through the steady-state balance condition under optical excitation:

$$R_a - R_b = R_c - R_d \quad (3.9)$$

where R_a, R_b, R_c, R_d [$\text{cm}^{-3}\text{s}^{-1}$] represent, respectively: - the capture rate of a free electron from the conduction band by the G-R center, - the emission rate of an electron from the center into the conduction band, - the emission rate of an electron from the center into the valence band, - the capture rate of a hole from the valence band by the center. These terms can be expressed as:

$$R_a = \sigma_n v_{th,n} n_n N_T (1 - F) \quad (3.10)$$

$$R_b = e_n N_T F \quad (3.11)$$

$$R_c = \sigma_p v_{th,p} p_n N_T F \quad (3.12)$$

$$R_d = e_p N_T (1 - F) \quad (3.13)$$

Here, σ_n and σ_p [cm^2] are the electron and hole capture cross-sections of the G-R centers; $v_{th,n}$ and $v_{th,p}$ [ms^{-1}] are the thermal velocities of electrons and holes, respectively; N_T [cm^{-3}] is the trap concentration; e_n and e_p [s^{-1}] are the electron and hole emission rates; and n_n and p_n [cm^{-3}] denote the concentrations of free electrons and holes in an N -type semiconductor.

Once the probability F is determined from the balance condition above, the recombination rate U_{SRH} can be expressed as the net difference $R_a - R_b$. After straightforward algebraic manipulation, one obtains:

$$U_{SRH} = \frac{n_n p_n - n_i^2}{\tau_{pn}(n_n + n_1) + \tau_{np}(p_n + p_1)} \quad (3.14)$$

This expression, valid for indirect bandgap semiconductors, is independent of the doping polarity. Hence, it can be written in a more general form:

$$U_{SRH} = \frac{np - n_i^2}{\tau_{pn}(n + n_1) + \tau_{np}(p + p_1)} \quad (3.15)$$

where

$$\tau_{pn} = \frac{1}{\sigma_p v_{th,p} N_T}, \quad \tau_{np} = \frac{1}{\sigma_n v_{th,n} N_T} \quad (3.16)$$

represent, respectively, the average hole lifetime in an N -type semiconductor and the average electron lifetime in a P -type semiconductor.

The parameters n_1 and p_1 are defined as:

$$n_1 = N_C e^{-\frac{E_C - E_T}{kT}} = n_i e^{\frac{E_T - E_i}{kT}}, \quad p_1 = N_V e^{-\frac{E_T - E_V}{kT}} = n_i e^{\frac{E_i - E_T}{kT}} \quad (3.17)$$

where N_C and N_V denote the effective density of states in the conduction band and in the valence band, respectively. while n_1 and p_1 correspond, respectively, to the electron and hole concentrations at thermodynamic equilibrium when the trap level E_T coincides with the Fermi level.

Introducing the carrier excesses:

$$\Delta n = n - n_0, \quad \Delta p = p - p_0 \quad (3.18)$$

the SRH recombination rate can be reformulated as:

$$U_{SRH} = \frac{\Delta n \Delta p + \Delta n p_0 + \Delta p n_0}{\tau_{pn}(n + n_1) + \tau_{np}(p + p_1)} \quad (3.19)$$

By imposing $\Delta n = \Delta p$, the carrier lifetime can be defined as:

$$\tau = \frac{\Delta n}{U_{SRH}} = \frac{\tau_{pn}(n_0 + n_1 + \Delta n) + \tau_{np}(p_0 + p_1 + \Delta n)}{n_0 + p_0 + \Delta n} \quad (3.20)$$

In an N -type semiconductor, where $n_0 \gg p_0$ at relevant temperatures, this leads to:

$$\frac{\tau}{\tau_{pn}} = \left[1 + \frac{1}{1+h} e^{\frac{E_T - E_i}{kT}} \right] + \zeta \left[\frac{h}{1+h} + \frac{1}{1+h} e^{\frac{2E_i - E_T - E_F}{kT}} \right] \quad (3.21)$$

where h is the normalized injection level:

$$h = \frac{\Delta n}{n_0} \quad (3.22)$$

and ζ is the ratio between the average electron lifetime in a P -type semiconductor and the average hole lifetime in an N -type semiconductor:

$$\zeta = \frac{\tau_{np}}{\tau_{pn}} \quad (3.23)$$

From the previous relation, this can also be expressed as:

$$\zeta = \frac{\sigma_n v_{th,n}}{\sigma_p v_{th,p}} \approx 0.827 \frac{\sigma_n}{\sigma_p} \quad (3.24)$$

At very low injection levels ($h \ll 1$), the lifetime stabilizes at a constant value known as the *low-level lifetime* τ_{LL} . In this case, the expression reduces to:

$$\frac{\tau_{LL}}{\tau_{pn}} = \left[1 + e^{\frac{E_T - E_i}{kT}} \right] + \zeta e^{\frac{2E_i - E_T - E_F}{kT}} \quad (3.25)$$

This shows that τ_{LL} depends exponentially on the trap level E_T and on the ratio of capture cross-sections. The *low-level lifetime* τ_{LL} increases as the recombination center moves away from midgap, reaching a minimum when located at midgap.

From an application standpoint, this observation is critical for the dynamic behavior of PiN diodes: in order to achieve high switching speeds, the excess carriers injected into the drift region must be rapidly removed. This requires a small τ_{LL} , achievable when the G-R centers are located as close as possible to midgap.

Conversely, at high injection levels ($h \gg 1$), the lifetime stabilizes again at a constant value, called the *high-level lifetime* τ_{HL} , and the expression

simplifies to:

$$\frac{\tau_{HL}}{\tau_{pn}} = 1 + \zeta \quad (3.26)$$

3.3 Recombination Current

When the current flowing across the P-N junction is very small, the current transport is dominated by the recombination of carriers within the depletion region of the junction. Now, let us consider the expression of the recombination rate derived by Shockley, Read, and Hall for indirect bandgap semiconductors:

$$U_{SRH} = \frac{np - n_i^2}{\tau_{pn} [(n + n_1) + \zeta(p + p_1)]} \quad (3.27)$$

Referring to the generalized mass-action law, in the depletion region under forward bias we have:

$$n(x)p(x) = n_i^2 e^{\frac{E_{Fn} - E_{Fp}}{kT}} = n_i^2 e^{\frac{qV}{kT}} \quad (3.28)$$

where V is the applied forward-bias voltage, and E_{Fn} , E_{Fp} are the electron and hole quasi-Fermi levels, respectively. From this relation, it follows that:

$$n(x)p(x) > n_i^2 \quad \forall x \in [-x_p, x_n] \quad (3.29)$$

where $[-x_p, x_n]$ denotes the spatial limits of the SCR (Fig. 4.1). This validates the earlier hypothesis and implies that $U_{SRH} > 0$. Therefore, the following relations must hold:

$$J_{pp}(-x_p) > J_{pn}(x_n) \quad (3.30)$$

$$J_{nn}(x_n) > J_{np}(-x_p) \quad (3.31)$$

Considering these results (schematically depicted in Fig. 3.2), and assuming equal electron and hole concentrations (which maximizes the recombination rate), we obtain:

$$n = p = n_i e^{\frac{qV}{2kT}} \quad (3.32)$$

Substituting this into the SRH expression, we get:

$$U_{\max} = \frac{n_i^2 e^{\frac{qV}{kT}} - n_i^2}{\tau_{pn} \left[\left(n_i e^{\frac{qV}{2kT}} + n_1 \right) + \zeta \left(n_i e^{\frac{qV}{2kT}} + p_1 \right) \right]} \quad (3.33)$$

If the recombination-generation centers are highly effective, such that $n_1 \simeq n_i$, $p_1 \simeq n_i$, and under the condition $V \gg \frac{kT}{q}$, the expression simplifies to:

$$U_{\max} \simeq \frac{n_i e^{\frac{qV}{2kT}}}{\tau_{pn}(1 + \zeta)} = \frac{n_i e^{\frac{qV}{2kT}}}{\tau_{SC}} \quad (3.34)$$

Consequently, the recombination current density, assuming a uniform recombination rate within the SCR, maximized with respect to carrier concentration, with G-R centers near midgap and $V \gg \frac{kT}{q}$, can be approximated as:

$$J_R = qU_{\max}W = \frac{qn_iW}{\tau_{SC}} e^{\frac{qV}{2kT}} \quad (3.35)$$

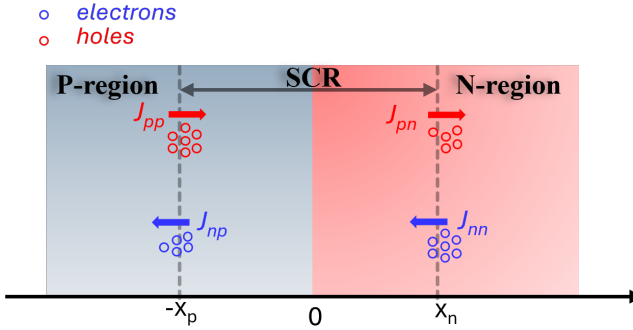


Figure 3.2. Schematic illustration of the current density components within the SCR.

3.4 Low Level Injection

At low injection levels within the drift region (i.e., when the concentration of minority carriers is well below the doping concentration of the drift region), the transport mechanism is governed by the diffusion of injected minority carriers in the (quasi-)neutral regions.

If the drift region is assumed to be long ($L_{pn} \ll W_{\text{drift}}$), the injected holes diffuse across the drift region (while partial recombination may occur). This leads, in the immediate proximity of the edge of the space-charge region (SCR), to a local imbalance of positive charge:

$$p_n(x_n) + N_{\text{drift}} > n_{n0} \quad (3.36)$$

where $p_n(x_n)$ is the minority hole concentration at the SCR boundary, N_{drift} is the donor concentration in the drift region, and n_{n0} is the equilibrium electron concentration in the drift region.

The presence of this excess positive charge generates a local electric field, which induces drift currents of both electrons and holes that oppose the imbalance. In other words, the electric field tends to counteract the very cause of its formation. Nevertheless, since the excess positive charge is quickly compensated by the accumulation of majority carriers, the resulting electric field remains relatively small.

The next step is to determine the distribution of minority carriers in the drift region. To this purpose, we adopt the continuity equation:

$$\frac{\partial p_n}{\partial t} = G_L - U - \frac{1}{q} \frac{\partial J_{pn}}{\partial x} \quad (3.37)$$

Assuming steady-state conditions (i.e., $\partial p_n / \partial t = 0$) and neglecting external generation ($G_L = 0$), the equation simplifies to:

$$-\frac{1}{q} \frac{dJ_{pn}}{dx} = U \quad \longrightarrow \quad -\frac{1}{q} \frac{d}{dx} \left(q\mu_{pn}p_nE - qD_{pn}\frac{dp_n}{dx} \right) \quad (3.38)$$

At low injection levels, the drift term (p_nE) is negligible, hence:

$$D_{pn} \frac{d^2 p_n}{dx^2} = U \quad (3.39)$$

Considering the general Shockley-Read-Hall recombination model and specifying the case of low-level injection with deep traps, while assuming $\tau_{pn} = \tau_{np}$, the recombination rate reduces to:

$$U \approx \frac{\Delta p_n}{\tau_{pn}} \quad (3.40)$$

Thus, the continuity equation becomes:

$$D_{pn} \frac{d^2 p_n}{dx^2} = \frac{\Delta p_n}{\tau_{pn}} \quad (3.41)$$

Recalling that

$$\Delta p_n = p_n - p_{n0} \quad (3.42)$$

$$L_{pn} = \sqrt{D_{pn} \tau_{pn}}, \quad (3.43)$$

we obtain:

$$\frac{d^2 \Delta p_n}{dx^2} = \frac{\Delta p_n}{L_{pn}^2} \quad (3.44)$$

For a sufficiently long drift region, the solution is:

$$\Delta p_n(x) = \Delta p_n(x_n) e^{-\frac{(x-x_n)}{L_{pn}}} \longrightarrow p_n(x) = p_{n0} + \Delta p_n(x_n) e^{-\frac{(x-x_n)}{L_{pn}}} \quad (3.45)$$

At this point, the goal is to derive the current density under the assumptions of low-level injection, long quasi-neutral regions, and the absence of generation-recombination processes inside the depletion region. Under these conditions, the following relations hold:

$$J_{pn}(x_n) = J_{pp}(-x_p) \quad (3.46)$$

$$J_{nn}(x_n) = J_{np}(-x_p) \quad (3.47)$$

Therefore, the total current density can be expressed as:

$$J = J_{nn}(x_n) + J_{pn}(x_n) = J_{np}(-x_p) + J_{pp}(-x_p) \quad (3.48)$$

Since minority-carrier currents are essentially governed by diffusion (the drift contribution being negligible under low injection), we obtain:

$$J \approx J_{pn,\text{diff}}(x_n) + J_{np,\text{diff}}(-x_p) = q \frac{D_{pn}}{L_{pn}} \Delta p_n(x_n) + q \frac{D_{np}}{L_{np}} \Delta n_p(-x_p) \quad (3.49)$$

By recalling the junction law, which relates the minority concentration at the SCR boundaries to the equilibrium concentration and the externally applied bias V , one has:

$$p_n(x_n) \approx p_{n0} e^{\frac{V}{V_T}} \approx \frac{n_i^2}{N_{\text{drift}}} e^{\frac{V}{V_T}} \quad (3.50)$$

Finally, the current density takes the form:

$$J = q \left(\frac{D_{pn}}{L_{pn} N_{\text{drift}}} + \frac{D_{np}}{L_{np} N_{A,\text{anode}}} \right) n_i^2 \left(e^{\frac{V}{V_T}} - 1 \right) \quad (3.51)$$

Considering that $N_{A,\text{anode}} \gg N_{\text{drift}}$, the expression reduces to:

$$J \approx q \frac{D_{pn}}{L_{pn} N_{\text{drift}}} n_i^2 \left(e^{\frac{V}{V_T}} - 1 \right) \quad (3.52)$$

3.5 High level Injection

The drift region is lightly doped (sometimes referred to as “intrinsic”), which allows the support of high reverse voltages. When a forward bias is applied, as already discussed, minority carriers are injected into the drift region. As the applied forward voltage increases, the minority carrier concentration inside the drift region rises, eventually reaching and then exceeding the doping concentration in the drift region.

Under these circumstances, charge neutrality requires that the concentrations of holes and electrons are the same:

$$n(x) = p(x) \quad (3.53)$$

At this point, high-level injection is triggered. Therefore, the high concentration of free carriers leads to an increase in the conductivity of

the drift region, significantly enhancing the conduction capability of the device. This phenomenon is referred to as *conductivity modulation*.

The carrier concentration in the drift region can be obtained by solving the continuity equations in steady-state conditions ($\partial n/\partial t = 0$):

$$-\frac{n}{\tau_{HL}} + D_n \frac{\partial^2 n}{\partial x^2} + \mu_n \frac{\partial(nE)}{\partial x} = 0 \quad (3.54)$$

$$-\frac{p}{\tau_{HL}} + D_p \frac{\partial^2 p}{\partial x^2} + \mu_p \frac{\partial(pE)}{\partial x} = 0 \quad (3.55)$$

From the results of equations (above), the current under high-level injection can finally be expressed as:

$$J_T \propto \exp\left(\frac{qV}{2kT}\right) \quad (3.56)$$

3.6 Forward Characteristics

The analysis of current flow in a PiN rectifier indicates that the relationship between the current density and the voltage drop across the device depends on the injection level. At very low current levels, the current is governed by space-charge generation and is proportional to $\exp(qV/2kT)$. When minority carrier injection into the drift region becomes dominant, with carrier concentrations still well below the background doping, the current flows by diffusion under low-level injection conditions, scaling as $\exp(qV/kT)$. As the forward current density further increases, the injected carrier density in the drift region exceeds the background doping concentration, leading to high-level injection. In this regime, the current once again follows a dependence proportional to $\exp(qV/2kT)$. The injected carrier concentration in the drift region then grows in proportion to the current density, producing an essentially constant voltage drop across the drift region. At even higher on-state current densities, recombination in the end regions begins to reduce the injected carrier density in the drift region. This effect causes a steeper rise in the on-state voltage drop.

This overall behavior is illustrated in Fig. 3.3, which shows a typical on-state characteristic of a silicon PiN rectifier under different modes of

operation.

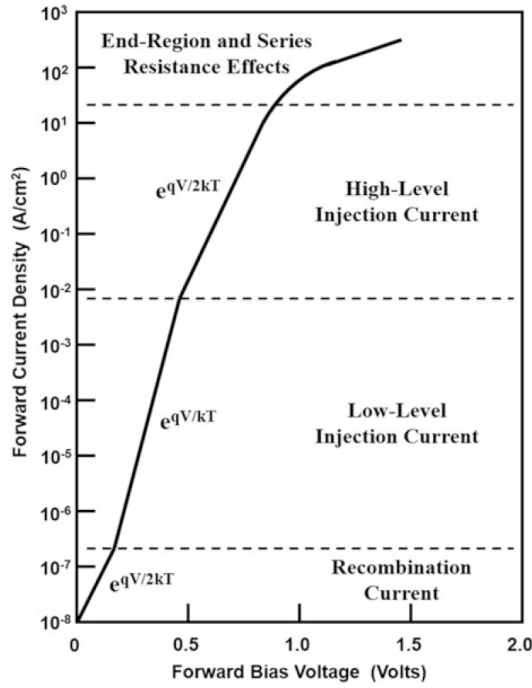


Figure 3.3. On-state characteristics for a silicon PiN rectifier [2].

3.7 Switching Behavior of Power Diodes

Power diodes used in high-efficiency energy conversion applications must not only exhibit low forward voltage drop and withstand very high reverse bias voltages without allowing significant reverse current, but also be capable of switching rapidly between the conducting (on-state) and blocking (off-state) conditions while minimizing power dissipation.

In fact, the transition from the blocking state to the conducting state, also called *forward recovery*, produces an overshoot in the anode voltage with a consequent increase in power dissipation. Conversely, the transition from the conducting state to the blocking state, known as *reverse recovery*,

is even more critical from the standpoint of power losses. In this case, in order to properly turn off the device, the stored charge in the drift region—represented by the excess holes—must be removed, leading to a large reverse current over a short time interval.

To ensure fast switching, the hole concentration in the drift region must vary rapidly. This can be achieved, for example, by choosing a low value for the average carrier lifetime. The turn-on and turn-off processes of a diode can be experimentally analyzed through a specific test, known as the *double-pulse test*, which uses an inductive load circuit consisting of an inductor connected in parallel with the diode and a switch (e.g., a power MOSFET) placed between the diode anode and ground. The test circuit is shown in Fig. 3.5.

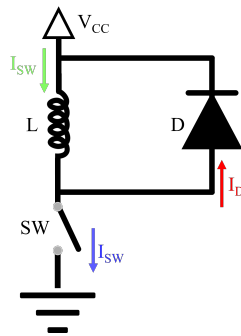


Figure 3.4. Inductive load test circuit.

Initially, the switch is closed, keeping the diode in the off-state, while the inductor charges. When the switch opens, the diode undergoes its turn-on transient. Finally, the switch closes again, initiating the diode's turn-off transient. This procedure allows evaluation of the device's switching performance, in terms of both forward recovery and reverse recovery.

3.7.1 Operation Phases

Phase 1 (Interval T_{ON}). With the switch closed, the inductor charges with a current that increases linearly as

$$i(t) = \frac{V_{CC}}{L} t. \quad (3.57)$$

During this interval, the diode is reverse-biased, since the voltage drop across the switch $V_{ON,SW}$ is negligible compared to the supply voltage V_{CC} :

$$V_D = V_{ON,SW} - V_{CC} \approx -V_{CC}. \quad (3.58)$$

Phase 2 (Interval T_{OFF}). When the switch opens, the current previously stored in the inductor, $i(T_{ON})$, begins to flow through the diode, initiating the turn-on transient.

Phase 3. After the interval T_{OFF} , the switch closes again. The voltage across the inductor changes abruptly from $-V_{ON}$ to $V_{CC} - V_{ON,SW}$, and the diode enters its turn-off transient, after which the current flows entirely through the switch.

Turn-On Behavior

When the switch opens, the diode must conduct the current I delivered by the inductor (previously charged during T_{ON}). The voltage drop across the diode initially rises until it reaches V_{ON} , the steady-state forward voltage corresponding to current I .

This delay is due to the fact that minority carriers (holes) injected into the drift region do not immediately reach the doping concentration N_D (Fig. 3.5 b). As a result, conductivity modulation is not instantaneously established, and the drift region resistance remains high. Consequently, the diode voltage overshoots up to V_{MAX} (possibly several tens of volts) before dropping back to V_{ON} at time t_4 , as shown in Fig. 3.5 a.

It is important to note that V_{MAX} increases with the current slew rate dI/dt , a critical aspect when the required current rise time is comparable to the carrier transit time through the intrinsic region.

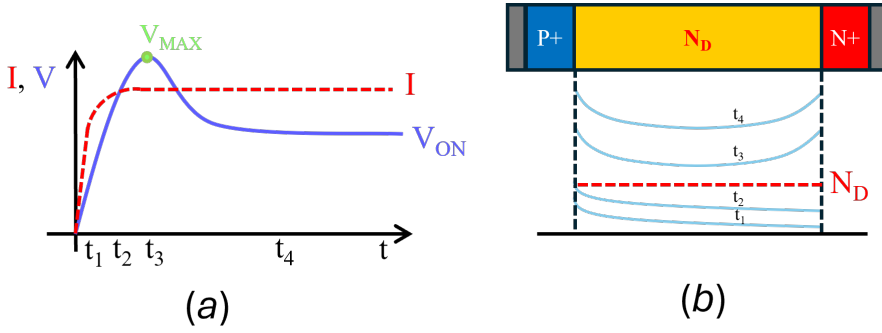


Figure 3.5. (a) Current and voltage during Turn-On, (b) holes distribution in drift region by varying time.

Turn-Off Behavior

During conduction, the large concentration of excess carriers in the drift region keeps the diode's forward voltage drop low. To switch from conduction to blocking, the stored plasma in the drift region must be removed. This transient process, known as *reverse recovery*, is illustrated in Fig. 3.6.

Assuming the switch closes at time t^* , the switch current I_{SW} increases linearly up to t_0 , while the diode current decreases linearly according to

$$I_D = I_L - I_{SW}. \quad (3.59)$$

At t_0 , the diode current reaches zero, but charge is still stored in the drift region, so conduction continues in the form of reverse current. After t_1 , the drift region begins to deplete, with depletion regions expanding toward the center until the stored charge is fully removed. Between t_1 and t_5 , significant power dissipation occurs due to the simultaneous presence of reverse current and increasing reverse voltage.

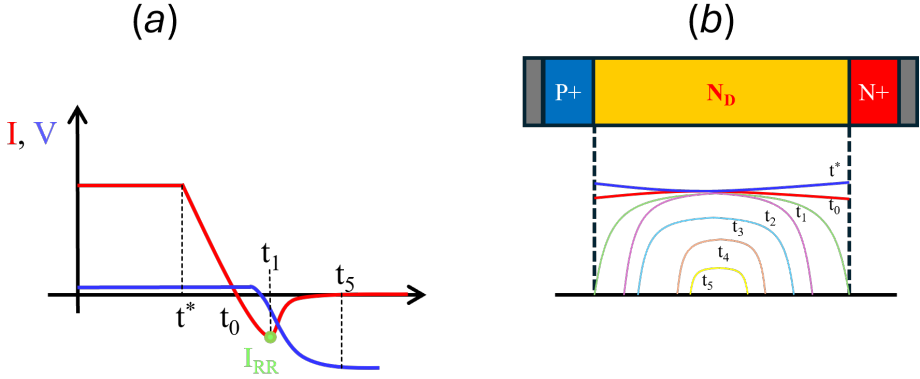


Figure 3.6. Reverse recovery behavior of the diode: (a) current and voltage waveforms, (b) charge distribution in the drift region by varying time.

Reverse Recovery Parameters

The main parameters characterizing reverse recovery are:

- Peak reverse recovery current I_{RR} ,
- Current slope dI/dt ,
- Reverse recovery time T_{RR} , defined as the time from current polarity reversal (positive to negative) until the diode blocks,
- Stored charge Q_{RR} that must be removed.

Assuming a triangular shape for the diode current during T_{RR} , the stored charge can be expressed as

$$Q_{RR} \approx \frac{T_{RR} I_{RR}}{2}. \quad (3.60)$$

Similarly, the peak reverse recovery current is obtained from the current slope as

$$\frac{dI}{dt} = \frac{2I_{RR}}{T_{RR}}. \quad (3.61)$$

The stored charge during T_{RR} must equal the charge accumulated in forward conduction, i.e.,

$$Q_{RR} = Q_F = I_F \tau, \quad (3.62)$$

where τ is the carrier lifetime. Combining these relations yields

$$I_{RR} \approx \sqrt{I_F \tau \frac{dI}{dt}}, \quad T_{RR} = 2 \sqrt{\frac{I_F \tau}{dI/dt}}. \quad (3.63)$$

These relations show that both I_{RR} and T_{RR} are proportional to the square root of the carrier lifetime. Hence, lower lifetime values favor faster turn-off transients. A diode with fast switching capability is referred to as a *fast recovery diode (FRD)*.

The design of FRDs is based on reducing carrier lifetime in the drift region to promote recombination. However, the need for a low lifetime to achieve fast switching is in conflict with the requirement of high conductivity in the drift region. Thus, an optimal trade-off must be found depending on the intended application:

- For low-frequency applications, a higher lifetime is preferable, reducing forward conduction losses.
- For high-frequency applications, a shorter lifetime is required to enable faster switching.

3.8 Silicon Carbide PiN Rectifiers

Due to the much higher electric field that can be sustained in silicon carbide (SiC), the required width of the drift region is significantly smaller than in a corresponding silicon (Si) device with the same breakdown voltage. The design parameters of the drift region for these rectifiers are compared in Table 3.1. For each breakdown voltage, the doping concentration in the drift region of 4H-SiC is approximately 200 times higher than that required for silicon.

The smaller drift region width also implies that the stored charge in a 4H-SiC PiN rectifier is much lower than in the silicon counterpart, leading to an improvement in switching behavior. However, this improved

Table 3.1. Comparison of drift-region design parameters for Si and 4H-SiC devices.

BV (V)	Silicon		4H-SiC	
	Doping (cm^{-3})	Thickness (μm)	Doping (cm^{-3})	Thickness (μm)
500	5.0×10^{14}	36	1.0×10^{17}	2.2
1000	2.0×10^{14}	81	4.0×10^{16}	5.3
2000	8.0×10^{13}	183	1.6×10^{16}	12.0
3000	5.0×10^{13}	294	1.0×10^{16}	20.0
5000	2.0×10^{13}	530	4.4×10^{15}	35.0
10 000	9.0×10^{12}	1200	1.7×10^{15}	80.0

switching performance comes at the cost of a significantly higher built-in potential, due to the larger bandgap of SiC, which results in an increased on-state voltage drop.

Typically, the power dissipation in a 4H-SiC PiN rectifier is about four times higher than in a silicon device. Thus, although the switching behavior is improved, the advantage is offset by substantial on-state power losses. For this reason, it is generally preferable to use SiC Schottky diodes for voltage ratings up to 5,000 V, and SiC PiN diodes for voltage ratings above 10,000 V [1].

Nevertheless, alternative SiC structures have been developed to combine the benefits of both PiN and Schottky diodes. Examples include Junction Barrier Schottky (JBS) and Merged PiN Schottky (MPS) devices, which merge the advantages of the PiN structure with those of the Schottky design.

In the next chapter, we will first discuss the Schottky structure, followed by an analysis of other device architectures such as JBS and MPS.

Chapter 4

Schottky Rectifier

A Schottky rectifier is formed by creating a non-linear electrical contact between a metal and the semiconductor drift region. It is an attractive unipolar device for power electronics applications because of its relatively low on-state voltage drop and fast switching behavior.

Schottky rectifiers have been widely used in low-voltage power supply circuits, where mature silicon technology provides excellent performance. However, in silicon-based Schottky devices, the maximum breakdown voltage is limited by the increasing resistance of the drift region.

In contrast, silicon carbide (SiC), with its much lower drift region resistance, enables the development of Schottky rectifiers with very high breakdown voltages. These devices not only exhibit fast switching speed but also suppress the large reverse recovery current observed in high-voltage silicon PiN rectifiers. As a result, switching losses are reduced not only in the rectifier itself but also in other components, such as IGBTs, within the power circuit.

This chapter first introduces the basic structure of the power Schottky rectifier, defining its constituent elements. The current transport mechanisms relevant to power devices are then analyzed for both forward and reverse operation. This provides the necessary context for the discussion of advanced device concepts in subsequent chapters. For a more detailed treatment of the fundamental concepts related to Schottky rectifiers, the reader is referred to dedicated texts [5].

4.1 Power Schottky Rectifier Structure

The basic one-dimensional structure of a Schottky rectifier is shown in Fig. 4.1, together with the electric field profile under reverse bias operation. If the drift region is uniformly doped, the applied voltage is supported across the drift region with a triangular electric field distribution. The maximum electric field occurs at the metal–semiconductor contact, and breakdown occurs when this field reaches the critical electric field of the semiconductor.

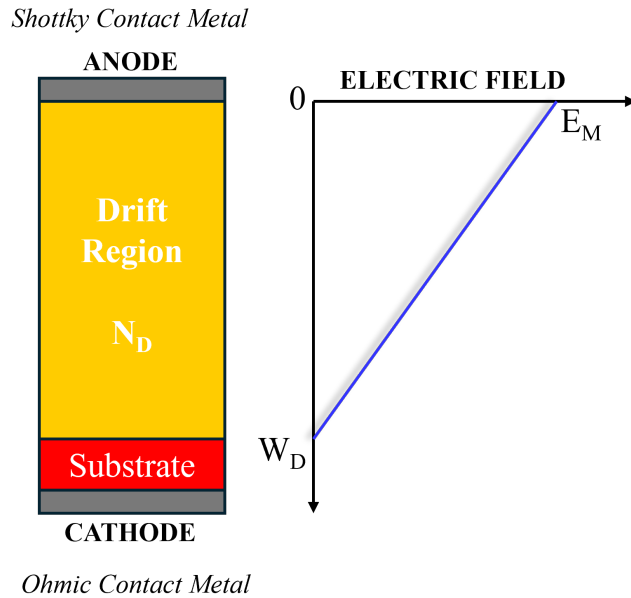


Figure 4.1. Schematic structure and Electric Field Distribution in a Schottky Rectifier.

When a negative bias is applied to the cathode, current conduction in the Schottky rectifier occurs by electron transport across the metal–semiconductor barrier and through the drift region as well as the substrate. The on-state voltage drop is determined by two contributions:

- the voltage drop across the metal–semiconductor interface,
- the ohmic voltage drop across the drift region, the substrate, and its ohmic contact.

At typical on-state current density levels, current conduction is dominated by majority carriers. Consequently, there is negligible minority carrier stored charge within the drift region of a Schottky rectifier. This allows a rapid transition from the on-state to the reverse-blocking off-state, as the depletion region is quickly established in the drift region.

The fast switching capability of Schottky rectifiers enables efficient high-frequency operation with low switching losses, making them well suited for switch-mode power supply applications. With the advent of high-voltage Schottky rectifiers based on SiC, their application is expected to expand to motor control and other high-power, high-frequency systems.

4.2 Schottky Barrier: Energy Band Structure and Physical Mechanisms

The *work function* $q\Phi$ is defined as the energy difference between the vacuum level E_0 and the Fermi level E_F . It can be interpreted as the energy that must be supplied to an electron at the Fermi level in order to remove it from the material. The work function of a semiconductor, $q\Phi_s$, is a function of both the doping type and concentration, which determine the position of the Fermi level E_{FS} . In contrast, in metals the band gap is either very small or nonexistent, and the Fermi level E_{FM} can be regarded as the highest occupied electronic state at zero temperature.

For semiconductors, the above definition of work function may appear less intuitive since the Fermi level generally lies within the forbidden gap. Nevertheless, the work function remains rigorously defined as the energy difference between the vacuum level and the Fermi level, regardless of its position within the gap. This should be interpreted in a statistical sense, reflecting the occupation probability of electronic states near the band edges.

Another important parameter for semiconductors is the *electron affinity*, $q\chi_s$, defined as the energy difference between the vacuum level E_0 and

the conduction band minimum E_C . In the case of flat bands (e.g., when the metal and semiconductor are electrically isolated, as in Fig. 4.2), which implies that no electric field is present inside the semiconductor, the relationship between the work function and the electron affinity is given by:

$$q\Phi_s = q\chi_s + qV_n, \quad (4.1)$$

where qV_n is the energy difference between the conduction band minimum and the semiconductor Fermi level.

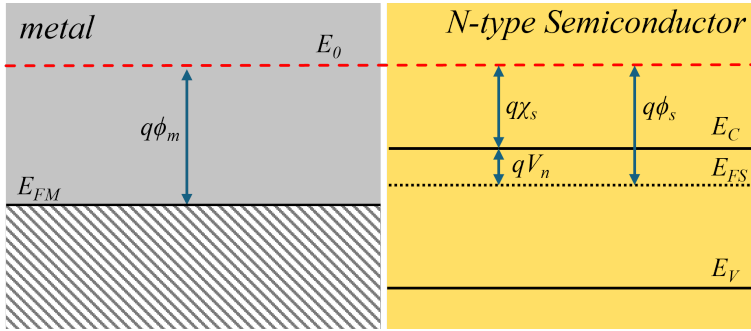


Figure 4.2. Band diagram, isolated metal and semiconductor.

To form a Schottky junction, i.e., to obtain a rectifying metal–semiconductor contact, let us consider bringing an N -type semiconductor into contact with a metal such that:

$$\Phi_m > \Phi_s, \quad (4.2)$$

where Φ_m is the metal work function. In this case, a space-charge region develops at the metal–semiconductor interface, resulting in the formation of an interfacial dipole and an electric field directed from the semiconductor toward the metal. This field opposes the flow of electrons from the semiconductor into the metal, as described in Ref. [5].

A useful expression for the Schottky barrier height is:

$$q\Phi_b = q(\Phi_m - \chi_s), \quad (4.3)$$

while the built-in potential of the Schottky diode is given by:

$$q\psi_{bi} = q(\Phi_b - V_n), \quad (4.4)$$

as illustrated in Fig. 4.3.

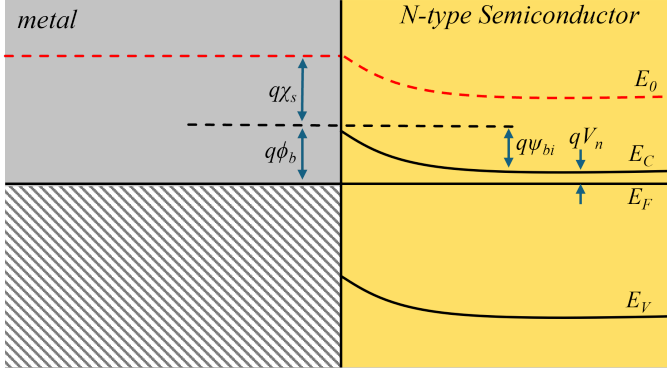


Figure 4.3. Energy-band diagram at thermodynamic equilibrium for an N-type metal–semiconductor junction with $\Phi_m > \Phi_s$.

The depletion region, at thermodynamic equilibrium, width can then be expressed as:

$$W = \sqrt{\frac{2\varepsilon_s}{qN_D}\psi_{bi}} \quad (4.5)$$

where ε_s is the semiconductor permittivity and N_D the donor concentration.

When a positive bias V_f is applied from anode to cathode (thus driving the junction out of thermal equilibrium), the Fermi level is no longer constant throughout the structure. Instead, the system is described by two distinct quasi-Fermi levels: E_{FM} in the metal and E_{FS} in the semiconductor. Their energetic separation is related to the applied forward bias by:

$$qV_f = E_{FS} - E_{FM}. \quad (4.6)$$

This bias reduces the effective Schottky barrier height, thereby allowing an increasingly larger flow of electrons from the semiconductor into the metal as V_f increases (Fig. 4.4). In the next chapter, we will briefly describe

the most relevant electron transport mechanisms underlying the theory of the Schottky junction.

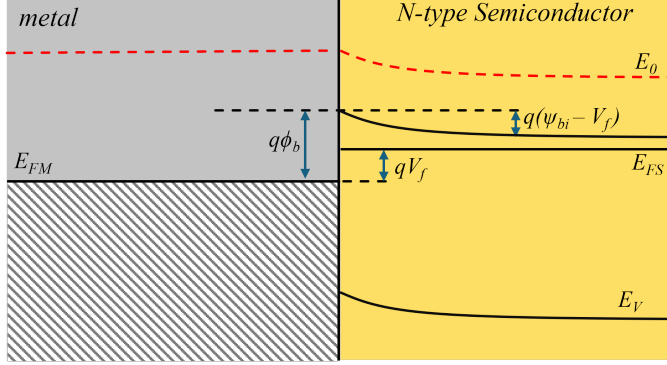


Figure 4.4. Energy-band diagram for an N-type metal–semiconductor junction under forward bias, with the condition $\Phi_m > \Phi_s$.

4.3 Forward Current-Transport Mechanism

Here we provide only a concise overview of the main transport mechanisms that govern the conduction properties of Schottky barriers. For a more detailed and rigorous treatment of these mechanisms, the reader is referred to specialized texts [5].

The different ways in which electrons can be transported across a metal–semiconductor junction under forward bias are schematically illustrated for an N-type semiconductor in Fig. 4.4. The corresponding inverse processes occur under reverse bias.

The primary mechanisms are:

- (a) emission of electrons from the semiconductor over the barrier into the metal;
- (b) quantum-mechanical tunneling through the barrier;
- (c) recombination in the space-charge region;
- (d) recombination in the neutral region (“hole injection”).

In practical Schottky-barrier diodes, mechanism (a) usually dominates, and such devices are commonly referred to as “nearly ideal.” In contrast, mechanisms (b), (c), and (d) are responsible for deviations from this ideal behavior [5].

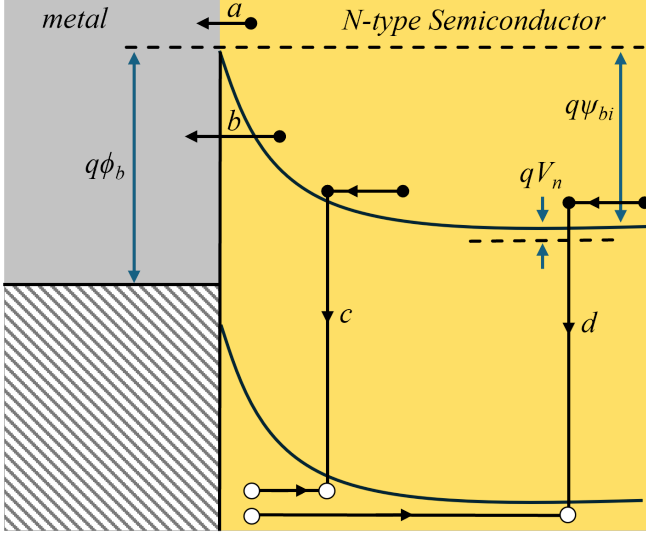


Figure 4.5. Transport processes in a forward-biased Schottky barrier.

4.4 Forward Conduction

Current flow across the metal–semiconductor junction occurs when a negative bias is applied to the N-type semiconductor region. In this case, the current is primarily carried by majority carriers—electrons in the case of an N-type semiconductor.

As mentioned earlier, the dominant current transport mechanism in both silicon and silicon carbide Schottky power rectifiers is *thermionic emission*. For high-mobility semiconductors such as silicon, gallium arsenide, and silicon carbide, the current density across the Schottky barrier can be described by the thermionic emission model:

$$J = AT^2 \exp\left(-\frac{q\Phi_b}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1 \right], \quad (4.7)$$

where A is Richardson's effective constant, T the absolute temperature, k Boltzmann's constant, Φ_b the Schottky barrier height, and V the applied forward voltage [5]. Typical values of the effective Richardson constant are $A = 110, 140$, and $146 \text{ A/cm}^2 \cdot \text{K}^2$ for N-type silicon, gallium arsenide, and 4H-SiC, respectively.

At forward bias, the exponential term dominates, and the forward current density can be expressed as:

$$J_F \approx J_S \exp\left(\frac{qV_f}{kT}\right), \quad (4.8)$$

where V_f is the forward voltage drop across the Schottky contact, while the saturation current density J_S is defined as:

$$J_S = AT^2 \exp\left(-\frac{q\Phi_b}{kT}\right). \quad (4.9)$$

In power Schottky rectifiers, a lightly doped drift region is required to sustain the reverse blocking voltage. A resistive voltage drop V_R develops across this drift region, which increases the total on-state voltage drop.

In addition, the device structure includes:

- the drift region resistance R_{drift} ,
- the substrate resistance R_{SUB} ,
- the ohmic contact resistance R_{CONT} .

The total series resistance is therefore:

$$R_{S,\text{tot}} = R_{\text{drift}} + R_{\text{SUB}} + R_{\text{CONT}}. \quad (4.10)$$

Accordingly, the total on-state voltage drop is given by:

$$V = V_f + J_F R_{S,\text{tot}}, \quad (4.11)$$

As discussed in Chapter 1, the specific on-resistance of the drift region is:

$$R_{\text{ON-IDEAL}} = \frac{4BV^2}{\mu_n \varepsilon_s E_c^3}, \quad (4.12)$$

where BV is the breakdown voltage, μ_n the electron mobility, ε_s the semiconductor permittivity, and E_c the critical electric field. For the same breakdown voltage, the drift region resistance of 4H-SiC is about 2000 times smaller than that of silicon.

The substrate contribution must also be considered because this is comparable to that for the drift region in some instances :

- In silicon, N^+ substrates with resistivity $\rho = 1 \text{ m}\Omega \cdot \text{cm}$ and thickness $t = 200 \text{ }\mu\text{m}$ yield:

$$R_{\text{SUB}} = \rho \cdot t = 2 \times 10^{-5} \text{ }\Omega \cdot \text{cm}^2.$$

- In 4H-SiC, substrates with $\rho = 0.02 \text{ }\Omega \cdot \text{cm}$ and $t = 200 \text{ }\mu\text{m}$ give:

$$R_{\text{SUB}} = 4 \times 10^{-4} \text{ }\Omega \cdot \text{cm}^2.$$

With optimized ohmic contacts, R_{CONT} can be reduced below $10^{-6} \text{ }\Omega \cdot \text{cm}^2$.

The saturation current is highly sensitive to the Schottky barrier height Φ_b and the temperature T .

- A reduction in Φ_b or an increase in T significantly raises J_S , thereby increasing both the forward current and the reverse leakage current.
- For silicon Schottky rectifiers, the forward voltage drop decreases with temperature due to the reduction in Schottky barrier voltage.
- For 4H-SiC rectifiers, the forward voltage drop increases with temperature because of enhanced resistive contributions in the drift region.

Figure 4.6 and 4.7 illustrates the forward conduction characteristics of silicon and silicon carbide Schottky rectifiers for various breakdown voltages. At $BV = 50 \text{ V}$ and a current density of 100 A/cm^2 , the series resistance has little effect. However, for $BV > 100 \text{ V}$, the series resistance limits the use of silicon Schottky rectifiers to low-voltage applications such as switch-mode power supplies.

By contrast, the lower drift region resistance of 4H-SiC enables operation at breakdown voltages up to several kilovolts, making these devices suitable for medium- and high-power systems.

The choice of Schottky barrier height is crucial:

- A lower barrier height reduces the on-state voltage drop but increases leakage current.
- A higher barrier height reduces leakage but increases conduction losses.

Thus, the design of a power Schottky rectifier requires optimization of Φ_b to balance on-state efficiency with acceptable reverse leakage.

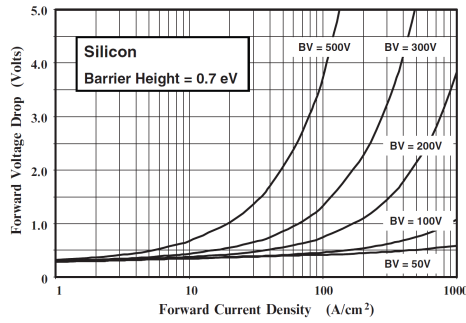


Figure 4.6. Forward Characteristics of Silicon Schottky Rectifiers.

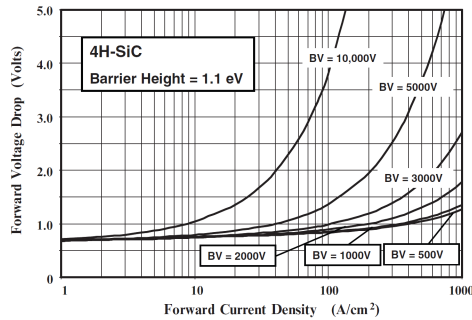


Figure 4.7. Forward Characteristics of Silicon Carbide Schottky Rectifiers.

4.5 Reverse Blocking

When a reverse bias is applied to the Schottky rectifier, the voltage is sustained across the drift region, with the maximum electric field located at the metal–semiconductor contact, as shown in Fig. 4.1. Since no voltage can be supported within the metal, the reverse blocking capability of the Schottky rectifier is governed by the same physics as an abrupt P–N junction [5].

Assuming a parallel-plane breakdown voltage, the drift region doping concentration and width for a silicon device can be expressed as:

$$N_D = 2 \times 10^{18} (BV_{PP})^{-4/3}, \quad (4.13)$$

$$W_D = 2.58 \times 10^{-6} (BV_{PP})^{7/6}, \quad (4.14)$$

where BV_{PP} is the parallel-plane breakdown voltage.

In practical power Schottky rectifiers, however, the breakdown voltage is limited by edge effects. Edge termination techniques have been developed to raise the breakdown voltage close to the parallel-plane value [1].

Due to the relatively small barrier height in silicon Schottky rectifiers, the thermionic emission component dominates. The leakage current under reverse bias can be obtained from the thermionic emission equation by substituting a negative bias of magnitude V_R . It is then determined by the saturation current:

$$J_L = -AT^2 \exp\left(-\frac{q\Phi_B}{kT}\right) = -J_S, \quad (4.15)$$

where A is the Richardson constant, T the absolute temperature, q the elementary charge, Φ_B the Schottky barrier height, and k Boltzmann's constant.

The leakage current is a strong function of both the barrier height and the temperature. To reduce leakage and minimize power dissipation in the blocking state, a large Schottky barrier height is desirable. However, as temperature increases, the leakage current rises rapidly, as shown in Fig. 4.7.

If the power dissipation caused by leakage becomes dominant, the re-

sulting temperature increase can trigger a positive feedback mechanism leading to *thermal runaway*. This destructive failure mode must be avoided by designing the device with a sufficiently high Schottky barrier height, even though this increases the on-state voltage drop. A larger barrier height is especially necessary for rectifiers intended for operation at high ambient temperatures.

It should be noted that in practice, the leakage current in power Schottky rectifiers is substantially higher than the ideal saturation current because of Schottky barrier lowering and tunneling effects.

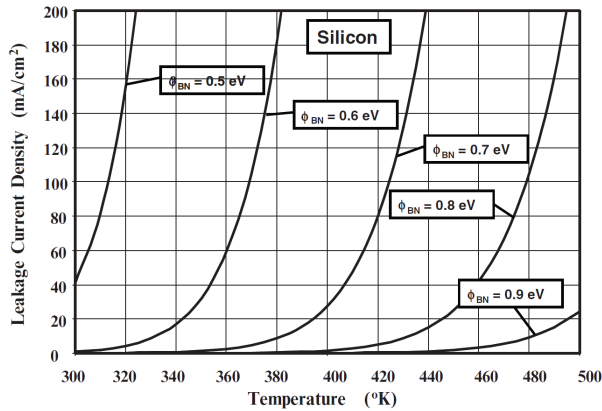


Figure 4.8. Temperature dependence of the leakage current for silicon schot-
tky rectifiers.

4.6 Schottky Barrier Lowering

Based on the previous analysis, the leakage current of an ideal Schottky rectifier should be independent of the magnitude of the applied reverse bias voltage. However, practical power Schottky rectifiers exhibit a significant increase in leakage current as the reverse bias voltage increases. This rise in leakage current is much greater than the space-charge generation current associated with the expanding depletion region.

During reverse blocking operation, it has been observed that the Schottky barrier height is reduced due to the *image-force lowering* phenomenon [1]. The reduction in barrier height is determined by the maximum electric field

E_M at the metal–semiconductor interface:

$$\Delta\Phi_B = \sqrt{\frac{qE_M}{4\pi\epsilon_S}}, \quad (4.16)$$

For a one-dimensional structure, the maximum electric field is related to the applied reverse bias voltage V_R by:

$$E_M = \sqrt{\frac{2qN_D}{\epsilon_S} (V_R + \Phi_{bi})}, \quad (4.17)$$

As an example, Fig. 4.9 shows the reduction in Schottky barrier height for silicon and 4H-SiC rectifiers with a drift region doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$. For the silicon structure, the barrier height reduction is about 0.065 eV at the maximum reverse bias voltage.

In contrast, silicon carbide devices sustain much larger electric fields in the drift region before the onset of impact ionization, which results in significantly larger barrier lowering. For the same doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$, the barrier lowering in silicon carbide is approximately three times greater than in silicon at the corresponding breakdown voltage (see Fig. 4.9).

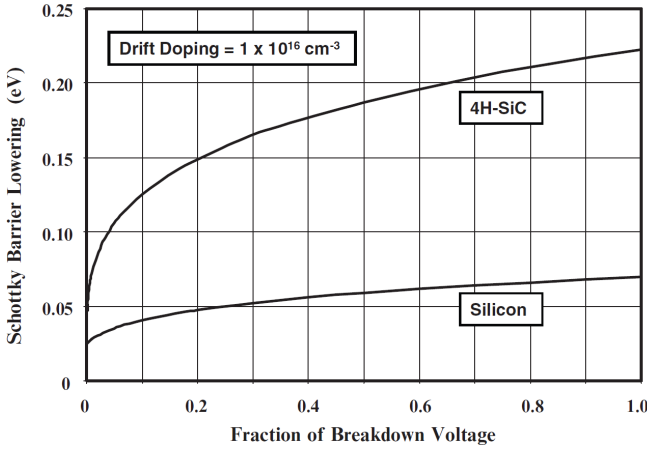


Figure 4.9. Schottky Barrier Lowering for Silicon and 4H-SiC Schottky Rectifiers.

This explains the much stronger increase in leakage current with reverse bias in SiC devices. To compare different devices, the reverse voltage was normalized to the breakdown voltage, which is about 50 V for silicon and 3000 V for 4H-SiC (see Fig. 4.9).

Including the effect of Schottky barrier lowering, the leakage current density can be written as:

$$J_L = -AT^2 \exp\left(\frac{-q(\Phi_B - \Delta\Phi_B)}{kT}\right), \quad (4.18)$$

where A is the Richardson constant, Φ_B the nominal Schottky barrier height, and kT the thermal energy.

Figure 4.10 compares the leakage current calculated with and without barrier lowering for a silicon device with a breakdown voltage of 50 V. The space-charge generation current was neglected in this analysis since it is much smaller than the current through the metal–semiconductor interface. It can be seen that the leakage current is enhanced by about a factor of five due to barrier lowering as the reverse voltage increases toward breakdown.

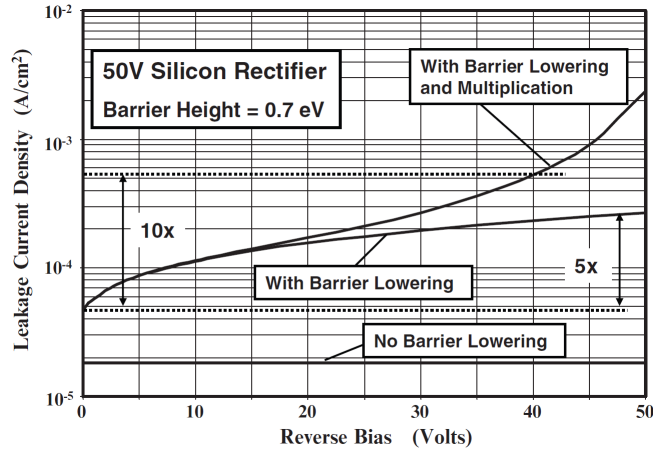


Figure 4.10. Leakage Current Density for a 50V Silicon Schottky Rectifier.

Experimental data, however, show that the actual reverse leakage current in silicon Schottky rectifiers rises even more steeply than predicted by the image-force lowering effect alone.

4.7 Pre-Breakdown Avalanche Multiplication

The large increase in leakage current observed in practical silicon power Schottky rectifiers can be explained by including the effect of *pre-breakdown avalanche multiplication*. At reverse bias voltages close to the breakdown voltage, the high electric fields inside the device lead to impact ionization and the generation of a large number of free carriers. These carriers are transported through the Schottky rectifier structure, significantly enhancing the leakage current.

The total number of electrons reaching the edge of the depletion region is greater than those injected across the metal–semiconductor contact by a factor M_n , which is the avalanche multiplication coefficient. This coefficient depends on both the maximum electric field E_M at the metal–semiconductor contact and the depletion layer width W_D .

The leakage current density for a silicon Schottky rectifier with a drift region doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$ is shown in Fig. 4.10, after including the influence of the pre-breakdown multiplication coefficient. The effect of M_n becomes evident at high reverse voltages, when the electric field approaches the semiconductor’s critical field for avalanche breakdown.

When both Schottky barrier lowering and pre-breakdown multiplication are taken into account, the calculated leakage currents are consistent with the behavior of commercially available silicon devices. These devices typically exhibit an order-of-magnitude increase in leakage current, rising from low reverse bias voltages to nearly 80% of the rated breakdown voltage.

4.8 Silicon Carbide Schottky Rectifiers

The enhanced Schottky barrier lowering observed in silicon carbide devices leads to a much more pronounced increase in leakage current with reverse bias, as shown in Fig. 4.11. According to the theoretical model, the leakage current is expected to increase by approximately three orders of magnitude as the reverse voltage approaches the breakdown voltage. However, experimental results for high-voltage silicon carbide Schottky rectifiers reveal a significantly larger increase in leakage current than predicted, despite the stronger barrier-lowering effect. In fact, the measured

leakage current increases by nearly six orders of magnitude with increasing reverse bias voltage.

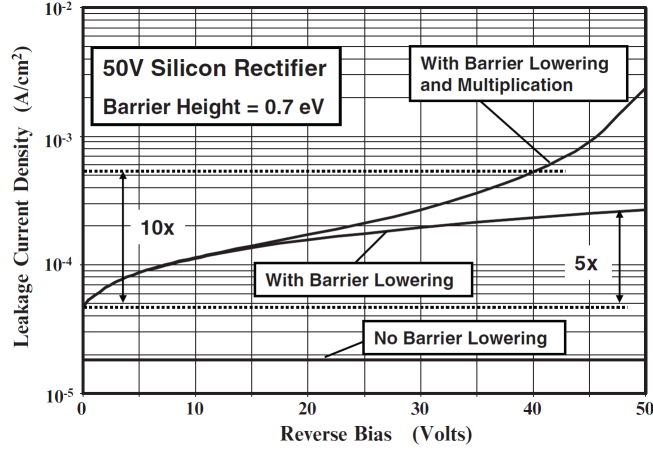


Figure 4.11. Leakage Current Density for a 3kV 4H-SiC Schottky Rectifier.

To explain this rapid rise in the leakage current, it is necessary to include the contribution of *field emission* (or tunneling). The thermionic-field emission model predicts a barrier lowering effect that is proportional to the square of the electric field at the metal–semiconductor interface. When combined with the thermionic emission model, the leakage current density can be expressed as:

$$J_A = AT^2 \exp\left(-\frac{q\phi_B}{kT}\right) \exp\left(\frac{q\Delta\phi_B}{kT}\right) \exp(C_T E_M^2), \quad (4.19)$$

where C_T is the tunneling coefficient. A value of $C_T = 8 \times 10^{-13} \text{ cm}^2/\text{V}^2$ was found to reproduce the experimentally observed six orders of magnitude increase in the leakage current, as shown in Fig. 4.11. Thus, inclusion of the tunneling mechanism enhances the leakage current by approximately three additional orders of magnitude beyond the contribution of Schottky barrier lowering alone.

As previously discussed, the leakage current in silicon carbide Schottky rectifiers increases much more rapidly with reverse voltage than in silicon

devices. Fortunately, larger Schottky barrier heights can be employed in silicon carbide structures, since an on-state voltage drop in the range of 1 to 1.5 V is acceptable for such high-voltage devices. This makes it possible to maintain an acceptable level of power dissipation in the reverse-blocking state.

For instance, in the case of a 3 kV 4H-SiC Schottky diode, the reverse power dissipation at room temperature is less than 1 W/cm^2 , compared with an on-state power dissipation of about 100 W/cm^2 . The expected increase in leakage current with temperature must, of course, be taken into account to ensure that reverse power dissipation remains below the on-state value, thereby guaranteeing stable operation.

Finally, the leakage current can be further suppressed by shielding the Schottky contact through the use of the Junction Barrier Schottky (JBS) rectifier structure, originally developed for silicon devices [1].

Junction Barrier and Merged PiN Schottky Rectifiers: Concepts, Challenges, and Modeling

In the case of Schottky rectifiers, it is necessary to balance the on-state (or conduction) power loss against the reverse-blocking power loss by optimizing the Schottky barrier height. When the barrier height is reduced, the on-state voltage drop decreases, leading to lower conduction power losses. However, this reduction also increases the leakage current, resulting in higher reverse-blocking losses. Power dissipation can therefore be minimized by lowering the barrier height, but at the cost of reducing the maximum allowable operating temperature. This trade-off is further complicated by the rapid rise in leakage current with increasing reverse bias voltage, caused by Schottky barrier lowering and pre-breakdown avalanche multiplication phenomena.

The first method proposed to mitigate the barrier lowering effect in vertical silicon Schottky rectifiers involved shielding through the incorporation of a P–N junction. The underlying idea was to form a potential barrier that shields the Schottky contact from the high electric fields generated in the semiconductor, achieved by embedding closely spaced P^+ regions around the contact. This design was named the *Junction Barrier Schottky (JBS)*

rectifier. In the JBS structure, the forward current is directed to flow through the undepleted gaps between the P^+ regions, thereby maintaining unipolar conduction. Besides reducing leakage current, the presence of P^+ regions also improves the ruggedness and reliability of the diode. Detailed optimization of silicon JBS rectifiers has been achieved by using sub-micron dimensions for the P^+ regions. Minimizing the area occupied by the P^+ regions reduces the spreading resistance of the drift region beneath the Schottky contact, further lowering the on-state voltage drop.

As shown in the previous chapter, the increase in leakage current with reverse bias is much more pronounced in silicon carbide Schottky rectifiers. This behavior arises from the stronger barrier lowering effect caused by the higher electric fields in SiC drift regions, together with the onset of thermionic-field emission (tunneling current). It is therefore evident that the field-suppression methods developed for silicon Schottky diodes are even more effective and valuable when applied to silicon carbide devices [1].

This chapter discusses the application of the junction barrier shielding concept to reduce the electric field at the metal–semiconductor contact in both silicon and 4H-SiC Schottky rectifiers. Alongside analytical models, the physical operation of these devices is analyzed through two-dimensional numerical simulations. It is shown that the JBS concept not only improves the performance of silicon devices but can also be extended to silicon carbide rectifiers to achieve even greater performance benefits.

In addition, within this chapter we also examine the 4H SiC *Merged PiN Schottky (MPS)* structure, which differs from the JBS design. In the MPS diode, the PiN region is intentionally involved in forward conduction. While this does not significantly affect the normal operating current range, it improves the robustness of the device under surge or peak current conditions. However, if the MPS is not carefully designed (e.g., due to a non-optimized ratio of geometric dimensions), it may exhibit a segment with negative differential resistance (NDR) in the forward I–V characteristics, known as *snapback*, which can seriously compromise device reliability. Therefore, at the end of this chapter, we will not only present design strategies to mitigate this effect but also introduce a compact electrothermal geometric model compatible with SPICE. This model enables highly accurate prediction of device behavior, even under operating conditions that are difficult to access with finite-element simulators such as SENTAU-

RUS TCAD.

5.1 Junction Barrier Schottky Structure

The elementary cell of a Junction Barrier Schottky (JBS) rectifier structure is illustrated in Fig. 5.1. It consists of a P^+ region placed around the Schottky contact to generate a potential barrier under the metal–semiconductor interface in the reverse-blocking mode, thereby shielding the Schottky contact. The magnitude of this potential barrier depends on the distance between the P-type regions and the depth of the P–N junction. A smaller spacing and a deeper junction favor an increase in the barrier magnitude, leading to a stronger reduction of the electric field at the Schottky contact. Reducing the electric field at the contact lowers the barrier lowering and field-emission effects, which is beneficial for minimizing leakage current at high reverse bias voltages.

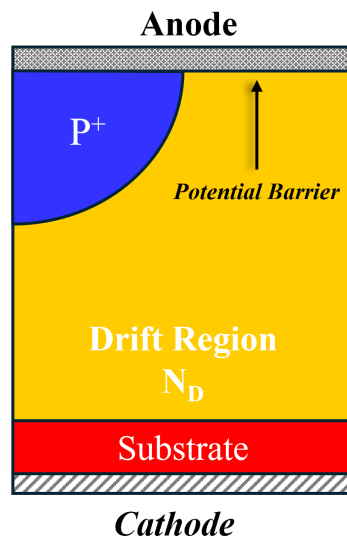


Figure 5.1. Junction Barrier Schottky (JBS) Rectifier Structure.

As discussed in the previous chapter, for an N -type semiconductor a rectifying Schottky contact is ideally formed when the metal work function

ϕ_m is larger than the semiconductor work function $\phi_{s,n}$ (where $\phi_{s,n}$ is the work function of the N-type semiconductor). However, this simple relation holds only in the absence of Fermi-level pinning and other interface effects, which in practice often play a significant role, as described in Ref. [5]. Conversely, when the same metal is interfaced with a P-type semiconductor, and under the simplified condition $\phi_m > \phi_{s,p}$ (where $\phi_{s,p}$ is the work function of the P-type semiconductor), the resulting contact is usually ohmic rather than rectifying. In real devices, however, the nature of the contact depends on a combination of metal work function, semiconductor electron affinity, doping concentration, and interface states.

In practice, depositing the same metal layer on both the N-type region and the P-type region is advantageous, since it reduces the number of masks required during processing for the device fabrication. However, particularly in the case of silicon carbide (less so for silicon), the ohmic contact formed on the P-type region is often inefficient, significantly limiting its ability to conduct under forward-bias conditions in the PiN region.

In this scenario, the P-type regions play an essential role primarily in determining the reverse-blocking behavior of the device, with only a modest influence on forward conduction, which becomes significant only at high voltages and/or elevated temperatures. While this is not necessarily a drawback—depending on the application—there are situations, such as when robustness against surge currents is required, in which it becomes necessary to form a dedicated ohmic contact on the P-type region. This enables efficient triggering of bipolar conduction, thereby mitigating harmful effects associated with current spikes in the device.

Structures that incorporate such dedicated ohmic contacts on the P-type regions are generally referred to as *Merged PiN Schottky (MPS)* rectifiers, although in both the literature and industry the nomenclature is not universally consistent. Nonetheless, the P-type regions are not intended to sustain forward conduction within the normal operating current range, since even with a good ohmic contact, the voltage drop across the diode is insufficient to strongly forward bias the P–N junction. For instance, silicon devices with low breakdown voltages typically operate with on-state voltage drops of about 0.45 V, which is well below the ~ 0.7 V required for strong injection across the P–N junction. The margin is even larger in silicon carbide due to its wider bandgap: typical 4H-SiC Schottky rectifiers

have on-state voltage drops below 1.5 V, compared to the ~ 3 V needed to induce significant injection from the P–N junction.

In silicon devices, the P–N junction is typically formed through an annealing cycle that creates a planar junction with lateral diffusion, as shown in Fig. 5.1. The extra area consumed by this lateral diffusion must be taken into account during the analytical modeling of the JBS structure. Furthermore, the cylindrical geometry of the junction causes the cathode potential to extend towards the Schottky contact, enhancing the electric field at the contact under reverse bias conditions. By contrast, in silicon carbide devices, ion implantation followed by annealing produces negligible lateral diffusion, so the P–N junction can be represented approximately with a rectangular geometry, as illustrated in Fig. 5.2.

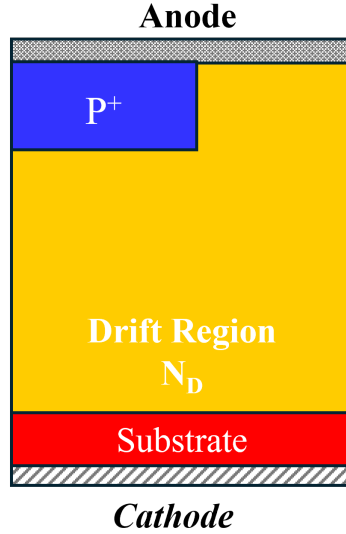


Figure 5.2. SiC Junction Barrier Schottky (JBS) Rectifier Structure.

The limited lateral diffusion in SiC is also a crucial factor in the design of edge terminations. For instance, in the case of field floating rings, the P-rings are placed closer together in silicon carbide than in silicon. This ensures proper field coupling of all termination rings, thereby allowing the structure to sustain higher electric fields during reverse-bias operation.

5.1.1 Forward Conduction Models

Analysis of the on-state voltage drop of the JBS rectifier requires considering the current constriction at the Schottky contact caused by the presence of the P⁺ region, as well as the increased resistance of the drift region due to current spreading from the Schottky contact to the N⁺ substrate. Several models can be developed for the spreading resistance, each suitable for different JBS rectifier designs. In addition, the distinct geometry of the P–N junction in silicon carbide also requires a dedicated model.

In the following, however, we will primarily focus on the silicon carbide JBS model, from which the compact geometric and electrothermal model with lumped parameters compatible with SPICE has been developed.

5.2 Silicon Carbide JBS Rectifier: Forward Conduction Model

In a JBS rectifier, the P–N junction grid is designed so that its depletion layers do not pinch off under zero and forward bias conditions. The JBS structure contains multiple conductive channels beneath the Schottky barrier through which current flows during forward-biased operation. The basic forward conduction mechanisms of a JBS rectifier are the same as those of a conventional Schottky rectifier, since under normal working conditions the current passes only through the metal–semiconductor junction. However, the presence of the P–N junction grid increases the series resistance of the drift region due to current constriction in the channel structure.

Unlike a conventional Schottky rectifier (without P–N grids), the total series resistance of a JBS rectifier is the sum of the conduction channel resistance through the P–N grid and the current spreading resistance in the drift region. Here, we consider the case of a P–N junction grid with a stripe geometry and cross-sectional dimensions as shown in Fig. 5.3.

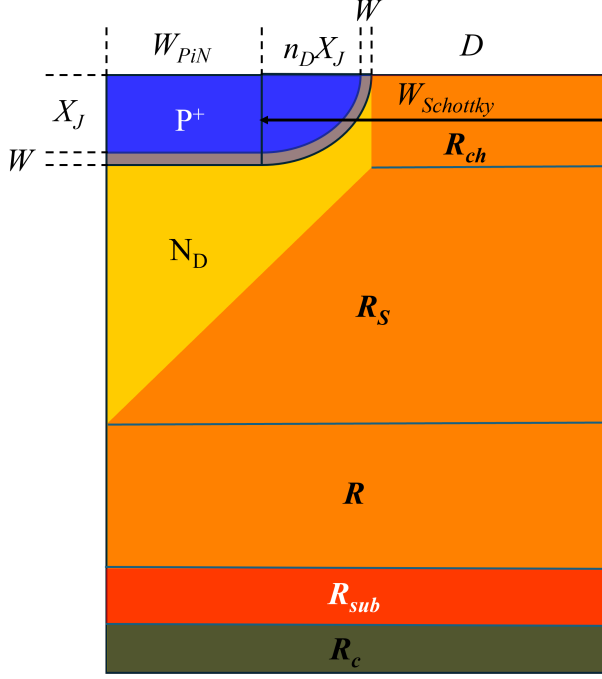


Figure 5.3. Geometric dimensions and density current distribution of 4H-SiC JBS structure under forward voltage.

In this model, the on-resistance of the epitaxial layer is divided into three components: channel resistance, spreading resistance, and drift region resistance. The lateral diffusion of the junction is assumed to be n_D percent of the vertical junction depth X_J .

The relationship between the forward voltage drop and the current density for a Schottky barrier must be modified to account for the area occupied by the P^+ region in the JBS rectifier structure. Within the JBS structure, the current density across the Schottky barrier (J_{FS}) is given by

$$J_{FS} = \frac{W_{PiN} + W_{Schottky}}{D} \cdot J_{FC} \quad (5.1)$$

where J_{FC} is the cell current density, obtained by dividing the total JBS rectifier current by the cell area. Using this expression, the voltage

drop across the Schottky barrier is:

$$V_{FS} = \Phi_B + \frac{kT}{q} \ln \left(\frac{W_{PiN} + W_{Schottky}}{D} \cdot \frac{J_{FC}}{AT^2} \right) \quad (5.2)$$

Here, V_{FS} is the voltage drop across the Schottky barrier, and D represents the actual width of the barrier, related to the structural dimensions and the junction depletion width:

$$D = W_{Schottky} - W - n_D X_j \quad (5.3)$$

with the depletion width given by:

$$W = \sqrt{\frac{2\epsilon_s}{qN_D} (V_{bi} - V_F)} \quad (5.4)$$

In addition to the voltage drop across the Schottky barrier, the voltage drops across the drift layer and substrate must also be included. The specific on-resistance of the JBS rectifier is determined by the resistance components shown in Fig. 5.3:

$$R_{on} = R_{ch} + R_S + R + R_{sub} + R_c \quad (5.5)$$

where R_{ch} is the conducting channel resistance, R_S is the spreading region resistance (assuming current spreading at a 45° angle, θ), R is the drift region resistance (with ρ_D as the drift-layer resistivity), R_{sub} is the substrate resistance, and R_c is the contact resistance.

The analysis of the channel, spreading, and drift region resistances yields:

$$R_{ch,sp} = \rho_D X_j \cdot \frac{W_{PiN} + W_{Schottky}}{D} \quad (5.6)$$

$$R_{S,sp} = \rho_D \tan \theta (W_{PiN} + W_{Schottky}) \ln \left(\frac{W_{PiN} + W_{Schottky}}{D} \right) \quad (5.7)$$

$$R_{sp} = \rho_D (d - X_j - (W_{PiN} + W_{Schottky} - D) \tan \theta) \quad (5.8)$$

For the computation of $R_{ch,sp}$ and $R_{S,sp}$, these regions can be approximated as having uniform electric field distribution and, correspondingly, uniform current density. Therefore, the resistance can then be expressed

as:

$$R_0 = \rho_0 \frac{l}{\Sigma} \quad (5.9)$$

where l is the length of the region along the current flow, and Σ is the cross-sectional area through which the current flows.

In the spreading region, however, neither the electric field nor the current density can be assumed uniform. To evaluate this resistance, we approximate the current density distribution as trapezoidal. As shown in Fig. 5.4, $l(x)$, the trapezoid base, varies with the coordinate x and can be written as:

$$l(x) = D + \tan \varphi \cdot x \quad (5.10)$$

with

$$\tan \varphi = \frac{W_{PiN} + n_D X_j}{t} \quad (5.11)$$

The infinitesimal resistance is then:

$$dR = \frac{\rho t dx}{Dt + (W_{PiN} + n_D X_j)x} \cdot \frac{1}{Z} \quad (5.12)$$

where Z is the cell length in the direction orthogonal to the cross-section. Integrating from $x = 0$ to $x = t$ (N^+ substrate) gives:

$$R = \frac{\rho \tan \theta}{Z} \ln \left(\frac{W_{cell}}{D} \right) \quad (5.13)$$

where

$$\tan \theta = \frac{t}{W_{PiN} + n_D X_j} \quad (5.14)$$

while

$$W_{cell} = D + W_{PiN} + n_D X_j = W_{PiN} + W_{Schottky} \quad (5.15)$$

It is worth noting that in the calculation of $W_{Schottky}$ we neglected W , since during forward conduction W rapidly decreases and can therefore be omitted. The specific drift region resistance is then obtained by multiply-

ing the cell resistance by the cell area ($W_{cell} \cdot Z$):

$$R = \rho(W_{PiN} + W_{Schottky}) \tan \theta \ln \left(\frac{W_{PiN} + W_{Schottky}}{D} \right) \quad (5.16)$$

Finally, by setting $\rho = \rho_D$, we recover the earlier expression for the spreading resistance $R_{S,sp}$.

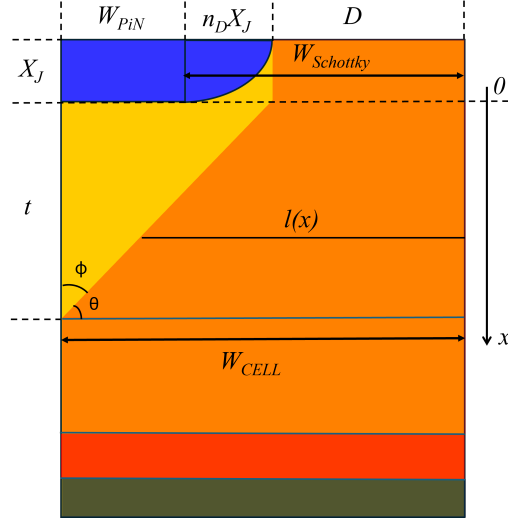


Figure 5.4. Geometric dimensions and current density distribution of the 4H-SiC JBS structure under forward voltage. In the analytical treatment, the depletion width W has been intentionally neglected in order to streamline the derivation.

5.3 Case Study: 10kV 4H-SiC MPS

As previously discussed, Merged PiN Schottky (MPS) diodes exhibit superior robustness against surge events compared to their JBS counterparts. The P-type regions in JBS structures, as described in the introductory sections of this chapter, primarily serve to enhance the blocking behavior of the device. They do not play a significant role in forward conduction, except under conditions of high voltage and/or elevated temperature.

In JBS structures, the contact on P-type region is typically formed using the same metal employed to create the Schottky contact. This fabrication strategy is advantageous because it reduces the number of photolithographic masks required. However, while this simplifies manufacturing, the ohmic contact thus obtained is often not highly efficient. Although this limitation does not necessarily represent a drawback for many applications, there exist specific use cases where the device must withstand very high and unpredictable current surges without failure. For such cases, MPS structures are preferred, as they incorporate an additional masking step to fabricate a dedicated ohmic contact on the P region.

By implementing a dedicated ohmic contact, the MPS diode can exploit bipolar conduction—not in the normal operating current range, but rather under extreme transient conditions, where very large current peaks occur. A schematic comparison of the forward I–V characteristics of a 4H-SiC JBS diode, a 4H-SiC MPS diode, and a 4H-SiC PiN diode is shown in Fig. 5.5.

Given these considerations, MPS structures, especially in SiC technology, are relatively uncommon and thus require further investigation in terms of modeling, design, and optimization. A central focus of this thesis is the study and circuit-level modeling of 4H-SiC MPS diodes. In particular, a compact geometric and electro-thermal model has been developed, capable of accurately predicting the forward behavior of these devices, even in scenarios where traditional TCAD simulations are less flexible.

As a case study, we refer to [3], which analyzes a 10 kV 4H-SiC MPS diode. A schematic cross-section of the proposed diode is presented in Fig. 5.6.

The structure includes:

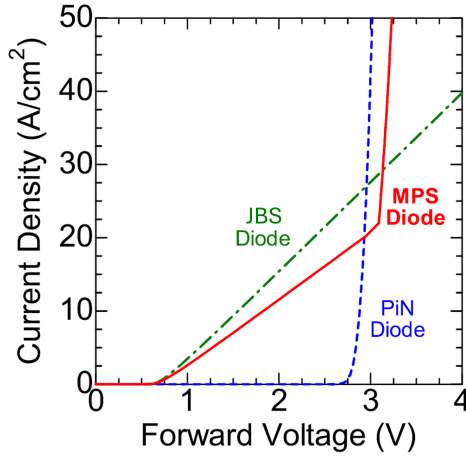


Figure 5.5. Forward I–V characteristics of MPS, JBS, and PiN diodes.

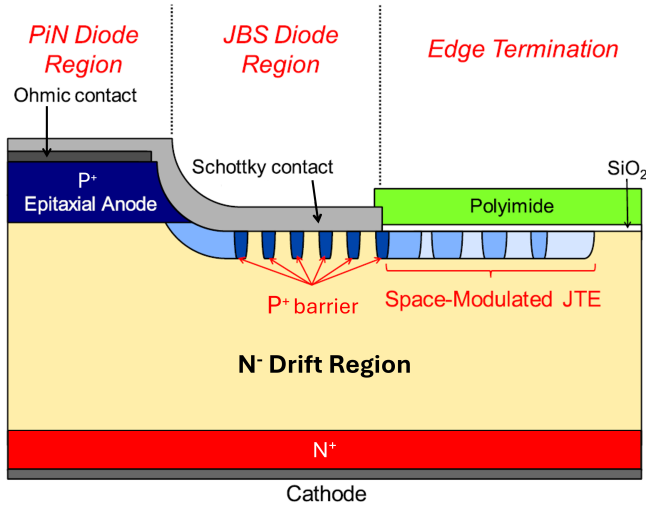


Figure 5.6. Schematic cross section of the 4H-SiC MPS diode proposed in [3]

- a termination region, designed to mitigate electric field crowding under reverse bias,
- an intermediate region where implanted P-type areas alternate with Schottky regions (a “JBS-like” section), providing the combined benefits of low forward conduction loss and Schottky protection in reverse,
- and finally, a P^+ epitaxial region that fully exploits bipolar conduction.

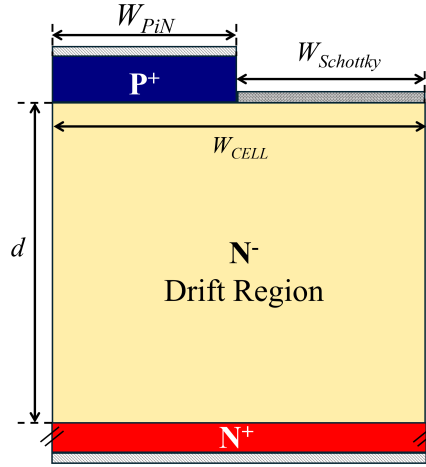


Figure 5.7. Schematic cross-section of the simplified 4H-SiC MPS structure

The choice of an epitaxial P^+ layer is particularly important, as it reduces the detrimental effects of ion implantation in SiC. Implantation typically introduces a high density of point defects, which severely hinder carrier injection and dramatically increase R_{on} in conventional SiC PiN diodes. For this reason, epitaxial-based structures such as the one shown in Fig. 5.6 are preferred over planar implanted counterparts. For modeling and forward conduction analysis, the structure is simplified into a compact representation consisting solely of alternating Schottky and P^+ epitaxial regions, as shown in Fig. 5.7.

The parameters used in the TCAD simulations (Sentaurus environment) are summarized in Table 5.1.

Table 5.1. Simulation parameters of the 4H-SiC MPS diode.

Parameter	Value
N^- doping concentration	$7 \times 10^{14} \text{ cm}^{-3}$
P^+ doping concentration	$1 \times 10^{19} \text{ cm}^{-3}$
N^+ doping concentration	$1 \times 10^{19} \text{ cm}^{-3}$
Drift region thickness, d	$95 \text{ } \mu\text{m}$
Drift region resistivity, ρ	$9.65 \text{ } \Omega \cdot \text{cm}$
Angle, θ	42°

While figure 5.8 schematically illustrates the approximated distribution of unipolar current density.

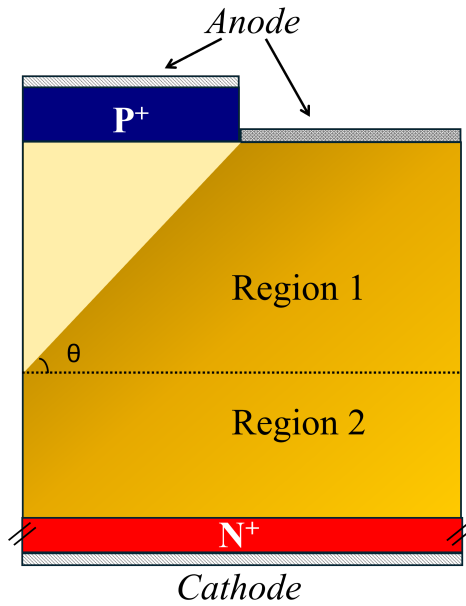


Figure 5.8. Schematic illustration of the approximated distribution of unipolar current density in the JBS current-distribution model

As already mentioned, these devices may exhibit the so-called *snap-back effect*, characterized by a negative differential resistance region in the forward I–V curve (see Fig. 5.9).

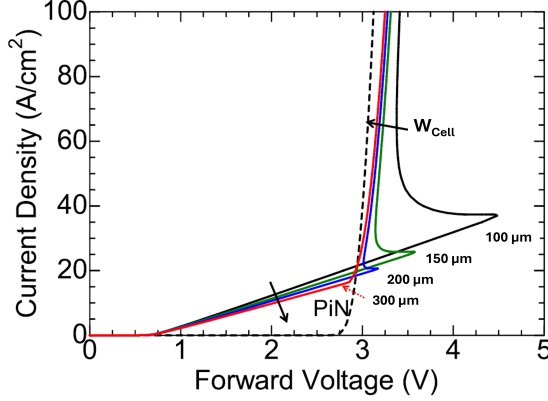


Figure 5.9. Simulated forward I–V characteristics of SiC MPS diodes by varying W_{Cell}

In the example of Fig. 5.7, the widths of the Schottky (W_{Schottky}) and PiN (W_{PiN}) regions are chosen equal, while the total active area is kept constant (1 cm^2). The variation is applied to the total cell width ($W_{\text{Cell}} = W_{\text{PiN}} + W_{\text{Schottky}}$), compensated by the orthogonal cell length Z , ensuring the total area remains fixed (Fig. 5.10).

$$\frac{W_{\text{Cell}}}{2d} > \frac{1}{\tan \theta} \quad (5.17)$$

Equation (5.17) expresses the design criterion required to prevent snapback, where d is the drift region length and θ is the current spreading angle.

This effect is particularly critical when multiple dice are paralleled within the same package, a widespread industrial practice to improve yield and achieve high current ratings without resorting to larger die sizes. Improper design can lead to current crowding and premature device failure. In [3], it is demonstrated that ensuring the condition in Equation (5.17) is sufficient to suppress snapback. This condition will be discussed in more detail in the following subsection, where the compact circuit models are

introduced.

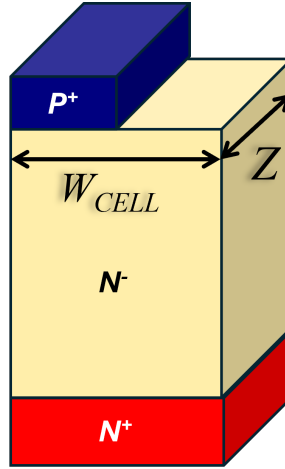


Figure 5.10. Schematic 3D illustration of simplified 4H-SiC MPS

5.4 Geometry-Scalable Physically-Based SPICE Compact Model for SiC MPS Diodes Including the Snapback Mechanism

This section presents a geometry-scalable electrothermal compact circuit model for 4H-SiC merged-PiN-Schottky (MPS) diodes, readily implementable in any SPICE-like simulator. The methodology and its validation have been extensively described in [6, 7, 8]. Here, we focus on the **geometric modeling** aspect, while the electrothermal modeling will be discussed in the following section. The proposed model accurately describes the behavior of a SiC MPS diode as a function of the cell width W_{Cell} and the PiN portion ratio $x(= W_{\text{PiN}}/W_{\text{Cell}})$, while also capturing the detrimental *snapback* phenomenon.

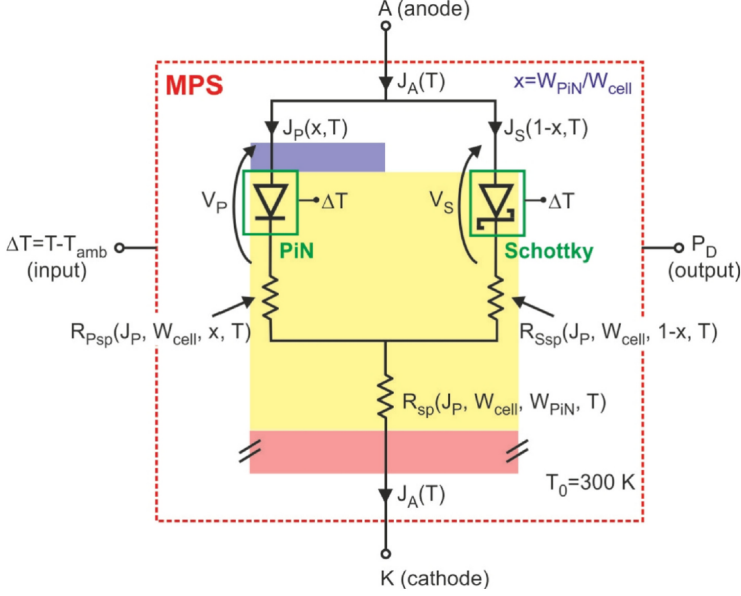


Figure 5.11. Sketch of the proposed model, which, apart from the standard anode and cathode terminals, is equipped with an input thermal node and an output power node to account for the electro-thermal (ET) feedback. Here, J_A , J_P , and J_S [A/cm^2] are the anode current density and the individual current densities conducted by the PiN and Schottky portions, respectively; $R_{P,sp}$, $R_{S,sp}$, and R_{sp} [$\Omega \cdot \text{cm}^2$] are the specific resistances of the PiN and Schottky portions, and of the drift region traversed by J_A .

Snapback Mechanism The snapback mechanism is associated to the presence of an NDR branch in the J_A - V_{AK} characteristic. In an MPS structure, two conditions are necessary for the occurrence of the snapback: (i) the ratio W_{PiN}/d is not sufficiently high (Fig. 5.7) to ensure the full polarization of the P^+N^- junction, and (ii) there is an increase in conductivity when the P^+N^- junction injects minorities into the drift region (conductivity modulation). The first condition is explained with the help of Fig. 5.12(a) which compares the electrostatic potential distributions of a snapback-affected device and a snapback-free one.

A low ratio W_{PiN}/d , like the one of the elementary cell in Fig. 5.12(a), only allows a small part of the voltage applied to the ends of the device

(V_{AK}) to actually bias the P^+N^- junction. For this reason, a V_{AK} significantly greater than the built-in potential (V_{BI}) must be applied to turn on the P^+N^- junction. Such a mechanism can be further clarified through the lumped-parameters model of Fig. 5.11.

The model consists of two branches in parallel, the first composed of a Schottky diode and a specific series resistance R_{Ssp} and the second by a P^+N^- diode and a specific series resistance R_{Psp} . Both connect to a common specific resistance R_{sp} .

When the Schottky diode begins to inject electrons, the current will flow into both R_{Ssp} and R_{sp} , thus producing two voltage drops with two opposite effects. While the voltage drop on R_{Ssp} promotes the activation of the P^+N^- diode, the voltage drop on R_{sp} will have the effect of delaying the activation of the P^+N^- diode. In a structure with a low W_{PiN}/d (Fig. 5.12(a)), the value of R_{sp} is large enough to produce a voltage drop such as to delay the activation of the P^+N^- junction. On the other hand, in a structure with a high value of W_{PiN}/d (Fig. 5.12(b)), the value of R_{sp} is negligible with respect to that of R_{Ssp} and most of V_{AK} is applied to the P^+N^- junction (Fig. 5.12(b)).

Once the P^+N^- junction begins to inject holes into the drift region, the concentration of minorities approaches and then exceeds that of the N^- doping. This increase in minorities within the drift region results in an increase in conductivity known as conductivity modulation; hence, the V_{AK} (initially due to the Schottky current only) reduces, thus increasing the effective portion of V_{AK} falling across the P^+N^- junction (positive feedback). As a result, a further increase in the MPS current (which now includes the bipolar PiN current) is sustained by a reduction in V_{AK} , that is, a snapback point followed by an NDR branch is observed (Fig. 5.13).

As we mentioned in the previous section, a criterion allowing to distinguish between a snapback-affected (unoptimized) and a snapback-free (optimized) structure was developed in [3]. Specifically, a device where:

$$\frac{W_{PiN}}{d} < \frac{1}{\tan \theta}$$

is unoptimized, whereas a device with:

$$\frac{W_{PiN}}{d} > \frac{1}{\tan \theta}$$

is optimized.

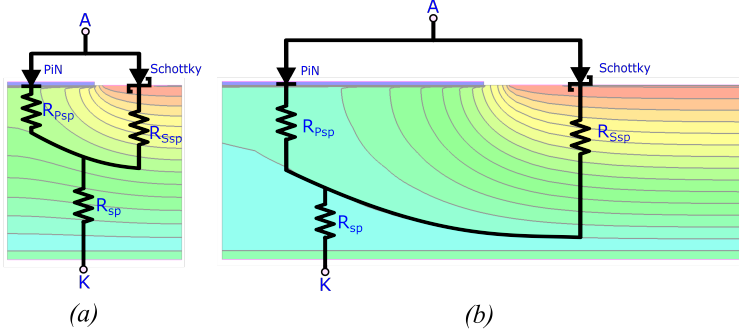


Figure 5.12. Overlap between the simplified lumped element circuit and the potential distribution for (a) a snapback-affected and (b) snapback-free device.

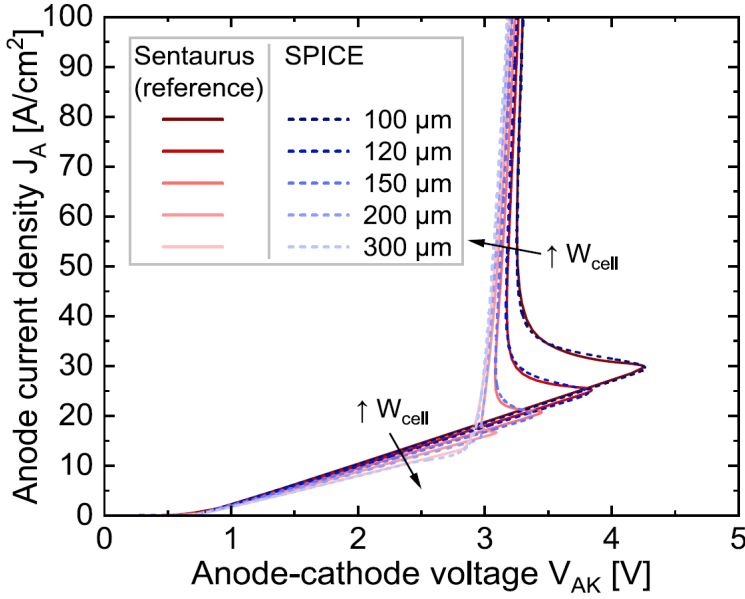


Figure 5.13. Senteraus TCAD (solid red lines, reference) and SPICE (dashed blue) isothermal (ET feedback deactivated) J_A - V_{AK} characteristics for $W_{cell} = 100, 120, 150, 200, 300 \mu\text{m}$, $W_{PiN} = W_{Schottky}$, and $T_{amb} = T_0 = 300 \text{ K}$.

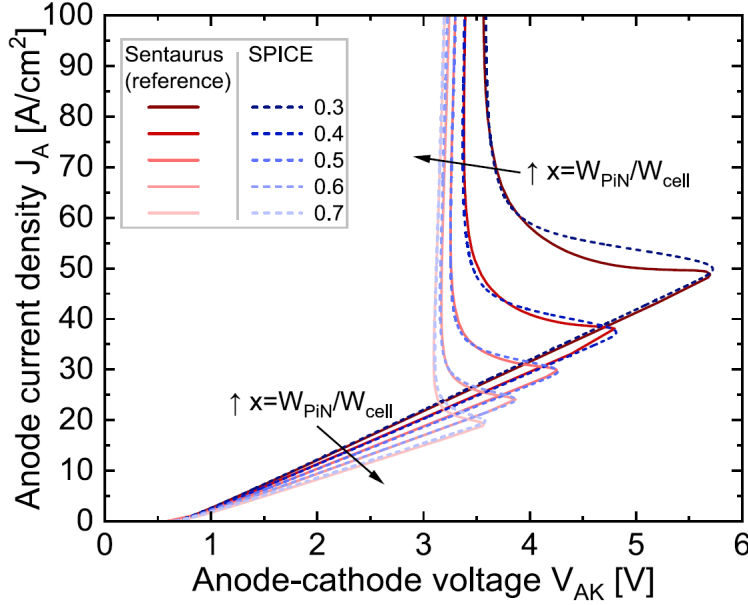


Figure 5.14. Senterus TCAD (solid red lines, reference) and SPICE (dashed blue) isothermal J_A - V_{AK} characteristics for $x = W_{\text{PiN}}/W_{\text{Cell}} = 0.3, 0.4, 0.5, 0.6, 0.7$, with $W_{\text{Cell}} = 100 \mu\text{m}$ and $T_{\text{amb}} = T_0 = 300 \text{ K}$. The model starts to deviate from the TCAD simulation as x decreases, which can be attributed to the decreasing validity of the assumption of a linearly spreading current.

TCAD Simulations and Parameter Extraction Two-dimensional TCAD simulations were performed using Synopsys Senterus, solving the Poisson and carrier continuity equations with a FEM-based approach [9]. The reference device structure consists of an N^- drift layer with doping $N^- = 7 \times 10^{14} \text{ cm}^{-3}$ and thickness $d = 95 \mu\text{m}$, chosen to achieve a blocking voltage of approximately 10 kV. However, all of these data are summarized in Table 3.

Two simulation campaigns were conducted:

- In the first campaign, W_{Cell} was varied between 100 and 300 μm while keeping $W_{\text{Schottky}} = W_{\text{PiN}}$.
- In the second campaign, $W_{\text{PiN}}/W_{\text{Cell}}$ was varied at a fixed $W_{\text{Cell}} =$

100 μm .

Obviously, the simulations were carried out while keeping the total device area constant at 1 cm^2 , according to the following simple relation:

$$Z = \frac{1 \text{ cm}^2}{W_{\text{Cell}}}$$

where Z is the cell length in the direction orthogonal to the cross section (see Fig. 5.10).

The simulation mesh included approximately 3000 nodes and 6000 elements (see Fig. 5.15). The Schottky barrier height was optimized to 1.09 eV to match experimental data reported in [3]. Each I - V curve required about 5 minutes of CPU time on a workstation with four Intel Xeon E7-8880v4 CPUs and 250 GB RAM. Additional simulations were run with the PiN and Schottky portions alternately removed to assist parameter extraction for the SPICE compact model.

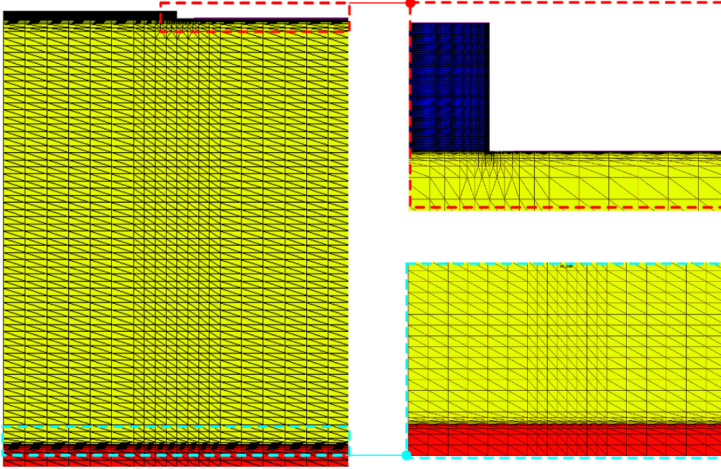


Figure 5.15. 2-D Geometry/mesh of the MPS diode in the Sentaurus TCAD environment and magnified views of the mesh refinement at the contacts and doping transition regions. The anode current provided by Sentaurus was multiplied by a proper factor to obtain the current density J_A [$\frac{\text{A}}{\text{cm}^2}$].

Geometric MPS Compact Model The MPS model was implemented in the form of a SPICE-compatible subcircuit and is illustrated in Fig. 5.11. The model, as mentioned before, consists of two parallel branches placed in series with a current-dependent specific resistance R_{sp} ; one branch includes the series connection of a P^+N^- diode and a current-dependent specific resistance R_{Psp} , while the other branch is composed of the series of a Schottky diode and a current-dependent specific resistance R_{Ssp} . The J_P density current dependence of R_{sp} and R_{Psp} is ascribable to conductivity modulation. This is supported by the hole distribution reported in Fig. 5.16, which shows that R_{sp} and R_{Psp} lie in the hole-flooded region;

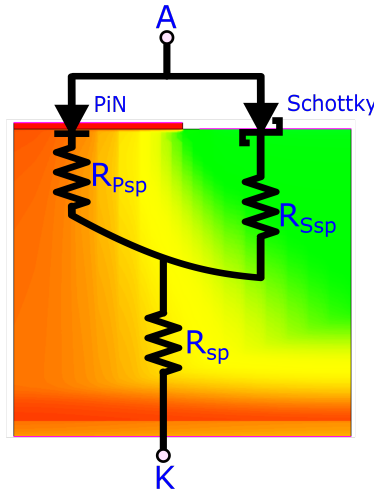


Figure 5.16. Overlap between the simplified circuit model and the holes distribution at the conductivity modulation onset.

therefore, when the J_P current increases, R_{sp} and R_{Psp} decrease. Nevertheless, R_{Psp} tends to a limit value R_0 ; the functional dependences of R_{sp} and R_{Psp} on the PiN current can be expressed as follows:

$$R_{sp}(J_P) = \frac{R_{u2}}{1 + \alpha J_P}, \quad (5.18)$$

$$R_{Psp}(J_P) = \frac{R_{u1}}{1 + \alpha J_P} + R_0 \quad (5.19)$$

where R_{u1} and R_{u2} are the specific resistance values under Schottky unipolar current condition ($J_P = 0$) offered by Region 1 and Region 2, respectively (Fig. 5.8), while R_0 as well as α are geometry-dependent fitting functions. Conversely, the value of R_{Ssp} grows with increasing J_P because the unipolar current path becomes less preferred with respect to the bipolar current path. The relation between R_{Ssp} and J_P was modeled according to the following equation:

$$R_{Ssp}(J_P) = R_{u1} + \gamma J_P \quad (5.20)$$

where γ is a fitting parameter shown in Table 4. The approach adopted to derive the expressions of R_{u1} and R_{u2} is based on the JBS current distribution model, as widely described in Section 5.2.2, with the consideration that, in our case study (10 kV 4H-SiC MPS), we have an epitaxial P⁺ region and therefore no channel region (and consequently no channel resistance).

In this approach, the two-dimensional current flow during unipolar operation is assumed to be divided into only two parts as shown in Fig. 5.8: the current spreading region (Region 1) and the uniform current-flow region (Region 2). In particular, the current is assumed to linearly diffuse in Region 1 with a spreading angle θ . For a given doping N^- , θ is almost insensitive to the MPS geometry and is therefore considered constant. Then, considering that the current flux distribution is uniform in Region 2 (as described in Section 5.2.2), it is possible to exploit the following formula:

$$R_{u2} = \rho (d - W_{PiN} \tan \theta) \quad (5.21)$$

while the spreading resistance under unipolar regime, here called R_{1u} , is calculated exploiting the same approach used for Equation 114:

$$R_{u1} = \rho \tan \theta \ln \left(\frac{W_{Cell}}{W_{Schottky}} \right) W_{Cell} \quad (5.22)$$

In these expressions, ρ is the resistivity value obtained from TCAD simulations under unipolar current condition ($J_P = 0$), which is reported in Table 5. Fig. 5.13 shows the comparison between the J_A - V_{AK} characteristics of the SPICE model and those obtained from TCAD simulations by varying W_{Cell} , keeping the same widths of the Schottky and PiN por-

tions. Subsequently, the model accuracy was verified for $W_{\text{PiN}} \neq W_{\text{Schottky}}$; Fig. 5.14 shows TCAD and SPICE $J_{\text{A}}-V_{\text{AK}}$ characteristics by varying the $W_{\text{PiN}}/W_{\text{Cell}}$ ratio.

Fitting Functions The fitting functions α and R_0 were identified by comparing the Sentaurus $J_{\text{A}}-V_{\text{AK}}$ characteristics of the MPS diode with those of SPICE under bipolar-current condition ($J_{\text{P}} > 0$). The parameter α can be described as the rate of conductivity modulation, and its dependence on the geometry can be explained as follows: a wider W_{PiN} causes a better polarization of the P^+N^- junction and thus, a higher injection rate of the holes into the drift region. As described by Eq. (5.23), α was modeled as a linear function of both $x = W_{\text{PiN}}/W_{\text{Cell}}$ and W_{Cell} , where α_0 and k^* are fitting parameters shown in Table 4, and W_0 is the reference cell width, set to 100 μm .

$$\alpha(W_{\text{Cell}}, x) = \alpha_0 + \frac{W_{\text{Cell}} - W_0}{W_0} + k^* \cdot (x - 0.5) \quad (5.23)$$

Finally, the parameter R_0 represents the lower bound of the conductivity-modulated resistance. Differently from α , it only depends on the total cell width W_{Cell} and not on the ratio $W_{\text{PiN}}/W_{\text{Cell}}$, and its variation was modeled as follows:

$$R_0 = \eta + \sqrt{\mu \cdot (W_{\text{Cell}} - W_0)} \quad (5.24)$$

where η and μ are fitting parameters reported in Table 5.2.

Table 5.2. Fitting parameters used in the MPS model.

Parameter	Value	Unit
α_0	0.475	cm^2/A
k^*	2.5	cm^2/A
η	1.06×10^{-3}	$\Omega \cdot \text{cm}^2$
μ	2.88×10^5	$\Omega^2 \cdot \text{cm}^3$
γ	1.15×10^{-3}	$\text{cm}^4\Omega/\text{A}$

5.4.1 Electrothermal Compact Model for SiC MPS Diodes Including the Snapback Mechanism

In the previous section, we focused on the geometric modeling of the circuit components shown in Fig. 5.11. In this section, we address the thermal modeling. This section is organized as follows: first, we present the mathematical modeling of the thermal problem, followed by the parameter calibration procedure, and finally the results of the electrothermal simulation.

Thermal Modeling Since in most SPICE-like circuit simulators the temperature is treated as a fixed (i.e., power-independent) parameter common to all components in the schematic, we employed the *thermal equivalent of Ohm's law* (TEOL), i.e., the thermal-electrical analogy, in order (i) to allow temperature-sensitive electrical parameters to vary dynamically during the simulation run and (ii) to enable different temperatures to be assigned to different devices/cells in case of multiple components. With the TEOL approach, temperatures, powers, and thermal resistances are represented as voltages, currents, and electrical resistances, respectively.

To explain the thermal modeling more effectively, we conceptually expand the circuit proposed in Fig. 5.11, moving from a high-level circuit representation (Fig. 5.11) to a lower-level representation (Fig. 5.17), which allows us to illustrate in detail how the thermal modeling was performed. Therefore, in this section, we will refer to the circuit in Fig. 5.17. As can be seen from Fig. 5.17, besides the anode and cathode terminals, the subcircuit is equipped with two additional nodes: an input node that provides the model with the temperature rise ΔT , and an output node that reports the dissipated power P_D . In the next sections, these nodes will be used to perform a static electrothermal (ET) simulation. The core components of the subcircuit are standard resistance-free diode instances at T_0 for the PiN and Schottky diodes.

Let us first consider the PiN diode. This device conducts the current:

$$J_P(T_0) = J_{P0} \left[\exp\left(\frac{V_P}{V_{T0}\eta_P}\right) - 1 \right] \quad (5.25)$$

where V_P is the voltage drop across the diode, J_{P0} and $V_{T0} = 0.02586$ V are the reverse saturation current density and thermal voltage at T_0 , re-

spectively, and η_P is the ideality factor.

The influence of the input temperature rise ΔT is included by placing in parallel with the diode a voltage-controlled current source that injects a correction current given by:

$$J_{P,\text{corr}}(T) = J_{P0} \left[\exp \left(\frac{V_P + \varphi_{0P}(T - T_0)}{V_T \eta_P} \right) \right] - J_P(T_0) \quad (5.26)$$

where $T = \Delta T + T_{\text{amb}}$, $V_T = kT/q$ ($k = 8.62 \times 10^{-5}$ eV/K being the Boltzmann constant), and φ_{0P} [V/K] is a temperature coefficient. The resulting current is:

$$J_P(T) = J_P(T_0) + J_{P,\text{corr}}(T) = J_{P0} \left[\exp \left(\frac{V_P + \varphi_{0P}(T - T_0)}{V_T \eta_P} \right) \right] \quad (5.27)$$

This approach was chosen because it was found to accurately reproduce the electrothermal behavior of junctions across a wide range of technologies (e.g., [10, 11]).

The resistance-free Schottky diode is modeled in a similar way. At T_0 , it conducts:

$$J_S(T_0) = J_{S0} \left[\exp \left(\frac{V_S}{V_{T0} \eta_S} \right) - 1 \right] \quad (5.28)$$

where V_S , J_{S0} , and η_S have the same meaning as their PiN diode counterparts. A voltage-controlled current source is connected in parallel to generate a correction current:

$$J_{S,\text{corr}}(T) = J_{S0} \left[\exp \left(\frac{V_S + \varphi_{0S}(T - T_0)}{V_T \eta_S} \right) \right] - J_S(T_0) \quad (5.29)$$

yielding the total current:

$$J_S(T) = J_S(T_0) + J_{S,\text{corr}}(T) = J_{S0} \left[\exp \left(\frac{V_S + \varphi_{0S}(T - T_0)}{V_T \eta_S} \right) \right] \quad (5.30)$$

The specific series resistances R_{Psp} and R_{Ssp} of the PiN and Schottky diodes are modeled as in Eqs. (116) and (117) but with temperature de-

$$R_{Psp} = R_0 + \frac{R_{u1} \left(\frac{T}{T_0} \right)^{m_T}}{1 + \alpha J_P \left(\frac{T}{T_0} \right)^{m_\alpha}} \quad (5.31)$$

$$R_{Sp} = R_{u1} \left(\frac{T}{T_0} \right)^{m_T} + \gamma J_P \left(\frac{T}{T_0} \right)^{m_\gamma} \quad (5.32)$$

$$R_{sp} = \frac{R_{u2} \left(\frac{T}{T_0} \right)^{m_T}}{1 + \alpha J_P \left(\frac{T}{T_0} \right)^{m_\alpha}} \quad (5.33)$$

The diagram illustrates the internal structure of a Micro Power Source (MPS) enclosed in a dashed blue box. The top terminal is labeled 'A (anode)' and the bottom terminal is labeled 'K (cathode)'. An input terminal on the left is labeled $\Delta T = T - T_{amb}$ Input, and an output terminal on the right is labeled P_D output. Inside the box, the MPS consists of two main branches: a PiN branch and a Schottky branch. The PiN branch includes a PiN diode, a Schottky diode, and a resistor $R_{Psp}(J_P, T)$. The Schottky branch includes a Schottky diode, a Schottky diode, and a resistor $R_{Ssp}(J_P, T)$. The total current $J_A(T)$ flows from the anode through the PiN and Schottky branches to the cathode. The diagram also shows various current densities ($J_P(T)$, $J_S(T)$, $J_{P,corr}(T)$, $J_{S,corr}(T)$) and voltages (V_P , V_S) associated with the diodes. A temperature parameter $T_0 = 300\text{ K}$ is indicated at the bottom left.

Figure 5.17. Representation at low level of the SPICE-compatible subcircuit implementing the analytical thermal model.

Parameter Calibration The calibration procedure for the model parameters is as follows. Parameters J_{S0} and η_S were optimized by comparing the Sentaurus characteristic of the structure without the PiN contact to the SPICE characteristic of the standard diode at $T_{\text{amb}} = T_0$ and $V_{AK} < 0.7$ V. The coefficient φ_{0S} was adjusted to achieve the best match between Sentaurus and SPICE characteristics at higher T_{amb} over the same V_{AK} range, where the thermionic effect results in a positive temperature coefficient.

A temperature-sensitive series resistance was then connected to the Schottky diode, with its value at T_0 tuned to match Sentaurus and SPICE results for $V_{AK} > 0.7$ V. In this range, a negative temperature coefficient is observed since the reduction in electron mobility in the drift region with increasing T_{amb} outweighs the increased thermionic emission. Assuming a temperature dependence $(T/T_0)^{m_T}$, the factor m_T was optimized by comparing Sentaurus and SPICE results for several T_{amb} .

The same procedure was applied to the structure without the Schottky contact, allowing calibration of J_{P0} , η_P , and φ_{0P} . The fitting functions R_0 , α , and γ were optimized to match the $J_A \sim V_{AK}$ characteristics from Sentaurus and SPICE simulations of the MPS at $T_{\text{amb}} = T_0$, as previously discussed in the section on geometric modeling. Parameters m_α and m_γ were tuned to achieve agreement between Sentaurus and SPICE results at T_{amb} in the range 320–400 K. These parameters are reported in Table 5.3, while the final comparison between Sentaurus and SPICE results is shown in Fig. 5.18. Notably, a single SPICE simulation run required less than 1 s on a standard PC.

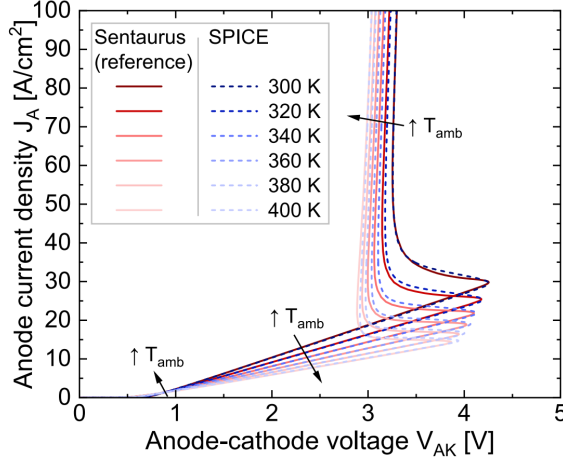


Figure 5.18. Sentaurus TCAD (solid red lines, reference) and SPICE (dashed blue) isothermal J_A - V_{AK} characteristics for $T_{\text{amb}} = 300, 320, 340, 360, 380, 400$ K, $W_{\text{cell}} = 100 \mu\text{m}$, and $W_{\text{PIN}} = W_{\text{Schottky}}$.

Electrothermal Simulation An electrothermal simulation, made possible through the TEOL-based approach, was performed by scaling the area-dependent model parameters and fitting functions to emulate a 4H-SiC MPS with $1.5 \text{ cm} \times 1.5 \text{ cm}$ area in a TO-247 (or TO-263) package at $T_{\text{amb}} = T_0 = 300$ K. The dissipated power $P_D = I_A \cdot V_{AK}$ (represented as a current in SPICE according to TEOL) was forced through a junction-to-ambient thermal resistance $R_{\text{TH}} = 0.5 \text{ K/W}$ (represented as an electrical resistance). The resulting temperature rise $\Delta T = T - T_{\text{amb}} = R_{\text{TH}} \cdot P_D$ (a voltage drop) was fed back to the model to update temperature-sensitive parameters. This approach inherently assumes a uniform temperature across the entire device. The ET simulation took less than 1 s on a standard PC. Results are illustrated in Fig. 5.19, where the ET I_A - V_{AK} characteristic is compared with the isothermal counterpart (self-heating disabled, $T = T_{\text{amb}}$). It is evident that self-heating causes a significant distortion of the curve relative to the isothermal case; more specifically, the thermally induced increase in resistances leads to a marked current reduction in both unipolar and bipolar conduction modes, as well as a suppression of the current triggering the snapback mechanism.

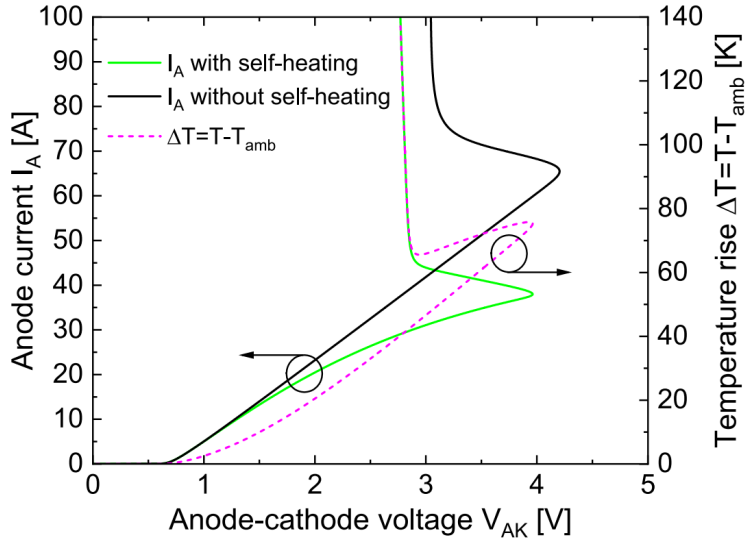


Figure 5.19. Outcomes of the ET simulation executed by SPICE. The I_A - V_{AK} characteristic of a $1.5 \text{ cm} \times 1.5 \text{ cm}$ 4H-SiC MPS with the ET feedback activated (left axis, solid green line) is shown along with the corresponding temperature rise above ambient ΔT (right axis, dashed magenta line). The thermal resistance R_{TH} (represented in SPICE as a standard electrical resistance according to the TEOL) was chosen equal to 0.5 K/W to emulate a TO-247 (or TO-263) package. Also shown is the isothermal I_A - V_{AK} curve at $T_{\text{amb}} = T_0$ (left axis, solid black line). Here, $W_{\text{cell}} = 100 \text{ }\mu\text{m}$ and $W_{\text{PiN}} = W_{\text{Schottky}}$.

Table 5.3. Calibrated electrothermal model parameters.

Parameter	Value	Unit
J_{P0}	1.9×10^{-45}	A/cm ²
η_P	1.027	—
φ_{0P}	1.08×10^{-2}	V/K
J_{S0}	1.1×10^{-12}	A/cm ²
η_S	1.0	—
φ_{0S}	3.75×10^{-3}	V/K
m_T	2.25	—
m_α	4	—
m_γ	7	—

5.4.2 Putting the Model to the Test: Application to the Surge Current Event

At the beginning of this chapter, we stated that SiC MPS diodes are preferred in applications where it is not possible to significantly reduce the system’s exposure to high current surges. Indeed, thanks to their bipolar conduction capability, this class of diodes can handle higher current levels compared to standard JBS diodes. However, these devices require proper geometrical design optimization; otherwise, the advantage of having bipolar conduction can turn into a drawback, as in the case of snapback.

As we have already explained, it is common practice among companies manufacturing power semiconductor devices to place multiple dice within the same package. This allows achieving very high rated currents while simultaneously maximizing yield (understood as the number of good dice per wafer). However, if this procedure is applied to non-optimized SiC MPS diodes — that is, diodes affected by snapback — it can result in severe current-focusing phenomena when several dice are connected in parallel within the same package, thereby significantly reducing device reliability.

In the following, using our geometry-scalable electrothermal compact circuit model of 4H-SiC MPS diodes, we simulate a possible scenario in which an inevitable technological mismatch generates an asymmetry in device behavior.

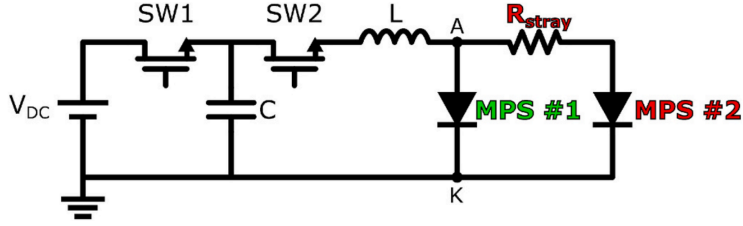


Figure 5.20. Simplified circuit schematic of the simulated resonant surge test setup.

For this purpose, a dynamic ET simulation of a resonant surge test was executed in SPICE. The analyzed setup, shown in Fig. 5.20, makes use of two paralleled MPS diodes to boost the current capability and operates as follows. First, capacitor C is charged to the DC supply voltage through switch SW1. Then, SW2 is closed, allowing the inductor L and capacitor C to resonate at a frequency $f = \frac{1}{2\pi\sqrt{LC}}$, thus discharging C through the paralleled MPS diodes under test. The values of L and C are typically chosen to achieve a resonance frequency $f = 50$ Hz [14], resulting in a half-sine current pulse of 10 ms being forced through the diodes.

Since the maximum temperature develops near the surface of the device on the anode side [15], the single-event temperature limit leading to device failure is typically associated with the melting temperature of the top aluminum metallization. Consequently, a temperature limit of approximately 1000 K is commonly used to indicate device destruction in simulations [?].

An unavoidable technological discrepancy between the two MPS diodes was emulated by adding a $1\text{ m}\Omega$ series resistance R_{stray} to MPS #2. This resistance may represent, for example, an asymmetry in the length of the metal interconnections, partial oxidation of a metallization, or, more generally, imperfections in electrical contact formation.

Fig. 5.21 compares the ET I_A - V_{AK} characteristic of the unbalanced MPS #2 with that of MPS #1. It can be observed that MPS #2: (i) suffers from a slightly lower current flow under unipolar conduction mode (positive differential resistance region, PDR), (ii) exhibits snapback at a higher V_{AK} , and (iii) conducts more current beyond snapback, i.e., in the negative differential resistance regions NDR1 and NDR2.

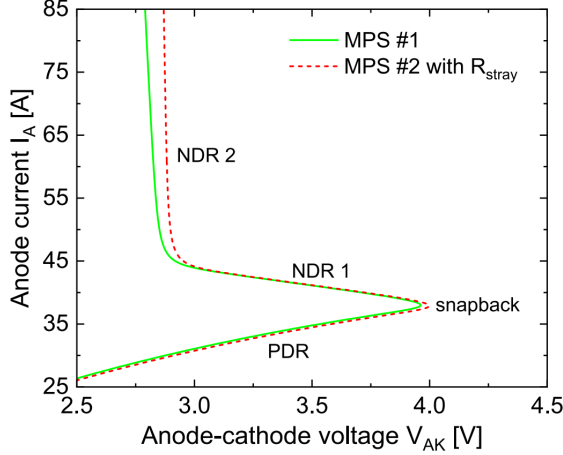


Figure 5.21. ET I_A - V_{AK} characteristics of the 1.5 cm $\times$ 1.5 cm 4H-SiC MPS #1 (solid green line, also reported in Fig. 8) and MPS #2 intentionally unbalanced with R_{stray} (dashed red line).

The SPICE simulation of the resonant surge test was performed by including a thermal capacitance (0.2 mJ/K) in parallel with the thermal resistance (0.5 K/W) of each MPS diode. The results are shown in Fig. 22. As the total anode current increases, the paralleled MPS diodes initially conduct almost the same current under unipolar mode (MPS #1 slightly prevails). After snapback (observable as a V_{AK} peak) is reached, this behavior reverses and MPS #2 starts conducting more current.

Then, a bifurcation phenomenon takes place: MPS #1 remains on the NDR1 region, while MPS #2 moves upward along the NDR2 branch. This transition occurs because, as the total current rises, MPS #2 is the first to enter the steeper NDR2 region, which attracts more current due to its lower resistance, thus providing a favorable path for current flow.

This phenomenon is detrimental because MPS #2 eventually bears most of the current, leading to a significant temperature rise (up to 200 K above T_{amb}). Such a high temperature further exacerbates current crowding through positive feedback: as shown in Fig. 5.19, it lowers the current threshold at which the NDR branches appear, making it even easier for MPS #2 to transition into the NDR2 region.

Eventually, both the total current and the current conducted by MPS

#2 decrease until snapback is reached again. Afterward, the current of MPS #1 drops along the unipolar PDR region, while MPS #2 attempts to climb back along the NDR1 branch.

All simulations were completed within a few seconds, regardless of the simulation tool used.

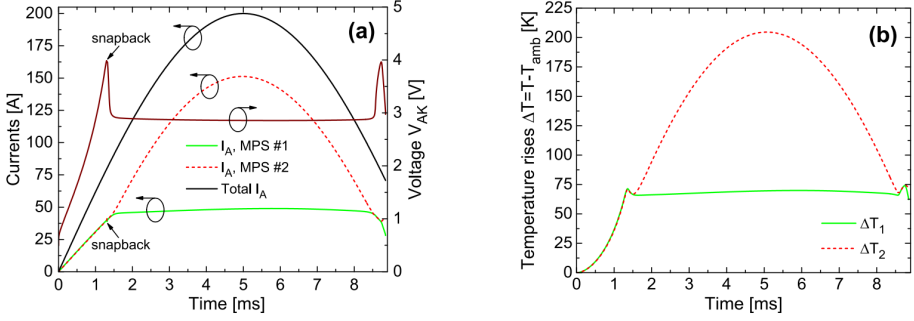


Figure 5.22. ET dynamic SPICE simulation of the surge test: (a) currents conducted by the two MPS diodes, as well as total current (left axis) and voltage V_{AK} (right axis); (b) temperature rises over ambient vs. time. Solid green lines are associated with MPS #1, whereas dashed red lines correspond to MPS #2 enriched with R_{stray} .

The dynamic ET simulation of a resonant surge test has evidenced that paralleling NDR-affected MPS devices is an unfortunate choice, as unavoidable technological discrepancies among them may lead to a markedly uneven current/temperature distribution, the hottest diode being thus prone to accelerated reliability degradation and reduction in mean time-to-failure. As the proposed model facilitates fast and accurate holistic analyses under various operational conditions, we believe that it can be fruitfully used as a valuable means to optimize the design of 4H-SiC MPS rectifiers, as well as of circuits based upon them.

5.5 Packaging Strategies for Boosting Surge Current Robustness of SiC JBS Diodes

In the previous sections, we analyzed the Merged PiN Schottky (MPS) structure and repeatedly emphasized that these devices are capable of handling higher current surges compared to their Junction Barrier Schottky (JBS) counterparts. This superior performance is enabled by their ability to exploit bipolar conduction.

In principle, JBS structures could also benefit from bipolar conduction, but the triggering conditions are much more difficult to achieve — requiring higher voltages and/or elevated temperatures — since they lack a dedicated ohmic contact on the P-region.

Nevertheless, other technological degrees of freedom can be exploited to improve the ability of a JBS diode to handle high surge current events. One example is the optimization of bonding techniques used to connect the dice within the package.

In this section, the surge current capability of a 60 A–1200 V 4H-SiC diode, fabricated by paralleling two 30 A dice, is experimentally evaluated. Three bond wire configurations are investigated using a nonrepetitive surge current test at 25 °C and 110 °C. The results reveal that the stitch configuration, which employs 3×20 mil bonding wires, significantly outperforms the alternative 4×15 mil and 4×12 mil counterparts in terms of maximum surge current robustness. An extensive analysis is also conducted to identify key differences in the failure mechanisms among the three configurations during surge current stress. A detailed discussion of this study is available in [16].

Introduction. As already mentioned, device manufacturers commonly embed two SiC dice in parallel within the same package to increase current capability. This approach offers two key advantages: (i) it improves fabrication yield, and (ii) it avoids modifications to the existing semiconductor production line. However, the parallel operation of multiple chips may result in uneven current sharing, requiring derating rules that limit full device utilization [17]. A device’s ability to withstand non-repetitive surge current events is quantified by the maximum single-pulse forward surge current (I_{FSM}) [18], defined as the amplitude of a 10 ms half-sine wave

current pulse applied before device failure [19, 20]. The surge current robustness of 4H-SiC JBS diodes has been previously studied for both single [21] and parallel dice [22]. However, to the best of our knowledge, no studies have examined the impact of sub-optimal bonding when paralleling diodes within the same package. In this section, we address this gap by assessing the surge current robustness of a SiC JBS composed of paralleled dice for different bond wire configurations between the dice. Our extensive experimental analysis includes the measurement of forward pulsed I-V characteristics, thermal resistance (R_{TH}) extraction, I_{FSM} evaluation, and post-failure imaging of the dice — obtained after chemical decapsulation and metal removal — to identify damage differences among the examined configurations.

Devices Under Test and Experimental Setup. The device under test (DUT) is a 60 A–1200 V 4H-SiC JBS diode composed of two 30 A dice connected in parallel within a TO-247 package. For a single die, three 20 mil bond wires are typically used (Fig. 5.23a). However, when two dice are placed in parallel within the same package, the limited space available on the T-Post lead prevents the use of two 20 mil bond wires per die, which would overlap and potentially cause physical damage (Fig. 5.23b). To address this limitation, three alternative bond wire configurations were implemented and tested (Fig. 5.24). In the first two configurations (Fig. 5.24a–b), the two 30 A dice are connected in parallel using four 12 mil and 15 mil bond wires, respectively, with two wires directly connecting the T-Post to each die. In the third configuration (Fig. 5.24c), three 20 mil bond wires are used to connect one die to the other, with only one die directly linked to the T-Post. This third configuration is referred to as the stitch configuration. A total of ten samples were fabricated for each configuration to ensure consistency in the experimental evaluation.

The I_{FSM} was evaluated using a resonant surge tester, as shown in Fig. 5.25a. In this test, a 10 ms half-sinusoidal current pulse (Fig. 5.25b) is applied to the DUT by charging the capacitor C to a given supply voltage and then discharging it through the inductor L . Robust devices must exhibit an I_{FSM} value at least ten times the nominal current rating.

Before performing the surge current tests, all DUTs underwent preliminary characterization to ensure proper bonding and reproducible electrical

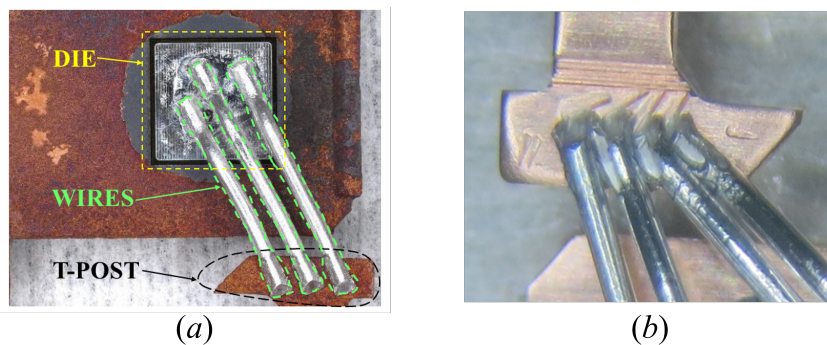


Figure 5.23. Top view of (a) a single-die 30 A–1200 V SiC JBS diode using three bond wires and (b) the T-Post with four 4×20 mil diameter bond wires (two per die for the two-die 60 A–1200 V DUT) detailing how these come in contact.

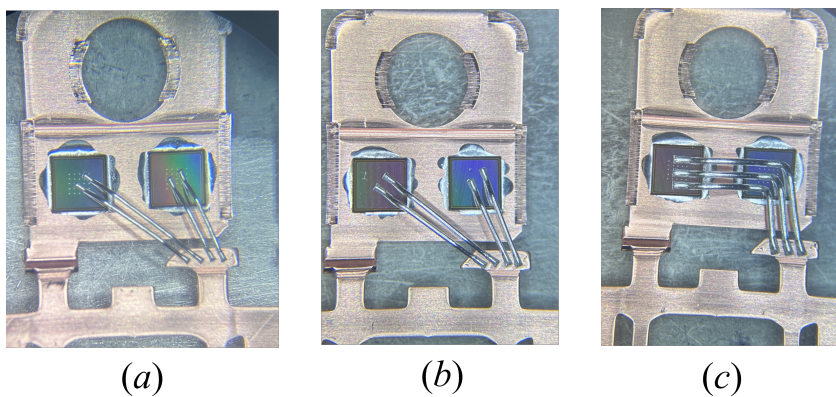


Figure 5.24. Pictures of the parallel dies attached on the TO-247 lead frame showcasing three different bond wire configurations: (a) 4×12 mil, (b) 4×15 mil, and (c) 3×20 mil (referred to as stitch).

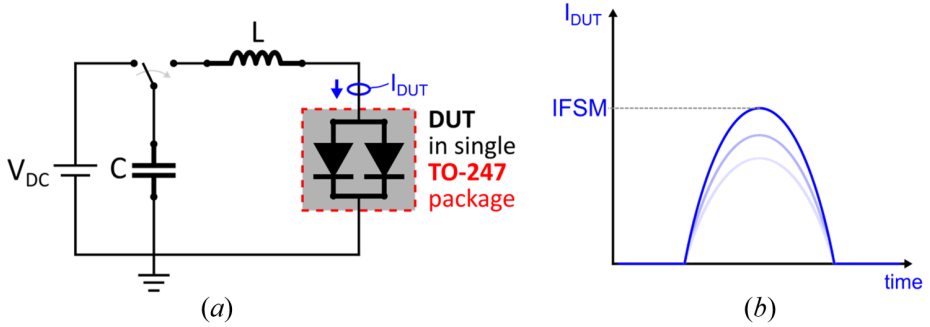


Figure 5.25. Schematic representation of (a) the surge current test setup and (b) the consecutive semi-sinusoidal current pulses.

behavior. The first step involved measuring pulsed (isothermal) forward I_F – V_F characteristics at both 25 °C and 175 °C. The junction-to-case thermal resistance (R_{TH}) was then experimentally extracted for each sample. After this preliminary characterization, the DUTs were divided into two batches and subjected to surge current tests at 25 °C and 110 °C. Each device underwent consecutive surge pulses with the current amplitude increased in 5 A increments between tests. A 2 minute interval was maintained between pulses to prevent cumulative heating effects, and no active cooling was applied. A DUT was considered to have failed when its leakage current increased tenfold compared to its pre-test value. The I_{FSM} value was recorded as the last applied surge current before failure was detected. After failure, the DUTs were chemically decapsulated and the metallization and SiO_2 layers were removed to enable detailed analysis of the damage mechanisms.

Results and Failure Analysis. The pulsed (isothermal) forward I_F – V_F characteristics for the different bonding wire configurations are shown in Figs. 5.26 and 5.27. At 25 °C, the I_F – V_F curves corresponding to the stitch, 2×12 mil, and 2×15 mil configurations exhibit no significant deviation up to the rated current (60 A). Beyond this current level, slight divergences begin to appear among the curves, attributable to the increasing voltage drop across the bonding wires. This effect becomes more pronounced as the current exceeds 60 A, where resistive voltage drops not only in the intercon-

nect wires but also near the wire-to-metal contact areas become significant. As expected, the 4×15 mil configuration shows a lower forward voltage drop compared to the 4×12 mil configuration, owing to its 25% larger wire diameter. Interestingly, despite using only 3×20 mil wires, the stitch configuration achieves an even lower forward voltage drop, indicating that factors beyond total wire cross-sectional area — such as wire arrangement and bonding contact area — significantly influence performance. When the temperature is increased to 175°C , a marked reduction in the slope of all I_F – V_F curves is observed compared to the 25°C characteristics. This behavior is primarily caused by phonon scattering, which dominates over the enhanced majority carrier injection resulting from thermionic emission, leading to a significant decrease in the forward I_F – V_F slope at high temperatures. An interesting exception is found in the control device, which exhibits a local increase in slope around 5 V (see Fig 5.27). To interpret this, it is important to recall that the analyzed devices are SiC JBS diodes, whose elementary cell consists of alternating P^+ implanted regions and Schottky regions. Unlike MPS diodes, the P^+N^- junction in JBS devices is not designed to conduct during forward operation; its main function is to suppress reverse leakage current, as previously described. This design simplifies fabrication and reduces cost by eliminating the need for a dedicated masking step to form an efficient ohmic contact on the P^+ region before Schottky metal deposition. However, the ohmic contact formed on the P^+ region, although inefficient, is not completely inactive. At elevated temperatures, the P^+N^- junction exhibits a reduced built-in potential due to increased free carrier concentration in the depletion region. As a result, around 5 V, the P^+N^- junction may begin to inject minority carriers into the drift region, causing an increase in the forward I_F – V_F slope. In contrast, for an optimized MPS diode, this behavior would typically appear already at room temperature and at lower forward voltages, around 3.3 V.

Fig. 5.28 presents the measured thermal resistance (R_{TH}) values highlighting that no significant differences in R_{TH} were observed among the various device groups. Despite the relatively uniform I_F – V_F characteristics within each configuration and similar R_{TH} values across all groups, the surge test results revealed substantial differences among the three configurations. Figs. 5.29 and 5.30 show the surge test results at 25°C and 110°C ,

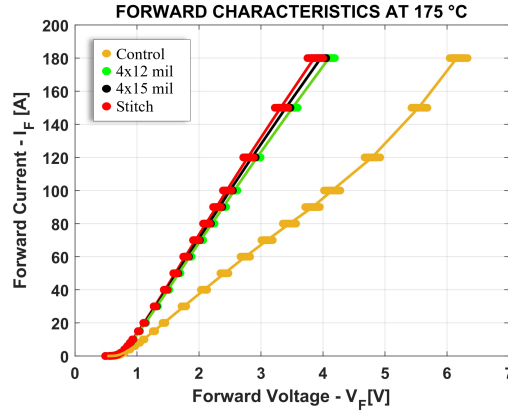


Figure 5.26. Experimental isothermal forward I_F - V_F characteristics at 25 °C for the three bond wire configurations.

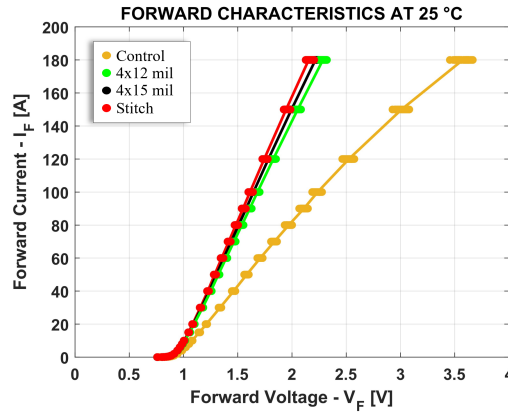


Figure 5.27. Experimental isothermal forward I_F - V_F characteristics at 175 °C for the three bond wire configurations.

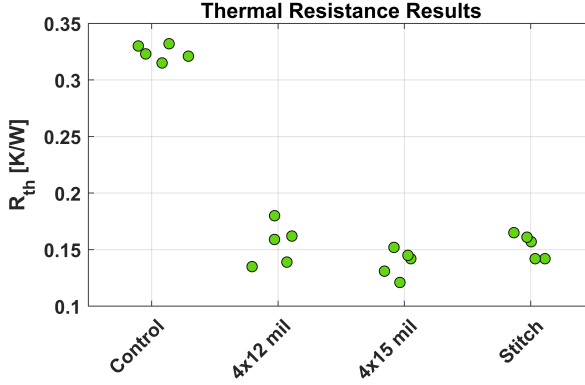


Figure 5.28. Extracted R_{TH} for the three configurations.

respectively, compared against a control device, a single 30 A–1200 V 4H-SiC diode with a standard 2×20 mil bonding wire configuration. The 4×12 mil and 4×15 mil configurations demonstrated significantly low surge robustness, with average I_{FSM} values of 460.5 A and 502.5 A, respectively, i.e., both falling well below the 10×60 A standard requirement. This result implies that a substantial derating is required compared to the theoretical 2×320 A expected from two parallel discrete control devices. In contrast, the stitch configuration achieved significantly higher I_{FSM} values and even met the 10×60 A requirement at 25 °C. This improved performance is attributed to the larger contact area between the wires and the top metal, which reduces voltage drops at the contacts under equal current conditions. The lower local power density and reduced heat concentration in this configuration help prevent metal melting in the contact regions during surge events, thereby minimizing degradation of the Schottky contact and preserving both blocking and forward characteristics. To further investigate the failure mechanisms observed in the surge test, a failure analysis was conducted. The devices were first chemically decapsulated to examine metal melting at the wire-to-metal contact points. The metallization was then removed through a delayering process to assess the structural integrity of the dice. Two distinct failure mechanisms were identified [22]:

- **Failure Type 1:** this failure is characterized primarily by metal melting at the contact areas, leading to Schottky contact degradation and deterioration of reverse characteristics. However, the diode retains some functionality.
- **Failure Type 2:** in addition to metal melting, this failure mode includes extensive structural damage, such as cracks in the chip and SiC substrate. The forward I_F - V_F curve becomes ohmic, indicating catastrophic device failure. This failure is strongly associated with high thermal stress and increased defect density in the substrate.

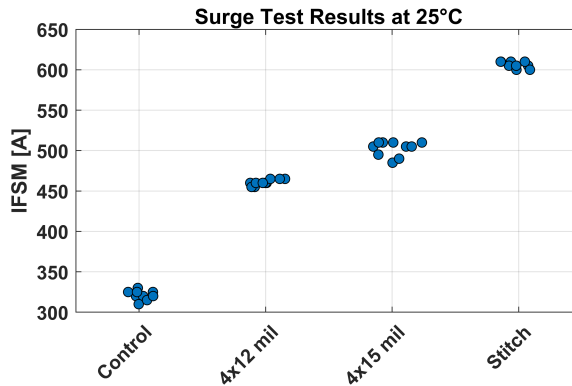


Figure 5.29. I_{FSM} results at 25 °C for the three configurations.

In the 4×12 mil and 4×15 mil configurations, both dies within the package exhibited Failure Type 2, characterized by severe melting of the metallization and structural damage (Figs. 5.31–5.32). By contrast, the stitch configuration, in some cases, exhibited a mixed failure pattern. In several instances, the die directly connected to the T-Post (right die) displayed features consistent with Failure Type 2: in addition to fusion between the bonding wires and the metallization, structural damage was observed, including cracks in the chip and in the SiC substrate (Figs. 5.33(b), (d), 5.34 and 5.35). This die exhibited neither blocking capability under reverse bias nor forward conduction. Conversely, the die located farther from the T-Post (left die) showed Failure Type 1, with localized melting between the bonding wires and the front-side metallization (Figs. 5.33(a), (c)). The

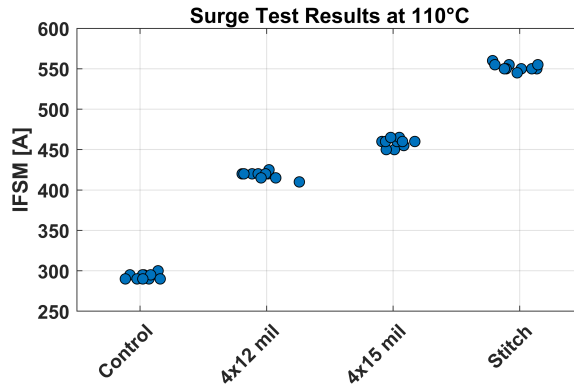


Figure 5.30. I_{FSM} results at 110 °C for the three configurations.

SiC substrate appeared essentially intact, and the die still retained a blocking capability (albeit degraded, as shown in Fig. 5.36). More specifically, within the stitch group, this asymmetric failure occurred in 3 of 10 devices tested at 25 °C and 4 of 10 devices tested at 110 °C. Only one device, belonging to the 25 °C test group, exhibited the inverse scenario, with the right die showing Failure Type 1 and the left die Failure Type 2. Notably, this sample had the lowest I_{FSM} among the stitch devices, although it still approached the 600 A requirement.

For all other devices in the stitch group, as well as for the 4×12 mil and 4×15 mil configurations, both dies exhibited Failure Type 2. This behavior can be rationalized by considering current distribution in the stitch configuration: the interconnect branch from the T-Post to the nearest die (right die) carries a higher current than the branch connecting the right die to the left die. As a result, the right die experiences greater Joule heating and thermal stress, making it more prone to Failure Type 2 than the left die.

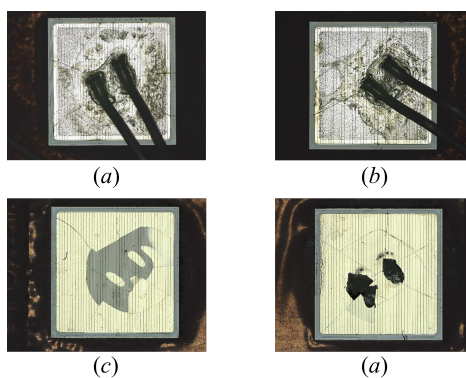


Figure 5.31. Left and right die of 4×12 mil bond wire configuration (a–b) after chemical decapsulation: evident burn marks on active area due to metal melting; (c–d) after delayering process: evident signs of cracks across active area.

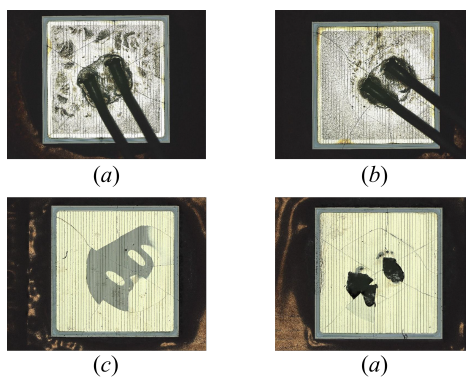


Figure 5.32. Left and right die of 4×15 mil bond wire configuration (a–b) after chemical decapsulation: evident burn marks on active area due to metal melting; (c–d) after delayering process: evident signs of cracks across active area.

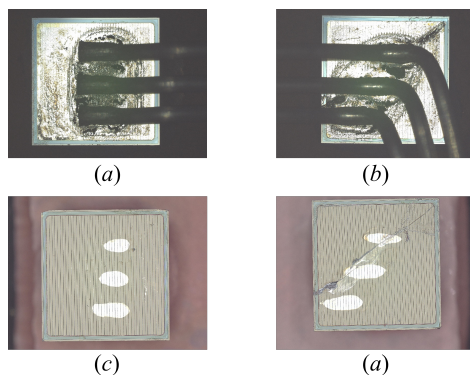


Figure 5.33. Left and right die of the stitch configuration (a–b) after chemical decapsulation: evident burn marks on active area due to metal melting; (c–d) after delayering process, no crack signs are present on the left die while evident crack marks are visible on the right die.

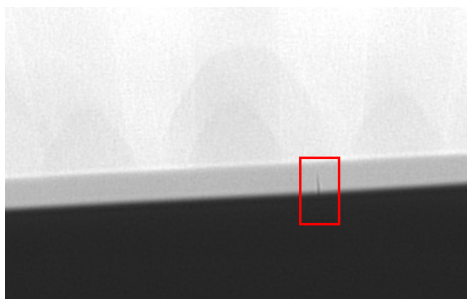


Figure 5.34. Side-view X-ray of the right die (stitch configuration); fracture within the SiC substrate

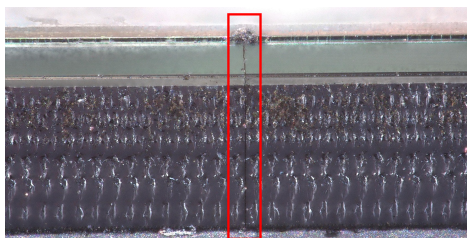


Figure 5.35. Side view of the right die (stitch configuration) showing an edge fracture on SiC substrate

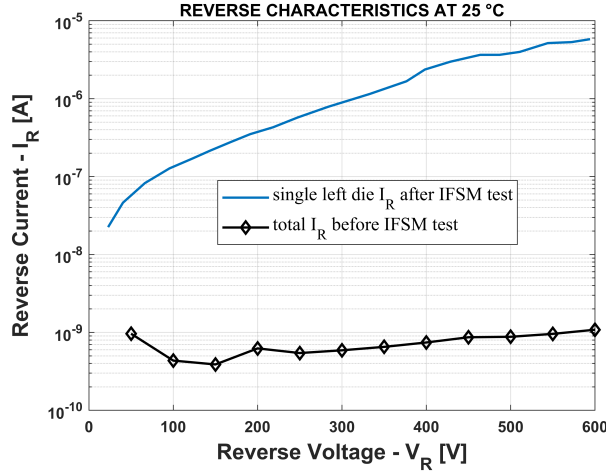


Figure 5.36. Experimental Reverse I_R - V_R characteristics: left die (blue solid line) measured after the IFSM test, and full stitch device (black solid line with markers) measured before the IFSM test; the applied voltage was limited to prevent damage.

Summary In this section we compared three types of 60 A–1200 V SiC diodes with different bond wire configurations. An extensive experimental characterization has been conducted, including measurements of pulsed (isothermal) I_F - V_F characteristics, thermal resistance, and surge current performance. Only minor discrepancies were observed in the I_F - V_F characteristics, where they only take place under high-current conditions, and in thermal resistances. However, the I_{FSM} performance varied significantly. The 4×12 mil and 4×15 mil configurations exhibited lower robustness, whereas the stitch configuration (3×20 mil) shows an I_{FSM} near the theoretical limit, almost double that of a single 30 A device, maximizing diode performance with minimal derating. The failure analysis further highlighted distinct failure mechanisms between the stitch and the other two configurations. These findings provide valuable guidance for designing high-current SiC JBS diodes, especially in applications requiring multiple dice per package due to wafer yield or production constraints.

Chapter 6

Power MOSFETs

6.1 Planar Power MOSFETs

The planar power MOSFET was the first commercially successful unipolar switch developed using silicon technology, once the issues related to the metal-oxide-semiconductor interface had been resolved for CMOS technology [1]. To reduce cost, the channel in these devices was created using the double-diffusion (DMOS) process. In the DMOS process, the P-base and N^+ source regions are formed by ion implantation, masked by a common edge defined by a refractory polysilicon gate electrode. A drive-in cycle after each implantation step moves the P-N junction laterally under the gate electrode. The separation between the N^+ /P-base junction and the P-base/N-drift junction under the gate defines the channel, allowing channel lengths to be reduced to sub-micron dimensions without requiring high-resolution lithography. This approach served the industry well from the 1970s into the 1990s, with planar power MOSFETs remaining available for power electronic applications.

In the 1990s, trench technology, originally developed for DRAMs, was adopted to introduce the UMOSFET structure for commercial applications. This was particularly important for reducing the channel and JFET components in planar MOSFETs designed for lower voltage applications (<30 V).

For silicon power MOSFETs, the on-resistance becomes dominated by the drift region resistance when the breakdown voltage exceeds 200 V. At

high breakdown voltages, the specific on-resistance exceeds $10^{-2} \Omega \cdot \text{cm}^2$, resulting in an on-state voltage drop greater than 1 V at a typical current density of 100 A/cm^2 . Consequently, the Insulated Gate Bipolar Transistor (IGBT) was developed in the 1980s to serve medium- and high-power systems. The superior performance of IGBTs in high-voltage applications relegated silicon MOSFETs to operating voltages below 100 V. Novel silicon structures utilizing the charge-coupling concept have extended the breakdown voltage of power MOSFETs to the 600 V range. However, their specific on-resistance remains relatively high, limiting their use to high-frequency applications where switching losses dominate.

In principle, the much lower drift region resistance in silicon carbide should enable power MOSFETs with very high breakdown voltages, offering both fast switching speed and superior safe operating area compared to high-voltage silicon IGBTs. This reduces both switching and conduction losses in power circuits. Unfortunately, silicon MOSFET structures cannot be directly applied to high-performance silicon carbide devices. First, limited dopant diffusion in silicon carbide prevents the use of the silicon DMOS process. Second, high electric fields in the gate oxide of silicon carbide MOSFETs can exceed its rupture strength, causing catastrophic failure in blocking mode at high voltages. Third, the smaller conduction band offset between silicon carbide and silicon dioxide can lead to hot carrier injection into the oxide, reducing stability. Additionally, the oxide-semiconductor interface quality in silicon carbide must be improved to ensure good threshold voltage control and channel mobility.

This chapter begins with a review of the basic principles of planar MOSFET operation. A planar MOSFET structure formed by staggered ion implantation of the P-base and N^+ source regions is then described. Next, the exacerbation of reach-through breakdown in silicon carbide is analyzed. Differences in threshold voltage between silicon and silicon carbide devices are discussed, and the limitations imposed by high doping concentrations and long channel lengths on achieving low specific on-resistance are highlighted.

6.1.1 Planar Power MOSFET Structure

The basic structure of the planar power MOSFET is illustrated in Fig. 6.1, showing the location of the ion implantation edges. Considering the low diffusion coefficients of dopants in silicon carbide, it was proposed that the P-base and N^+ source ion implantations be staggered using photoresist masks, rather than being defined by the gate edge. Additionally, it was suggested that the P-base region be first amorphized to achieve a more uniform dopant distribution, thereby suppressing reach-through. This approach, employing staggered P-base and N^+ source implants, was subsequently adopted by several research groups to fabricate high-voltage devices [1]. Such devices are commonly referred to as DIMOSFETs, owing to the Double-Implant process used in their fabrication.

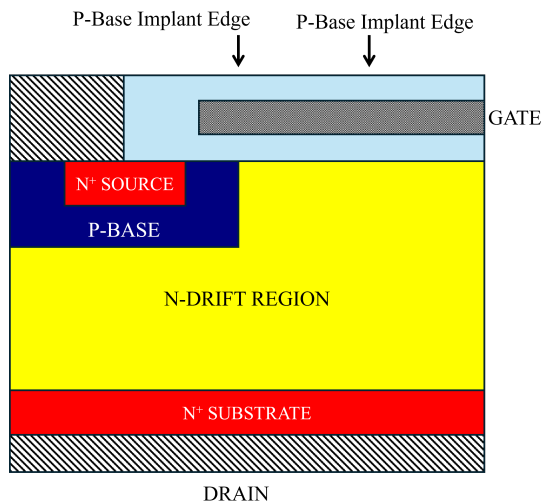


Figure 6.1. The Planar Power MOSFET Structure.

6.1.2 Blocking Characteristics

In the forward-blocking mode of the planar power MOSFET, the applied voltage is supported by a depletion region extending on both sides of the P-base/ N -drift junction.. The maximum blocking voltage is reached when the electric field at this junction equals the critical electric field for

avalanche breakdown, provided that the parasitic $N^+/P/N$ bipolar transistor is completely suppressed [2]. This suppression is achieved by short-circuiting the N^+ source and P-base regions using the source metal.

However, a large leakage current can occur if the depletion region in the P-base reaches the N^+ source region, a phenomenon known as *reach-through*. To prevent reach-through from limiting the breakdown voltage, the doping concentration N_A and thickness W_P of the P-base region must be carefully designed.

Assuming uniform doping on both sides of the P-base/N-drift junction, the applied drain voltage is supported by the P-base and N-drift regions with a triangular electric field distribution, as shown in Fig. 6.2. The maximum electric field occurs at the P-base/N-drift junction, and the depletion width in the P-base region W_P is related to the maximum electric field E_m by:

$$W_P = \frac{\varepsilon_S E_m}{q N_A} \quad (6.1)$$

where ε_S is the permittivity of silicon carbide and N_A is the doping concentration of the P-base region.

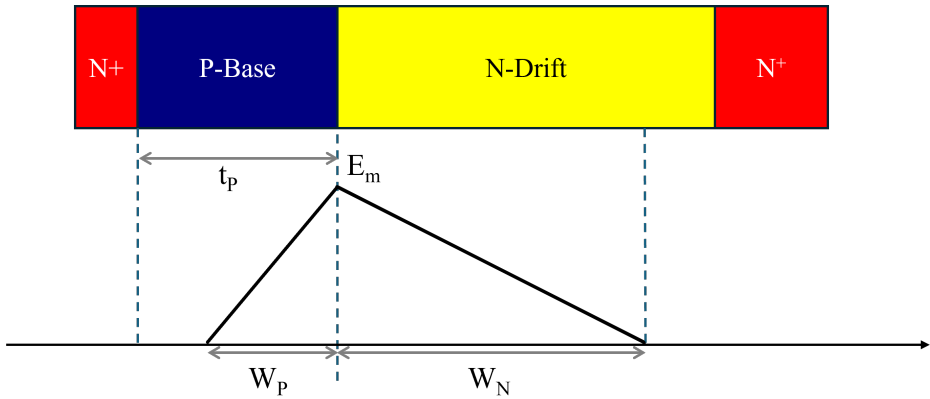


Figure 6.2. Reach-Through in a Power MOSFET Structure.

The minimum P-base thickness required to avoid reach-through can be obtained by assuming that the maximum electric field reaches the critical electric field E_c at full depletion:

$$t_P = \frac{\epsilon_S E_c}{q N_A} \quad (6.2)$$

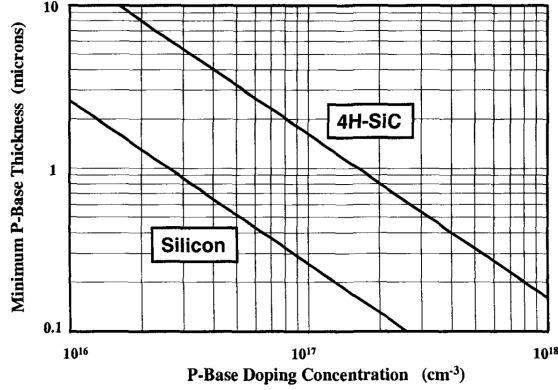


Figure 6.3. Comparison of Minimum P-Base Thickness to prevent Reach-Through Breakdown in 4H-SiC and Silicon.

The calculated minimum P-base thickness for 4H-SiC power MOSFETs is compared with that for silicon in Fig. 6.3. For any given P-base doping concentration, the required thickness for 4H-SiC is about six times larger than that for silicon. Consequently, the minimum channel length in SiC MOSFETs is much larger than in their silicon counterparts, which significantly increases the on-resistance R_{ON} . This problem is further exacerbated by the lower channel inversion-layer mobility observed in SiC.

The minimum P-base thickness required to prevent reach-through decreases with increasing doping concentration, as shown in Fig. 6.3. For silicon power MOSFETs, a typical P-base doping concentration of $N_A = 1 \times 10^{17} \text{ cm}^{-3}$ yields a threshold voltage between 1 V and 2 V for a gate oxide thickness of 500–1000 Å. At this doping level, the P-base thickness can be reduced to approximately 0.5 μm without reach-through limiting the breakdown voltage. In contrast, for 4H-SiC, the doping concentration must exceed $N_A > 4 \times 10^{17} \text{ cm}^{-3}$ to prevent reach-through for the same P-base thickness, which results in a higher threshold voltage (discussed in the next section).

The maximum blocking voltage capability of the power MOSFET struc-

ture is ultimately determined by the N-drift region doping and thickness, as discussed in Section 1. However, under forward-blocking conditions, a significant electric field also develops in the gate oxide. Using Gauss's law, the electric field in the oxide E_{ox} is related to the electric field in the underlying semiconductor E_{semi} by:

$$E_{\text{ox}} = \frac{\varepsilon_{\text{semi}}}{\varepsilon_{\text{ox}}} E_{\text{semi}} \quad (6.3)$$

where $\varepsilon_{\text{semi}}$ and ε_{ox} are the dielectric constants of the semiconductor and the oxide, respectively.

For silicon devices, the maximum electric field in the drift region remains below 3×10^5 V/cm, so the corresponding oxide field E_{ox} does not exceed its reliability limit of about 3×10^6 V/cm. In contrast, for 4H-SiC, when the semiconductor field approaches its critical breakdown field, the oxide field can reach values around 9×10^6 V/cm, which exceeds the reliability limit and can lead to catastrophic oxide rupture.

Therefore, it is crucial to monitor and limit the electric field in the gate oxide during the design of SiC MOSFETs. Novel device structures that shield the gate oxide from excessive electric field have been proposed and experimentally demonstrated to mitigate this problem.

6.1.3 Forward Conduction

Current flow between the drain and source can be induced by creating an inversion layer channel on the surface of the P-base region. The current path is illustrated in Fig. 6.4 by the dotted area. The current flows through the inversion layer channel formed due to the applied gate bias into the JFET region via the accumulation layer formed above it under the gate oxide. It then spreads into the N-drift region at a 45° angle and becomes uniform through the rest of the structure.

The total on-resistance for the planar power MOSFET structure is determined by the resistance of these components in the current path:

$$R_{\text{on,sp}} = R_{\text{CH}} + R_{\text{A}} + R_{\text{JFET}} + R_{\text{D}} + R_{\text{subs}} \quad (6.4)$$

where R_{CH} is the channel resistance, R_{A} is the accumulation region resistance, R_{JFET} is the resistance of the JFET region, R_{D} is the resistance

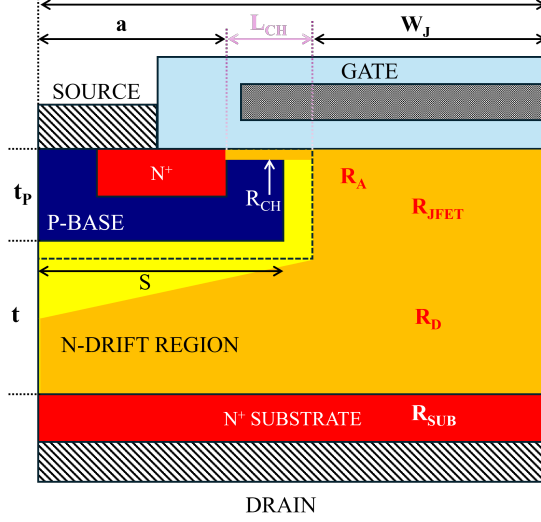


Figure 6.4. Current Flow Path in the Planar 4H-SiC Power MOSFET

of the drift region after taking into account current spreading from the JFET region, and R_{subs} is the resistance of the N^+ substrate. These resistances can be analytically modeled by using the current flow pattern indicated by the shaded regions in Fig. 6.4 (practically the same approach as in the JBS structures chapter).

The specific channel resistance is given by:

$$R_{\text{CH}} = \frac{pL_{\text{CH}}}{\mu_{\text{inv}}C_{\text{ox}}(V_{\text{G}} - V_{\text{T}})} \quad (6.5)$$

where L_{CH} is the channel length as shown in Fig. 6.4, μ_{inv} is the inversion layer electron mobility, C_{ox} is the specific capacitance of the gate oxide, V_{G} is the applied gate bias, and V_{T} is the threshold voltage. The specific capacitance can be obtained using:

$$C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \quad (6.6)$$

where ε_{ox} is the dielectric constant of the gate oxide and t_{ox} is its thickness.

The specific resistance of the accumulation region is given by:

$$R_A = K \frac{p(W_J - W_P)}{\mu_a C_{ox}(V_G - V_T)} \quad (6.7)$$

where μ_a is the electron mobility in the accumulation layer and K accounts for two-dimensional current spreading from the channel into the JFET region (typical value $K \approx 0.6$ for silicon devices). W_P is the zero-bias depletion width at the P-base/N-drift junction, determined by:

$$W_P = \sqrt{\frac{2\epsilon_S V_{biP}}{qN_D}} \quad (6.8)$$

where V_{biP} is the built-in potential of the P-N junction, typically 3.3 V for 4H-SiC.

The specific JFET region resistance is:

$$R_{JFET} = \rho_D t_P \frac{p}{W_J - W_P} \quad (6.9)$$

where t_P is the depth of the P-base region.

The drift region spreading resistance is obtained as:

$$R_D = \rho_D p \ln \left(\frac{p}{W_J - W_P} \right) + \rho_D (t - s - W_P) \quad (6.10)$$

where t is the thickness of the drift region below the P-base region and s is the width of the P-base region.

The resistance contribution from the N^+ substrate is:

$$R_{subs} = \rho_{subs} t_{subs} \quad (6.11)$$

where ρ_{subs} and t_{subs} are the resistivity and thickness of the substrate, respectively. A typical value for this contribution is $4 \times 10^{-4} \Omega \cdot \text{cm}^2$.

The specific on-resistances of 4H-SiC planar MOSFETs with a drift region doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$ and thickness of $20 \mu\text{m}$ were modeled using the above analytical expressions. A gate oxide thickness of $0.1 \mu\text{m}$ and a cell dimension $a = 1 \mu\text{m}$ (achievable with $0.5 \mu\text{m}$ design rules) were used. The accumulation mobility was assumed to be twice the inversion layer mobility, and a K -factor of 0.1 was used for correlation with simulations. The P-base depth was $1 \mu\text{m}$, and the effective gate drive

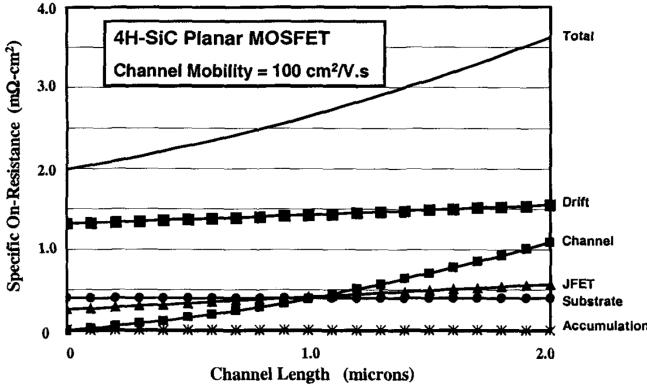


Figure 6.5. On-Resistance Components for a 4H-SiC Planar MOSFET.

$(V_G - V_T)$ was 20 V.

The results (Fig. 6.5) show that the drift region resistance dominates even at channel lengths of 2 μm . At $L_{\text{CH}} = 1 \mu\text{m}$, the total specific on-resistance is $2.7 \text{ m}\Omega \cdot \text{cm}^2$, about three times the ideal value. However, the breakdown voltage of the structure was found to be well below the ideal parallel-plane value (3000 V), due to reach-through effects.

The JFET width must be optimized to minimize $R_{\text{on,sp}}$ and to control the electric field at the gate oxide interface. Fig. 6.6 shows that $R_{\text{on,sp}}$ rises sharply when $W_J < 0.7 \mu\text{m}$, due to severe current constriction. A minimum $R_{\text{on,sp}}$ occurs around $W_J = 1 \mu\text{m}$.

When the inversion layer mobility is $25 \text{ cm}^2/\text{Vs}$, the channel resistance becomes comparable to the drift resistance, doubling $R_{\text{on,sp}}$ to $\approx 4 \text{ m}\Omega \cdot \text{cm}^2$ at $L_{\text{CH}} = 1 \mu\text{m}$. At $2.5 \text{ cm}^2/\text{Vs}$, the channel resistance dominates, raising $R_{\text{on,sp}}$ to $18 \text{ m}\Omega \cdot \text{cm}^2$.

Finally, Fig. 6.9 shows that $R_{\text{on,sp}}$ approaches the ideal limit for breakdown voltages above 5 kV when $\mu_{\text{inv}} = 100 \text{ cm}^2/\text{Vs}$. However, for breakdown voltages below 1 kV, channel resistance dominates and significantly reduces the expected advantage of 4H-SiC over silicon. This highlights the need for process technologies that achieve high inversion layer mobility in 4H-SiC MOSFETs.

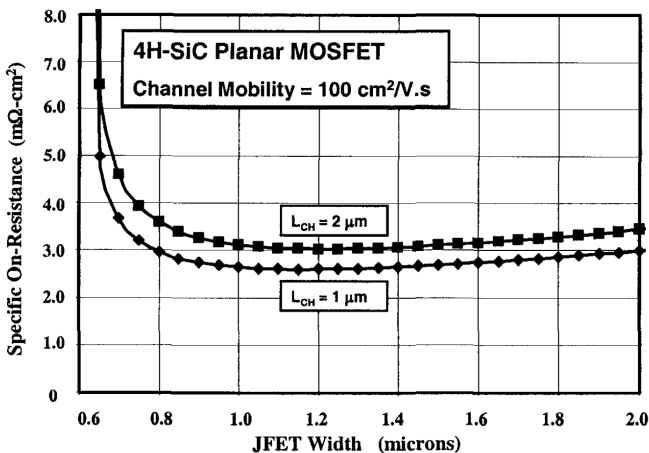


Figure 6.6. Impact of JFET Width on the On-Resistance for a 4H-SiC Planar MOSFET.

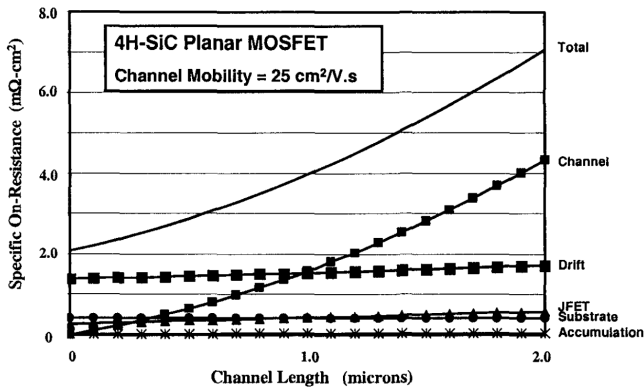


Figure 6.7. Impact of JFET Width on the On-Resistance for a 4H-SiC Planar MOSFET.

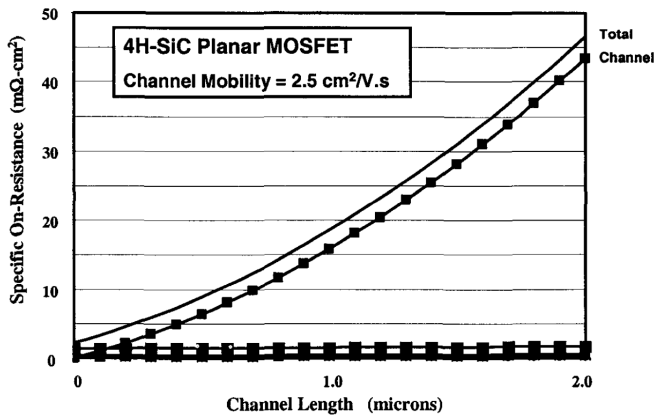


Figure 6.8. On-Resistance Components for a 4H-SiC Planar MOSFET.

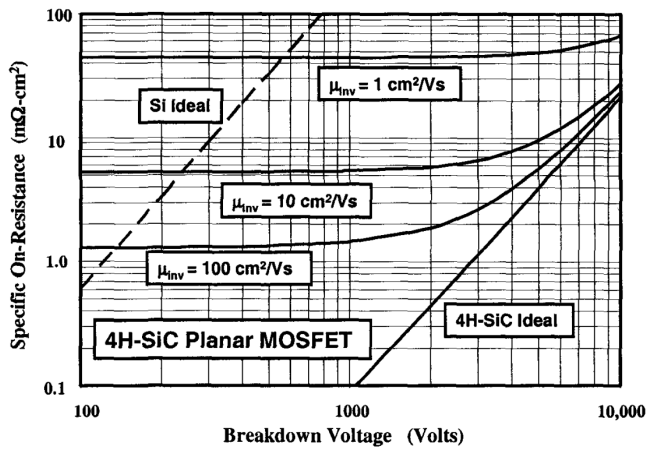


Figure 6.9. Threshold voltage of 4H-SiC planar MOSFETs. Dashed lines include the impact of n^+ polysilicon gate and an oxide fixed charge of $2 \times 10^{11} \text{ cm}^{-2}$.

6.1.4 Threshold Voltage

The threshold voltage (V_T) of the power MOSFET is a critical design parameter from an application standpoint. A minimum threshold voltage above 1 V is typically required to ensure immunity against unintended turn-on events caused by voltage spikes or electrical noise. Conversely, an excessively high threshold voltage is undesirable because the voltage available for forming the inversion channel charge is determined by the difference ($V_G - V_T$), where V_G is the applied gate bias voltage and V_T is the threshold voltage. In most high-voltage power electronic systems—especially those employing silicon carbide (SiC) devices—the gate drive voltage rarely exceeds 10 V. Based on this constraint, the threshold voltage should ideally be kept below 3 V in order to minimize the contribution of the channel resistance to the overall on-state resistance [1].

The threshold voltage can be modeled as the gate bias at which the onset of strong inversion occurs in the channel. It can be expressed as:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{4\epsilon_s q N_A \phi_F}}{C_{ox}} \quad (6.12)$$

where V_{FB} is the flat-band voltage, $\phi_F = \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right)$ is the Fermi potential, ϵ_s is the semiconductor permittivity, q is the electronic charge, N_A is the P-base doping concentration, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the oxide capacitance per unit area, k is Boltzmann's constant, and T is the absolute temperature. The presence of positive fixed oxide charges introduces a negative shift in the threshold voltage given by:

$$\Delta V_T = -\frac{Q_{ox}}{C_{ox}} \quad (6.13)$$

An additional negative shift, typically up to 1 V, can be obtained by using a heavily doped n^+ polysilicon gate electrode, as is commonly adopted in silicon power MOSFETs.

The analytically calculated threshold voltage for 4H-SiC planar MOSFETs is shown in Fig. 6.10 for a gate oxide thickness of 0.1 μm . For comparison, the corresponding result for a silicon power MOSFET with the same oxide thickness is also shown. In silicon devices, a threshold voltage of about 3 V is achieved with a P-base doping concentration of

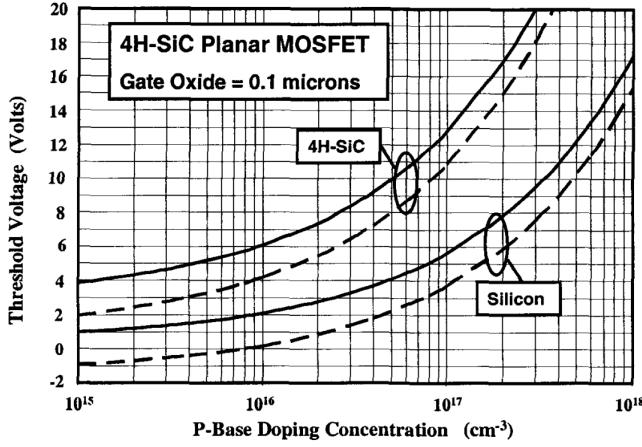


Figure 6.10. Threshold voltage of 4H-SiC planar MOSFETs. Dashed lines include the impact of n^+ polysilicon gate and an oxide fixed charge of $2 \times 10^{11} \text{ cm}^{-2}$.

$1 \times 10^{17} \text{ cm}^{-3}$. At this doping level, the depletion width in the P-base region is less than $0.5 \mu\text{m}$, as illustrated in Fig. 6.3, even when the electric field in the semiconductor approaches the critical breakdown field. This allows silicon power MOSFETs to be designed with channel lengths shorter than $0.5 \mu\text{m}$ without encountering reach-through breakdown limitations. In contrast, for 4H-SiC devices, a P-base doping concentration of about $3 \times 10^{17} \text{ cm}^{-3}$ is required to maintain a depletion width below $1 \mu\text{m}$ when the electric field approaches the critical breakdown level. At this doping concentration, the threshold voltage for a 4H-SiC MOSFET approaches 20 V. This substantially higher threshold voltage originates from the wider bandgap of SiC and the higher P-base doping concentration required to suppress reach-through breakdown. Such a condition represents a fundamental challenge in achieving acceptable threshold voltages in silicon carbide power MOSFETs when using conventional silicon-based structures. Innovative device architectures capable of electrostatically shielding the P-base region can be employed to overcome this limitation.

The threshold voltage can also be reduced by decreasing the gate oxide thickness (t_{ox}). For example, when t_{ox} is reduced to $0.05 \mu\text{m}$, the threshold voltage of a silicon power MOSFET decreases to just below 2 V, as

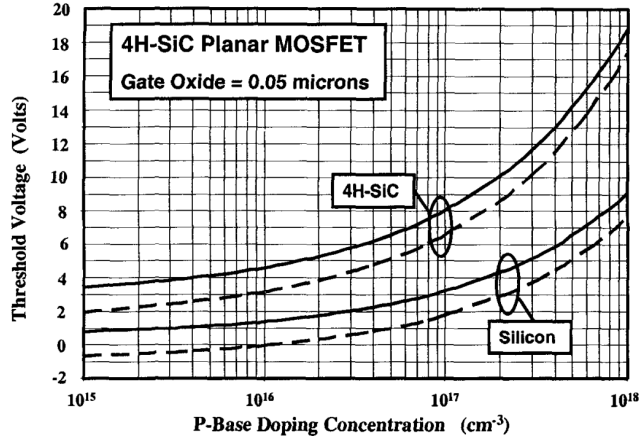


Figure 6.11. Threshold voltage of 4H-SiC planar MOSFETs. Dashed lines include the impact of n^+ polysilicon gate and an oxide fixed charge of $2 \times 10^{11} \text{ cm}^{-2}$.

shown in Fig. 6.11. This design approach is common for low-voltage silicon MOSFETs that operate with logic-level (5 V) gate drives. For a 4H-SiC MOSFET with the same oxide thickness, the threshold voltage decreases to about 10 V, which is still relatively high for most practical applications. Further reduction of the gate oxide thickness to $0.025 \text{ }\mu\text{m}$ leads to a threshold voltage below 1 V for silicon MOSFETs, provided that the P-base doping concentration is increased to $2 \times 10^{17} \text{ cm}^{-3}$. Under the same conditions, the threshold voltage for 4H-SiC MOSFETs drops to approximately 6 V, which is only marginally acceptable for high-voltage operation. However, operating very high-voltage power MOSFETs with such thin gate oxides introduces significant challenges in terms of manufacturability and long-term reliability due to the high electric fields occurring beneath the gate oxide in the semiconductor.

The threshold voltage of power MOSFETs decreases with increasing temperature. This dependence is illustrated in Fig. 6.13 for both 4H-SiC and silicon MOSFETs with a gate oxide thickness of $0.025 \text{ }\mu\text{m}$. The variation of V_T with temperature is relatively modest, indicating that the temperature-induced shift in threshold voltage is not a critical consideration in the design of 4H-SiC power MOSFETs.

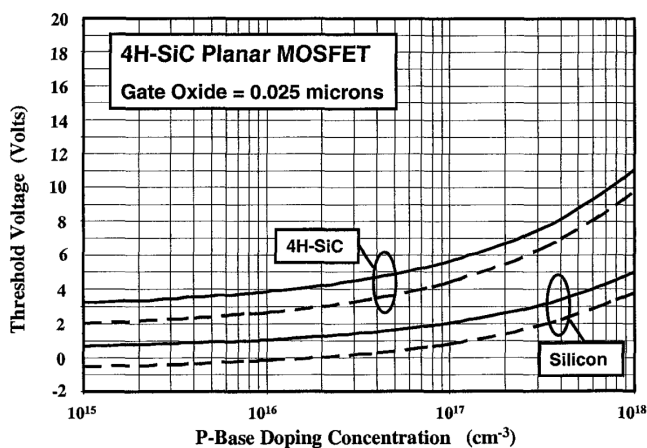


Figure 6.12. Threshold voltage of 4H-SiC planar MOSFETs. Dashed lines include the impact of n^+ polysilicon gate and an oxide fixed charge of $2 \times 10^{11} \text{ cm}^{-2}$.

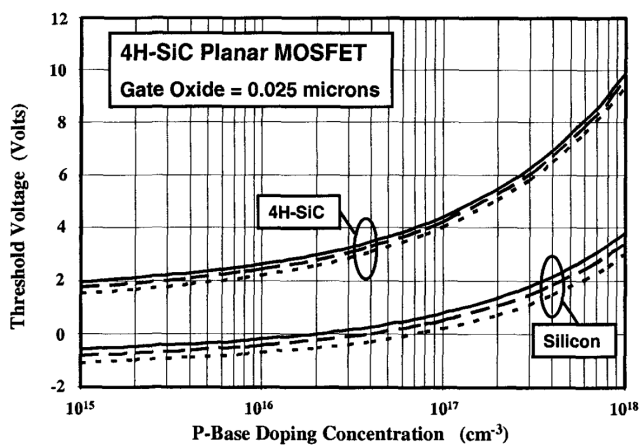


Figure 6.13. Threshold voltage of 4H-SiC planar MOSFETs. (Solid line: 300 K; dashed line: 400 K; dotted line: 500 K).

6.1.5 Hot Eletron Injection

In any MOSFET structure, electron injection into the gate oxide can occur when the carriers acquire sufficient energy in the semiconductor to overcome the potential barrier at the semiconductor–oxide interface [1]. The energy band offsets between the semiconductor and silicon dioxide are shown in Fig. 6.14 for both silicon and 4H–SiC for comparison purposes. Due to the wider bandgap of 4H–SiC, the conduction band offset between the semiconductor and the silicon dioxide is significantly smaller than that of silicon, as illustrated below.

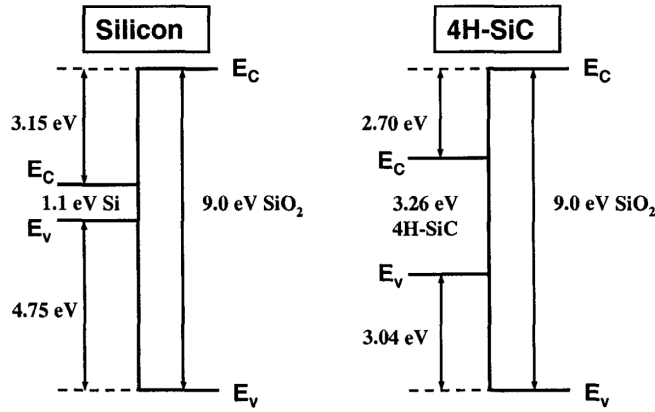


Figure 6.14. Energy Band Offsets between Oxide and Semiconductors.

The energy band diagram for the 4H–SiC/silicon dioxide interface under a positive gate bias is illustrated in Fig. 6.15. This bias condition corresponds to the typical on-state operation mode of power MOSFETs. In this configuration, the gate electrode is assumed to be composed of polysilicon. As can be observed, a relatively narrow potential barrier is formed at the semiconductor–oxide interface, which can be penetrated by electron tunneling from the conduction band into the oxide layer. This process gives rise to a Fowler–Nordheim tunneling current, resulting in the injection of electrons into the oxide.

This tunneling phenomenon has been experimentally observed in both 6H–SiC and 4H–SiC MOS capacitors. The electrons trapped within the gate oxide can subsequently cause a shift in the threshold voltage of the

MOSFET, leading to long-term reliability concerns in device operation.

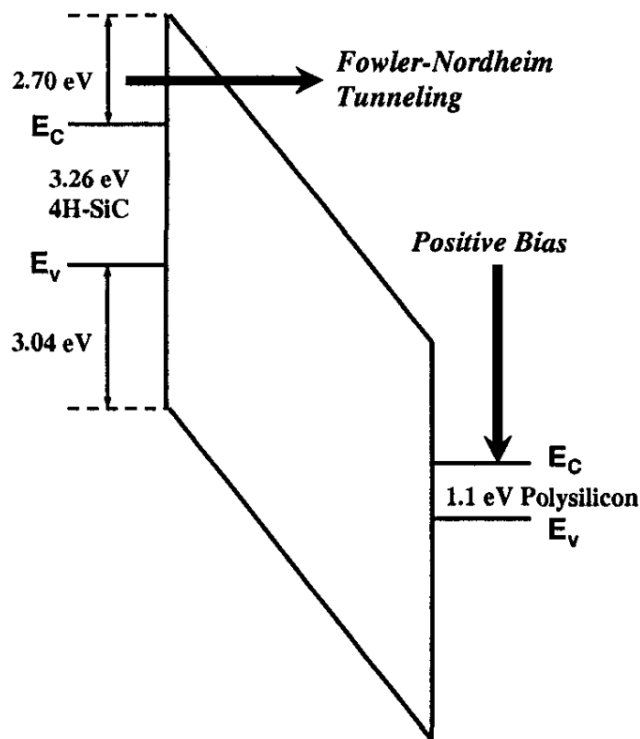


Figure 6.15. Energy Band Diagram for the Polysilicon/Oxide/4H-SiC Structure.

6.1.6 On state and Output Characteristics

The on-state voltage drop of the planar 4H-SiC power MOSFET structure is determined primarily by its specific on-resistance. This parameter was extracted through numerical simulations performed at a gate bias of 20 V [1]. A relatively high gate bias was required due to the large threshold voltage of these devices, as previously discussed in earlier sections of this chapter. As expected, the specific on-resistance strongly depends on both the width of the JFET region and the mobility of the channel inversion layer.

A representative transfer characteristic is shown in Fig. 6.16 for a device featuring a JFET width of 1 μm . From these transfer characteristics, it can be observed that the threshold voltage, which directly influences the on-resistance, is approximately 10 V. This value closely matches the analytical prediction derived in the previous section for a P-base doping concentration of $9 \times 10^{16} \text{ cm}^{-3}$ and a gate oxide thickness of 0.1 μm . The figure also illustrates the influence of the channel inversion layer mobility: as expected, a reduction in mobility leads to a corresponding decrease in the drain current.

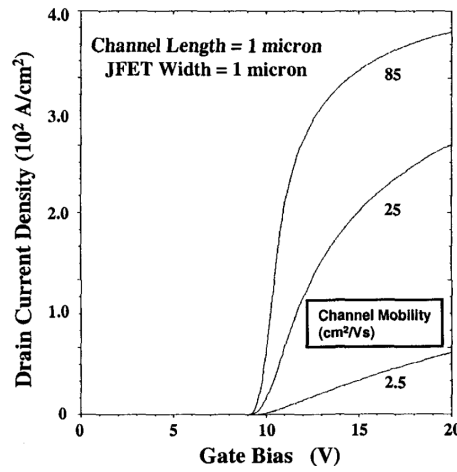


Figure 6.16. Transfer Characteristics of the 4H-SiC Planar MOSFETs.

The specific on-resistances obtained from the on-state simulations are compared in Fig. 6.17 with the analytically calculated values derived from the model developed earlier. Three different JFET region widths were considered in this comparison, highlighting the influence of geometric scaling on device performance.

The output characteristics of a power MOSFET define the operational region within which the device can function safely during switching transients. The current-voltage trajectories during transient operation must remain within the boundaries established by these output characteristics. For a power MOSFET, one boundary is determined by the on-resistance, while another is defined by the breakdown voltage. These two limits es-

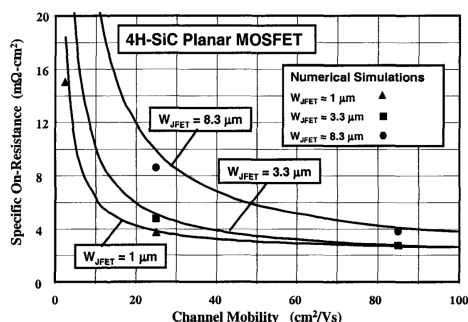


Figure 6.17. Specific On-Resistance for the 4H-SiC Planar MOSFETs.

establish the maximum on-state current that can be sustained—after accounting for the thermal impedance of the package—as well as the maximum off-state voltage that can be applied without incurring excessive leakage-induced power dissipation. A third boundary is imposed by the gate-controlled current saturation, where the magnitude of the output resistance becomes critical. A higher output resistance is desirable, as it provides improved control of the drain current through modulation of the gate bias voltage.

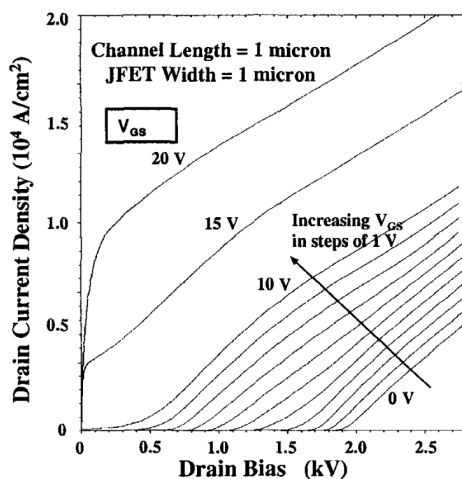


Figure 6.18. Output Characteristics of a 4H-SiC Planar MOSFET.

The output characteristics of the planar 4H-SiC power MOSFET were analyzed by biasing the gate at various voltage levels while sweeping the drain voltage up to 2800 V. The results for the device with a JFET width of 1 μm are presented in Fig. 6.18. It can be observed that a significant current flow begins when the drain voltage exceeds approximately 1900 V, even under zero gate bias conditions. This current conduction is attributed to the reach-through breakdown phenomenon discussed in previous sections. The presence of this reach-through current degrades the output resistance across all positive gate bias levels. Furthermore, as illustrated in Fig. 6.19, an additional degradation of output resistance and a reduction in maximum blocking voltage occur when the JFET width is increased. Consequently, the overall output characteristics of the planar 4H-SiC MOSFET structure are inferior to those obtained for the Baliga-Pair configuration described in the previous chapter.

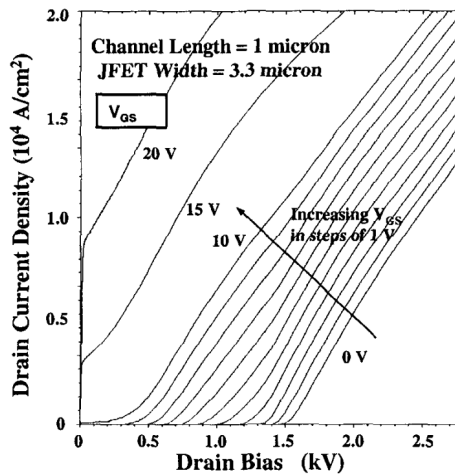


Figure 6.19. Output Characteristics of a 4H-SiC Planar MOSFET.

6.2 Trench-Gate Power MOSFETs

The silicon trench-gate power MOSFET, introduced in the 1990s, evolved from trench technology originally developed for DRAMs. Prior to its adoption, the reduction of specific on-resistance in silicon power MOSFETs was limited by low channel density and the resistance of the JFET region. Although progressive lithographic scaling in the 1970s and 1980s had improved the DMOSFET structure, these advancements eventually reached saturation [1].

The introduction of the trench-gate (UMOSFET) architecture enabled a substantial increase in channel density and eliminated the JFET resistance contribution, leading to major performance improvements in low-voltage (< 50 V) MOSFETs. Early prototypes, fabricated in the mid-1980s, demonstrated much lower specific on-resistance compared to conventional DMOSFETs [1]. However, issues such as trench surface quality and oxide reliability had to be resolved before commercialization. By the 1990s, the trench-gate MOSFET became the dominant technology for portable electronic applications such as laptops and PDAs.

In silicon DMOSFETs, the channel and JFET resistances dominate when the breakdown voltage falls below 50 V, as the drift region contribution becomes negligible. In contrast, due to the much lower specific drift resistance of silicon carbide, these same resistive components become dominant even at breakdown voltages approaching 5000 V, particularly when channel mobility is limited. This observation motivated the development of trench-gate architectures for SiC devices. Furthermore, the P-base region in trench-gate SiC MOSFETs can be formed by epitaxial growth, which was more technologically mature than ion implantation for producing P-type layers in SiC.

The trench-gate MOSFET structure offers significantly lower specific on-resistance than the DMOSFET; however, in SiC implementations, the gate oxide is directly exposed to the high electric field in the drift region during blocking mode. This represents a key reliability concern. To mitigate this issue, modified structures employing shielding regions have been proposed to reduce the electric field at the gate oxide interface, enabling the realization of robust SiC MOSFETs. In this chapter, the results of the two-dimensional numerical analysis of the basic trench-gate silicon

carbide MOSFET structure are presented. Finally, the on-state, reverse, and short-circuit performances of a 3.3 kV quasi-planar trench MOSFET are compared with those of a conventional planar device using advanced three-dimensional TCAD simulations.

6.2.1 Trench-Gate Power MOSFET structure

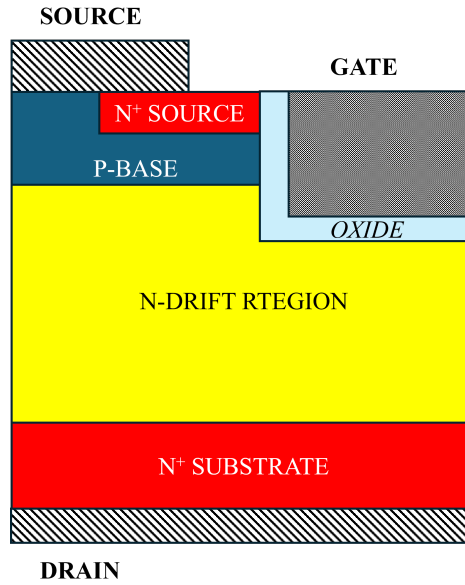


Figure 6.20. The Trench-Gate Power MOSFET Structure.

The basic structure of the trench-gate power MOSFET is shown in Fig. 6.20. This device can be fabricated either by epitaxial growth of the P-base region over the drift region, or by introducing P-type dopants through ion implantation. The first 4H-SiC UMOSFET structures were realized using epitaxial growth for the P-base region, mainly due to the difficulties in activating P-type dopants implanted in silicon carbide [1].

However, this fabrication method requires either the removal of the P-type layer at the device edges to form a mesa edge termination, or the implementation of multiple trench-isolated guard rings. The trench-gate structure itself is typically fabricated by reactive ion etching to create U-

shaped trenches. Subsequently, the gate oxide is thermally grown and the trench is refilled with polysilicon, following a process similar to that used for silicon-based UMOSFETs.

It should be noted that the P-base region is short-circuited to the N^+ source region through the source metallization. While this configuration is routinely achieved in silicon devices using a common ohmic contact for both the N^+ and P-type regions, it has proven challenging in silicon carbide. Different metals are generally required to form reliable ohmic contacts in SiC, with titanium commonly used for N-type regions and aluminum for P-type regions. In such cases, it may be preferable to short-circuit the source-base junction in a direction orthogonal to the cross-section shown in the figure. This configuration is also beneficial for reducing the cell pitch, thereby increasing the overall channel density.

6.2.2 Blocking Characteristics

When the trench-gate power MOSFET operates in the forward blocking mode, the applied voltage is sustained by the depletion region formed on both sides of the P-base/N-drift junction. The maximum blocking voltage is reached when the electric field at this junction becomes equal to the critical electric field for avalanche breakdown, provided that the parasitic N^+ /P/N bipolar transistor is completely suppressed. This suppression is achieved by short-circuiting the N^+ source and P-base regions through the source metallization, as illustrated in the upper left portion of the cross-section.

However, significant leakage current can occur if the depletion region in the P-base extends and reaches the N^+ source region, a phenomenon known as reach-through. To prevent this from limiting the breakdown voltage, both the doping concentration and the thickness of the P-base must be carefully designed. The physical mechanisms governing the reach-through process are identical to those previously described for the planar MOSFET structure. Consequently, the design guidelines established earlier, with reference to Fig. 6.3, are equally applicable to the trench-gate configuration. This implies that the minimum channel length required for silicon carbide trench-gate devices is considerably larger than that for silicon devices, resulting in a substantial increase in on-resistance. This degradation is further exacerbated by the lower channel inversion layer mobility char-

acteristic of silicon carbide.

The minimum P-base thickness required to avoid reach-through breakdown decreases with increasing doping concentration, as shown in Fig. 6.3. For 4H-SiC, the P-base doping concentration must exceed $2 \times 10^{17} \text{ cm}^{-3}$ to prevent reach-through when the P-base thickness is $1 \text{ }\mu\text{m}$. Such high doping levels, however, lead to an increased threshold voltage, as discussed in the previous chapter.

The maximum blocking voltage capability of the trench-gate MOSFET structure is determined primarily by the doping concentration and thickness of the drift region. Nevertheless, in the trench-gate configuration, the gate extends into the drift region, thereby exposing the gate oxide to the high electric fields that develop under forward blocking conditions. In 4H-SiC, the electric field in the oxide can reach values as high as $9 \times 10^6 \text{ V/cm}$ when the field in the semiconductor approaches its breakdown strength. This not only exceeds the oxide reliability limit but can also lead to catastrophic failure due to oxide rupture. The situation is further aggravated by electric field enhancement at the trench corners (location A in the figure). To overcome this limitation, innovative device architectures have been proposed and demonstrated that effectively shield the gate oxide from excessive electric fields.

6.2.3 Forward Conduction

Current flow between the drain and source in a trench-gate power MOSFET is established by forming an inversion layer channel along the surface of the P-base region. The current path is illustrated in Fig. 6.21 by the shaded area. Electrons flow from the N^+ source region into the N^- drift region through the inversion layer channel formed on the vertical sidewalls of the trench as a result of the applied gate bias. The current then spreads into the drift region from the bottom of the trench at approximately a 45° angle, eventually becoming uniform through the remainder of the structure. The total specific on-resistance ($R_{\text{on,sp}}$) of the trench-gate power MOSFET is determined by the resistive components along this conduction path:

$$R_{\text{on,sp}} = R_{\text{CH}} + R_{\text{D}} + R_{\text{subs}} \quad (6.14)$$

where R_{CH} is the channel resistance, R_D is the drift region resistance (including current spreading effects), and R_{subs} is the resistance of the N^+ substrate. These components can be analytically modeled based on the current flow distribution illustrated in Fig. 6.21.

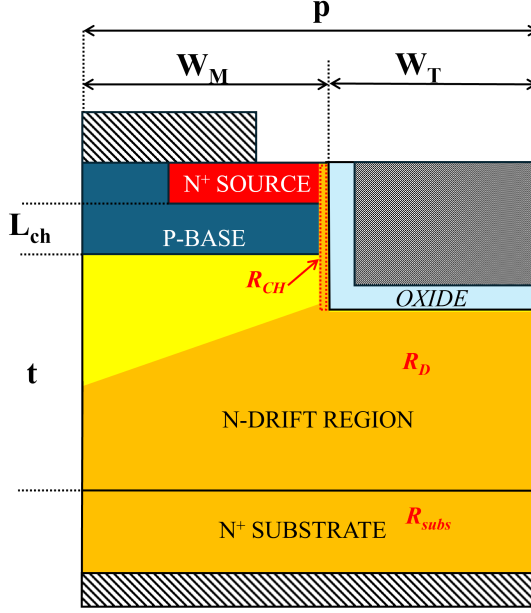


Figure 6.21. Current Flow Path in the Trench-Gate 4H-SiC Power MOSFET.

The specific channel resistance can be expressed as:

$$R_{CH} = \frac{pL_{CH}}{\mu_{inv}C_{ox}(V_G - V_T)} \quad (6.15)$$

where μ_{inv} is the electron mobility in the inversion layer, C_{ox} is the specific capacitance of the gate oxide, V_G is the applied gate bias, and V_T is the threshold voltage. The oxide capacitance per unit area is given by:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (6.16)$$

where ε_{ox} is the dielectric constant of the gate oxide and t_{ox} is its thickness.

The drift region spreading resistance is calculated as:

$$R_D = \rho_D p \ln\left(\frac{p}{W_T}\right) + \rho_D (t - W_M) \quad (6.17)$$

where t is the drift region thickness beneath the P-base region, W_T is the trench width, and W_M is the mesa width (as shown in Fig. 6.21).

The substrate resistance contribution is given by:

$$R_{\text{subs}} = \rho_{\text{subs}} t_{\text{subs}} \quad (6.18)$$

where ρ_{subs} and t_{subs} are the resistivity and thickness of the substrate, respectively. A typical value for this contribution is approximately $4 \times 10^{-4} \Omega\text{-cm}^2$.

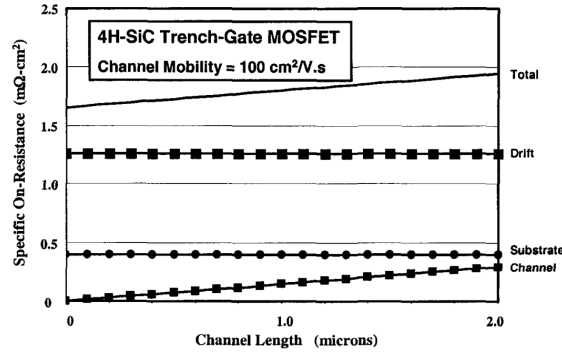


Figure 6.22. On-Resistance Components for a 4H-SiC Trench-Gate MOSFET.

Using these analytical expressions, the specific on-resistance of 4H-SiC trench MOSFETs was modeled for a drift region doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$ and a thickness of $20 \mu\text{m}$, corresponding to a breakdown voltage of about 3000 V. To exploit the scaling advantage of the trench-gate architecture, a gate oxide thickness of $0.05 \mu\text{m}$ was used. The mesa width (W_M) and trench width (W_T) were both set to $0.25 \mu\text{m}$, values achievable using $0.5 \mu\text{m}$ design rules. The effective gate drive voltage ($V_G - V_T$) was taken as 5 V, assuming a gate drive voltage of 10 V and a threshold voltage of 5 V—consistent with the inversion-mode 4H-SiC MOSFET model described in Chapter 9.

The various on-resistance components are illustrated in Fig. 6.22 for a channel mobility of $100 \text{ cm}^2/\text{Vs}$. Experimental studies on planar 4H-SiC MOSFETs have demonstrated even higher inversion layer mobilities, suggesting that such performance could also be achievable in trench-gate devices. As expected, only the channel resistance increases with increasing channel length, since the cell pitch remains constant. The results indicate that the drift region resistance dominates: for a $1 \mu\text{m}$ channel length, a total specific on-resistance of $1.8 \text{ m}\Omega\cdot\text{cm}^2$ is obtained, which is within a factor of two of the ideal drift region resistance.

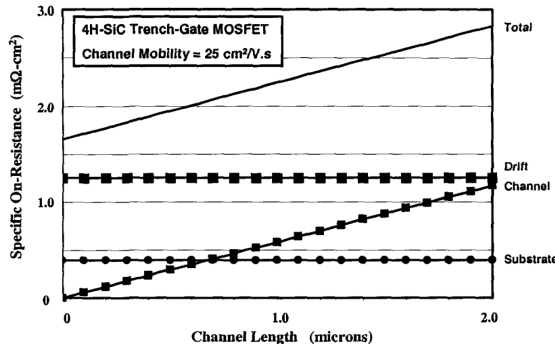


Figure 6.23. On-Resistance Components for a 4H-SiC Trench-Gate MOSFET.

The previous results assume a channel mobility of $100 \text{ cm}^2/\text{Vs}$. However, most research groups report significantly lower inversion layer mobilities in 4H-SiC structures. The influence of reduced mobility on trench-gate MOSFET performance is shown in Figs. 6.23 and 6.24 for mobilities of 25 and $2.5 \text{ cm}^2/\text{Vs}$, respectively. At $\mu_{\text{inv}} = 25 \text{ cm}^2/\text{Vs}$, the channel resistance becomes comparable to that of the drift region, raising the total specific on-resistance to $2.3 \text{ m}\Omega\cdot\text{cm}^2$. When the mobility is further reduced to $\mu_{\text{inv}} = 2.5 \text{ cm}^2/\text{Vs}$, the channel resistance becomes dominant, increasing the specific on-resistance to approximately $7.5 \text{ m}\Omega\cdot\text{cm}^2$ for a $1 \mu\text{m}$ channel length.

These findings indicate that, despite the high channel density of the trench-gate architecture, the channel resistance can still dominate the overall on-resistance if the inversion layer mobility is low. The relative contribution of the channel resistance depends on the drift region resistance,

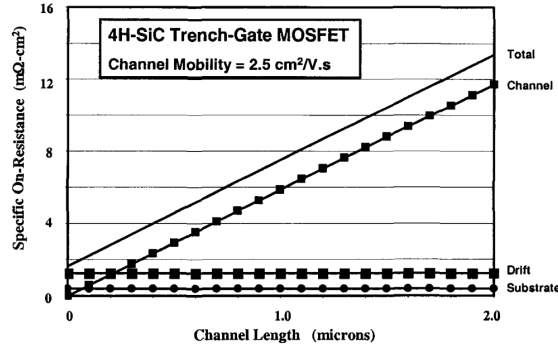


Figure 6.24. On-Resistance Components for a 4H-SiC Trench-Gate MOSFET.

which in turn is a function of the device breakdown voltage. To clarify this relationship, consider a 4H-SiC trench-gate MOSFET with a $0.5\ \mu\text{m}$ cell pitch (based on $0.5\ \mu\text{m}$ design rules), a $1\ \mu\text{m}$ channel length, and a $0.1\ \mu\text{m}$ gate oxide thickness. The drift region parameters are adjusted to achieve different breakdown voltages. For this oxide thickness, the threshold voltage is about 15 V, and the gate drive voltage was set to 20 V in the analysis. The specific on-resistance as a function of breakdown voltage is shown in Fig. 6.25 for $\mu_{\text{inv}} = 25\ \text{cm}^2/\text{V}\cdot\text{s}$.

At low breakdown voltages (below 600 V), the drift region thickness t becomes smaller than the mesa width W_M . Under these conditions, the current does not spread at a 45° angle from the trench bottom but instead flows directly from a width W_T to a cross-sectional width $p = W_M + W_P$. The drift region resistance in such cases can be expressed as:

$$R_D = \rho_D p \ln\left(\frac{p}{W_T}\right) \quad (6.19)$$

From Fig. 6.25, it can be concluded that the specific on-resistance of 4H-SiC trench-gate MOSFETs approaches the ideal drift-region limit for breakdown voltages exceeding 5000 V, even with a channel mobility of $25\ \text{cm}^2/\text{V}\cdot\text{s}$. However, for breakdown voltages below 1000 V, the channel resistance becomes the limiting factor. At 1000 V, the expected improvement in specific on-resistance over silicon power MOSFETs is approxi-

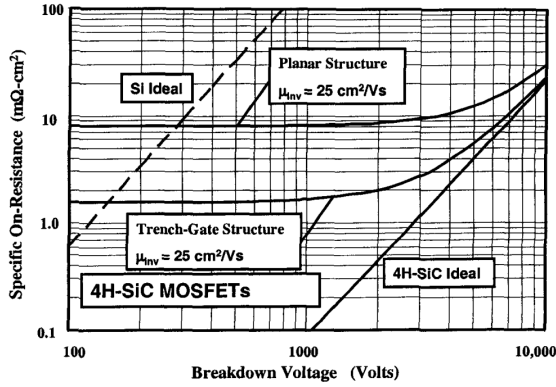


Figure 6.25. Specific On-Resistance for 4H-SiC Trench-gate MOSFETs

mately $100\times$, compared to the $2000\times$ theoretical advantage in drift region performance alone. For comparison, the performance of planar inversion-mode 4H-SiC MOSFETs is also shown in Fig. 6.25, based on identical channel length, oxide thickness, and mobility. The trench-gate structure demonstrates a fivefold reduction in specific on-resistance due to its higher channel density. These results emphasize the importance of developing advanced fabrication techniques—similar to those used for low-voltage silicon UMOSFETs—to achieve small cell pitches and fully exploit the benefits of the trench-gate 4H-SiC MOSFET design.

The analytical on-resistance model presented here, originally developed to highlight the critical role of channel inversion layer mobility in SiC trench-gate MOSFETs, assumes that the entire applied drain bias is supported by the N-drift region. However, in low-voltage devices, the N-drift doping concentration becomes comparable to that of the P-base, so that a significant portion of the voltage drop occurs within the P-base region as well. An extended model that accounts for this effect predicts a further reduction in the overall specific on-resistance. Nevertheless, for SiC trench-gate MOSFETs designed to support around 1000 V, the total on-resistance remains fundamentally limited by the channel inversion layer mobility.

6.2.4 Threshold Voltage

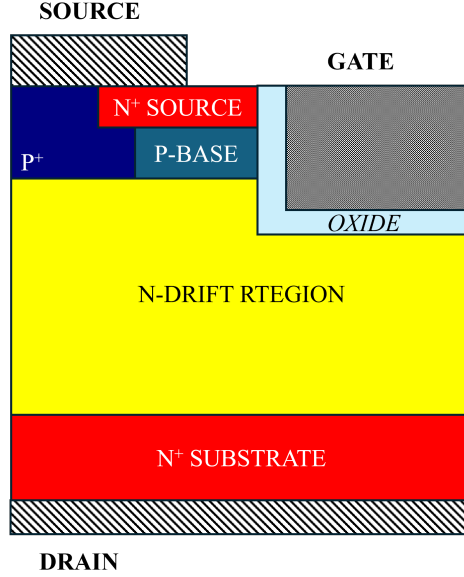


Figure 6.26. Enhanced Trench-Gate Power MOSFET Structure.

The threshold voltage of the trench-gate inversion-mode MOSFET structure can be modeled using the same physical principles previously described for the planar inversion-mode MOSFET. The threshold voltage for 4H-SiC devices can be estimated from the analytical relations and graphical data provided in that discussion. Based on this analysis, a gate oxide thickness of approximately $0.05 \mu\text{m}$ and a P-base doping concentration of $1 \times 10^{17} \text{cm}^{-3}$ yield a threshold voltage of about 5 V.

However, such a relatively low P-base doping concentration may lead to a reach-through-induced breakdown, as observed in planar 4H-SiC MOSFETs. To mitigate this limitation, a structural enhancement is illustrated in Fig. 6.26. In this configuration, a highly doped P^+ region is incorporated beneath the source region to prevent the depletion region from extending excessively into this area of the device. A thin, lightly doped P-base region is then formed adjacent to the trench sidewalls, effectively controlling the threshold voltage.

The inclusion of the P^+ region not only stabilizes the threshold voltage but also suppresses reach-through within the neighboring P-base region, thereby enabling the device to sustain high drain voltages up to the breakdown limit imposed by the drift region.

6.2.5 On state and Output Characteristics

The on-state voltage drop of the trench-gate 4H-SiC power MOSFET structure is primarily determined by its specific on-resistance. From numerical simulations performed with a gate bias of 10 V, it was observed that the current flows through the inversion channel and then spreads from the bottom of the trench into the drift region. This behavior results from the formation of an accumulation region at the trench bottom caused by the applied positive gate bias. The current then distributes into the drift region at an angle of approximately 45° before becoming uniform throughout the rest of the device. These results are consistent with the assumptions used in deriving the analytical model for forward conduction.

The specific on-resistance was simulated for various values of channel inversion-layer mobility. In these simulations, a drain bias of 1 V was applied while sweeping the gate bias up to 20 V in order to extract the transfer characteristics. A drain bias of 1 V was selected since the on-state voltage drop of such structures typically lies in this range. The resulting transfer characteristic, shown in Fig. 6.27 for a device with a cell pitch of $1\ \mu\text{m}$, indicates that the threshold voltage determining the on-resistance is approximately 5 V, allowing proper device operation at a gate bias of 10 V. This value is consistent with the analytical prediction discussed in the previous chapter for a P-base doping concentration of $9 \times 10^{16}\ \text{cm}^{-3}$ and a gate oxide thickness of $0.05\ \mu\text{m}$. The impact of varying the channel inversion-layer mobility is also illustrated in this figure: as expected, a reduction in channel mobility results in a lower drain current.

The specific on-resistance values obtained from the on-state simulations are compared in Fig. 6.28 with those calculated analytically using the model developed in the previous section. In the simulations, the channel mobility values were extracted from the current–voltage characteristics of a lateral 4H-SiC MOSFET structure, employing the same interface degradation factor used for the vertical 4H-SiC trench-gate MOSFET simulations. The analytical predictions show excellent agreement with the numerical

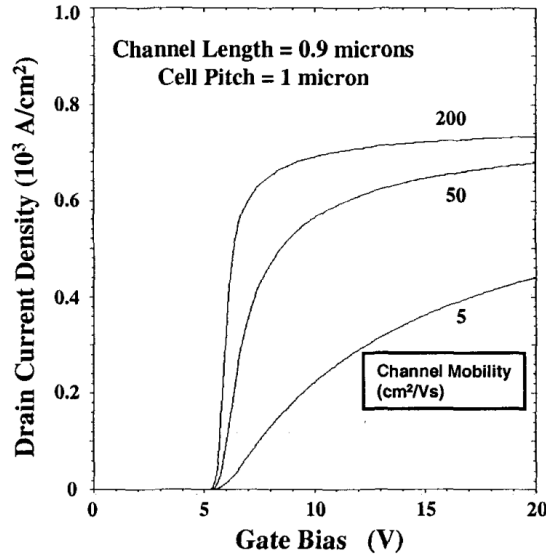


Figure 6.27. Transfer Characteristics of the 4H-SiC Trench-Gate MOSFETs.

results, thereby validating the analytical model for use in the design of trench-gate 4H-SiC power MOSFETs. From the comparison, it can be concluded that a channel mobility exceeding $50 \text{ cm}^2/\text{V}\cdot\text{s}$ is sufficient to achieve a low specific on-resistance for a 3 kV trench-gate 4H-SiC power MOSFET with a $1 \mu\text{m}$ cell pitch.

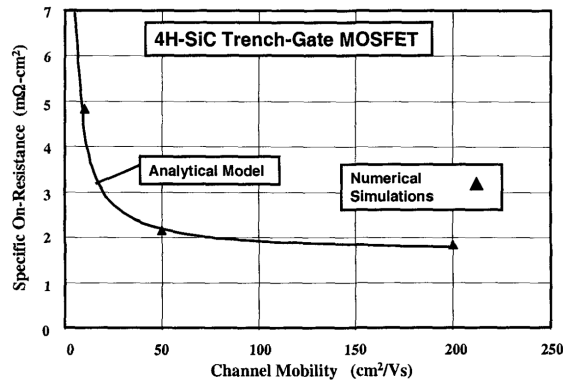


Figure 6.28. Specific On-Resistance for the 4H-SiC Trench-Gate MOSFETs.

The output characteristics of a power MOSFET define the region within which the device can safely operate during switching transients in power applications. The current–voltage loci during transient operation must remain within the limits set by these characteristics. The output characteristics of the 4H-SiC trench-gate power MOSFET structure were obtained by biasing the gate at various voltages and sweeping the drain voltage up to 2800 V. The results, shown in Fig. 6.29 for a structure with a 1 μm cell pitch, demonstrate excellent performance up to a gate bias of 10 V, with high output resistance and stable current control. However, it is important to note that the electric field within the gate oxide reaches its breakdown strength at a drain bias of approximately 1000 V. This represents a significant limitation to the safe operating area (SOA) of the trench-gate 4H-SiC MOSFET structure and must be carefully considered during device design and operation.

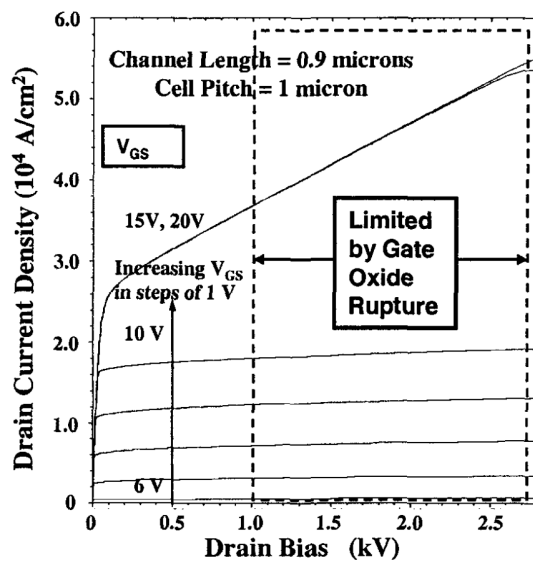


Figure 6.29. Output Characteristics of a 4H-SiC Trench-Gate MOSFET.

6.3 Recap of Conventional SiC MOSFET Architectures and Emerging Device Concepts

Throughout this dissertation, the two most established silicon carbide (SiC) MOSFET architectures — namely the **planar** and the **trench** structures — have been analyzed in detail. Both are mature technologies for medium- to high-voltage power applications (typically in the 600 V–1.7 kV range), yet they present distinct trade-offs in terms of channel mobility, gate-oxide reliability, and specific on-resistance ($R_{\text{on,sp}}$) [23, 24].

Planar SiC MOSFETs. The planar architecture represents the first generation of commercial SiC MOSFETs [23]. The inversion channel is formed laterally along the SiC/SiO₂ interface, parallel to the wafer surface. This configuration offers excellent **oxide reliability** and benefits from **well-established fabrication processes**, but the lateral channel limits the **current density** and leads to a relatively higher **specific on-resistance**, since only a portion of the surface area contributes to conduction [23]. In addition, short-channel and mobility-degradation mechanisms at the SiC/SiO₂ interface further constrain scaling [25].

Trench SiC MOSFETs. In trench MOSFETs, the inversion channel is formed vertically along the sidewalls of deep trenches etched into the SiC substrate. This geometry significantly enhances **cell density** and enables **lower** $R_{\text{on,sp}}$ compared to planar devices [23]. Nevertheless, the design introduces reliability concerns associated with **gate-oxide stress** at trench corners and increases **process complexity**, particularly in achieving smooth and passivated trench interfaces to avoid electric-field crowding [24]. Shielding and optimized trench profiles are often adopted to mitigate field concentration and improve robustness.

Recent Technological Evolutions. Recent advancements in SiC power MOSFET technology aim to combine the performance advantages of trench and planar structures while mitigating their drawbacks [26]. Representative directions include:

- **Double-Trench MOSFETs (DT-MOS)** — employ both gate and source trenches to improve charge balance and reduce R_{on} (address-

ing field crowding and conduction loss) [23];

- **Shielded Gate Trench MOSFETs (SGT-MOS)** — integrate a P-type region or a field-plate beneath the gate to *shield* the oxide from high electric fields, improving $E_{\max}$ robustness and breakdown voltage (BV) [24];
- **FinFET-like or Vertical Fin MOSFETs** — utilize a narrow SiC fin to increase channel control and enhance mobility, with recent demonstrations and analyses in SiC pointing to improved electrostatic control [27];
- **Superjunction (SJ) and Charge-Balanced Structures** — achieve an improved BV – $R_{\text{on,sp}}$ trade-off through engineered lateral charge compensation; foundational theory and limits are discussed in [28, 29, 30, 31].

Table 6.1. Comparison of main SiC MOSFET architectures: main pros, cons, and maturity.

Type	Pros	Cons	Status
Planar	Reliable oxide; easy process	High R_{on} ; low current	Comm. (Gen. 1–2)
Trench	Low R_{on} ; compact cell	Oxide stress; complex etch	Comm. (Gen. 3–4)
D-Trench	Balanced field; low loss	Difficult process; yield risk	R&D
Shielded	High BV ; safe oxide	Larger cell; extra masks	Pilot
FinFET	Good control; high μ	Hard fab; heat issues	Research
SuperJct.	Best BV – R_{on} trade-off	Tight doping control	Demo

Overall, SiC MOSFET technology continues to evolve toward structures that offer higher electric-field tolerance and improved channel controllability [26]. In this context, the emergence of **Gate-All-Around (GAA) SiC MOSFETs** represents a promising step forward, providing full electrostatic control of the channel and enabling new performance-scaling opportunities in the 1.2 kV class. Early device concepts and TCAD-based evaluations in SiC report encouraging trends for $R_{\text{on,sp}}$ and switching capability [32, 33, 34].

6.4 1.2 kV SiC Gate-All-Around MOSFET Concept and Design

The next generation of power electronic devices must deliver both high energy efficiency and high power conversion density. As extensively discussed in Chapter 2, Silicon Carbide (SiC) has emerged as the most promising semiconductor for advanced power electronics, thanks to its high critical electric field, fast switching capability, and high-temperature operation [1]. The outstanding performance of SiC, compared to conventional silicon (Si), continues to drive research efforts aimed at improving SiC device quality and reliability. Nevertheless, several technological challenges still hinder the full exploitation of SiC's material advantages.

From a device design perspective, two main architectural approaches are reported in the literature to realize high-voltage SiC MOSFETs:

- (i) Planar-gate MOSFETs;
- (ii) Trench-gate MOSFETs.

The drift region can be implemented either as a constant-doping layer or using charge-balanced structures such as Superjunction [28, 29] or Semi-Superjunction [31] configurations. All these device concepts require a termination region, which occupies a significant portion of the die area, especially in high-voltage designs. Since the termination defines the device Breakdown Voltage (BV), it directly affects both performance and manufacturing cost.

In this section, a novel SiC MOSFET architecture without a dedicated termination region is proposed and analyzed through TCAD simulations. The concept is based on **SiC pillars**, epitaxially grown on an n^+ Si substrate and fully surrounded by silicon dioxide. In the proposed **Gate-All-Around (GAA) SiC MOSFET**, the gate electrode completely wraps around the pillar region, providing full electrostatic control of the channel. The absence of a termination region is enabled by the vertical electric field distribution: the electric field peaks inside the oxide rather than at the SiC surface, thus avoiding edge breakdown phenomena.

This our work on SGAA devices has been primarily addressed in two publications [33, 34]. In a separate study [35], we demonstrated the effectiveness of incorporating a ferroelectric material as the gate oxide to

mitigate thermal stress during short-circuit tests. The main findings are summarized in the following sections.

6.4.1 The Proposed Device

A schematic representation of the proposed GAA SiC MOSFET is shown in Fig. 6.30. The overall structure consists of multiple n-type SiC cylindrical pillars (unit cells), each surrounded by a silicon dioxide layer and connected in parallel. The pillars are grown on a heavily doped n^+ Si substrate, which acts as a common drain contact. On the top surface, a P-body region forms the channel, surrounded by a thin SiO_2 gate oxide that is connected to the gate electrode. Although high- k dielectrics could potentially improve gate control, in this work standard silicon dioxide has been considered in order to evaluate the intrinsic device performance using conventional materials.

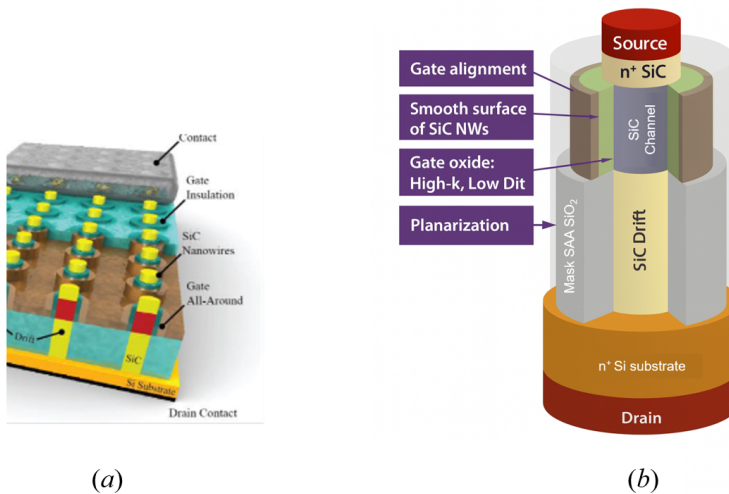


Figure 6.30. a) A sketch of the overall SiC GAA MOSFET design concept, b) A detail of the single pillar structure.

The TCAD model of the proposed device is assumed to be rotationally symmetric along the vertical axis, as illustrated in Fig. 6.31. Both the SiC pillar and the surrounding oxide contribute to the active area of the device. The geometrical relationship between the pillar and oxide regions

is defined as illustrated in Fig. 6.31(b), where $L_1 = 2(R_{CH} + R_{o2})$. Further design parameters are summarized in Table 6.2. The cylindrical geometry of the single cell enables the use of a 2D axisymmetric mesh to simulate the full 3D electrostatic behavior with reduced computational cost. Standard physical models were adopted for the TCAD simulations, including carrier mobility, recombination, and impact ionization models. Fixed interface charges at the SiC/SiO₂ boundary were also considered.

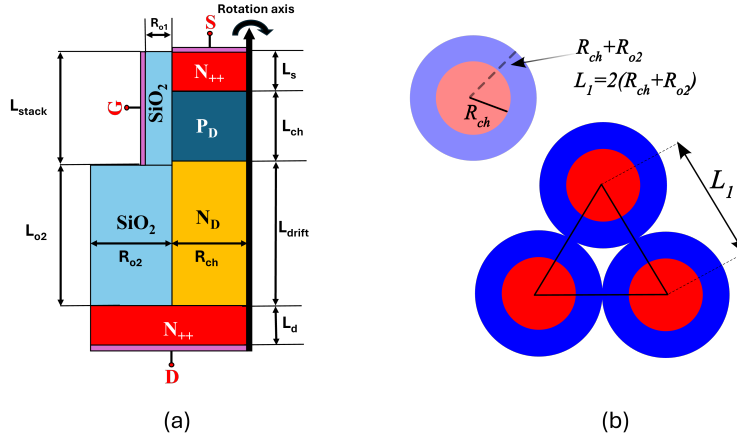


Figure 6.31. A sketch of the TCAD structure. a) A vertical section of a single pillar and b) the spatial distribution assumed among the pillars within this work.

Table 6.2. Design Parameters of the Proposed SiC GAA MOSFET.

Parameter	Value	Parameter	Value
R_{o1}	$0.05 \mu\text{m}$	L_{drift}	$6 \mu\text{m}$
R_{o2}	$0.2 \mu\text{m}$	L_{stack}	$0.7 \mu\text{m}$
L_{o2}	$5.9 \mu\text{m}$	R_{ch}	$2 \mu\text{m}$
L_d, L_s	$0.1 \mu\text{m}$	L_{ch}	$0.5 \mu\text{m}$
N^{++}	$5 \times 10^{18} \text{cm}^{-3}$	P_D	$4 \times 10^{17} \text{cm}^{-3}$
		N_D	$1.1 \times 10^{16} \text{cm}^{-3}$

6.4.2 Quantum Confinement Considerations

When the radius of the SiC pillar becomes comparable to a few tens of nanometers, it approaches the characteristic length scale associated with the electron de Broglie wavelength, and **quantum confinement effects** start to appear [36]. The (non-relativistic) electron wavelength can be estimated by:

$$\lambda = \frac{h}{\sqrt{2m^*E}}, \quad (6.20)$$

where h is Planck's constant, m^* is the electron effective mass, and E is the kinetic energy of the electron, which can be approximated by the thermal energy $E \approx kT$, where k is the Boltzmann constant and T the absolute temperature.

Assuming $m^* = 0.3m_0$ (typical for 4H-SiC) and $T = 300$ K, we obtain:

$$\lambda = \frac{6.63 \times 10^{-34}}{\sqrt{2 \times 0.3 \times 9.11 \times 10^{-31} \times 4.14 \times 10^{-21}}} \approx 8\text{--}10 \text{ nm}. \quad (6.21)$$

Hence, when the channel radius R_{CH} approaches ~ 10 nm, the confinement energy becomes non-negligible, leading to discrete energy levels and a widening of the effective bandgap E_G . This behavior marks the transition from classical to quantum transport.

In Synopsys TCAD, this phenomenon is modeled using the **Modified Local Density Approximation (MLDA)** approach [9], which accounts for quantum corrections to the electron density distribution and allows a more accurate description of inversion-layer mobility.

When $R_{CH} \gg 10$ nm, the electrons in the channel can be considered as free particles, and bulk-like transport models are valid. However, when $R_{CH} \approx 10$ nm, both electronic and optical properties start deviating from their bulk values, as the inversion layer thickness approaches the **exciton Bohr radius**. In this regime, the energy spectrum becomes discrete and E_G becomes size-dependent — a hallmark of the quantum confinement effect. For a rigorous mathematical and physical treatment of this effect—and its engineering implications—see [36].

6.4.3 Device Dimensions, Simulation Setup and Results

The length of the drift region (L_{drift}) was set to $6\text{ }\mu\text{m}$, allowing a breakdown voltage (BV) of approximately 1300 V, without requiring a dedicated termination region. The extensive numerical characterization of the proposed structure is carried out through TCAD simulations, including both the static forward (J_D – V_{GS} and J_D – V_{DS}) and reverse characteristics. All the numerical results reported in this work refer to a configuration in which the source region is connected to the P-body through an ohmic contact located along the symmetry axis.

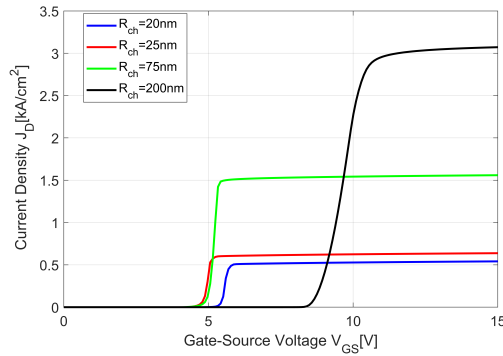


Figure 6.32. Sub-threshold transfer characteristics for different pillar radius R_{ch} .

Figure 6.32 shows the sub-threshold J_D – V_{GS} characteristics for devices with channel radii (R_{ch}) of 20 nm, 25 nm, 75 nm, and 200 nm. Assuming that the threshold voltage V_{TH} is defined as the gate voltage V_{GS} at which $J_D = 10\text{ A/cm}^2$, and that the sub-threshold slope is evaluated at $J_D = 10^{-10}\text{ A/cm}^2$, a peculiar dependence of V_{TH} on the radius is observed: it decreases as the radius is reduced down to 75 nm, but increases again for radii below 25 nm (see Fig. 6.33).

More specifically, the sub-threshold region exhibits two coexisting effects that influence the V_{TH} –radius dependence:

- (i) As the radius decreases, the drain current increases for very low V_{GS} values (e.g., $V_{GS} = 2.5\text{ V}$);

- (ii) The sub-threshold slope initially increases with decreasing radius down to 75 nm, and then decreases for smaller radii.

The latter effect is governed by the ratio between the oxide capacitance (C_{OX}) and the depletion capacitance (C_D). The slope in the sub-threshold region is expressed as:

$$S = \frac{q}{\ln(10) kT} \left(\frac{C_{OX}}{C_{OX} + C_D} \right), \quad (6.22)$$

where q is the elementary charge, k is the Boltzmann constant, and T is the absolute temperature.

The oxide capacitance per unit area for a cylindrical structure is given by:

$$C_{OX} = \frac{\varepsilon_{OX}}{\ln \left(\frac{R_{ch} + R_{o1}}{R_{ch}} \right) R_{ch}}, \quad (6.23)$$

where ε_{OX} is the oxide permittivity.

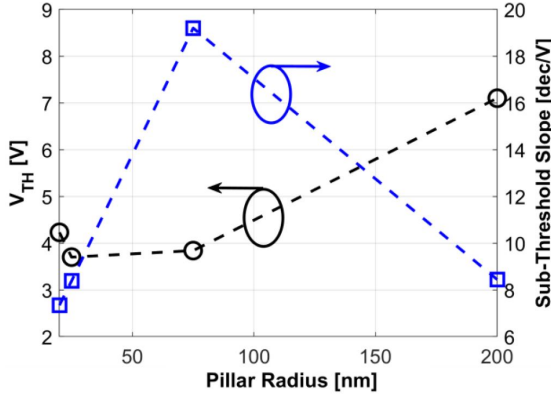


Figure 6.33. V_{TH} and Sub-threshold slope dependence on the pillar radius R_{ch} .

As shown in Fig. 6.34, C_{OX} increases as the radius decreases, leading to a reduction in V_{TH} , which is inversely proportional to C_{OX} . When the pillar radius becomes sufficiently small, the P-body depletion region extends across the entire pillar cross-section. At this point, the P-body capaci-

tance behaves as that of a cylindrical capacitor with silicon permittivity. For very small radii, C_{OX} continues to increase according to (6.23), but C_D rises even faster, thereby reducing the sub-threshold slope and causing an increase in V_{TH} . When the radius is below 50 nm, the depletion capacitance C_D dominates, further decreasing the slope and enhancing the threshold voltage.

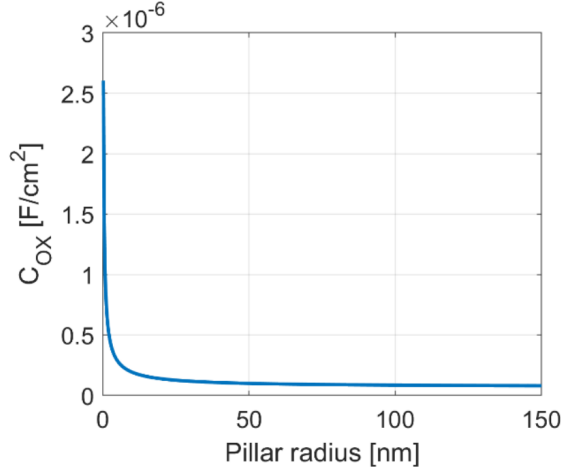


Figure 6.34. Analytical C_{OX} dependence on the pillar radius R_{ch} .

The analysis of the high-current regime is performed by evaluating the current density within the SiC portion of the pillar. Assuming that the oxide spacer between pillars has constant thickness, the overall current density per device area scales down proportionally to a geometric factor. The high-current J_D - V_{GS} curves in Fig. 6.35 show that a smaller radius leads to higher series resistance at large current levels. For this design, the channel resistance is comparable to—or even smaller than—the drift region resistance, resulting in current limitation by the drift region at low gate voltages. The main advantage of the proposed configuration is that the conduction channel extends around the entire perimeter of the pillar. However, the on-resistance (R_{ON}) is ultimately limited by the narrow drift region.

In Fig. 6.36, the extracted capacitances C_{ISS} , C_{OSS} , C_{DS} , and C_{RSS} are shown for a radius of 75 nm. Results indicate that the gate-to-drain

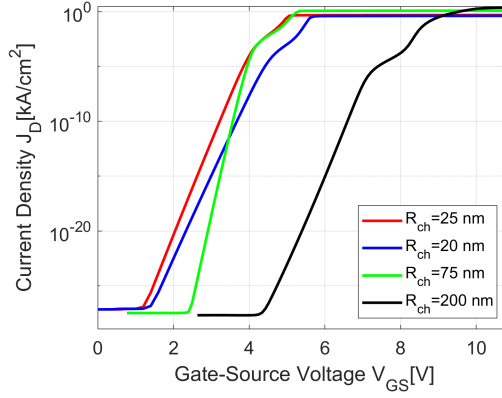


Figure 6.35. High current transfer curves for different pillar radius R_{ch} .

(G/D) and gate-to-source (G/S) overlaps are negligible. Interestingly, as C_{DS} remains very small, this leads to $C_{RSS} \approx C_{OSS}$, with both showing similar variation with the drain voltage.

Figure 6.37 reports the J_D - V_{DS} characteristics for four different radius values. For $R_{ch} > 75$ nm, the saturation current slightly decreases, whereas it increases more than linearly for radii of 20 nm and 25 nm. The corresponding on-resistance (R_{ON}), extracted at $J_D = 200$ A/cm², is shown in Fig. 6.38.

The blocking J_D - V_{SD} characteristics for the same designs are reported in Fig. 6.39. For a fixed interface charge density (Q_F) at the SiC/SiO₂ interface, the breakdown voltage (BV) remains nearly constant.

Finally, Fig. 6.40 reports the reverse J_D - V_{SD} characteristics for two different Q_F values and two radii. The results clearly show that Q_F significantly affects the BV : higher Q_F values lead to a lower breakdown voltage.

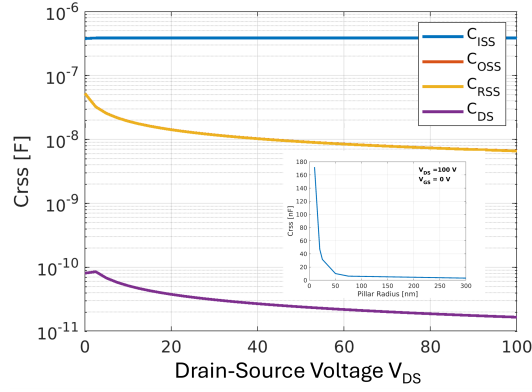


Figure 6.36. C_{ISS} , C_{OSS} , C_{RSS} and C_{DS} values for pillar radius of 75 nm. In the insert the dependence of the C_{RSS} vs the pillar radius R_{ch} . $ActiveArea = 1 \text{ cm}^2$.

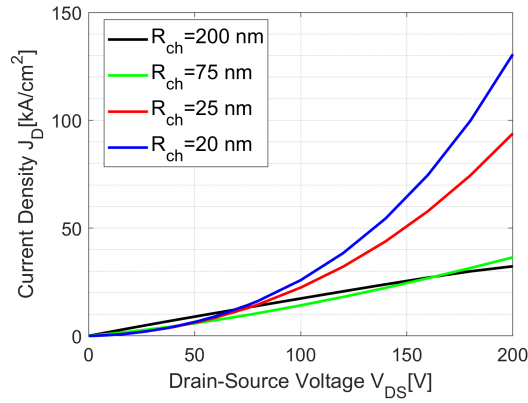


Figure 6.37. Output curves for different pillar radius R_{ch} . $V_{GS} = 15 \text{ V}$, $T = 25^\circ\text{C}$. $ActiveArea = 1 \text{ cm}^2$.

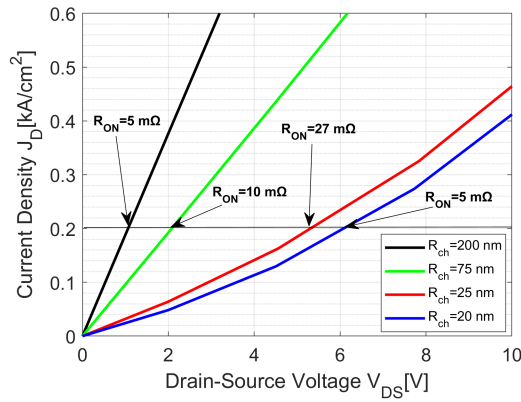


Figure 6.38. A zoom of the output curves for different pillar radius R_{ch} . $V_{GS} = 15 \text{ V}$, $T = 25^\circ\text{C}$. $\text{ActiveArea} = 1 \text{ cm}^2$.

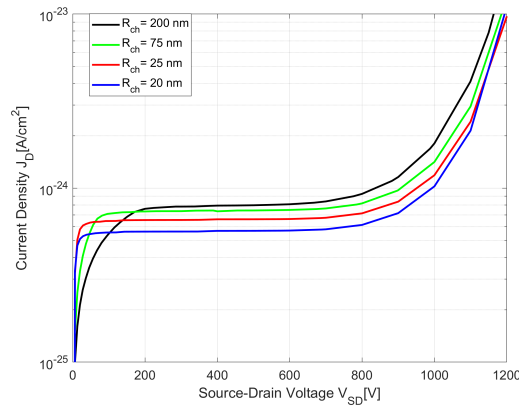


Figure 6.39. blocking $J_D - V_{SD}$ curves for different pillar radius R_{ch} .

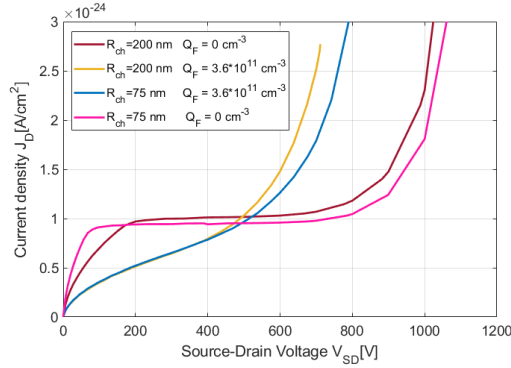


Figure 6.40. Blocking $J_D - V_{SD}$ curves for two (Q_F values 0 cm^{-3} and $3.6 \times 10^{11} \text{ cm}^{-3}$) and two pillar radius values. $R_{ch} = 200 \text{ nm}$ and $R_{ch} = 75 \text{ nm}$.

6.4.4 Evaluation of Short Circuit Capability of The SiC SGAA

The short-circuit capability was assessed by means of electro-thermal simulations. Figure 6.41 reports both the drain current (I_D) and the maximum device temperature for channel radii of 50 nm and 1 μm . As expected, the structure exhibits poor short-circuit ruggedness due to the large fraction of silicon dioxide in the active stack. For the 1 μm pillar, even though the current turns off, the temperature does not return to its initial value; instead, it remains elevated and eventually triggers a delayed thermal-runaway failure. Neither structure can withstand a 1 μs short-circuit pulse. For the 50 nm pillar, the maximum temperature rises abruptly to very high values. *The test circuit and the short-circuit stress conditions (including supply, gate drive, pulse width, and boundary conditions) will be described in detail in the next section.* An additional effect is observed during the short-circuit event for the 50 nm pillar: the temperature peak occurs on the drain side rather than on the P-body side (see Fig. 6.42). Conversely, for the larger (1 μm) pillar the temperature peak is located beneath the P-body region, as typically expected. Overall, the proposed structure shows very limited short-circuit capability.

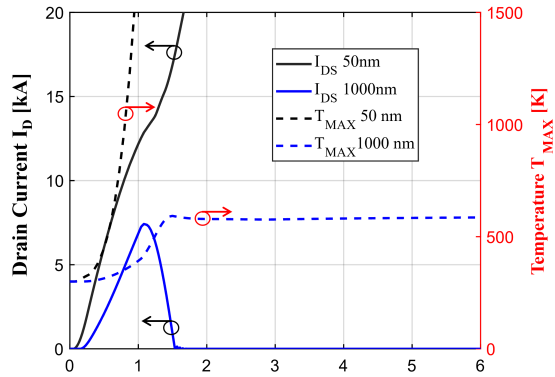


Figure 6.41. Short circuit waveforms for two pillar radius values.

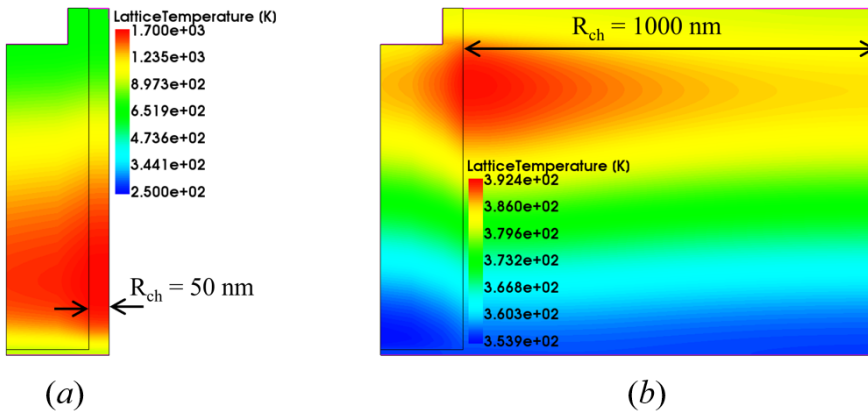


Figure 6.42. Temperature distribution at the end of the 1 ms pulse into the a) 50 nm structure and the b) 1000 nm.

6.4.5 SiC GAA MOSFETs: Electrothermal Gains Enabled by Ferroelectric Gate Stacks

In planar MOSFETs, it has been demonstrated that integrating a ferroelectric material (e.g., HfO_2) into the gate stack can improve thermal management during transient events by leveraging the temperature-dependent dielectric behavior (Figs. 6.43–6.44) described by Curie–Weiss theory [37]. Building on this concept, in this section we propose, for the first time, the integration of a SiO_2 /ferroelectric gate stack into the SGAA architecture, replacing the conventional oxide layer (Fig. 6.45). This novel design—referred to as **FERRO POWER SGAA**—exploits the reduction in dielectric constant with temperature (Fig. 6.44) to mitigate current overshoot during short-circuit conditions, thereby enhancing device robustness.

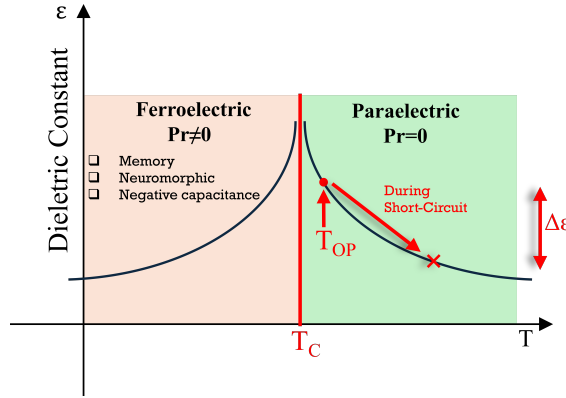


Figure 6.43. Typical temperature behavior of the dielectric constant in ferroelectric materials. While conventional low-power applications operate below the Curie temperature (T_C) to exploit ferroelectric properties, the FERRO POWER SGAA is designed to function above T_C , leveraging the temperature-dependent decrease in permittivity to enhance short-circuit robustness.

Therefore, in this work, unlike the standard SGAA design, the gate oxide is replaced by a SiO_2 /ferroelectric stack as shown in Fig. 6.45, where the vertical cross-section of a single FERRO POWER SGAA cell is reported. The SiO_2 layer ensures high-quality interface properties with SiC, while the ferroelectric layer—operating in its paraelectric phase (i.e., above its Curie temperature, T_C)—exhibits a dielectric constant that decreases

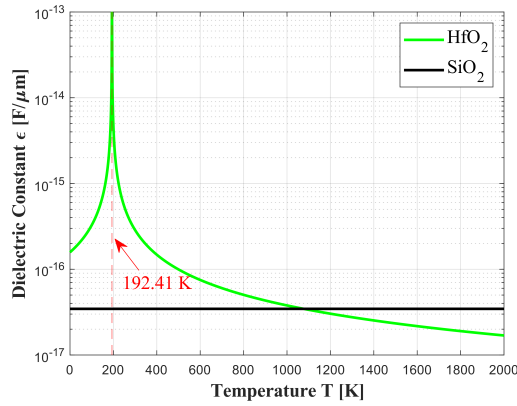


Figure 6.44. Temperature dependence of the dielectric constant: ferroelectric HfO_2 [$\epsilon(T)$] vs. SiO_2 (ϵ_{OX}).

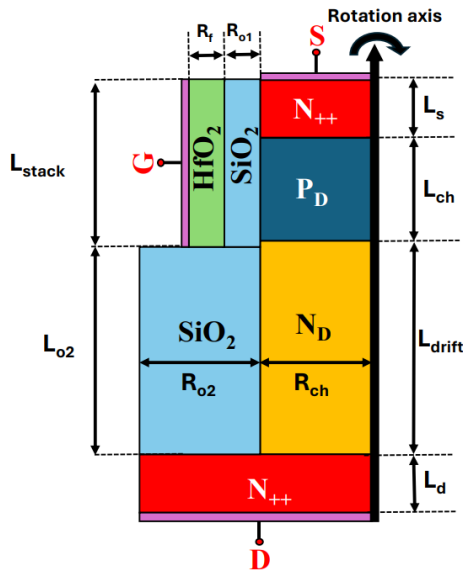


Figure 6.45. A sketch of the TCAD structure of the FERRO POWER SGAA.

with increasing temperature (Figs. 6.43–6.44). The ferroelectric material considered in this study is hafnium oxide (HfO_2), an overview of which is given in the following discussion.

For a standard SGAA MOSFET, the drain current follows

$$I_D(T) \propto C_{OX} \mu(T) \left[(V_{GS} - V_{TH}(T)) V_{DS} - \frac{1}{2} V_{DS}^2 \right], \quad (6.24)$$

where C_{OX} is the cylindrical gate-oxide capacitance per unit area:

$$C_{OX} = \frac{\varepsilon_{OX}}{\ln\left(\frac{R_{ch} + R_{ol}}{R_{ch}}\right) R_{ch}}. \quad (6.25)$$

Here, μ is the carrier mobility, ε_{OX} is the dielectric permittivity of SiO_2 , and V_{GS} , V_{DS} , and V_{TH} denote the gate–source voltage, drain–source voltage, and threshold voltage, respectively. Equation (6.24) highlights the temperature-dependent parameters μ and V_{TH} . As temperature rises, V_{TH} typically decreases due to increased carrier generation, which tends to increase I_D [1]. Carrier mobility μ may initially improve due to reduced Coulomb scattering but generally declines at higher temperatures due to phonon scattering [38]. Overall, I_D often decreases at high temperature because of mobility degradation. However, during high-current or prolonged short-circuit conditions, leakage currents may dominate, potentially causing thermal runaway.

The key innovation of the FERRO POWER SGAA lies in replacing the temperature-invariant C_{OX} with a temperature-dependent gate capacitance. This mitigates V_{TH} reduction and suppresses temperature/current surges. The effect is achieved by integrating a ferroelectric layer into the gate stack, exploiting its temperature-sensitive permittivity [39]. Electrically, the gate stack behaves as two cylindrical capacitors in series: one with constant capacitance (SiO_2) and one with temperature-dependent capacitance (ferroelectric). Ferroelectric materials exhibit spontaneous polarization reversible via an external electric field, showing a temperature-dependent hysteresis in the polarization–electric field (P–E) curve [40, 41]. According to Landau’s theory [39], the phase transition at T_C marks the shift to the paraelectric phase, eliminating hysteresis [42]. The temperature dependence of the relative permittivity ε_r follows the Curie–Weiss

law:

$$\varepsilon_r(T) = \lambda \frac{C_{CW}}{T - T_C}, \quad (6.26)$$

with the sign factor λ defined as

$$\lambda = \begin{cases} -1, & T < T_C, \\ 1, & T \geq T_C, \end{cases} \quad (6.27)$$

so that the absolute dielectric constant reported in Fig. 6.49 reads

$$\varepsilon(T) = \varepsilon_r(T) \varepsilon_0. \quad (6.28)$$

Here, C_{CW} is the Curie–Weiss constant and ε_0 is the vacuum permittivity. It should be noted that ε_r is highly sensitive to processing conditions, including annealing, doping, and grain structure [43].

The capacitance per unit area of a cylindrical ferroelectric capacitor is given by

$$C_{FE}(T) = \frac{\varepsilon(T)}{\ln\left(\frac{R_{ch} + R_{o1} + R_f}{R_{ch} + R_{o1}}\right) (R_{ch} + R_{o1})}, \quad (6.29)$$

where the parameters are summarized in Table 9.

Lastly, the total gate-stack capacitance per unit area in the FERRO POWER SGAA (series combination of SiO_2 and ferroelectric) is

$$C_{FE,\text{stack}}(T) = \frac{C_{FE}(T) C_{OX}}{C_{FE}(T) + C_{OX}}, \quad (6.30)$$

whose temperature dependence is shown in Fig. 6.46.

Unlike low-power ferroelectric devices (e.g., memory, negative-capacitance switches) that operate below T_C to exploit hysteresis, the FERRO POWER SGAA is designed to operate above T_C . During normal operation and switching, the temperature exceeds T_C (see red dot in Fig. 6.48), placing the ferroelectric in its paraelectric phase. During short-circuit events, additional temperature rise reduces $C_{FE,\text{stack}}$ due to the drop in $\varepsilon_r(T)$ (red cross in Fig. 6.43). This diminishes gate coupling and slows current growth—creating a negative electrothermal feedback that helps stabilize the device. Importantly, above T_C the device exhibits no hysteresis, which

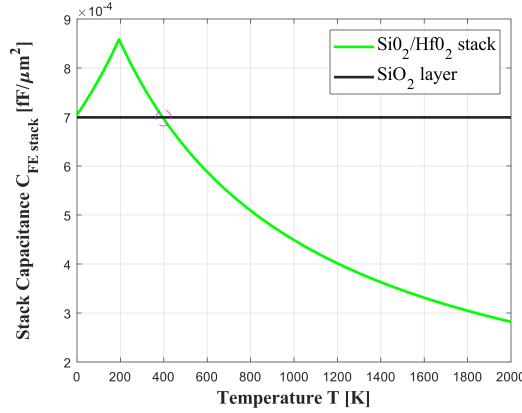


Figure 6.46. Comparison between the capacitance of the $\text{SiO}_2/\text{HfO}_2$ stack (81.25 nm) and that of a SiO_2 layer (50 nm). The two capacitances are equal at the operating temperature of 400 K.

is desirable in switching applications. The oxide and ferroelectric thicknesses must be chosen to match the performance of a standard SGAA at the designated operating temperature. The FERRO POWER SGAA is thus expected to behave equivalently during normal operation, while outperforming under short circuit. This performance equivalence and enhancement are formally expressed as

$$C_{FE,stack}(T) = C_{RE} \quad \text{if } T = T_{OP}, \quad (6.31)$$

$$C_{FE,stack}(T) < C_{RE} \quad \forall T > T_{OP}, \quad (6.32)$$

where T_{OP} is the operating temperature (400 K), and C_{RE} represents the cylindrical gate capacitance of a reference SGAA MOSFET at the same temperature. Equation (6.31) ensures that the output and transfer characteristics of the proposed device align with those of the reference SGAA device, whereas Eq. (6.32) guarantees enhanced short-circuit robustness at temperatures exceeding T_{OP} .

To ensure a fair comparison, the *standard* SGAA and the *FERRO POWER* SGAA structures are **identical** and were simulated using the **same device parameters** reported in Table 6.2; in this case, the channel radius is fixed at $R_{ch} = 2 \mu\text{m}$. Under these common settings, and in order

to achieve a one-to-one *DC matching* at T_{OP} with the conventional SGAA, the gate dielectric of the FERRO POWER SGAA was implemented as a $\text{SiO}_2/\text{HfO}_2$ stack with a **total thickness of 81.25 nm, equally split** between the two layers, *instead of the 50 nm* SiO_2 gate oxide used in the standard structure (see Table 6.2). The effectiveness of this choice in reproducing the reference DC characteristics is illustrated in Figs. 6.47 and 6.48, while the short-circuit performance is shown in Fig. 6.51.

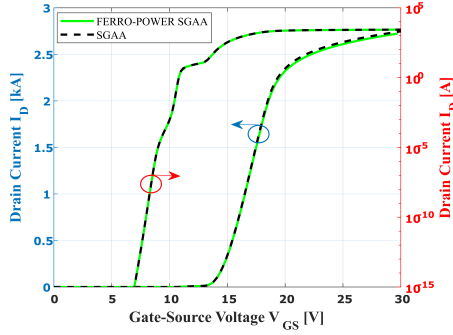


Figure 6.47. Comparison of the static performance of the FERRO POWER SGAA and SGAA at the operative temperature of 400 K: Isothermal transfer characteristics in linear and logarithmic scales for $V_{DS} = 20$ V.

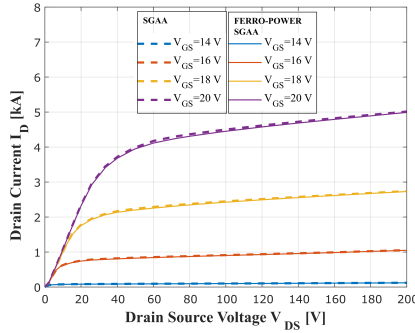


Figure 6.48. Comparison of the static performance of the FERRO POWER SGAA and SGAA at the operative temperature of 400 K: Isothermal output characteristics by varying V_{GS} .

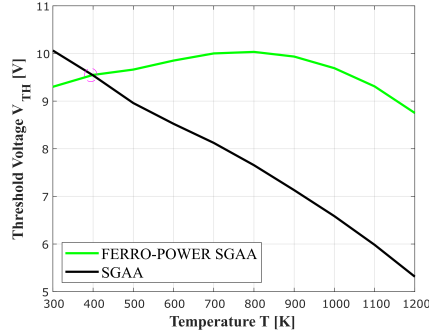


Figure 6.49. V_{TH} comparison between FERRO POWER SGAA and standard SGAA. V_{TH} is extracted from isothermal simulations as the gate voltage at which the channel electron density equals the ionized acceptor density. Analysis performed at $V_{DS} = 0$ V to avoid 2D effects.

6.4.6 Results: Electrothermal Behavior in Short-Circuit Conditions

Mixed-mode electrothermal TCAD simulations represent a powerful tool for evaluating the behavior of power devices under real operating conditions. In our short-circuit analysis, the simulated test circuit consists of a gate-connected pulse source (V_{GG}), with the drain terminal biased at the supply voltage (V_{BUS}). To emulate parasitic effects introduced by the packaging, stray inductances of 7 nH and 40 nH are added at the source and drain terminals, respectively [24, 44]. The short-circuit testbench and the corresponding component values are reported in Fig. 6.50 and Table 6.3, respectively. To model transient self-heating, a thermal contact was applied to the drain surface of the FERRO POWER SGAA MOSFET. This enables the implementation of a mixed (Robin-type) thermal boundary condition, where the heat exchange with the environment is represented by a surface thermal resistance (r_{th} , orange dashed line in Fig. 6.50), and the ambient temperature is set at 300 K.

However, due to the novelty of the SGAA architecture, no experimental thermal data are currently available for this specific device configuration. As a result, the r_{th} value adopted in the simulations ($0.01 \text{ cm}^2\cdot\text{K}/\text{W}$) was extrapolated from literature studies on planar MOSFETs [24, 45], de-

spite the significant differences in geometry, manufacturing technology, and thermoelectric behavior between planar and SGAA MOSFETs. In spite of this limitation, the goal of this work is not to determine an exact value for r_{th} , but rather to demonstrate the potential of incorporating a ferroelectric material to mitigate harmful thermal effects during short-circuit events. Therefore, the absolute value of r_{th} is not critical in this context; what truly matters is the *relative* electrothermal performance under identical thermal boundary conditions when comparing the FERRO POWER SGAA to the standard SGAA.

Finally, short-circuit tests were performed at 800 V with a pulse duration of 5 μ s, in accordance with established methodologies for assessing short-circuit robustness in 1.2 kV SiC MOSFETs [46, 47, 48]. As shown in Fig. 6.51, the FERRO POWER SGAA initially conducts more current during the first 1.5 μ s, owing to its higher C_{OX} (Fig. 6.46) and lower threshold voltage V_{TH} in the 300–400 K range (Fig. 6.49). However, beyond 400 K (i.e., above T_{OP}), this trend inverts: around 1.5 μ s, the drain current of the FERRO POWER SGAA drops sharply below that of the standard SGAA. At approximately 2.3 μ s, a thermal crossover occurs: the temperature rise of the FERRO POWER SGAA slows down, leading to a lower final peak temperature by the end of the gate pulse (5 μ s), compared to the standard SGAA.

Table 6.3. Short-circuit testbench parameters.

Element	Symbol	Value
Bus voltage	V_{BUS}	800 V
Gate drive (amplitude)	$V_{GG,amp}(t)$	18 V
Gate pulse width	t_p	5 μ s
Gate resistor	R_G	5 Ω
Source sense resistor	R_S	1 m Ω
Stray inductance (source)	L_{STRAY1}	7 nH
Stray inductance (drain)	L_{STRAY2}	40 nH
Thermal resistance (surface)	r_{th}	0.01 cm ² K/W

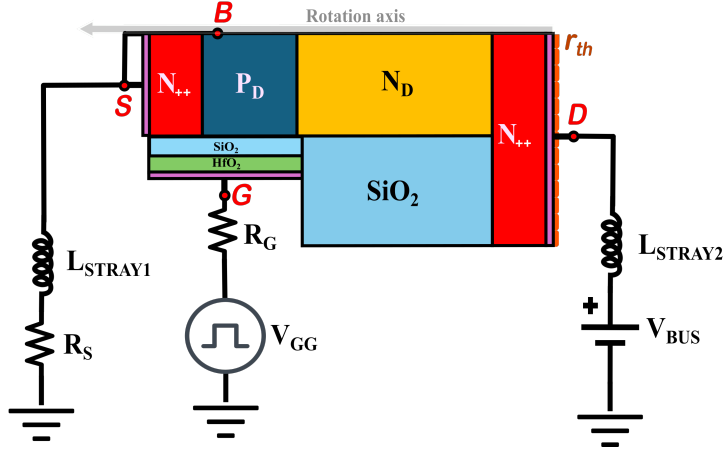


Figure 6.50. Electro-thermal mixed-mode circuit used to simulate the short-circuit event of the devices under test (DUT).

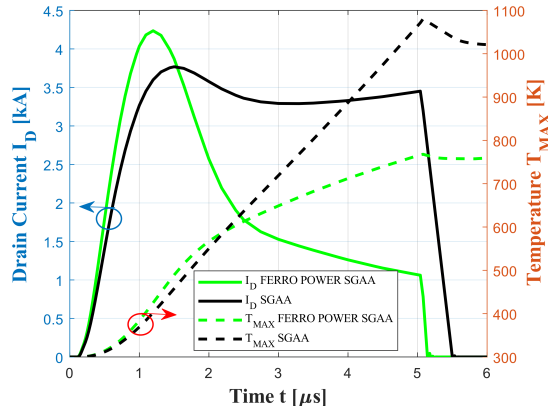


Figure 6.51. Short-circuit behavior of FERRO POWER SGAA vs. standard SGAA. Drain-current (I_D) and surface-temperature waveforms for both devices during a short-circuit event with $V_{BUS} = 800$ V applied for $5 \mu s$.

6.4.7 Case Study: Ferroelectric HfO₂

As previously mentioned, the device operates above the Curie temperature (T_C), where the polarization–electric field (P–E) curve no longer exhibits hysteresis. Consequently, this study focuses exclusively on the Curie–Weiss behavior of the dielectric constant, deliberately excluding any effects related to polarization hysteresis. Hafnium oxide (HfO₂) is selected as the ferroelectric material for this case study due to its proven compatibility with CMOS technology. Depending on the processing conditions—such as film thickness, oxidant dose, and annealing treatment—HfO₂ can exhibit ferroelectric properties in both doped [49] and undoped [50] forms. Moreover, its integration into semiconductor processes is well established, as the non-ferroelectric phase of HfO₂ is already widely used as a high- k dielectric in modern integrated circuits [51, 52].

The temperature dependence of the dielectric constant in the paraelectric phase of HfO₂ was extracted from experimental data reported in [53]. The inverse dielectric constant ($1/\epsilon$) was fitted using the Curie–Weiss law, yielding a Curie temperature (T_C) of 193 K and a Curie–Weiss constant (C_{CW}) of 3447 K. This T_C ensures sufficient thermal margin, guaranteeing that the device operating temperature remains well above the ferroelectric–paraelectric transition point. These parameters were implemented in Sentaurus simulations via a user-defined physical model. While HfO₂ has been extensively studied for its ferroelectric behavior below T_C —particularly across various dopants and concentrations—its dielectric behavior above T_C has received significantly less attention. To date, the only available studies are [37, 54, 55], where the advantages of using HfO₂ above T_C in planar power MOSFETs were first demonstrated. This work showed that the temperature-dependent dielectric constant can help suppress local temperature and current-density peaks during short-circuit events, thereby mitigating unwanted thermal drift and improving device robustness.

6.4.8 Summary

In this study, we have proposed a novel SiC-based power MOSFET architecture, termed the **FERRO POWER SGAA**. A key limitation of the conventional SGAA design lies in its poor robustness under short-circuit conditions, primarily due to the low thermal conductivity of the surrounding SiO₂ gate oxide. In our design, we integrated a ferroelectric stack—specifically SiO₂/HfO₂—instead of the usual SiO₂. Above the Curie temperature T_C , HfO₂ operates in the paraelectric regime, exhibiting a temperature-dependent dielectric constant that decreases with increasing temperature, following the Curie–Weiss law. Electrically, the SiO₂/HfO₂ stack behaves as two series capacitors. The equivalent gate capacitance $C_{FE,stack}$ was dimensioned to match the DC characteristics (both transfer and output) of the FERRO POWER SGAA to those of the reference SGAA at the operating temperature $T_{OP} = 400$ K, while simultaneously enhancing short-circuit resilience by leveraging the thermal drop in permittivity beyond T_{OP} . Mixed-mode TCAD simulations show that the FERRO POWER SGAA exhibits a substantially lower peak temperature at the end of a 5 μ s gate pulse compared to the standard SGAA. Although it shows a higher peak drain current in the 300–400 K range—due to the higher gate capacitance and lower threshold voltage—its drain current rapidly decreases beyond T_{OP} , leading to a significantly lower average current over the entire pulse duration. These results confirm that integrating a ferroelectric gate stack can significantly improve short-circuit robustness in cylindrical SiC GAA MOSFETs.

Conclusions

This dissertation has developed along two complementary research lines.

Line I — Compact electrothermal modeling and experiments on SiC JBS/MPS diodes. The first line focused on a scalable, SPICE-compatible compact model for SiC merged-PiN-Schottky (MPS) diodes capable of describing both unipolar and bipolar conduction while accounting for temperature and self-heating effects. Crucially, the model also captures the *snapback* phenomenon, which can strongly impact the reliability of MPS diodes by triggering local current focusing and premature device failure. The proposed circuit framework offers, for the first time to our knowledge, a lumped-parameter interpretation of snapback that can inform the design of power semiconductor devices beyond MPS structures, wherever similar conduction mechanisms arise.

The model's validity was demonstrated in a realistic case where two non-optimally matched parallel diodes—with small structural differences—were subjected to surge testing. Compared with full electrothermal simulations, the compact approach proved simpler and faster to deploy in scenarios that are often cumbersome for standard device simulators, significantly reducing pre-processing and runtime while maintaining physical fidelity.

Within this first research line, an experimental campaign was also carried out on a specific class of 1.2 kV SiC JBS diodes to optimize die *wire-bonding* strategies inside the package with the goal of improving surge

robustness. Pulsed I–V, thermal resistance, and surge measurements were performed, complemented by failure analysis, across three distinct bonding configurations. The study experimentally showed that the “stitch” configuration delivers superior surge robustness compared to the alternatives. Furthermore, failure analysis highlighted clear differences in the dominant failure mechanisms across the three options. These results will be expanded in a future journal paper, where additional simulations and thermo-physical analysis will be used to explain the physical origin of the observed asymmetry in failure modes.

Line II — Study and development of 1.2 kV SiC Gate-All-Around (GAA) MOSFETs. The second line addressed the study, development, and simulation of 1.2 kV SiC Gate-All-Around (GAA) MOSFETs. Mixed-mode electrothermal TCAD simulations (as well as static and dynamic analyses) revealed several attractive physical–electrical properties. The MOSFET channel, wrapped at 360° by the gate oxide, enables superior electrostatic control and a more uniform electric-field distribution. Notably, this architecture can eliminate the dedicated termination region and thereby increase the active area, improving the trade-off between specific on-resistance and blocking capability.

However, because the GAA structure is fully surrounded by silicon dioxide, it demonstrates limited capability to handle thermal stress—especially during short-circuit events. To address this limitation, the final part of the dissertation proposes, and for the first time demonstrates via TCAD, the effectiveness of integrating a ferroelectric (HfO_2) gate stack within the SGAA to limit current and thus self-heating during short-circuit transients. Based on experimental dielectric data for HfO_2 reported in the literature, we developed a temperature-dependent permittivity model implemented in Synopsys Sentaurus through a user-defined physical model (Physical Model Interface, PMI), since standard TCAD tools do not natively support temperature-dependent dielectric constants. The results indicate that a ferroelectric gate stack can introduce a beneficial negative electrothermal feedback under stress, thereby enhancing short-circuit robustness without penalizing nominal operation.

Overall perspective. Across both research lines, the contributions span modeling, experimental methodology, and device-architecture innovation: (i) a scalable electrothermal compact model for SiC JBS/MPS diodes—including snapback—with TCAD validation and application to surge scenarios; (ii) a systematic, measurement-driven assessment of bonding strategies to improve surge robustness in 1.2 kV SiC JBS diodes; (iii) the conception and advanced TCAD evaluation of a 1.2 kV SiC GAA MOSFET, including a ferroelectric gate-stack solution that mitigates thermal stress in short-circuit conditions. Together, these results provide concrete guidelines for both device designers and circuit engineers targeting efficient, reliable SiC power electronics in transportation and related high-performance applications.

Bibliography

- [1] B. J. Baliga. *Silicon Carbide Power Devices*. World Scientific, Singapore, 2005.
- [2] B. J. Baliga. *Advanced Power Rectifier Concepts*. Springer, New York, NY, USA, 2009.
- [3] H. Niwa, J. Suda, and T. Kimoto. Ultrahigh-voltage SiC MPS diodes with hybrid unipolar/bipolar operation. *IEEE Transactions on Electron Devices*, 64(3):874–881, March 2017.
- [4] Massimo Rudan. *Physics of Semiconductor Devices*. Springer, Cham, Switzerland, 2nd edition, 2018.
- [5] E. H. Rhoderick and R. H. Williams. *Metal-Semiconductor Contacts*. Clarendon Press (Oxford Univ. Press), Oxford, U.K., 2nd edition, 1988.
- [6] V. Terracciano, A. Borghese, M. Boccarossa, V. D’Alessandro, and A. Irace. A geometry-scalable physically-based SPICE compact model for SiC MPS diodes including the snapback mechanism. *Solid State Phenomena*, 360:67–74, 2024.
- [7] V. d’Alessandro, V. Terracciano, A. Borghese, M. Boccarossa, and A. Irace. A simple electrothermal compact model for SiC MPS diodes including the snapback mechanism. In *Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Budapest, Hungary, September 2023.
- [8] A. Borghese, V. Terracciano, M. Boccarossa, A. Irace, and V. D’Alessandro. A geometry-scalable electrothermal compact circuit model of SiC merged-PiN-Schottky diodes accounting for the snapback mechanism: Application to current surge events. *Microelectronics Reliability*, 168, 2025.

-
- [9] Synopsys, Inc. *Sentaurus Device User Guide*, version r-2020.09 edition, September 2020.
 - [10] V. d'Alessandro, F. Di Napoli, P. Guerriero, and S. Daliento. A novel circuit model of PV cell for electrothermal simulations. In *Proc. IET Renewable Power Generation Conference (RPG)*, 2014.
 - [11] V. d'Alessandro, G. Sasso, N. Rinaldi, and K. Aufinger. Influence of scaling and emitter layout on the thermal behavior of toward-THz SiGe:C HBTs. *IEEE Transactions on Electron Devices*, 61(10):3386–3394, October 2014.
 - [12] Cadence Design Systems, Inc. *PSpice User's Manual*, orcad 16.5 edition, 2011.
 - [13] Analog Devices, Inc. Ltspice, 2023. Version 17.1.9.
 - [14] T. Hunger et al. Numerical and experimental study on surge current limitations of wire-bonded power diodes. In *Proc. PCIM Europe*, Nuremberg, Germany, 2007. Online.
 - [15] J.-H. Chen, Y. Wang, X.-X. Fei, M.-T. Bao, and F. Cao. Novel layout design of 4h-SiC merged PiN Schottky diodes leading to improved surge robustness. *Chinese Physics B*, 32(9), 2023.
 - [16] V. Terracciano, A. Borghese, C. Ceresa, V. d'Alessandro, and A. Irace. Optimal bonding of 4h-sic parallel diodes in a single TO-247 package for improved surge current robustness: experimental investigation. HAL preprint, 2025. Presented at ESREF 2025. Extended journal version accepted in *Microelectronics Reliability* (Elsevier), forthcoming.
 - [17] A. Borghese et al. Statistical analysis of the electrothermal imbalances of mismatched parallel SiC power MOSFETs. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(3):1527–1538, September 2019.
 - [18] JEDEC Solid State Technology Association. Section 3: Diodes and rectifiers. JEDEC Standard JESD77-B, 2000.
 - [19] A. Buttay et al. Surge current capability of ultra-wide-bandgap Ga₂O₃ Schottky diodes. *Microelectronics Reliability*, 114, November 2020.
 - [20] F.-J. Hsu, H.-T. Hung, and C.-T. Yen. Impact of layout arrangement on surge current and avalanche robustness of silicon carbide JBS diodes. In *Proc. IEEE Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, pages 314–317, China, May 2023.
 - [21] W. Zhong et al. Electro-thermal analysis of 1.2kv–100a SiC JBS diodes under surge current stress. In *Proc. SSLChina IFWS*, pages 22–25, Shenzhen, China, November 2019.
-

-
- [22] B. Zhang et al. The surge current failure and thermal analysis of 4h-SiC Schottky barrier diode. *IEEE Transactions on Electron Devices*, 71(6):3805–3810, June 2024.
 - [23] B. J. Baliga. *Advanced Power MOSFET Concepts*. Springer, Boston, MA, USA, 2010.
 - [24] G. Romano et al. A comprehensive study of short-circuit ruggedness of silicon carbide power MOSFETs. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4:978–987, 2016.
 - [25] M. Noborio, Y. Kanzaki, J. Suda, and T. Kimoto. Experimental and theoretical investigations on short-channel effects in 4h-SiC MOSFETs. *IEEE Transactions on Electron Devices*, 52:1954–1962, 2005.
 - [26] Y. Zhang, F. Udrea, and H. Wang. Multidimensional device architectures for efficient power electronics. *Nature Electronics*, 5:723–734, 2022.
 - [27] F. Udrea et al. The finfet effect in silicon carbide mosfets. In *Proc. 33rd Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, pages 75–78, Nagoya, Japan, 2021.
 - [28] T. Fujihira. Theory of semiconductor superjunction devices. *Japanese Journal of Applied Physics*, 36:6254, 1997.
 - [29] W. Saito. Comparison of theoretical limits between superjunction and field plate structures. In *Proc. 25th Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, pages 241–244, Kanazawa, Japan, 2013.
 - [30] H. Kang and F. Udrea. True material limit of power devices—applied to 2-d superjunction mosfet. *IEEE Transactions on Electron Devices*, 65:1432–1439, 2018.
 - [31] M. Boccarossa, K. Melnyk, A. B. Renz, P. M. Gammon, V. Kotagama, V. A. Shah, L. Maresca, A. Irace, and M. Antoniou. A 3.3 kv SiC semi-superjunction MOSFET with trench sidewall implantations. *Micromachines*, 16(2), 2025.
 - [32] D. Yang, S. Wirths, L. Knoll, Y. Han, D. M. Buca, and Q. T. Zhao. Enhanced device performance with vertical SiC gate-all-around nanowire power MOSFETs. In *Key Engineering Materials*, volume 945, pages 77–82, 2023.
 - [33] L. Maresca, V. Terracciano, A. Borghese, M. Boccarossa, M. Riccio, G. Breglio, A. Mihaila, G. Romano, S. Wirths, L. Knoll, and A. Irace. Sic GAA mosfet concept for high power electronics performance evaluation through advanced TCAD simulations. *Solid State Phenomena*, 360:75–80, 2024.
-

-
- [34] L. Maresca, V. Terracciano, A. Borghese, M. Boccarossa, M. Riccio, G. Breglio, S. Wirths, and A. Irace. Evaluation of switching performances and short-circuit capability of a 1.2 kv SiC GAA MOSFET through TCAD simulations. In *Key Engineering Materials*, volume 1021, pages 17–23, September 2025.
 - [35] V. Terracciano, A. Borghese, M. Boccarossa, A. Irace, G. A. Salvatore, and L. Maresca. Electrothermal performance enhancement of silicon carbide gate-all-around MOSFETs using a ferroelectric gate stack. In *Proceedings of the 31st International Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2025)*, Naples, Italy, September 2025. IEEE.
 - [36] N. S. Mohammad. Understanding quantum confinement in nanowires: basics, applications and possible laws. *Journal of Physics: Condensed Matter*, 26, 2014.
 - [37] M. Boccarossa, L. Maresca, A. Borghese, M. Riccio, G. Breglio, A. Irace, and G. A. Salvatore. The Ferro-Power MOSFET: Enhancing short-circuit robustness in power switches with a ferroelectric gate stack. *IEEE Access*, 13:59264–59274, 2025.
 - [38] A. Pérez-Tomás et al. Field-effect mobility temperature modeling of 4h-SiC metal-oxide-semiconductor transistors. *Journal of Applied Physics*, 100(11), December 2006.
 - [39] Q. Huang et al. High-breakdown and low-leakage 4h-SiC MOS capacitor based on HfO₂/SiO₂ stacked gate dielectric in trench structures. *Nanomaterials*, 15(5), February 2025.
 - [40] C.-H. Jang, H.-S. Kim, H. Kim, and H.-Y. Cha. Temperature- and frequency-dependent ferroelectric characteristics of metal-ferroelectric-metal capacitors with atomic-layer-deposited undoped HfO₂ films. *Materials*, 15(6), March 2022.
 - [41] Z. Chen, L. Song, H. Zhao, Y. Zhang, and W. Cao. Temperature- and electric field-dependence of polarization hysteresis for a [001]_c-poled PMN-PT single crystal. *Journal of the Asian Ceramic Society*, 10(1):203–214, January 2022.
 - [42] J. Suchanicz et al. Lead-free (Na_{0.5}Bi_{0.5})_{1-x}Ba_xTiO₃ single crystals ($0 \leq x \leq 0.05$) and their dielectric and pyroelectric properties. *Integrated Ferroelectrics*, 108(1):98–105, October 2009.
 - [43] M. Hoffmann, U. Schroeder, C. Künneth, A. Kersch, S. Starschich, U. Böttger, and T. Mikolajick. Ferroelectric phase transitions in nanoscale HfO₂ films enable giant pyroelectric energy conversion and highly efficient supercapacitors. *Nano Energy*, 18:154–164, November 2015.
-

- [44] F. Richardeau, A. Borghese, A. Castellazzi, A. Irace, V. Chazal, and G. Guibaud. Effect of gate–source bias voltage and gate–drain leakage current on the short–circuit performance of FTO–type SiC power MOSFETs. In *Proc. 33rd Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, pages 255–258, Nagoya, Japan, May 2021.
 - [45] G. Romano et al. Short–circuit failure mechanism of SiC power MOSFETs. In *Proc. IEEE 27th Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, pages 345–348, Hong Kong, China, May 2015.
 - [46] F. Boige, A. Fayyaz, A. Castellazzi, F. Richardeau, and S. Vinnac. Short–circuit robustness of parallel SiC MOSFETs and fail–safe mode strategy. In *Proc. 21st European Conf. on Power Electronics and Applications (EPE '19 ECCE Europe)*, pages P.1–P.10, Genoa, Italy, September 2019.
 - [47] J. Kim and W. Sung. Improved short–circuit ruggedness for 1.2–kv 4h–SiC MOSFET using a deep P–well implemented by channeling implantation. *IEEE Electron Device Letters*, 42(12):1822–1825, December 2021.
 - [48] Y. Xing et al. 1200–v SiC MOSFET short–circuit ruggedness evaluation and methods to improve withstand time. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(5):5059–5069, October 2022.
 - [49] P. D. Lomenzo et al. Universal Curie constant and pyroelectricity in doped ferroelectric HfO₂ thin films. *Nano Energy*, 70, August 2020.
 - [50] T. Nishimura, L. Xu, S. Shibayama, T. Yajima, S. Migita, and A. Toriumi. Ferroelectricity of nondoped thin HfO₂ films in TiN/HfO₂/TiN stacks. *Japanese Journal of Applied Physics*, 55(S2), August 2016.
 - [51] A. Pal, V. K. Narasimhan, S. Weeks, K. Littau, D. Pramanik, and T. Chiang. Enhancing ferroelectricity in dopant–free hafnium oxide. *Applied Physics Letters*, 110(2), January 2017.
 - [52] J. H. Choi, Y. Mao, and J. P. Chang. Development of hafnium–based high–k materials—a review. *Materials Science and Engineering: R: Reports*, 72(6):97–136, 2011.
 - [53] A. K. Tagantsev et al. Ferroelectric materials for microwave tunable applications. *Journal of Electroceramics*, 11:5–66, 2003.
 - [54] M. Boccarossa, L. Maresca, A. Borghese, M. Riccio, G. Breglio, A. Irace, and G. A. Salvatore. Non–linear gate–stack effect on the short–circuit performance of a 1.2–kv SiC MOSFET. *Solid State Phenomena*, 360:59–65, 2024. Presented at the 35th Int. Symp. on Power Semiconductor Devices & ICs (ISPSD 2023), Hong Kong.
-

- [55] M. Boccarossa, L. Maresca, A. Borghese, M. Riccio, G. Breglio, A. Irace, and G. A. Salvatore. Threshold voltage temperature dependence for a 1.2-kv SiC MOSFET with non-linear gate stack. In *Proc. 17th Int. Seminar on Power Semiconductors (ISPS)*, pages 51–54, Prague, Czech Republic, January 2023.
-

Author's publications

1. V. Terracciano, A. Borghese, M. Boccarossa, V. d'Alessandro, and A. Irace. A geometry-scalable physically-based SPICE compact model for SiC MPS diodes including the snapback mechanism. *Solid State Phenomena*, 360:67–74, 2024. DOI: 10.4028/p-b9ImzL.
2. V. d'Alessandro, V. Terracciano, A. Borghese, M. Boccarossa, and A. Irace. A simple electrothermal compact model for SiC MPS diodes including the snapback mechanism. In *Proc. Int. Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Budapest, Hungary, Sep. 2023. DOI: 10.1109/THERMINIC60375.2023.10325871.
3. A. Borghese, V. Terracciano, M. Boccarossa, A. Irace, and V. d'Alessandro. A geometry-scalable electrothermal compact circuit model of SiC merged-PiN-Schottky diodes accounting for the snapback mechanism: application to current surge events. *Microelectronics Reliability*, 168:115668, 2025. DOI: 10.1016/j.microrel.2025.115668.
4. V. Terracciano, A. Borghese, C. Ceresa, V. d'Alessandro, and A. Irace. Optimal bonding of 4H-SiC parallel diodes in a single TO-247 package for improved surge current robustness: experimental investigation. HAL preprint, 2025. (Presented at ESREF 2025.) *Extended journal version accepted in Microelectronics Reliability (Elsevier), forthcoming.*
5. L. Maresca, V. Terracciano, A. Borghese, M. Boccarossa, M. Riccio, G. Breglio, A. Mihaila, G. Romano, S. Wirths, L. Knoll, and A. Irace. SiC GAA MOSFET concept for high power electronics performance evaluation through advanced TCAD simulations. *Solid State Phenomena*, 360:75–80, 2024. DOI: 10.4028/p-lhRi4M.

6. V. Terracciano, A. Borghese, M. Boccarossa, A. Irace, G. A. Salvatore, and L. Maresca. Electrothermal performance enhancement of silicon carbide gate-all-around MOSFETs using a ferroelectric gate stack. In *Proc. 31st Int. Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2025)*, Naples, Italy, Sep. 2025. DOI: 10.1109/THERMINIC65879.2025.
 7. C. Scognamillo, A. Borghese, K. Melnyk, I. Nistor, V. d'Alessandro, M. Boccarossa, V. Terracciano, M. Riccio, A. P. Catalano, G. Breglio, N. Lophitis, M. Antoniou, M. Rahimo, A. Irace, and L. Maresca. Out-of-SOA performance of 3.3 kV SiC MOSFETs: comparison between planar and quasi-planar trench. In *Proc. SIE 2024, Lecture Notes in Electrical Engineering*, vol. 1263, pp. 369–374. Springer, Cham, 2025. DOI: 10.1007/978-3-031-71518-1_44.
 8. A. Borghese, M. Boccarossa, V. Terracciano, L. Maresca, M. Riccio, and A. Irace. Effect of the load inductor on the avalanche ruggedness of 1200-volt silicon diodes during unclamped inductive switching. HAL preprint, 2025. (Presented at ESREF 2025.) *Extended journal version accepted in Microelectronics Reliability (Elsevier), forthcoming.*
-